DATE: July 15, 2004

# Beko

## SERVICE MANUAL

107cm (42 Inch) Wide Plasma Display Module

## MODEL : 42” S3.1 PDP

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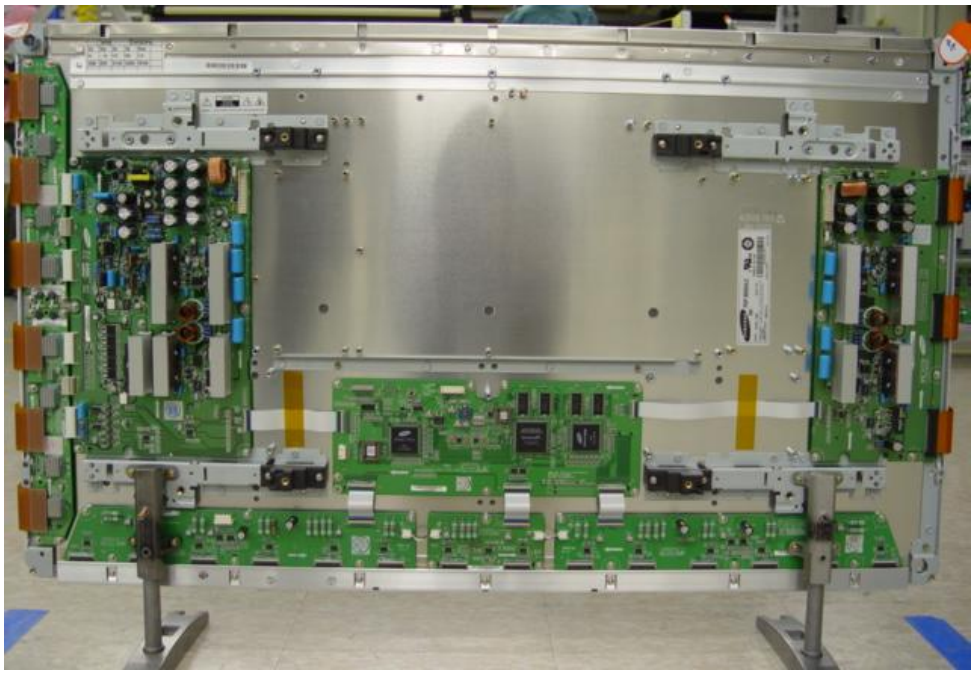
# 1. Overview

## 1-1 Model Name of Plasma Display

**MODEL : 42” S3.1 PDP (S42SD-YD05)**

## 1-2 External View



【 M1 = X Board + Y Board + Logic Board 】

**1-3 Specifications**

| No | Item | Specification | |
|---|---|---|---|
| 1 | Pixel | 852 (H) × 480 (V) pixels (1 pixel = 1 R,G,B cells) | |
| 2 | Number of Cells | 2556 (H) × 480 (V) | |
| 3 | Pixel Pitch | 1.095 (H) ㎜ × 1.110 (V) ㎜ | |
| 4 | Cell Pitch | R | 0.365 (H) ㎜ × 1.110 (V) ㎜ |
| | | G | 0.365 (H) ㎜ × 1.110 (V) ㎜ |
| | | B | 0.365 (H) ㎜ × 1.110 (V) ㎜ |
| 5 | Display size | 932.940 (H) ㎜ × 532.800(V) ㎜<br>[ 36.73 inch × 20.98 inch ] | |
| 6 | Screen size | Diagonal 42" Color Plasma Display Module | |
| 7 | Screen aspect | 16 : 9 | |
| 8 | Display color | 16.77 million colors | |
| 9 | Viewing angle | Over 160°<br>(Angle with 50% and greater brightness perpendicular to PDP module) | |
| 10 | Dimensions | 982 (W) × 582 (H) × 52.9 (D) ㎜ | |
| 11 | Weight | Module 1 | About 16.6 kg |
| 12 | Packing weight | Module 1 | 240kg ± 5kg (including modules) / 10pcs/BOX |
| 13 | Packing size | L 1175 * W 1140 * H 970 (mm) / 10pcs/BOX | |
| 14 | Broadcasting reception<br>Vertical frequency<br>and<br>Video/Logic Interface | PL42SD003C | 60Hz/ 50Hz, LVDS |
| | | | |
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| | | | |

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## 2. PRECAUTIONS

**** To prevent the risks of unit damage, electrical shock and radiation, take the following safety, service, and ESD precautions.**

### 2-1 Handling Precautions for Plasma Display

- PDP module use high voltage that is dangerous to human. Before operating PDP, always check the dust to prevent circuit short. Be careful touching the circuit device when power is on.
- PDP module is sensitive to dust and humidity. Therefore, assembling and disassembling must be done in no dust place.
- PDP module has a lot of electric devices. Service engineer must wear equipment(for example , earth ring) to prevent electric shock and working clothes to prevent electrostatic.
- PDP module use a fine pitch connector which is only working by exactly connecting with flat cable. Operator must pay attention to a complete connection when connector is reconnected after repairing.
- The capacitor's remaining voltage in the PDP module's circuit board temporarily remains after power is off. Operator must wait for discharging of remaining voltage during at least 1 minute.

### 2-2 Safety Precautions for Service (Handling, prevention of a electrical shock, measure against power outage, etc)

**( Safety Precautions )**

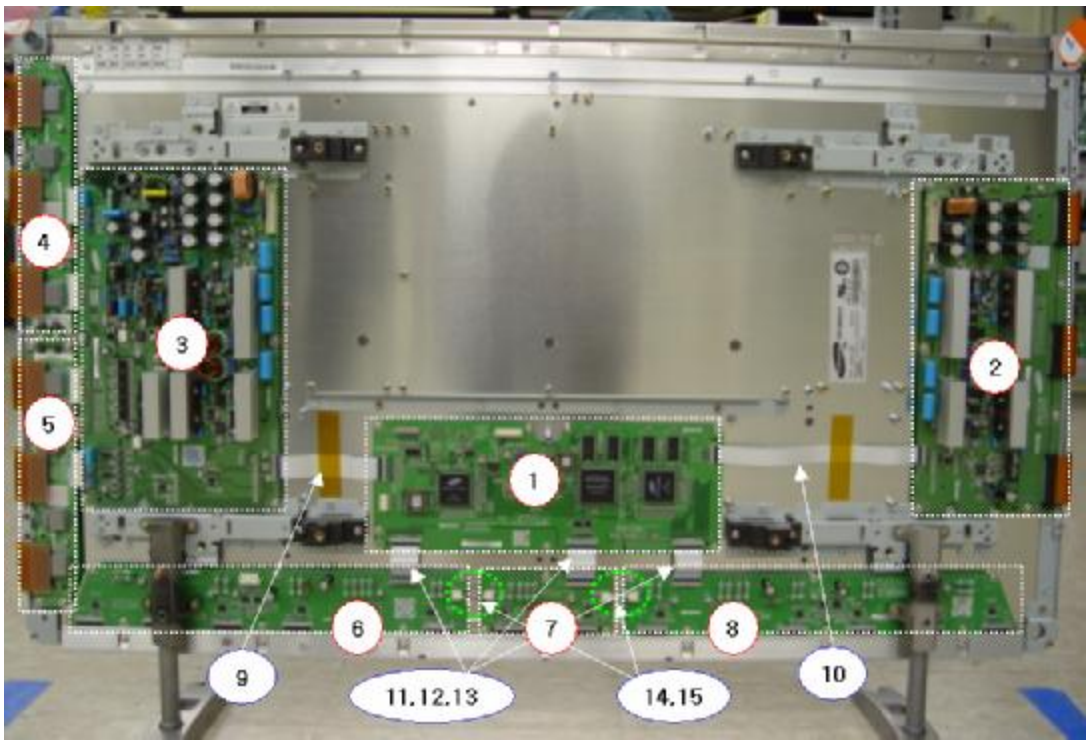
- Before replacing a board, discharge forcibly The remaining electricity from board.
- When connecting FFC and TCPs to the module, recheck that they are perfectly connected.
- To prevent electrical shock, be careful not to touch leads during circuit operations.
- To prevent the Logic circuit from being damaged due to wrong working, do not connect/disconnect signal cables during circuit operations.
- Do thoroughly adjustment of a voltage label and voltage-insulation.
- Before reinstalling the chassis and the chassis assembly, be sure to use all protective stuffs including a nonmetal controlling handle and the covering of partitioning type.
- Caution for design change : Do not install any additional devices to the module, and do not change the electrical circuit design.
- For example: Do not insert a subsidiary audio or video connector. If you insert It, It cause danger on safety. And, If you change the design or insert, Manufactor guarantee will be not effect. .
- If any parts of wire is overheats of damaged, replace it with a new specified one immediately, and identify the cause of the problem and remove the possible dangerous factors.
- Examine carefully the cable status if it is twisted or damaged or displaced. Do not change the space between parts and circuit board. Check the cord of AC power preparing damage.
- Product Safety Mark : Some of electric or implement material have special characteristics invisible that was related on safety. In case of the parts are changed with new one, even though the Voltage and Watt is higher than before, the Safety and Protection function will be lost.
- The AC power always should be turned off, before next repair..
- Check assembly condition of screw, parts and wire arrangement after repairing. Check whether the material around the parts get damaged.

**( Precaution when repairing ESD )**

- There is ESD which is easily damaged by electrostatics.(for example Integrated circuit, FET ) Electrostatic damage rate of product will be reduced by the following technics
- Before handling semiconductor parts/assembly, must remove positive electric by ground connection, or must wear the antistatic wrist-belt and ring. ( It must be operated after removing dust on it – It comes under precaution of electric shock.)
- After removing ESD assembly, put on it with aluminum stuff on the conductive surface to prevent charging.
- Do not use chemical stuff using Freon. It generates positive electric that can damage ESD.
- Must use a soldering device for ground-tip when soldering or de-soldering ESD.
- Must use anti-static solder removal device. Most removal device do not have antistatic which can charge a enough positive electric enough damaging ESD.
- Before removeing the protective material from the lead of a new ESD, bring the protective material into contact with the chassis or assembly that the ESD is to be installed on.
- When handing an unpacked ESD for replacement, do not move around too much. Moving (legs on the carpet, for example) generates enough electrostatic to damage the ESD.
- Do not take a new ESD from the protective case until the ESD is ready to be installed. Most ESD have a lead, which is easily short-circuited by conductive materials (such as conductive foam and aluminum)

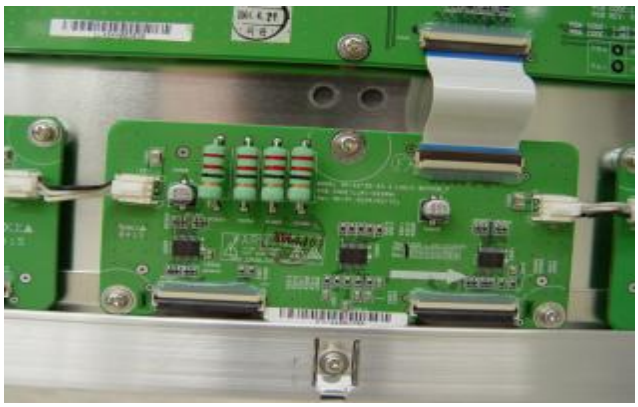
## 3.NAME & FUNCTION

### 3-1 Layout of Assemblies



| No. | Code No. | Location | 品名 |
|---|---|---|---|
| 1 | LJ92-00975A | Logic Main | ASSY PCB LOGIC MAIN |
| 2 | LJ92-00943A | X-Main | ASSY PCB X MAIN |
| 3 | LJ92-00944B | Y-Main | ASSY PCB Y MAIN |
| 6 | LJ92-00811A | Logic E Buffer | ASSY PCB BUFFER |
| 7 | LJ92-00812A | Logic F Buffer | ASSY PCB BUFFER |
| 8 | LJ92-00813A | Logic G Buffer | ASSY PCB BUFFER |
| 9 | LJ92-00796A | Y-Buffer (upper) | ASSY PCB BUFFER |
| 10 | LJ92-00797A | Y-Buffer (lower) | ASSY PCB BUFFER |
| 11 | 3809-001397 | Logic + Y-Main | FFC CABLE-FLAT |
| 12 | 3809-001396 | Logic + X-Main | FFC CABLE-FLAT |
| 13 | 3809-001414 | Logic + Logic Buf'(E) | FFC CABLE-FLAT |
| 14 | 3809-001414 | Logic + Logic Buf'(F) | FFC CABLE-FLAT |
| 15 | 3809-001414 | Logic + Logic Buf'(G) | FFC CABLE-FLAT |
| 16 | LJ39-00109A | Logic Buf'(E) + Logic Buf'(F) | LEAD CONNECTOR |
| 17 | LJ39-00109A | Logic Buf'(F) + Logic Buf'(G) | LEAD CONNECTOR |
| 18 | LJ39-00139A | SMPS + Video SMPS | LEAD CONNECTOR |
| 19 | LJ39-00140A | SMPS + Logic Buffer(E) | LEAD CONNECTOR |
| 20 | LJ39-00143A | SMPS + Logic Main | LEAD CONNECTOR |
| 21 | LJ39-00142A | SMPS + Y-Main | LEAD CONNECTOR |
| 22 | LJ39-00179A | SMPS + X-Main | LEAD CONNECTOR |

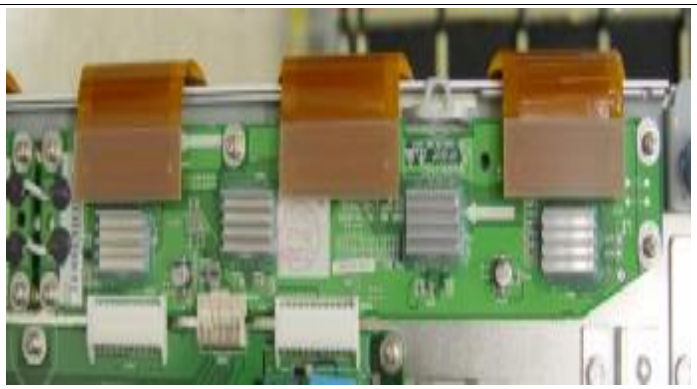
1. L-Main



7. F-Buffer

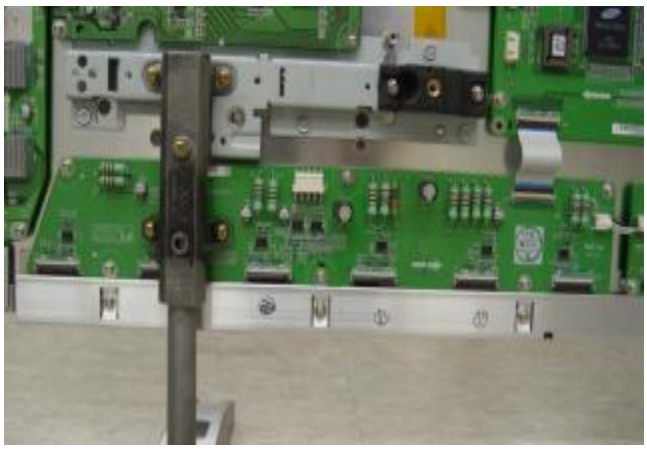
2. X-Main

3. Y-Main



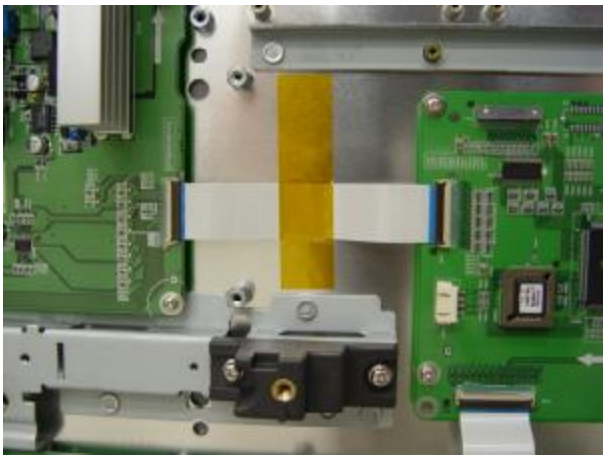
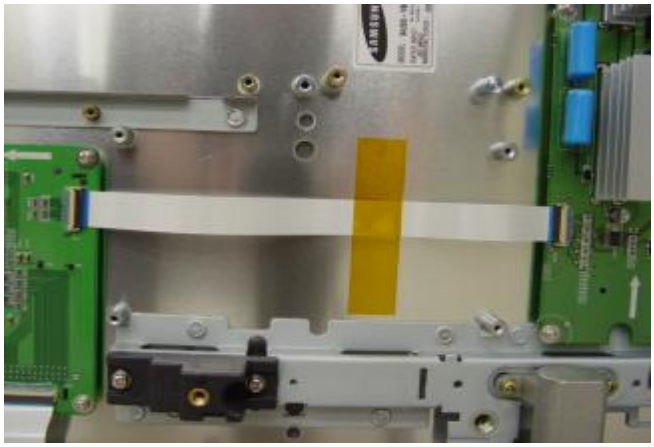
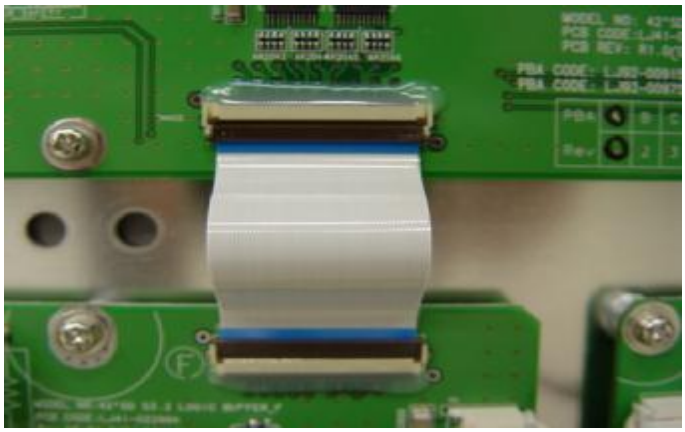
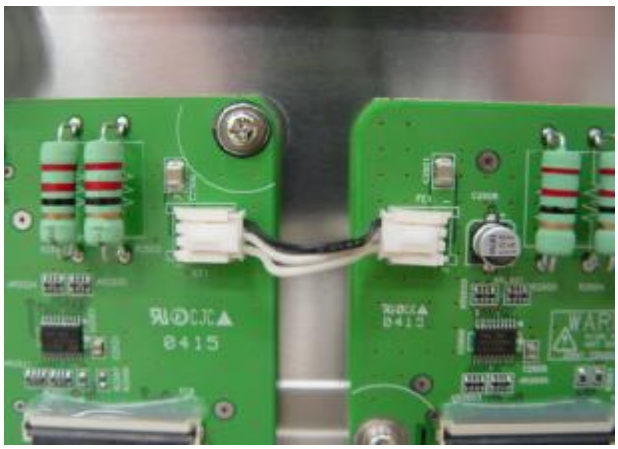
4, Y-Buffer (upper)

5. Y-Buffer (lower)



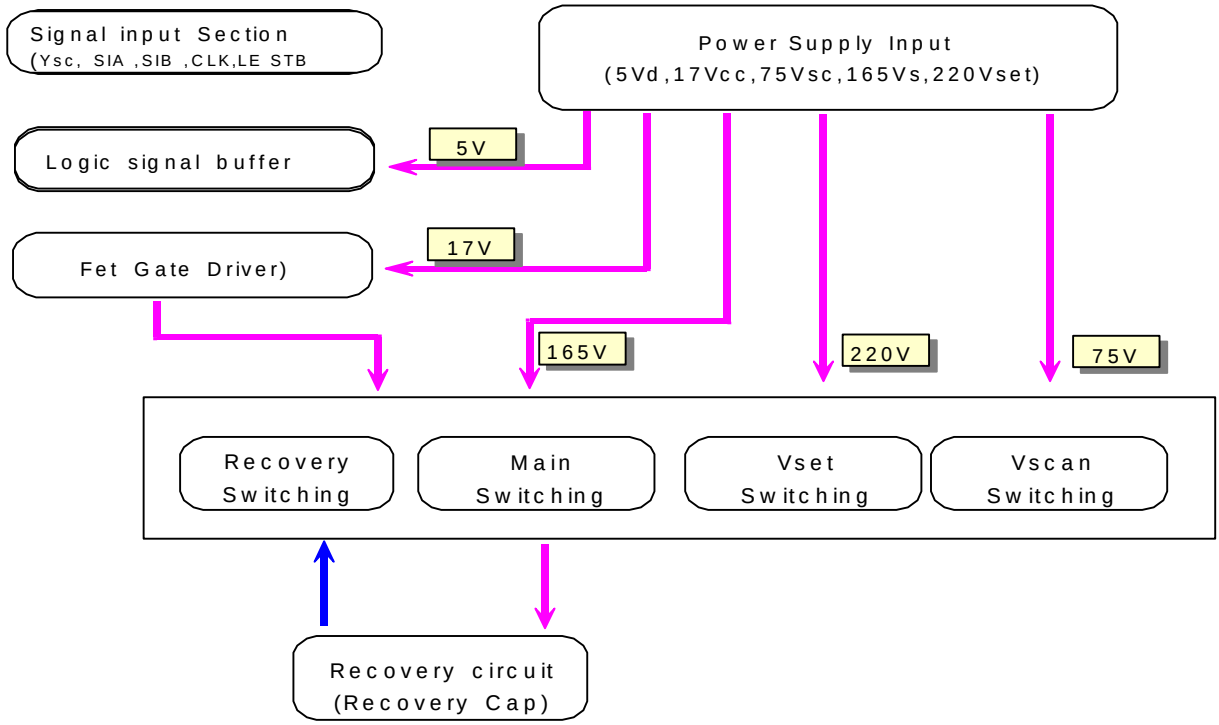
6. E-Buffer

8. G-Buffer

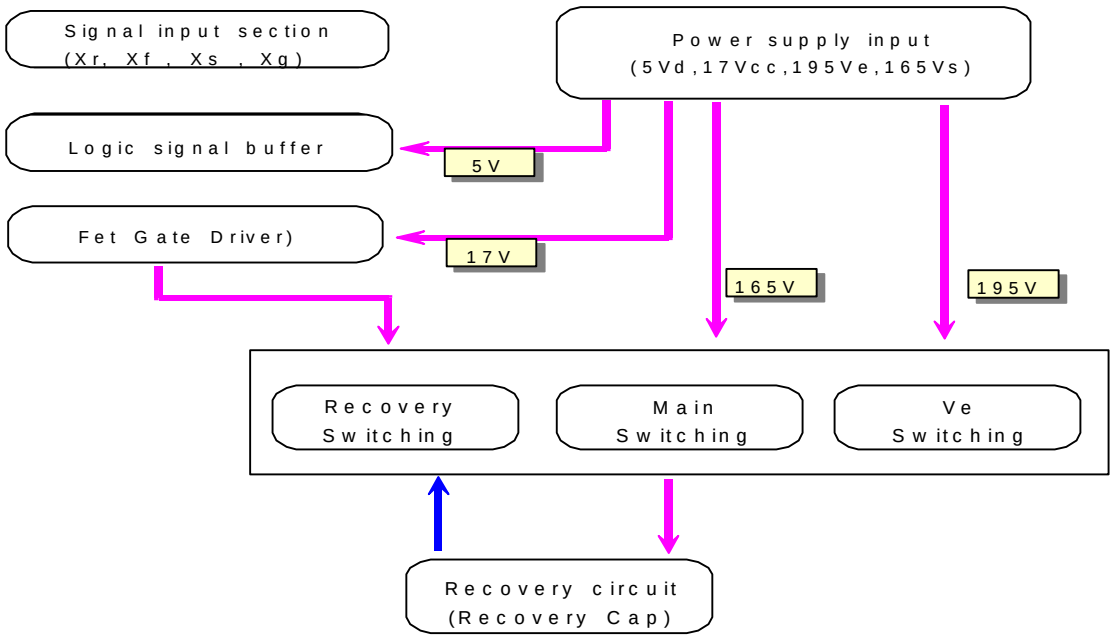
| | |
|---|---|
|  |  |
| 9. Logic + Y-Main | 10. Logic + X-Main |
|  |  |
| 11. 12. 13. Logic + Logic Buf'(E,F,G) | 14. 15. Logic Buffer |

**3-2 BLOCK DIAGRAM**

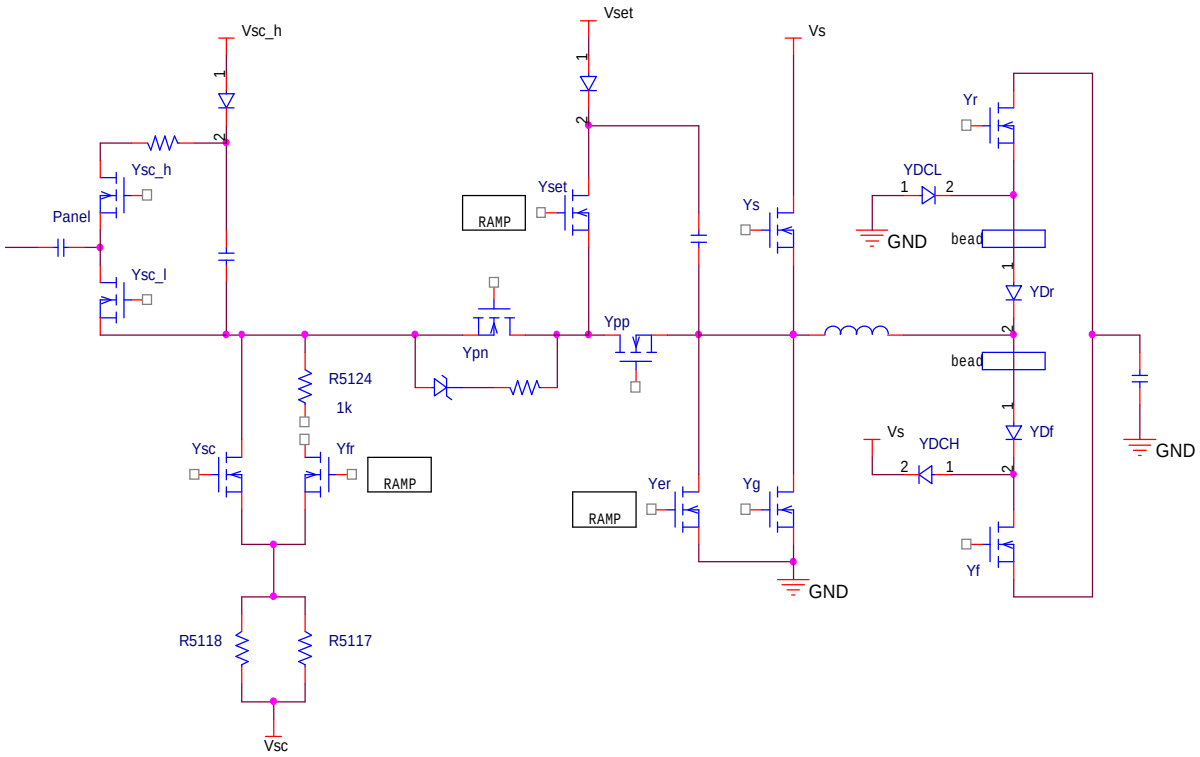
3-2-1 **BLOCK DIAGRAM FOR DRIVE CIRCUIT OPERATION**

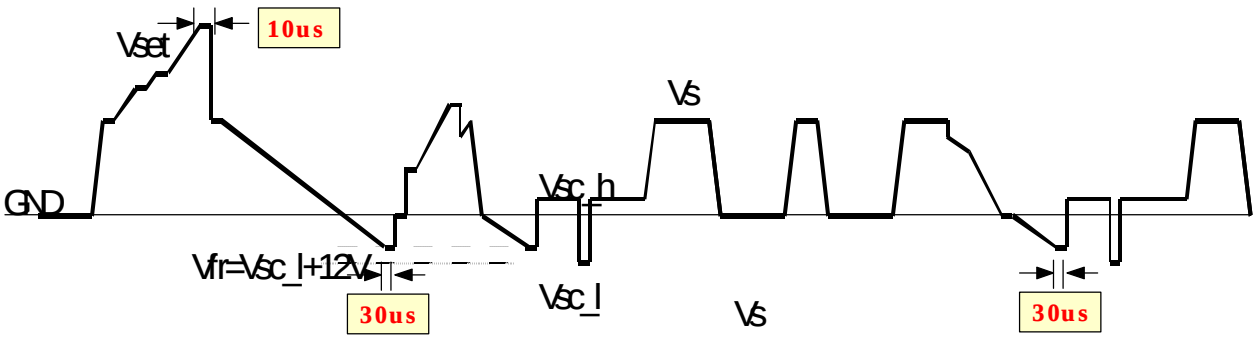



**< DRIVE Y Board >**



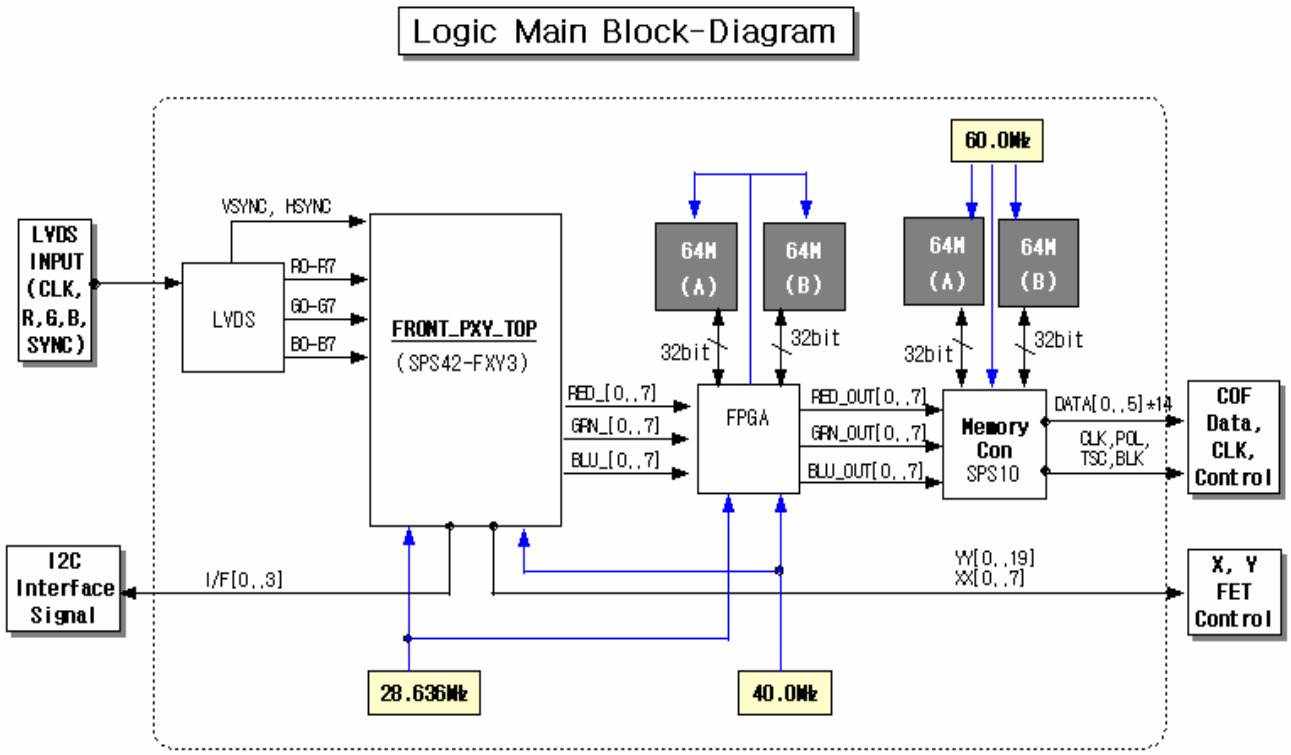

**< DRIVE X Board >**




**< Drive waveforms >**

3-2-2 Block Diagram for Logic circuit




### 3-3 Main function of Each Assembly

- X-main board : The X-main board generate a drive signal by switching the FET in synchronization with logic main board timing and supplies the X electrode of the panel with the drive signal through the connector.
  1) Maintain voltage waveforms (including ERC)
  2) Generate X rising ramp signal
  3) Maintain Ve bias between Scan intervals
- .Y-main board : The Y-main board generate a drive signal by switching the FET in synchronization with the logic Main Board timing and sequentially supplies the Y electrode of the panel with the drive signal through the scan driver IC on the Y-buffer board. This board connected to the panel's Y terminal has the following main functions.
  1) Maintain voltage waveforms (including ERC)
  2) Generate Y-rising Falling Ramp
  3) Maintain V scan bias
- Logic main board : The logic main board generates and outputs the address drive output signal and the X ,Y drive signal by processing the video signals. This Board buffers the address dirve output

signal and feeds it to the address drive IC (COF module)

(video signal- X Y drive signal generation , frame memory circuit / address data rearrangement)

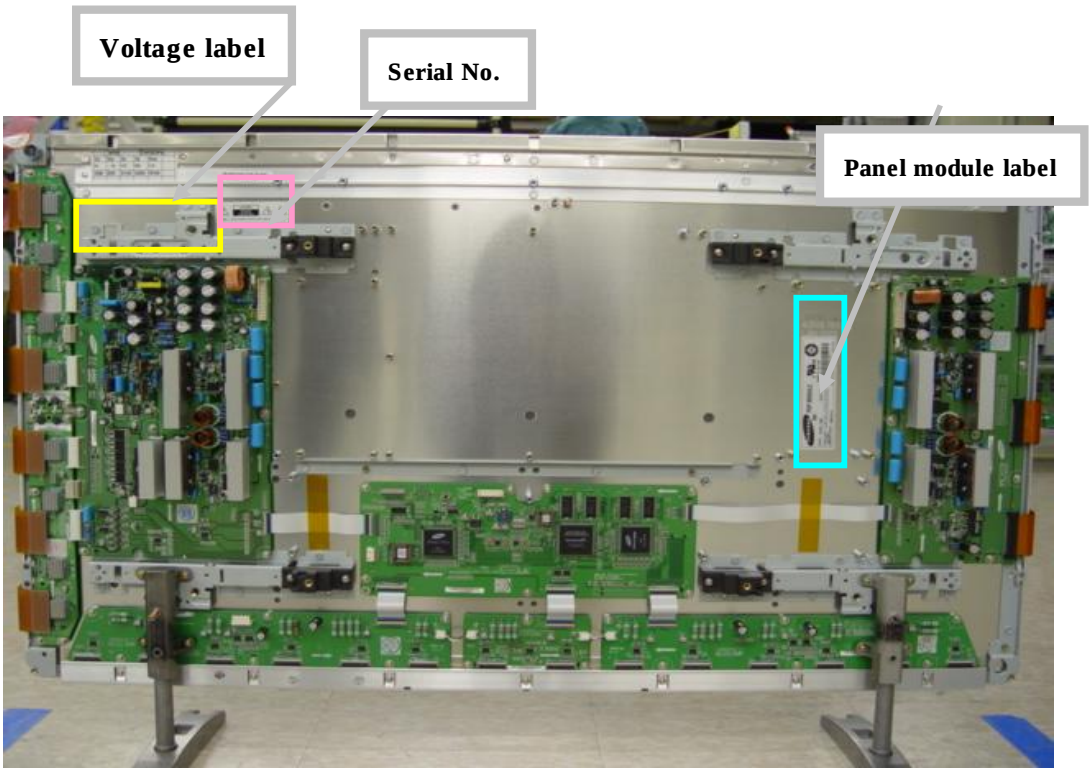
■.Logic buffer(E,F) : The logic buffer transmits data signal and control signal.

■.Y-buffer board (Upper, Lower) : The Y-buffer board consisting of the upper and lower boards supplies the Y-terminal with scan waveforms. The board comprises 8 scan driver IC's (ST microelectronics STV 7617 : 64 or 65 output pins) , but 4 ICs for the SD class

■.AC Noise Filter : The AC Noise filter has function for removing noise(low Frequency) and blocking surge. It effects Safety standards(EMC,EMI)

■.TCP( Tape Carrier Package ) : The TCP applies Va pulse to the address electrode and constitutes address discharge by the potential difference between the Va pulse and the pulse applied to the Y electrode. The TCP comprise 4 data driver Ics(STV7610A :96 pins output pins) 7 TCPs are required for signal scan .

### 3-4 PRODUCT/ SERIAL LABEL LOCATION




## 4. OPERATION CHECKING AFTER RECTIFICATION

### 4-1 Flow chart

* A/S Check Point *

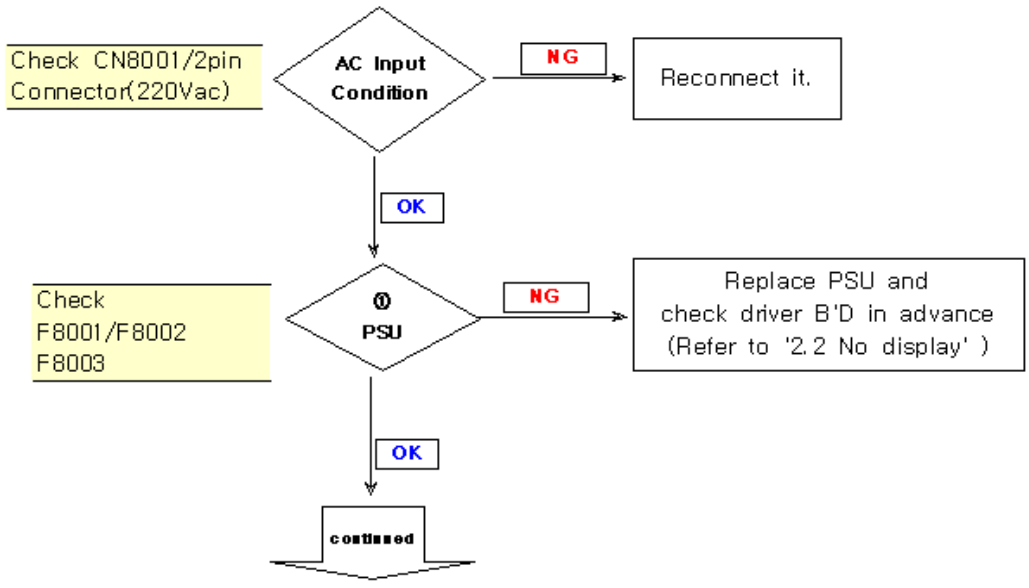
1.Checking the voltage for each assembly

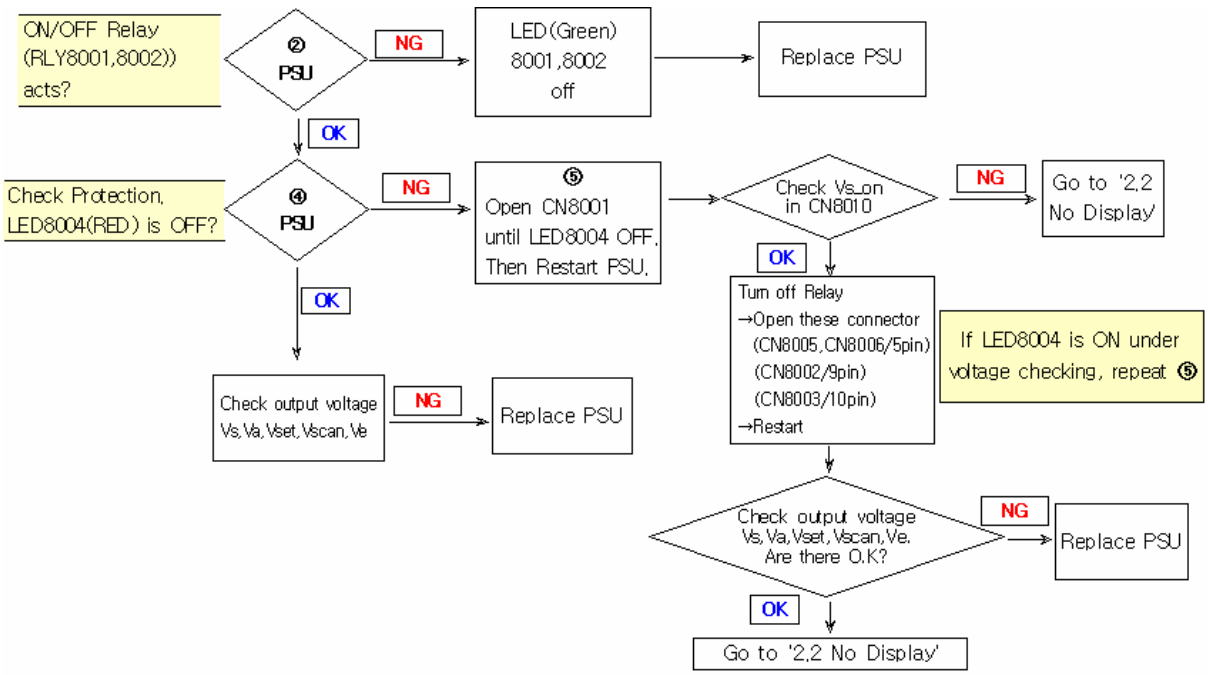
2. Judging the Logic board working or not

3. Adjusting the output signal through test points

4. Checking the panel's crack

### 4-1-1 No voltage output

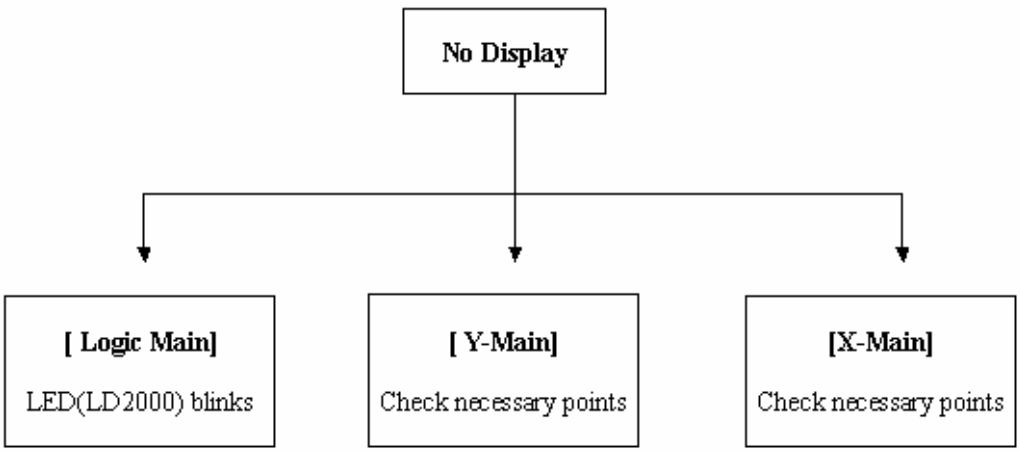


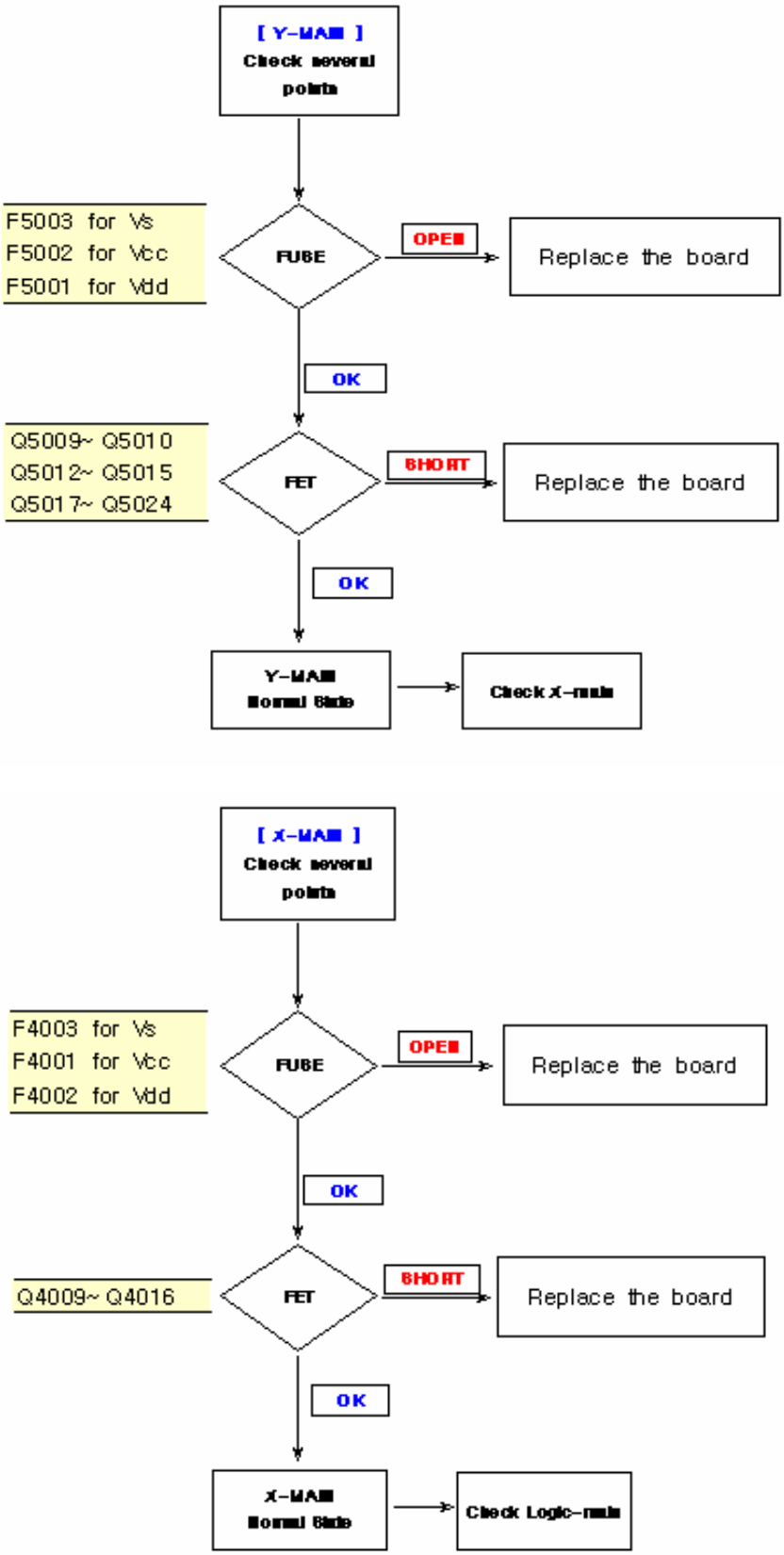


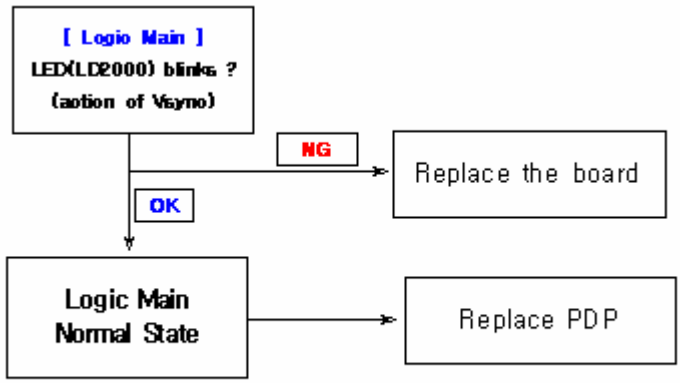

**4-1-2 NO display** (operating Voltage but an image doesn't exist on Screen)

⇒ No Display is related with Y-MAIN, X-MAIN, Logic Main and so on.

This page shows you how to check the boards, and the following pages show you how to find the defective board.



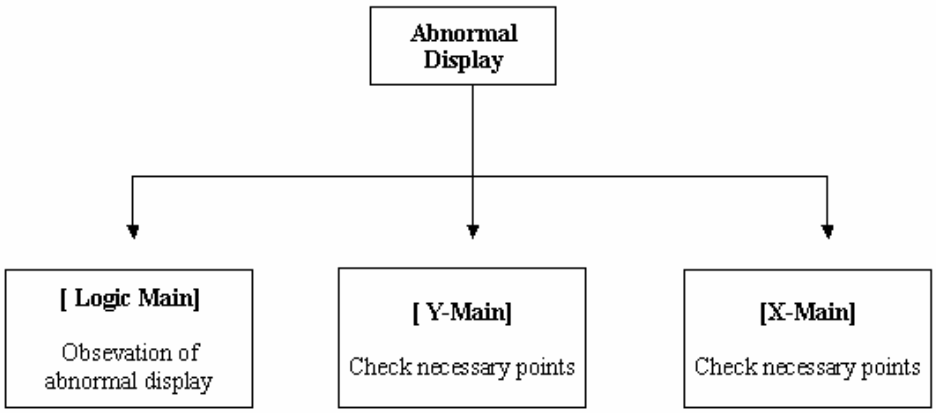

[ Y-MAIN ]
Check several points
F5003 for Vs
F5002 for Vcc
F5001 for Vdd
FUSE
OPEN
Replace the board
OK
Q5009~ Q5010
Q5012~ Q5015
Q5017~ Q5024
FET
SHORT
Replace the board
OK
Y-MAIN Normal State
Check X-main
[ X-MAIN ]
Check several points
F4003 for Vs
F4001 for Vcc
F4002 for Vdd
FUSE
OPEN
Replace the board
OK
Q4009~ Q4016
FET
SHORT
Replace the board
OK
X-MAIN Normal State
Check Logic-main

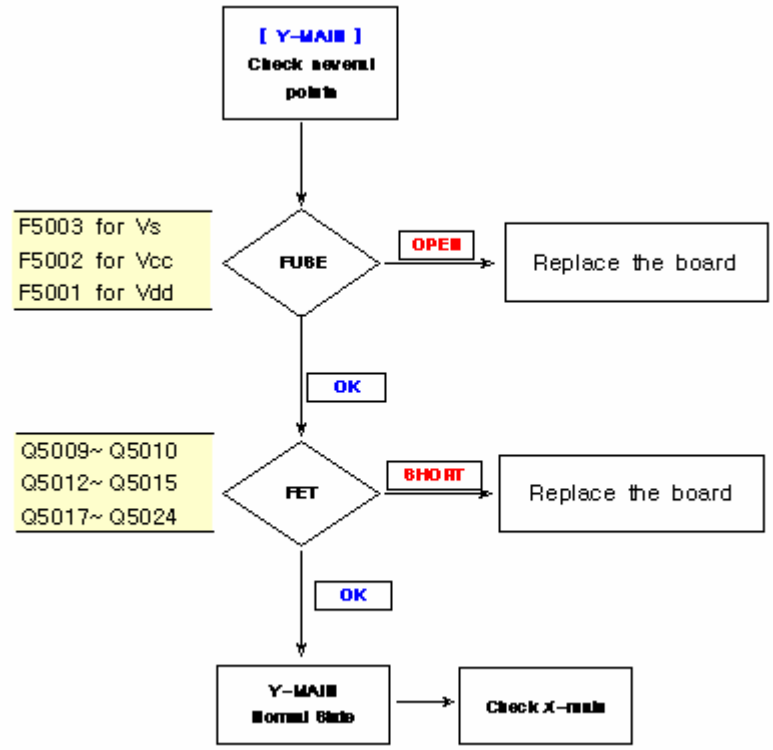


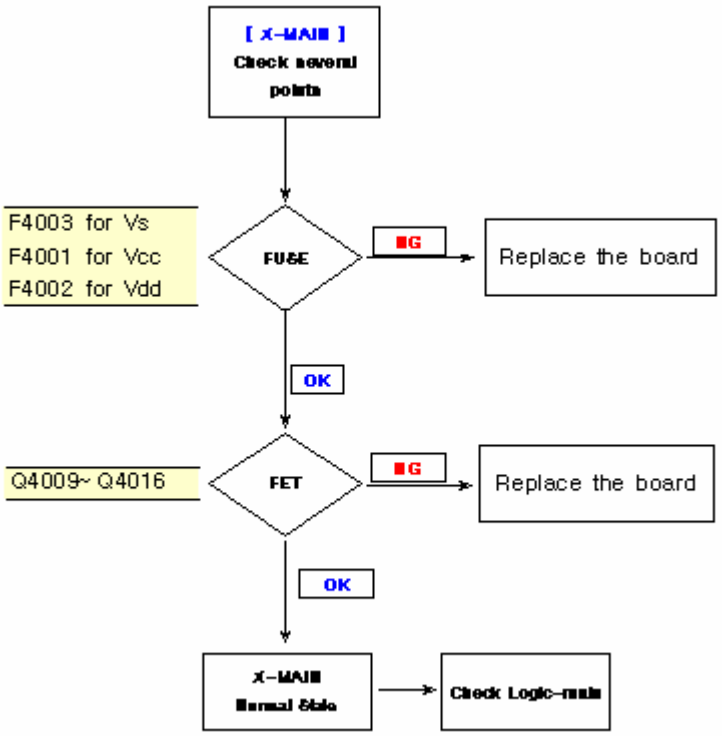

**4-1-3 Abnormal Display** (Abnormal Image is on Screen. (except abnormality in Sustain or Address)

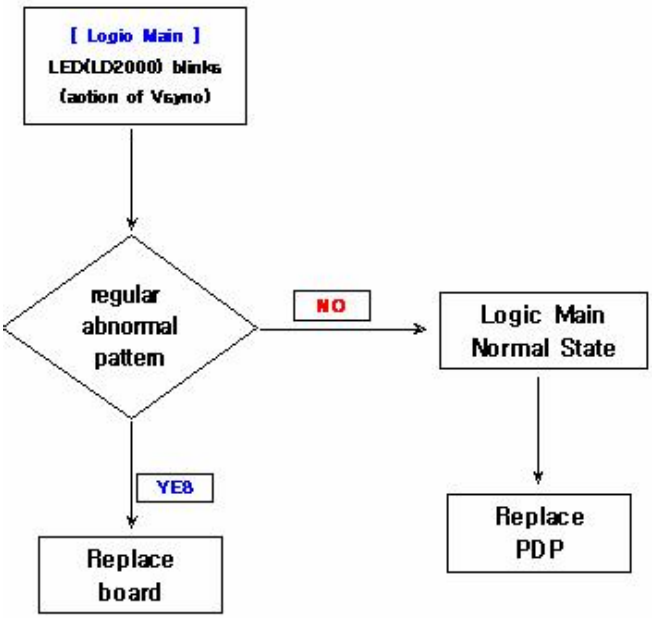
⇒ Abnormal Display is related with Y-MAIN, X-MAIN, Logic Main and so on.

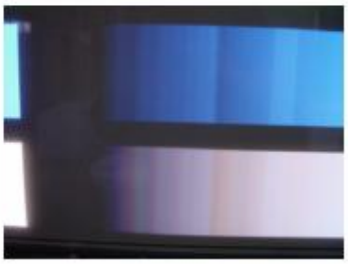
This page shows you how to check the boards, and the following pages show you how to find the defective board.



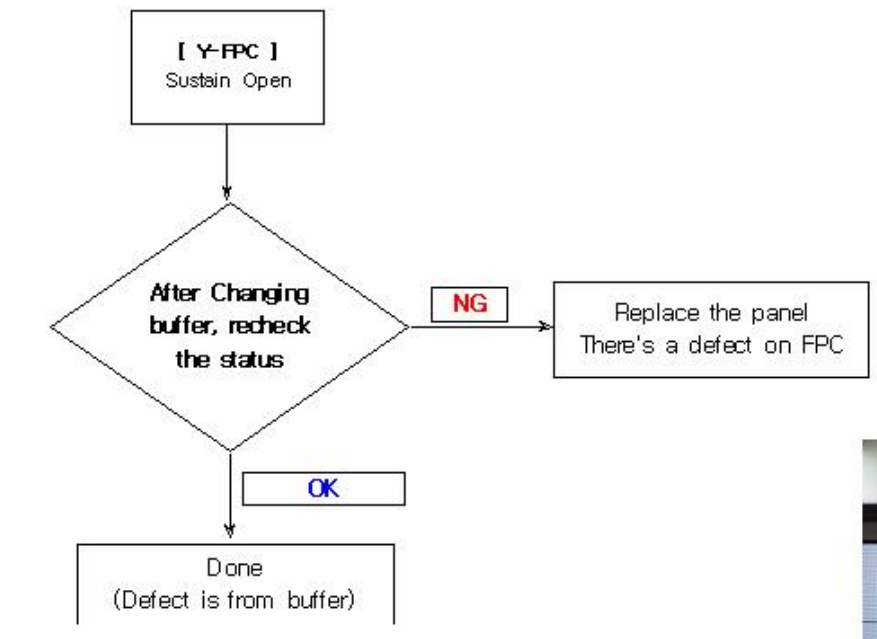

[ Y-MAIN ]
Check several points
F5003 for Vs
F5002 for Vcc
F5001 for Vdd
FUSE
OPEN
Replace the board
OK
Q5009~ Q5010
Q5012~ Q5015
Q5017~ Q5024
FET
SHORT
Replace the board
OK
Y-MAIN Normal State
Check X-main


[ X-MAIN ]
Check several points
F4003 for Vs
F4001 for Vcc
F4002 for Vdd
FUSE
NG
Replace the board
OK
Q4009~ Q4016
FET
NG
Replace the board
OK
X-MAIN Normal State
Check Logic-main

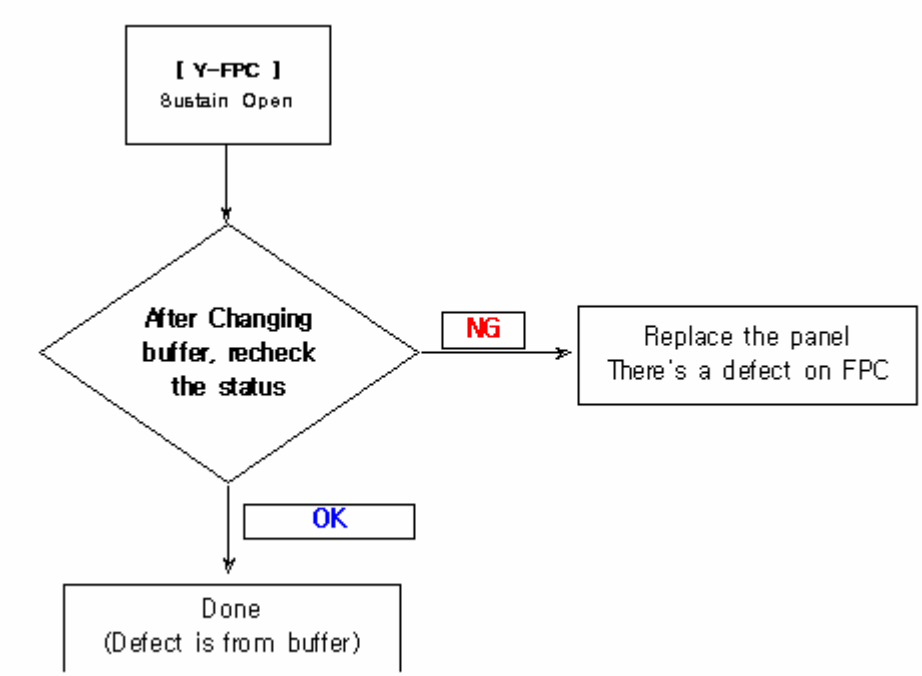


**4-1-4 Sustain Open** (some horizontal lines don't exist on screen)



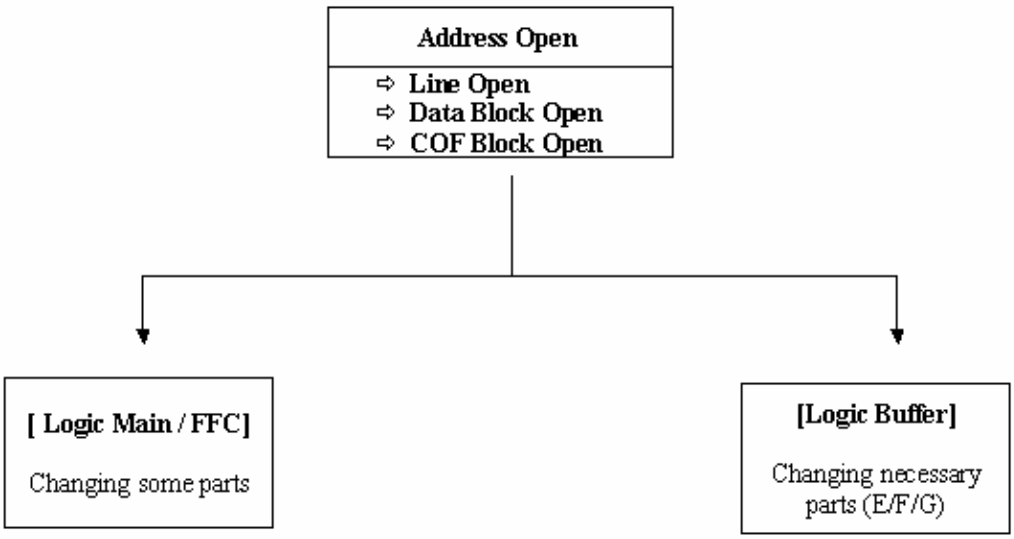

**4-1-5 Sustain Short (** some horizontal lines appear to be linked on Video )

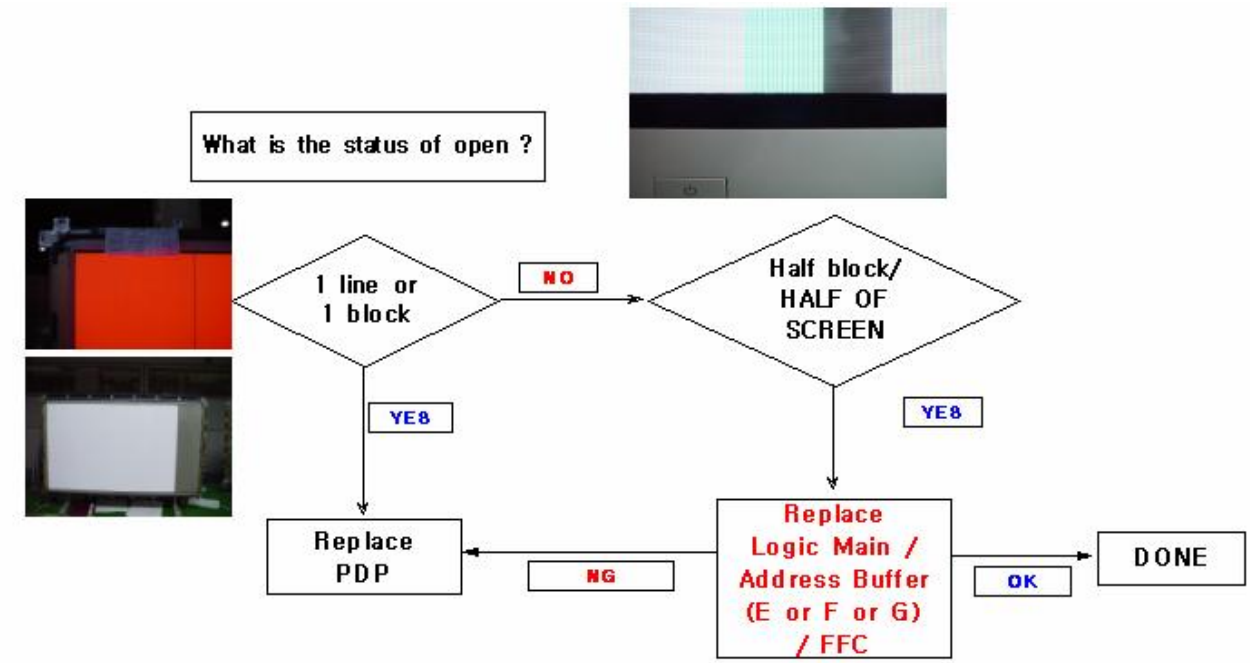



**4-1-6 Address Open (** some vertical lines don't exist on screen )

⇒ Address Open is related with Logic Main, Logic Buffer, FFC, TCP and so on.

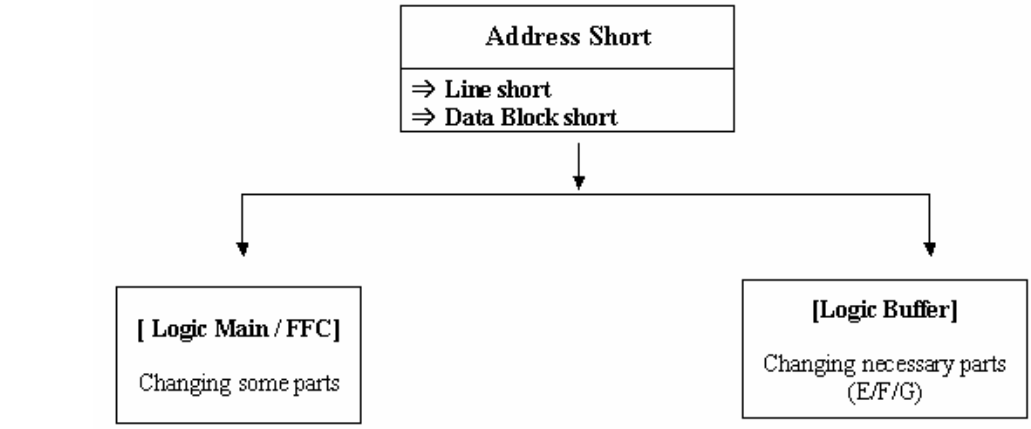
This page shows you how to check the boards, and the following pages show you how to find the defective board.

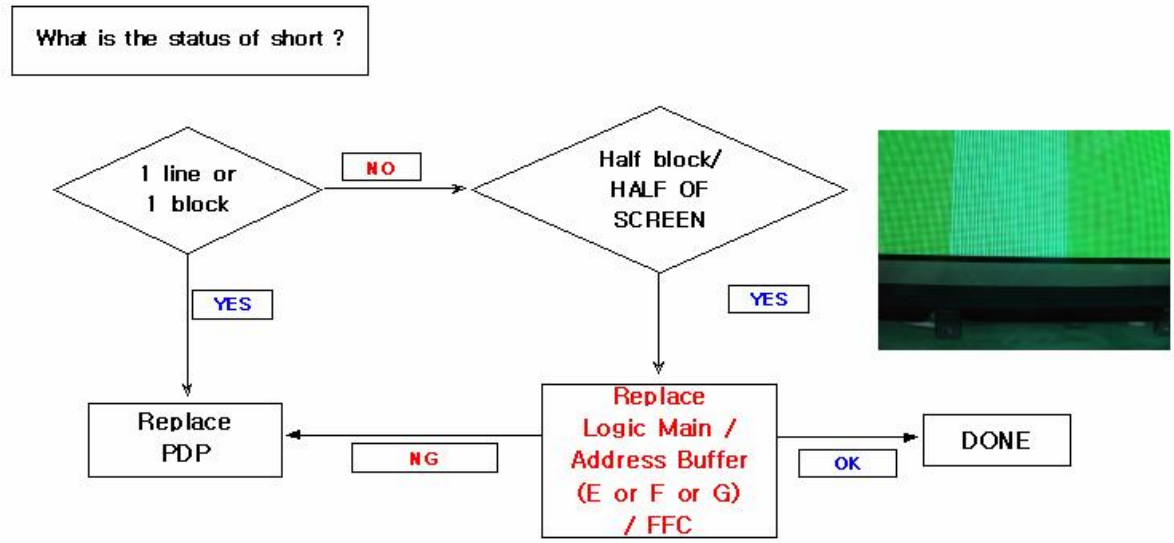



**4-1-7 Address Short** (some vertical lines appear to be linked on screen

⇒ Address Short is related with Logic Main, Logic Buffer, FFC, TCP and so on.
This page shows you how to check the boards, and the following pages show you how to find the defective board.

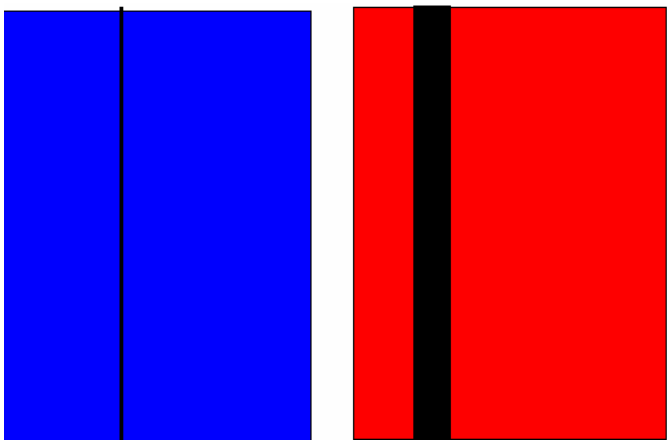
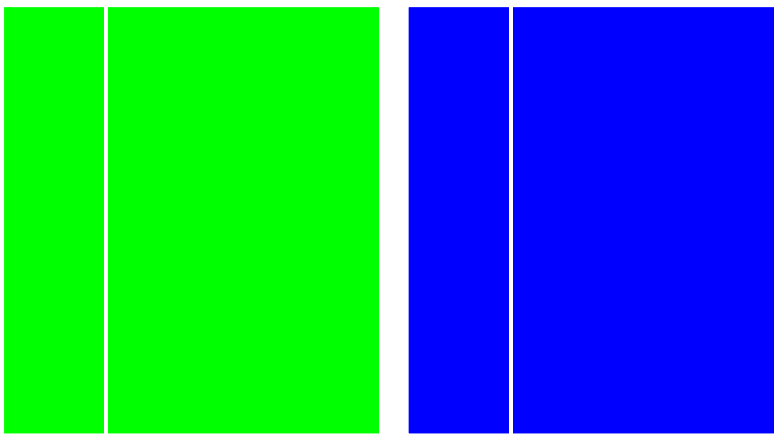


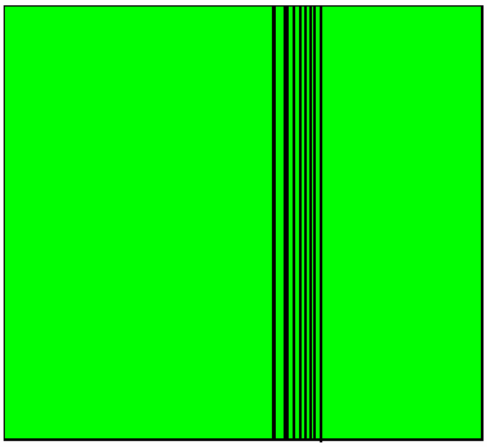
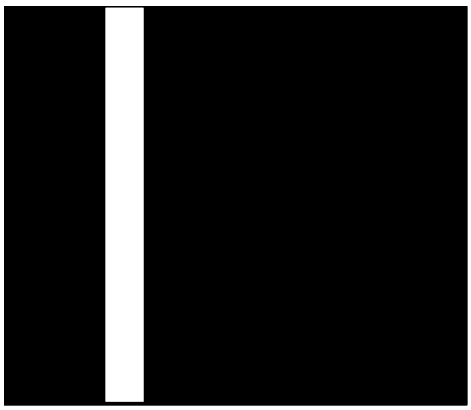
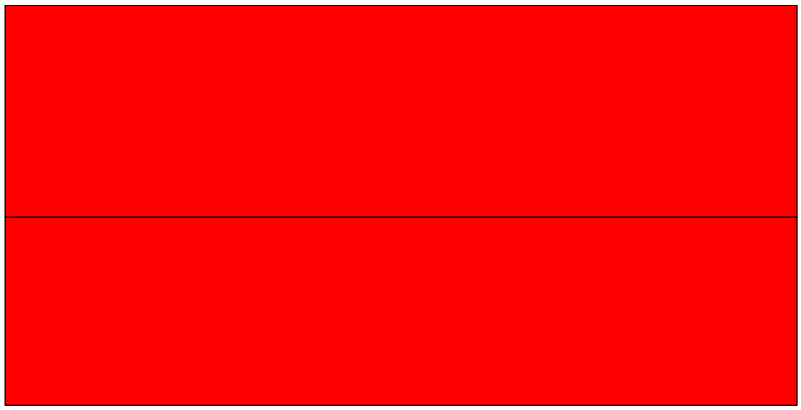

## 4-2 DEFECTS, SYMPTONS AND DETECTIVE PARTS

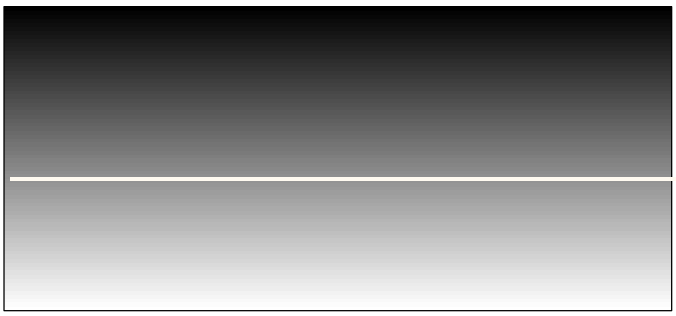
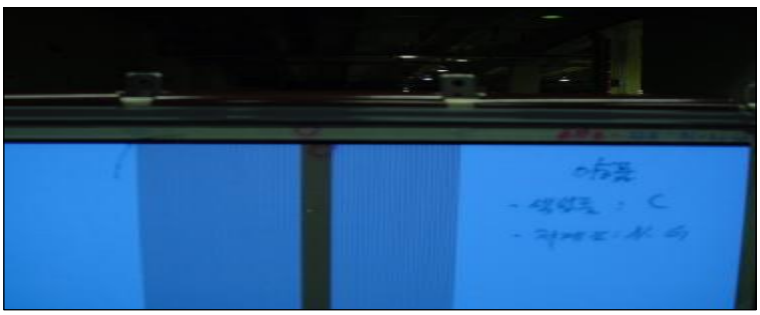
| Condition Name | Description | Related Board |
|---|---|---|
| ■ No Voltage Output | Operating Voltages don't exist. | PSU |
| ■ No Display | Operating Voltages exist, but an Image doesn't exist on screen | Y-MAIN, X-MAIN, Logic Main, Cables |
| ■ Abnormal Display | Abnormal Image(not open or short) is on screen. | Y-MAIN, X-MAIN, Logic Main |
| ■ Sustain Open | some horizontal lines don't exist on screen | Scan Buffer, FPC of X / Y |

| | | |
|---|---|---|
| ■ Sustain Short | some horizontal lines appear to be linked on screen | Scan Buffer, FPC of X / Y |
| ■ Address Open | some vertical lines don't exist on screen | Logic Main, Logic Buffer, FFC,TCP |
| ■ Address Short | some vertical lines appear to be linked on screen | Logic Main, Logic Buffer ,FFC,TCP |

| ◈ Defect: Address(vertical stripe) Open | ◈ Defect: Address(vertical stripe) Short |
|---|---|
| Symptom : A line or block does not light up in address electrode direction.(1 line ,block open) | ■ Symptom: Another color simultaneously appears because adjacent data recognizes the single pattern signal |
|  |  |
| ■Cause<br>① manufacturing : Panel electrode single line/ foreign material./electrostatic/ TCP defect | ■Cause<br>① manufacturing : Panel electrode short / Foreign material conductive foreign object inside TCP |

| | |
|---|---|
| ② Parts : TCP, Board connection defect<br>③ Operation : Assembly error / Film damage | ② Part : TCP/buffer defect lighting electrode cutting defect |

| ◈ Defect: Address output error | ◈ Defect: Sustain(horizontal stripe) Open |
|---|---|
| ■ Symptom.: A defect other than address open and short Data printout signal error occurring at certain Gradation or pattern   | ■ Symptom : One or more line do not light up in Sustain direction  ■Cause : ① manufacturing : .Panel bus electrode single line FPC pressure defect ② Parts : FPC/board/connection disconnection ③ operation : assembly error. |

| ◈ Defect: Sustain(horizontal stripe) Short | ◈ Defect: Dielectric material layer damage |
|---|---|
| ■Symptom : Combined or adjacent lines are short in sustain direction. The line appear brighter than other at Ramp gradation pattern or low gradation patter  | ■ Symptom: Burn caused by the damage of address bus dielectric layer appears in the panel discharge/non discharge area. sustain also open/short occurs by the damage of address sustain printout  <Add Block and Line Open> |

■Cause

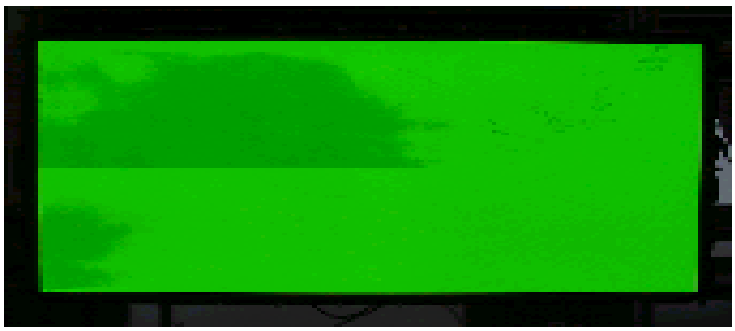
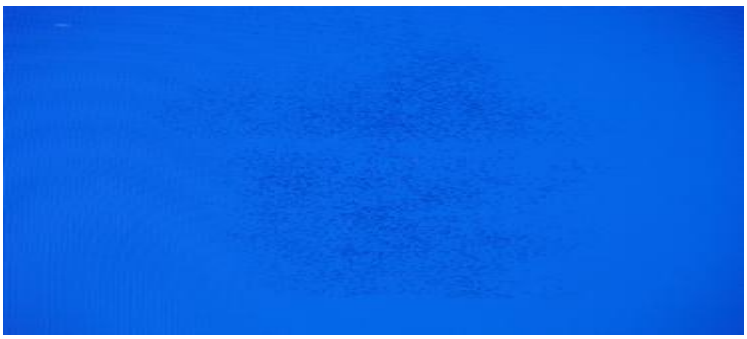
① manufacturing : Panel electrode short/Foreign material.

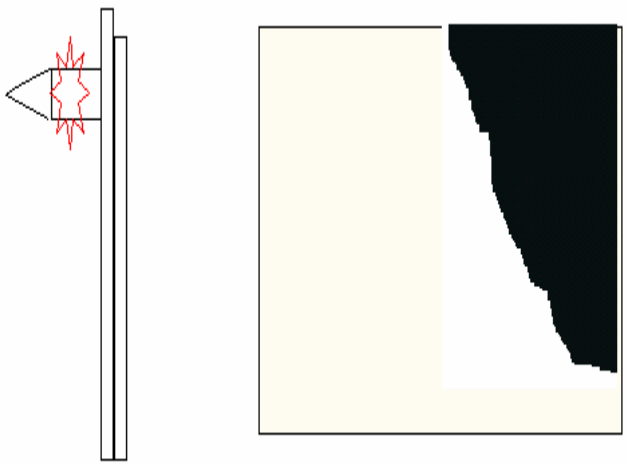
② Parts : Board/ connector/pin error

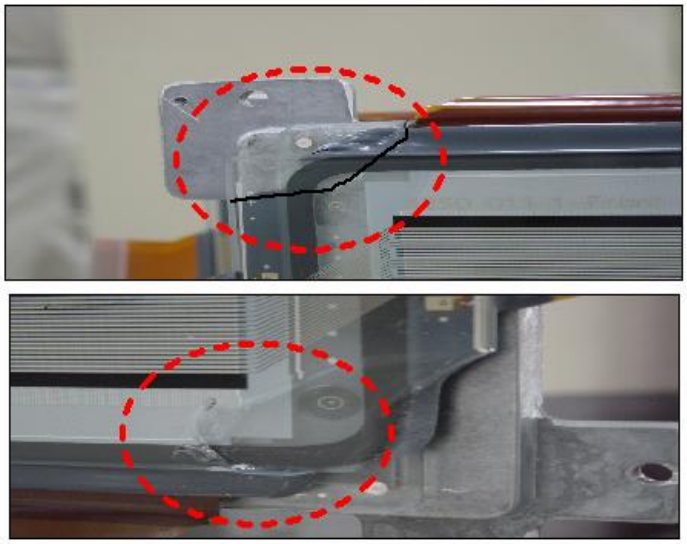
③ Operation : connector / assembling error

<Add and Sustain Open>

■Cause : layer uneven / abnormal voltage / foreign material repair failed

| ◈ Defext: F/White low discharge | ◈ Defect: Weak discharge |
|---|---|
| ■Symptom : Low discharge caused by unstable cells occurring at full white pattern if high (60 degree) or normal temparature. | ■Symptom : Normal discharge but cells appear darker due to weak light emission occurring mainly at low (5 degree) Full white/Red/Green/Blue pattern or gradation pattern |
|  |  |
|  |  |
| ■ Cause<br>① Panel : MgO source / dielectric thickness cell pitch/phosphor<br>② Circuit : drive waveform/ voltage condition | ■ Cause<br>① Panel : MgO deposition count and thinckness / aging condition<br>② Circuit : drive waveform/ voltage condition |

| ◈ Defect : panel damage | ◈ Defect: Exhaust pipe damage |
|---|---|
| ■ Symptom : Panel crack or break. No image appears in some cause depending on the damaged parts and damage level. | ■ Symptom. : Crack in break if exhaust pipe an image is partially lacking or the panel noise occurs depending on the damaged parts and with the passage of time  |



■ Cause

① Manufacturing : Flatness/palette pin interruption

② Operation : overload of panel corner / careless handling

③ Panel : Flatness / assembly error

■ Cause : Careless panel handling

## 5. Disassembling / Assembling

### 5-1 Tools and measurement equipment

#### 5-1-1. Tools

1) (+) type Screw Drivers : to screw the screws
2) Air Blower
3) Earth Ring
4) Small Driver : to adjust potentiometer
5) Dummy Discharge Resistor : 2.4kOhm/10W

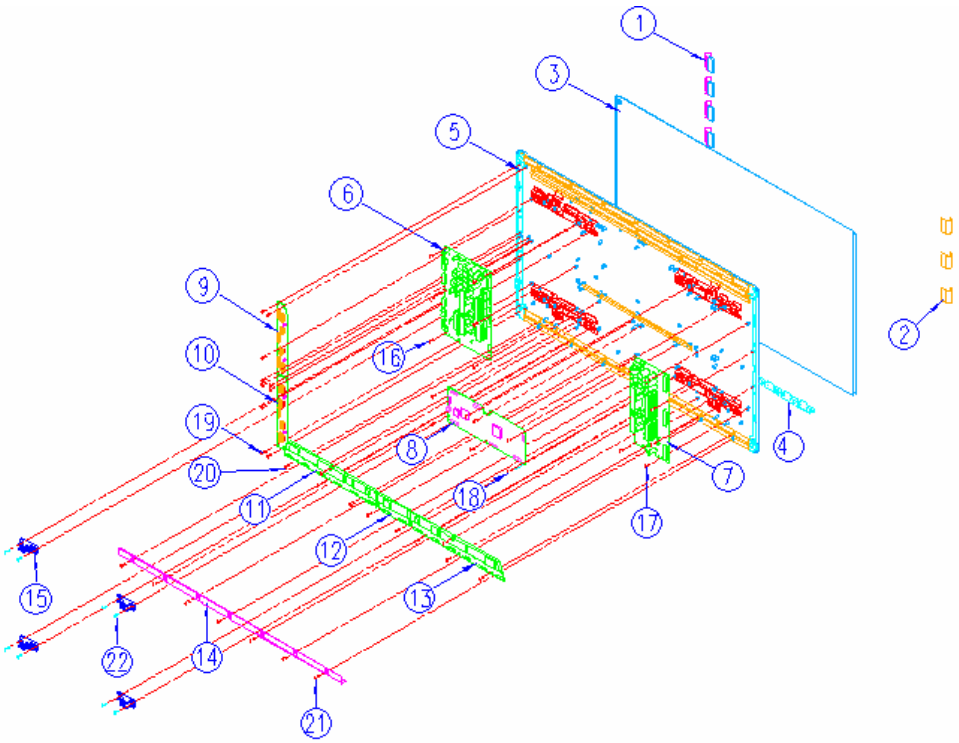
#### 5-1-2. Measuring Equipment

1) Oscilloscope : 500MHz sampling
2) Probe : 10:1

3) Digital Multi-meter

4) Signal Generator

## 5-2 Exploded View

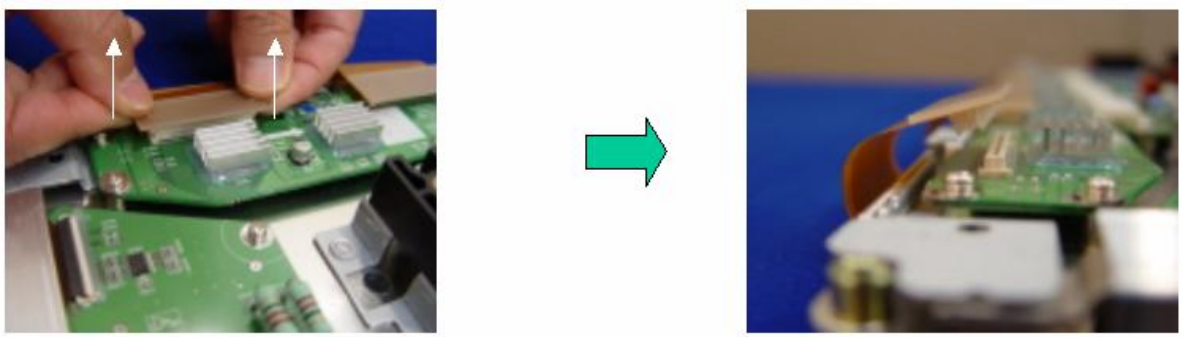


| 항 번 | P/No | 품 명 | 수 량 | 비 고 |
|---|---|---|---|---|
| 1 | LJ94-00002A | Y-FPC | 6 | 42SD,58x61mm(H*V),86LINES,0.6PITCH,80P |
| 2 | LJ39-00114A | X-FPC | 3 | 42SD,S2.0,80,1,GOLD,FPC,X-COMMON,FPC,80P |
| 3 | DP42S006C | Panel | 1 | PANEL:2,SYMMETRY,SINGLE,365X365X365,982X582 |
| 4 | LJ94-00019A | TCP Film | 14 | TCP,52.65X55MM,0.25PITCH,STV7620M/S6PR001,UPILEX-S |
| 5 | LJ93-00105F | Assy,Chassis Base | 1 | LJ64-00195B,AL5052,984*584*T2.0 |
| 6 | LJ92-00944B | Y-Drive | 1 | 42SD V3.1,LJ41-02016A,-,SDI,Y MAIN,310*190*T1.6,TCP |
| 7 | LJ92-00943A | X-Drive | 1 | 42SD V3,LJ41-02015A,SEC,SDI,X MAIN,310*140*T1.6 |
| 8 | LJ92-00975B | Logic-Main | 1 | 42SD V3.1,LJ41-01968A,FGL,SDI,L/MAIN,320*120*T1.6 |
| 9 | LJ92-00796A | Y-Buffer(UP) | 1 | S3.0,LJ41-02059A,-,SDI,Y BUFFER UP,253*45*T1.6,V3 |
| 10 | LJ92-00797A | Y-Buffer(Lower) | 1 | S3.0,LJ41-02059A,-,SDI,Y BUFFER LO,253*45*T1.6,V3 |
| 11 | LJ92-00811A | Logic-Buffer(E) | 1 | 42SD,LJ41-01709A,-,SDI,E BUFFER,372*60*T1.6,V3 TCP |
| 12 | LJ92-00812A | Logic-Buffer(F) | 1 | 42SD,LJ41-01710A,-,SDI,F BUFFER,123*60*T1.6,V3 TCP |
| 13 | LJ92-00813A | Logic-Buffer(G) | 1 | 42SD,LJ41-01711A,-,SDI,G BUFFER,372*60*T1.6,V3TCP |
| 14 | LJ93-00120A | TCP Cover Plate | 1 | LJ63-01613A,LJ02-02061A,LJ02-02062A |
| 15 | LJ60-00119A | Spacer Mount | 4 | 42SD V3.1,ABS,L67.5,BLK,T3,W23,FOR_SONY |
| 16 | 6006-001196 | Screw | 7 | WSP,PH,+,M3,L10,NI PLT,SWRCH10A |
| 17 | 6006-001196 | Screw | 8 | WSP,PH,+,M3,L10,NI PLT,SWRCH10A |
| 18 | 6006-001196 | Screw | 7 | WSP,PH,+,M3,L10,NI PLT,SWRCH10A |
| 19 | 6006-001196 | Screw | 10 | WSP,PH,+,M3,L10,NI PLT,SWRCH10A |
| 20 | 6006-001196 | Screw | 15 | WSP,PH,+,M3,L10,NI PLT,SWRCH10A |
| 21 | 6006-001196 | Screw | 7 | WSP,PH,+,M3,L10,NI PLT,SWRCH10A |
| 22 | 6006-001200 | Screw | 8 | WSP,PH,+,M4,L12,NI PLT,SWRCH18A |

## 5-3 Disassembling & Re-assembling

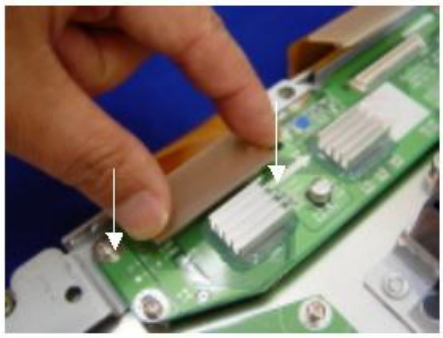
### 5-3-1 Disassembling & Re-assembling of FPC (Flexible Printed Circuit) and Y-Buffer(Upper and Lower)

1. Removal procedures



1) Full out the FPC from Connector by holding the lead of the FPC with hands.

2. Assembling Procedures

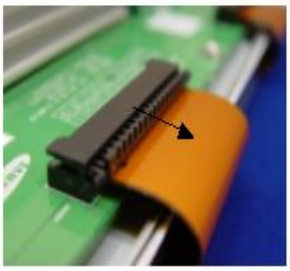


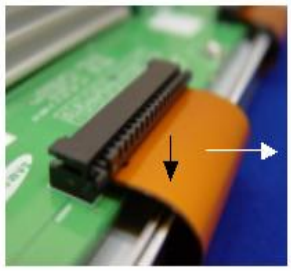
1) Push the lead of FPC with same strength until to be connected completely.

* Notice : Be careful do not get a damage on the connector pin during connecting by mistake.

## 5-3-2 Assembling & Disassembling of Flat Cable Connector of X-Main Board

1. Disassembling Procedure



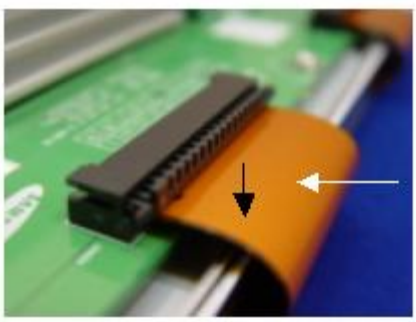


1) Pull out the clamp of connector.

2) Pull Flat cable out press down lightly.

3) Turn the Flat cable reversely.

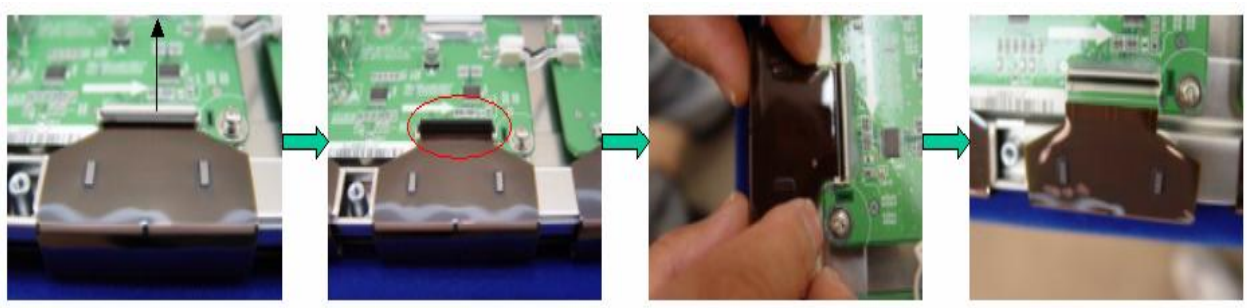
2. Assembling Procedure



1) Put the Flat cable into the connector press down lightly until locking sound (“Dack”) comes out.

### 5-3-3 Assembling & Disassembling the FFC and TCP from Connector

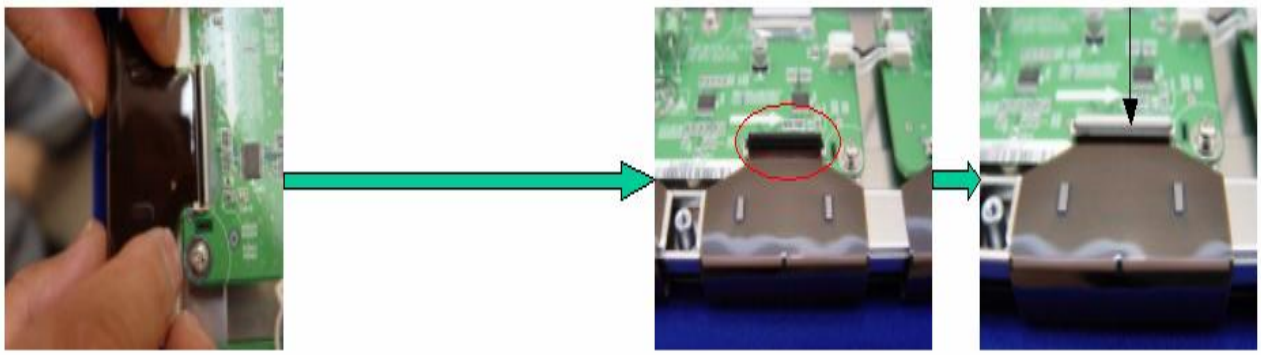
#### 1. Disassembling of TCP



1) Open the clamp carefully.

2) Pull the TCP out from Connector.

#### 2. Assembling of TCP



1) Put the TCP into the Connector carefully

2) Close the clamp completely.
( The sound (“ Dack”) comes out. )

* Notice : TCP and Connector was connected surely.

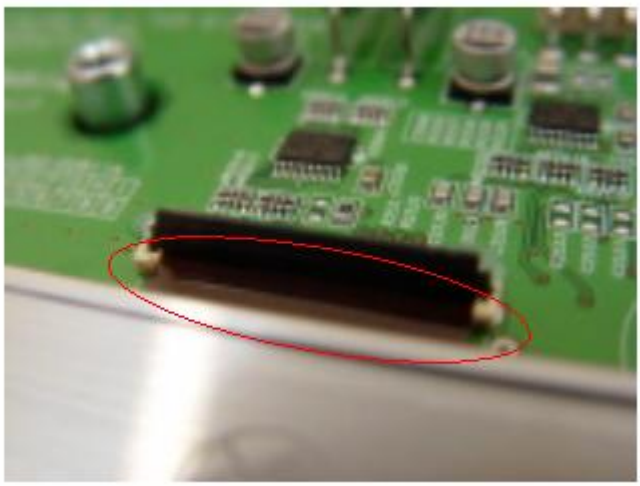
* Notice :

1) Checking whether the foreign material is on the Connector inside before assembling of TCP.

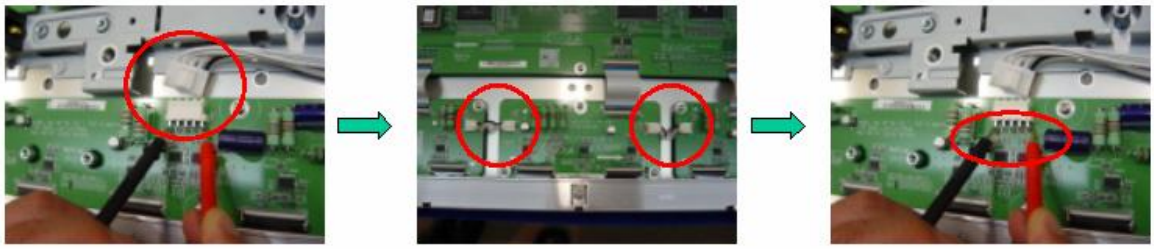
2) Be careful do not get a damage on the board by ESD during handling of TCP.

### 3. Misassembling of TCP

1) The misassembling of TCP is the cause of defect.



### 4. Checking method of misassembling of TCP



1) Disconnecting H3 from CN8006 of LBE.

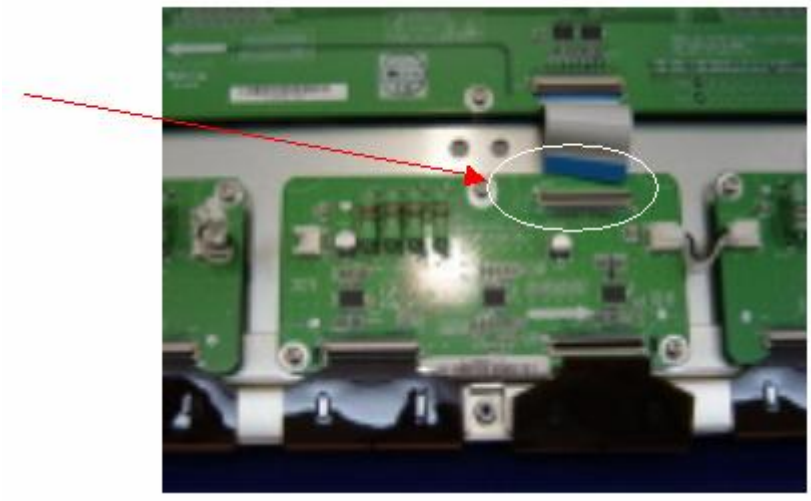
2) Whether H8 and H9 are connected.

3) Checking the resistance between Pin 1 and 5.

Resistance > a few [ K Ohm] : OK

Resistance < 20 Ohm : At least ,more than 1pc of TCP is wrong.

### 5. Assembling & Disassembling of FFC

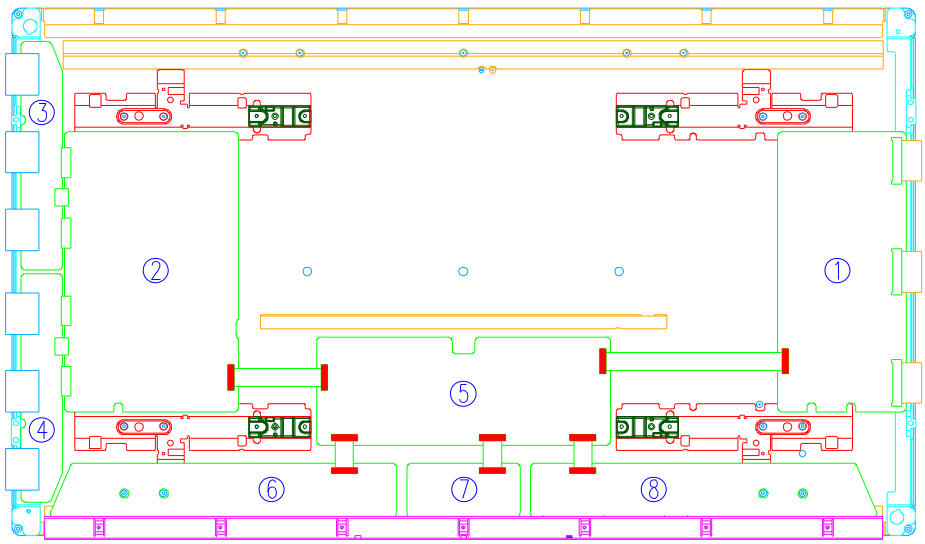


( This is the photo of the assembling of FFC )

The procedure of assembling and disassembling of FFC is the same as TCP.

### 5-3-4 Exchange of LBE, LBF, LBG board

**( Photo 1 )**



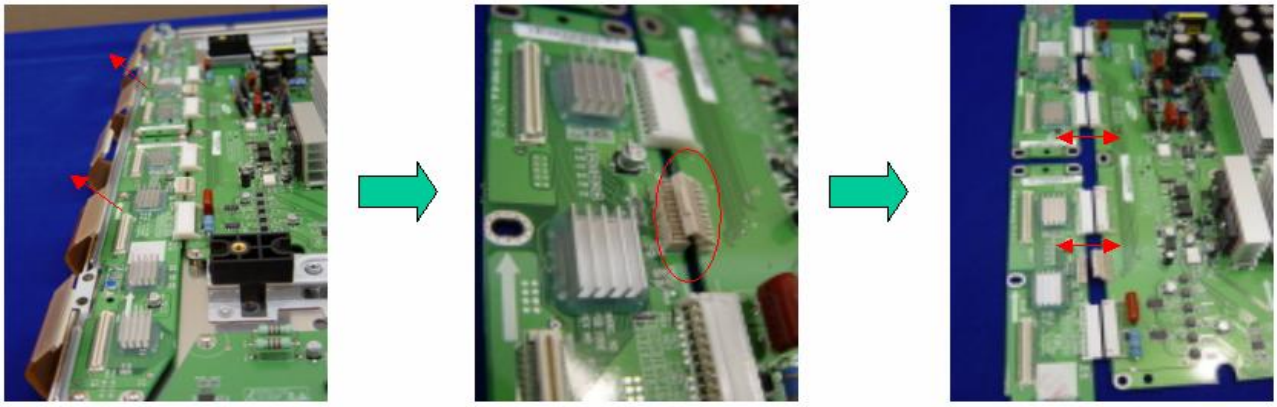

**( Photo 2 )**

1) Remove the screws in order of 2-3-5-7-1-4 from heat sink and then get rid of heat sink. ( Photo 1 )
2) Remove the TPC, FFC and power cable from the connectors.
3) Remove all of the screws from defected board.
4) Remove the defected board.
5) Replace the new board and then screw tightly.
6) Get rid of the foreign material from the connector.
7) Connect the TCP,FFC and power cable to the connector.
8) Reassemble the TCP heat sink.
9) Screw in order of 4-1-7-6-5-3-2. ( Photo 2 )
   If you screw too tightly, it is possible to get damage on the Driver IC of TCP.

* Logic

### 5-3-5 Exchange YBU, YBL and YM board

1) Separate all of the FPC connector of YBU (Y-Buffer upper) and YBL (Lower). ( Photo 1 )
2) Separate all of the connector of CN5001 and CN5008 from Y-Main.
3) Loosen all of the screws of YBU, YBL and YM.
4) Remove the board from chassis.
5) Remove the connector of CN5006 and CN5007 among YBU, YBL and YM.
6) Remove the YBL and YBU from Y-main.
7) Replace the defected board.



8) Reassemble the YBU and YBL to the Y-Main.

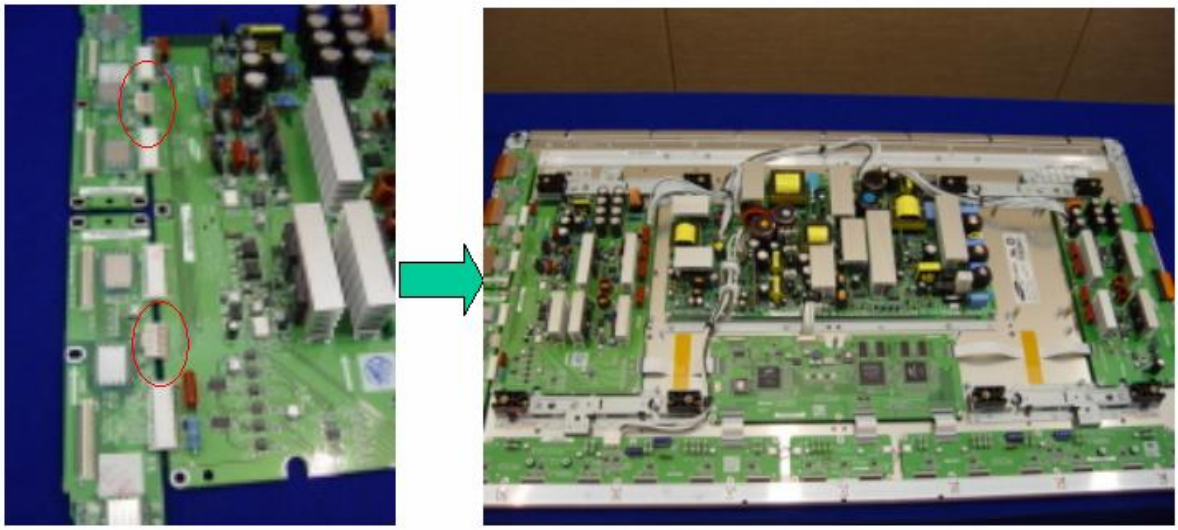
9) Connect the connector of CN5006 and CN5007 among YBU, YBL and YM.

10) Arrange the board on the chassis and then screw to fix.

11) Connect the FPC and YM of panel to the connector.

12) Supply the electric power to the module and then check the waveform of board.

13) Turn off the power after the waveform is adjusted.



# 6. Operation Check after Repair Service

## 6-1 Check Item

| | Check Item | Specification | Remarks |
|---|---|---|---|
| Module assemble check | TCP Assembling condition | Securely connected or tightened | |
| | Drive board | | |
| | Y BUFFER | | |
| | Logic & Logic Buffer | | |
| | Harness | Securely connected | |
| | Material Mixing | No material mixing | |

.

## 6-2 Check Procedure

1) Visual check as following

a. Assembling condition of module.

b. No problem on the connection of module.

c. The grounding and easily short-circuited parts are not damaged.

2)Check the Dip Switch is located module inside.

3) Turn on the power to PDP module, and then check that LED lights up and the SET is working well.

4) Check the power voltage after turn on the power, and then check the Display condition by tapping slightly the Y-FPC 2 or 3 times.

5) Check whether something wrong during Full White Pattern period.

6) If something wrong, each voltage should be set to the standard voltage by using Multi-Tester and adjusting tools.

7) Adjust the waveform, using Oscilloscope for the waveform adjusting point.

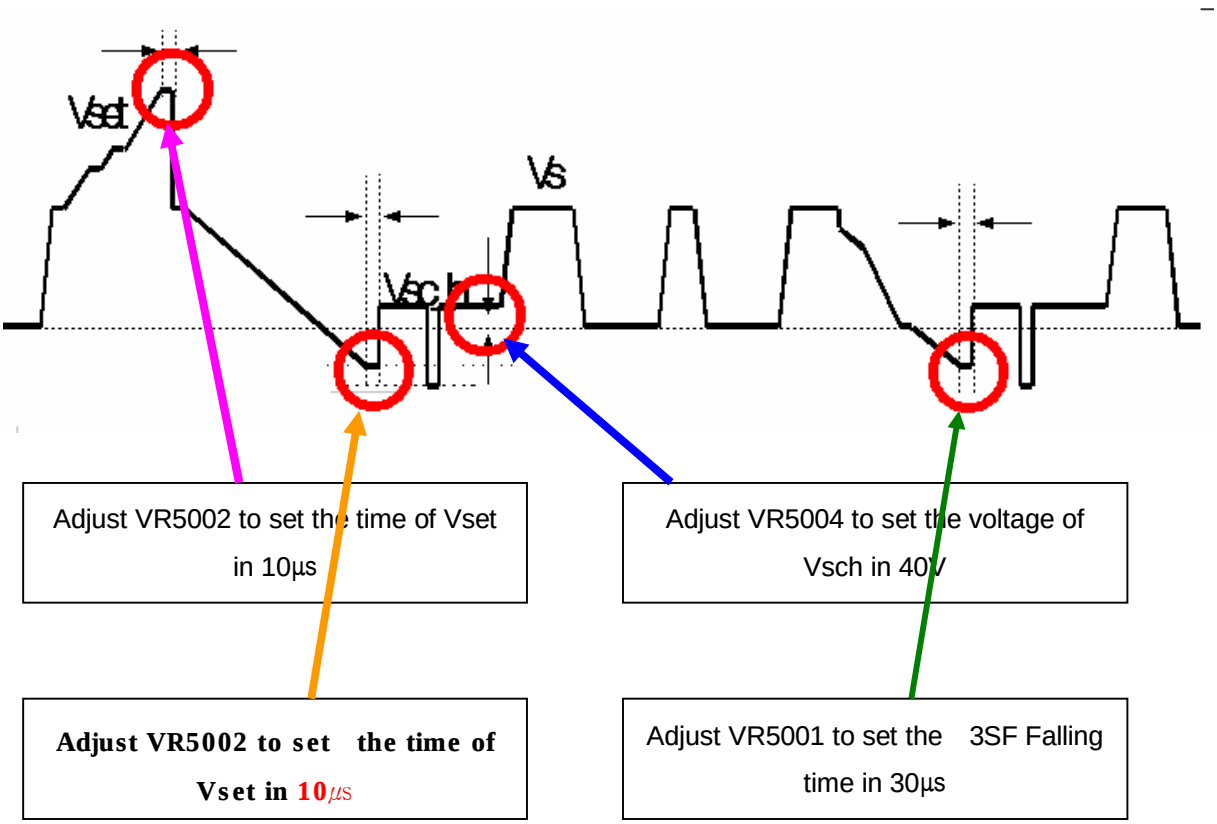
8) Check the discharge of front panel by changing the image for each pattern.

9) Check the Low-discharge, Over-discharge and panel condition by adjusting the Pattern Generator Level.

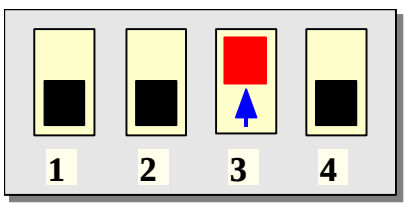
# 7. Operation Check

## 7-1 Adjustment Specification, Checking Position etc.

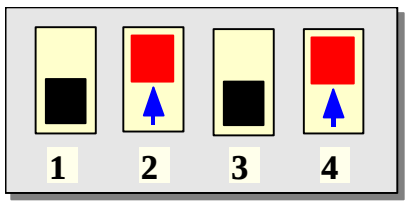
### V3.1 TCP Ramp Waveform Inclination Adjustment ( Y-Board )




*** Dip Switch Mode**




< Internal >




<External>

### 7-2 Adjusting procedure

1) Get Pattern to be Full White.

2) Adjust Vsch to 40V by using VR5004 ( Vsch should be connected to “+” unit of Multimeter).

Vsch is over 95V than Vsc_l.

3) Check the waveform using Oscilloscope.

① Triggering through V_TOGG of LOGIC Board.

② Connect the OUT 4 Test Point at the center of Y_buffer to other channel, and then check the first SF operating waveform of 1TV-Field.

③ Check the waveform as before by adjusting Horizontal Division.

Check the Reset waveform when the V_TOGG Level is changed.

④ Set the Vset to 10us by adjusting VR5002.

GND maintenance section should be checked after the Vertical Division is readjusted to '2V or 5V'.

⑤ Set the Falling maintenance time to 30us by adjusting R5003.

⑥ Change the waveform position of Oscilloscope to 3SF and then set the Falling maintenance time to 30us by adjusting the VR5001.

GND maintenance section should be checked after the Vertical Division is readjusted to '2V or 5V'.

※ Special Notice

When you adjust the inclination of waveform, do check and adjustment being based on the Reset waveform of 1st Sub-field of 1st Frame and then move to 3rd Sub-field for adjusting.

## **8.** SPARE PART LIST FOR THE PANEL

| Beko Part Code | Part Definition |
|---|---|
| **X53.101** | PCB ASSY X MAIN ASSY (LJ92-00943A) |
| **X53.102** | PCB ASSY LOGIC-BUFFER(E) (LJ92-00811A) |
| **X53.103** | PCB ASSY LOGIC-BUFFER(F) SDI 42V3 (LJ92-00812A) |
| **X53.104** | PCB ASSY LOGIC-BUFFER(E) SDI 42V3 (LJ92-00813A) |
| **X53.105** | PCB ASSY Y-BUFFER(UP) SDI 42V3 (LJ92-00796A) |
| **X53.106** | PCB ASSY Y-BUFFER(DOWN) SDI 42V3 (LJ92-00797A) |
| **X53.107** | PCB ASSY LOGIC-BOARD SDI 42V3 (LJ92-00975E) |
| **X53.108** | PCB ASSY SMPS(PSU)SDI 42V3(LJ44-00068A) |
| **X53.109** | PCB ASSY Y-BOARD SDI 42V3 (LJ92-00944B) |
| **X51.112** | FPC 58x61mm(H*V),86LINES,0.6PITCH,80P (LJ94-00002A) |
| **X51.113** | FFC CABLE -FLAT LOGIC-XBOARD (3809-001396)<br>60V,105C,210MM,30P,0.5MM,UL20861 |
| **X51.115** | FFC CABLE -FLAT LOGIC-YBOARD (3809-001397)<br>60V,105C,105MM,40P,0.5MM,UL20861 |
| **X53.116** | FFC CABLE -FLAT 42V3 LOGIC-L-BUFFER (3809-001414) |
| **X53.116** | FFC CABLE -FLAT 42V3 LOGIC-L-BUFFER (3809-001414) |
| **X53.116** | FFC CABLE -FLAT 42V3 LOGIC-L-BUFFER (3809-001414) |
| **X53.117** | CABLE SMPS-LOGIC 42V3 (LJ39-00143A) |
| **X53.118** | CABLE SMPS-L.BUFFER(E) 42V3 (LJ39-00140A) |
| **X53.119** | CABLE SMPS-XBOARD 42V3 (LJ39-00179A) |
| **X53.120** | CABLE SMPS-YBOARD 42V3 (LJ39-00142A) |
| **X51.120** | CABLE L.BUFFER-L.BUFFER (LJ39-00109A) |
| **X51.120** | CABLE L.BUFFER-L.BUFFER (LJ39-00109A) |