SHARP SERVICE MANUAL

CODE: 00ZERA57VOSME

ER-A570 OPTION

SRN (IN-LINE) INTERFACE

ER-A6IN

RS-232 INTERFACE

ER-A5RS

CONTROL ROM

MODEL ER-A57R1

(For "V" version)

CONTENTS

Parts marked with "! " is important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

SHARP CORPORATION

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The contents are subject to change without notice.

● Precautions

1. Downloading the data from the ER-02FD in the inline system

To download the data from the ER-02FD onto the ECR in the inline system, the following procedure must be observed.

1) Download the data from the ER-02FD onto the ECR using the SRV #998.
2) Execute the SRV RESET operation.
3) Execute either the INLINE RAM CLEAR operation (#899) or the INLINE SET UP 1 JOB operation (#895).
4) Check the SRV #970 to see if the ECR memory capacity exceeds the packaged RAM memory capacity. If it does, add an optional RAM and follow the same procedure all over again from step 1).

I. SRN (IN-LINE) SYSTEM FOR ER-A570

ER-A6IN

MODEL ER-A57R1 (For ER-A570)

(OPTIONS FOR ER-A570)

CONTENTS

CHAPTER 1. ER-A570 SRN (IN-LINE) SYSTEM CONFIGURATION

The ER-A570 in-line system conforms to the SHARP Retail Network that consists of a master and a maximum of 15 satellites (inclued the one backup master).

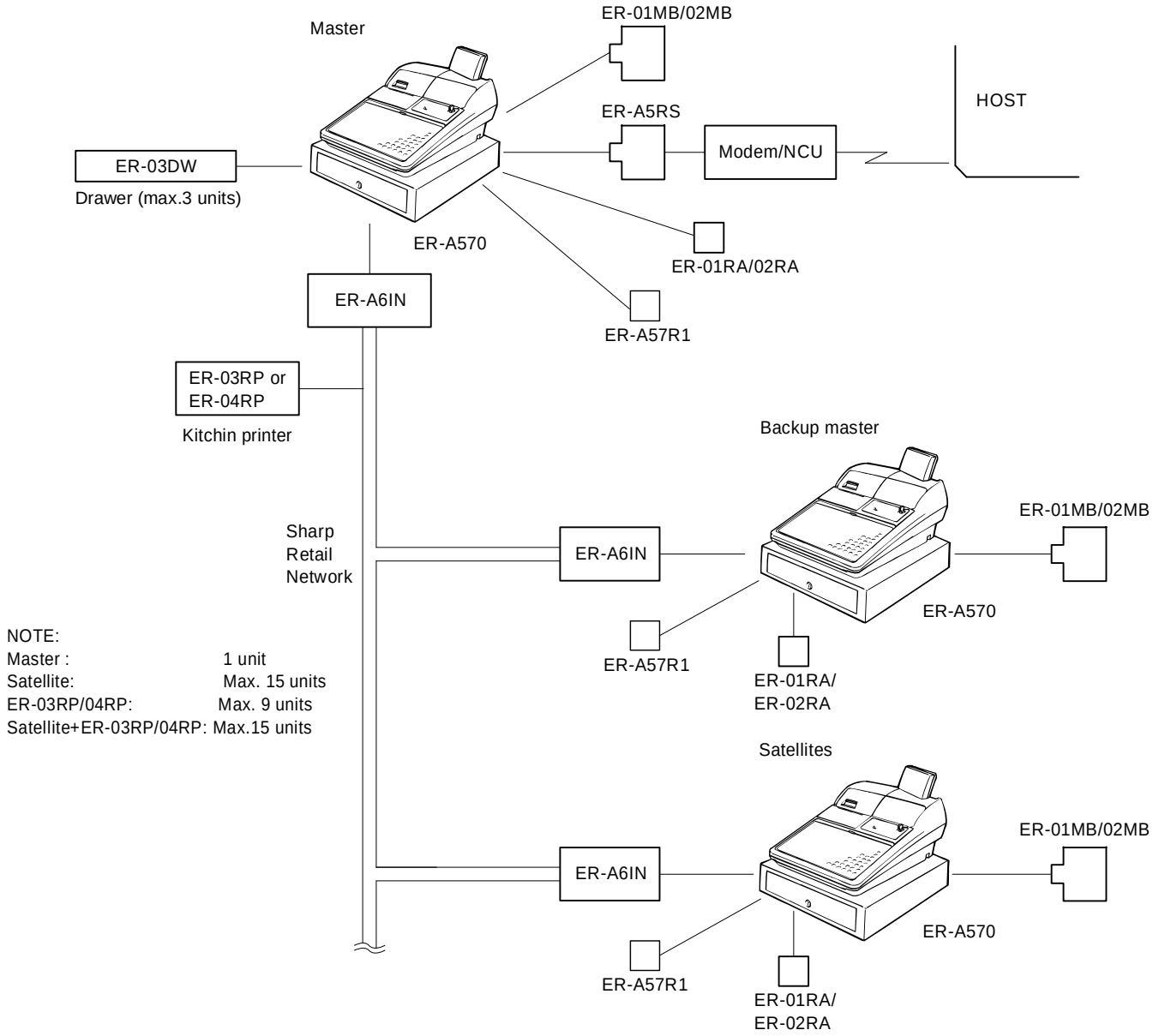


Fig. 1-1

CHAPTER 2. HARDWARE REQUIREMENTS

1. Master System

The following optional units are required to complete the master system configuration.

The master may require additional RAM for allocating the IRC files.

1) ER-A6IN: SRN I/F control board
2) ER-01RA: Option RAM chip (32KB)
   ER-02RA: Option RAM chip (128KB)
   ER-01MB: Option RAM board (Max. 512K bytes)
   ER-02MB: Option RAM board (1M bytes)
3) ER-A57R1: Option device control ROM (1 chip)

- The ROM chip (ER-A57R1) is installed on the main PWB of ER-A570.

2. Satellite system (inclued the backup master)

The following optional units are required to complete the Satellite systems configuration.
The satellite may require additional RAM for allocating the IRC files.

1) ER-A6IN: SRN I/F control board
2) ER-01RA: Option RAM chip (32KB)
   ER-02RA: Option RAM chip (128KB)
   ER-01MB: Option RAM board (Max. 512K bytes)
   ER-02MB: Option RAM board (1M bytes)
3) ER-A57R1: Option device control ROM (1 chip)

- The ROM chip (ER-A57R1) is installed on the main PWB of ER-A570.

3. Components

NO	MANE	PARTS CODE	Q'ty
1	PWB UNIT	CPWBX7317RC01	1
2	PWB BRACKET	LANGT7466RCZ Z	1
3	CONNECTOR BRACKET	LANGT7510RCZ Z	1
4	SCREW (FOR HOLDING OF THE PWB AND PWB BRACKET)	LX –BZ6665RCZZ	2
5	SCREW (FOR : PWB BRACKET AND PWB BRACKET, PWB BRACKET AND MAIN CHASSIS, GND WIRE.)	LX–BZ6774R CZZ	5
6	WIRING TIE	LBNDJ2004SCZ Z	1
7	SPACER	PSPAN7039XCZZ	1
8	FERRITE CORE (FOR INTERNAL CABLE)	RCORF6666 RCZZ	1
9	INTERNAL CABLE	QCNW–6856RCZ Z	1
10	BNC-T CONNECTOR	QCNC–6811RC 0C	1

CHAPTER 3. TRANSMISSION SYSTEM SPECIFICATIONS

1. Transmission Method

1) Carrier sense multiple access with collision detect (CSMA/CD)
2) Single channel, half duplex
3) High level data link controller (HDLC)

2. Transmission Medium

1) Topology: Common Bus System
2) Coaxial cable RG-58/u

3. Transmission Speed

480KBPS/1MBPS (Selectable) ... SRV mode JOB#922.

4. Data Transfer Method

Packet-data transfer method
Data side of 1 paket is MAX. 270 Byte.

5. Maximum Length of Transmission Cable

1000m (3281 ft) . . . trunk cables + branch cables; however, branch cable length is 10m (5m × 2) for each terminal.

6. Max Terminals

16 Terminals max. (15 satellites, 1 master)

7. Physical Organization

The branch cable is not included in the standard accessories of the ER-A6IN. Please order with the following code.

PARTS CODE	PRICE RANK	DESCRIPTION
QCNW-6835RCZZ	BM	Branch cable

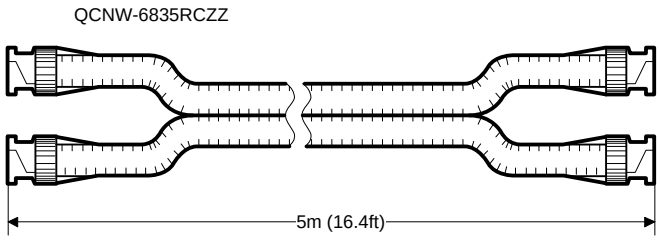


Fig. 3-1

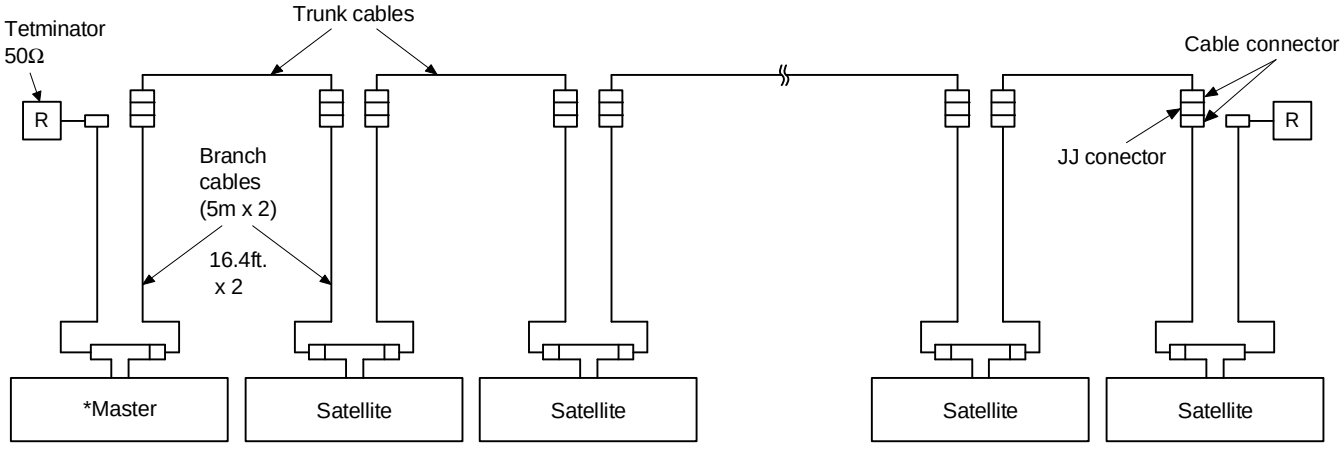


Fig. 3-2 physical organization

*NOTE: The master can be located anywhere within the SRN (IRC) network configuration.

8. Packet Format

F 8 Bits	1 Opening flag (8 Bits) (01111110) (7E)
DA 8 Bits	2 Destination address (00-FEH) (SRN Terminal Number)
SA 8 Bits	3 Source address (00-FEH)
TYPE 8 Bits	4 Packet type (DATA/ACK/RACK/NRDY)
CH NO 8 Bits	5 Channel No. (01H = CH1; 02H = CH2)
DLS 8 Bits	6 Circuit status: Buffer full, RE-transmit, Unable
	7 Dummy
BCL 8 Bits	8 Number of bytes at the data unit
BCH 8 Bits	
DATA max. 270 bytes.	9 DATA Number of data bytes (270 Bytes)
CRC 8 Bits	Φ CRC check code
CRC 8 Bits	
F 8 Bits	Γ Closing flag (8 Bits) (01111110) (7E)

Fig. 3-3 Packet format

1 Opening flag (7E)
The open flag (7E) is sent at the beginning of each packet. As the SRN control circuit (receiving side) receives the flag, it will start the receiving operation.

NOTE: The packet begins with the open flag (8 Bits) and ends with a closing flag (8 Bits).

2 Destination address (00H – FEH)
The destination address indicates where the packet is addressed (receiving unit) too. The terminal number of each unit is converted into a hexadecimal number to be used for the destination address.

3 Source Address (00H – FEH)
The source address indicates the sending unit (transmit unit). The terminal number of each unit is converted into a hexadecimal number to be used for the source address.

4 Types of packets
There are four types of packets each are used to indicate the type of packet to be transferred.

00: DATA packet
(summary and preset data)

01: ACK packet
The acknowledging packet that is sent to the transmitting side from the receiving side to indicate that the packet was received properly.

02: RACK packet
The acknowledging packet that will be sent to the receiving side to indicate that the ACK packet has been properly received by the sending side.

03: NRDY packet
The acknowledge packet that is sent to the sending side to indicate that it is not ready to receive data.

5 Channel No.
Indicates that channel of the packet. (Channel 1 or Channel 2)

6 Circuit status
In the case of the NRDY packet, it indicates why the NRDY packet was issued.

1) Unable to handle received data because the receiving side is in the BUSY state.

2) Unable to handle received data because the receiving buffer is full.

7 Number of data bytes
Indicates the number of bytes of data, which is a data, packet status that will be converted into hexadecimal numbers before transmission. Maximum number of bytes is 270.

8 Data
Transfer data is contained in this field. Size of data is limited to a maximum of 270 bytes. It can only exist in the data packet.

9 CRC check code
This check code is used to detect any errors in the transmit data. A CRC code is generated from the sending side to be sent to the receiving side.
At the receiving side, the CRC check code is generated on the basis of the same formula as the sending side to verify it against the CRC check code receive.

Φ Closing flag (7E)
The closing flag is sent at the end of the packet. When the IRC control circuit at the receiving side receives the flag, it terminates the operation.

9. Type of packet

Two types of packet formats are available for the SHARP RETAIL NETWORK. One is the data packet (the content of data is judged by the host level). The other is the control packet which is responded to by the controller level and has three types of packets: ACK packet, RACK packet and NRDY (NOT READY) packet.

(1) DATA packet: is used for sending and receiving data. Its contents are judged at the host level.

(2) ACK packet: is a response sent from the sink station to the source station by the link level (of DATA packet) when the DATA packet is properly received.

(3) NRDY (NOT READY) packet is a response packet of the link level. It is used in case it is unable to receive in the host level or no space is available in its receive buffer despite the the error check CRC of the DATA packet is normal.

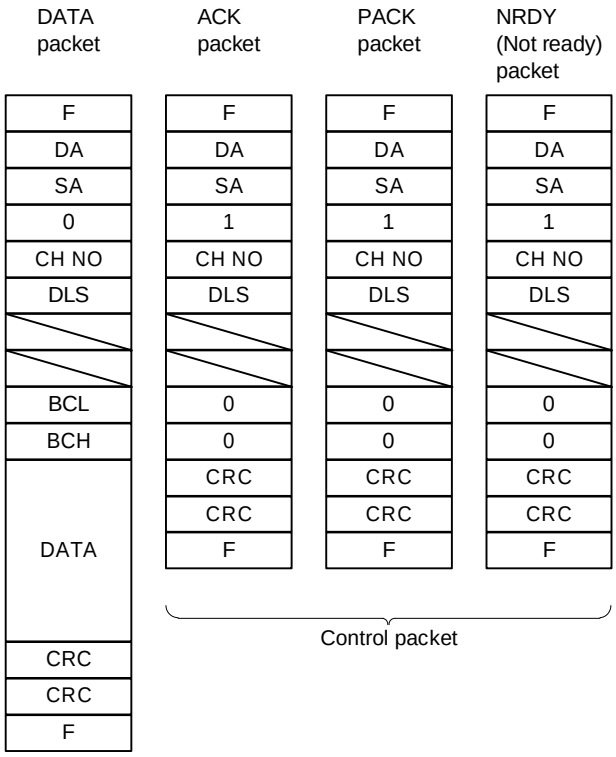
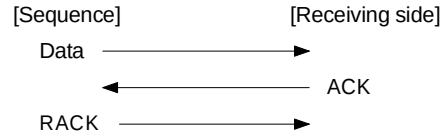


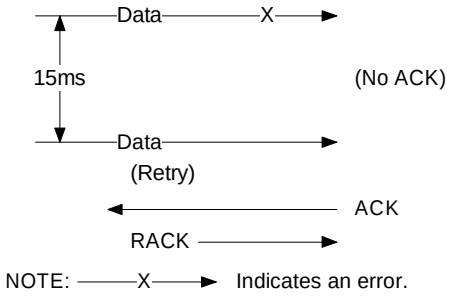
Fig. 3-4 Types of packets

10. Transmission Procedure

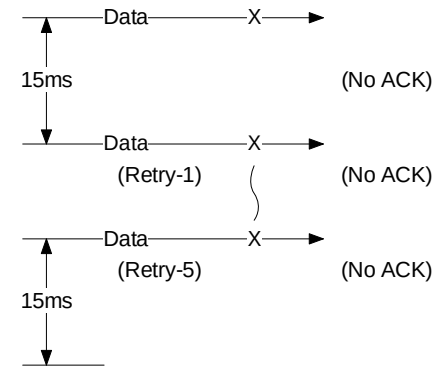
1 Normal sequence



2 Abnormal sequence-1
(when there is a single data error)

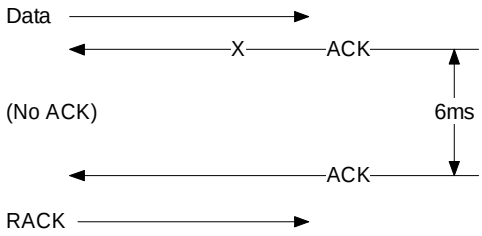


3 Abnormal sequence-2
(when there are six successive data errors)

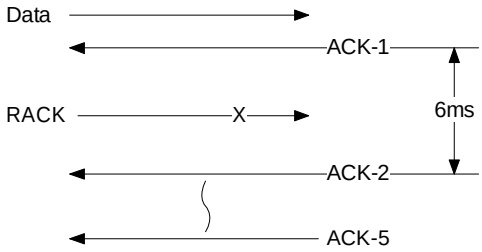


Communication is disabled due to full retry counts . . . "PW-OFF" (power off) will be printed on the master unit.

4 Abnormal sequence-3 (when ACK is in error)

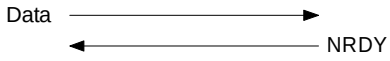


5 Abnormal sequence-4 (when RACK is in error)



Full ACK retry counts. If RACK were not detected after five retries to send ACK, it assumes RACK to be in error, and so the receiving operation terminates normally.

6 Abnormal sequence-5
(receiving side not enabled to receive data)

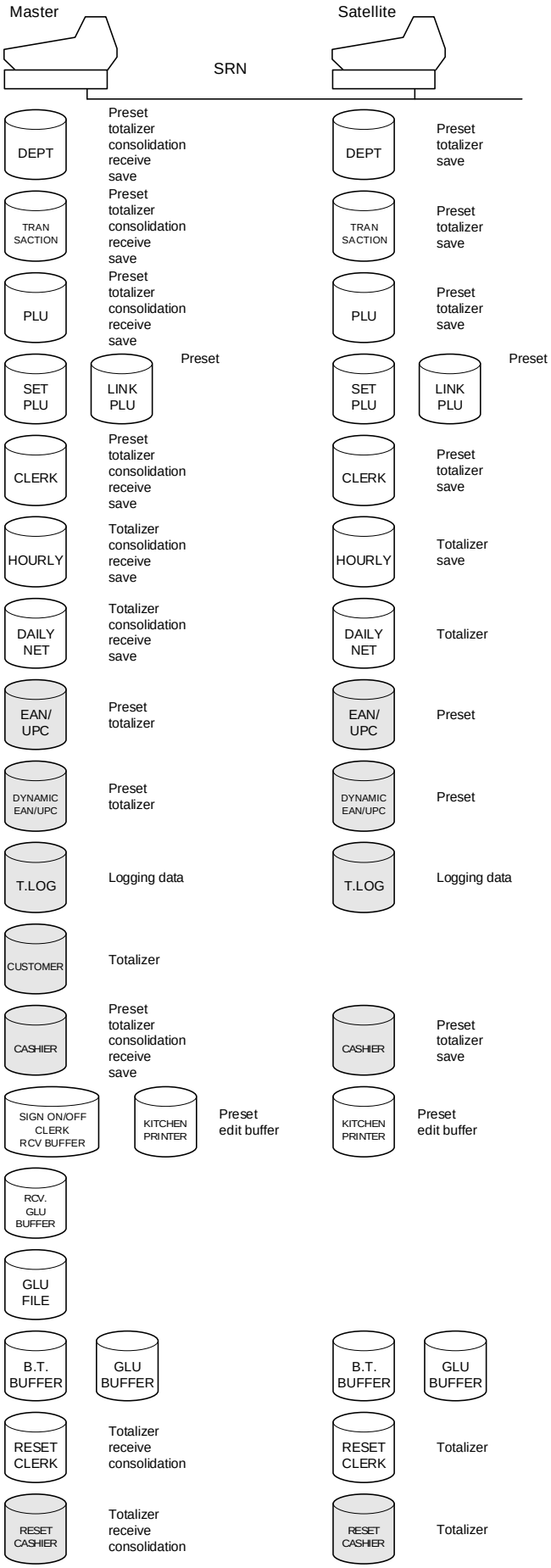


11. Terminal Number Assignment

when the IRC option is installed, an IRC terminal number must also be supplied. This number is in the range of 1 to 254. The number is specified in the PGM 2 mode at installation time. It is necessary to specify an number for each device connected to the IRC including the master. It should be noted that the IRC terminal number and the register number are not related. Section 10 of this manual indicates how this number is specified.

- IRC terminal number (3 digits max.): *000 ~ 254
  *000: OFF line machine
- Register number (4 digits max.): *0 ~ 9999
  *0: can not be used in the IRC operation.

CHAPTER 4. FILE/DATA ALLOCATION IN THE IN-LINE SYSTEM



(in the ER-A570, the shaded section ( ) is not used.)

Fig. 4-1

* 1 ; In case of system report job disable on back-up master, consolidation and receive files need not be created in back-up master.
* 2 ; The clerk totalizer file only need to have one blocks.
* 3 ; The clerk consolidation/receive/save files need not be created in case of floating clerk system.
* 4 ; The sign on/off clerk file need not be created in case of individual clerk system.

CHAPTER 5. PROGRAM DATA UPDATING

1. General

There are two ways of updating the preset data for the ER-A570 in-line system.

1) To download the reset file of the master to a satellite after clearing preset file of the slave.

   This mode can be used at the time the machine is installation.

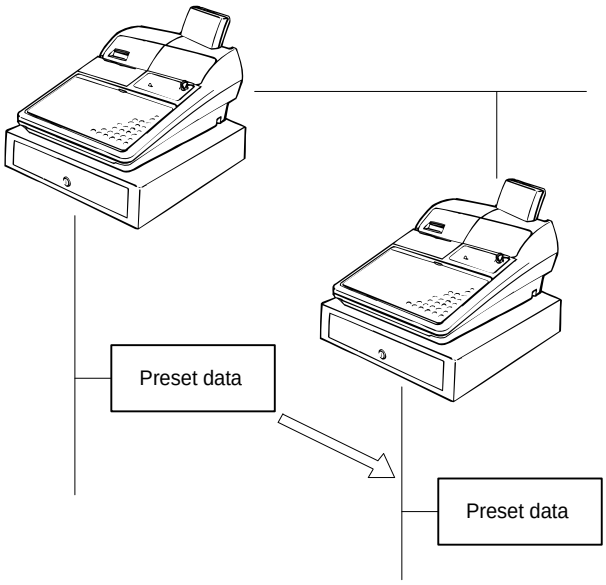


Fig. 5-1

2) To download the preset file of the master to the preset file of a slave without clearing the slave"s preset file. (Downloading file with a job number in 5000)

   This mode can be used at the time of correcting preset data.

   Data process on the satellite to which the master preset file is downloaded

   (a) When a preset file whose job number is 4000s is downloaded, the contents of the corresponding file in the satellite is zero cleared before saving the data received from the master.

   (b) When a preset file whose job number is 5000s is downloaded, the contents of the corresponding file in the satellite is replaced by the preset file sent from the master.

2. Down-Loading Job List

List of Down load jobs

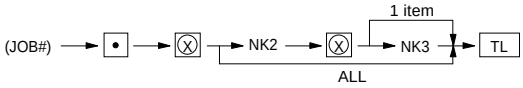
Mode	Job	Item	Note
SRV	800	SRV parameter	Including the machine parameter relating to inline operations. ("#902, #920 d" is not downloaded.) PGM2 secret code preset
	845	Training text CLK No.	
	850	Free Key layout	
PGM	4100	Dept preset	with clearing function
	4119	Direct Dept/PLU key	
	4200	PLU/LINK/SET preset	with clearing function
	4300	Transaction preset	with clearing function
	4220	LINK PLU preset	with clearing function
	4221	SET PLU preset	with clearing function
	4400	Clerk preset	
	4600	Other preset	
	4610	Date, time	
	4614	Logo text	
	4644	Message text	
	4654	Guidance text	
	4700	TAX preset	
	4800	ONLINE preset	
	4950	IRC KP preset	
	4900	PGM preset relating to inline operations	
	4999	All PGM preset	
	5100	Dept preset	without clearing function
	5200	PLU/LINK/SET preset	without clearing function
	5220	LINK PLU preset	without clearing function
	5221	SET PLU preset	without clearing function
	5300	Transaction preset	without clearing function
			without clearing function
			without clearing function

#4200 and #5200 don't include stock data.
#4600 Other preset : Optional feature preset, VP preset, Hourly report, Stack report, Secret code PGM1, X1/Z1, X2/Z2, Auto key, PLU Level range.
#4400 exists in only clerk individual system.
#4200 include link PLU and set PLU presets.

3. Key operation

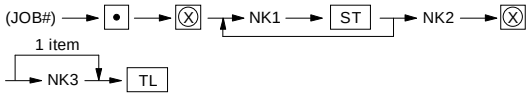
1) Down-loading of PGM-mode program data on DEPT/PLU

(a) Down-loading to all the satellites in the system



NK2: Register No.

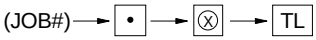
(b) Down-loading to the satellite specified



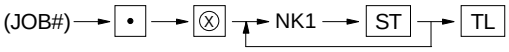
NK1: Register No.
NK2: Start code
NK3: End code

2) Down-loading of other program data

(a) Down-loading to all the satellites in the system



(b) Down-loading to the satellite specified



NK1: Register No.

4. Others

1) If a transmission error occurs, the machine number of a satellite in which the error has occured is printed In that case, the manager retry function becomes available.

2) After transmission termination, the master prints the receipt/journal to that effect.

3) Broadcast communication

SRV mode down load job and PGM mode #4XXX (with clear job) job is used by broadcast communication.

Broadcast communication method:
The master is communicated to all satellites at a time.

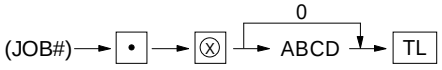
The download of broardcast communication is as follows
a) Master downloads to all satellites.
(Broadcast communication)
<DISPLAY: SENDING>
b) All satellites receives the data.
c) Master checks communication error to each satellite. (Normal cumminocation)
<DISPLAY : each register number>

NOTE: Setting of SRV mode programming JOB #920-C "BROADCAST COMMUNICATION"

- When the ER-03RP/04RP is in the inline system, set up in the following two methods*

1) Set JOB #920-C "BROADCAST COMMUNICATION" to "NOTHING."
2) When performing broadcast downloading (#4XXX), turn off the power of the ER-03RP/04RP, or turn off/on the power of the ER-03RP/04RP after execution of downloading.

CHAPTER 6. SRV-MODE PROGRAMMING



M: Master
S: Satellite

<table>
<tr><th>No.</th><th>Job#</th><th>M/S</th><th>Item</th><th>Key sequence</th></tr>
<tr><td>1</td><td>#902 MRS = 0000</td><td>M/S</td><td>902-A: 1. Choice of inline</td><td>
<table>
<tr><td>1. Inline</td><td>902-A</td></tr>
<tr><td>No</td><td>0</td></tr>
<tr><td>Yes</td><td>1</td></tr>
</table>
</td></tr>
<tr><td>2</td><td>#918 MRS = 0000</td><td>M/S</td><td>918-A: 1. Printing of text of a tied PLU in set PLU
2. Direct non tendering finalization after previous tender entry
3. Output of set PLU to KP</td><td>
<table>
<tr><th>1. Printing of text of a tied PLU in set PLU</th><th>2. Direct non tendering finalization after previous tender entry</th><th>3. Output of set PLU to KP</th><th>918-A</th></tr>
<tr><td rowspan="4">Yes</td><td rowspan="2">Disable</td><td>By tied PLU</td><td>0</td></tr>
<tr><td>Set PLU's KP</td><td>1</td></tr>
<tr><td rowspan="2">Enable</td><td>By tied PLU</td><td>2</td></tr>
<tr><td>Set PLU's KP</td><td>3</td></tr>
<tr><td rowspan="4">No</td><td rowspan="2">Disable</td><td>By tied PLU</td><td>4</td></tr>
<tr><td>Set PLU's KP</td><td>5</td></tr>
<tr><td rowspan="2">Enable</td><td>By tied PLU</td><td>6</td></tr>
<tr><td>Set PLU's KP</td><td>7</td></tr>
</table>
<table>
<tr><td>1. Red color printing on KP when PLU's unit price is zero</td><td>918-B</td></tr>
</table>
</td></tr>
<tr><td></td><td></td><td>M/S</td><td>918-B: 1. Red color printing on KP when PLU's unit price is zero</td><td>
<table>
<tr><td>No</td><td>0</td></tr>
<tr><td>Yes</td><td>2</td></tr>
</table>
</td></tr>
<tr><td></td><td></td><td>M/S</td><td>918-C: 1. Printing of Z counter on Z1/Z2 report
2. Comulating orders in KP
3. Printing the DEPT./PLU text on KP in double size character</td><td>
<table>
<tr><th>1. Printing of Z counter on Z1/Z2 report</th><th>2. Comulating orders in KP</th><th>3. Printing the DEPT./PLU text on KP in double size character</th><th>918-C</th></tr>
<tr><td rowspan="4">Yes</td><td rowspan="2">Yes</td><td>No</td><td>0</td></tr>
<tr><td>Yes</td><td>1</td></tr>
<tr><td rowspan="2">No</td><td>No</td><td>2</td></tr>
<tr><td>Yes</td><td>3</td></tr>
<tr><td rowspan="4">No</td><td rowspan="2">Yes</td><td>No</td><td>4</td></tr>
<tr><td>Yes</td><td>5</td></tr>
<tr><td rowspan="2">No</td><td>No</td><td>6</td></tr>
<tr><td>Yes</td><td>7</td></tr>
</table>
</td></tr>
<tr><td></td><td></td><td>M/S</td><td>918-D: 1. Tip paid includes cash tip
2. Clearing of tip totalizer at clerk Z1 report
3. Printing of tip totalizer on the clerk report</td><td>
<table>
<tr><th>1. Tip paid includes cash tip</th><th>2. Clearing of tip totalizer at clerk Z1 report</th><th>3. Printing of tip totalizer on the clerk report</th><th>918-D</th></tr>
<tr><td rowspan="4">Yes</td><td rowspan="2">No</td><td>No</td><td>0</td></tr>
<tr><td>Yes</td><td>1</td></tr>
<tr><td rowspan="2">Yes</td><td>No</td><td>2</td></tr>
<tr><td>Yes</td><td>3</td></tr>
<tr><td rowspan="4">No</td><td rowspan="2">No</td><td>No</td><td>4</td></tr>
<tr><td>Yes</td><td>5</td></tr>
<tr><td rowspan="2">Yes</td><td>No</td><td>6</td></tr>
<tr><td>Yes</td><td>7</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>No.</th><th>Job#</th><th>M/S</th><th>Item</th><th>Key sequence</th></tr>
<tr><td rowspan="4">3</td><td rowspan="4">#920 MRS = 0000</td><td>S</td><td>920-A: 1. Buck up master function</td><td>
<table>
<tr><td>1. Buck up master function</td><td>920-A</td></tr>
<tr><td>Not</td><td>0</td></tr>
<tr><td>Exit</td><td>1</td></tr>
</table>
</td></tr>
<tr><td>M/S</td><td>920-B: 1. System report and down load job is executed in the buck up master
2. The GLU finalization is executed in the setellite
3. The clerk system</td><td>
<table>
<tr><td>1. System report and down load job is excuted in the back up master</td><td>2. The GLU finalization is executed in the satellite</td><td>3. The clerk system</td><td>920B</td></tr>
<tr><td rowspan="2">Disable</td><td rowspan="2">Enable</td><td>Centralized</td><td>0</td></tr>
<tr><td>Individual</td><td>1</td></tr>
<tr><td rowspan="2">Disable</td><td>Centralized</td><td>2</td></tr>
<tr><td>Individual</td><td>3</td></tr>
<tr><td rowspan="2">Enable</td><td rowspan="2">Enable</td><td>Centralized</td><td>4</td></tr>
<tr><td>Individual</td><td>5</td></tr>
<tr><td rowspan="2">Enable</td><td>Centralized</td><td>6</td></tr>
<tr><td>Individual</td><td>7</td></tr>
</table>
</td></tr>
<tr><td>S</td><td>922-C: 1. Broad cast communication
2. PGM-mode programming at the satellite</td><td>
<table>
<tr><td>1. Broadcast communication</td><td>2. PGM mode programming at the satellite</td><td>920-C</td></tr>
<tr><td rowspan="2">Exist</td><td>Disable</td><td>0</td></tr>
<tr><td>Enable</td><td>1</td></tr>
<tr><td rowspan="2">Nothing</td><td>Disable</td><td>4</td></tr>
<tr><td>Enable</td><td>5</td></tr>
</table>
<table>
<tr><td>1.Machine assignment</td><td>920-D</td></tr>
</table>
</td></tr>
<tr><td>M/S</td><td>920-D: 1. Machine assignment</td><td>
<table>
<tr><td>Standalone</td><td>0</td></tr>
<tr><td>Satellite</td><td>1</td></tr>
<tr><td>Master</td><td>2</td></tr>
<tr><td>Backup master</td><td>3</td></tr>
</table>
</td></tr>
<tr><td>4</td><td>#922 MRS = 0008</td><td>M/S</td><td>922-A, B</td><td>Not used. (Fixed at "00".)</td></tr>
<tr><td></td><td></td><td></td><td>922-C, D: 1. SRN transmission speed and carrier-off waiting time</td><td>
<table>
<tr><td>1. Transmission speed</td><td>2. Carrier-off waiting time</td><td>922-C,D</td></tr>
<tr><td rowspan="4">480K BPS</td><td>12.8 msec</td><td>00</td></tr>
<tr><td>3.2 msec</td><td>01</td></tr>
<tr><td>6.4 msec</td><td>02</td></tr>
<tr><td>9.6 msec</td><td>04</td></tr>
<tr><td rowspan="4">1M BPS</td><td>6.4 msec</td><td>08</td></tr>
<tr><td>1.6 msec</td><td>09</td></tr>
<tr><td>3.2 msec</td><td>10</td></tr>
<tr><td>4.8 msec</td><td>12</td></tr>
</table>
</td></tr>
<tr><td>5</td><td>#923 MRS = 0000</td><td>M/S</td><td>923-A, B, C, D:</td><td>Not used. (Fixed at "0000")</td></tr>
<tr><td>6</td><td>#924 MRS = 0000</td><td>M/S</td><td>924-A: 1. Report printing when consolidation daily and periodic cashier reading or resetting
2. PLU save file</td><td>
<table>
<tr><td>1. Report printing when consolidation daily and periodic cashier reading or resetting is taken.</td><td>2. PLU save file</td><td>924-A</td></tr>
<tr><td rowspan="2">Printing of report on individual register</td><td>Not</td><td>0</td></tr>
<tr><td>Exist</td><td>1</td></tr>
<tr><td rowspan="2">Printing of both i.e. reports on individual machines and consolidation report on the entire system</td><td>Not</td><td>4</td></tr>
<tr><td>Exist</td><td>5</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>No.</th><th>Job#</th><th>M/S</th><th>Item</th><th>Key sequence</th></tr>
<tr><td>6</td><td>#924 MRS = 0000</td><td>M/S</td><td>924-B: 1. Save file except for PLU
2. Programming whether or not to lock REG mode entries after individual daily total resetting
1 Locking after clerk resetting
2 Locking after term clerk resetting</td><td>
<table>
<tr><th>1. Save file except for PLU</th><th>2. Locking after clerk resetting</th><th>3. Locking after term clerk resetting</th><th>924-B</th></tr>
<tr><td rowspan="4">Not</td><td rowspan="2">Yes</td><td>Yes</td><td>0</td></tr>
<tr><td>No</td><td>1</td></tr>
<tr><td rowspan="2">No</td><td>Yes</td><td>2</td></tr>
<tr><td>No</td><td>3</td></tr>
<tr><td rowspan="4">Exit</td><td rowspan="2">Yes</td><td>Yes</td><td>4</td></tr>
<tr><td>No</td><td>5</td></tr>
<tr><td rowspan="2">No</td><td>Yes</td><td>6</td></tr>
<tr><td>No</td><td>7</td></tr>
</table>
</td></tr>
<tr><td></td><td></td><td></td><td>924-C: 1. Programming whether or not to lock REG mode entries after individual daily total resetting. When the system has no save file
1 Locking after hourly resetting
2 Locking after general resetting</td><td>
<table>
<tr><th>1. Locking after hourly resetting</th><th>2. Locking after general resetting</th><th>924-C</th></tr>
<tr><td rowspan="2">Yes</td><td>Yes</td><td>0</td></tr>
<tr><td>No</td><td>1</td></tr>
<tr><td rowspan="2">No</td><td>Yes</td><td>2</td></tr>
<tr><td>No</td><td>3</td></tr>
</table>
</td></tr>
<tr><td></td><td></td><td></td><td>924-D: 1. Programming whether or not to lock REG mode entries after individual periodic total resetting. When the system has no save file
1 Locking after daily net resetting
2 Locking after general resetting</td><td>
<table>
<tr><th>1. Locking after hourly resetting</th><th>2. Locking after general resetting</th><th>924-D</th></tr>
<tr><td rowspan="2">Yes</td><td>Yes</td><td>0</td></tr>
<tr><td>No</td><td>1</td></tr>
<tr><td rowspan="2">No</td><td>Yes</td><td>2</td></tr>
<tr><td>No</td><td>3</td></tr>
</table>
</td></tr>
<tr><td>7</td><td>#925 MRS = 0000</td><td>M/S</td><td>925-A: 1. Selection of the method of daily total general consolidation resetting at the master
Method-1: Those data that has individually been reset and the current sales data are reset together
Method-2: Only those data that has individually been reset is reset
2. Clearing of the individual resetting memory at the time of consolidation daily total general resetting
Individual resetting memory=IRM
3. Execution of Job #199 when consolidation daily total general resetting has not been taken.</td><td>
<table>
<tr><th>1. Selection of the method of the daily total general consolidation resetting at the master</th><th>2. Clearing of the IRM</th><th>3. Execution of Job#199</th><th>925-A</th></tr>
<tr><td rowspan="4">Method-1</td><td rowspan="2">Yes</td><td>Disable</td><td>0</td></tr>
<tr><td>Enable</td><td>1</td></tr>
<tr><td rowspan="2">No</td><td>Disable</td><td>2</td></tr>
<tr><td>Enable</td><td>3</td></tr>
<tr><td rowspan="4">Method-2</td><td rowspan="2">Yes</td><td>Disable</td><td>4</td></tr>
<tr><td>Enable</td><td>5</td></tr>
<tr><td rowspan="2">No</td><td>Disable</td><td>6</td></tr>
<tr><td>Enable</td><td>7</td></tr>
</table>
</td></tr>
<tr><td></td><td></td><td></td><td>925-B: 1. Any entry operation is inhibited until Job #199 is executed after consolidation daily total general resetting has been taken.
2. Various individal resetting.</td><td>
<table>
<tr><th>1. Any entry operation is inhibited until job#199</th><th>2. Various individual resetting</th><th>925-B</th></tr>
<tr><td rowspan="2">Yes</td><td>Disable</td><td>0</td></tr>
<tr><td>Enable</td><td>1</td></tr>
<tr><td rowspan="2">No</td><td>Disable</td><td>2</td></tr>
<tr><td>Enable</td><td>3</td></tr>
</table>
</td></tr>
<tr><td></td><td></td><td></td><td>925-C: 1. Report printing when consolidation daily and periodic total general reading or resetting is taken.</td><td>
<table>
<tr><th>1. Report printing</th><th>925-C</th></tr>
<tr><td>Both i. e. report on individual machines and Consolidation report on the entire system.</td><td>0</td></tr>
<tr><td>Consolidation report on the entire system</td><td>1</td></tr>
<tr><td>Report on individual register</td><td>2</td></tr>
</table>
</td></tr>
</table>

No.	Job#	M/S	Item	Key sequence
7	#925 MRS = 0000	M/S	925-D: 1. PLU stock control system 2. Resetting in the open store state.	

1. PLU stock control system	2. Resetting in the open store state	925-D
Centralized	Disable	0
	Enable	1
Individual	Disable	2
	Enable	3

<<Detailed descriptions of the parameter for Job #925>>

925-A 1 Method of daily general resetting of the entire system at the master:
It is specified whether only those data that has individually been reset or that data and the current sales data should be reset when resetting of the entire system is take.
Note here that if the machine is programmed to disable individual resetting (by B of SRV-mode programming Job #925), not only individual resetting but also resetting of the entire system cannot be achieved unless "Those data that has individually been reset and the current sales data are reset together" has been selected.

2 Automatic clearing of the individual resetting memory at the time of consolidation daily total general resetting No/Yes
The machine can be programmed to clear the individual resetting memory when general Z1 resetting of the entire system is taken. If the memory is not cleared data is accumulated each time individual resetting is taken until job #99 is executed.

3 Execution of Job #99 when consolidation daily total general resetting has not been taken Enable/Disable:
Job #99 can be executed even if general Z1 resetting of the entire system is not taken.

925-B 4 Any entry operation is inhibited until Job #99 is executed after consolidation or individual daily total general resetting has been taken No/Yes:
This parameter enables the master to restrict the resetting job at satellites.

5 Individual resetting Enable/Disable:
The master alone can be made capable of resetting by selecting "Disable".
When selecting "Enable", or "Disable", however, the selection of the resetting method mentioned 1 above should well be noted.

925-C 6 Type of printing of daily total and periodic total general X/Z reports:
The following three types are available:
a) Printing of only X/Z reports on individual machines
b) Printing of a consolidation X/Z report only
c) Printing of X/Z reports on individual machines, followed by the printing of a consolidation X/Z report

Note: This programming 1 - 4 is valid for the system that has the save file.
Reading of SRV-mode program data

925-D 7 PLU stock control in the inline system
a) Stock control in inline system is available in two types: individual and centralized systems.
b) Centralized stock control system
Program data only stock is only stored in the master.
Stock data in each satellite must be zero before a stock entry is made.
When a consolidaton report is taken, stock data in respective satellites are consolidated and is add to stock data in the master.
Then the sum is printed.
Stock data in each satellite is reset to zero at this time.

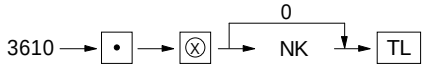
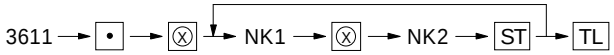
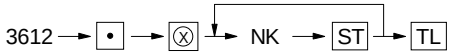
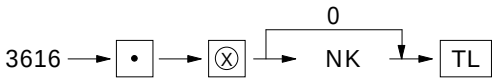
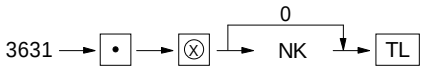
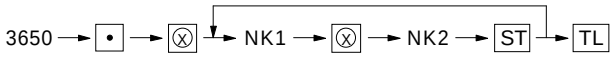
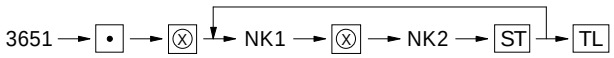
Notice) In this system, stock counter in each satellite is always negative.
So, Entry which makes the PLU stock counter negative must be Allowed unconditionally. (SRV. JOB#906-A)

c) Individual control system
Program data on stock is stored in the master and stellites, respectively.
When a consolidation report is taken, stock data in the master and satellites is consolidated and printed.
The consolidation does not affect the stock data in the master.

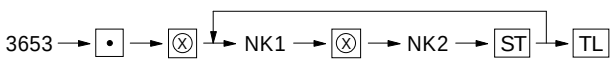
<table>
<tr><th>No.</th><th>Job#</th><th>M/S</th><th>Item</th><th>Key sequence</th></tr>
<tr><td>8</td><td>#926 MRS=0004</td><td>M/S</td><td>926-A: 1. Sending "last void data" on KP
2. Sending "past void data" on KP</td><td>
<table>
<tr><th>1. Sending "last void data" on KP</th><th>2. Sending "past void data" on KP</th><th>926-A</th></tr>
<tr><td rowspan="2">Yes</td><td>Yes</td><td>0</td></tr>
<tr><td>No</td><td>1</td></tr>
<tr><td rowspan="2">No</td><td>Yes</td><td>2</td></tr>
<tr><td>No</td><td>3</td></tr>
</table>
</td></tr>
<tr><td></td><td>M/S</td><td>926-B: 1. Program reset in PGM2 mode
2. Sending "refund data" on KP</td><td>
<table>
<tr><th>1. Program reset in PGM2 mode</th><th>2. Sending "refund data" on KP</th><th>926-B</th></tr>
<tr><td rowspan="2">Disable</td><td>Yes</td><td>0</td></tr>
<tr><td>No</td><td>1</td></tr>
<tr><td rowspan="2">Enable</td><td>Yes</td><td>2</td></tr>
<tr><td>No</td><td>3</td></tr>
</table>
</td></tr>
<tr><td></td><td>M/S</td><td>926-C:</td><td>Not used (Fixed at "0")</td></tr>
<tr><td></td><td></td><td>926-D: 1. Dept./PLU text printing
2. Check VP</td><td>
<table>
<tr><th>1. Dept./PLU text printing</th><th>2. Check VP format</th><th>926-D</th></tr>
<tr><td rowspan="4">Normal</td><td>Normal</td><td>0</td></tr>
<tr><td>Euro check</td><td>1</td></tr>
<tr><td>French check</td><td>2</td></tr>
<tr><td>German check</td><td>3</td></tr>
<tr><td rowspan="4">Double</td><td>Normal</td><td>4</td></tr>
<tr><td>Euro check</td><td>5</td></tr>
<tr><td>French check</td><td>6</td></tr>
<tr><td>German check</td><td>7</td></tr>
</table>
</td></tr>
<tr><td>9</td><td>#931 MRS=0000
#937 MRS=0000</td><td>M/S</td><td>931: CONSOLIDATION Z1 COUNTER
937: CONSOLIDATION Z2 COUNTER</td><td>931 → [•] → [Ⓧ] → XXXX → [TL]
937
XXXX: Inital value for the counter.</td></tr>
<tr><td>10</td><td>#897</td><td>M/S</td><td>Inline system in which kitchen printers alone are connected.
• Function
a) In this inline system any inline job (consolidation, down-loading, UP-loading, etc) is inhibited.
b) SRV parameter JOB#922 is set to "0008" programming of the terminal number of the master. K.P. preset file and K.P. edit buffer is created. The above jobs, etc are performed.
c) The above system requires the following selection in programming JOB#920-D. Register is standalone. =0</td><td>897 → [•] → [Ⓧ] → [TL]</td></tr>
<tr><td>11</td><td>#898</td><td>M/S</td><td>Inline resetting
• Function
This operation clears only the work memory for inline operations.
The program memory for inline operations re-mained uncharged even after the resetting here is performed.
Inline communications can also be achieved.</td><td>898 → [•] → [Ⓧ] → [TL]</td></tr>
</table>

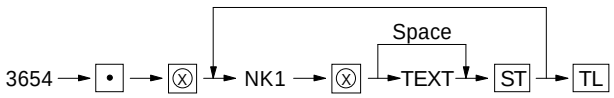
No.	Job#	M/S	Item	Key sequence
12	#899	M/S	Clearing the memories for inline operations. ● Function This operation clears all the inline program data memory and work memory. After carrying out this clearing operation, any inline communication is inhibited until the necessary data for inline operations are re-programmed. This function automatically create the inline files by following SRV preset. MASTER MACHINE : (SRV #920 D=2) Consolidation file and the receive file is created. When clerk file is centraized, SIGN ON/OFF CLERK file is created. BACKUP MASTER MACHINE : (SRV #920 D=3) RECEIVE GLU BUFFER is created. When clerk file is centraized, SIGN ON/OFF CLERK file is created. When system report/downloading job is possible on backup master, consolidation file and the receive file is created. All machine : When the system has the save file, the save file is created. File area is shifted to secure the work memory for inline operation. The "in use" flag of the clerk program data file is cleared. (at the master) All records in the clerk program data file are erased. (at the satellite)	899 → [•] → [⊗] → [TL]
13	#895	M/S	Set ip 1 job operation	Refer to CHAPTER 10.

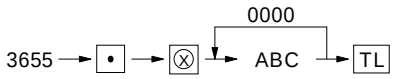
CHAPTER 7. PGM2 MODE PROGRAMMING

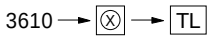
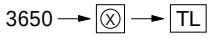
No.	Job#	M/S	Item	Key sequence
1.	#3610	M/S	• Terminal number	 NK: Terminal No. = 0 ~ 254
2.	#3611	M	• Master list (Generation)	 NK1: Terminal No. = 1 ~ 254 NK2: Register No. = 1 ~ 999999
3.	#3612	M	• Master list (Delection)	 NK: Register No. = 1 ~ 999999
4.	#3616	M	• Terminal number of the quest check file buck-up master.	 NK: Machine No. = 1 ~ 999999 NK = 0: When the back up master does not exist in the inline system. MRS = 0
5.	#3631	M	• Decide whether to enable or disable the manager retry function when a transmission error occurs	 NK:0 = Manager retry function ENABLE 1 = Manager retry function DISABLE MRS = 0
6.	#3650	M/S	• Terminal number of K.P. K.P.=Kitchine printer	 NK1: K.P. No. = 1 ~ 9 NK2: Terminal No. = 0 ~ 254 ∗ NK2 = 0: When the K.P. deletion
7.	#3651	M/S	• Data transmission of K.P.	 NK1: K.P. No. = 1~9 NK2:

Data transmission	NK2
Enable	0
Disable	1

8.	#3653	M/S	• Second K.P. No.	 NK1: K.P. No. = 1 ~ 9 NK2: Second K.P. No. = 1 ~ 9 ∗ NK2 = 0: When the non second K.P.

<table>
<tr><th>No.</th><th>Job#</th><th>M/S</th><th>Item</th><th>Key sequence</th></tr>
<tr><td>9.</td><td>#3654</td><td>M/S</td><td>• K.P. name</td><td> 

NK 1: K.P. No. = 1~9
TEXT: Max. 12character</td></tr>
<tr><td>10.</td><td>#3655</td><td>M/S</td><td>• Print format for K.P.</td><td> 

A:
<table>
<tr><th>PLU/DEPT code</th><th>A</th></tr>
<tr><td>Print</td><td>0</td></tr>
<tr><td>Skip</td><td>1</td></tr>
</table>
C:
<table>
<tr><th>Amount</th><th>C</th></tr>
<tr><td>Print</td><td>0</td></tr>
<tr><td>Skip</td><td>1</td></tr>
</table>
B:
<table>
<tr><th>Unit price</th><th>B</th></tr>
<tr><td>Print</td><td>0</td></tr>
<tr><td>Skip</td><td>1</td></tr>
</table></td></tr>
<tr><td>11.</td><td>#3610</td><td>M/S</td><td>• Inline preset reading</td><td> 
</td></tr>
<tr><td>12.</td><td>#3650</td><td>M/S</td><td>• Kitchen printer preset reading</td><td> 
</td></tr>
</table>

CHAPTER 8. TROUBLE SHOOTING JOBS

M : Master
S : Satellite
BM : Backup master

No.	JOB#	ITEM	MODE	S/M	KEY SEQUENCE
1	#5810	Master declaration	PGM2	BM/M	5810 → [•] → [Ⓧ] → [TL]
2	#5820	Recover declaration	PGM2	BM/M	5820 → [•] → [Ⓧ] → [TL]
3	#5940	Clerk preset file in use flag foreed to clear	PGM2	M	5940 → [•] → [Ⓧ] → [TL]
4	#5990	All item sales data memory manual clear	PGM2	M/S	5990 → [•] → [Ⓧ] → [TL]
5	#5994	Clerk sales data memory manual clear	PGM2	M/S	5994 → [•] → [Ⓧ] → NK → [TL] NK : Clerk No.
6	#5996	Hourly sales data memory manual clear	PGM2	M/S	5996 → [•] → [Ⓧ] → [TL]
7	#5997	Daily net sales data memory manual clear	PGM2	M/S	5997 → [•] → [Ⓧ] → [TL]
8	#5700	Sign on clerk report	PGM2	M/S	5700 → [•] → [Ⓧ] → [TL]

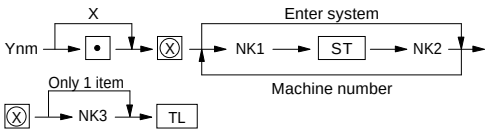
CHAPTER 9. READING (X) AND RESETTING (Z) REPORTS

(1) Job #Ynm: Y = 1 when the master is in the X1/Z1 mode.
Y = 2 when the master is in the X2/Z2 mode.

(2) Master consolidation report command entry sequence

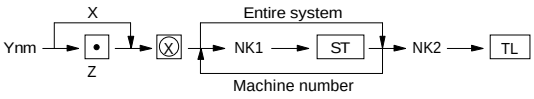
(a) To specify a range

NK1 : Machine number
NK2 : START number
NK3 : END number



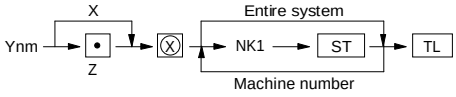
(b) To specify a department or group

NK1 : Machine number
NK2 : DEPT number



(c) To specify nothing

NK1 : Machine number



(3) Individual report command entry sequence

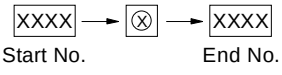
The same key operation as the standalone is required for entry of an individual report JOB#.

(4) Syetem sales report for master/backup master

	MODE ∗1								
	OP X/Z		X1/Z1		X2/Z2		∗3 DATA FOR		
REPORT NAME	X	Z	X1	Z1	X2	Z2	JOB#	READING	NOTE
GENERAL			Φ	Φ	Φ	Φ	1 x 00	—	
DEPT/GROUP			Φ		Φ		1 x 10	—	
IND. GROUP			Φ		Φ		1 x 12	GROUP No	
GROUP TOTAL			Φ		Φ		1 x 13	—	
PLU BY RANGE			Φ	Φ	Φ	Φ	1 x 20	PLU CODE	∗2
PLU BY DEPT			Φ	Φ	Φ	Φ	1 x 21	DPT CODE	
PLU IND. GR.			Φ		Φ		1 x 22	GROUP No	
PLU GR. TL			Φ		Φ		1 x 23	—	
PLU STOCK			Φ				1 x 24	PLU CODE	∗2
PLU ZERO SALES			Φ		Φ		1 x 27	ALL	
PLU ZERO SALES BY DEPT			Φ		Φ		1 x 27	DPT CODE	
PLU MINIMUM STOCK			Φ				1 x 28	ALL	
TRANSACTION			Φ		Φ		1 x 30	—	
TL-ID			Φ				1 x 31	—	
COMMISSION SALES			Φ		Φ		1 x 32	—	
TAX			Φ		Φ		1 x 32	—	
CHIFF			Φ				1 x 34	—	
ALL CLERK			Φ	Φ	Φ	Φ	1 x 40	—	
IND. CLERK	Φ	Φ	Φ	Φ	Φ	Φ	1 x 41	∗4	
HOURLY (ALL)			Φ	Φ			1 x 60		
(RANGE)			Φ				1 x 60	∗2	
DAILY NET					Φ	Φ	1 x 70		
GLU			Φ	Φ			1 x 80	∗2	
GLU BY CLERK			Φ	Φ			1 x 81		
BALANCE			Φ		Φ		1 x 82		
STACKED REP			Φ	Φ	Φ	Φ	1 x 90 – 1 x 91		
Reset clear				Φ		Φ	1 x 99		

∗1 X1 : Daily X report Z1 : Daily Z report
X2 : Preriodic X report Z2 : Periodic Z report

∗2 The time interval range, or PLU code range can be specified by entering the start and end numbers according to the following procedure. When specifying a single time interval, PLU code, the start number has only to be entered.



Stop of printing reports: These system reports do not execute this specification.

∗3 When 1 is entered in the forth digit of a job code, Inline system reports are printed.

Example: System daily general report; job code 1100
System periodic general report; job code 1200

∗4 In case of floating clerk system, this daily report can be printed at any satellite.
(The periodic report can not be printed at any satellite.)

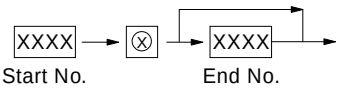
(5) Individual report jobs for the master/backup master/satellite

	MODE ∗1								
	OP X/Z		X1/Z1		X2/Z2		∗3 DATA FOR		
REPORT NAME	X	Z	X1	Z1	X2	Z2	JOB#	READING	NOTE
GENERAL			Φ	Φ	Φ	Φ	00	—	
DEPT/GROUP			Φ		Φ		10	—	
IND. GROUP			Φ		Φ		12	GROUP No	
GROUP TOTAL			Φ		Φ		13	—	
PLU BY RANGE			Φ	Φ	Φ	Φ	20	PLU CODE	∗2
PLU BY DEPT			Φ	Φ	Φ	Φ	21	DPT CODE	
PLU IND. GR.			Φ		Φ		22	GROUP No	
PLU GR. TL			Φ		Φ		23	—	
PLU STOCK			Φ				24	PLU CODE	∗2
PLU ZERO SALES			Φ		Φ		27	ALL	
PLU ZERO SALES BY DEPT			Φ		Φ		27	DPT CODE	
PLU MINIMUM STOCK			Φ				28	ALL	
TRANSACTION			Φ		Φ		30	—	
TL-ID			Φ				31	—	
COMMISSION SALES			Φ		Φ		32	—	
TAX			Φ		Φ		33	—	
CHIFF			Φ				34	—	
ALL CLERK			Φ	Φ	Φ	Φ	40	—	∗4
IND. CLERK	Φ	Φ	Φ	Φ	Φ	Φ	41	—	∗4
HOURLY (ALL)			Φ	Φ			60		
(RANGE)			Φ				60		*2
DAILY NET					Φ	Φ	70		
GLU			Φ	Φ			80	∗2	
GLU BY CLERK			Φ	Φ			81		
BALANCE			Φ		Φ		82		
STACKED REP			Φ	Φ	Φ	Φ	90 – 91		

∗1 X1 : Daily X report Z1 : Daily Z report

X2 : Preriodic X report Z2 : Periodic Z report

∗2 The time interval range, or PLU code range can be specified by entering the start and end numbers according to the following procedure. When specifying a single time interval, PLU code, the start number has only to be entered.



∗3 When 2 is enterd in the third digit of a job code, periodic reports are printed.

Example: Daily general report; job code 100
Periodic general report; job code 200

∗4 In case of clerk centrized, this report can not be printed at master/backup master/satellites.

CHAPTER 10. SOFTWARE INSTALLATION PROCEDURE FOR IN-LINE SYSTEM

1. SATELLITE

SRV

1) 902 → [•] → [⊗] → 1XXX → [TL] ; INLINE YES
2) 920 → [•] → [⊗] → 1 → [TL] ; SATELLITE MACHINE.
3) 899 → [•] → [⊗] → [TL] ; INLINE RAM CLEAR.

PGM2

4) 2612 → [•] → [⊗] → M-No. → [TL] ; OWN MACHINE NO.
5) 3610 → [•] → [⊗] → T-No. → [TL] ; OWN TERMINAL NO.

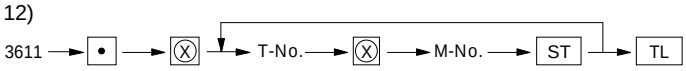
2. MASTER

SRV

6) 902 → [•] → [⊗] → 1XXX → [TL] ; INLINE YES
7) 920 → [•] → [⊗] → 2 → [TL] ; MASTER MACHINE.
8) Programs the other necessary SRV JOBs (#924,925)
9) 899 → [•] → [⊗] → [TL] ; INLINE RAM CLEAR

PGM

10) 2612 → [•] → [⊗] → M-No. → [TL] ; OWN MACHINE NO.
11) 3610 → [•] → [⊗] → T-No. → [TL] ; OWN TERMINAL NO.
12) ; MACHINE MASTER LIST



13) Programs the other necessary PGM JOBs.
14) 4900 → [•] → [⊗] → [TL] ; DOWN LOADING (IN-LINE PARAMETER DATA)
(ALL PRESET DATA)

SRV

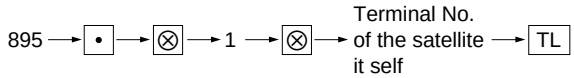
15) 800 → [•] → [⊗] → [TL] ; DOWN LOADING (SRV PARAMETER)
16) 850 → [•] → [⊗] → [TL] ; DOWN LOADING (KEYBOARD)

PGM

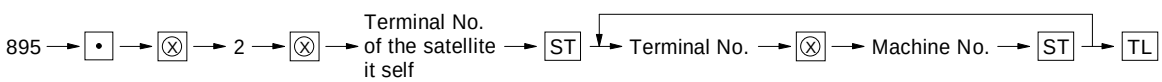
17) 4999 → [•] → [⊗] → [TL] ; DOWN LOADING (ALL PGM PRESETS)

3. Set-up 1 job operation

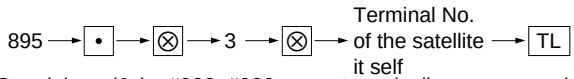
1) Satellite (Jobs #902, #920, #899, and #3610 are auto-matically programmed.) must do PGM JOB#2612.



2) Master (Jobs #902, #920, #899, #3610, #3611, and #4900 are automatically programmed.) must do PGM JOB#2612.



3) Back-up master (Jobs #902, #920, #899 and #3610 are auto-matically programmed.) ,mast do PGM JOB#2612.



4) Standalone (Jobs #902, #920 are automatically programmed.) must do PGM JOB#2612.

895 → [•] → [⊗] → [TL]

II. RS-232 SYSTEM FOR ER-A570

ER-A5RS

MODEL ER-A57R1 (For ER-A570)

(OPTION FOR ER-A570)

CONTENTS

■ WHAT IS AN RS-232 INTERFACE?

- EIA (Electronics Industries Association) standard RS-232 is associated with the transfer of binary serial data, control signals and timing signals between modems and data terminals.
- The RS-232 interface is one of the devices generally used for the exchange of information between a computer and a peripheral device.
- This interface (ER-A5RS) was designed to conform to the EIA standard, but in particular it was designed for connection between the ER-A570 and a data processing machine.
- It becomes necessary to set communication specifications of the ER-A5RS (e.g. baud rate) matched to those of the data processing machine, when the ER-A5RS is connected with a data processing machine that is equipped with the RS-232 interface.
- The Dip switch on the ER-A5RS interface circuit board must be used to choose the specifications.
- Refer to Section 3 "RS-232 Interface Specifications" for details of communication specifications.

CHAPTER 1. GENERAL

This option (ER-A57R1 and ER-A5RS) is the RS-232 interface option for the ER-A570 cash register. It enables the ER-A570 to perform on-line data communications.
When this option is used for on-line data communications, the ER-A570 can be connected to a host computer. Also, their connection can be made via modems.
When this option is used together with a multiplexer (to be procured in the market), it allows the host computer to be connected to more than one ER-A570.

CHAPTER 2. COMPONENTS

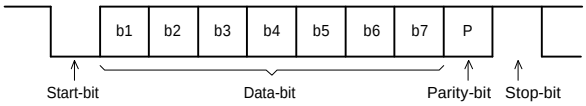
ER-A5RS

NO	NAME	PARTS CODE	Q'ty
1	PWB UNIT	CPWBS7292RC01	1
2	BRACKET	LANGT7466RCZZ	1
3	SCREW (FOR PWB AND BRACKET)	LX–BZ6665RCZZ	2
4	SCREW (FOR HOLDING OF THE PWB BRACKET, AND BRACKET TO BRACKET)	LX–BZ6774RCZZ	3
5	SCREW (FOR HOLDING OF THE RS-232 CABLE CORE)	XHBSD30P08000	2
6	WIRING TIE	LBNDJ2004SCZZ	1
7	CLAMP (FOR RS-232 CABLE)	LHLDW6814RCZZ	2
8	SPACER	PSPAN7039XCZZ	1
9	FERRITE CORE (FOR EXTERNAL CABLE)	RCORF6658RCZZ	2

CHAPTER 3. SPECIFICATIONS OF RS-232 INTERFACE

1. Online interface

a) Interface : RS-232
b) Duplex type : Half-duplex / Full-duplex
c) Line configuration : Direct connection/Modem connection
d) Data rate : 19200, 9600, 4800, 2400, 1200, 600 and 300 bps (Programable)
e) Synchronizing mode : Asynchronous
f) Parity check : Vertical parity check (odd)
g) Code : ASCII
h) Bit sequence : LSB first
i) Data format : 1 start bit + 7 data bits + 1 parity + 1 stop bit



j) Protocol : Polling/selecting (Simple procedure)
k) Transmission line :
Cable : Shielded cable
Connector (ECR side) : D-sub 9 pin (female type) connector Inch pitch (4-40 UNC) lock screw
Connector cover : Shielded cover

The table shows the relationship between the data rate and the recommended cable length.

Data rate	Recommended cable length
19,200 bps	3.75 meters
9,600 bps	7.5 meters
4,800 bps	15 meters
2,400 bps	30 meters
1,200 bps	60 meters

CHAPTER 4. BLOCK DIAGRAM AND SYSTEM CONFIGURATION

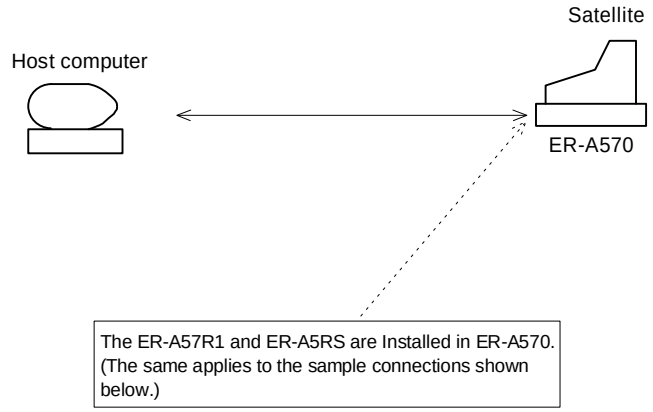
1. System Configuration

1) On-line data communication

On-line data communication is allowed only when the ER-A570 is a stand-alone machine or an in-line master. The protocol is the simple procedure. (The on-line option is not usable if the ER-A570 is an in-line satellite.)

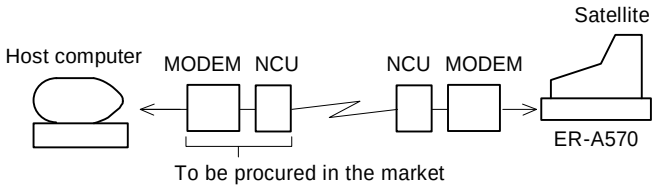
1 **Direct connection**

a) One-to-one connection

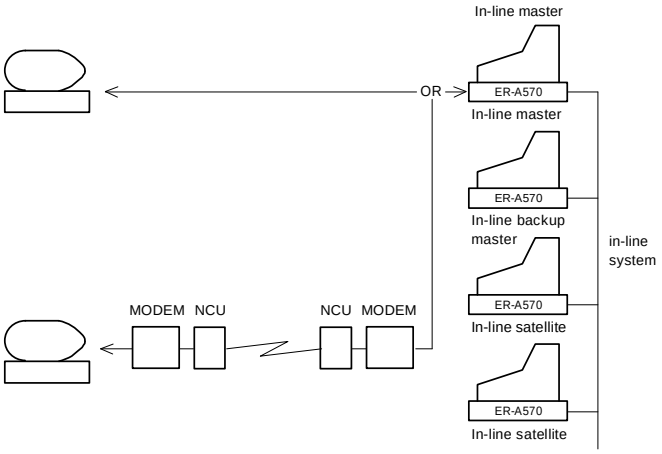


2 **Connection via modems**

a) One-to-one connection

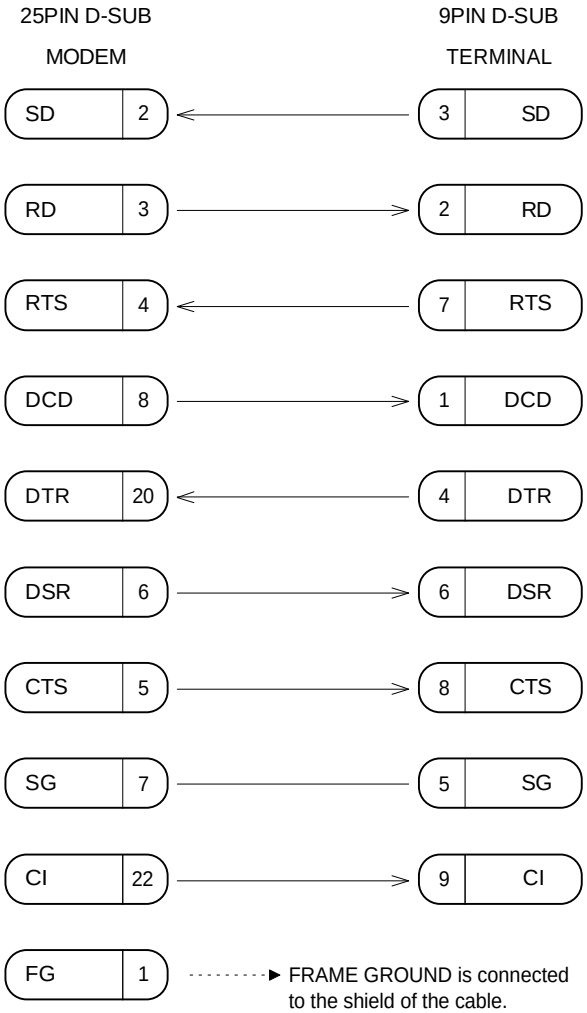


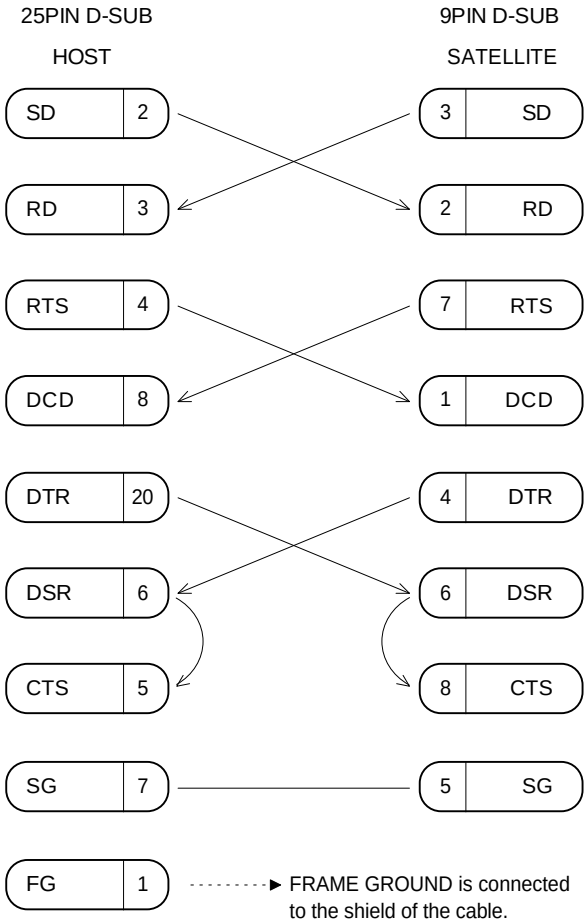
2) On-line data communication and in-line system connection



* The ER-A6IN is required for the inline (SRN) system.

CHAPTER 5. SIGNAL CONNECTION





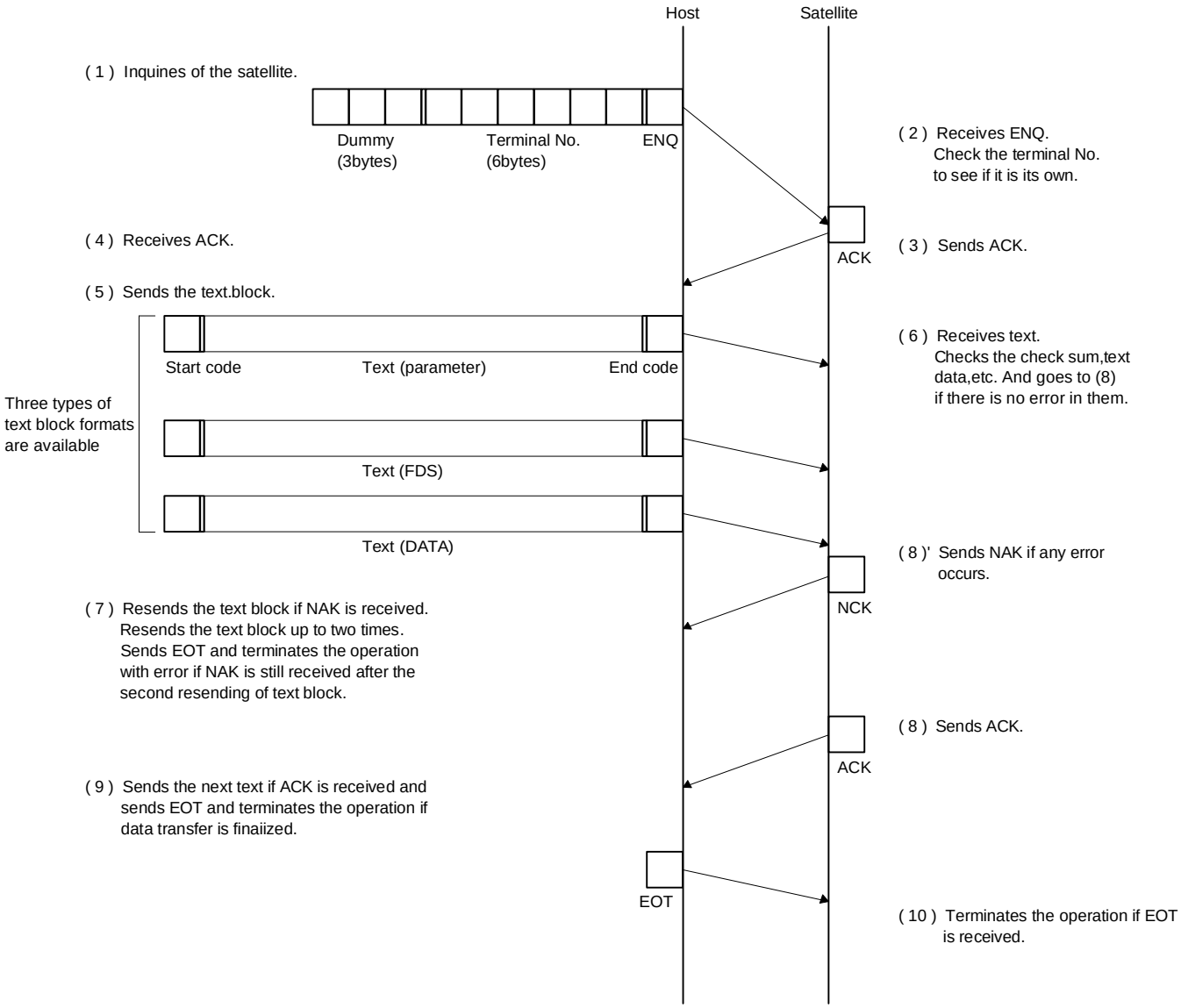
SD : TRANSMITTED DATA
RD : RECEIVED DATA
DTR : DATA TERMINAL READY
DSR : DATA SET READY
RTS : REQUEST TO SEND
DCD : DATA CARRIER DETECTOR
CTS : CLEAR TO SEND
FG : FRAME GROUND

DIAGRAM

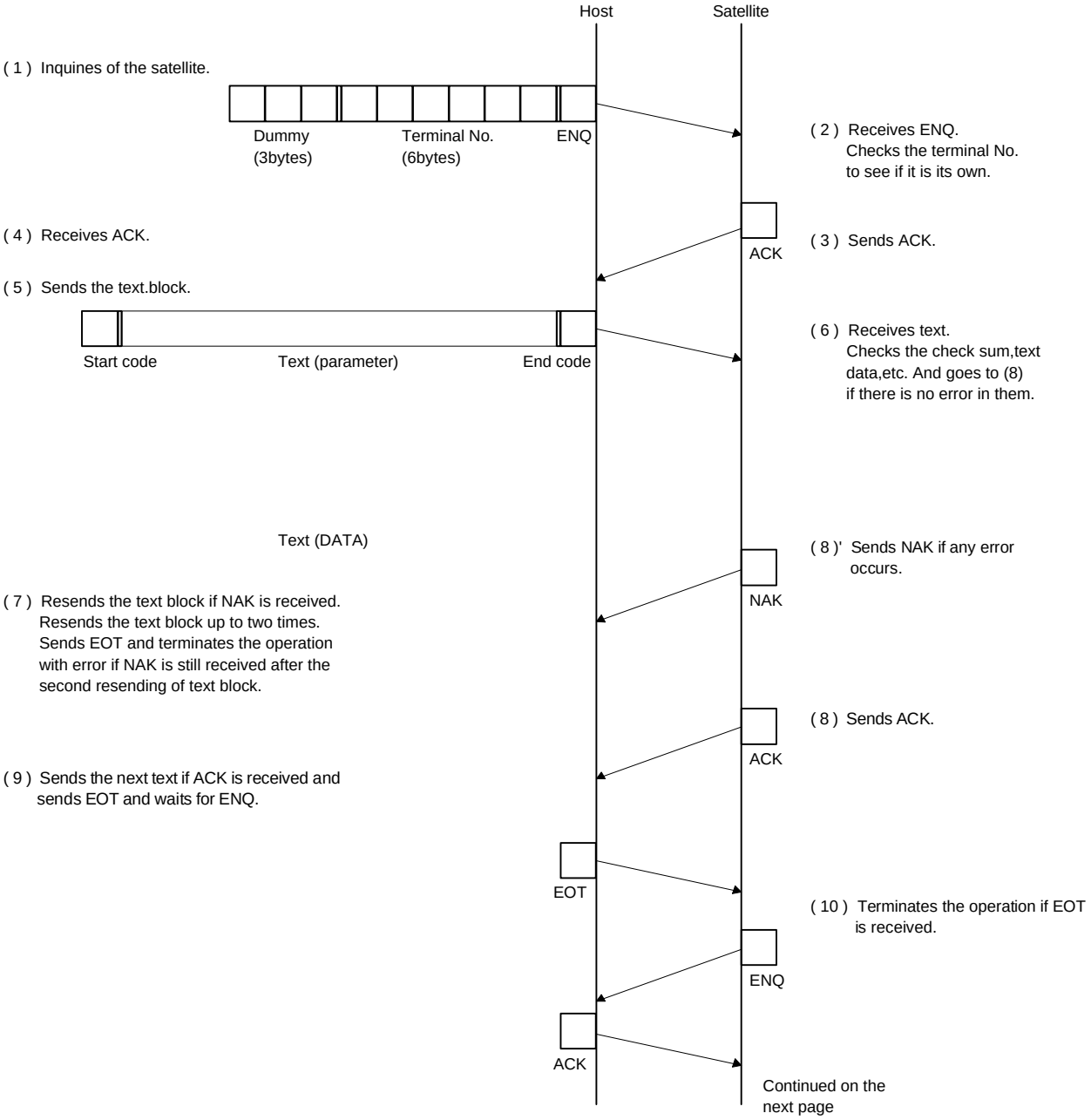
1. Connection between the master (Host) and Satellite

2. Connection between the terminal and MODEM

SD : TRANSMITTED DATA
RD : RECEIVED DATA
DTR : DATA TERMINAL READY
DSR : DATA SET READY



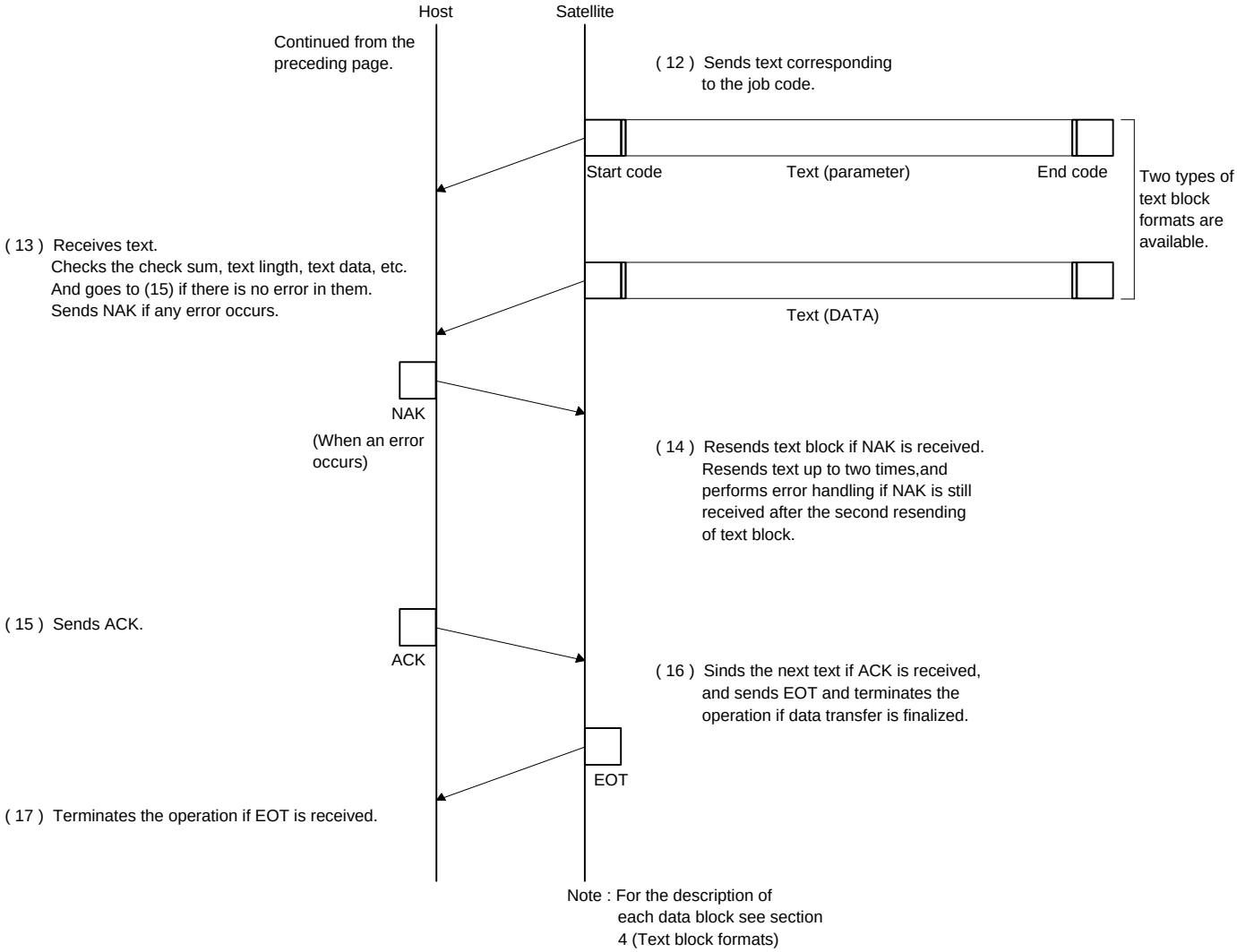
RTS : REQUEST TO SEND
DCD : DATA CARRIER DETECTOR
CTS : CLEAR TO SEND
CI : CALLING INDICATOR
FG : FRAME GROUND



CHAPTER 6. RS-232 PROTOCOL

1. Basic protocol specification

1) Data transmission from the host to a satellite



2) Data transmission from satellite to the host

2. Transmission control procedure matrix

1) Down-loading matrix for the host

STATE / EVENT	Initial	After sending ID ENQ	After sending text
	0	1	2
ENQ	—	—	—
ACK	—	Sends text and goes to 2.	Sends text and goes to 2. Sends EOT and then goes to 0. (Normal end)
NAK	—	—	Resends the text and then goes to 2. If the host has resent the text two times, it sends EOT and goes to 0. (ERROR END)
EOT	—	—	The host goes to 0. (ERROR END)
TEXT	—	—	—
TIME-UP	—	Resends ID ENQ and then goes to 1. If the host has resent ID ENQ two times,it sends EOT and goes to 0. (ERROR END)	Resends the text and then goes to 2. If the host has resent the text two times,it sends EOT and goes to 0. (ERROR END)
KEY ENTRY	Sends ID ENQ and goes to 1.	—	—

Time-up: One second after sending of ID ENQ.
Four seconds after sending of text.

2) Up-loading matrix for the host

STATE / EVENT	Initial	After sending ID ENQ	After sending text
	0	1	2
ENQ	—	—	—
ACK	—	Sends text and goes to 2.	Sends EOT and goes to 3.
NAK	—	—	Resends the text and then goes to 2. If the host has resent the text two times, it goes to 0. (ERROR END)
EOT	—	—	The host goes to 0. (ERROR END)
TEXT	—	—	—
TIME-UP	—	Resends ID ENQ and then goes to 1. If the host has resent ID ENQ two times, it goes to 0. (ERROR END)	Resends the text and then goes to 2. If the host has resent the text two times, it goes to 0. (ERROR END)
KEY ENTRY	Sends ID ENQ and goes to 1.	—	—

Time-up: One second after sending of ID ENQ.
Four seconds after sending of text.

STATE / EVENT	After sending EOT	After sending ACK	After sending NAK
	3	4	5
ENQ	Sends ACK and goes to 4.	After the host has received ENQ, resends ACK and goes to 4. After the host has received TEXT, ignores the ENQ.	—
ACK	—	—	—
NAK	—	—	—
EOT	The host goes to 0 (ERROR END)	After the host has received TEXT, goes to 0. (Normal end) After the host has received ENQ, goes to 0.(ERROR END)	The host goes to 0. (ERROR END)
TEXT	—	The host checks the text block, if the block is correct, the host sends ACK and goes to 4. If it is not correct, the host sends NAK and goes to 5. If transmission cannot be continued, the host sends EOT and goes to 0.	The host checks the checks the text block, if the block is correct, the host sends ACK and goes to 4. If it is not correct, the host sends NAK and goes to 5. If transmission cannot be continued, the host sends EOT and goes to 0. (ERROR END)
TIME-UP	Resends EOT and goes to 3. If the host has resent the EOT two times, it goes to 0. (ERROR END)	The host goes to 0. (ERROR END) Time-up is 7 seconds	The host goes to 0. (ERROR END) Time-up is 7 seconds
KEY ENTRY	—	—	—

Time-up: Two second after sending of EOT.

3) Down-loading matrix for the sattelite

STATE / EVENT	Initial	After sending ACK	After sending NAK
	0	1	2
ID-ENQ	Satellite checks the terminal No.:If it is correct, satellite sends ACK and goes to 1. If it is not correct, Satellite ignores the ID-ENQ.	Satellite checks the terminal No.:If it is correct, satellite sends ACK and goes to 1. If it is not correct, Satellite ignores the ID-ENQ.	—
ACK	—	—	—
NAK	—	—	—
EOT	—	After satellite has received TEXT, goes to 0. (Normal end) Before satellite has received TEXT, ignores the EOT	Satellite goes to 0. (ERROR END)
TEXT	—	Satellite checks the text block, if the block is correct, Satellite sends ACK and goes to 1. If it is not correct, satellite sends NAK and goes to 2. If transmission cannot be continued, satellite sends EOT and goes to 0. (ERROR END)	Satellite checks the text block, if the block is correct, Satellite sends ACK and goes to 1. If it is not correct, satellite sends NAK and goes to 2. If transmission cannot be continued, satellite sends EOT and goes to 0. (ERROR END)
TIME-UP	—	Satellite sends EOT, and goes to 0. (ERROR END) Time-up is 7 secondsThe host goes to 0.	The host goes to 0. (ERROR END) Time-up is 7 seconds

4) Up-loading matrix for the satellite

STATE / EVENT	Initial	After receiving ID-ENQ and sending ACK.	After sending NAK
	0	1	2
ID-ENQ	Satellite checks the terminal No.:If it is correct, satellite sends ACK and goes to 1. If it is not correct, satellite ignores the ID-ENQ.	Satellite checks the terminal No.:If it is correct, satellite sends ACK and goes to 1. If it is not correct, satellite ignores the ID-ENQ.	—
ACK	—	—	—
NAK	—	—	—
EOT	—	—	Satellite goes to 0. (ERROR END)
TEXT	—	Satellite checks the text block, if the block is correct, satellite sends ACK and goes to 3. If it is not correct, Satellite sends NAK and goes to 2. If transmission cannot be continued, satellite sends EOT and goes to 0. (ERROR END)	Satellite checks the text block, if the block is correct, Satellite sends ACK and goes to 3. If it is not correct, Satellite sends NAK and goes to 2. If transmission cannot be continued, satellite sends EOT and goes to 0. (ERROR END)
TIME-UP	—	Satellite goes to 0. (ERROR END) Time-up is 7 seconds	Satellite goes to 0. (ERROR END) Time-up is 7 seconds

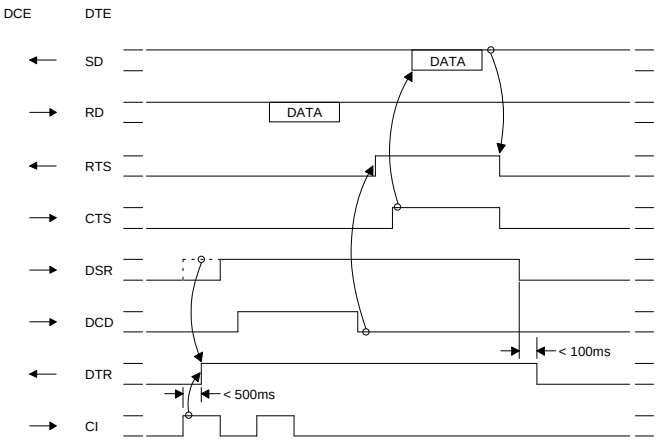
STATE / EVENT	After receiving text and sending ACK	After sending ENQ	After sending TEXT
	3	4	5
ID-ENQ	—	—	—
ACK	—	Satellite sends the text and goes to 5.	Satellite sends the text and goes to 5, or sends the EOT and goes to 0. (Normal END)
NAK	—	—	Resends the text and then goes to 5. If satellite has resent the text two times, sends EOT and goes to 0. (ERROR END)
EOT	Satellite sends ENQ and goes to 4.	Resends the ENQ and then goes to 4. If Satellite has resent the ENQ two times, sends EOT and goes to 0. (ERROR END)	Satellite goes to 0. (ERROR END)
TEXT	Satellite checks the text block, if the block is correct, satellite sends ACK and goes to 3. If it is not correct, satellite sends NAK and goes to 2. If transmission cannot be continued, satellite sends EOT and goes to 0. (ERROR END)	—	—
TIME-UP	The host goes to 0. (ERROR END) Time-up is 7 seconds	Resends the ENQ and then goes to 4. If satellite has resent the ENQ two times, sends EOT and goes to 0. (ERROR END)	Resends the text and then goes to 5. If satellite has resent the text two times, sends EOT and goes to 0. (ERROR END)

Time-up: Four seconds after sending of text.
Two second after sending of ENQ.

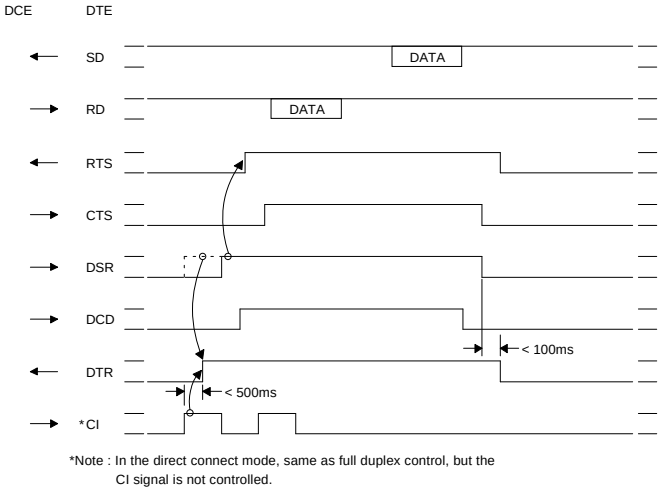
CHAPTER 7. CONTROL SIGNAL SEQUENCE

1. Online transmission

1) Half duplex transmission



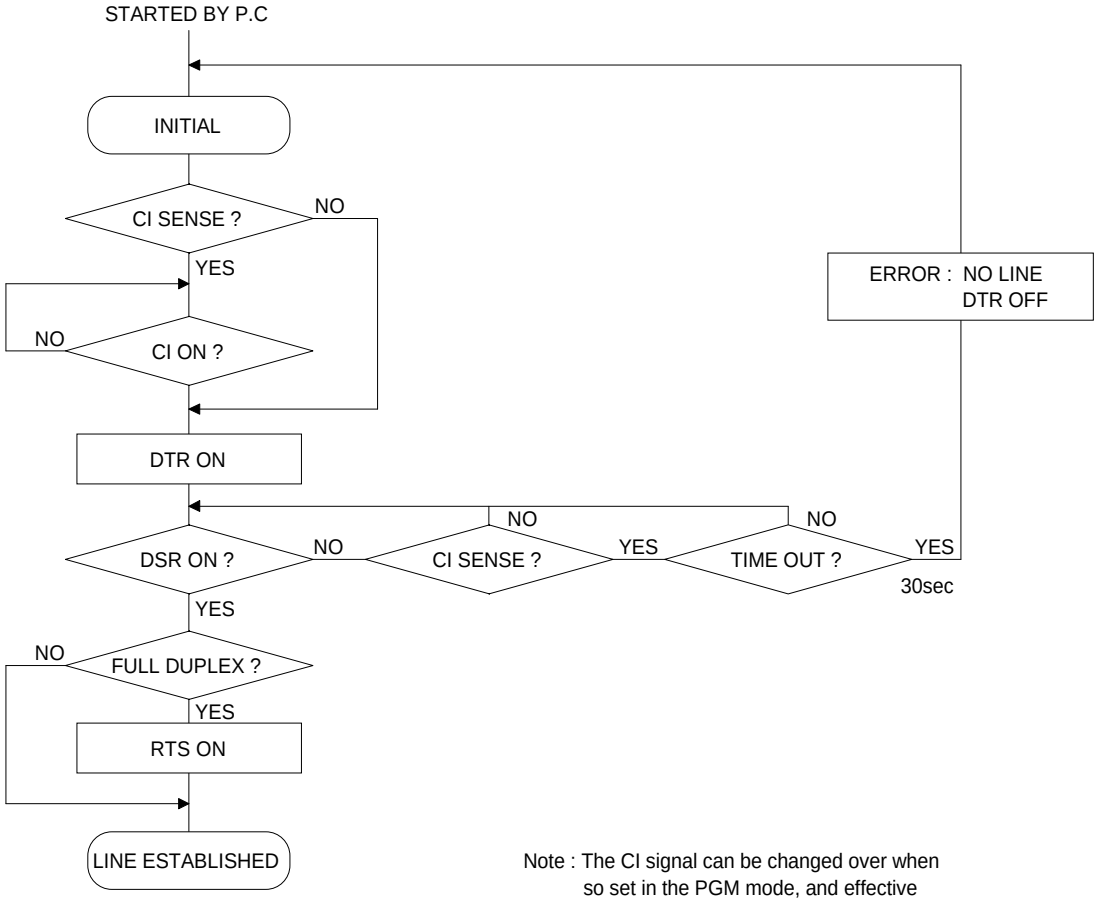
2) Full duplex transmission



*Note : In the direct connect mode, same as full duplex control, but the CI signal is not controlled.

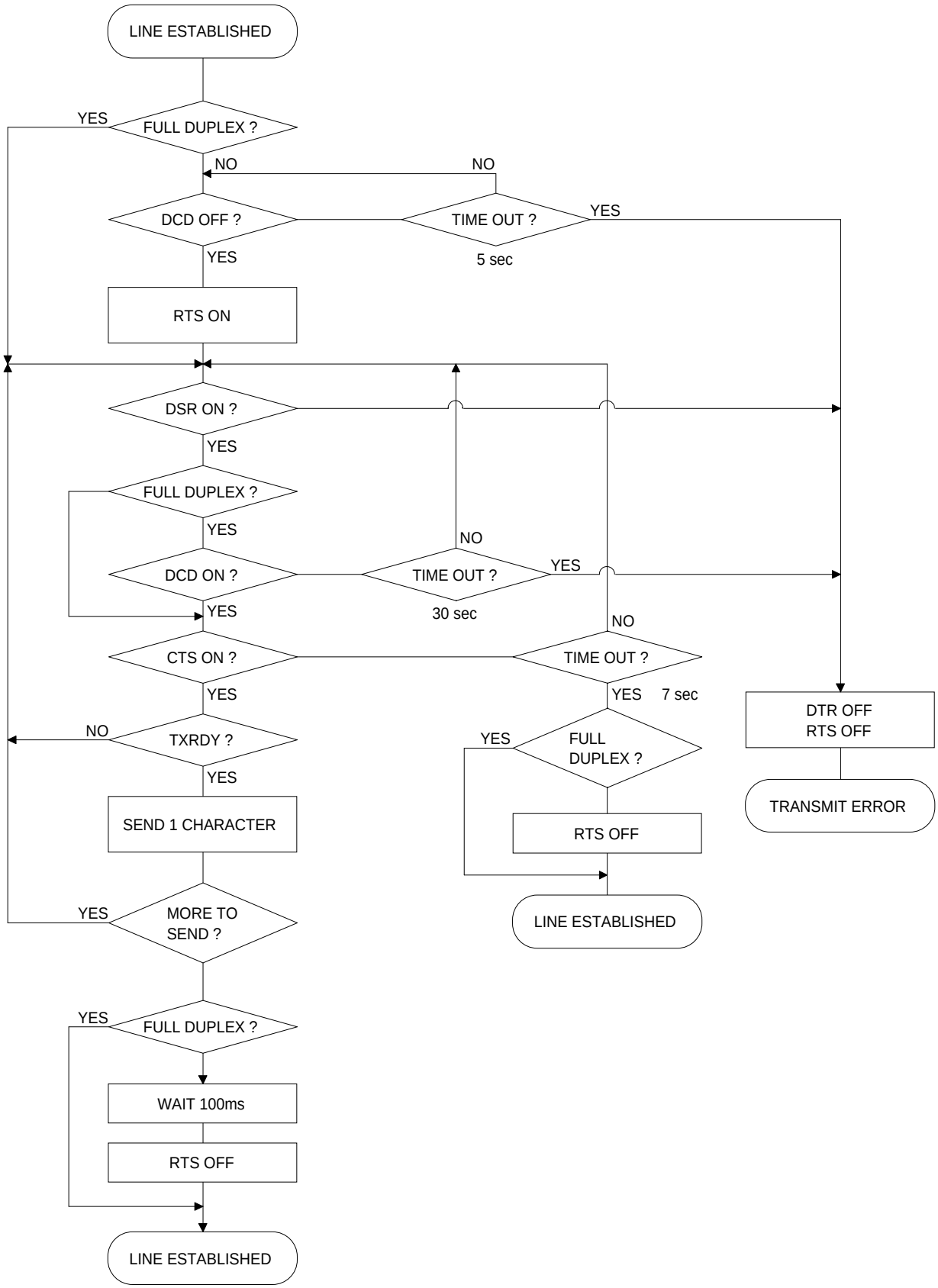
*Note: In the direct connect mode, same as full duplex control, but the CI signal is not controlled.

3) Line connection sequence flow

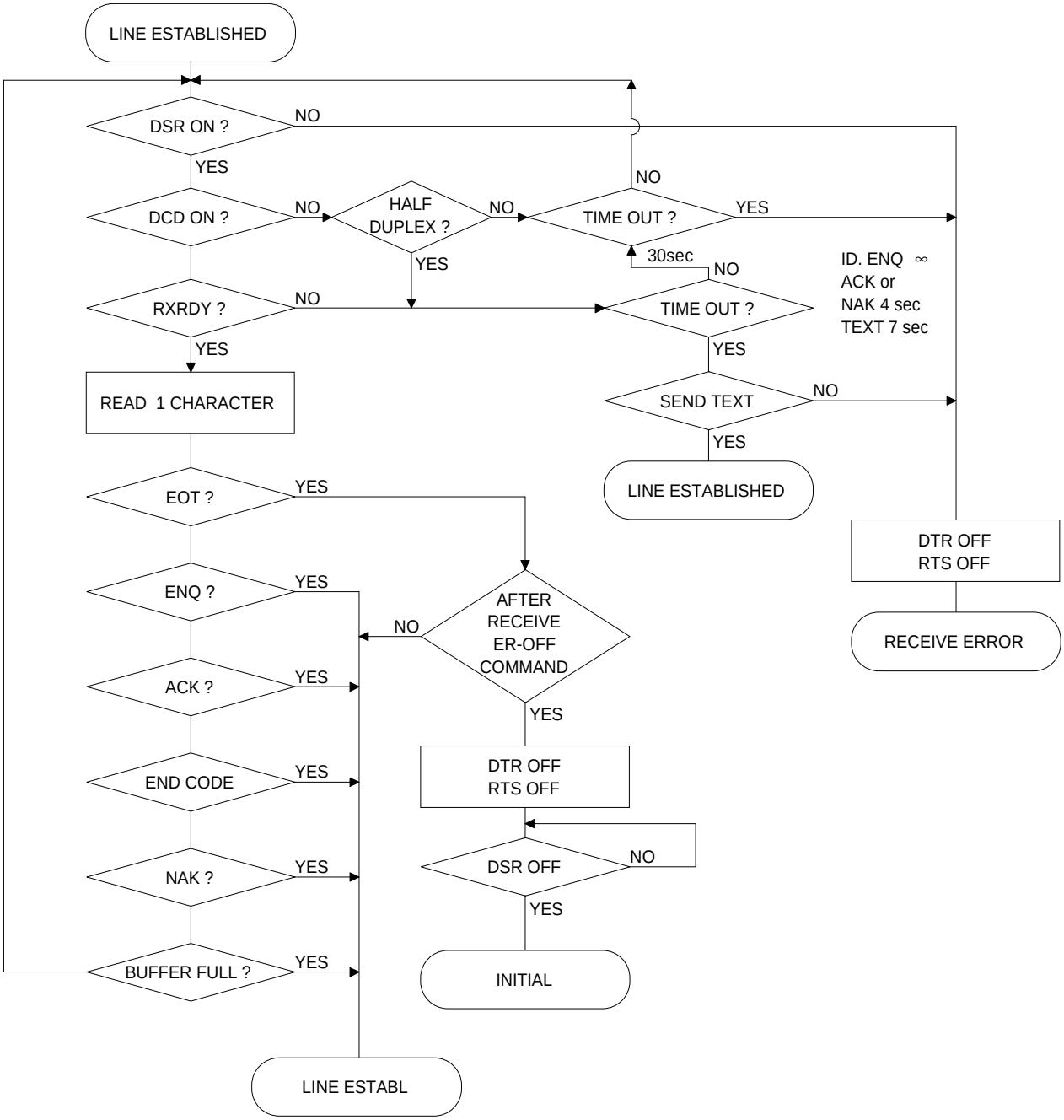


Note : The CI signal can be changed over when so set in the PGM mode, and effective at ECR side.

4) Transmission sequence flow



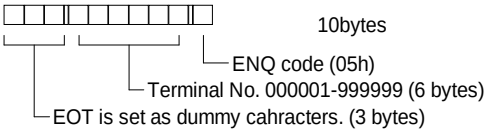
5) Receiving sequence flow



CHAPTER 8. DATA BLOCK FORMAT

1. Basic format

1) ID-ENQ :



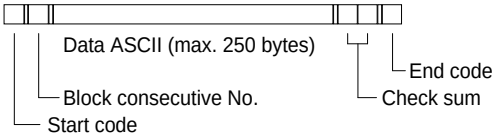
2) ACK : ☐ 1 byte 06h

3) NAK : ☐ 1 byte 15h

4) EOT : ☐ 1 byte 04h

5) ENQ : ☐ 1 byte 05h

6) TEXT :



Start code : This code may not be provided.
Null is impermissible.

End code : This code may not be provided.
Null or any same code as the start code is not permissible.

When master reset is performed, the default is assumed:

Start code = 02h
End code = 0Dh

Block consecutive No. : This number starts with 30h and cycles like this: 30h, 31h — 39h, 30h, 31h (Ring counter system)

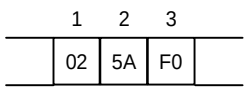
Check sum : 2 bytes hex number
Low-order 8-bit data of the complement of 2 for the sum of text data.

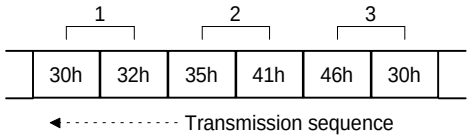
RAM data: : Even number of data that is obtained by dividing one byte of RAM data into high-order 4 bits and low-order 4 bits and converting them to ASCII codes shown in the code conversion table.

Code conversion table .

Print code (high-order or low-order 4 bits)		Line image
Bit image	Hexadecimal	ASCII
0000	0	30h
0001	1	31h
0010	2	32h
0011	3	33h
0100	4	34h
0101	5	35h
0110	6	36h
0111	7	37h
1000	8	38h
1001	9	39h
1010	A	41h
1011	B	42h
1100	C	43h
1101	D	44h
1110	E	45h
1111	F	46h

Example





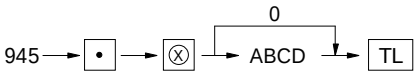
CHAPTER 9. RS-232 application

1. RS-232 preset

1) SRV programming

[JOB#945] MRS = 0000

The assignment of RS-232 channel by each devices.



945-A: Channel No. for ONLINE = 0 to 7.
945-B: Not used. (Fixed at "0")
945-C: Not used. (Fixed at "0")
945-D: Not used. (Fixed at "0")

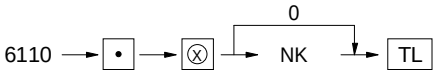
* When channel No. is zero, system is nothing.
* Do not select the same channel number with two or more devices.
* Use the switches on the I/F board to set the channel No. for the I/F board connector. (Refer to the RS-232 channel setting in IV. HARDWARE DESCRIPTION FOR ER-A5RS.)

2) PGM programming

Job#	PGM-MODE programming for online operation
6110	Programming of the terminal number
6111	Programming of the modem control
6112	Programming of the transmission data rate (Bau rate)
6113	Programming of the start and end code.
6110	Online Preset reading

[JOB#6110] MRS = 000001

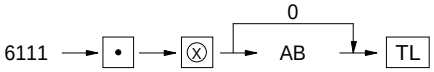
Programming of the terminal number



NK: Terminal No. = 0 to 999999

[JOB#6111] MRS = 00

Porgramming of the modem control



6111-A: 1. Sensing of the CI signal Yes/No

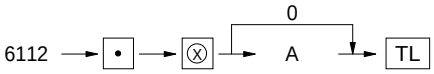
1. Sensing of the CI signal	6111-A
No	0
Yes	1

6111-B: 1. Duplex type

1. Duplex type	6111-B
Full duplex system	0
Half duplex system	1

[JOB#6112] MRS = 5

Programming of the transmission bau rate

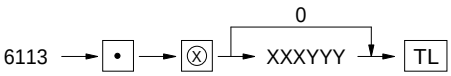


6112-A: Transmission bau rate

Transmission bau rate	6112-A
300 bps	0
600 bps	1
1200 bps	2
2400 bps	3
4800 bps	4
9600 bps	5
19200 bps	6

[JOB#6113] MRS = 002013

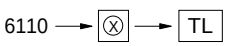
Programming of the start and end code



XXX: Start code = 02H (STX)
YYY: End code = 0DH (CR)

[JOB#6110]

Online preset reading



III. TEST FUNCTION FOR ER-A6IN AND ER-A5RS

CHAPTER 1. General

This test program, is contained in the ER-A57R1 (option ROM), has been developed for the purpose of confirming the operations of the I/F board check conducted by the ER-A5RS and ER-A6IN mounted in the ER-A570.

CHAPTER 2. Structure (RS-232 test & inline test)

1 RS-232 test (RS-232 port test conducted by ER-A5RS
The following structure is required to execute RS-232 test program.

- ER-A570
- ER-A5RS (I/F PWB Unit)
- Loopback connector for testing (UKOG-6705 RCZZ)
- ER-A57R1 (option control ROM)

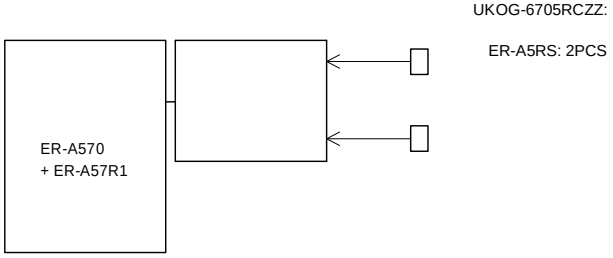


Diagram of the loopback connector

2 Inline test
The following structure is required to execute the inline test program.

- ER-A570
- ER-A6IN (inline I/F PWB unit)
- ER-A57R1 (option control ROM)
- Branch line (main line) cable (for transmission test)
- Terminator (50Ω)

CHAPTER 3. Activation

This test program can be activated by inputting 3-digit number → TL with the mode switch in the "SRV" position.

CHAPTER 4. Test Job & Code

1 RS-232 I/F check

JOB & CODE	Contents
500	Channel check
501	RS-232 channel 1 check
502	RS-232 channel 2 check
503	RS-232 channel 3 check
504	RS-232 channel 4 check
505	RS-232 channel 5 check
506	RS-232 channel 6 check
507	RS-232 channel 7 check

2 Inline I/F check

JOB & CODE	Contents
600	IRC TEST 1
601	IRC TEST 2
602	IRC TEST 3
603	IRC TEST 4: DATA transmission test (SATELLITE setting)
604	IRC TEST 5: DATA transmission test (MASTER setting)

CHAPTER 5. Cautions

- Options should be installed with the power supply turned off.
- When setting the RS232C channels, avoid setting two or more ports to the same channel. The ER-A570 allows installation of max. two units of the ER-A5RS. In this case also, avoid setting two ports of the ER-A5RS to the same channel. If not, the hardware may be damaged.
- Concerning the inspection items whose display formats are not presented in this test function, nothing appears on the display screen. (blank display)

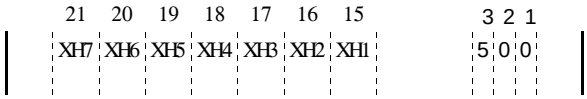
CHAPTER 6. RS-232 Test

1. Channel check

1 Activation
The program is activated by JOB#500
SRV mode: 500 → TL

2 Contents to be tested
Information about connected RS-232 channel is printed.

Πραντανγ
δτγτ



CHn = 0 : Presence of channel
1 : Ansence of channel

3 Confirmed content
Printed contents and the setting of channel changeover switch on PWB are compared and confirmed.

4 Release

The program is terminated after the above contents are printed.

RS-232 channel setting (SW OFF: 1, SW ON: 0)

* Refer to the silk print on the I/F board.

ER-A5RS CN2			
SW1			Channel
6	5	4	
0	0	0	Invalid
0	0	1	Channel 1
0	1	0	Channel 2
0	1	1	Channel 3
1	0	0	Channel 4
1	0	1	Channel 5
1	1	0	Channel 6
1	1	1	Channel 7

ER-A5RS CN1			
SW1			Channel
3	2	1	
0	0	0	Invalid
0	0	1	Channel 1
0	1	0	Channel 2
0	1	1	Channel 3
1	0	0	Channel 4
1	0	1	Channel 5
1	1	0	Channel 6
1	1	1	Channel 7

2. RS-232 Channel 1 ~ 7 check

1 Activation

The program is activated by JOB#501~507.

SRV mode: 501 → TL : Channel 1

502 → TL : Channel 2

503 → TL : Channel 3

504 → TL : Channel 4

505 → TL : Channel 5

506 → TL : Channel 6

507 → TL : Channel 7

2 Contents to be tested

If the channel specified by JOB#CODE is not set, the machine performs the mis-operation processing. When the channel is set, the machine conducts the loop check concerning the channel specified by JOB#CODE by using the loopback connector.

The following three items are checked:

1 Control signal check

2 Data transfer check

3 Timer check (RS-232 onboard timer)

Check 1 Control signal check ($\overline{ERn}$-$\overline{DRn}$•$\overline{CIn}$, $\overline{RSn}$-$\overline{CDn}$•$\overline{CSn}$ loop check)

OUTPUT		INPUT			
$\overline{ERn}$	$\overline{RSn}$	$\overline{DRn}$	$\overline{CIn}$	$\overline{CDn}$	$\overline{CSn}$
OFF	OFF	OFF	OFF	OFF	OFF
OFF	ON	OFF	OFF	ON	ON
ON	OFF	ON	ON	OFF	OFF
ON	ON	ON	ON	ON	ON

The read check about the above INPUT items and interrupt check of $\overline{CS}$, $\overline{CI}$ and $\overline{CD}$ are performed.

Read check: $\overline{ER}$ and $\overline{RS}$ are switched over in the order as shown in the above table to confirm the logic of $\overline{DR}$, $\overline{CI}$, $\overline{CD}$ and $\overline{CS}$.If the read logic is different from the one in the table, error print-outs occur.

Interrupt check: Allows the interruption of either of $\overline{CS}$, $\overline{CI}$ and $\overline{CD}$ one by one. (The mask is released.)
The interruption does not take place when each signal is turned on. Or if the interruption occurs when a signal is turned off, error print-outs occur.

Each of the above checks should be made in four cycles.

Note) $\overline{ERn}$ control selector jumper switch on the I/F board must be switched to the software control side.

Check 2 Data transfer check (SDn-RDn loop check)
In this check, transfer 256-byte loopback data of $00 ~ $FF.

Note) The above check should be made with the baud rate set at 9600BPS.

Check 3 Timer check
Before making check 2 , set the corresponding timer at 10ms for RCVDT activation, and check to see that:
1) $\overline{TRQ1}$ is not generated during the execution of check 2 .
2) $\overline{TRQ1}$ is generated in 10msec. after check 2 is finished.

3 Contents to be checked

If an error occurs during the above checks, following error print-outs occur. Even if an error occurs during check 1 , the test is continued after the corresponding error print-out has occurred, but if an error occurs during the execution of check 2 or 3 , the test is terminated after the corresponding error print-out has occurred.
Note that when check 1 , 2 or 3 terminates, the termination print-out occurs irrespective of any errors that have occurred during the check. (The program terminates normally only when no error print-out has occurred.)

ERROR	ERROR PRINT	Contents
1	E1-ER DR	$\overline{ERn}$-$\overline{DRn}$ ERR
2	E2-ER CI	$\overline{ERn}$-$\overline{CIn}$ ERR
3	E3-RS CD	$\overline{RSn}$-$\overline{CDn}$ ERR
4	E4-RS CS	$\overline{RSn}$-$\overline{CSn}$ ERR
5	E5-CI INT	Interruption error of $\overline{CIn}$
6	E6-CD INT	Interruption error of $\overline{CDn}$
7	E7-CS INT	Interruption error of $\overline{CSn}$
8	E8-TXEMP	TXEMPn error
9	E9-TXEMP I	Interruption error of TXEMPn
10	E10-TXRDY	TXRDYn error
11	E11-TXRDY I	Interruption error of TXRDYn
12	E12-RCVRDY	RCVRDYn error (Reception is impossible. TRQ1 has occurred during execution of check 2 .)
13	E13-RCVRDY I	Interruption error of RCVRDY
14	E14-SD RD	SDn-RDn ERR (Data error)
15	E15-SD RD	SDn-RDn ERR (Data error, Flaming error)
16	E16-TIMER	TIMERn error ($\overline{TMRQn}$ cannot be set after termination of check 2 .)
17	E17-TIMER I	Interruption error of TRQ1

Errors that may occur during check 1 (control signal check): E1 ~ E7
Errors that may occur during check 2 (data transfer check): E8 ~ E15
Errors that may occur during check 3 (timer check): E12, E16 and E17

4 Cancellation

The program automatically terminates when a check is finished.

Termination print-out:

50n	n : 1 ~ 7

CHAPTER 7. INLINE CHECK

1. IRC TEST 1

1 Getting started
Get started with JOB #600.

SRV mode: 600 → TL

2 Test content
The ROM and the RAM on the ER-A6IN are checked as well as an interruption by CTC and carrier sense are checked. Also the ADLC functions and send/receive DMA are checked by means of the self loop function of ADLC (MC6854). In addition, the other signals are checked.

3 Check content
The end print is checked.
First the status of the number of resending is printed by the SRN handler command (Diag 2), then diag 0, 1, and 5 commands are executed. If any error occurs, an error print is made to show the error status.

α Print of the number of resending by diag 2 command

```
DATA   RETRY  CNT. = XXX
ACK    RETRY  CNT. = YYY
```

(Note) XXX and YYY are in decimal (000~255)

β Error print by diag 0 command

Error status (0: Normal or not checked yet, 1: Abnormal)

```
E0-XXXXXXXX
  (b7b6b5b4b3b2b1b0)
```

b0: RAM check error
b1: ROM sum check error
b2: CTC, CH2, or CH3 interruption (Timer interruption) is not effective.
b3: Interruption with the carrier OFF is not effective, or the mirror image with the carrier OFF shows the carrier ON.
b4: Transmission complete interruption (DMAC TC UP interruption) is not effective.
b5: A corrosion is generated.
b6: An expected interruption is made.
b7: An error occurs. (Always 1 in when in error print)

(Note)

- When a RAM error occurs, the other checks are not performed.
- When a ROM sum check error occurs, the other checks except for the RAM error check are not performed.

χ Error print by diag 1 command

Error status (0: Normal, 1: Abnormal)

```
E0-XXXXXXXX
  (b7b6b5b4b3b2b1b0)
```

b0: Transmission complete interruption (DMAC TC UP interruption) is not effective.
b1: An underrun error occurs.
b2: An overrun error occurs.
b3: Abnormal data number transmitted by DMA
b4: Abnormal data number received by DMA
b5: Data transmitted by DMA are difference from data received by DMA.
b6: n unexpected interruption is made.
b7: An error occurs. (Always 1 when in error print)

δ Error print by diag 5 command

The table below shows the names of the signals to be checked and their directions.

Signal name	Direction
Power failure notice	Host → Controller
Power ON initializing	Host → Controller
Power ON continuation	Host → Controller
Power failure process end	Host ← Controller
CH1 received data present	Host ← Controller
CH2 received data present	Host ← Controller

```
E5-XXXXXXXX              H>C
  (b7b6b5b4b3b2b1b0)
```

Check that the target bits in two kinds of status (ST1 and ST2) obtained by diag 5 command are "0" for ST1 and "1" for ST2. (The other bits should be masked.) In the other cases, the error occurring bit is shown as "1" and the error print is made in the above format. If the target bit is "0," it is normal.

ST1: Sense in the controller in non-active state of a signal in the direction of host → controller.
ST2: Sense in the controller in active state of a signal in the direction of host → controller.

B7: 0 (Not used.)
B6: Power failure notice
B5: 0 (Not used.)
B4: 0 (Not used.)
B3: 0 (Not used.)
B2: 0 (Not used.)
B1: Power ON continuation
B0: Power ON initializing

Similarly to the above procedure, the signals in the direction from the controller to the host obtained by diag 5 command are checked. If the target bit is "1," it shows defective operation, If "0," it is normal.

The error print in that case is made as shown below:

```
E5-XXXXXXXX              C>H
  (b7b6b5b4b3b2b1b0)
```

B7: 0 (Not used.)
B6: 0 (N0t used.)
B5: 0 (Not used.)
B4: CH2 received data present
B3: CH1 received data present
B1: 0 (Not used.)
B0: 0 (Not used.)

4 End

The end print is made and the operation is terminated automatically.

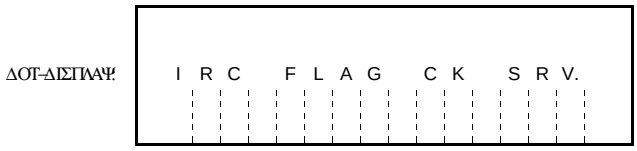
```
600
```

2. IRC test 2 (FLAG send)

1 Getting started
Get started with JOB #601.

SRV mode: 601 → TL

2 Content
FLAG (7EH) is continuously transmitted. The following display is given during the execution. (Execution of diag command 3)



3 Test check content
The FLAG to be transmitted is checked by the hardware.

601

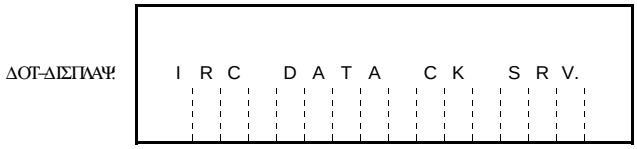
4 Cancellation
To cancel this test, perform the SRV reset.

3. IRC test 3 (DATA send)

1 Getting started
Get started with JOB #602.

SRV mode: 602 → TL

2 Test content
Data of 256 byte in 00 - 0FFH are formed as one packet, and the packets are continuously transmitted in the packet interval of 12.8 msec at 480 kbps. (Execution of diag command 4)



3 Check content
The data to be transmitted are checked by the hardware.

602

4 Cancellation
To cancel this test, perform the SRV reset.

4. IRC test 4, 5 (Data transmission test)

This test is intended to perform data transmission test in an actually configured system. The system to be tested is composed of one set of master machine (set by JOB #604) and max. 15 sets of slave machines (set by JOB #603).

Note for starting the test:

- When testing a set in which the IRC setting has been already made, be sure to cancel the inline setting in the following procedure before performing this test.

  To cancel the inline setting:

  SRV mode: 902 → • → Ⓧ → 0XXX → TL

  XXX: Set as required.

- When testing an already configured system, cancel the inline setting of the set which are not to be tested in the above procedure or disconnect their signal lines. (Disconnect the inner cable and the joint connector.) If the test is executed without cancelling the inline setting of a set which is not to be tested, the data in the set may be destroyed.
- Cancel the inline setting of all the sets in the system before performing the transmission test (JOB #603, JOB #604) setting. Perform the satellite machine setting (JOB #603) before performing the master machine setting (JOB #604).

Note for terminating the test:

- After terminating the test of all the sets used in the test (by the program resetting), perform setting of each set.
- For the set whose inline setting was cancelled before the test because its IRC setting had been made, perform the inline setting in the following procedure. This test will not affect the other settings.

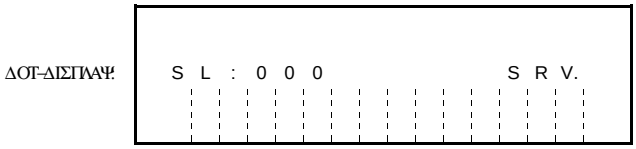
To set the inline setting YES:

SRV mode: 902 → • → Ⓧ → 1XXX → TL

1 Satellite machine setting (JOB #603)

Starting

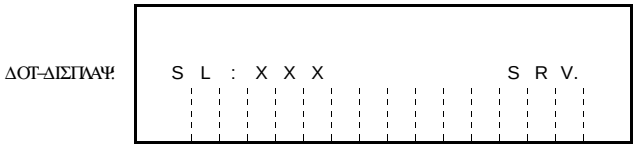
SRV mode: 603 → TL



Test terminal No. input and test start

XXX → TL

(XXX: 000 - 254)
XXX: Test slave machine terminal No.

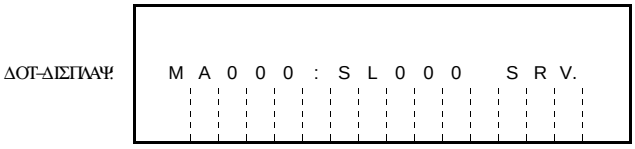


With the above procedure, setting and starting of the satellite machine to be tested are finished, and the master machine is ready for starting.
Data transmission with the master is performed and the sequence number of received data is displayed on the display.
When using two or more satellite machines for testing, perform the above procedure for every satellite machine to be tested. In this case, avoid repetition of the terminal number.

2 Master machine setting (JOB #604)
The master machine setting should be performed after the completion of the satellite machine setting. If the master machine is started before starting the satellite machine, an transmission error may occur.

STARting

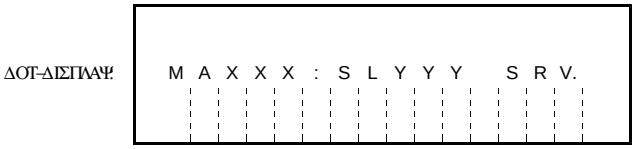
SRV mode: 604 → [TL]



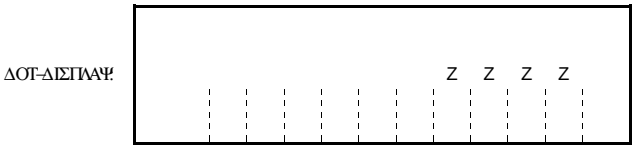
Test terminal No. input and test start

XXX → YYY → [ST] → [TL]

If there are two or more satellite machines, repeat the procedure.
(XXX, YYY: 000 ~ 254)
XXX : Terminal No. of the master machine to be tested
YYY : Terminal No. of the satellite machine to be tested
Note: Do not use the same terminal No. to any of the master and the satellite machines.



With the above procedure, data transmission is started with the satellite machine in standby state.
When data transmission is started, the sequence No, of transmitted data is displayed on the 7SEG DISPLAY of the master and the satellite machines.



ZZZZ: Sequence No. → 0000 → 9999 →

3 Test content
a. A sequence No. of 2 byte and the format below composed of 0AAH data of 254 byte are transmitted from the master to the satellite.
The sequence No. is displayed on the 7SEG DISPLAY of the master.
b. The satellite returns the received data back to the master.
The sequence No. of the received data is displayed on the 7SEG DISPLAY of the satellite.
c. The master receives the data and then checks the sequence No. and 0AAH data.
If there are two or more satellite machines, steps a and b are repeated. If all data sent from the satellite are normal, the master increments the sequence No.

The above steps a through c are repeated.

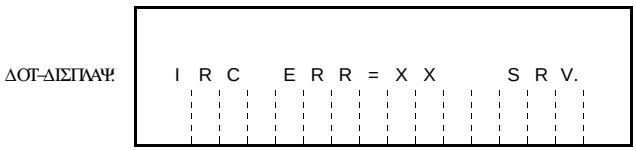
Test data format (1 packet: 256 byte)

1	2	3	4	5	• • • • • • • • •	254	255	256	(BYTE)
ZZ	ZZ	AA	AA	AA	• • • • • • • • •	AA	AA	AA	

ZZZZ : Sequence No. 2 byte (Integral number 4 digits)
AA : Transmitted data (0AAH) x 254 byte

4 Error display
When an error occurs during the data transmission test, the following display is given and the error print is made.
To cancel the error, perform the program resetting (power OFF/ON in the SRV mode).

Error display:



XX: Error code

Error print

(Satellite side)

E-XX	603	

(Master side)

E-XX YYY	604	ΨΨΨ ΣΑτε ϖερμ ινολ No. ωηεν αν ερρορ οχχυρρεδ

XX= 01: Abnormal command (except during transmitting)
02: No received data
03: Reception size YES
Received data remained
04: The remote station not ready (in transmitting)
The remote station is not ready for reception and returns back "NRDY."
05: Receiving side buffer full
The controller receiving buffer in the remote station is full.
06: Resend error (in transmitting)
Retry over (5 times) without reply
07: Collision error (in transmitting)
When data transmitting collision occurs, retry over (16 times) after random time (0 - 255 ms).
08: Line busy time out
Transmission is not made because of transmission between the other remote stations, and data transmitting wait time is out.
09: Reception size over (in receiving)
The reception buffer size is insufficient.
0A: Hhard error
Abnormal interface (no SRN interface or abnormal SRN controller)

IV. HARDWARE DESCRIPTION FOR ER-A6IN AND ER-A5RS

CHAPTER1. ER-A6IN

1. Block Diagram

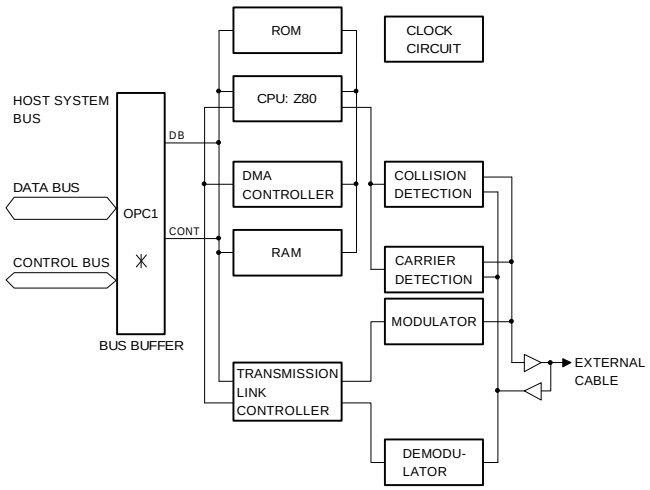


Fig. 1 SRN controller board block diagram

Fig. 1 shows the block diagram of the controller board of the SHARP RETAIL NETWORK. The Controller is connected to the system bus of the host system as one of I/O. Inside of the controller consists of Z-80 CPU, transmission link controller, DMA control circuit, ROM, RAM, modulator, demodulator, carrier detection circuit, collision detect circuit and so on.

Data communications with the host system is performed by the handshaking by byte. The controller side functions with DMA (Direct Memory Access) and is capable of data transmission without waiting for the host system side.

* OPC1 is used only as a bus buffer. (In order to provide compatibility between the host CPU in the ECR side and H8/510.)

2. CPU Description (Z-80)

For details on the CPU, see the Cash Register Basic Manual.
Pin Connections (C-MOS Version used)

Pin	Signal name	Input/ Output	Description
1	A11	Out	Address Bus A11
2	A12	Out	Address Bus A12
3	A13	Out	Address Bus A13
4	A14	Out	Address Bus A14
5	A15	Out	Address Bus A15
6	ϕ	In	CLK4 (MHz)
7	D4	I/O	Data Bus D4
8	D3	I/O	Data Bus D3
9	D5	I/O	Data Bus D5
10	D6	I/O	Data Bus D6
11	VCC	—	+5V
12	D2	I/O	Data Bus D2
13	D7	I/O	Data Bus D7
14	D0	I/O	Data Bus D0
15	D1	I/O	Data Bus D1
16	$\overline{\text{INT}}$	In	Interrupt
17	$\overline{\text{NMI}}$	In	Non Maskable Interrupt
18	$\overline{\text{HALT}}$	Out	HALT
19	$\overline{\text{MREQ}}$	Out	Memory Request
20	$\overline{\text{IOREQ}}$	Out	I/O Request
21	$\overline{\text{RD}}$	Out	Read
22	$\overline{\text{WR}}$	Out	Write
23	$\overline{\text{BUSAK}}$	Out	Bus acknowledge
24	$\overline{\text{WAIT}}$	In	$\overline{\text{WAIT}}$
25	$\overline{\text{BUSRQ}}$	In	Bus Request
26	$\overline{\text{RES}}$	In	Reset
27	$\overline{\text{M1}}$	Out	M1 cycle
28	$\overline{\text{RFSH}}$	Out	Refresh
29	GND	—	GND
30	A0	Out	Address Bus A0
31	A1	Out	Address Bus A1
32	A2	Out	Address Bus A2
33	A3	Out	Address Bus A3
34	A4	Out	Address Bus A4
35	A5	Out	Address Bus A5
36	A6	Out	Address Bus A6
37	A7	Out	Address Bus A7
38	A8	Out	Address Bus A8
39	A9	Out	Address Bus A9
40	A10	Out	Address Bus A10

3. Description of MB62H149

1) Outline

The MB62H149 is a semi-custom LSI chip for the peripheral circuits in the SRN (SHARP Retail Network), its main function is to communicate data with the host CPU and control the peripheral circuits and transmission control circuits of the Sub CPU (Z-80). Fig. 2. shows the general configuration of the functions:

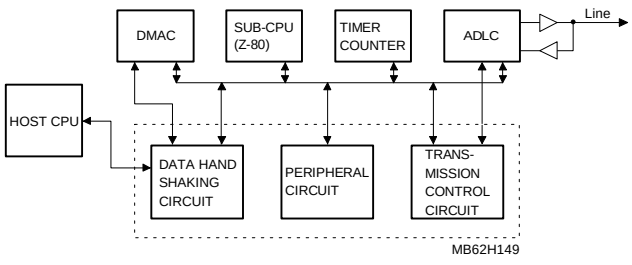


Fig. 2

2) Internal functions

(1) Data handshaking circuit

Is used because data processing speeds vary and the timing of the HOST CPU and SUB CPU do not synchronize, the MB62H149 is used for data handshaking. When the data handshaking portion is broken down, the system consists of a Write Signal from the HOST CPU to the MB62H149, Read Signal from the MB62H149 of the SUB CPU, Write Signal from the SUB CPU to the MB62H149 and Read Signal from the MB62H149 of the HOST CPU, all of which from two blocks as shown.

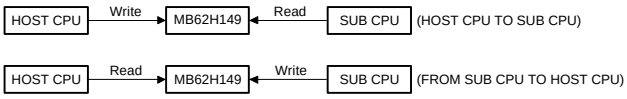


Fig. 3

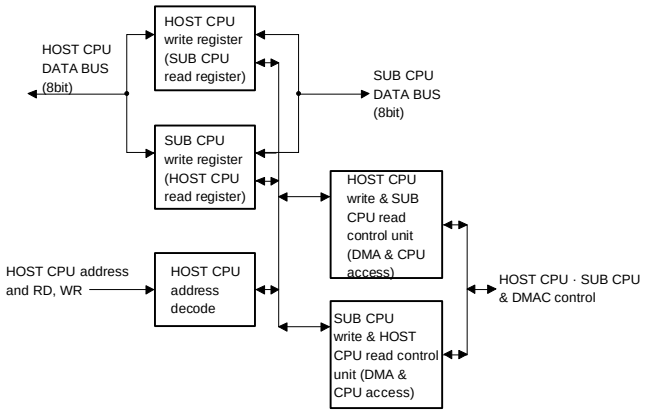


Fig. 4

(2) Peripheral circuit

The peripheral circuit consists of an I/O address generation unit on the SUB CPU, block dividing circuit, and the wait signal control unit.

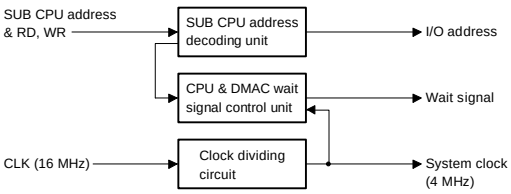


Fig. 5

(a) I/O address generation circuit
A total of 11 I/O addresses are generated by A0, A1, A4, A5 and RD and WR signals.

(b) CPU and DMAC wait signal control unit
Clocks into the CPU (Z-80), SUB CPU and its peripheral LSI, DMAC and CTC are operated respectively on 4 MHz.
While, the ADLC (MC68B54) (Advanced Data Link Control) is operated by the E (Enable clock) of 2 MHz according to restrictions in terms of the hardware of the LSI.
It is necessary to synchronize the timing of the write and read in the ADLC.
To control synchronization, timing, and input, the wait signal goes into the CPU for CPU access and into the DMAC for DMA access. This block is a circuit to generate such wait signal.

(c) Clock dividing circuit
This block divides the blocks according to the CLK supplied from outside to generate the clock for CPU, DMAC and CTC and the E and transmission clock rate (480 KBPS or 1 MBPS selectable) for the ADLC.

(3) Transmission control circuit

The transmission control circuit is divided into the modem unit, carrier detect unit, collision detect unit.

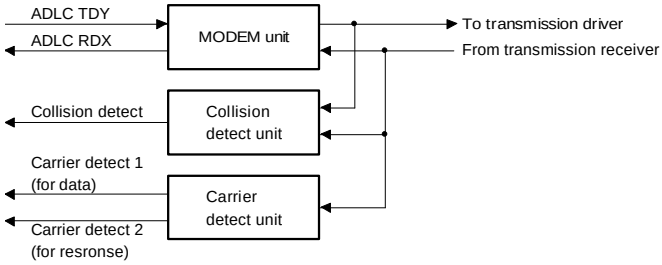


Fig. 6

(a) Modem circuit
The transmission data input from the ADLC are PE modulated (phase encoding modulation), the circuit to be output to the transmission driver and the reception data input from the transmission receiver are demodulated and produced at the ADLC.

(b) Collision detect circuit
The data transmitted from the home station is received and detects a collision on the transmission line by means of an exclusive OR gate.

(c) Carrier detect circuit
This circuit detects whether data is flowing on the transmission line. It consists of a circuit which immediately senses a no data status on the line. When data is not on the line the circuit functions to sense an elapse of the fixed time rate. The immediate sensing circuit is used for response testing and the delayed sensing circuit is used for data testing.
The fixed time rate is selectable according to the transmission speed as shown below via SRV-mode programming. Job #922.

Transmission speed	Delay time
1 MBPS	1.6m sec, 3.2m sec, 4.8m sec, 6.4m sec.
480 KBPS	3.2m sec, 6.4m sec, 9.6m sec, 12.8m sec.

3) Terminal Name and Description (MB62H149)

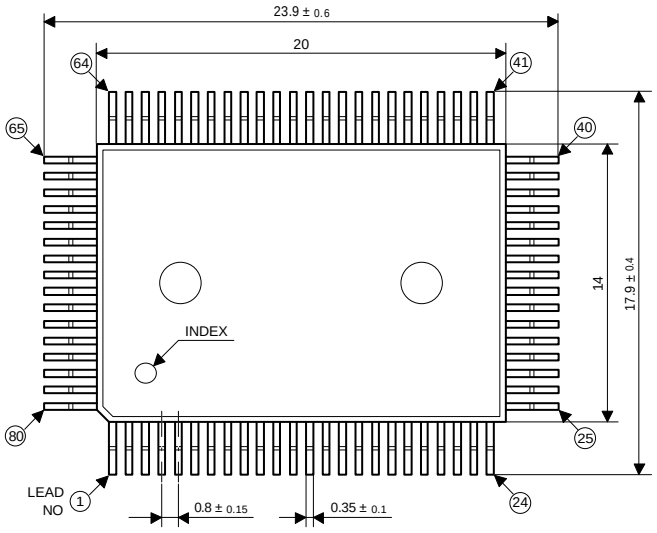


Fig. 7

Pin No.	Terminal name	Host/ Sub	In/ Out	Description
1	CLK	Sub	In	Clock in (16 MHz)
2	—	—	—	N.U.
3	$\overline{\text{IORQ}}$	Sub	In	I/O request
4	$\overline{\text{MREQ}}$	Sub	In	Memory request
5	$\overline{\text{RDS}}$	Sub	In	Read from sub
6	$\overline{\text{WRS}}$	Sub	In	Write from sub
7	$\overline{\text{INTS}}$	Sub	Out	Interrupt to sub
8	ϕ	Sub	Out	Clock out
9	TM0	Sub	In	Timer 0
10	TM1	Sub	Out	Timer 1
11	$\overline{\text{MRD}}$	Sub	Out	Memory read
12	VSS	—	—	GND
13	$\overline{\text{WAIT}}$	Sub	Out	Wait signal
14	A15	Sub	Out	Address bus for DMA
16	A9	Sub	Out	
17	A8	Sub	Out	
18	A5	Sub	In	
19	A4	Sub	In	
20	A1	Sub	In	
21	A0	Sub	In	
22	DAK01	Sub	In	DMA acknowledge 0+1
23	—	—	—	N.U.
24	$\overline{\text{MWR0}}$	Sub	Out	Memory write
25	D7	Sub	I/O	Data bus
26	D6	Sub	I/O	
27	D5	Sub	I/O	
28	D4	Sub	I/O	
29	D3	Sub	I/O	
30	D2	Sub	I/O	
31	D1	Sub	I/O	
32	D0	Sub	I/O	
33	VDD	—	—	+5V
34	—	—	—	N.U.
35	$\overline{\text{RES}}$	Host	In	Reset
36	$\overline{\text{IO/WR}}$	Sub	I/O	I/O write
37	$\overline{\text{IO/RD}}$	Sub	I/O	I/O read
38	AEN	Sub	In	Address enable from DMAC
39	AST	Sub	In	Address strobe from DMAC
40	TCS	Sub	In	Terminal count
41	DAK23	Sub	In	DMA acknowledge 2+3
42	$\overline{\text{DRQRS}}$	Sub	Out	DMA request read to sub
43	$\overline{\text{DRQWS}}$	Sub	Out	DMA request write to sub
44	$\overline{\text{RDH}}$	Host	In	Read from Host
45	$\overline{\text{WRH}}$	Host	In	write from Host
46	$\overline{\text{INTH}}$	Host	Out	Interrupt to host
47	$\overline{\text{DAK}}$	Host	In	DMA acknowledge from host
48	TCH	Host	In	Terminal count from host
49	$\overline{\text{DRQWH}}$	Host	Out	DMA request read to host
50	$\overline{\text{DRQWH}}$	Host	Out	DMA request write to host
51	$\overline{\text{CS}}$	Host	In	Chip select from host
52	VSS	—	—	GND
53	—	—	—	N.U.
54	DB0	Host	I/O	Data bus
55	DB1	Host	I/O	Data bus
56	DB2	Host	I/O	Data bus
57	DB3	Host	I/O	Data bus
58	DB4	Host	I/O	Data bus
59	DB5	Host	I/O	Data bus
60	DB6	Host	I/O	Data bus
61	DB7	Host	I/O	Data bus
62	AB0	Host	In	Address bus from host
63	—	—	—	N.U.
64	AB1	Host	In	Address bus from host
65	COL	Sub	In	Collision detect signal
66	RDI	Sub	In	Receive data from receiver
67	TDI	Sub	Out	Transmmit data to driver
68	$\overline{\text{RTS}}$	Sub	In	Request to send
69	RXC	Sub	Out	Receive clock to ADLC
70	RXD	Sub	Out	Receive data to ADLC
71	TXC	Sub	Out	Transmmit clock
72	TXD	Sub	In	Transmmit data
73	VDD	—	—	+5V
74	E	Sub	In	Enable clock to ADLC
75	$\overline{\text{IRQ}}$	Sub	In	Interrupt request from ADLC
76	$\overline{\text{LCS}}$	Sub	Out	Link controller chip select
77	—	—	—	N.U.
78	RS1	Sub	Out	Register select 1
79	RS0	Sub	Out	Register select 0
80	MSK	Sub	Out	Mask signal

4) Pin Assingment and timing Charts

Pin function will be described for the host and sub system.

(1) Host pin description

1 DB0—DB7 (data bus) Input/Output, 3-state
Pins 54—61
These lines (data bus) are use for hardware flag assignments: 8-bit data write, hardware flag recognition, and 8-bit data read from the host.

2 $\overline{\text{RDH}}$ (Read from host), Input
Pin 44
An active low signal which is used when the host reads the hardware flag and 8-bit data through the data bus.

3 $\overline{\text{WRH}}$ (Write from sub), Input
Pin 45
An active low signal which is used when the host writes the hardware flag and 8-bit data through the data bus.

4 $\overline{\text{CS}}$ (Chip select from host), Input
Pin 51
An active low signal which is used when the host reads or writes the hardware flag and 8-bit data through the data bus.

5 AB0, AB1(Address bus from host), Input
Pin 62, 64
An input signal used to select the register when the host reads or writes the hardware flag and 8-bit data through the data bus.

6 $\overline{\text{DAK}}$ (DMA Acknowledge from host), Input
Pin 47
Not used (+5v)

7 $\overline{\text{DRQRH}}$ (DMA Request read to haos), Output
Pin 49
Not used

8 $\overline{\text{DRQWH}}$ (DMA request write to host), Output
Pin 50
Not used

9 TCH (Terminal count from host), Input
Pin 48
Not used

Φ $\overline{\text{INTH}}$ (Interrupt to host), Output
Pin 46
An active low signal which is used to inform the interrupt signal that the controller has the information to read or write.

Γ $\overline{\text{RES}}$ (Reset), Input
Pin 35
Asynchronous reset signal from the host which is used to reset registers within the controller.

- HOST read timing.

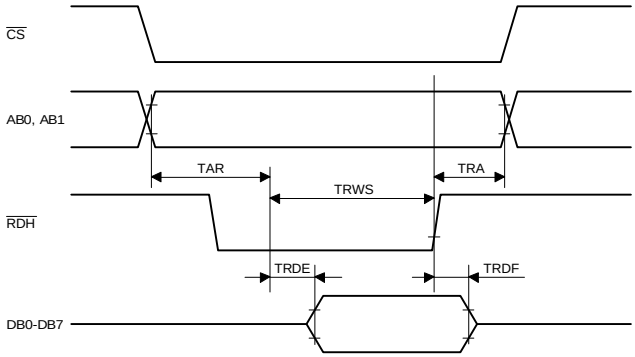


Fig. 8

- HOST write timing.

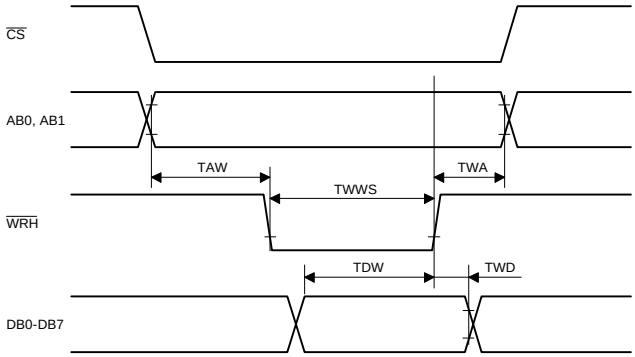


Fig. 9

(2) Sub system pin description

1 D0 – D7 (Data bus) Input Output (3-state)
Pin 32 – 25
These lines (data bus) are used for hardware flag assignments: 8 bit data write, hardware flag recognition, and 8-bit data read from the subsystem.

2 $\overline{\text{IORQ}}$ (I/O request), Input
Pin 3
An active low memory request input from the subsystem (Z-80A) which is used to create I/O control signals in conjunciton with RDS, WRS, A0, A1, A4 and A5.

3 $\overline{\text{MREQ}}$ (Memory request), Input
Pin 4
An active low memory request input from the subsystem (Z-80A) which is used to create I/O control signals in conjunction with RDS and WRS.

4 $\overline{\text{RDS}}$ (Read from sub), Input
Pin 5
Data read signal received from the subsystem (Z-80A) wihch is used to create I/O and memory data read control signal.

5 $\overline{\text{WRS}}$ (Write from sub), Input
Pin 6
Data write signal received from the subsystem (Z-80A) which is used to create I/O and memory data write control signal.

6 $\overline{\text{MRD}}$ (Memory read), Output
Pin 11
Memory data read control signal sent to the subsystem (memory) which is created with MREQ and RDS.

7 $\overline{\text{MWRO}}$ (Memory write), Output
Pin 24
Memory data write control signal sent to the subsystem (memory) which is created with MREQ and RDS.

8 $\overline{\text{IO/WR}}$ (I/O write), Input/Output (3-state)
Pin 36
I/O data write control signal sent to the subsystem (peripheral I/O) which is created with IORQ And WRS.
During the DMA mode, it is received from the DMAC to create the memory to I/O data transfer control signal.

9 $\overline{\text{IO/RD}}$ (I/O read), Input/Output (3-state)
Pin 37
I/O data read control signal sent to the subsysystem (peripheral I/O) which is created with IORQ and WRS. During the DMA mode, it is received from the DMAC to create the I/O to memory data transfer control signal.

Φ AO, A1, A4, A5 (Address bus from sub CPU), In
Pin 21, 20, 19, 18
An input signal used to create the selection signal which the sub reads the hardware flag and subsystem (peripheral I/O) 8-bit data through the data bus.

Γ A8, A9, A10, A15 (Address bus for DMA), Output (3-state)
Pin 17, 16, 15, 14
Used to create the memory address information on the basis of the information from the DMAC during the DMA cycle. The output has 3-stats and retains a high impedance except during the DMA cycle.

H AEN (Address enable from DMAC), In
Pin 38
An input from the DMAC which is used to enable the DMAC to control by isolating the system address bus from the CPU (Z-80A) during the DMA cycle.
That is, A8, A9, A10, and A15 are set to output condition from their high impedance state.

I AST (Address strobe from DMAC), In
Pin 39
An input from the DMAC which is used to latch the information from the DMAC Sent on the data bus with AST In the DMAC cycle to create A8, A9, A10, and A15 address information.

ϑ DAK01 (DMA acknowledge 0+1), Input
Pin 22
The subsystem uses four DMA channels; one each for transmitting and receiving of data (DAK0, DAK1), and for read and write of received data (DAK2, DAK3), DAK01 is a logical OR of DAK0 with DAK1 which is used for DMA control of transmission data.

K DAK23 (DMA acknowledge 2+3), Input
Pin 41
This signal is a logical OR of DAK2 and DAK3 and is used for DMA control of transmission data.

Λ $\overline{\text{DRQRS}}$ (DMA request read to sub CPU), Output
Pin 42
An active low DMA request to the sub CPU to read data which is normally connected to the DMA controller of the sub.

M $\overline{\text{DRQWS}}$ A request to write to sub CPU), Outut
Pin 43
An active low DMA request to the sub CPU to write data which is normally connected to the DMA controller of the sub CPU.

N TCS (Terminal count from sub), Input
Pin 40
An active high signal which the subsystem uses to inform that the current DMA cycle is the final cycle.

O $\overline{\text{INTS}}$ (Interrupt to sub), Input
Pin 17
An interrupt which the controller uses to inform the sub that it has data to be read or written. This output is a half duty oscillation signal when active.

Π $\overline{\text{WAIT}}$ (Wait signal), Output
Pin 13
This signal is used to provide synchronization for the DMAC and the sub CPU with the link controller (ADLC) when transferring data with the link controller (ADLC), that is, to wrtie a command to the ADLC, to read status, and to write or read transmit or receive data. This line is normally an input to the DMAC and sub CPU WAIT (ready) line.

Θ CLK (Clock input), Input
Pin 1
Basic frequency input which is used to derive system clock, transmit/receive clock, and internal sync clock, [16MHz]

P ϕ (clock out), Output
Pin 8
A system clock output which the basic oscillation is divided by four, Since the basic frequency is normally at 16MHz, the system clock output is a 4MHz.

Σ TXC (Transmit clock), Output (for SRN)
Pin 71
As the basic frequency is divided 1/16 or 1/32, it is supplied as the transmit clock for the SRN system.
Choice of 1/16 and 1/32 is dependent on the sub CPU.

T TXD (Transmit data from ADLC), Input (for SRN)
Pin 72
Transmit data from the link controller (ADLC).

Y TDI (Transmit data to driver), Output (for SRN)
Pin 67
Transmit data which TXD is phase encoded with the transmit clock which is an input to the line driver of the SRN.

ς RDI (Receiver data from receiver), Input (for SRN)
Pin 66
Phase encoded data from the other end via the line receiver of the SRN.

Ω RXD (Receive data to ADLC), Input (for SRN)
Pin 70
Receive data (RXD) output as the phase encoded data from the other end received via the receiver are demodulated within the controller to separate it into the receive data (RXD) and receive clock, which is normally an input to the link controller (ADLC).

Ξ RXC (Receive clock to ADLC), Output (for SRN)
Pin 69
An output of the receive clock (RXC) which is normally supplied to the link controller (ADLC).

Ψ $\overline{\text{RTS}}$ (Request to send), Input (for SRN)
Pin 68
An input from the link controller (ADLC) which becomes active low during transmission. The controller uses it for controlling the collision detect circuit and modem circuit.

Z $\overline{\text{LCS}}$ (Link controller chip select), Output
Pin 76
A chip select signal for the link controller (ADLC) in which the sub CPU synchronizes with the DMCA.

[$\overline{\text{IRQ}}$ (Interrupt request from ADLC), Input
Pin 75
An Interrupt request from the link controller (ADLC).

∴ E (Enable clock to ADLC), Input
Pin 74
Link controller (ADLC) enable clock which the sub CPU synchronizes with the DMAC for data read to write.

] RS0 (Register select 0), Outpt
Pin 79
Command and status register select signal for the link controller (ADLC).

⊥ RS1 (Register select 1), Output
Pin 78
Command and status register select for the link controller (ADLC) which is used in conjunction with RS0 above.

_ MSK (Mask signal), Output
Pin 80
Used to mask the signal to avoid DMA looping, except for other than the data transmit/receive DMA request signal (input from the link controller (ADLC), normally).

‾ COL (Collision detect signal), Input
Pin 65
To avoid collision on the line, the data sent, from this side are compared with the data on the line. In other words, when the data sent are equal to the on line, no collision is assumed existing. If not equal, an occurrence of data collision is assumed. This line is, therefore, the input of the data sent from this side.

α TM0 (Timer 0), Input
Pin 9
A clock of a given interval (100 msec) sent from the subsystem's timer and counter. It is used to create the carrier off wait signal and back-off timer within the controller.

β TM1 (Timer 1), Output
Pin 10
Back-off timer output is a clock pulse ten times the TM0 frequency (T1=10xT0), where T1 is TM 1 clock and T0 is a TM0 clock.

- Sub CPU read timing chart

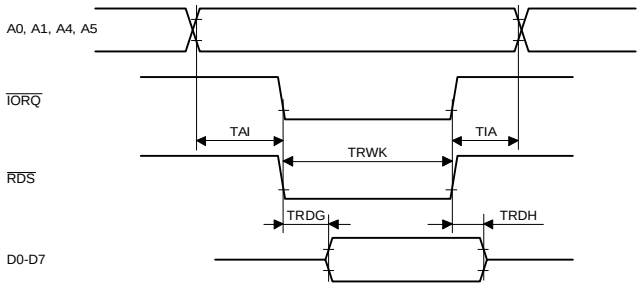


Fig. 10

- Sub CPU write timing

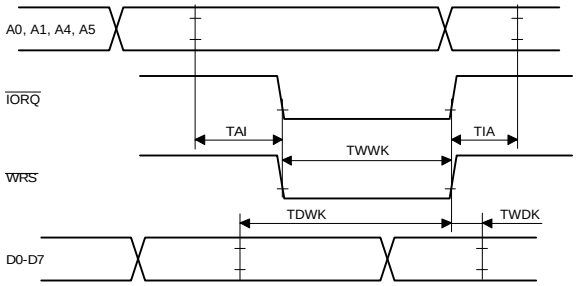


Fig. 11

- Sub DMA memory write timing

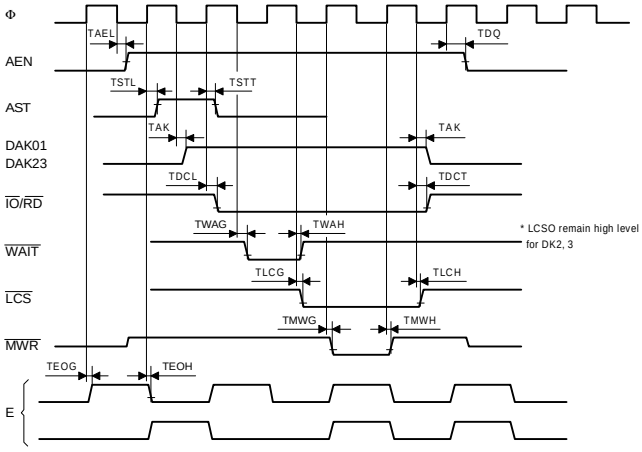


Fig. 12

- MRD timing

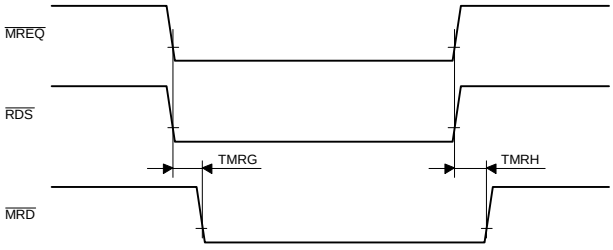


Fig. 13

- MWR timing

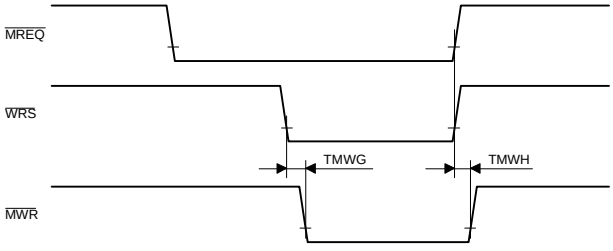


Fig. 14

- CLK

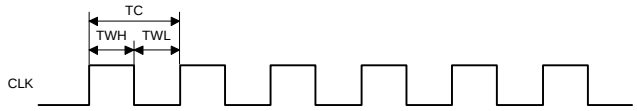


Fig. 15

- A8, A9, A10, A15 timings

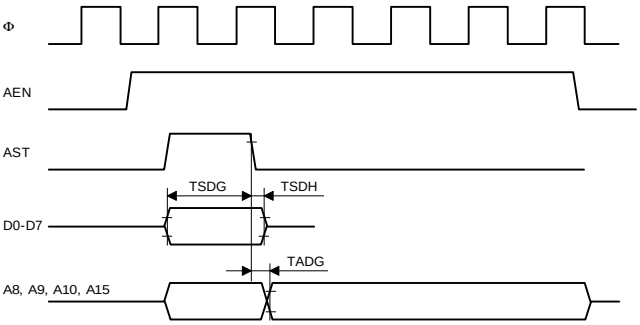


Fig. 16

- MSK, RSO timings

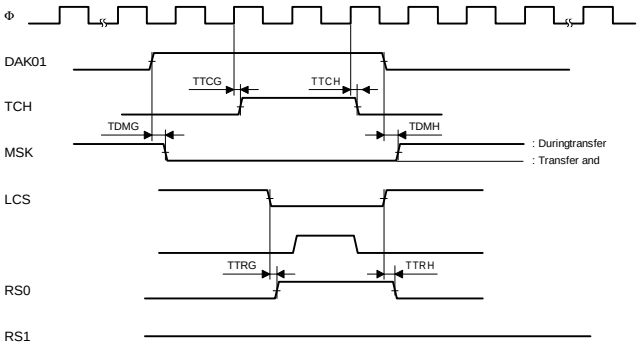


Fig. 17

- TXC, TDI timings

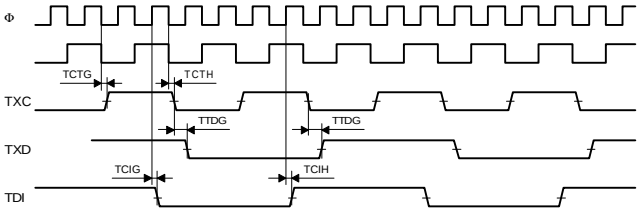


Fig. 18

- RXC, RXD timings

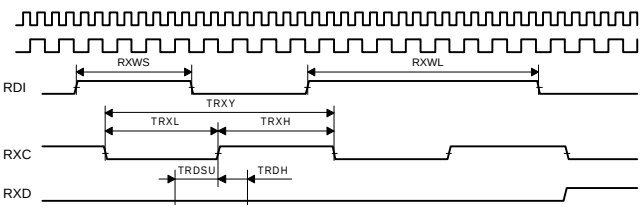


Fig. 19

- Collision generation time

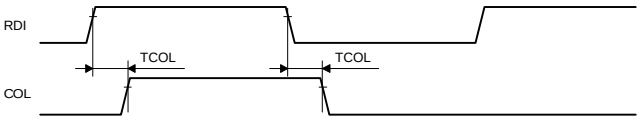


Fig. 20

4. Description of the DMA controller (DMAC; μPD8257-2)

The μPD8257 DMAC is a signal-chip, programmable DMA controller designed to control DMA transfers between the I/O devices and memory. The following outlines the DMAC operations:

1) DMA Opretion

Data transfer between I/O devices and memory is normally done via the CPU (see Fig. 21).

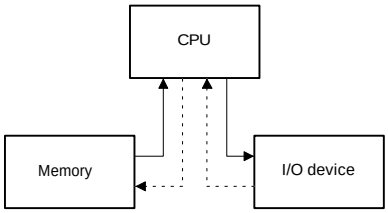


Fig. 21

The memory contents are temporarily stored in the CPU's internal register before being written into an I/O device at the next step.
In contrast, the DMA controller allows data to be directly transferred between memory and I/O devices without the CPU (See Fig. 22).

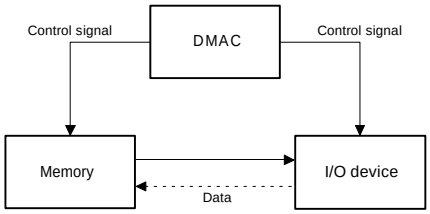


Fig. 22

The DMAC (8257) permits data transfers only between memory and I/O devices. (Some type of DMACs allow data transfer between memories).

2) Actual DMAC Operations

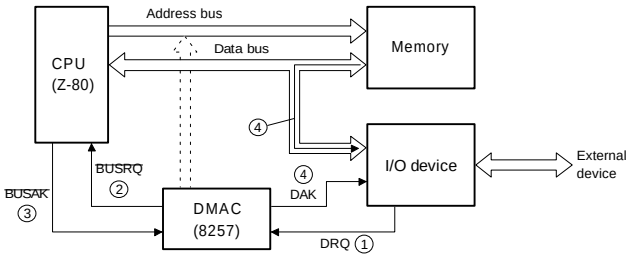


Fig. 23

Transfer from memory to I/O device

1 When the CPU wants to start a DMA cycle, it sets the number of bytes to be transferred and the first address of the tansfer memory area into the registers within the DMAC. The applicable I/O device issues a DMA Request (DRQ) to the DMAC.

2 Receving the DRQ signal, the DMAC issues a $\overline{\text{BUSRQ}}$ (Bus Request) to the CPU to request for bus access control.

3 Upon receipt of the $\overline{\text{BUSRQ}}$, the CPU floats both data and address buses and returns a $\overline{\text{BUSAK}}$ to the DMA as soon as it completes the current instruction execution cycle.
Bus access control is now passed to the DMAC.

4 The DMAC creates as memory Chip Select signal from the address bus, and outputs the transfer data address and RD signal to place the transfer data onto the data bus. At this point the DMAC issues a DAK (DMA Acknowledge) to the I/O device to let to the I/O device read the memory data on the data bus. The above sequence is repeated until a single DMA cycle is completed.

* On this board, DMA transfer is performed between the ADLC and memory, and between memory and MB62H149.
The DAK01 (pin 37) and DAK23 (pin 41) of the MB62H149 are the results of the logical OR of DAK0 with DAK1 and DAK2 with DAK3 of the DMAC, respectively. The DMAC's DAK is controlled by the MB62H149.

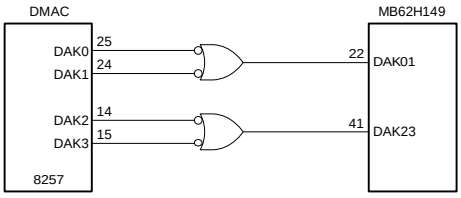


Fig. 24

DAK01 is used for the DMA cycle for data transfer, while DAK23 is used for data transfer with the host processor.

3) DMAC (8257-2) Pin Functions

Pin No.	Signal name/in-out/Description
1	$\overline{\text{I/OR}}$ (I/O Read) – Active Low Input/output (3 state) This pin functions as an input when is Slave mode. Application of a Low level to this pin reads the 8-bit status register value or the upper/lower byte of the 16-bit DMA address register or 16-bit TC regsiter. When in the Master mode this pin serves as a control output, which allows the device to receive data from an I/O device during the DMA write cycle.
2	$\overline{\text{I/OW}}$ (I/O Write) – Active Low input/output (3 state) This pin function as an input when in Slave mode. Application of a Low level to this pin enables the data to be loaded into the 8-bit mode set register or the upper/lower byte of the 16-bit DMA address register or TC register. When in the Master mode this pin serves as a control output, which allows the device to write data into an I/O device.
3	$\overline{\text{MEMR}}$ (Memory Read) – Active Low output (3 state) This pin is used to enable to be read from the addressed memory location during DMA read cycle. It is set to a high impedance when in the Slave mode.
4	$\overline{\text{MEMW}}$ (Memory Write) – Active Low output (3 state) This pin is used to enable data to be writen in to the addressed memory location during DMA write cycle. It is set to high impedance when in the Slave mode.
5	MARK (Mark) – Output This pin is used to indicate to the selected I/O device that the current DMA cycle is the 128th cycle as counted from the preceding MARK. A MARK always occurs at every 128 cycles as counted from the end of a data block. It occurs at every 128 cycle as counted from the beginning of a data block only if the total number (n) of DMA cycles is an integral multiple of 128 (and the value (n-1) is loaded in the TC register).
6	READY (Ready) – Input If the low-speed memory used requires an extended memory cycle, appliyng an asynchronous Low level signal to this pin causes the DMAC to place wait cycles on its internal state to extend the memory read/write cycle.
7	HLDA (Hold Acknowledge) – Input This pin accepts an BUSAK signal returned from the CPU (Z-80) when the CPU acknowledges a hold request. The signal indicates that the DMAC (μPD8257) has acquired bus access control. Once this signal is returned, the bus outputs of the CPU are set to high impedance.
8	ADDSTB (Address Strobe) – Output This pin is normally connected to the STB Input of the μPD8212 as a strobe, which is used to write the upper byte of memory address from the data bus into the μPD8212 .
9	AEN (Address Enable) – Output This pin is used to set the address and control bus outputs of the Z-80 CPU to high impedance if needed. It may also be used to disable the system address bus by using the enable input of the address bus driver within the system. This is to disable any response from non-DMA devices during the DMA cycle. It may also be used to disconnect the μPD8257's data bus from the system data bus, so that no special timing restriction be required for the sytem bus when the μPD8257 wants to transfer the upper byte of DMA address through its data bus. When the μPD8257 is used for I/O device configuration (in contrast to memory map configuration), this AEN output is disabled so that an I/O device is not selected when a DMA address is pleaced on the address bus. An I/O device must be selected bye the DMA acknowledge output to the four channels.
10	HRQ (Hold Request) – Output This pin is used to request system bus access control. It is connected to the BUSRQ input of the Z-80 when only one chip of μPD8257 is used in the system. When two or more chips are used, an additional priority encoder is required to assign priority to the multiple HRQ signal lines.
11	$\overline{\text{CS}}$ (Chip Select) – Active Low input When in the Slave mode, this pin enables the I/O Read or I/O Write input of the μPD8257 when the device is to be read or written, respectively. When in the Master mode, the $\overline{\text{CS}}$ is automatically disabled to prevent the device itself from being selected during DMA operation.
12	CLK (Clock) – Input Clock in (4MHz)
13	RESET (Reset) – Input This pin normally accepts an asynchronous Reset output from the CPU. The Reset signal resets all control signals and places the device into the Slave mode. Once a Reset signal is received, the μPD8257 aborts its current operation regardless of the device status and enters the Idle set (SI).
25, 24, 14, 15	$\overline{\text{DACK0}}$-$\overline{\text{DACK3}}$ (DMA Acknowledge) – Active Low output These pins indicate to the I/O devices attached to the respective channels that the DMA cycle has been acknowledged.
19 – 16	DRQ0-DRQ3 (DMA Request) – Input These Pins are independent, asynchronous DMA request channels used for I/O devices to request DMA cycle to the μPD8257. DRQ3 has the lowest priority, while DRQ0 has the highest, as long as the Rotary Priority mode is not selected. DRQn input is kept high until a $\overline{\text{DACK}}$n is received. During the Multi DMA Cycle mode (Burst mode), DRQn is kept high until the $\overline{\text{DACK}}$n for the last cycle is received.

Pin No.	Signal name/in-out/Description
30 – 26 23 22, 21	DO-D7 (Data Bus) – Input/output (3 state) When the μPD8257 is programmed by the CPU (Z-80), the data bus accepts the upper/Lower byte of DMA address and TC register value output from the CPU, or 8-bit data to be loaded into the Mode Set register (Slave mode). When the CPU wants to read the value of the DMA address register, TC register, or status register, the data bus is used to transfer the pertinent data value to the CPU (Slave mode). During the DMA cycle (when the μPD8257 is bus master), the data bus is used to transfer the upper byte of memory address from a DMA address register to the μPD8212. This address byte is transferred at the beginning of a DMA cycle. The data bus is subsequently used to transfer memory data in the remaining portion of the DMA cycle.
32 – 35	A0-A3 (Address Bus) – Input/output (3 state) When in the Slave mode, these pins serve as inputs to select a register to be read or written. Hen in the Master mode, these pins output the lower 4 bits of 16-bit memory address.
37 – 40	A4-A7 (Address Bus) – Output (3 state) When in the Master mode, these pins output bits 4-7 of the 16-bit memory address. Hen in the Slave mode, these pins are ser to high impedance.
36	TC (Terminal Count) – Output The TC output Indicates to the currently selected I/O device that the current DMA cycle is the last cycle of the data block. If the TC stop bit of the Mode Set register is set, the selected channel will be automatically disabled at the end of the DMA cycle. The TC signal is output when bit 14 of the TC register on the selected channel is reset to zero. The value (n-1) must be loaded in the lower 14 bits of the TC register, where "n" is the number of DMA cycles to be executed.

5. Oscillator Circuit

The LSI system clocks and transfer clocks for the ER-52TR system are obtained by dividing a single master clock. The master clock (16.0 MHz) is applied to the CLK pin (pin 1) of the MB62H149, where it is divided into system clocks for the individual LSI chips. The resulting clocks of ϕ(4MHz) and TXC (1 or 0.5 MHz) appear at pins 8 and 71,, respectively.

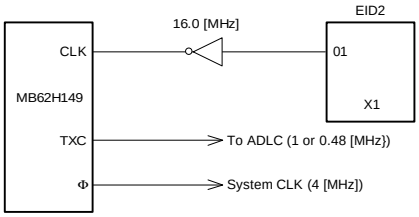


Fig. 25

6. Serial/Parallel Conversion for Data Transmission

1) General

Since a serial synchronous transmission scheme is used for SRN communications, serial/parallel conversion is equired on the sen d/receive data. The serial/parallel converter circuit uses an MC68B54 Advanced Data Link Controller (ADLC). The ADLC converts D0-D7 parallel data into serial data in synchronicity with the TXC signal (pin 5), and converts serial data (RXD) into parallel in synchronicity with the RXC signal (pin 4).

Pin No.	Symbol	Pin name and function	Input/ Output
1	VSS	Ground pin	–
2	$\overline{RTS}$	This pin indicates that send data exists in the TxFIF0. If CR2b7 is set to one, this output is set to Low. This pin is set to High when a Close flag has been transmitted after a frame is completed, an Abort is transmitted, CR2b7 is reset in the Mark Idle state (RTS remains at Low if CR2b7 is reset to zero in any state other than the Mark Idle state), or the $\overline{RESET}$ input is held at Low. (Requeset Data Input)	Out
3	RXD	Receiver Data input to accept received data. (Receiver Data Input)	In
4	RXC	Receiver Clock input to accept a synchronization signal for the received data input. (Receiver Clock Input)	In
5	TXC	Transmitter Clock input, used to synchronize the transmit data output. When in the Loop mode (including Test mode), the signal at this pin must be in-phase with the RxC. (Transmitter Clock Input)	In
6	TXD	TRansmit Data output. (Transmit Data output)	Out
7	$\overline{IRQ}$	Interrupt Request output. This pin is set Low if an interrupt occurred and the corresponding Enable bit is set. It is set High when the cause of the interrupt is removed or the Enable bit is reset. (Interrupt Request Output)	Out
8	$\overline{RESET}$	RESET input. If a Low signal is applied to this pin, the RxReset (CR1b6) and TxReset (CR1b7) are set to one, which resets the Rx and Tx circuits, respectively. The TxAbort (CR4b5), $\overline{RTS}$ (CR2b7), Loop Mode (CR3b5), and Loop on Line/DTR (CR367) are reset to zero. All initial status conditions are reset. The $\overline{RTS}$ and $\overline{LOC/DTR}$ output pins are set to High when the corresponding control registers are reset, and the TxD output is placed in Mark Idle state. While the $\overline{RESET}$ inputs is kept at Low, none of the control register bits mentioned above can be updated. If the RESET input is set to High, the reset condition continues until CR1b6 and CR1b7 are reset to zeros by software. (RESET Input)	In
9	$\overline{CS}$	Chip Select input. Read/write access to the device is enabled only if this input is Low and the Enable input is High. (Chip Select Input)	In
10 11	RS0 RS1	Register Select inputs. These inputs are used with the R/W input (CR1b0) to address a register within the device for read/write access. (Register Select Input)	In
12	R/W	Read/Write Control input used to indecate tha direction of the data flow. The Data I/O buffer is placed in the Output mode if this input is High; it is placed in Input mode if this Low. (Read/Write Control Input)	In
13	E	Enable Clock input used to time the CS, RS0, RS1, and R/W inputs. Data read/write access to the device is enabled only if this input is kept high. This pin is also used for data transfer through the RxFIFO of TxFIFO. (Enable Clock Input)	In
14	VCC	This pin accepts a +5V power supply. (Voltage Source)	I/O
15 ~22	D7 – D0	Bidirectional data bus used to transfer data with the system. It is a three-state bus except during Read access. (Data Bus)	I/O
23	RDSR	Receive Data Service Request output. This pin reflects the value of ST1b0. A high state of this pin indicates that the RxFIFO is in request for service. When the RxFIFO is read, the RDSR outputs is reset to Low. (The RxFIFO here refers to the one (CR2b1 = 0) or two (CR2b1 = 1) nearest to the data bus.) When in the Preferred Status mode (CR2b0 = 1) , this pin is kept Low as long as the other status condition exists. (Receive Data Service Request Output)	Out
24	TDSR	Transmitter Data Service Request output. This pin outputs the value of ST1b6 in any mode other than the FC mode (CR2b3 = 1). A high state of this pin indicates that the TxFIFO requests service. When data is written into the TxFIFO, the RDSR is reset to Low. (The TxFIFO here refers to the one (CR2b1 = 0) or two (CR2b1 = 1) nearest to the data bus.) This pin is kept Low when the $\overline{RESET}$ pin is at an active Low. $\overline{CTS}$ pin is High, or CR1b7 is High. When in the Preferred Status mode (CR2b0 = 1), this pin is also kept High if the Tx-Underrun condition exists. (Transmitter Data Service Request Output)	Out
25	$\overline{FD}$	Flag Detect output. This pin remains Low for a one-bit time interval (while Receiver Clock = RxC) after the last flag bit is detected. (Flag Detect Output)	Out

Pin No.	Symbol	Pin name and function	Input/ Output
26	$\overline{\text{LOC}}$/$\overline{\text{DTR}}$	Loop On Line Control/Data Terminal Ready output. This pin functions as the $\overline{\text{DTR}}$ in any mode other than Loop mode (CR3b5 = 0). It is set Low if CR3b7 is set to one, and is set High when the same bit is set to zero. When in the Loop mode (CR3b5 = 1), this pin functions as the $\overline{\text{LOC}}$, which is used to control the external loop interface hardware between On Loop and Off Loop. If CR3b7 is set to zero, this pin is set High when RxD = 01111111 is detected, causing the hardware to go into the On Loop. If CR3b7 is set to zero, this pin is set High when RxD = 11111111 is detected, causing the hardware to return to the Off Loop. If the $\overline{\text{RESET}}$ input is set Low, CR3b5 is set to zero (Non-Loop Mode), which sets CR3b7 to zero. As a result, this pin issues a High level signal. (Loop On Line Control/Data Terminal Ready Output)	Out
28	$\overline{\text{CTS}}$	Clear to Send input. Setting this pin to High disables ST1b6 and related IRQ. If SR1b4 is set and this pin is enabled, an IRQ is issued. Low-to-High transition at the CTS input is set in SR1b4, which is cleared by CR2b6 or CR1b7. (Clear to Send Input)	In
27	$\overline{\text{DCD}}$	Loop On Line Control/Data Terminal Ready output. Setting this pin to High resets the Receiver register and sets SR2b5, which causes an IRQ to be issued if enabled. Low-to-High transition at the DCD input is set in ST2b5, which cleared by CR2b5 or CR1b6. (Loop On Line Control/Data Terminal Ready Output)	In

3) Pin Configuration (top view)

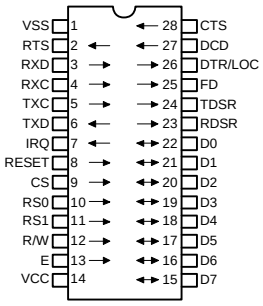


Fig. 26

7. Modulator/Demodulatro circuit

Phase encoding (PE) modulation is used for SRN communications.
The PE modulation has a changing point in the signal at the center of the bit, the timing signal is regenerated from this signal, making the modulation and demodulation simpler by providing continuous signals for the DC conponents.

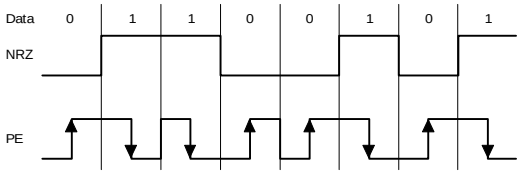


Fig. 27 PE Modulation

Serial send data applied from the ADLC to TXD (pin 72) of the MB62H149 and the TXC synchronization signal is subject to PE modulation. The resulting signal is output through TDI (pin 67) of the MB62H149 to the transmission driver.
Received data is applied from the receiver to RDI (pin 66) of the MB62H149, where it is demodulated into serial receive data and synchronization clock. They are output to the ADLC through RXS (pin 70) and RXC (pin 69), respectively.
The modulator and demodulator are located within the MB62H149.

8. Transmitter and Receiver Circuits

1) Transmitter

The modulated send data output through TDI (pin 67) of the MB62H149 is controlled by the RTS (Request to Send) signal transferred from the ADLC during transmission.
The TDI is NAND'ed with RTS, so that data transmission is disabled when the RTS is high.
RTS is Low state during transmission and Transistor Q2 is turned ON. When transmitting data "1", the output at pin 12 of the NAND gate (IC7) is set Low. (the RTS is Low) Since pin 11 of the following transistor (IC7) is set Low, it is turned off.
When hte RTS is set Low, transistor Q1 turned on through an inverter, which applies a bese current to Q2, turnit it on. When Q2 and pins 10 and 9 of IC7 are turned on, the output transistors IC7 (pins 6 and 5) are turned on. Since the output trasistors are common-emitter circuit, data "1" is obtained at LINE.

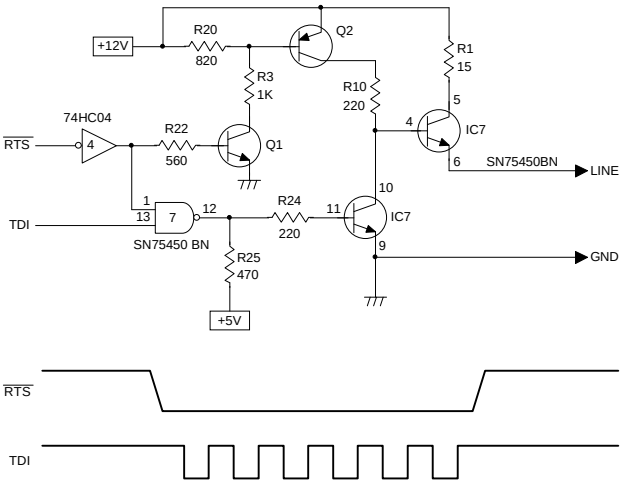


Fig. 28

2) Receiver

The receiver provides the following two functions:

1) Data reception

2) Collision detection

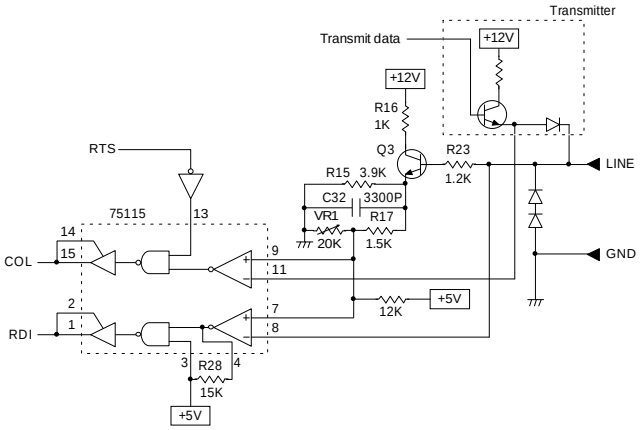


Fig. 16-29

1 Data reception
The 75115 is a dual-channel receiver containing two comparators. One of the comparators is used to detect received data (RDI). The data received from the line is applied to the negative input (pin 5) of the comparator. The received data is also amplified by Q3, integrated by R15 and C32, and voltage-divided by R17 and VR1 before being applied to the positive input (pin 7) of the same comparator, This assures reliable identification of "0" and "1" levels even if the received data signal is distorted due to a lond line length.

Note: If Transistor Q1 is replaced for servicing, the VR1 requires readjustment. See the section for adjustment.

2 Collision detection

The other comparator in the 75115 is used for collision detection. The SRN communication uses only a single transmission line, and the transmission line is connected to each terminal. Only one pair of terminals can communicate with each other over the transmission line at a time. If the transmission line is busy, other terminals must wait to transmit until the line becomes available. The line busy condition is monitored by the collision detector. The line signal is applied to the positive input (pin 9) of the comparator, while the local send signal is applied to the negative input (pin 11) of the same comparator, so that correct transmission can be monitored by comparing the line signal with the transmission signal. If two terminals attempt transmission at the same time, data collision will occur on te line, which results in the line signal being different from the local transmission signal. Detecting this difference, the collision detector outputs a COL signal to indicate it to the CPU.

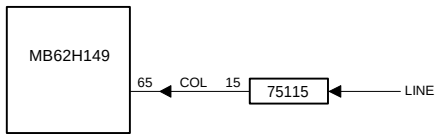
9. Collision detect circuit

The access system employs the carrier sense multiple access with collision detect (CSMA/CD) with a BUS type topology. The access system has no control station on the network and checks the space area condition of the circuit according to the prosece is available.
Collision is detected sometimes due to the delay on the circuit or the simulataneous data sending, but the collision is detected immediately by the collision detect circuit and prevents the deterioration of the transmission efficiency by ptoviding the backoff process (binary exponential backoff). The carrier sence is detected by the two stages of the dta packet and response packet to prevent the collision of the response packet. This permits higher efficiency for heavy loads.
Collision detect circuit is located within the MB62H149 custom LSI.

10. Carrier detect circuit

This circuit detects whether data is flowing on the transmission line. It consists of a circuit which immediately senses a no data status on the line.

Fig. 30



When data is not on the line the circuit functions to sense an elapse of the fixed time rate the immediate sensing circuit is used for response testing and the delayed sensing circuit is used for data testing.
This circuit is located within MB62H149 custom LSI.

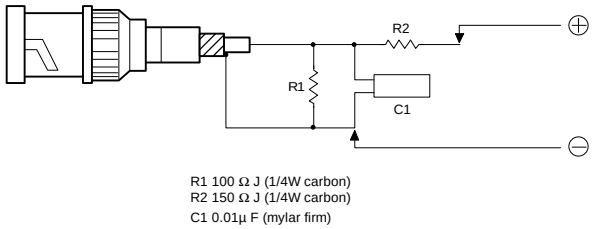
11. ADJUSTMENT FOR SRN (IN-LINE) INTERFACE BOARD

If transistor Q3 in the transmitter/receiver section has been replaced or if the SRN level requires readjustment, the following alignment is required:

1) Tools and Instruments Required

1 Oscilloscope (50MHz or better) 1
2 ER-A570 1
3 ER-A57R1 1

2) Dummy Network Specifications



R1 100 Ω J (1/4W carbon)
R2 150 Ω J (1/4W carbon)
C1 0.01µ F (mylar firm)

Fig. 1 Dummy network

The oscillator should be connected to the points indicated by ⊕ and ∃ .
⊕: Connect the positive side of the oscillator.
∃ : Connect the negative side of the oscillator.

3) Connections

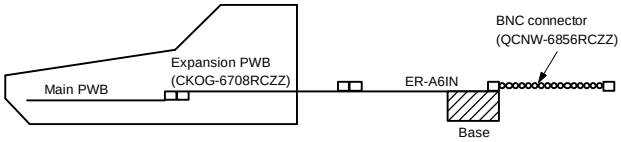


Fig. 2

1 Attach the expansion PWB (CKOG–6708RCZZ) to the main PWB.
2 Attach the ER-A6IN to the expansion PWB. (Place a base under the ER-A6IN to stabilize it.)
3 Attach the BNC connector (QCNW–6856RCZZ) to the ER-A6IN.

4) Alignment Procedure

1 When Using an Oscillator

a) Checking the 1MHz oscillator output

Using an oscilloscope check the 1MHz oscillator's output waveform.

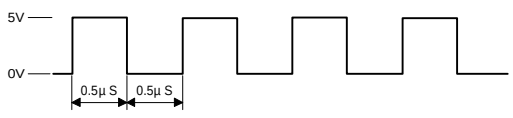


Fig. 3 1MHz oscillator output waveform

NOTE: The oscillator used should have an output impedance of 50Ω.

b) Connecting the oscillator and its adjustment

Connect a dummy network or branch-trunk network on to the output of the ER-A6IN installed in the ER-A570, and connect the oscillator to the dummy or branch-trunk network.

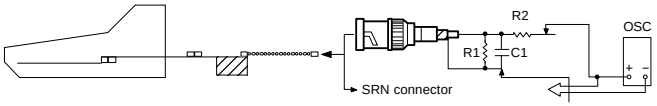


Fig. 4 Connection

∗ Waveform adjustment

Adjust VR1 until the signal waveform as shown in Fig. 5 is obtained across TP (pin 1 of the 75115) and GND pin.

Turning VR1 clockwise extends the interval of T1.

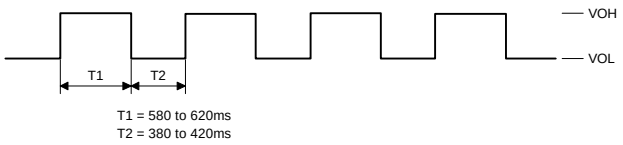


Fig. 5 Receiver regeneration waveform (with dummy network)

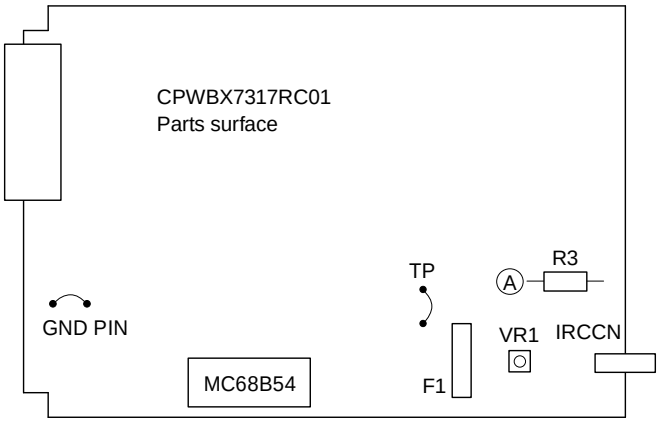


Fig. 6 Board location

2 When the Branch Trunk Network and Two ECR'S are Available.

a) Connecting terminals

Both ends of the network must be terminated with a 50Ω terminator. If only two active terminals are to be tested and left on the network, disconnect all other terminals from the network. (In this case as well, both ends of the trunk network must be terminated with 50Ω).

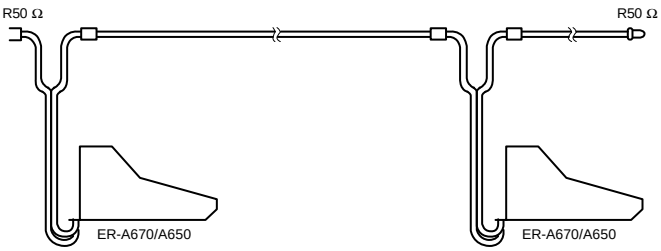


Fig. 7 Terminal connection

b) Receive level adjustment

i) Turn on both the objective terminal of receive level adjustment (receiver terminal) and the terminal which sends the adjusting signal (transmitter terminal).

ii) Run the diagnostic program JOB#603 on the transmitter terminal to send a flag.

Key operations: MODE switch: SRV position

601 → TL

iii) Checking transmitter terminals' output waveform

Using an oscilloscope, check the transmitter terminal's output signal waveform.

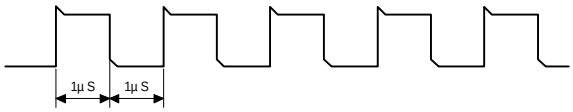


Fig. 8 Transmitter terminal's output waveform (at transmitter output)

At the receiver terminal, the transmitter terminal's output waveform is subject to attenuation and distortion due to the length of the trunk cable (this depends on the characteristics of the cable itself).

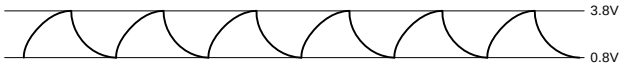


Fig. 9 Example of distorted signal waveform at the receiver terminal (RG58/U 400m)

With the receiver terminal adjust VR1 (5kΩ) on the ER-A6IN board until the waveform as shown in Fig. 10 is obtained at TP (pin 1 of the 75115). (For the location of VR1, see Fig. 6 Board location of this subsection).

Clockwise rotation of VR1 extends the High level pulse width of the signal at TP (pin 1 of the 75115).

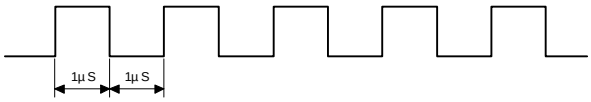


Fig. 10 Waveform at TP (pin 1 of the 75115 IC in the receiver terminal)

5) Other Checks (These Checks should be done After the Receive Level Adjustment is Completed).

1 Line driver bias control circuit

Make sure that the voltage at the A-side lead of the R3 resistor (150Ω, 3W) shown in Fig. 6 is properly switched.

Procedure:

i) Connect a terminating resistor or read network to the BNC connector, QCNW-6856RCZZ (Fig. 2).

ii) Run the diagnostic program JOB#604, and make sure that the voltage at point A (in Fig. 6) is switched as shown in Fig. 10.

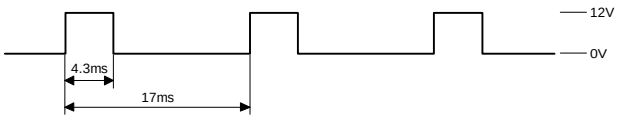


Fig. 11 bias circuit switching waveform

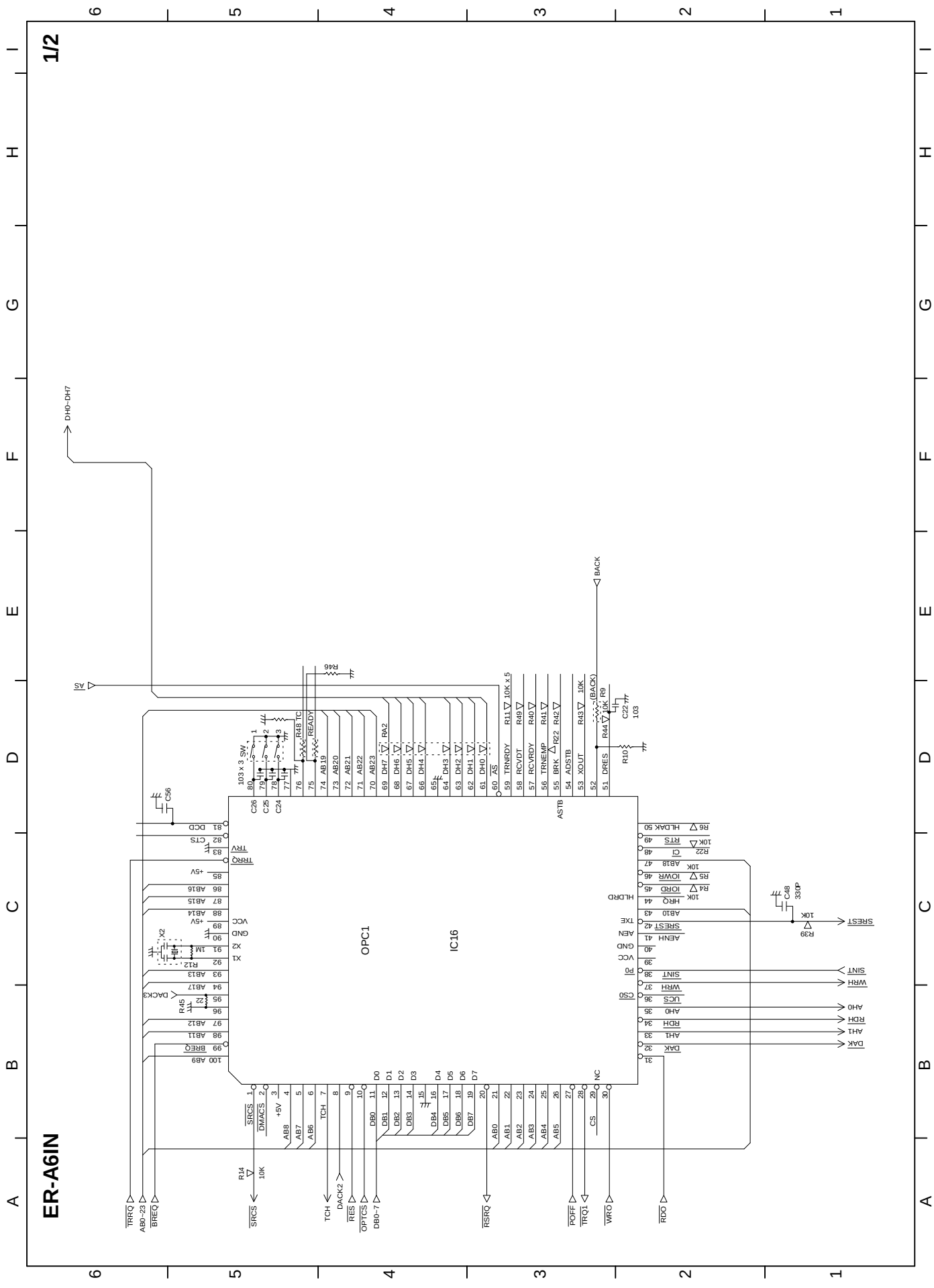
Key operation:

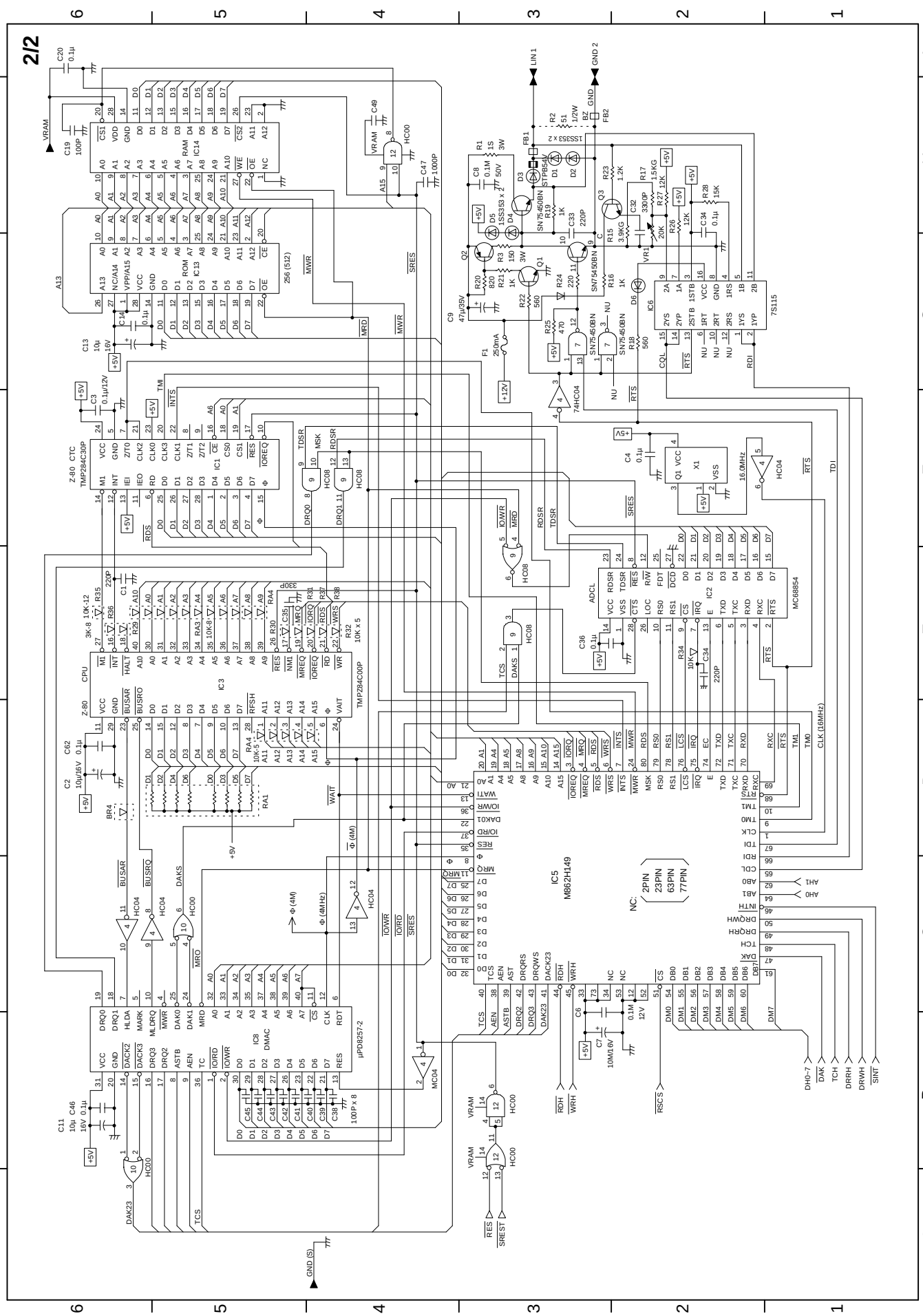
602 → TL

iii) If the waveform as shown in Fig. 15 is not obtained, it is most probable that transistor Q3 (2SA509) is defective.

2 For the other check items, refer to III. TEST FUNCTION.

12. Circuit diagram




2/2
Z-80 CPU
Z-80 CTC
TMPZ84C00P
TMP284C-30P
μPD8257-2
IC5
M862H149
MC68854
7S115
74HC04
HC00
HC04
HC08
HC32
HC86
HC138
HC244
HC245
HC373
HC374
HC688
VRAM
RAM IC14
ROM IC13
256 (512)
2PIN
23PIN
63PIN
77PIN
NC:
CLK (16MHz)
16.0MHz
+5V
+12V
GND
GND (S)
MRD
MWR
IORD
IOWR
SRES
RES
SREST
RDH
WRH
RSC5
DH0~7
DAK
TCH
DRRH
DRWH
SINT

ER-A6IN

OPTCN1

SIGNAL	No.	No.	SIGNAL
GND	1	35	GND
GND	2	36	GND
$\overline{\text{RDO}}$	3	37	(ϕ)
$\overline{\text{WRO}}$	4	38	NU1
+5V	5	39	$\overline{\text{BREQ}}$
+5V	6	40	$\overline{\text{BACK}}$
A23	7	41	$\overline{\text{TRQ2}}$
A22	8	42	$\overline{\text{TRQ1}}$
A21	9	43	$\overline{\text{EXINT1}}$
A20	10	44	$\overline{\text{EXINT0}}$
A19	11	45	$\overline{\text{TRRQ}}$
A18	12	46	$\overline{\text{RSRQ}}$
A17	13	47	$\overline{\text{RFSH}}$
A16	14	48	$\overline{\text{IPLON}}$
A15	15	49	D7
A14	16	50	D6
A13	17	51	D5
A12	18	52	D4
A11	19	53	D3
A10	20	54	D2
A9	21	55	D1
A8	22	56	D0
A7	23	57	$\overline{\text{POFF}}$
A6	24	58	VRAM
A5	25	59	(+12V)
A4	26	60	A3
+24V	27	61	+24V
+24V	28	62	+24V
A1	29	63	A2
A0	30	64	$\overline{\text{RES}}$
$\overline{\text{RESET}}$	31	65	$\overline{\text{AS}}$
$\overline{\text{OPTCS}}$	32	66	NU2
GNDP	33	67	GND
GNDP	34	68	GND

OPTCN2

SIGNAL	No.	No.	SIGNAL
GND	1	36	GND
GND	2	37	GND
GND	3	38	GND
$\overline{\text{RDO}}$	4	39	(ϕ)
$\overline{\text{WRO}}$	5	40	NU1
$\overline{\text{BREQ}}$	6	41	+5V
$\overline{\text{BACK}}$	7	42	+5V
A23	8	43	$\overline{\text{TRQ2}}$
A22	9	44	$\overline{\text{TRQ1}}$
A21	10	45	$\overline{\text{EXINT1}}$
A20	11	46	$\overline{\text{EXINT0}}$
A19	12	47	$\overline{\text{TRRQ}}$
A18	13	48	$\overline{\text{RSRH}}$
A17	14	49	$\overline{\text{RFSH}}$
A16	15	50	$\overline{\text{IPLON}}$
A15	16	51	D7
A14	17	52	D6
A13	18	53	D5
A12	19	54	D4
A11	20	55	D3
A10	21	56	D2
A9	22	57	D1
A8	23	58	D0
A7	24	59	$\overline{\text{POFF}}$
A6	25	60	VRAM
A5	26	61	A3
A4	27	62	(+12V)
+24V	28	63	+24V
+24V	29	64	+24V
A1	30	65	A2
A0	31	66	$\overline{\text{RES}}$
$\overline{\text{RESET}}$	32	67	$\overline{\text{AS}}$
$\overline{\text{OPTCS}}$	33	68	NU2
GNDP	34	69	GND
GNDP	35	70	GND

IRCCN

No.	SIGNAL
1	LIN
2	GND

13. PWB layout

1 Parts side

2 Solder side

CHAPTER 2. ER-A5RS

1. General

The ER-A5RS is composed of the following blocks:

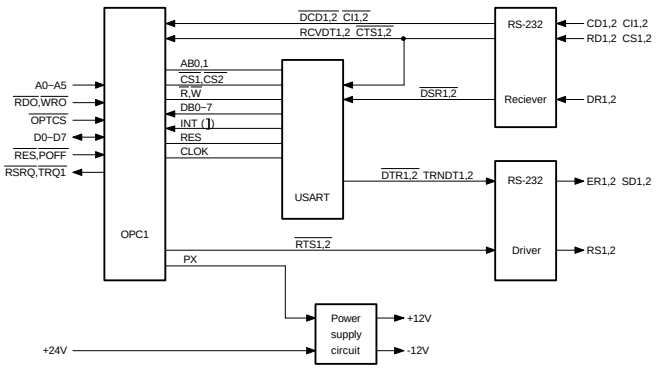
1) RS-232 receiver (75189A)

2) RS-232 driver (75188)

3) USART (MB89371A)

4) Gate array (OPC1: F256004PJ)

2. Block diagram



INT (⌋): TRNRDY1,2 RCVRDY1,2 TRNEMP1,2 BRK1,2

3. Description of main LSI

3-1. OPC1 (F256004PJ)

1) General description

The OPC1 is a gate array of integrated peripheral circuits of RS-232/Simple IRC interface.
One chip of the OPC1 is equipped with four communication circuits. (Three of them are for RS-232 only: UNIT 0 ~ 2, one is for selection of simple IRC/RS-232: UNIT 3)
The ER-A5RS uses UNIT0 (RS-232 interface) and UNIT7 (RS-232 interface).

UNIT NO.	Purpose	ER-A5RS
UNIT0	RS-232	Used.
UNIT1	RS-232	Used.
UNIT2	RS-232	Not used.
UNIT3	RS-232/Simple IRC	Not used.

Each UNIT of the OPC1 has the following functions:

1 Timer function
Used for the timer between characters in data reception.

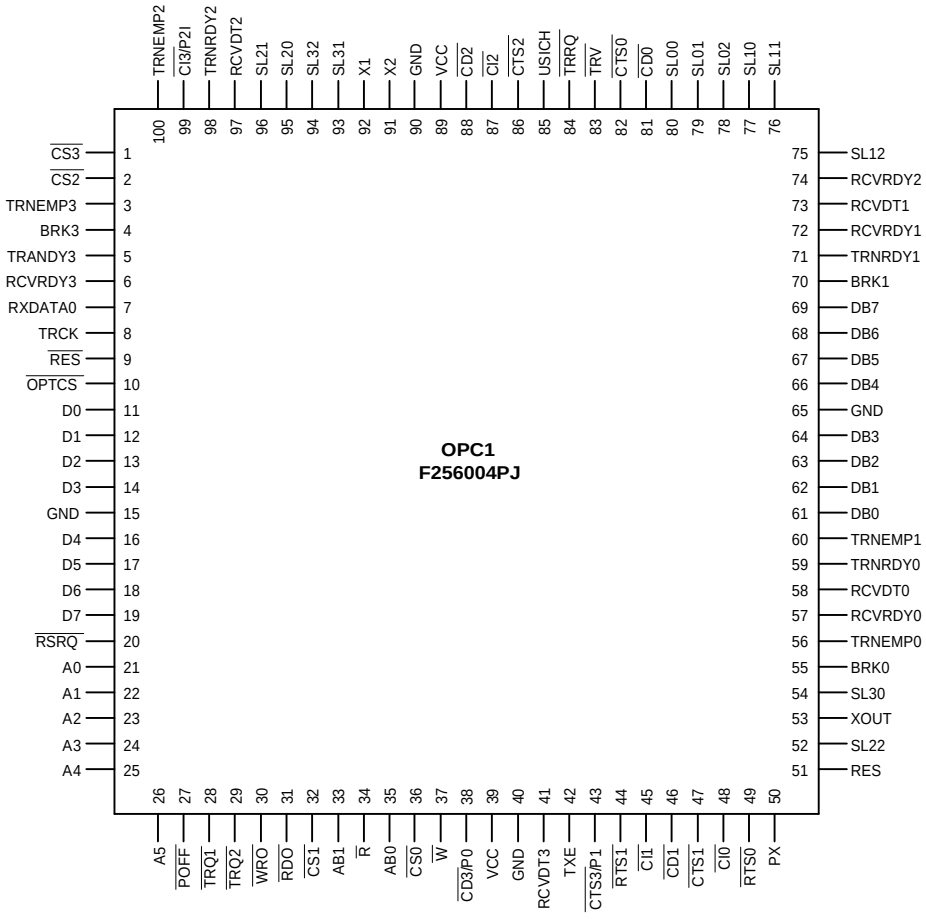
2 Address decode
USART chip select output and own select.

3 Interruption control
$\overline{RSRQ}$, $\overline{TRRQ}$ output using outputs from USART (TRNRDY, TRNEMP, RCVRDY, BRK) and RS-232 control signals ($\overline{CI}$, $\overline{CTS}$, $\overline{CD}$) as interruption factors.
(For the simple IRC, TRNEMP is excluded.)

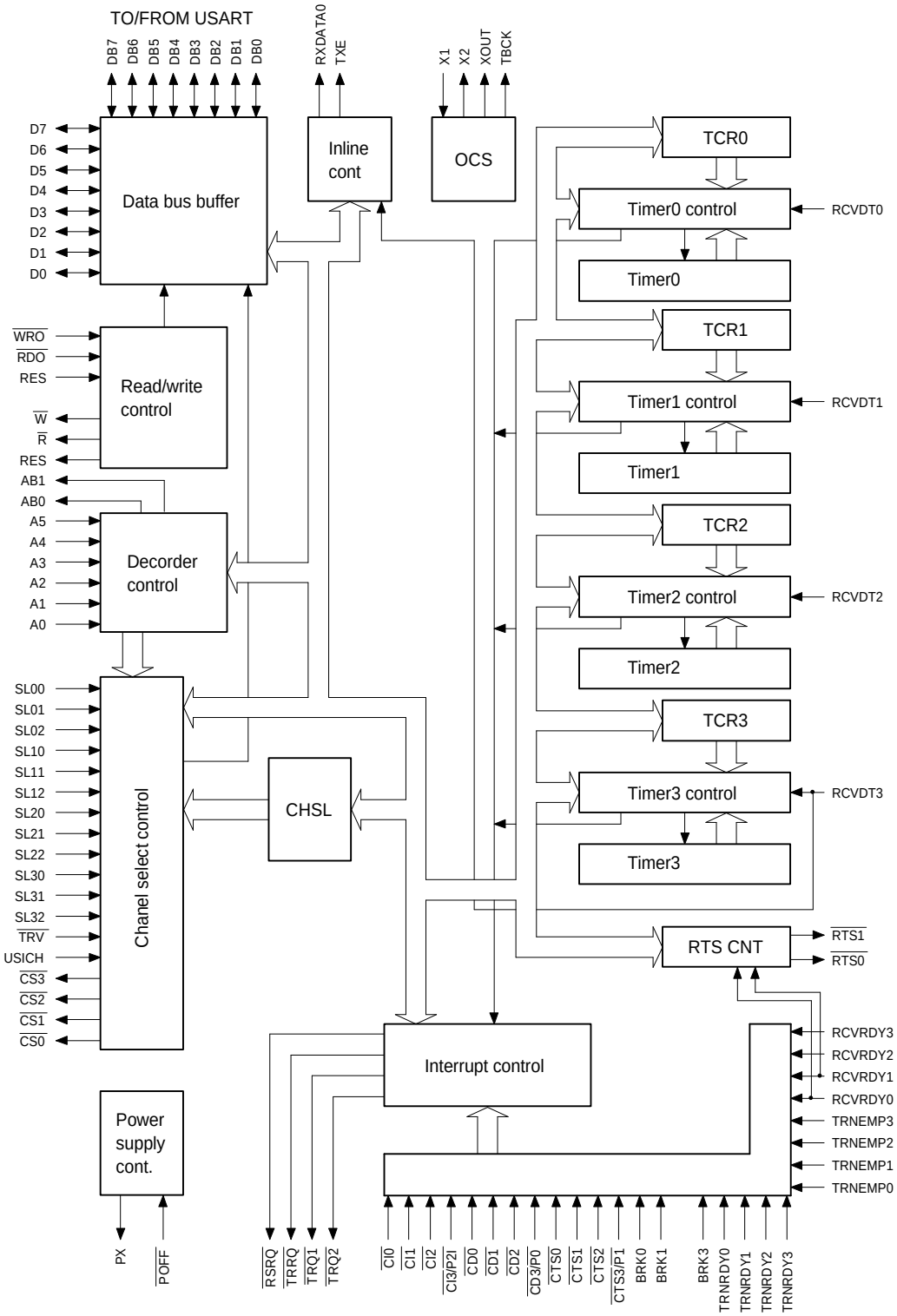
* $\overline{RSRQ}$: For RS-232
$\overline{TRRQ}$(Not used): For simple IRC

4 Simple IRC send/receive control (UNIT3 only) : Not used

2) Pin configuration



3) Block diagram



4) Pin description

OPC1 pin table

The signals marked with "-" at the end are LOW active signals. Example: "CS1-" = "$\overline{CS1}$"

No.	Pin No.	Pin name	I/O	Pin	ER-A5RS	Description
1	80	SL00	I	ICU	SL00	RS-232/UNIT0 channel select
2	79	SL01	I	ICU	SL01	
3	78	SL02	I	ICU	SL02	
4	77	SL10	I	ICU	SL10	RS-232/UNIT1 channel select
5	76	SL11	I	ICU	SL11	
6	75	SL12	I	ICU	SL12	
7	95	SL20	I	ICU	GND	RS-232/UNIT2 channel select
8	96	SL21	I	ICU	GND	
9	52	SL22	I	ICU	GND	
10	54	SL30	I	ICU	GND	RS-232/UNIT3 channel select
11	93	SL31	I	ICU	GND	
12	94	SL32	I	ICU	GND	
13	36	CS0-	O	O	CS1-	RS-232 USART chip select
14	32	CS1-	O	O	CS2-	
15	2	CS2-	O	O	NC	
16	1	CS3-	O	O	NC	RS-232/INLINE USART chip select
17	81	CD0-	I	IS	DCD1-	RS-232 control signal CD- input
18	46	CD1-	I	IS	DCD2-	
19	88	CD2-	I	IS	GND	
20	38	CD3-/P0-	I	IS	GND	RS-232 CD-/INLINE P0-
21	82	CTS0-	I	IS	CTS1-	RS-232 control signal CTS- input
22	47	CTS1-	I	IS	CTS2-	
23	86	CTS2-	I	IS	GND	
24	43	CTS3-/P1-	I	IS	GND	RS-232 CTS-/INLINE P1-
25	48	CI0-	I	IS	CI1-	RS-232 control signal CI- input
26	45	CI1-	I	IS	CI2-	
27	87	CI2-	I	IS	GND	
28	99	CI3-/P2I	I	IS	GND	RS-232 CI-/INLINE P2I
29	55	BRK0	I	ISC	BRK1	RS-232 USART BREAK signal
30	70	BRK1	I	ISC	BRK2	
31	27	POFF-	I	IS	POFF-	POFF signal (LOW: P-OFF, HIGH: P-ON)
32	4	BRK3	I	IS	GND	RS-232/INLINE USART BREAK signal
33	57	RCVRDY0	I	ISC	RCVRDY1	RS-232 USART RCVRDY signal
34	72	RCVRDY1	I	ISC	RCVRDY2	
35	74	RCVRDY2	I	ISC	GND	
36	6	RCVRDY3	I	IS	GND	RS-232/INLINE USART RCVRDY signal
37	59	TRNRDY0	I	ISC	TRNRDY1	RS-232 USART TRNRDY signal
38	71	TRNRDY1	I	ISC	TRNRDY2	
39	98	TRNRDY2	I	ISC	GND	
40	5	TRNRDY3	I	IS	GND	RS-232/INLINE USART TRNRDY signal
41	56	TRNEMP0	I	ISC	TRNEMP1	RS-232 USART TRNEMP signal
42	60	TRNEMP1	I	ISC	TRNEMP2	
43	100	TRNEMP2	I	ISC	GND	
44	3	TRNEMP3	I	IS	GND	RS-232/INLINE USART TRNEMP signal
45	58	RCVDT0	I	ISC	RCVDT1	RS-232 RCVDT signal (LOW: TIMER START)
46	73	RCVDT1	I	ISC	RCVDT2	
47	97	RCVDT2	I	ISC	GND	
48	41	RCVDT3	I	IS	GND	RS-232/INLINE RCVDT signal
49	20	RSRQ-	O	3S	RSRQ-	RS-232 IRQ- signal
50	83	TRV-	I	ISC	+5V	INLINE YES/NO
51	7	RXDATA0	O	O	NC	INLINE RXDATA OUT
52	42	TXE	O	O	NC	INLINE TRNS ENABLE
53	84	TRRQ-	O	3S	NC	INLINE IRQ- signal
54	28	TRQ1-	O	3S	$\overline{TRQ1}$	TIMER IRQ signal (RS-232)

No.	Pin No.	Pin name	I/O	Pin	ER-A5RS	Description
55	29	TRQ2-	O	3S	NC	TIMER IRQ signal (INLINE)
56	11	D0	I/O	IOU	D0	DATA BUS (MAIN)
57	12	D1	I/O	IOU	D1	
58	13	D2	I/O	IOU	D2	
59	14	D3	I/O	IOU	D3	
60	16	D4	I/O	IOU	D4	
61	17	D5	I/O	IOU	D5	
62	18	D6	I/O	IOU	D6	
63	19	D7	I/O	IOU	D7	
64	61	DB0	I/O	IOU	DB0	DATA BUS (USART)
65	62	DB1	I/O	IOU	DB1	
66	63	DB2	I/O	IOU	DB2	
67	64	DB3	I/O	IOU	DB3	
68	66	DB4	I/O	IOU	DB4	
69	67	DB5	I/O	IOU	DB5	
70	68	DB6	I/O	IOU	DB6	
71	69	DB7	I/O	IOU	DB7	
72	21	A0	I	I	A0	ADDRESS BUS (MAIN)
73	22	A1	I	I	A1	
74	23	A2	I	I	A2	
75	24	A3	I	I	A3	
76	25	A4	I	I	A4	
77	26	A5	I	I	A5	
78	10	OPTCS-	I	I	OPTCS-	OPTION CHIP SELECT (from MAIN)
79	31	RDO-	I	I	RDO-	READ signal (from MAIN)
80	30	WRO-	I	I	WRO-	WRITE signal (from MAIN)
81	9	RES-	I	IS	RES-	RESET signal (from MAIN)
82	34	R-	O	O	R-	READ signal (To USART)
83	37	W-	O	O	W-	WRITE signal (To USART)
84	51	RES	O	O	RES	RESET signal (To USART)
85	92	X1	O		X1	Oscillation circuit
86	91	X2	I		X2	
87	53	XOUT	O	O	XOUT	Clock for USART
88	8	TRCK	O	O	NC	T/R clock for 1CH USART
89	35	AB0	O	O	AB0	Address bus for USART
90	33	AB1	O	O	AB1	
91	85	USICH	I	ISC	GND	UNIT3 USART 1CH/2CH select
92	50	PX		O	PX	Power source clock
93	39	VCC			+5V	
94	89	VCC			+5V	
95	15	GND			GND	
96	40	GND			GND	
97	65	GND			GND	
98	90	GND			GND	
99	49	RTS0-	O	O	RTS1-	RS-232 control signal RTS- output
100	44	RTS1-	O	O	RTS2-	

ICU : CMOS level input (internal pullup resistor)
O : Output
IS : TTL level input (internal schmit circuit)
ISC : CMOS level input (internal schmit circuit)
3S : Three state output
IOU : I/O port (internal pullup resistor)

3-2. USART (MB89371A)

1) General

The MB89371A (Serial data transmitter/receiver, 2 units) is a versatile-use interface LSI for communication lines, which is equipped with two sets of equivalent units of the MB89251A (serial data transmitter/receiver), the baud rate generating section, and the interruption adjustment section.

It is positioned between the line Modem and the computer, and used for serial/parallel conversion of data, data send/receive operation check, and the synchronization mode selection according to the program assignment.

The transmitter section converts parallel data into serial data, and adds the parity bit, the start bit, and the stop bit to them, and transmits them. In the synchronization mode, it transmits synchronization characters during no transmission data period. In the advancement synchronization mode, it allows selection of transmission clocks and transmission baud rates.

The receiving section converts serial data into parallel data, and checks parities to judge that data are properly transmitted.

In the synchronization mode, it detects synchronization characters and makes synchronization of transmission/reception operations with the transmitter side. In the advancement synchronization mode, it allows selection of transmission clocks and reception baud rates.

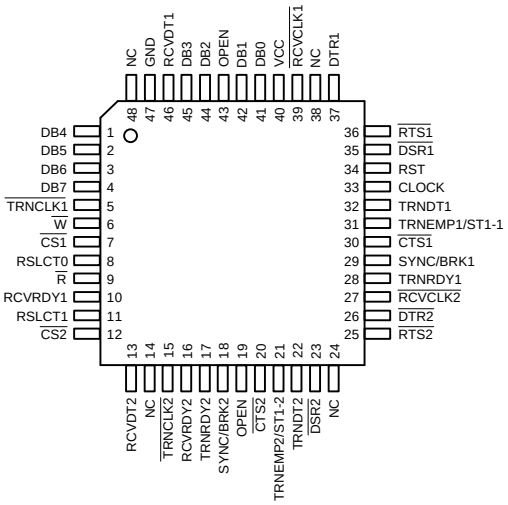
The baud rate generating section generates clock pulse signals which are used in transmission and reception and delivered through the baud rate selecting section to the SDTR section.

It provides the loop back diagnostic function which crosses interface lines of the Modem and loops transmission and reception signals, facilitating the operation check.

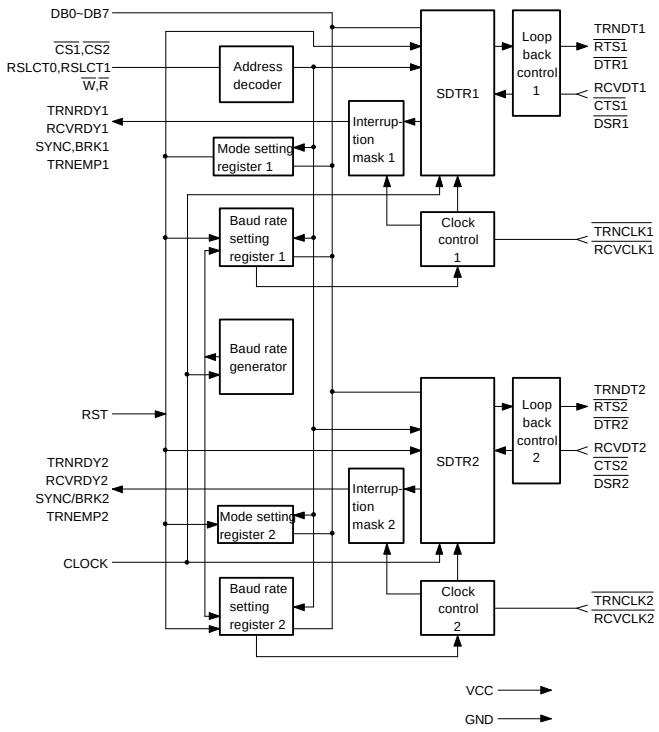
Features

- Two independent channels of SDTR.
- Built-in baud rate generator which allows setting for each channel
- External clock available
- Internal clock output available.
- Maskable interruption generating circuit
- Two channels are assigned to different address spaces.
- Baud rate DC ~ 240K baud (with external clocks)
- Full duplex communication
- Program assignment in synchronization mode
  - Data bit length: 5 - 8 bits
  - Character synchronization system: Internal synchronization, external synchronization
  - Number of synchronized characters: Single character, double characters
  - Parity occurrence and check: parity valid/invalid
even parity, odd parity
- Operations in the synchronization mode
  - Overrun error and parity error detection
  - Transmit/receive buffer state acknowledgment
  - Synchronization character detection
  - Automatic insertion of synchronization character
- Program assignment function in the advancement synchronization mode
  - Data bit length: 5 ~ 8 bits
  - Stop bit length: 1, 1½, 2 bits
  - Baud rate: Transmission clock, reception clock x 1, x 1/16, x 1/64
  - Parity occurrence and check: Parity valid, invalid
Even parity, odd parity
- Operations in the advancement synchronization mode
  - Detection of framing error, overrun error, parity error
  - Transmission/reception buffer state acknowledgment
  - Break characters detection
- Error start bit detection
- IBM Bi-sync system operation allowed.
- Duplex buffer system in the transmission and the reception sections.
- Loop back diagnostic functions
- I/O signal level TTL compatible
- Compatible with standard microprocessor in connecting pins and signal timing.
- Standard 42 pin plastic DIP, 48 pin plastic QFP
- +5V single power source

2) Pin configuration



3) Block diagram



4) Pin description

No.	Pin No.	Pin name	I/O	ER-A5RS	
1	1	DB4	I/O	DB4	Data bus
2	2	DB5	I/O	DB5	
3	3	DB6	I/O	DB6	
4	4	DB7	I/O	DB7	
5	41	DB0	I/O	DB0	
6	42	DB1	I/O	DB1	
7	44	DB2	I/O	DB2	
8	45	DB3	I/O	DB3	
9	46	RCVDT1	I	RCVDT1	RS-232 reception data signal
10	13	RCVDT2	I	RCVDT2	
11	47	GND	–	GND	
12	5	TRNCLK1-	I	GND	Data transmission clock
13	15	TRNCLK2-	I	GND	
14	6	W-	I	W-	Write signal
15	7	CS1-	I	CS1-	RS-232 chip select
16	12	CS2-	I	CS2-	
17	8	RSLCT0	I	AB0	Address bus
18	11	RSLCT1	I	AB1	
19	9	R-	I	R-	Read signal
20	10	RCVRDY1	O	RCVRDY1	RS-232 data reception enable signal
21	16	RCVRDY2	O	RCVRDY2	
22	28	TRNRDY1	O	TRNRDY1	RS-232 data transmission enable signal
23	17	TRNRDY2	O	TRNRDY2	
24	29	BRK1	O	BRK1	Break code detection signal
25	18	BRK2	O	BRK2	
26	30	CTS1-	I	(CTS1-)GND	RS-232 clear to send signal
27	20	CTS2-	I	(CTS2-)GND	
28	31	TRNEMP1	O	TRNEMP1	RS-232 transmission buffer empty signal
29	21	TRNEMP2	O	TRNEMP2	
30	14	NC	–	NC	
31	24	NC	–	NC	
32	38	NC	–	NC	
33	48	NC	–	NC	
34	19	OPEN		NC	
35	43	OPEN		NC	
36	32	TRNDT1	O	TRNDT1	RS-232 transmission data signal
37	22	TRNDT2	O	TRNDT2	
38	35	DSR1-	I	DSR1-	RS-232 data set ready signal
39	23	DSR2-	I	DSR2-	
40	36	RTS1-	O	NC	Request to send signal
41	25	RTS2-	O	NC	
42	37	DTR1-	O	DTR1-	RS-232 data terminal ready signal
43	26	DTR2-	O	DTR1-	
44	39	RCVCLK1-	I	GND	Data reception clock
45	27	RCVCLK2-	I	GND	
46	33	CLOCK	I	CLOCK	Clock signal
47	34	RST	I	RES	RESET signal
48	40	VCC	–	+5V	+5V

4. Power supply circuit

The ER-A550 supplies +5V to +24V, and ±12V is generated from +24V in the DC/DC convertor circuit.

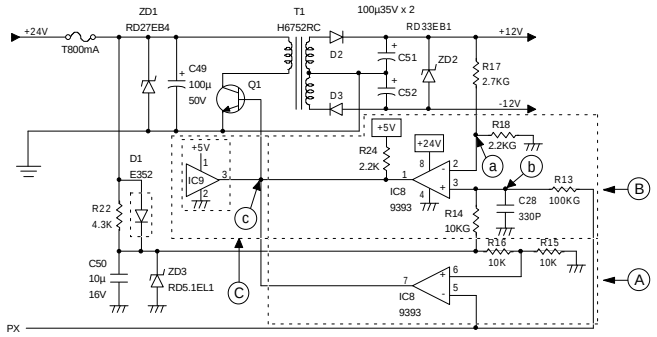


Fig. 4-1

(1) The PX signal from the OPC1 alternately turns on and off the comparator output of IC 8 (pin 7), which causes Q1 to turn on and off. (Circuit A)

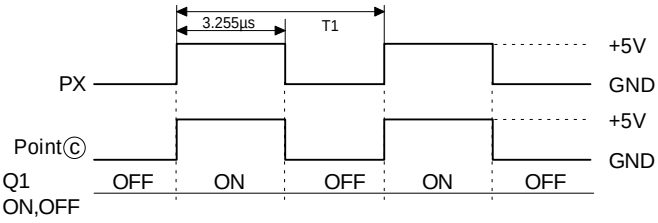


Fig. 4-2

T1: Software starting: 26.04us
Normal operation: 13.02us

∗ After POFF cancel (Power ON), software start is made for 13.3ms.

Duty (Q1: ON/OFF) : Software strating: 12.5%
Noemalperation : 25%

(2) The potential at point α is 4.8V when the output voltage is +12V(About +11V). A load fluctuation causes the +12V output to change. At point β of the comparators (+) side, a triangular waveform appears as shown in Fig. 4-2.

(3) The comparator (IC No. 8...Circuit B), the potential at point α is compared with that of point β . If the potential at point α is lower than point β , Q1 activating time is prolonged to raise the output voltage (by increasing the duty cycle). On the contrary, if the potential at point α is higher, the transistor activating time is hortened to decrease the output voltage (by decreasing the duty cycle). As Q1 duties cycles are varied by detecting the +12V output fluctuation in the comparator (Circuit B), the output voltage is regulated at a constant level.

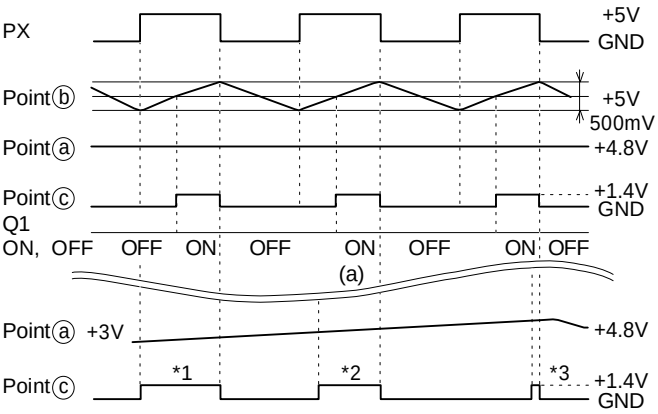


Fig. 4-3

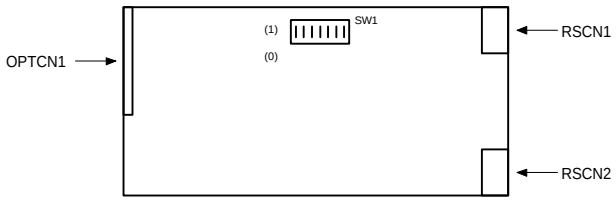
Potential at point a changes according to a fluctuation in the +12V output. Waveform at point a differs depending on the state of +12V output.

(4) The pin 3 output of the IC9 chip at circuit X is at a high level when the pin 1 input is at 5V. But, when it drops below 4.5V, the line goes to the GND level. This causes Q1 to turn off so that +12V and 12V are shut off. It is provided for prevention from malfunction in the logic circuit when the +5V supply from malfunction in the logic circuit when the +5V supply from the ER-A550 main frame drops.

∗ IC9: Not used

5. ER-A5RS channel setting

The ER-A5RS ports can be set to channel 1 - 7 and invalid (inhibit) with SW1 on the PWB.

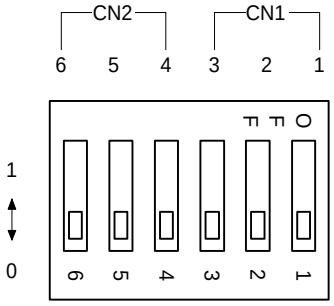


SW1 setting contents
SW1 1~3 are used for channel setting of RS-232 connector 1 (RSCN1).
SW1 4~6 are used for channel setting of RS-232 connector 2 (RSCN2).

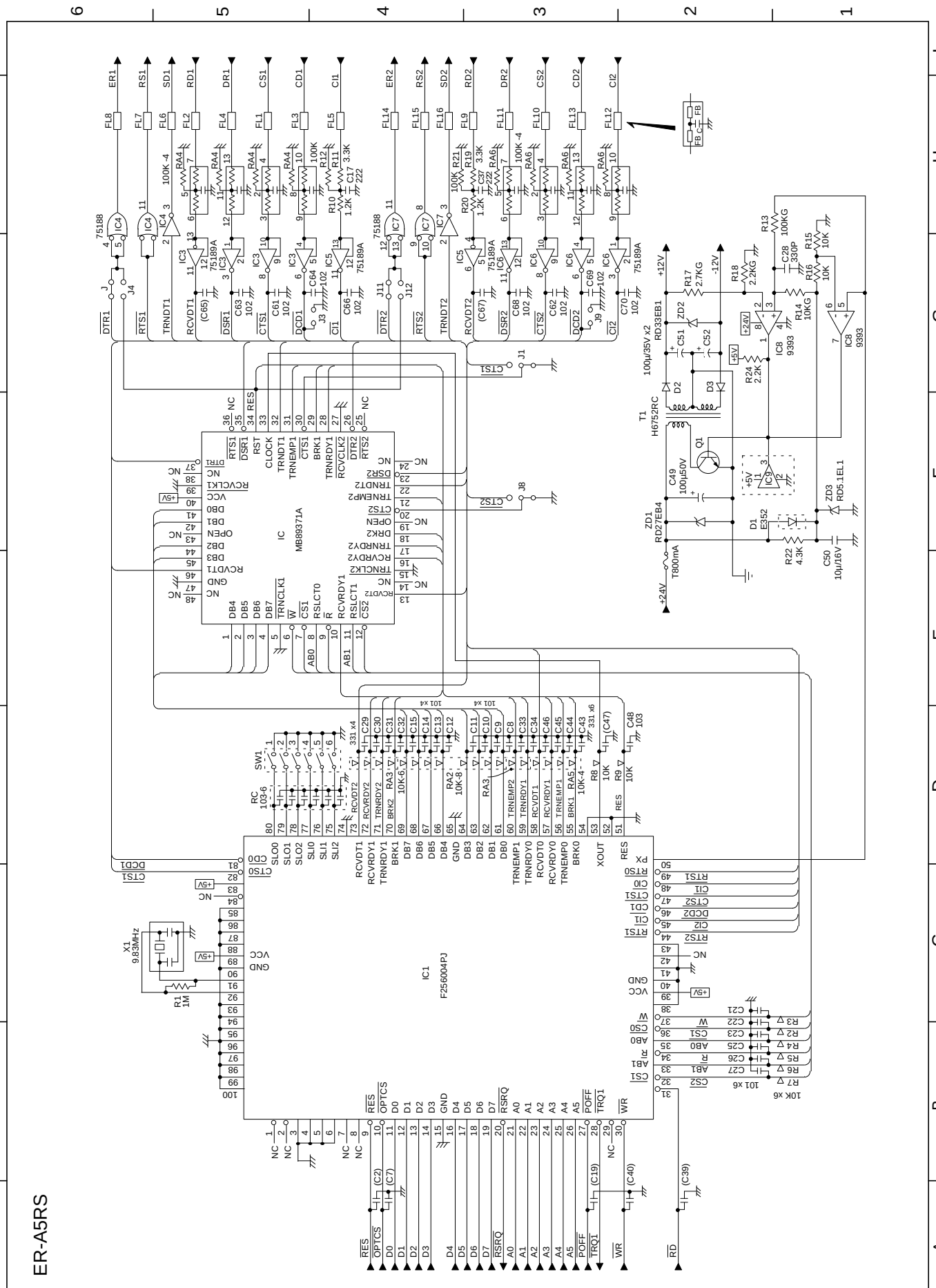
SW1			RSCN1 setting
3	2	1	
0	0	0	RS-232 invalid
0	0	1	Channel 1
0	1	0	Channel 2
0	1	1	Channel 3
1	0	0	Channel 4
1	0	1	Channel 5
1	1	0	Channel 6
1	1	1	Channel 7

SW1			RSCN2 setting
6	5	4	
0	0	0	RS-232 invalid
0	0	1	Channel 1
0	1	0	Channel 2
0	1	1	Channel 3
1	0	0	Channel 4
1	0	1	Channel 5
1	1	0	Channel 6
1	1	1	Channel 7

Note
1) If RSCN1 port and RSCN2 port of the ER-A5RS are set to the same channel, RSCN2 port becomes invalid and only RSCN1 is valid.
2) If RSCN of the ER-A5IN and the ER-A5RS connector are set to the same channel, the buses compete and the operation cannot be assured. In addition, it may break the hardware. Never set the two to the same channel. Be sure to set them to different channels or to set invalid.



6. Circuit diagram



ER-A5RS

OPTCN1

SIGNAL	No.	No.	SIGNAL
GND	1	35	GND
GND	2	36	GND
$\overline{\text{RDO}}$	3	37	(ϕ)
$\overline{\text{WRO}}$	4	38	NU1
+5V	5	39	$\overline{\text{BREQ}}$
+5V	6	40	$\overline{\text{BACK}}$
A23	7	41	$\overline{\text{TRQ2}}$
A22	8	42	$\overline{\text{TRQ1}}$
A21	9	43	$\overline{\text{EXINT1}}$
A20	10	44	$\overline{\text{EXINT0}}$
A19	11	45	$\overline{\text{TRRQ}}$
A18	12	46	$\overline{\text{RSRQ}}$
A17	13	47	$\overline{\text{RFSH}}$
A16	14	48	$\overline{\text{IPLON}}$
A15	15	49	D7
A14	16	50	D6
A13	17	51	D5
A12	18	52	D4
A11	19	53	D3
A10	20	54	D2
A9	21	55	D1
A8	22	56	D0
A7	23	57	$\overline{\text{POFF}}$
A6	24	58	VRAM
A5	25	59	(+12V)
A4	26	60	A3
+24V	27	61	+24V
+24V	28	62	+24V
A1	29	63	A2
A0	30	64	$\overline{\text{RES}}$
$\overline{\text{RESET}}$	31	65	$\overline{\text{AS}}$
$\overline{\text{OPTCS}}$	32	66	NU2
GNDP	33	67	GND
GNDP	34	68	GND

OPTCN2

SIGNAL	No.	No.	SIGNAL
GND	1	36	GND
GND	2	37	GND
GND	3	38	GND
$\overline{\text{RDO}}$	4	39	(ϕ)
$\overline{\text{WRO}}$	5	40	NU1
$\overline{\text{BREQ}}$	6	41	+5V
$\overline{\text{BACK}}$	7	42	+5V
A23	8	43	$\overline{\text{TRQ2}}$
A22	9	44	$\overline{\text{TRQ1}}$
A21	10	45	$\overline{\text{EXINT1}}$
A20	11	46	$\overline{\text{EXINT0}}$
A19	12	47	$\overline{\text{TRRQ}}$
A18	13	48	$\overline{\text{RSRQ}}$
A17	14	49	$\overline{\text{RFSH}}$
A16	15	50	$\overline{\text{IPLON}}$
A15	16	51	D7
A14	17	52	D6
A13	18	53	D5
A12	19	54	D4
A11	20	55	D3
A10	21	56	D2
A9	22	57	D1
A8	23	58	D0
A7	24	59	$\overline{\text{POFF}}$
A6	25	60	VRAM
A5	26	61	A3
A4	27	62	(+12V)
+24V	28	63	+24V
+24V	29	64	+24V
A1	30	65	A2
A0	31	66	$\overline{\text{RES}}$
$\overline{\text{RESET}}$	32	67	$\overline{\text{AS}}$
$\overline{\text{OPTCS}}$	33	68	NU2
GNDP	34	69	GND
GNDP	35	70	GND

RSCN1

No.	SIGNAL
1	CD1
2	RD1
3	SD1
4	ER1
5	GND
6	DR1
7	RS1
8	CS1
9	CI1

RSCN2

No.	SIGNAL
1	CD2
2	RD2
3	SD2
4	ER2
5	GND
6	DR2
7	RS2
8	CS2
9	CI2

7. PWB layout