CMP 200 FUNCTIONAL DRAWINGS	
DESCRIPTION	**DRAWING NUMBER**
DC Bus and Power Distribution	MD-0831
System ON	MD-0832
Room Interface	MD-0833
X-Ray Exposure - Radiographic	MD-0834
kV Control and Feedback	MD-0835
Filament Drive and mA Control	MD-0836
Low Speed Starter	MD-0837
Automatic Exposure Control (AEC)	MD-0838
Serial Communications	MD-0839
DAP	MD-0840
Aux 24VAC / 24VDC Power Dist (optional)	MD-0841

THE PART NUMBER OF THE ORIGINAL AEC BOARD IN THE GENERATOR FOR WHICH THIS MANUAL WAS PREPARED IS LISTED BELOW:

AEC BOARD PART NUMBER (AS ORIGINALLY SHIPPED)
See Drawing List for the AEC Board Part Number for this particular unit.

REFER TO PAGE 4 FOR LOGIC LEVELS, NOTES, ETC, REFERENCED BY THIS SYMBOL: ⬡

AC MAINS INPUT

F1, F2, F4, F5

E1 + / E2 - → INVERTER BOARD

J5-5, J5-7, J10-1, J10-3, J5-3, J5-1

D7

MAIN CONTACTOR DRIVE FROM MD-0832

THIS TRANSFORMER AND ASSOCIATED WIRING IS ONLY FITTED ON UNITS CONFIGURED FOR 120 VAC BOOST, OR WITH THE 24VAC / 24VDC POWER DIST OPTION

N.C. 480V, N.C. 400V, 240V, 210V, 120V, 0V → SEE MD-0841

E16 ** E15, E14, F7, F6 → ***120/240 VAC*** TO LOW SPEED STARTER MD-0837

D5, R16, C11, R11, R17, R14, R13

F5, K2, F4

+12V → D8 → ***SOFT-START CONTACTOR DRIVE*** FROM MD-0832

2, 5, U5, 1, 4

J6-12 / J11-12, J6-6 / J11-6 → ***SOFT-START SENSE*** TO MD-0832

F8, F9

E10, E6 * E8, K6 → ***BUCKY DRIVE*** TO MD-0833

J9-1, J9-3, J9-7, E3, E4 * E5, F10, E11

+24 V, +12V, D10

D1, C2, C4

J1-4 / J12-6, J1-5 / J12-5 (+35 V)

J1-8 / J12-2, J1-9 / J12-1 (-35 V)

24 VAC TO MD-0833

24 VDC TO MD-0833

0V, 29V, 26V, 18V, 0V, 18V, 120V, 208V, 240V

J3-1, J3-4, J3-3, J3-5, J3-2

F1, F2, F3

D3, R27, DS1, C6, D4

J1-1 / J12-9, J1-2 / J12-8 (+24 V)

J1-6 / J12-4, J1-7 / J12-3 (TP9)

H.V. AUXILIARY BOARD

THIS SHEET DEPICTS 1 PH. UNITS. REFER TO PAGE 2 FOR 3 PH. 400/480 V UNITS, AND PAGE 3 FOR 3 PH. 208 V UNITS

* ***E3, E4, E5, E6, E8, E10, E11 CONFIGURE THE BUCKY OUTPUTS FOR +24 VDC, 120 VAC, OR 240 VAC. REFER TO CHAPTER 8 FOR DETAILS.***

** ***E14, E15, E16 CONFIGURE THE LOW SPEED STARTER BOOST VOLTAGE FOR 120 OR 240 VAC. REFER TO CHAPTER 2 FOR DETAILS.***

ON / OFF COMMAND 2 FROM MD-0832 → ① → TP12 → D4

+24V → +5V SWITCHING REGULATOR CIRCUIT (U10 AND ASSOCIATED COMPONENTS) → TP13 (+5V)

+24V → +12V SWITCHING REGULATOR CIRCUIT (U12 AND ASSOCIATED COMPONENTS) → TP14 (+12V) → D6

+24 V → F1, K1, D39 → ***ON / OFF COMMAND 1*** FROM MD-0832

+12V → -12V SWITCHING REGULATOR CIRCUIT (U15 AND ASSOCIATED COMPONENTS) → TP11 (-12 V)

+24V → +15V SWITCHING REGULATOR CIRCUIT (U9 AND ASSOCIATED COMPONENTS) → TP10 (+15V) → D2

GENERATOR CONTROL BOARD

+35 V, J15-1 / J1-1, F2

J15-3 / J1-3 → -12 V

TP2, J15-5 / J1-5, J15-6 / J1-6

J15-2 / J1-2, F1 → -35 V

+12 V, J15-4 / J1-4

FILAMENT SUPPLY BOARD

+12 V, J7-13, +24 V, J7-19, J7-17, J7-11 (-12 V)

REFER TO MD-0838 (***AEC***) FOR PINOUTS OF THE +/-12 VDC AND +24 VDC SUPPLIES

AEC BOARD

FLUORESCENT LAMP

LCD DISPLAY ASSEMBLY

+5V, TP9 ③, J5-1, J5-5

300 VAC BACKLIGHT POWER SUPPLY (Q1, Q2, T1, ETC), C36

② TP2, + 5 / -20VDC POWER SUPPLY & REGULATOR (U12, L1, D3-D7, ETC), TP7 (+5V), TP8 (-20V)

J3-8, J8-8, F1

TP9, J3-3, J8-3, TP3

CONSOLE BOARD

DRAWN G. SANWALD	DATE 11 FEB 2003	**DC BUS & POWER DISTRIBUTION**
CHECKED Steve Blake	18 FEB 2003	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	**MD-0831 REV F**
		SHEET 1 OF 4

AC MAINS INPUT

F3 F2 F1 F5 F4

ALTERNATE TRANSFORMER. (USED ON UNITS WITH THE AUX 24VAC / 24VDC POWER DISTRIBUTION OPTION)

480V 400V 240V 210V 120V 0V — SEE MD-0841

480V 400V 240V 120V 0V

DS1

E1 + * INVERTER BOARD E2 -

EMC CAPACITOR BOARD

* 50 KW UNITS USE TWO INVERTER BOARDS

J5-5 J5-7 J10-1 J10-3 J5-3 J5-1

D7

MAIN CONTACTOR DRIVE FROM MD-0832

D5

+12 V TP11 J6-1 J6-2 J11-1 J11-2 +12 V

F6 F7 — 120/240 VAC TO LOW SPEED STARTER MD-0837

E16 ** E15 E14

K2 F5 F4 R11 R27 R17 R14

F8 F9

+12V

SOFT-START CONTACTOR DRIVE FROM MD-0832

D8

2 5 U5 1 4 R13

J6-12 J11-12 J6-6 J11-6

SOFT-START SENSE TO MD-0832

BUCKY DRIVE TO MD-0833

E10 E6 * E8 K6 E3 E4 * E5 F10 E11

J9-5 J9-1 J9-3 J9-7

+24 V +12V D10

D1 C2 R28 C4 R29

+35 V TP2 J1-4 J1-5 J12-6 J12-5

TP3 J1-8 J1-9 J12-2 J12-1 -35 V

24 VAC TO MD-0833

24 VDC TO MD-0833

0V N.C. 120V N.C. 240V 400V 480V — 29V 26V 18V 0V 18V

J3-1 J3-4 J3-3 J3-5 J3-2 F1 F2 F3

D3 D4 R30 DS1 C6

+24 V TP1 J1-1 J1-2 J12-9 J12-8 +24 V -35 V

TP12 J1-6 J1-7 J12-4 J12-3 TP9

H.V. AUXILIARY BOARD

ON / OFF COMMAND 2 FROM MD-0832

1 TP12 D4

+12V -12V SWITCHING REGULATOR CIRCUIT (U15 AND ASSOCIATED COMPONENTS) TP11 -12 V

+24V +5V SWITCHING REGULATOR CIRCUIT (U10 AND ASSOCIATED COMPONENTS) TP13 +5V

+24V +12V SWITCHING REGULATOR CIRCUIT (U12 AND ASSOCIATED COMPONENTS) D6 TP14 +12V

+24V +15V SWITCHING REGULATOR CIRCUIT (U9 AND ASSOCIATED COMPONENTS) D2 TP10 +15V

+35 V J15-1 J1-1 F2 J15-3 J1-3 -12 V

TP2 J15-5 J1-5 J15-6 J1-6

J15-2 J1-2 F1 -35 V +12 V -35 V

J15-4 J1-4

FILAMENT SUPPLY BOARD

+12 V J7-13 +24 V J7-19 J7-17 J7-11 -12 V

REFER TO MD-0838 (*AEC*) FOR PINOUTS OF THE +/-12 VDC AND +24 VDC SUPPLIES

AEC BOARD

FLUORESCENT LAMP

LCD DISPLAY ASSEMBLY

+5V TP9 3 300 VAC BACKLIGHT POWER SUPPLY (Q1, Q2, T1, ETC) J5-1 J5-5 C36

2 TP2 + 5 / -20VDC POWER SUPPLY & REGULATOR (U12, L1, D3-D7, ETC) TP7 +5V TP8 -20V

J3-8 J8-8 F1

TP9 TP3 J3-3 J8-3

CONSOLE BOARD

GENERATOR CONTROL BOARD

THIS SHEET DEPICTS 3 PH. 400/480 V UNITS. REFER TO PAGE 1 FOR 1 PH. UNITS, AND PAGE 3 FOR 3 PH. 208 V UNITS

* E3, E4, E5, E6, E8, E10, E11 CONFIGURE THE BUCKY OUTPUTS FOR +24 VDC, 120 VAC, OR 240 VAC. REFER TO CHAPTER 8 FOR DETAILS.

** E14, E15, E16 CONFIGURE THE LOW SPEED STARTER BOOST VOLTAGE FOR 120 OR 240 VAC. REFER TO CHAPTER 2 FOR DETAILS.

DRAWN G. SANWALD	DATE 11 FEB 2003	DC BUS & POWER DISTRIBUTION
CHECKED Steve Blake	18 FEB 2003	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	MD-0831 REV F
		SHEET 2 OF 4

AC MAINS INPUT

F3 F2 F1 F5 F4

DS1

E1 + INVERTER BOARD E2 -

EMC CAPACITOR BOARD

THIS TRANSFORMER AND ASSOCIATED WIRING IS ONLY FITTED ON UNITS CONFIGURED FOR 120 VAC BOOST, OR WITH THE 24VAC / 24VDC POWER DIST OPTION

N.C. 480V
N.C. 400V
240V
210V
120V
0V

SEE MD-0841

J5-5 J5-7 J10-1 J10-3 J5-3 J5-1

D7

MAIN CONTACTOR DRIVE FROM MD-0832

D5

+12 V +12 V

J6-1 J11-1
J6-2 J11-2

E16 ** E15 F7
E14
F6

120/240 VAC TO LOW SPEED STARTER MD-0837

R16
C11
R11
R17
R14

F5 K2
F4

+12V

SOFT-START CONTACTOR DRIVE FROM MD-0832

D8

2 5 U5 1 4

R13

J6-12 J11-12
J6-6 J11-6

SOFT-START SENSE TO MD-0832

BUCKY DRIVE TO MD-0833

F8 F9 E10

J9-1 E6 * E8 K6
J9-3 E3
J9-7 E4 * E5 F10
E11

+24 V +12V

D10

+35 V

J1-4 J12-6
J1-5 J12-5

C2
C4

D1

24 VAC TO MD-0833

J1-8 J12-2
J1-9 J12-1

-35 V -35 V

24 VDC TO MD-0833

+24 V

J1-1 J12-9
J1-2 J12-8

R27
C6
DS1

D3 D4

J1-6 J12-4
J1-7 J12-3

TP9

0V
29V
26V
18V
120V
0V
18V
208V
240V

J3-1 F1
J3-4 F2
J3-3
J3-5 F3
J3-2

H.V. AUXILIARY BOARD

THIS SHEET DEPICTS 3 PH. 208 V UNITS. REFER TO PAGE 1 FOR 1 PH. UNITS, AND PAGE 2 FOR 3 PH. 400/480 V UNITS

ON / OFF COMMAND 2 FROM MD-0832

1 TP12 D4

+24V +5V SWITCHING REGULATOR CIRCUIT (U10 AND ASSOCIATED COMPONENTS) TP13 +5V

+12V +12V SWITCHING REGULATOR CIRCUIT (U12 AND ASSOCIATED COMPONENTS) TP14 +12V

D6

+24V +15V SWITCHING REGULATOR CIRCUIT (U9 AND ASSOCIATED COMPONENTS) TP10 +15V

D2

+12V -12V SWITCHING REGULATOR CIRCUIT (U15 AND ASSOCIATED COMPONENTS) TP11 -12 V

GENERATOR CONTROL BOARD

+24 V F1 K1

D39

ON / OFF COMMAND 1 FROM MD-0832

J15-1 +35 V
J15-3
J15-5
J15-6
J15-2 -35 V
J15-4

J1-1 F2 +35 V
J1-3 -12 V
J1-5 TP2
J1-6
J1-2 F1 -35 V
J1-4 +12 V

FILAMENT SUPPLY BOARD

J7-13 +12 V
J7-19 +24 V
J7-17
J7-11 -12 V

REFER TO MD-0838 (**AEC**) FOR PINOUTS OF THE +/-12 VDC AND +24 VDC SUPPLIES

AEC BOARD

FLUORESCENT LAMP

LCD DISPLAY ASSEMBLY

J5-1 J5-5

+5V TP9 3 300 VAC BACKLIGHT POWER SUPPLY (Q1, Q2, T1, ETC) C36

2 TP2 + 5 / -20VDC POWER SUPPLY & REGULATOR (U12, L1, D3-D7, ETC) TP7 +5V TP8 -20V

J3-8 J8-8 F1

TP9 TP3
J3-3 J8-3

CONSOLE BOARD

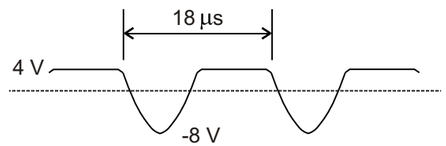
* E3, E4, E5, E6, E8, E10, E11 CONFIGURE THE BUCKY OUTPUTS FOR +24 VDC, 120 VAC, OR 240 VAC. REFER TO CHAPTER 8 FOR DETAILS.

** E14, E15, E16 CONFIGURE THE LOW SPEED STARTER BOOST VOLTAGE FOR 120 OR 240 VAC. REFER TO CHAPTER 2 FOR DETAILS.

DRAWN G. SANWALD	DATE 11 FEB 2003	DC BUS & POWER DISTRIBUTION
CHECKED Steve Blake	18 FEB 2003	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	MD-0831 REV F
		SHEET 3 OF 4

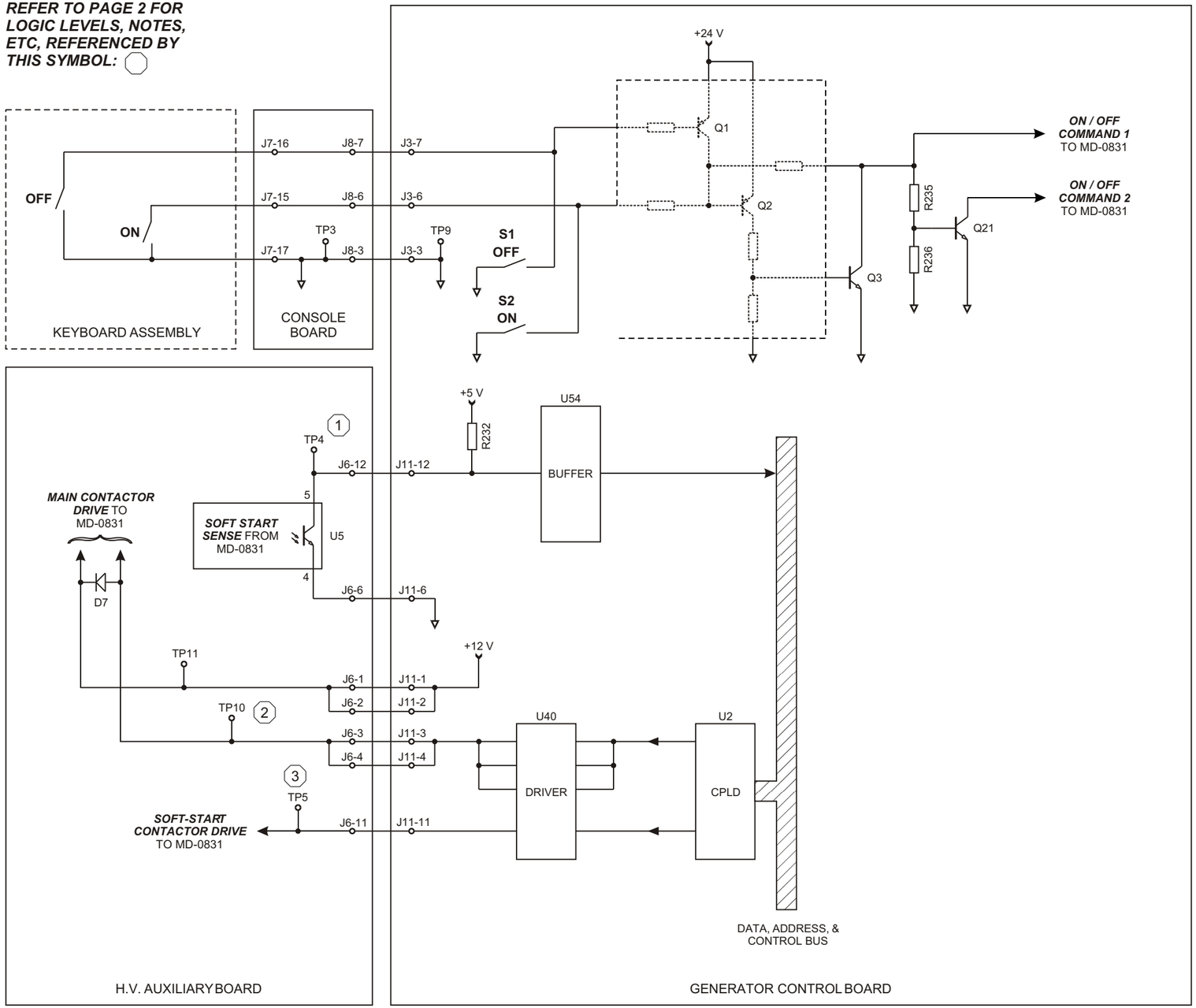
NOTE REFERENCE	REMARKS
1	“LOW” (APPROXIMATELY 0 VDC) DISABLES THE +5 V, +/-12 V, AND +15 V REGULATORS (GENERATOR SWITCHED OFF). “HIGH” (APPROXIMATELY 24 VDC) ENABLES THESE REGULATORS (GENERATOR SWITCHED ON VIA THE CONSOLE ON/OFF SWITCHES, OR VIA THE ON/OFF SWITCHES ON THE GENERATOR CONTROL BOARD) .
2	+24 VDC IS PRESENT AT THIS POINT WHEN THE GENERATOR IS SWITCHED ON, ENERGIZING K1 ON THE GENERATOR CONTROL BOARD.
3	THE VOLTAGE WAVEFORM AT THIS TEST POINT IS DEPICTED IN FIGURE 1 BELOW.

FIGURE 1



DRAWN G. SANWALD	DATE 11 FEB 2003	DC BUS & POWER DISTRIBUTION
CHECKED Steve Blake	18 FEB 2003	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	MD-0831 REV F
		SHEET 4 OF 4

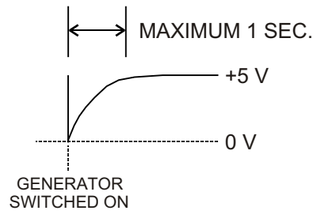
REFER TO PAGE 2 FOR LOGIC LEVELS, NOTES, ETC, REFERENCED BY THIS SYMBOL: ⬡



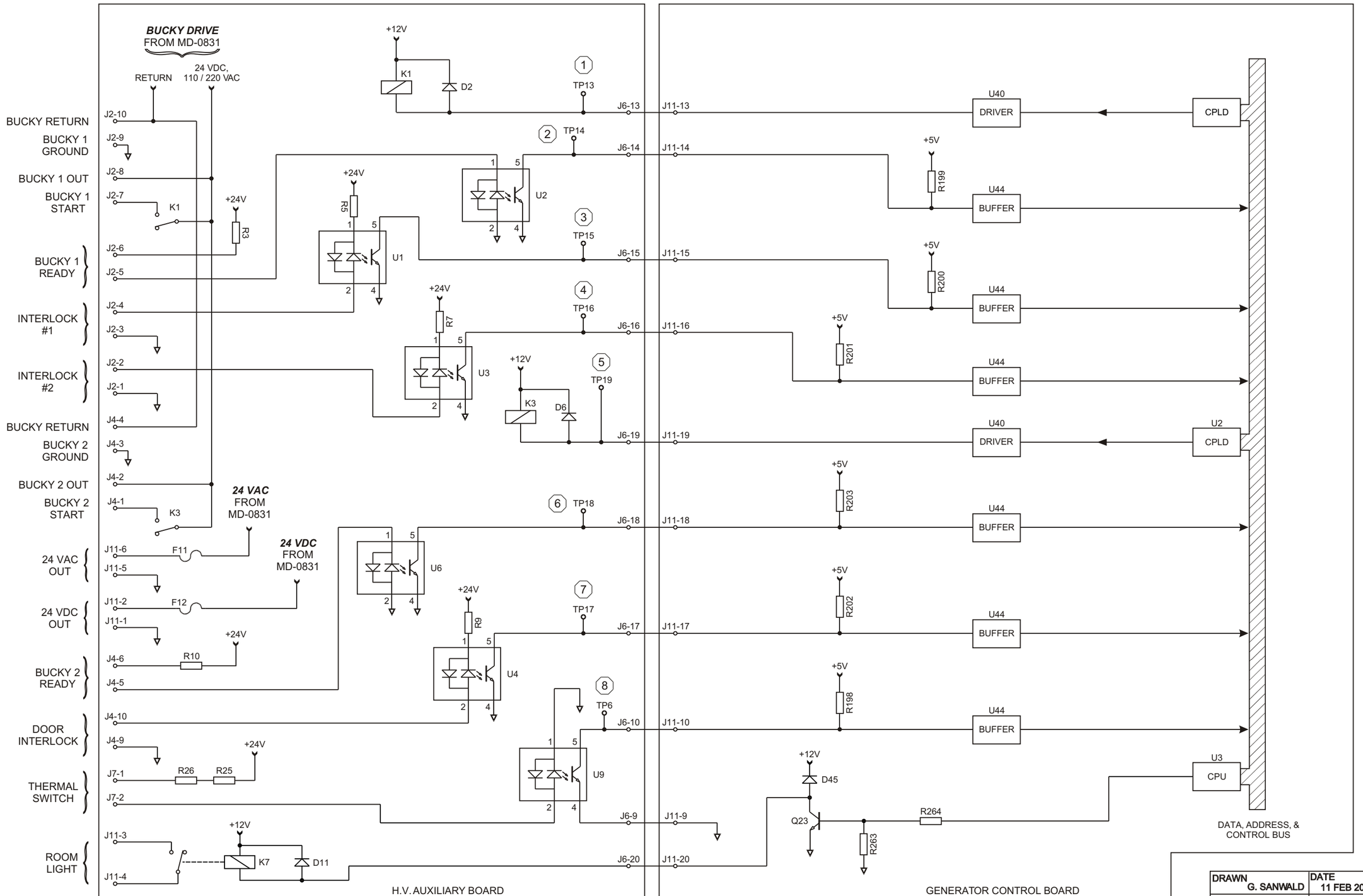
DRAWN G. SANWALD	DATE 11 FEB 2003	**SYSTEM "ON"**
CHECKED Steve Blake	18 FEB 2003	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	**MD-0832 REV A**
		SHEET 1 OF 2

NOTE REFERENCE	REMARKS
1	THE VOLTAGE WAVEFORM AT THIS TEST POINT IS DEPICTED IN FIGURE 1 BELOW.
2	“LOW” (APPROXIMATELY 0 VDC) ENERGIZES THE MAIN POWER CONTACTOR IN THE GENERATOR, (”HIGH”, + 12 VDC = NOT ENERGIZED). THIS CONTACTOR IS ENERGIZED AFTER THE MAIN BUS CAPACITORS ARE CHARGED, APPROXIMATELY 10 SECONDS AFTER POWER-ON.
3	“LOW” (APPROXIMATELY 0 VDC) ENERGIZES THE SOFT START CONTACTOR K2 ON THE H.V. AUXILIARY BOARD, (”HIGH”, + 12 VDC = NOT ENERGIZED). THIS CONTACTOR IS ENERGIZED FOR A MAXIMUM OF APPROXIMATELY 10 SECONDS AFTER POWER-ON IN ORDER TO CHARGE THE DC BUS CAPACITORS.

FIGURE 1



DRAWN G. SANWALD	DATE 11 FEB 2003	SYSTEM “ON”
CHECKED Steve Blake	18 FEB 2003	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	MD-0832 REV A
		SHEET 2 OF 2



REFER TO CHAPTER 3 OF THE SERVICE MANUAL FOR ADDITIONAL DETAILS REGARDING INTERFACING OF BUCKYS, INTERLOCKS, ETC.

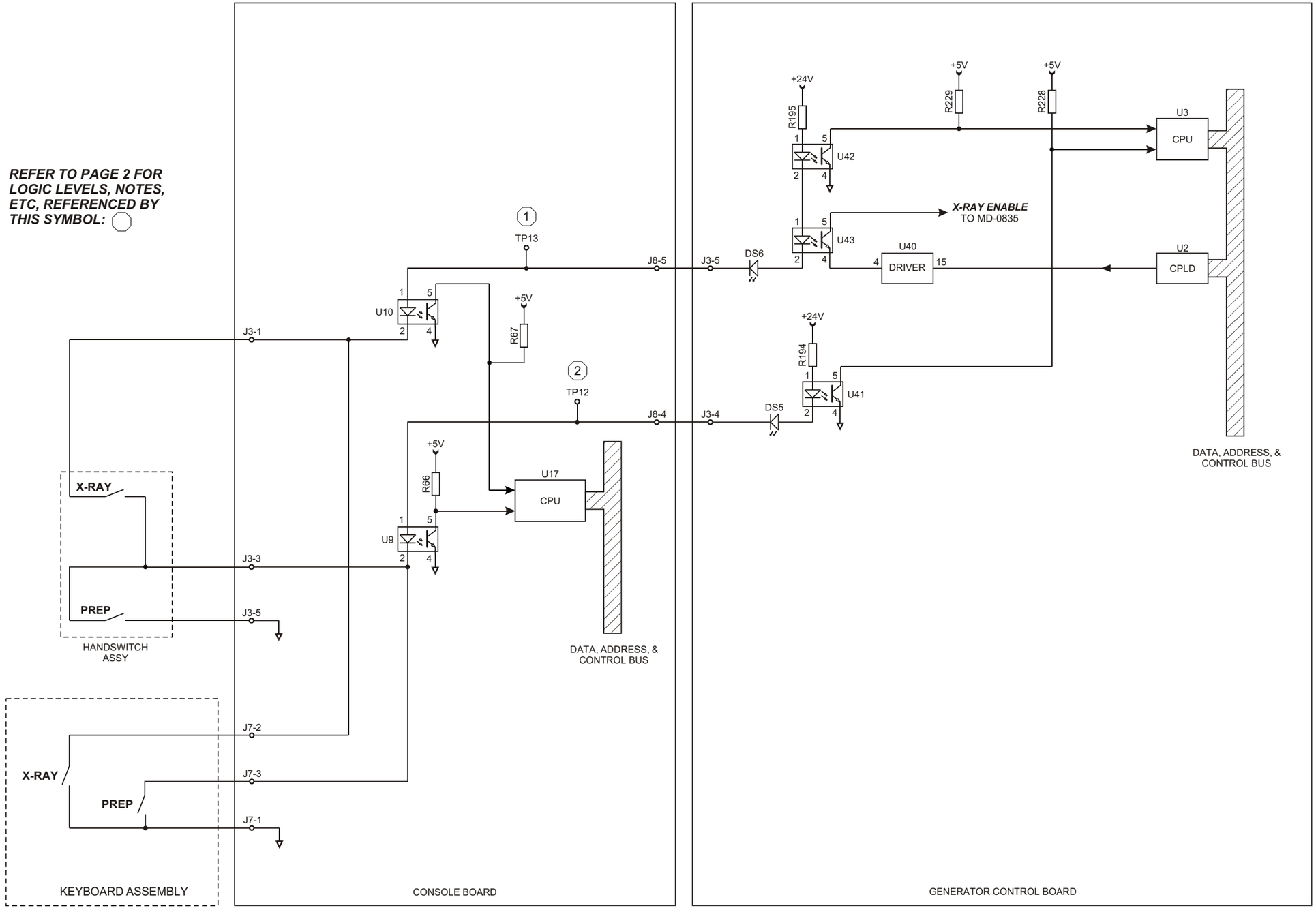
REFER TO PAGE 2 FOR LOGIC LEVELS, NOTES, ETC, REFERENCED BY THIS SYMBOL: ⯃

DRAWN G. SANWALD	DATE 11 FEB 2003	**ROOM INTERFACE**
CHECKED Steve Blake	18 FEB/03	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	**MD-0833 REV C**
		SHEET 1 OF 2

NOTE REFERENCE	REMARKS
1	“LOW” (APPROXIMATELY 0 VDC) = BUCKY 1 START. “HIGH” (APPROXIMATELY +12 VDC) = BUCKY 1 NOT REQUESTED TO START.
2	“LOW” (APPROXIMATELY 0 VDC) = BUCKY 1 READY. “HIGH” (APPROXIMATELY +5 VDC) = BUCKY 1 NOT READY.
3	“LOW” (APPROXIMATELY 0 VDC) = 40” S.I.D. INTERLOCK CLOSED. “HIGH” (APPROXIMATELY +5 VDC) = 40” S.I.D. INTERLOCK OPEN.
4	“LOW” (APPROXIMATELY 0 VDC) = 72” S.I.D. INTERLOCK CLOSED. “HIGH” (APPROXIMATELY +5 VDC) = 72” S.I.D. INTERLOCK OPEN.
5	“LOW” (APPROXIMATELY 0 VDC) = BUCKY 2 START. “HIGH” (APPROXIMATELY +12 VDC) = BUCKY 2 NOT REQUESTED TO START.
6	“LOW” (APPROXIMATELY 0 VDC) = BUCKY 2 READY. “HIGH” (APPROXIMATELY +5 VDC) = BUCKY 2 NOT READY.
7	“LOW” (APPROXIMATELY 0 VDC) = DOOR INTERLOCK CLOSED. “HIGH” (APPROXIMATELY +5 VDC) = DOOR INTERLOCK OPEN.
8	“LOW” (APPROXIMATELY 0 VDC) = THERMAL SWITCH CLOSED. “HIGH” (APPROXIMATELY +5 VDC) = THERMAL SWITCH OPEN.

DRAWN G. SANWALD	DATE 11 FEB 2003	**ROOM INTERFACE**
CHECKED Steve Blake	18 FEB/03	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	**MD-0833 REV C**
		SHEET 2 OF 2

REFER TO PAGE 2 FOR LOGIC LEVELS, NOTES, ETC, REFERENCED BY THIS SYMBOL: ⬡



DRAWN G. SANWALD	DATE 11 FEB 2003	**X-RAY EXPOSURE (RADIOGRAPHIC)**
CHECKED Steve Blake	13 FEB/03	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	**MD-0834 REV A**
		SHEET 1 OF 2

NOTE REFERENCE	REMARKS
1	“LOW” (APPROXIMATELY 0 VDC) = X-RAY REQUESTED. “HIGH” (APPROXIMATELY +24 VDC) = X-RAY NOT REQUESTED.
2	“LOW” (APPROXIMATELY 0 VDC) = PREP REQUESTED. “HIGH” (APPROXIMATELY +24 VDC) = PREP NOT REQUESTED.

DRAWN G. SANWALD	DATE 11 FEB 2003	**X-RAY EXPOSURE (RADIOGRAPHIC)**
CHECKED Steve Blake	13 FEB/03	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	**MD-0834 REV A**
		SHEET 2 OF 2

REFER TO PAGE 2 FOR LOGIC LEVELS, NOTES, ETC, REFERENCED BY THIS SYMBOL: ⬡

1

TP26

U2
CPLD

2

TP27

+5V +5V +12V

U39

U57

INVERTER "SHOOT THRU" DETECTOR CIRCUITS

INVERTER "SHOOT THRU" SENSE, FROM PAGE 2

J10-1 J10-3

T3

R193

INVERTER "SHOOT THRU" SENSE, FROM PAGE 2

J16-1 J16-3

T4

R246

1V = 20 kV OF H.V. FEEDBACK

TP8

R225

R122 R127 R126 R120

U28A U28B

R124 R128 R125 R131

R130 R133 R134

R135

U30B

J9-6 J9-5 J9-7 J9-8

KV FEEDBACK SIGNAL FROM PAGE 2

3

TP23

U2
CPLD

+5V +5V

R123 R121

U29

R129

R132

GATE DRIVE CIRCUIT FOR MOSFET INVERTER (INCLUDES Q9, 10, 12, 13)

J5-1 J5-2 J5-3 J5-4 J13-1 J13-2 J13-3 J13-4

INVERTER DRIVE SIGNAL CONTINUED ON PAGE 2

U45
A/D CONV

R217

R216

+12V +12V

R161

R164 Q16

U3
CPU

R165 Q17

R169

R166

R171

1V = 15 kV OF H.V. DEMAND **TP5**

U46
D/A CONV

R220

R170 R177 R178 R179

U50A U35A

R181

D34

ERROR AMPLIFIERS INCLUDES U36A, U36B

U36A U36B

D35 R183

D33

R176

U37A

R187

VCO

INCLUDES U19, U20, U21, U34, U55, Q15

8

TP16

+5V

R64

U17A U18A

U17B U18B

TP2 TP3 10

R65 R76

4

TP23

U3
CPU

R78

Q14

R81

5

TP15

+12V

U22

R96

R97 R99

D16-D19

T2 T1

CURRENT SENSE

7

TP19

+5V

R69 R71

+5V

R68 R70

9

TP17

J9-9

J3-9

H.V. OIL TANK

6

TP18

U2
CPLD

R94

R98 R95

-12V

R72

Q11

R73

J6-1 J6-4

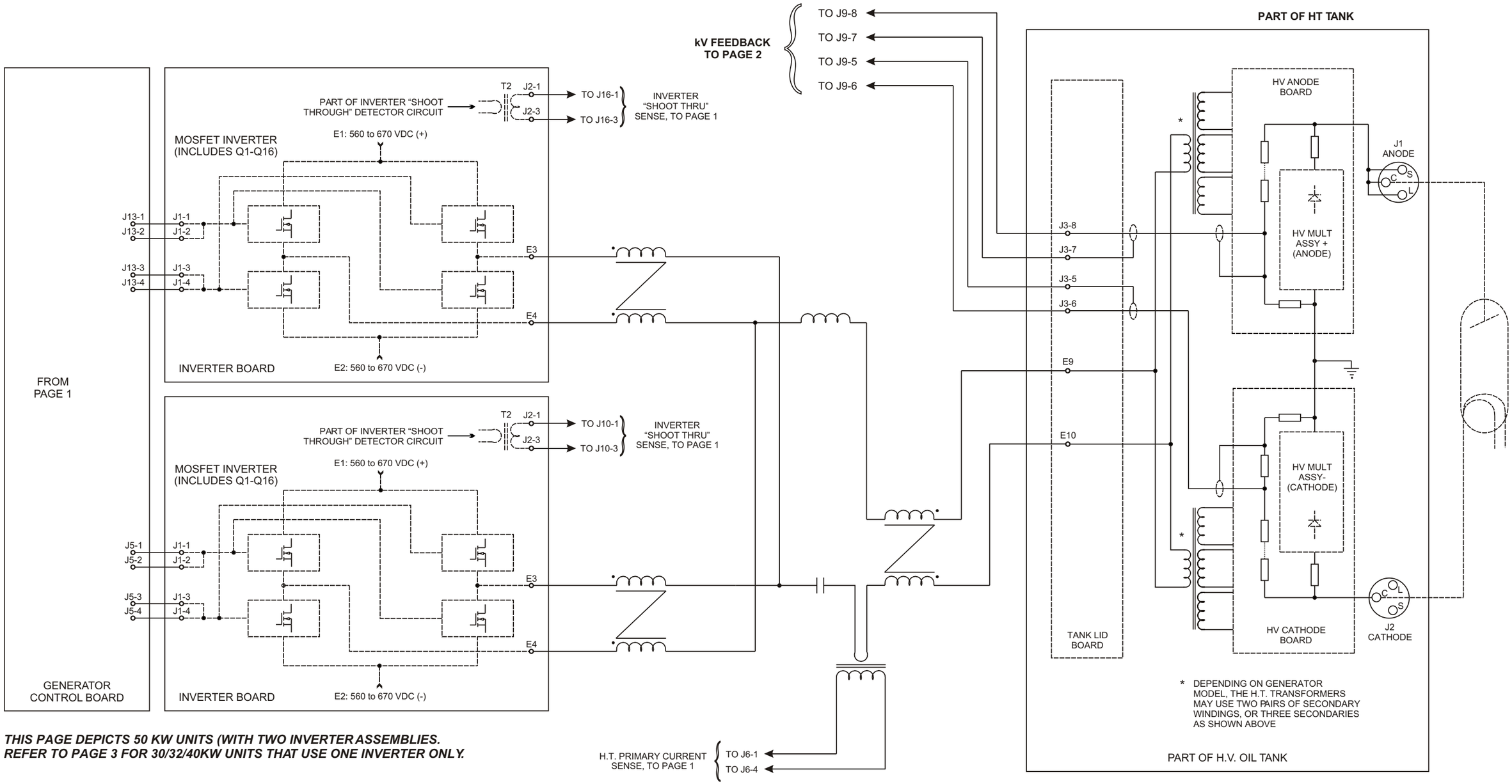
H.T. PRIMARY CURRENT SENSE FROM PAGE 2

X-RAY ENABLE FROM MD-0834

DATABUS D0..D7

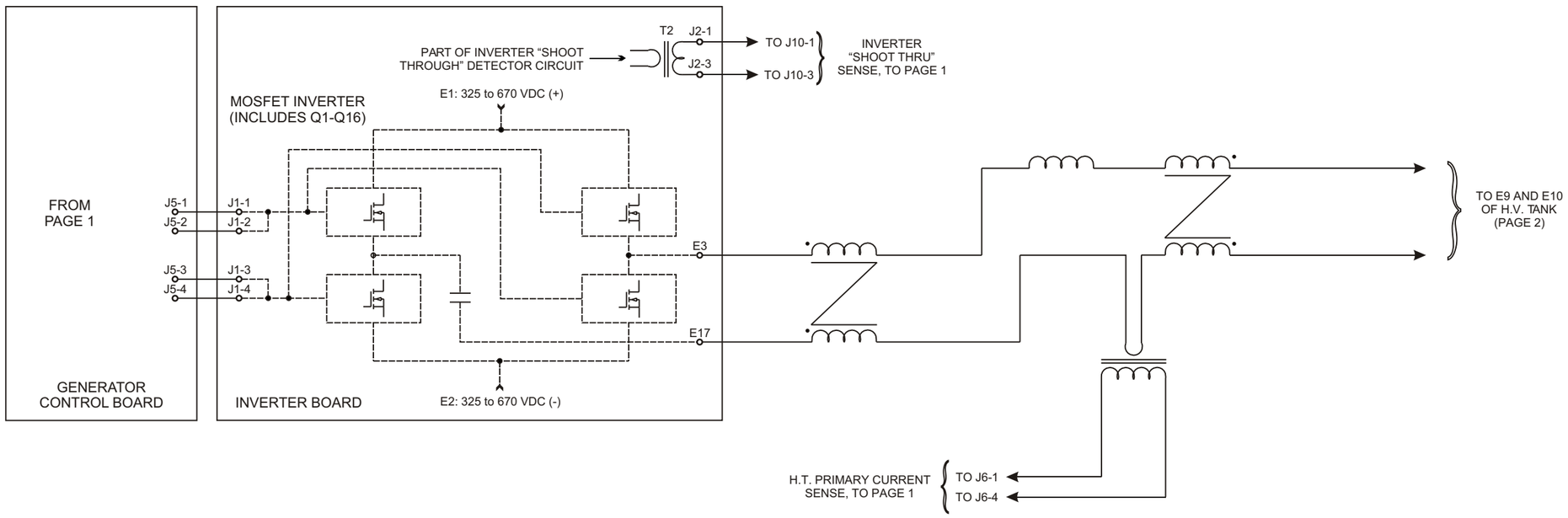
GENERATOR CONTROL BOARD

DRAWN G. SANWALD	DATE 11 FEB 2003	**KV CONTROL & FEEDBACK**
CHECKED Steve Blake	18 FEB/03	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	**MD-0835 REV A**
		SHEET 1 OF 3



THIS PAGE DEPICTS 50 KW UNITS (WITH TWO INVERTER ASSEMBLIES. REFER TO PAGE 3 FOR 30/32/40KW UNITS THAT USE ONE INVERTER ONLY.

DRAWN G. SANWALD	DATE 11 FEB 2003	KV CONTROL & FEEDBACK
CHECKED Steve Blake	18 FEB/03	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	MD-0835 REV A
		SHEET 2 OF 3



NOTE REFERENCE	REMARKS
1	A NARROW PULSE WILL BE PRESENT AT THIS TEST POINT IF AN INVERTER "SHOOT THROUGH" HAS BEEN DETECTED. THE VOLTAGE WAVEFORM AT THIS TEST POINT IS DEPICTED IN FIGURE 1 BELOW. THIS PULSE MAY BE VERY DIFFICULT O DETECT, AS THE INVERTER DRIVE WILL BE SHUT DOWN WHEN A "SHOOT THROUGH" IS DETECTED, THUS REMOVING THE FAULT CONDITION.
2	AS PER # 1.
3	A NARROW PULSE WILL BE PRESENT AT THIS TEST POINT IF KV OVER VOLTAGE HAS BEEN DETECTED (130 KV FOR 125 KV UNITS, 163 KV FOR 150 KV UNITS). REFER TO FIGURE 1. THIS PULSE MAY BE VERY DIFFICULT TO DETECT, AS THE HIGH VOLTAGE WILL BE SHUT DOWN WHEN THE OVER VOLTAGE CONDITION IS DETECTED, THUS REMOVING THE FAULT CONDITION.
4	LOW (APPROXIMATELY 0 VDC) = X-RAY REQUESTED BY THE CPU, HIGH (APPROXIMATELY +5 VDC) = NO X-RAY REQUEST BY THE CPU.
5	A NARROW PULSE WILL BE PRESENT AT THIS TEST POINT IF INVERTER OVER CURRENT HAS BEEN DETECTED. THE VOLTAGE WAVEFORM AT THIS TEST POINT IS DEPICTED IN FIGURE 1 BELOW. THIS PULSE MAY BE VERY DIFFICULT O DETECT, AS THE INVERTER DRIVE WILL BE SHUT DOWN WHEN AN OVER CURRENT CONDITION S DETECTED, THUS REMOVING THE FAULT CONDITION.
6	LOW (APPROXIMATELY 0 VDC) = NO FAULT PRESENT, ALLOW AN X-RAY EXPOSURE. HIGH (APPROXIMATELY +5 VDC) = X-RAY EXPOSURE INHIBITED.
7	LOW (APPROXIMATELY 0 VDC) = X-RAY REQUESTED BY CONSOLE, HIGH (APPROXIMATELY +5 VDC) = X-RAY NOT REQUESTED.
8	LOW (APPROXIMATELY 0 VDC) = NAND GATES U17A, U17B DISABLED. HIGH (APPROXIMATELY +5 VDC) = NAND GATES ENABLED, THUS ALLOWING INVERTER GATE DRIVE.
9	LOW (0 VDC) = H.V. TANK CONNECTED, HIGH (APPROXIMATELY +5 VDC) = H.V. TANK NOT CONNECTED.
10	THE VOLTAGE AT TP2 AND TP3 SHOULD BE A 50% DUTY CYCLE SQUARE WAVE, RANGING IN FREQUENCY FROM APPROXIMATELY 80 kHz TO APPROXIMATELY 250 kHz, DEPENDING ON GENERATOR OUTPUT POWER. SEE FIGURE 2.

FIGURE 1

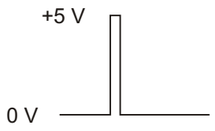
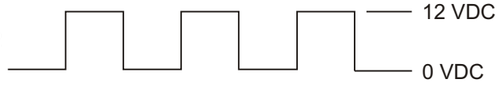


FIGURE 2



DRAWN G. SANWALD	DATE 11 FEB 2003	KV CONTROL & FEEDBACK
CHECKED Steve Blake	18 FEB/03	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	MD-0835 REV A
		SHEET 3 OF 3

REFER TO PAGE 3 FOR LOGIC LEVELS, NOTES, ETC, REFERENCED BY THIS SYMBOL: ⬡

GENERATOR CONTROL BOARD

FILAMENT SUPPLY BOARD

MAXIMUM FILAMENT CURRENT LIMIT CIRCUIT

SET MAX CURRENT

JW1

3 — 6.5 A

2 — 5.5 A

1

U1A

RN3A

-12V

ERROR AMPLIFIER, PWM REGULATOR, AND FILAMENT CURRENT DRIVERS

+35V

Q6

Q12

Q7

Q13

C22

-35V

U3

PWM REGULATOR

U4B

U1B

U52B

U48 D/A CONV

R206

R218

RN1A

RN1B

RN3G

RN5G

RN4H

RN3F

RN3H

D6

TP4

TP3

TP21

TP4

RN5D

+12V

K1

J14-6

J2-6

J14-5

J2-5

J14-11

J2-11

J14-2

J2-2

RN1C

U2 CPLD

R227

R226

Q19

D38

TP29

TP28

U45 A/D CONV

R215

R213

DATABUS D0..D7

FILAMENT CURRENT SENSE, RMS CONVERTER, AND FILAMENT FEEDBACK

U2B

U4A

U7 RMS CONVERTER

D12, 13 D 27, 28

T1

R21

J5-2 J5-1 J5-4 J5-3

J4-2 J4-1 J4-4 J4-3

L

S

J2 CATHODE

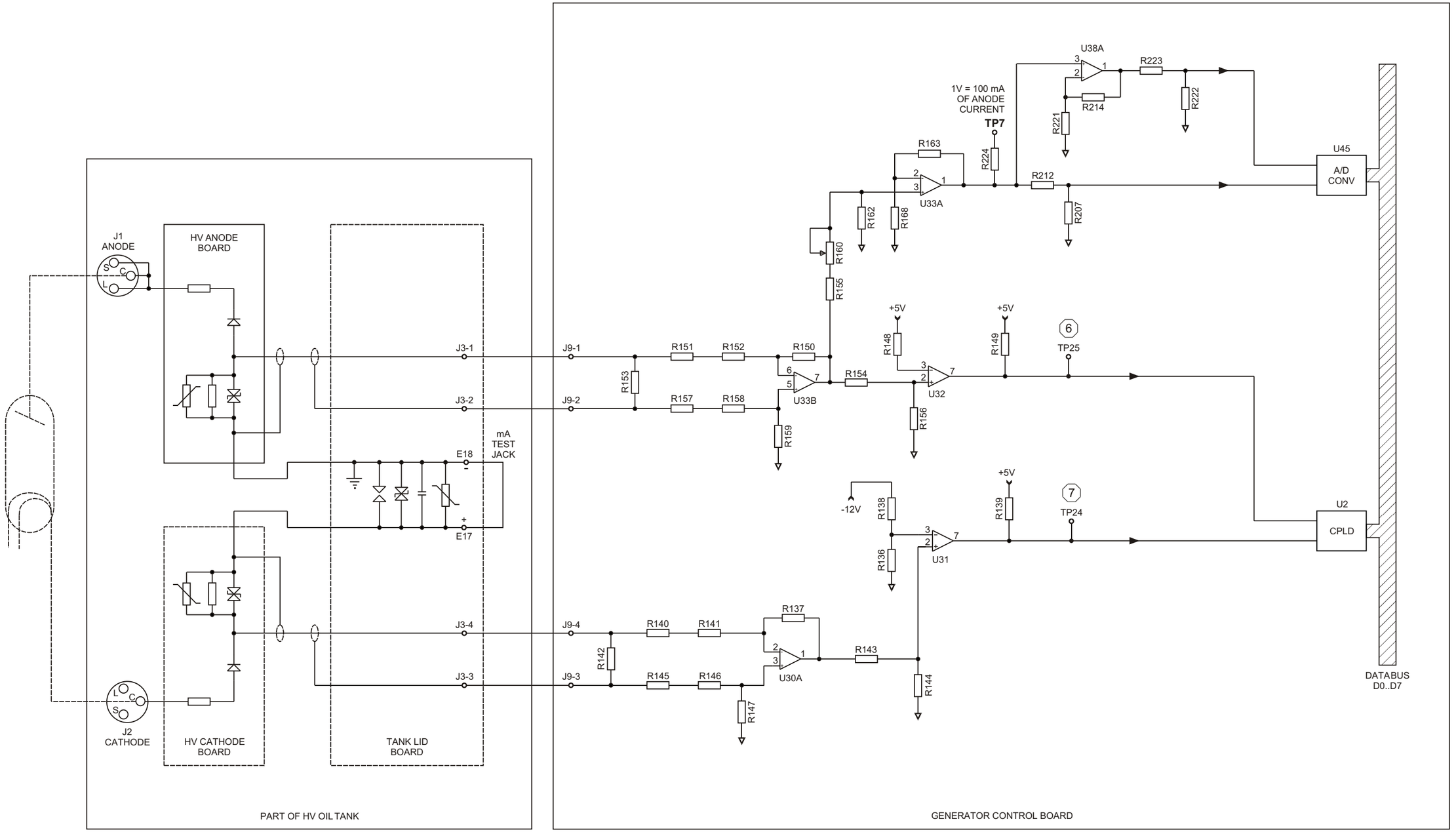
C L S

HV CATHODE BOARD

TANK LID BOARD

PART OF H.V. OIL TANK

DRAWN G. SANWALD	DATE 11 FEB 2003	**FILAMENT DRIVE & MA CONTROL**
CHECKED Steve Blake	18 FEB/03	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	**MD-0836 REV B**
		SHEET 1 OF 3



DRAWN G. SANWALD	DATE 11 FEB 2003	**FILAMENT DRIVE & MA CONTROL**
CHECKED Steve Blake	18 FEB/03	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	**MD-0836 REV B**
		SHEET 2 OF 3

NOTE REFERENCE	REMARKS
1	1 VOLT AT THIS TEST POINT = 1 AMP OF FILAMENT DEMAND.
2	“LOW” (APPROXIMATELY 0 VDC) ENERGIZES K1 ON THE FILAMENT SUPPLY BOARD (SMALL FILAMENT), “HIGH” (APPROXIMATELY +12 VDC) DE-ENERGIZES K1 (LARGE FILAMENT).
3	0.6 VOLT AT THIS TEST POINT = 1 AMP OF ACTUAL FILAMENT CURRENT.
4	1 VOLT AT THIS TEST POINT = 1 AMP OF ACTUAL FILAMENT CURRENT.
5	PWM OUTPUT. THE WAVEFORM WILL BE AS PER FIGURE 1 FOR LOW AND HIGH FILAMENT CURRENT DEMAND.
6, 7	A NARROW PULSE WILL BE PRESENT AT THESE TEST POINTS DURING SEVERE ANODE OR CATHODE OVER CURRENTS (I.E. TUBE OR TANK ARCS). REFER TO FIGURE 2. THESE PULSES MAY BE VERY DIFFICULT TO OBSERVE, AS THE HIGH VOLTAGE WILL SHUT DOWN WHEN A FAULT IS DETECTED, THUS REMOVING THE OVER CURRENT SITUATION.

FIGURE 1

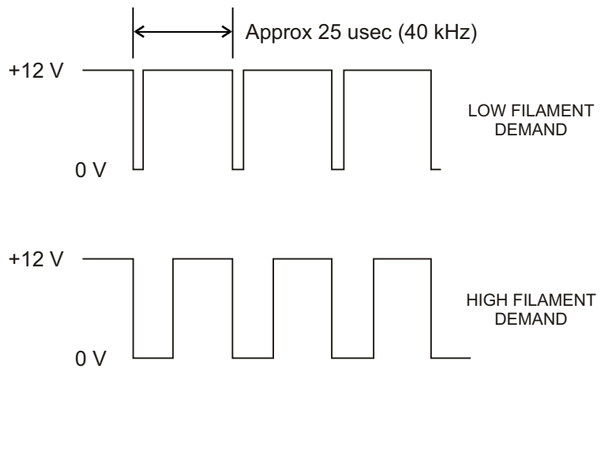
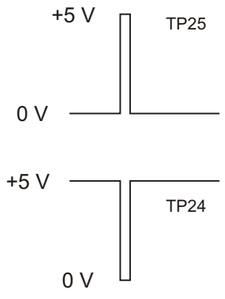
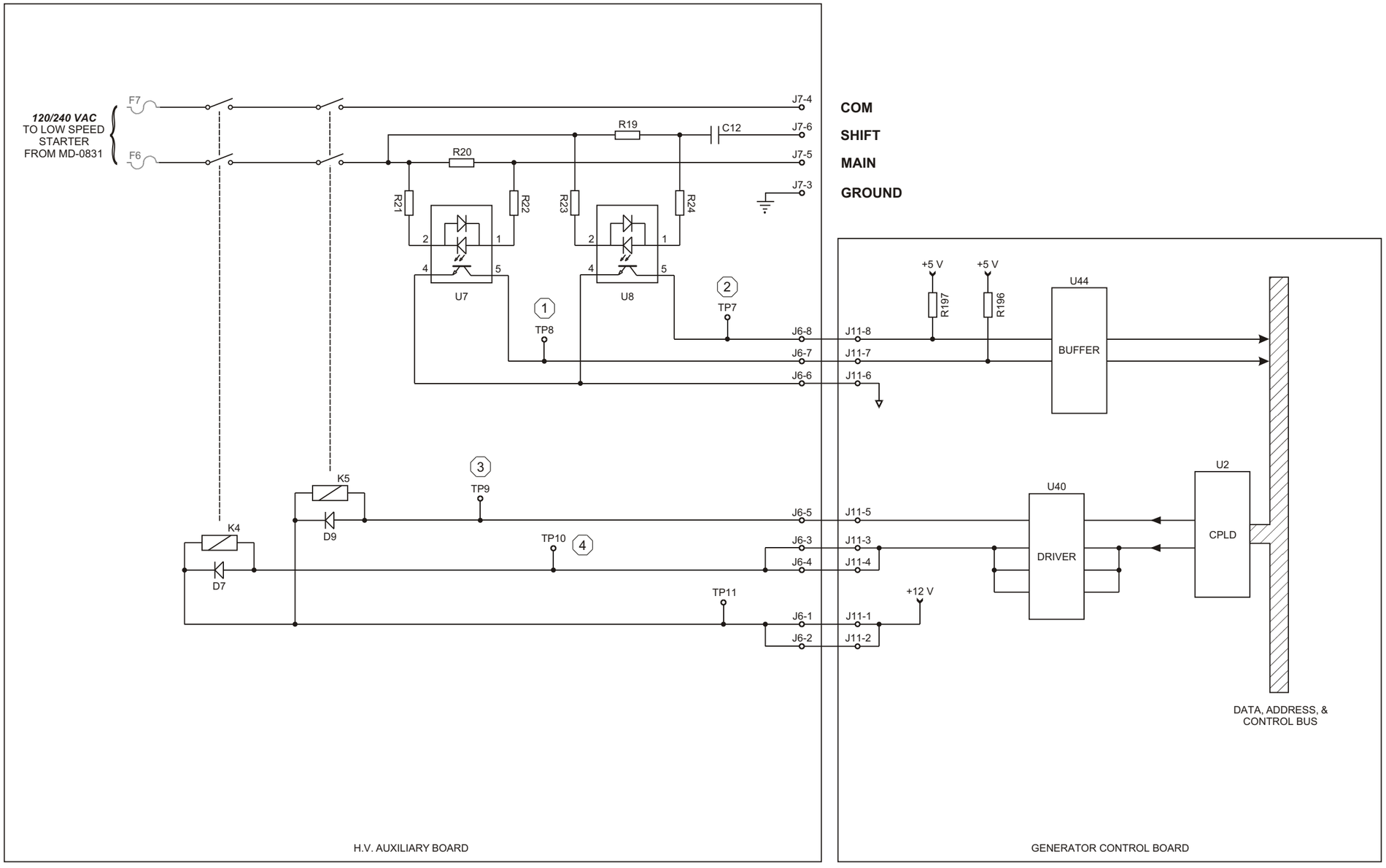


FIGURE 2



DRAWN G. SANWALD	DATE 11 FEB 2003	FILAMENT DRIVE & MA CONTROL
CHECKED Steve Blake	18 FEB/03	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	MD-0836 REV B
		SHEET 3 OF 3



REFER TO PAGE 2 FOR LOGIC LEVELS, NOTES, ETC, REFERENCED BY THIS SYMBOL: ⬡

DRAWN G. SANWALD	DATE 11 FEB 2003	**LOW SPEED STARTER**
CHECKED Steve Blake	18 FEB/03	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	**MD-0837 REV B**
		SHEET 1 OF 2

NOTE REFERENCE	REMARKS
1	MAIN STATOR CURRENT SENSE. IF MAIN CURRENT IS LOW, THIS WILL BE APPROXIMATELY +5 VDC. PULSES AT 120 HZ WILL BE PRESENT AS SHOWN IN FIGURE 1 AT NORMAL STATOR CURRENT.
2	PHASE-SHIFT STATOR CURRENT SENSE. IF SHIFT CURRENT IS LOW, THIS WILL BE APPROXIMATELY +5 VDC. PULSES AT 120 HZ WILL BE PRESENT AS SHOWN IN FIGURE 1 AT NORMAL STATOR CURRENT.
3	“LOW” (APPROXIMATELY 0 VDC) FOR APPROXIMATELY 1.8 SEC DURING PREP, THEN PULSED LOW FOR 500 MSEC EVERY 5 SECONDS DURING PREP. REFER TO FIGURE 2.
4	“LOW” (APPROXIMATELY 0 VDC) ENERGIZES K4 ON THE H.V. AUXILIARY BOARD, (”HIGH”, + 12 VDC = NOT ENERGIZED). THIS RELAY IS ENERGIZED AFTER THE MAIN BUS CAPACITORS ARE CHARGED, APPROXIMATELY 10 SECONDS AFTER POWER-ON.

FIGURE 1

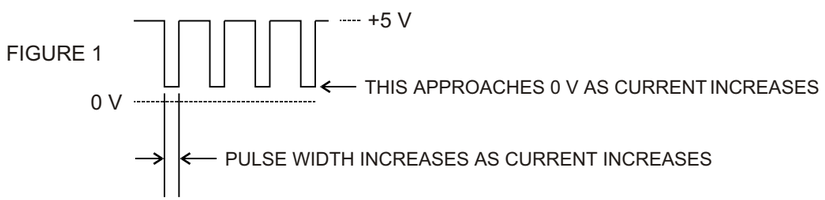
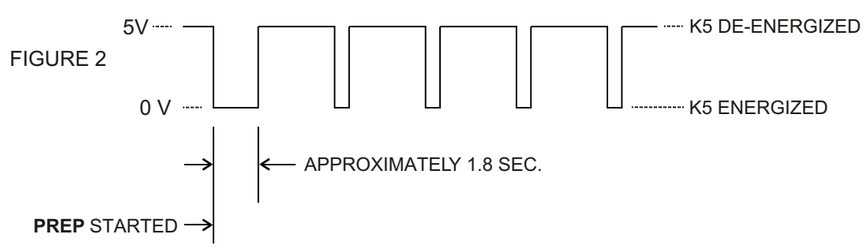
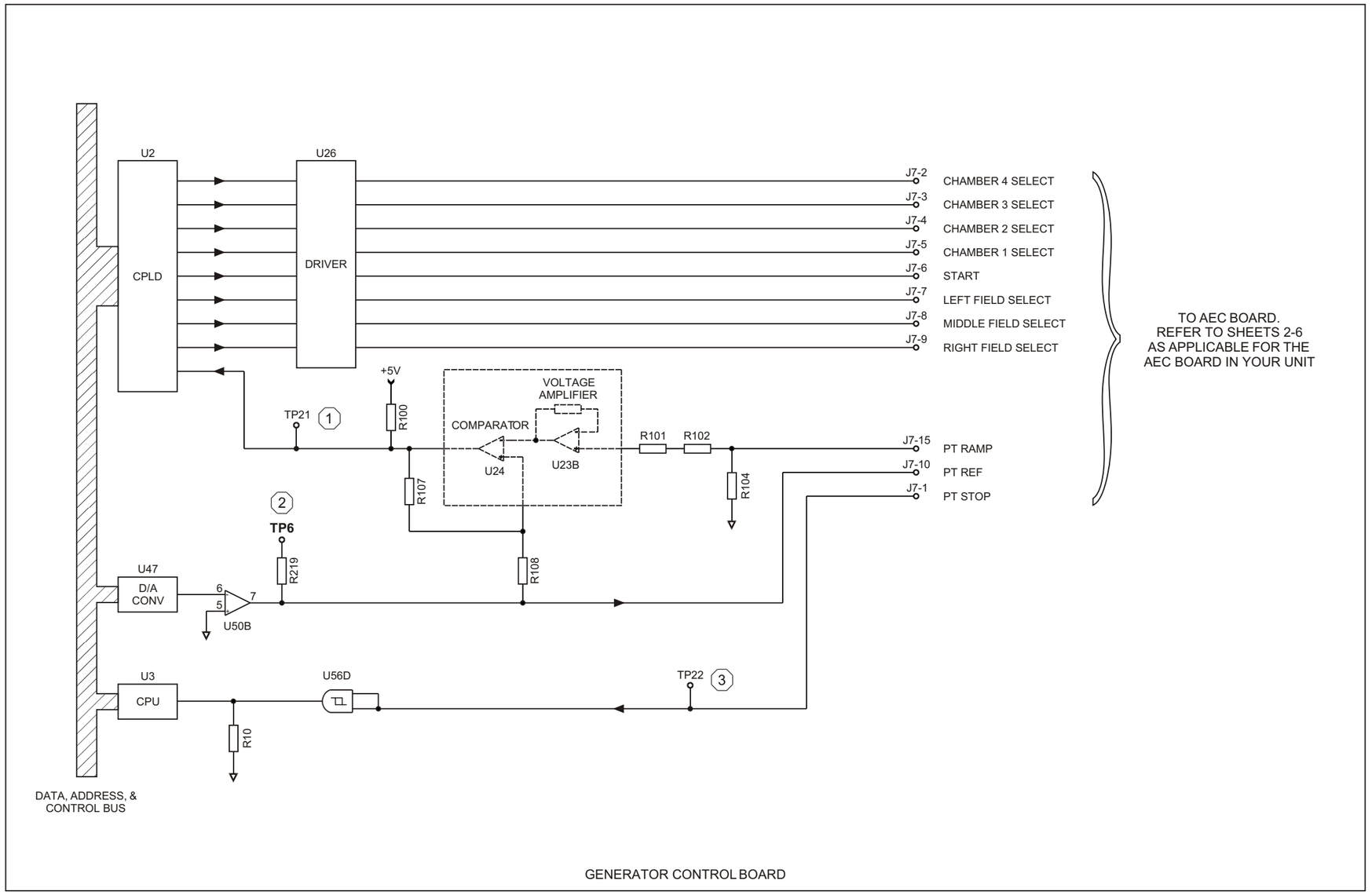


FIGURE 2



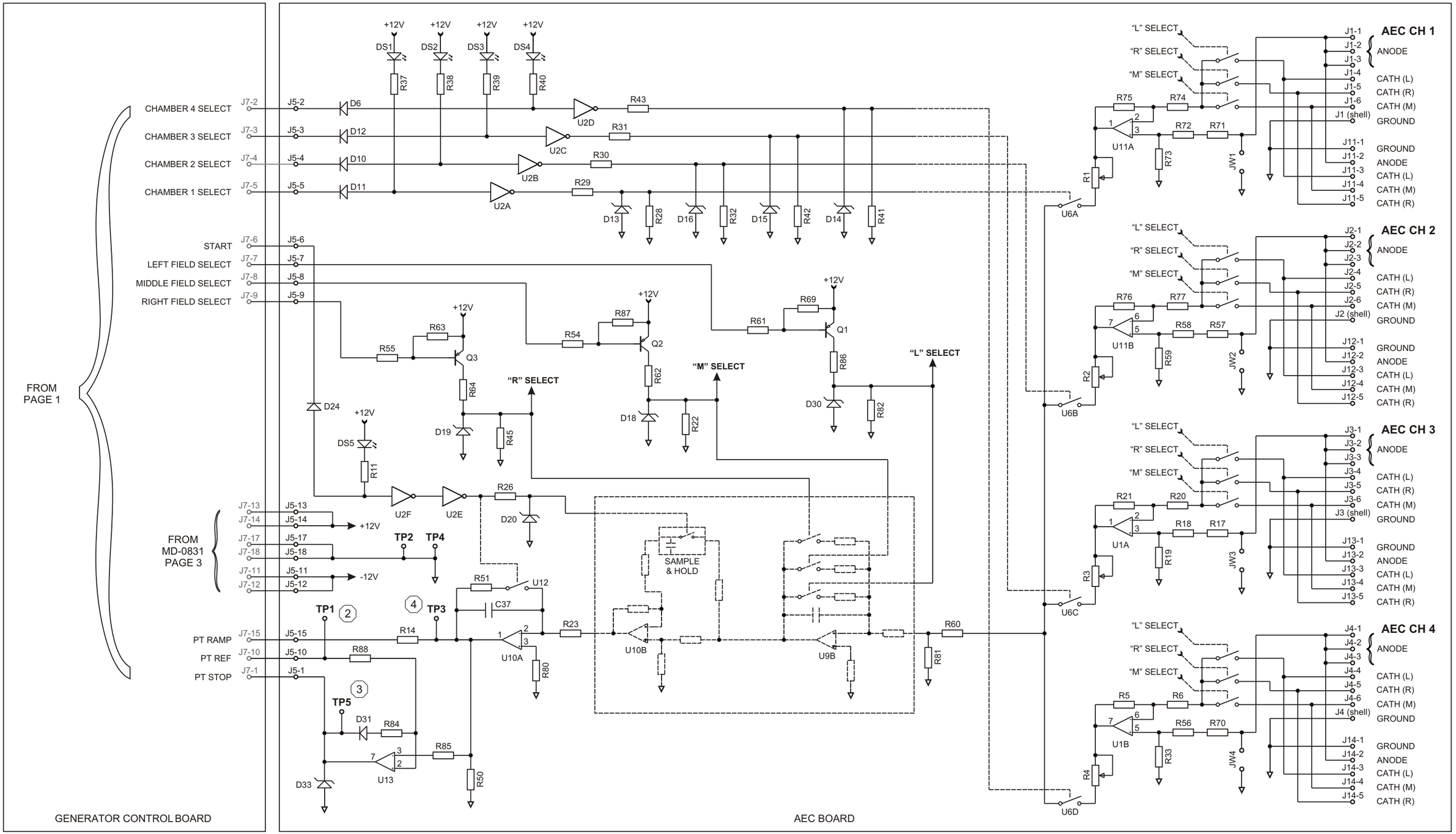
DRAWN G. SANWALD	DATE 11 FEB 2003	LOW SPEED STARTER
CHECKED Steve Blake	18 FEB/03	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	MD-0837 REV B
		SHEET 2 OF 2

REFER TO PAGE 7 FOR LOGIC LEVELS, NOTES, ETC, REFERENCED BY THIS SYMBOL: ⬡



GENERATOR CONTROL BOARD

DRAWN G. SANWALD	DATE 13 FEB 2003	AEC
CHECKED Steve Blake	18 FEB/03	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	MD-0838 REV C
		SHEET 1 OF 7

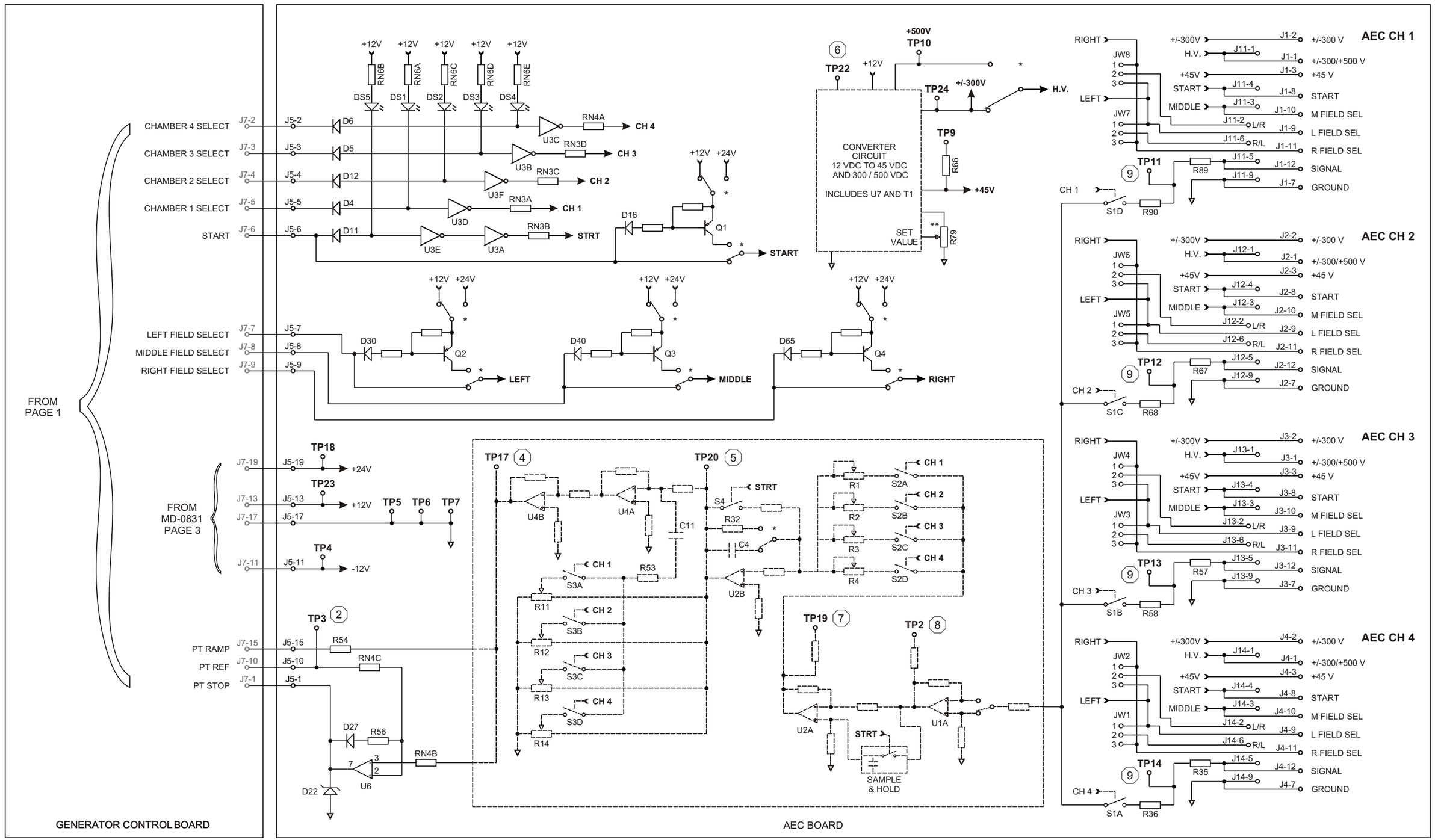


THIS SHEET APPLIES TO AEC BOARD ASSEMBLY 733347

REFER TO CHAPTER 3D FOR INSTALLATION AND CALIBRATION DETAILS.

DESIGNATES AN ANALOG SWITCH. THESE ARE I.C. "SWITCHES" THAT ARE SWITCHED ON / OFF BY APPLYING THE APPROPRIATE LOGIC LEVEL (0V = OFF, 12V = ON).

DRAWN G. SANWALD	DATE 13 FEB 2003	AEC
CHECKED Steve Blake	18 FEB/03	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	MD-0838 REV C
		SHEET 2 OF 7



THIS SHEET APPLIES TO AEC BOARD ASSEMBLY 734614

REFER TO CHAPTER 3D FOR INSTALLATION AND CALIBRATION DETAILS.

THE +/- 12V OUTPUTS ON J1 TO J4 AND J11 TO J14 ARE NOT SHOWN ON THIS DIAGRAM. THESE ARE DETAILED ON THE CONNECTOR PIN OUT TABLES IN CHAPTER 3D.

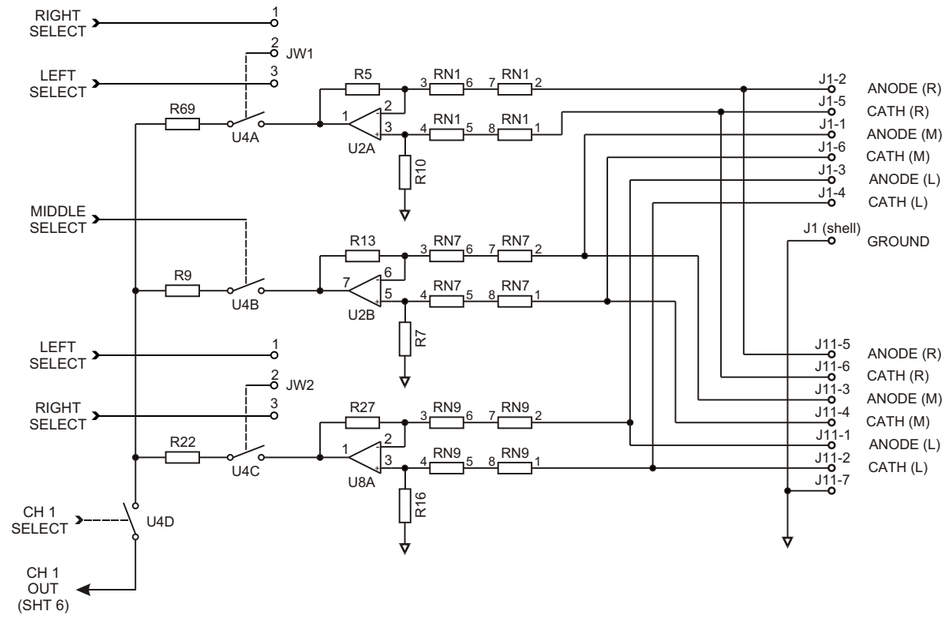
** R79 ADJUSTS THE +45V, +300V, AND +500V OUTPUTS FROM THE DC TO DC CONVERTER CIRCUIT. REFER TO CHAPTER 3D FOR DETAILS.

DESIGNATES AN ANALOG SWITCH. THESE ARE I.C. “SWITCHES” THAT ARE SWITCHED ON / OFF BY APPLYING THE APPROPRIATE LOGIC LEVEL.

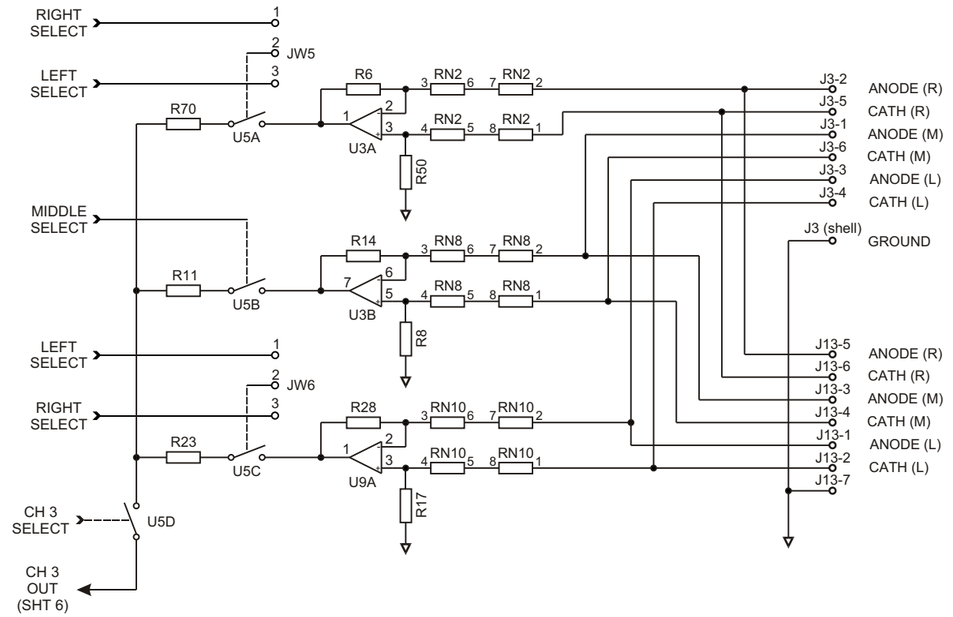
DESIGNATES A FACTORY CONFIGURED LOGIC OR SIGNAL LEVEL. AEC BOARDS ARE CONFIGURED AT THE TIME OF ORDER TO BE COMPATIBLE WITH THE SPECIFIED AEC CHAMBER(S). FOR EXAMPLE, THE **START** SIGNAL TO THE CHAMBER MAY BE FACTORY CONFIGURED TO BE ACTIVE LOW (0 V), ACTIVE HIGH (+12 V), OR ACTIVE HIGH (+24 V).

DRAWN G. SANWALD	DATE 13 FEB 2003	AEC
CHECKED Steve Blake	18 FEB/03	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	MD-0838 REV C
		SHEET 3 OF 7

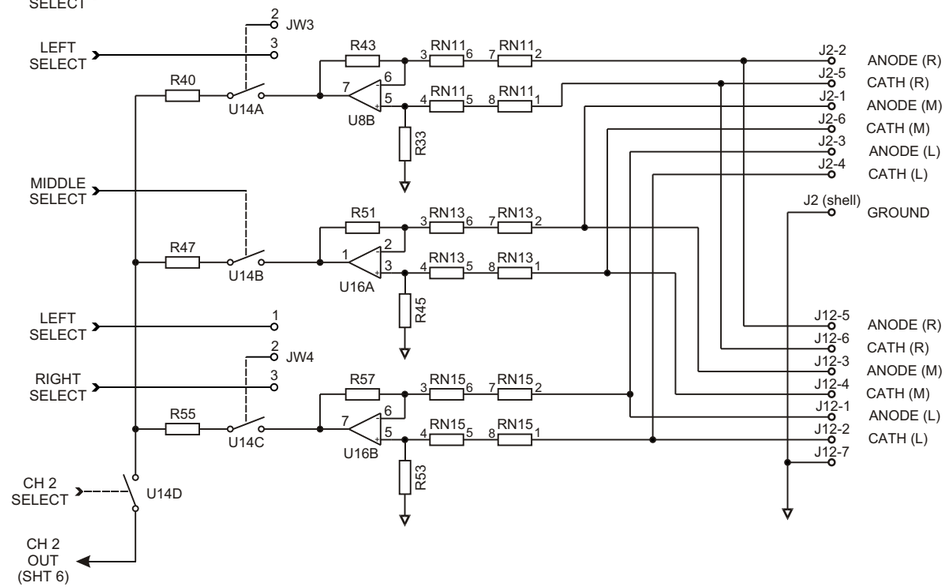
AEC CH 1



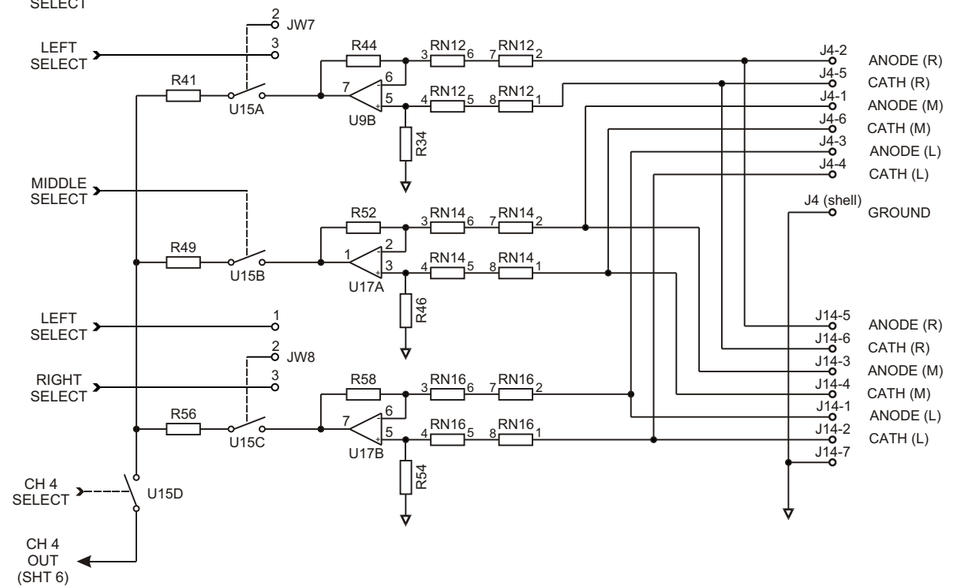
AEC CH 3



AEC CH 2



AEC CH 4

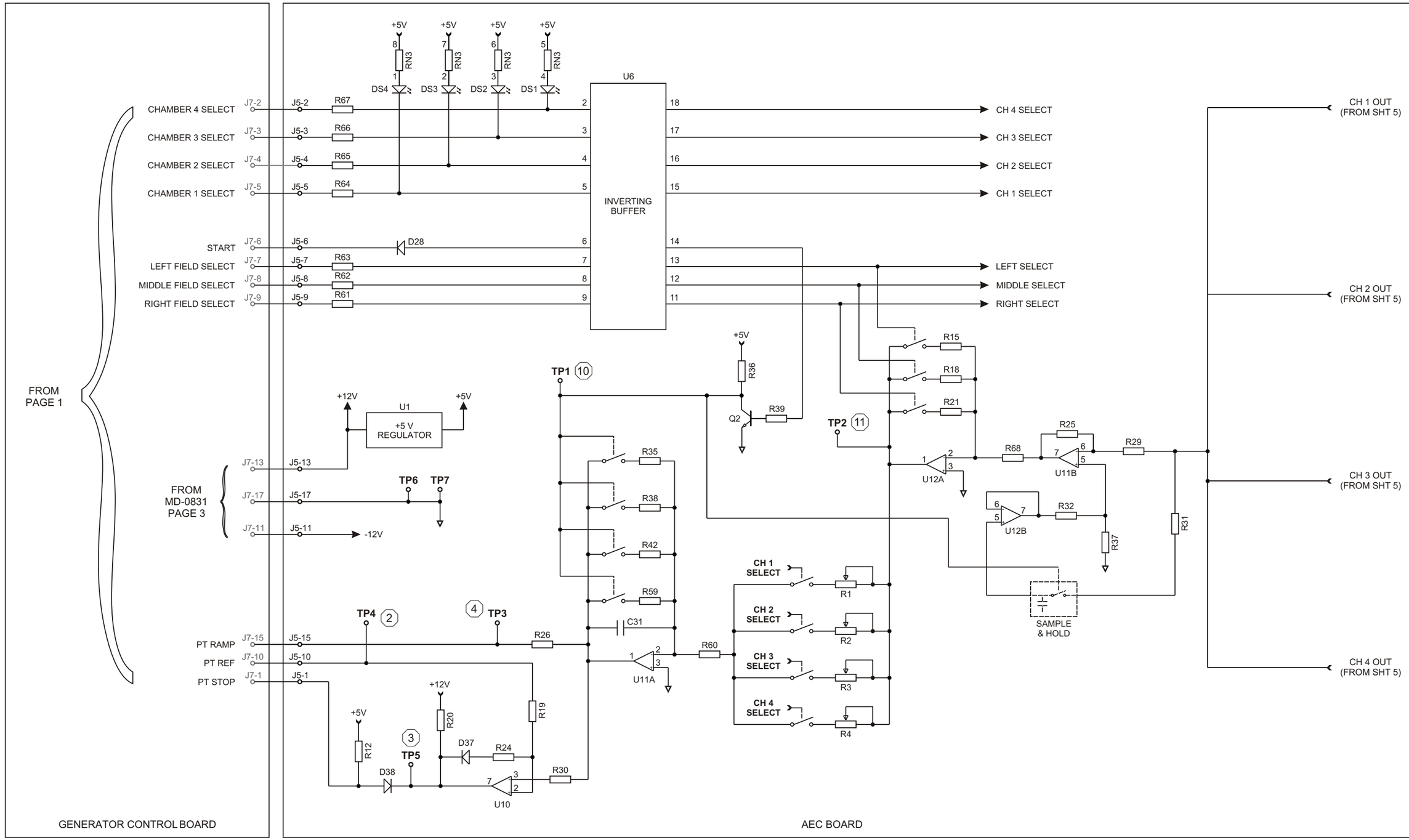


THIS SHEET APPLIES TO AEC BOARD ASSEMBLY 737992. THIS PAGE SHOWS THE INPUT CIRCUITS; THE SIGNAL PROCESSING CIRCUITS ARE CONTINUED ON THE NEXT PAGE.

REFER TO CHAPTER 3D FOR INSTALLATION AND CALIBRATION DETAILS.

DESIGNATES AN ANALOG SWITCH. THESE ARE I.C. “SWITCHES” THAT ARE SWITCHED ON / OFF BY APPLYING THE APPROPRIATE LOGIC LEVEL (0V = OFF, 5V = ON).

DRAWN G. SANWALD	DATE 13 FEB 2003	AEC
CHECKED Steve Blake	18 FEB/03	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	MD-0838 REV C
		SHEET 4 OF 7

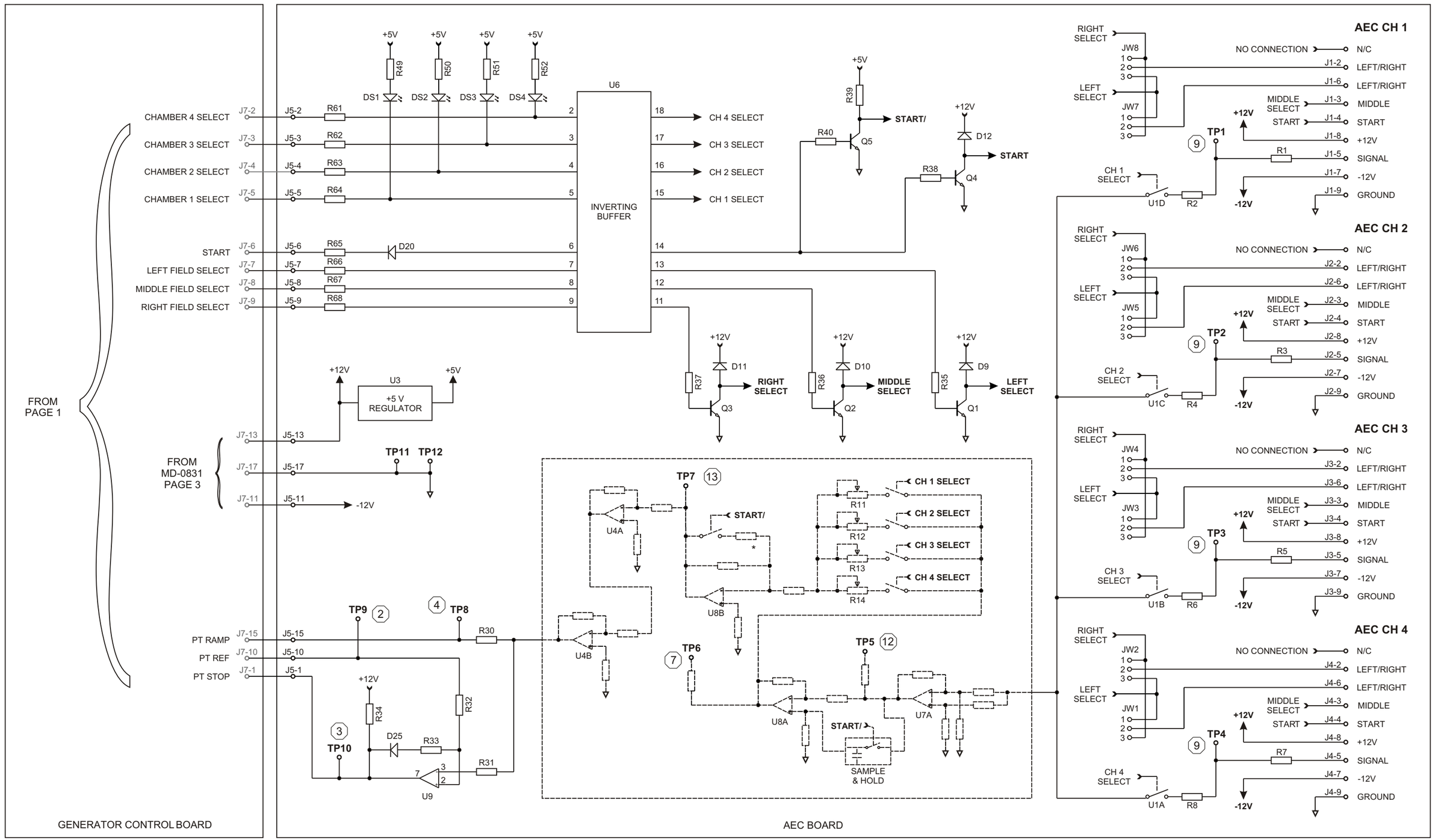


THIS SHEET APPLIES TO AEC BOARD ASSEMBLY 737992. THIS PAGE SHOWS THE SIGNAL PROCESSING CIRCUITS; THE INPUT CIRCUITS ARE SHOWN ON THE PREVIOUS PAGE.

REFER TO CHAPTER 3D FOR INSTALLATION AND CALIBRATION DETAILS.

DESIGNATES AN ANALOG SWITCH. THESE ARE I.C. “SWITCHES” THAT ARE SWITCHED ON / OFF BY APPLYING THE APPROPRIATE LOGIC LEVEL (0V = OFF, 5V = ON).

DRAWN G. SANWALD	DATE 13 FEB 2003	AEC
CHECKED Steve Blake	18 FEB/03	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	MD-0838 REV C
		SHEET 5 OF 7



THIS SHEET APPLIES TO AEC BOARD ASSEMBLY 737998

REFER TO CHAPTER 3D FOR INSTALLATION AND CALIBRATION DETAILS.

DESIGNATES AN ANALOG SWITCH. THESE ARE I.C. “SWITCHES” THAT ARE SWITCHED ON / OFF BY APPLYING THE APPROPRIATE LOGIC LEVEL.

DRAWN G. SANWALD	DATE 13 FEB 2003	AEC
CHECKED Steve Blake	18 FEB/03	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	MD-0838 REV C
		SHEET 6 OF 7

NOTE REFERENCE	REMARKS
1	GENERATES A PULSE PER FIGURE 1 WHEN THE AEC RAMP IS APPROXIMATELY 5 % OF THE AEC REFERENCE IF THE AEC RAMP IS ON THE CORRECT TRAJECTORY.
2	AEC REFERENCE VOLTAGE, 0 TO +10 VDC, DEPENDING ON AEC TECHNIQUE. THE LENGTH OF THE AEC EXPOSURE IS PROPORTIONAL TO THE AEC REFERENCE VOLTAGE.
3	AEC STOP (PT STOP) SIGNAL. THIS IS NORMALLY HIGH (APPROXIMATELY +5 VDC), SWITCHING LOW WHEN THE AEC RAMP = THE AEC REFERENCE VOLTAGE. REFER TO FIGURE 1.
4	AEC RAMP. THIS IS A SIGNAL RAMPING FROM 0 TOWARD +10 VDC, THE ACTUAL MAGNITUDE WILL DEPEND ON THE AEC TECHNIQUE. REFER TO FIGURE 2.
5	AS PER # 4.
6	PWM OUTPUT. THIS WILL BE VARIABLE WIDTH PULSES (PULSE WIDTH INCREASING AT INCREASING LOAD), UP TO A MAXIMUM OF 50% DUTY CYCLE. REFER TO FIGURE 4.
7	AEC RAMP OR DC VOLTAGE. THIS IS A RAMP OR DC VOLTAGE, DEPENDING ON AEC CHAMBER TYPE (INTEGRATING OR NON-INTEGRATING). REFER TO FIGURE 3.
8	AS PER # 7, EXCEPT THAT THE RAMP OR DC VOLTAGE WILL BE POSITIVE GOING AND NOT OF THE SAME MAGNITUDE.
9	THE VOLTAGE AT THIS TEST POINT IS THE OUTPUT OF THE AEC CHAMBER. REFER TO THE AEC CHAMBER MANUFACTURERS DOCUMENTATION FOR DETAILS.
10	THIS IS THE START SIGNAL. “HIGH” (5 VDC) = $\overline{\text{START}}$ = ANALOG SWITCHES CLOSED, “LOW” (0 VDC) = START = ANALOG SWITCHES OPEN.
11	THIS WILL BE A NEGATIVE DC VOLTAGE. THE MAGNITUDE OF THE DC VOLTAGE IS DEPENDENT ON THE AEC TECHNIQUE IN USE.
12	AS PER # 7, EXCEPT THAT THE POLARITY WILL BE POSITIVE.
13	THE POLARITY AND MAGNITUDE OF THE RAMP AT THIS POINT SHOULD BE APPROXIMATELY THE SAME AS THE **PT RAMP** OUTPUT. NOTE REFERENCE 4.

FIGURE 1

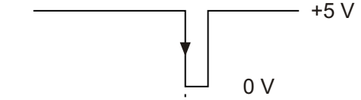


FIGURE 2

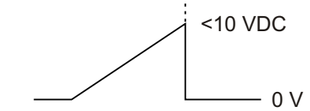
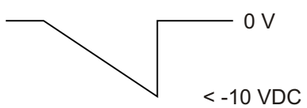
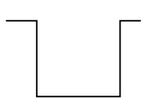


FIGURE 3



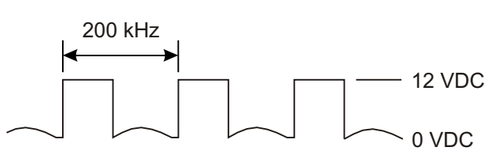
INTEGRATING
AEC CHAMBERS

OR

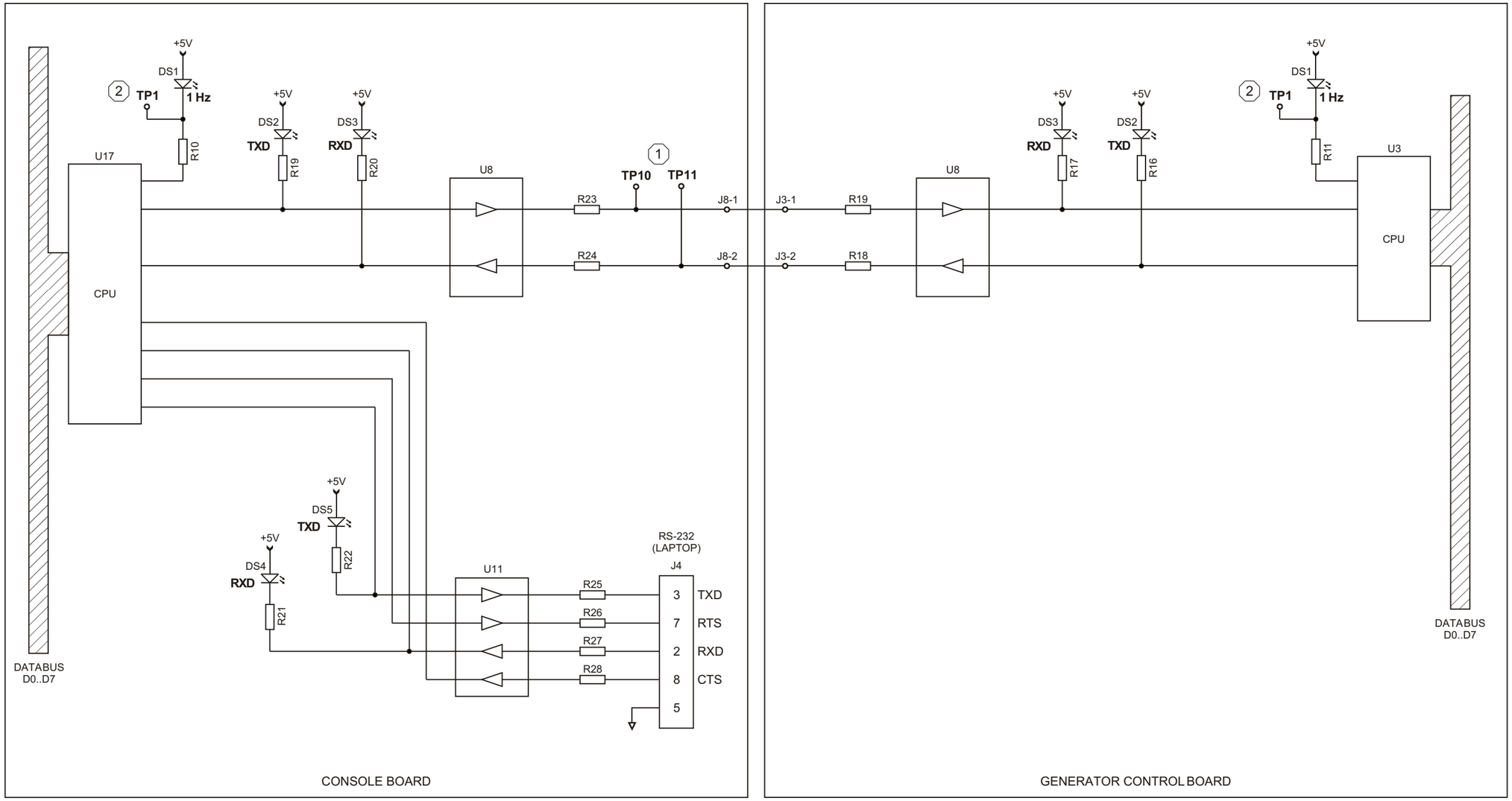


NON-INTEGRATING
AEC CHAMBERS

FIGURE 4



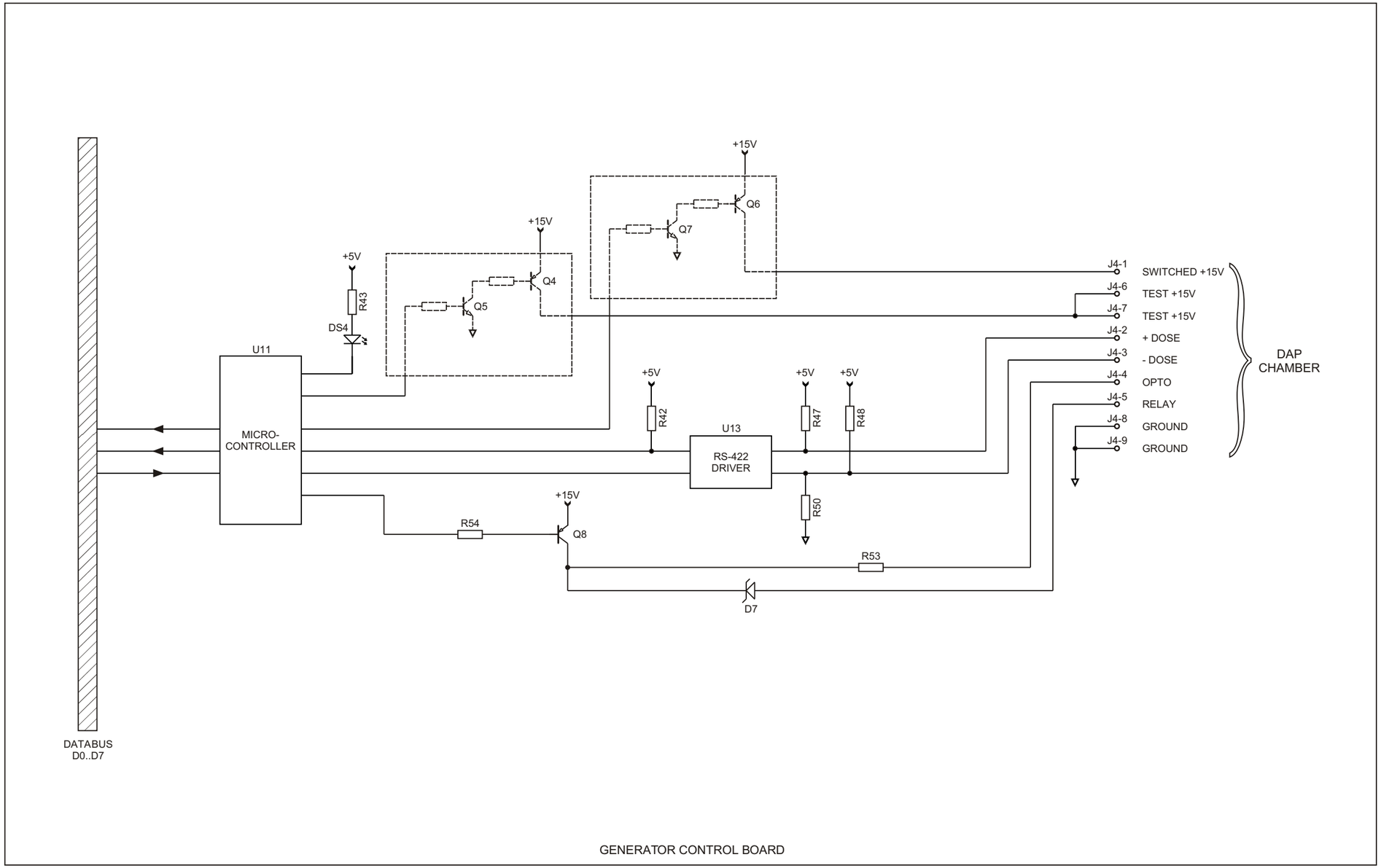
DRAWN G. SANWALD	DATE 13 FEB 2003	AEC
CHECKED Steve Blake	18 FEB/03	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	MD-0838 REV C
		SHEET 7 OF 7



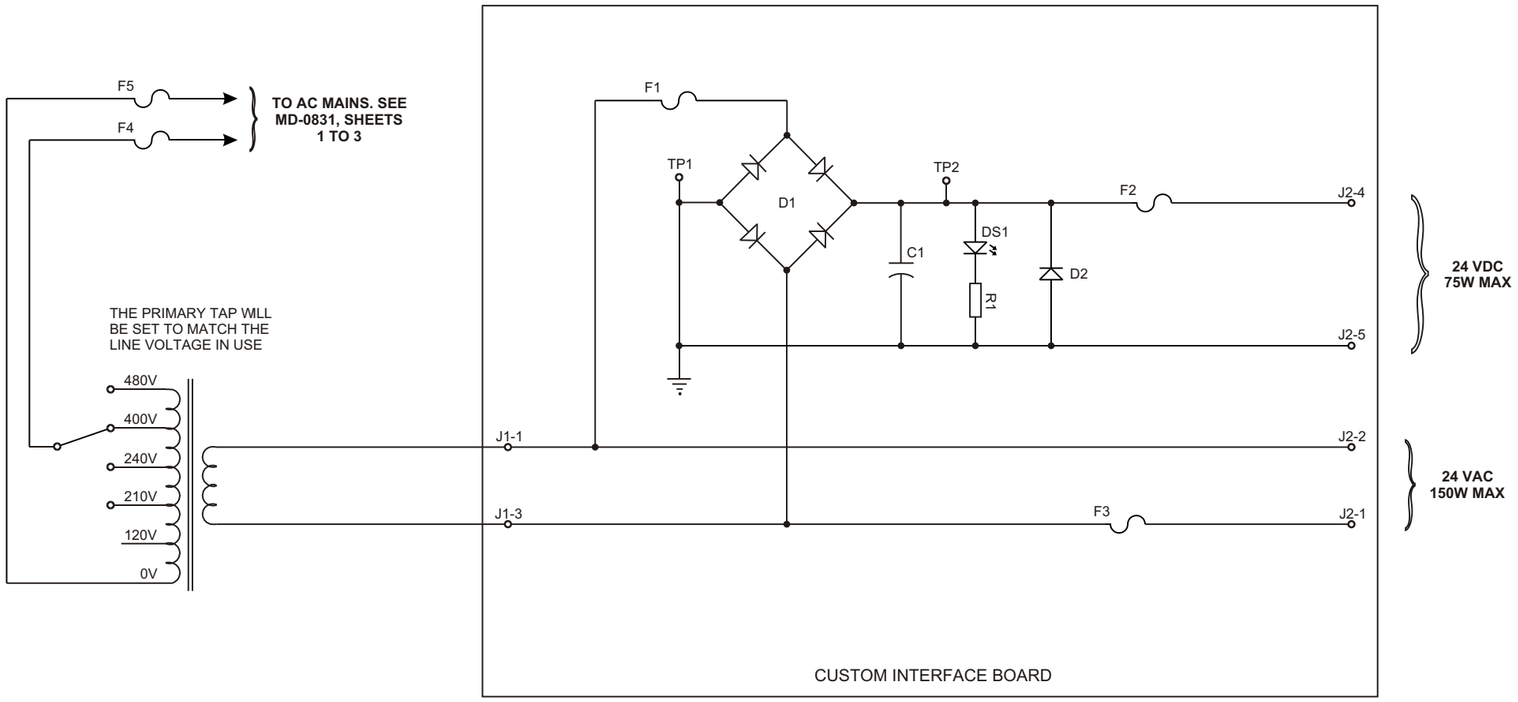
1. A PULSE TRAIN WILL BE OBSERVED AT TP10, TP11 DURING CONSOLE - GENERATOR COMMUNICATION. THE TXD AND RXD LEDs ON THE CONSOLE BOARD AND GENERATOR CONTROL BOARD WILL FLASH TO INDICATE THE PRESENCE OF THESE PULSES.

2. THIS LED SHOULD FLASH AT A CONSTANT 1 HZ RATE, INDICATING THAT THE CPU IS FUNCTIONAL.

DRAWN G. SANWALD	DATE 11 FEB 2003	**SERIAL COMMUNICATIONS**
CHECKED Steve Blake	18 FEB/03	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	**MD-0839 REV A**
		SHEET 1 OF 1



DRAWN G. SANWALD	DATE 11 FEB 2003	DAP
CHECKED Steve Blake	18 FEB/03	
DES.\MFG.\AUTH. ED WOOD	FEB 13/03	MD-0840 REV A
		SHEET 1 OF 1



DRAWN G. SANWALD	DATE 15 JULY 2003	AUX 24VAC / 24VDC POWER DIST (OPTIONAL)
CHECKED JAC	15 JULY 2003	
DES.\MFG.\AUTH. J. CUNNINGHAM	15 JULY 2003	MD-0841 REV A
		SHEET 1 OF 1