

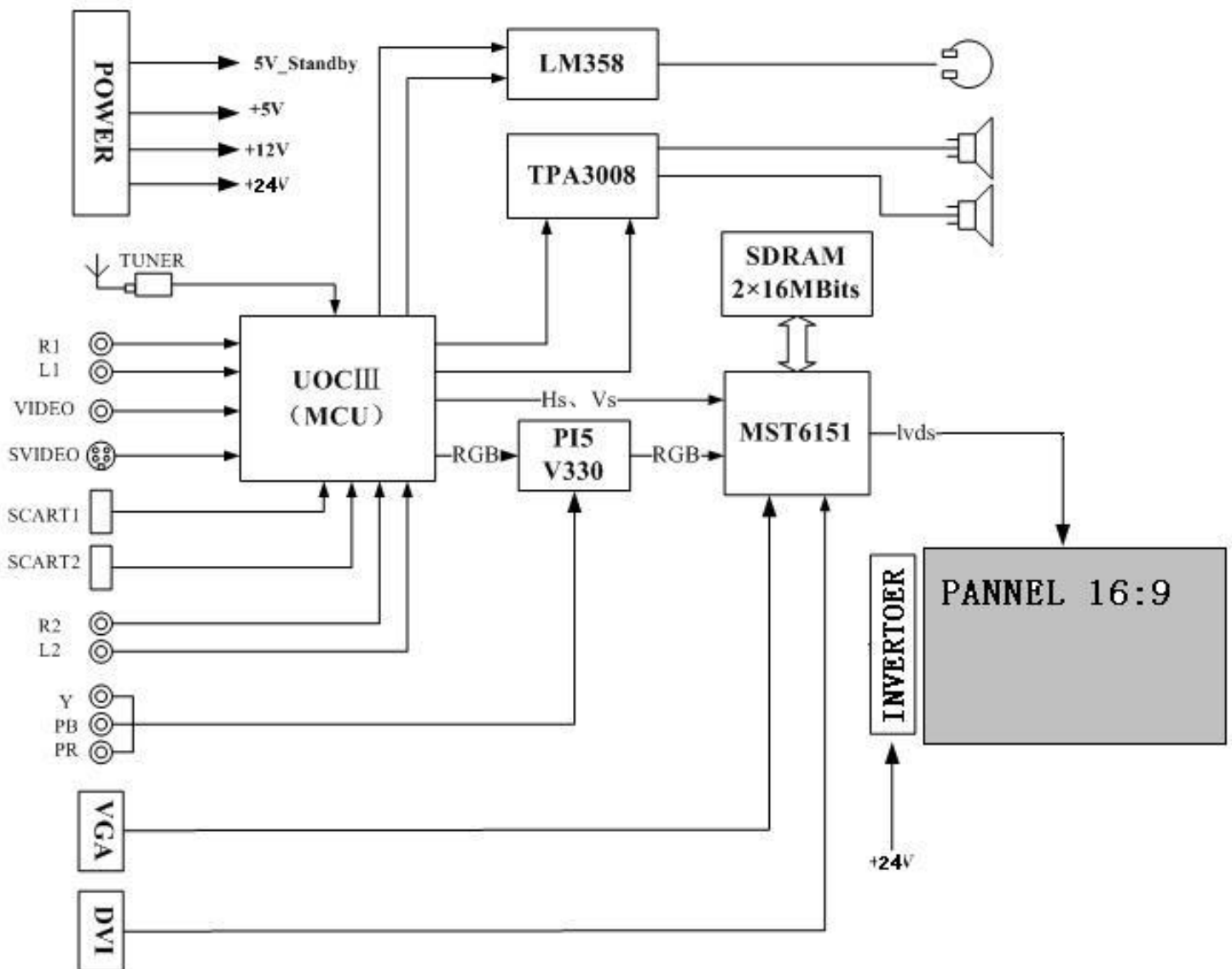
LM21 Chassis Service manual V1.0

(Dec. 2005)

Foxit Reader Pro (Evaluation Version)

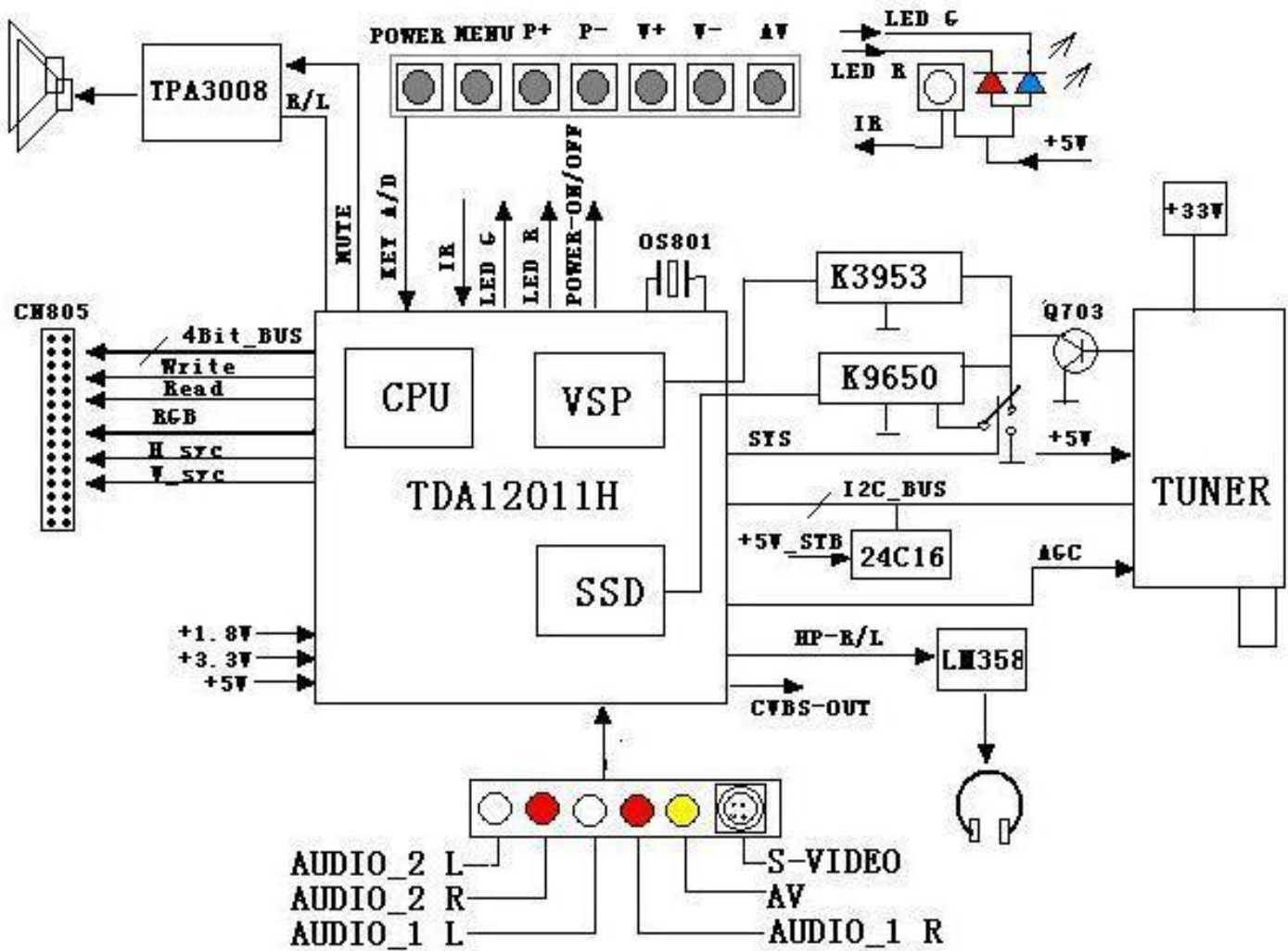
East kit electronic (China) Company Limited

Block diagram



LM21 chassis was combined with PHILIPS 3rd 'One Chip' technology named UOCIII chip set. The chip is integrated by a 51 Core MPU as control center, and 128Kbyte or 256Kbyte code Flash-ROM. The PHILIPS VSP (Video signal processor) is used as TV's picture processor and SSD (Sound signal DSP) used as TV's audio signal processor. The IF signal is output from tuner and amplified by Pre. Amplify department. After the signal through the picture SAW and sound SAW Filter(quasi separate) then it was input the UOCIII chip. Inside the chip the signal was demodulate YC separate and RGB decode by VSP; the DSP of SSD department was worked for FM-demodulate, NICAM or A2 stereo decode, all kinds of audio effect processes include BASS, Treble, Volume and 5 section equalizer etc. the video output of UOCIII is RGB, H_sync, V_sync; audio output is L, R channel audio signal. The RGB,H,V_sync and Y PbPr input were selected by a video switch named FSAV330, through the video switch they were into MST6151A, the scale chip. Inside the chip A/D depart change video signal into digital signal at first. Second the 3D de-interlace part process the digital video. After the movement correction, color progress etc. finally the scaling engine scale the picture into 1366 x 768 and output in LVDS format to the LCD panel. MST6151A was also have a VGA port and DVI port for different high quality signal input. But all analog video (eg. AV; S-video; SCART) was input into UOCIII chip at first, than the signals were into MST6151A after they were changed into RGB signal. At the same time the audio signal was processed by SSD part inside the UOCIII then the audio will be amplified by TPA3008 (TI's class-D power amplifier) before they were input into louder speaker. UOCIII chip was also with a headphone audio output, the headphone signal were amplified by LM358 (NS' double operate amplify). All parts of system were controlled by 51_core MCU inside UOCIII through I2C bus except scale chip. The scaler MST6151A was controlled though 4 Bit parallel bus.

Signal Flowing Chart (analog part)



The analog video part and audio part chips of system were assembled in one main board with tuner. The RF signal passed the tuner was changed frequency in IF signal, before it was transferred in Prep. Amplify. The Pre Amplify was made up with Q703, it was used to compensate the IF losing through the SAW filter. The 33V tuning voltage was outputted by Q504, L511, C530. They were buildup an oscillator to produce 5V AC current approximately 500kHz. Then AC current was rectified by voltage multiplier(D504 double diode). The voltage is changed with the tuner's demodulation in different channels. The Prep. Amp. Amplified IF signal before it pass through the SAW filters(K3953,K9650). IF signal were inputted into UOCIII chip after passed the quasi separate architecture SAW filters. K9650's pass band could be switched for compatible DK.BG,I and L/L'. so Q701 and D701 were combined band switch circuit to change K9650's pass band. When IF was inputted into UOCIII, the VSP part demodulate the video signal, the comb filter separate Y/C signal, the color matrix compose RGB signal. Finally RGB signal and negative pole were transmitted to socket CN805, the cable lines transmit the signal into the digital PCB. At the same time of video demodulation the TeleTXT signal was also decoded by VSP part and the TXT was over lap RGB signal in OSD format. The audio signal was demodulated by DSP inside SSD part(include German's A2 format and British's NICAM format decode). The back part of SSD worked as sound processor. It's include volume, bass, treble adjust; 5 sections equalizer and BBE effect. At last L/R channel sound was outputted form UOCIII chip's Pin-60, Pin-61 to TPA3008's input ports. After been power amplified audio signal was transmitted to loudspeaker.

Functions for each module:

1) Tuner, Pre. Amplify and SAW filters:

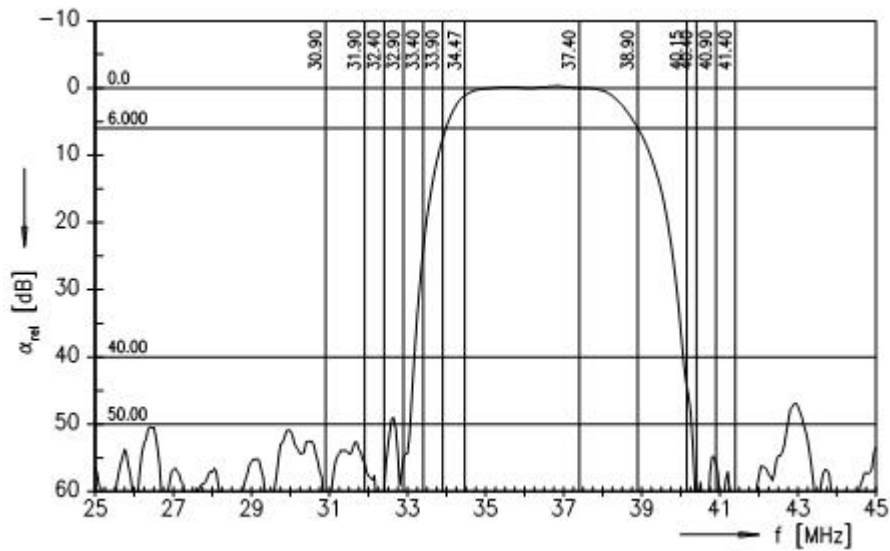
The tuner with frequency synthesizer was PAL/SCAM compatible and controlled by I2C bus. Tuner's Pin-1 is AGC control Pin, The AGC voltage was outputted by UOCIII's Pin-98(AGC_out), the range of AGC is 0V~4V which have 64 ranks adjusting in factory menu. The Pin-2 is NC(not connect). The tuner's slave address was selected by Pin-3, it was connected to GND, so the tuner's slave

address is 0xC0. Pin-4(SCL)and Pin-5(SDA) were I2C control bus. They were connected to I2C BUS through 2 100Ω resistors(R702,R704). Pin-6 is NC. Pin-7 is tuner’s 5V supply pin. Pin-8 is NC. Pin-9 is 33V tuning voltage supply pin, the voltage of the pin will changed from 6V~20V when tuner adjust at different channel. Pin-10 is NC. Pin-11 is IF output pin. The R707 and C703 were matched input impedance of Pre. Amplify. Been the Pre. Amplify, Q703’s gain was select by the ratio of R706 : R711. In system the Pre. Amplify’s gain was 7 times.

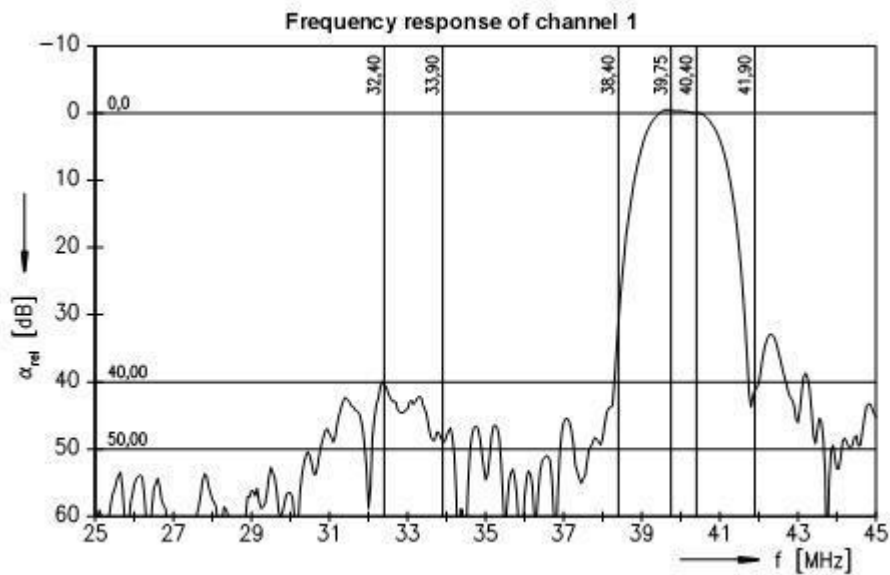
The tuner’s Pin define were list in the form as follows:

Pin No.	Terminal name	Define and Description	Voltage
1	AGC	(AGC voltage supply)	4.0V Gain Max.
2	——	——	——
3	AS	(Slave Address Selection Line)	-0.3V To 5.5V
4	SCL	SCL (Serial Clock Line)	-0.3V To 5.5V
5	SDA	SDL (Serial Data Line)	-0.3V To 5.5V
6	NC	NC (No Connected)	——
7	BP	(+B For PLL & Mixer)	+5V
8	——	——	——
9	BT/LOCK	(Tuning Voltage Supply)	33.0V
10	——	——	——
11	IF1	(IF Output)	——

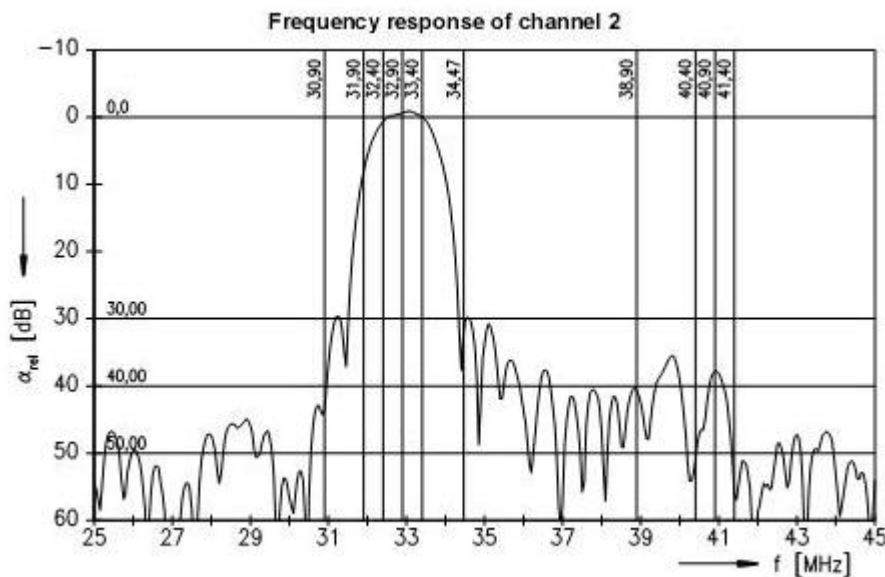
After been Pre. Amplified, the IF signal will pass the SAW filter. The picture SAW is K3953(EPCOS part number), K3953’s pass band is 33.9MHz~38.9MHz, it’s baud chart is listed as follows:



The audio’s SAW filter is K9650(EPCOS part number). It could be switched at 2 pass band. Channel 1 is for 40.40MHz audio carry frequency of L’-NICAM stereo audio signal. The baud chart is as follows:



Channel 2 is for 32.35MHz and 33.40MHz sound carry frequency just like DK,BG,I and L' audio system. The baud chart is as follows:

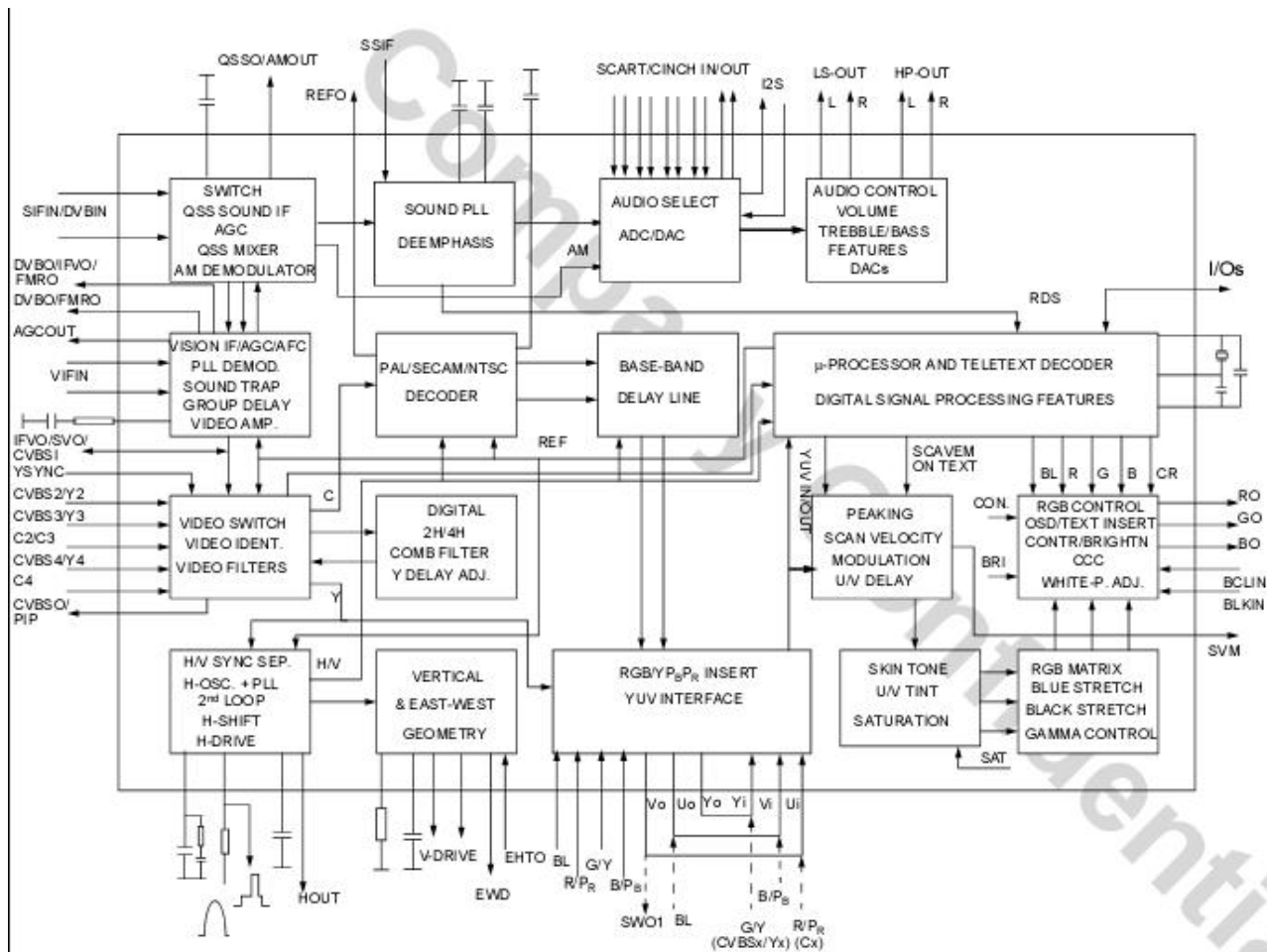


By the way, the part to produce tuning voltage was combined with Q504, D504. the oscillator outputted AC current was rectified by voltage multiplier(D504 double diode) and output 33V DC approximately. If the oscillator was out of work, the 33V tuning voltage will disappear. As the result, the tuner could not search the program. The 500KHz 5V sine wave should be test at Q504's base port by oscilloscope's probe.

2) The parts of UOCIII chip

The UOCIII chip is headquarter of the system's analog signal processor and logical control. The chip has many kinds of configuration and part number. In LM21 chassis, the chip's part number is TDA12021H1/N1D82. Base on PHILIPS chip nomination ruler, TDA12021H1/N1D82 was 'face down' pin configuration chip. It has multi system function, 10 pages TeleTXT storage, audio DSP part, BBE effect and 256Kbyte code FLASH ROM.

Inside chip's function block diagram is as follows:



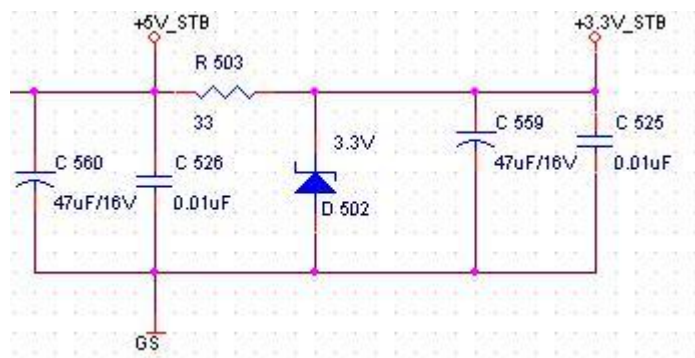
The chips pins list is as follows:

QFP-128 0.8 mm pitch "face down version"			
1	P1.5/TX	98	AVL/SWO/SSIF/REFIN/REFOUT
2	P1.4/RX	99	AUDIOIN6L
3	P1.2/INT2	100	AUDIOIN5R
4	VSSC3	101	AUDOUTSL
5	VDDC3	102	AUDOUTSR
6	P2.5/PWM4	103	DECSDEM
7	P2.4/PWM3	104	AMOUT/QSSO/AUDEEM
8	VSSC1/P	105	GND2
9	P3.3/ADC3	106	PLLIF
10	P3.2/ADC2	107	SIFAGC/DVBAGC
11	DECV1V8	108	DVBO/IFVO/FMRO
12	VDDC1(1.8)	109	DVBO/FMRO
13	P3.1/ADC1	110	VOC8V
14	P3.0/ADC0	111	AGC2SIF
15	P2.3/PWM2	112	VP2
16	P2.2/PWM1	113	SVOIF/OUT/CVBSI
17	P2.1/PWM0	114	AUDIOIN4L
18	P2.0/PMW	115	AUDIOIN4R
19	VDDP(3.3V)	116	CVBS4/Y4
20	P1.7/SDA	117	C4
21	P1.6/SCL	118	AUDIOIN2L/SSIF
22	P1.3/T1	119	AUDIOIN2R
23	P0.0/I2SDI1	120	CVBS2/Y2
24	P0.1/I2SDO1	121	AUDIOIN3L
25	P0.2/I2SDO2	122	AUDIOIN3R
26	P0.3/I2SCLK	123	CVBS3/Y3
27	P0.4/I2SWS	124	C2/C3
28	VSSC2	125	AUDOUTSL
29	VDDC2	126	AUDOUTLSR
30	P1.1/TO	127	AUDOUTHPL
31	P1.0/INT1	128	AUDOUTHPR
32	INT0/P0.5	129	CVBSO/PIIP
33	VDDC1(1.8)	130	BO
34	VSSC1	131	GO
35	VDDA2(3.3V)	132	BLKIN
36	VDDA1(3.3V)	133	BCLIN
37	VDDA(1.8V)	134	VP3
38	GND4	135	GND3
39	VREFAD_POS	136	BP _{IN} 3
40	VREFAD_NEG	137	GY _{IN} 3
41	VDDA1(3.3V)	138	RP _{IN} 3
42	BO	139	INSW3
43	RO	140	VOUT(SWO1)
44	BLKIN	141	UOUT(INSW2)
45	BCLIN	142	YOUT
46	VP3	143	YSYNC
47	GND3	144	YIN(GY2/CVBS/YX)
48	BP _{IN} 3	145	UIN(BP _{IN} 2)
49	GY _{IN} 3	146	VIN(RP _{IN} 2/C-X)
50	RP _{IN} 3	147	VDComb
51	INSW3	148	VSComb
52	VOUT(SWO1)	149	HOUT
53	UOUT(INSW2)	150	FBISO/CSY
54	YOUT	151	SVM
55	YSYNC	152	
56	YIN(GY2/CVBS/YX)	153	
57	UIN(BP _{IN} 2)	154	
58	VIN(RP _{IN} 2/C-X)	155	
59	VDComb	156	
60	VSComb	157	
61	HOUT	158	
62	FBISO/CSY	159	
63	SVM	160	

The UOCIII chip have a complex power supply system. The chip needs 3 kinds of voltage like as 3.3V, 1.8V, 5V. The chip's total power supply pins are listed in the form as follows:

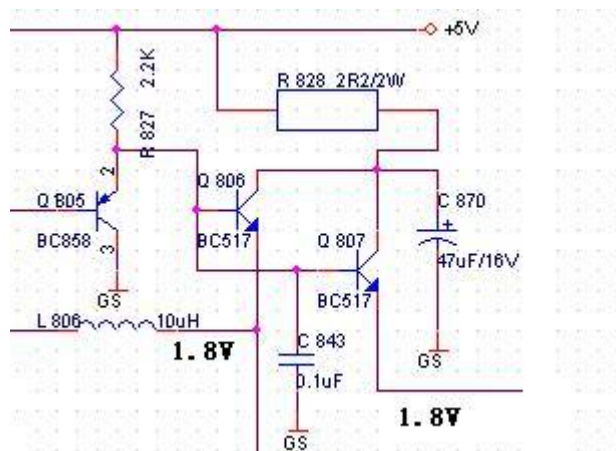
Voltage	Pin NO.	Pin name	Marching filter inductor
3.3V	PIN-4	VDDA3 (3.3V)	L808
	PIN-5	VREF_POS_LSL	L809
	PIN-7	VREF_POS_LSR+HPR	
	PIN-9	VREF_POS_HPR	
	PIN-88	VDDA1	L821
	PIN-90	VREFAD/POS	L816
	PIN-94	VDDA2(3.3V)	L815,R858
	PIN-110	VDDP(3.3V)	L818
5V	PIN-15	VP1	L807
	PIN-45	VCC 8V	L810
	PIN-47	VP2	L811
	PIN-69	VDD comb	L812
	PIN-82	VP3	L831
1.8V	PIN-3	VDDC4	L806
	PIN-93	VDDA(1.8V)	L814
	PIN-96	VDDadc(1.8V)	
	PIN-100	VDDC2	L817
	PIN-118	DECV1V8	L819
	PIN-124	VDDC3	L820

On the other hand, there is a 5V-STB power supply net in the PCB. It was inputted from Pin2 of socket CN501. The net provides 5V Standby voltage independently for CPU working in standby mode. After tune on AC power switch, 5V-STB net always has 5V voltage not only in normal mode but also in standby mode. At the same time, this 5V net passed D502(3.3V Zener diode) and output 3.3V for CPU core and SSD's A/D reference voltage.



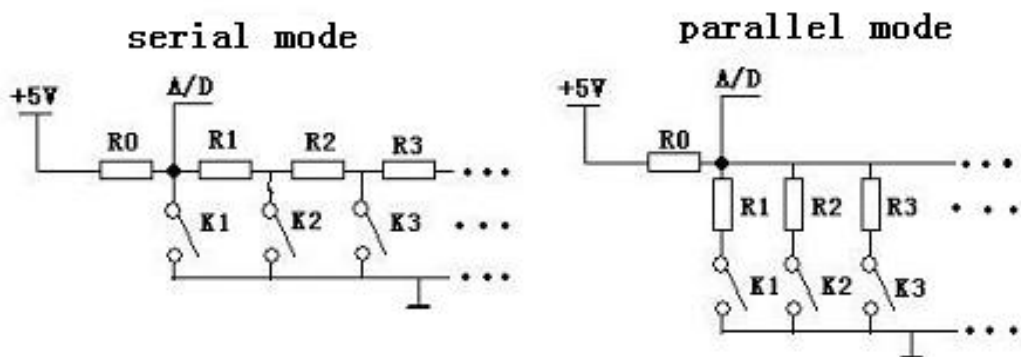
The UOCIII chip's core voltage(1.8V) was produced by the circuit follows. Q806 and Q807 are both Darlington transistor. UOCIII's Pin-14(DECDIG) supply tune on voltage to Q805's base, the voltage of Q805's emitter is steadied about 3.3V, this voltage was inputted into Q806 and Q807's base, Darlington transistor's V_{be} is $0.7V \times 2 = 1.4V$, finally we get $1.8V(3.3V - 1.4V \approx 1.8V)$ at Q806, Q807's emitter point. After filtered by inductor (eg. L806), 1.8V was inputted in UOCIII chip.

Unfortunately when 3.3V or 1.8V net were out of work, as the result, the CPU inside UOCIII could not be programmed update FLASH-ROM. As an experience, if the system could not be updated software in FLASH, you should check each power supply pin of UOCIII listed in the form before. If you want to learn more about software update and download code into FLASH-ROM, please reference <LM21 chassis software update service manual>.



3) The keys on front cabinet:

There are 7 keys on the front cabinet. The keys' architecture was combined with resistors delivery net. The CPU's A/D port will read the key's delivery voltage. To suit for more cabinets, the keys' architecture was serial and parallel 2 modes. Alternative key modes the delivery voltages of each button are same. The key's architecture modes, delivery voltage and resistors were shown below.

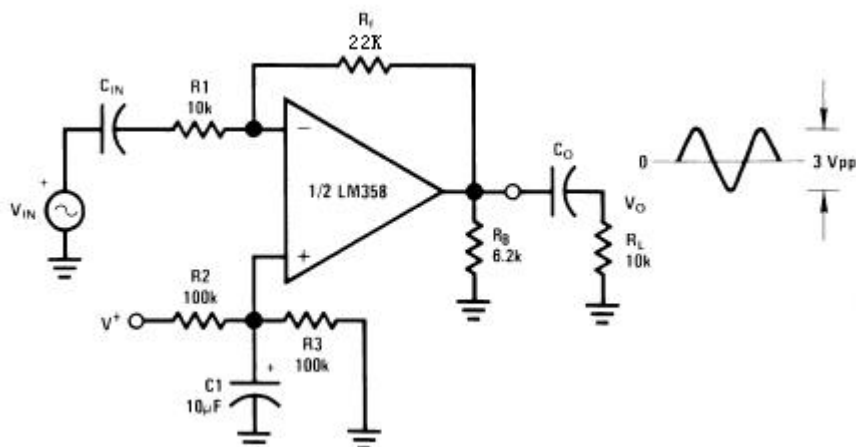


Delivery voltage		0V	0.4V	0.8V	1.2V	1.6V	2.0V	2.4V
Function		POWER	AV	V-	P-	P+	V+	MENU
Part No.	R0	R1	R2	R3	R4	R5	R6	R7
Serial	3.3K	470Ω	560Ω	820Ω	1.5K	1.8K	3.9K	Null
Parallel	3.3K	0Ω	470Ω	1K	1.8K	3K	5.1K	9.1K

When no button was pushed, CPU's A/D pin(Pin-120 ADC3) should get a voltage upper than 2.4V. By the way, the keys' net were supplied by 5V-STB, the 5V is always exist even through in standby mode. A red & blue double LED is used as the TV's indicator light. The LED is red when TV in standby mode and blue in normal mode. The infrared remote sensor was mini type packaged by resin and worked at 5V. The remote code was transmitted by shielded cable to UOCHH's Pin-97(INT0).

4) Headphone power amply part.

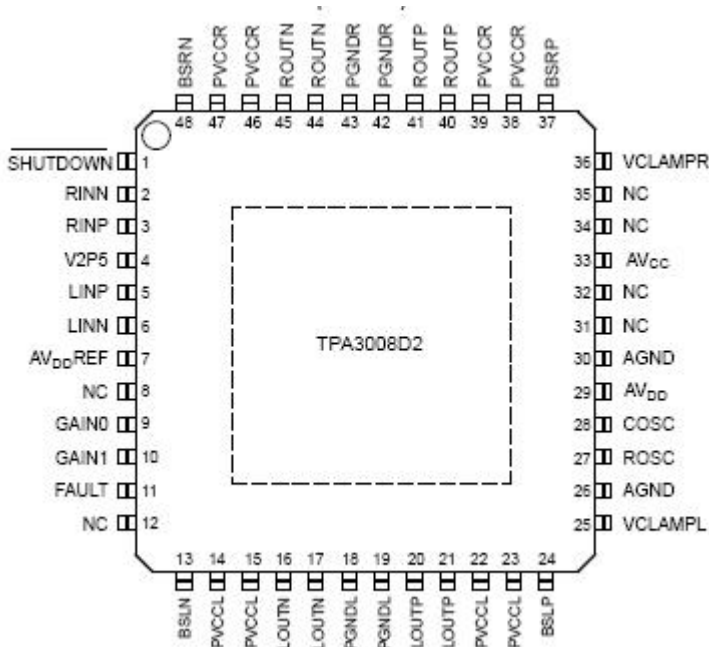
To suit for more headphone's impedance(8Ω~33Ω), the NS's double operational amplifiers LM358 was used as headphone power amply.



One channel of amplify was shown up. It's an AC coupled inverting amplifier, the gain of amplify was select by ratio of R_f/R_1 . The headphone amplify has independence audio source, the audio signals were outputtet by UOCIII's Pin-62(AUDOUTHOL), Pin-63(AUDOUTHOR). For this reason, TV set will not MUTE automatically when the headphone plugged in headphone jack. The headphone has independence volume control in OSD menu too.

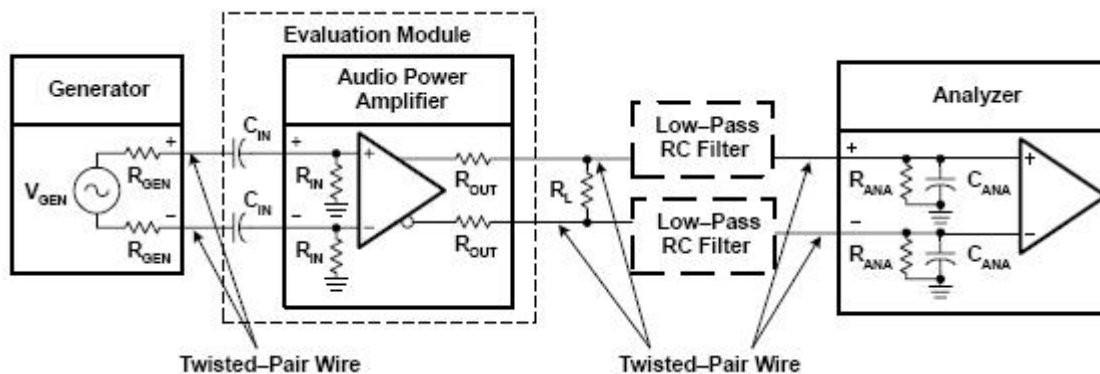
5)The CLASS D main power amplify

To using power supply efficiently, the Class-D amplify was used as the main power amplify. The chip's part number is TPA3008 made by TI. It could output 7W approximately on 8Ω loudspeaker at 12V working voltage. The chip's pins list was not very complex, it was shown as follows:

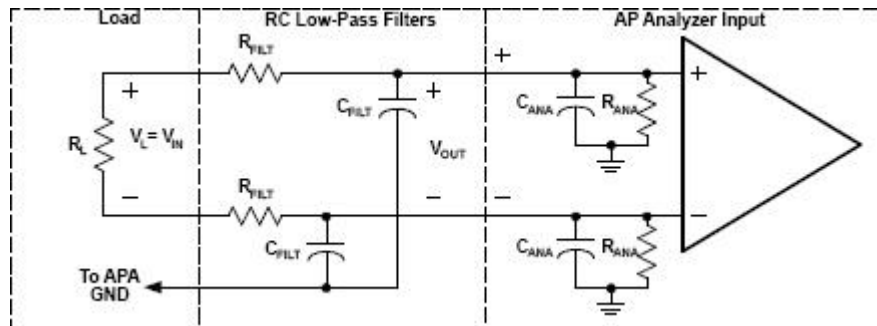


When 12V was supplied on chip at normal working mode. It's meaning chip's power supply OK that a 5V could be test on Pin-7(AVDDREF). For TPA3008's working voltage is 12V, the 5V reference voltage was produced by the circuit net inside the chip. The 5V reference voltage is a symbol flag of 12V power supply state. The Pin-1(SHUTDOWN) is used to shutdown the output of the chip in MUTE mode. At normal mode, the pin's level is HIGH and it's LOW at MUTE mode.

Been a CLASS-D power amplify, the chip output difference signal. A duple input oscilloscope is necessary when you test the waveform on loudspeaker. But the oscilloscope's probes could not connect directly on loudspeaker. A low pass RC filter is need to filter signal and isolating the probes. The test circuit was shown below:



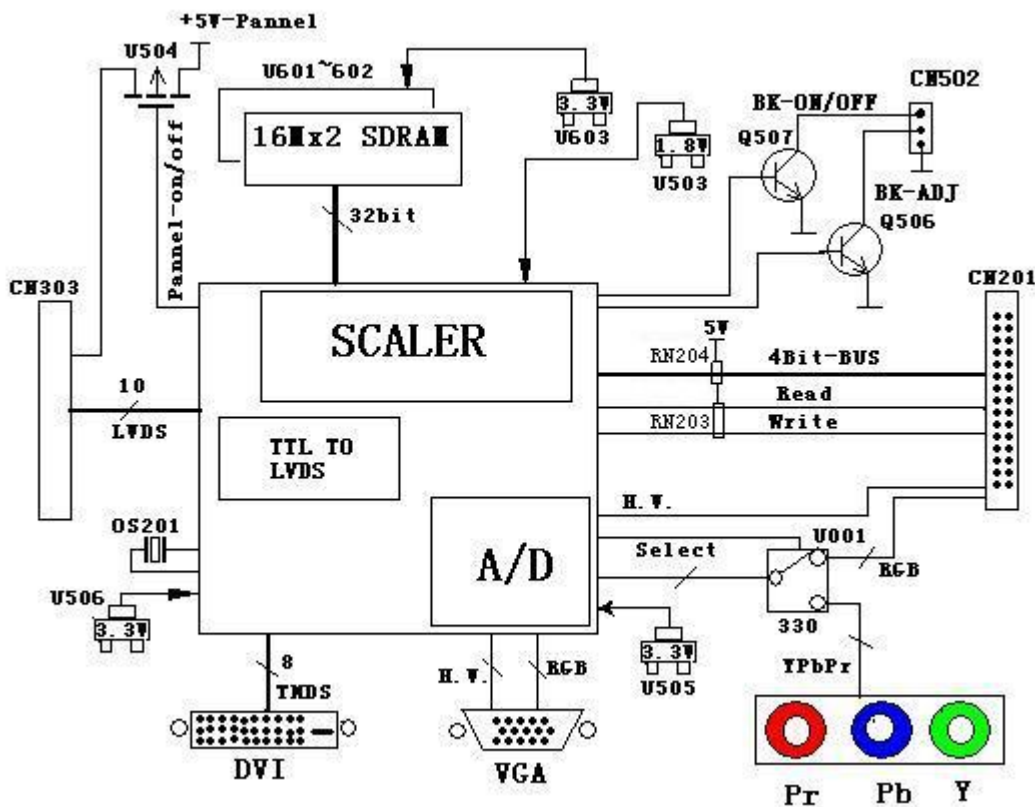
The low pass RC filter's architecture is like as follow:



In normal condition, R-filt and C-filt's type value is list as follows:

MEASUREMENT	R-filt	C-filt
Efficiency	1000Ω	5,600pF
All other measurements	100Ω	56,000pF

Signal Flowing Chart (digital part)



The scale chip MST6151A is the main component on the digital PCB. Many parts were integrated inside the chip, it's include A/D convertor, video signal de-interlace changer, picture scaler, digital video interface (DVI), TTL to LVDS convertor etc. After the RGB signal was processed by UOCIII, the signal was connected to digital PCB through socket CN201. The RGB signal and Y PbPr are both connected to video switch chip FSAV330, and input to the analog port of 6151A after FSAV330 selected. On the other hand, the second analog input port of 6151A connects VGA port; its digital input port connects DVI port for digital difference signal(TMDS). MST6151A communicate with CPU by a special 4Bit bus and was controlled by Read, Witer and ALE signal. there are 2 piece of 16Mbit SDRAM on the PCB, the SDRAMs are used to save digital video data for MST6151A when it's doing scale and de-interlace operation. Finally the processed video signal was converted to LVDS signal which was outputted to socket CN303 and connected to LCD panel through a shielded cable with 5 twisted pairs. The 4 LDO(Low Dropout Voltage Regulator) were used to produce 3.3V and 1.8V DC to supply relative parts.

1) The power supply of digital PCB:

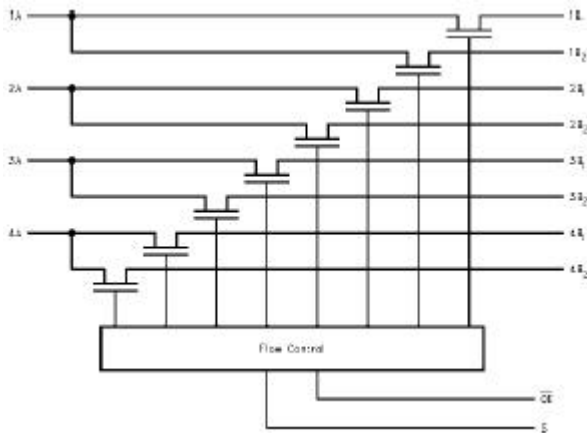
All digital PCB's DC power supply nets were changed from 5V net. For example, different parts of PCB need 3.3V & 1.8V DC were produced by different LDO(Low Dropout Voltage Regulator). U603 was supply 3.3V for SDRAM, U506(3.3V)for MST6151A's PLL (phase lock loop)part, U505(3.3V) for A/D part, U503(1.8V) for chip's core voltage. When the PCB connect 5V, the DC

voltage was exist on each LDO's output pin. There is short cut circuit in the output net if a LDO without output voltage.

By the way, the power of panel's logic circuit was supplied by the net(5V-PANEL) independently. It was controlled by a switch(U504) made by double P-channel MOS named SI9933. Finally the 5V output to CN303 and connect to panel trough wires in shielded cable.

2) The video switch:

FSAV330 is a high speed video switch with max pass band to 300MHz. Been a CMOS chip, FSAV330 is simpler than Bi-polar chip's architecture. The chip's inside was shown below:



On the reason of FSAV330 is a COMS chip, it could be destroyed easily when its input port connect to negative voltage. Pin-1 is the select pin for output. At Y PbPr, DVI, VGA mode Pin-1 should be High-level(about 3.3V), otherwise it is LOW-level.

3) The power supply of MST6151A:

MST6151A is a large scale integration IC which was packaged in 208 PIN-PQFP. It supports a lot of video formats input. The main task of the chip is AD convert analog video and scaling the video suit for LCD panel displaying. The chip has SDRAM interface, so the chip's pins are very dense. Please pay attention to check pins, they should not be connected each other and short cut to GND. MST6151A has 8 serials power supply nets in total, every power supply net has a serial of pins. they are listed as:

Net name	Pin number	voltage	Function explanation
AVDD-ADC	17,34	3.3V	A/D part power supply pins
AVDD-DVI	4,10	3.3V	DVI interface power supply pins
AVDD-MPLL	204	3.3V	Main PLL power supply pins
VDDP	66,162,182	3.3V	Digital Output part power supply pins
VDDM	86,102,113,125,139,154	3.3V	MEMORY interface power supply pins
AVDD-PLL	12	3.3V	A/D PLL power supply pins
AVDD-PLL2	109	3.3V	A/D PLL2 power supply pins
VDDC	63,79,131,156,173,185,195	1.8V	Core power supply
VDDC	49	1.8V	Core power supply after L201 filter

4) The bus of MST6151A:

MST6151A was controlled by a special half byte(4Bit) bus. It need 2 transmission clocks to send a byte data. Adding 4control lines (Read, Write, INT, ALE), the bus is total 8 lines connected between MST6151A and CPU for data communication and logic control. The 8 lines of bus were connected on digital PCB through CN201. Two 33Ω parallel resistors(RN201 & RN202) are linked bus in series and Two 10KΩ parallel resistors(RN203 & RN204) are pull up 5V resistors. When you check the bus, please pay attention on RN201, RN202, RN203, RN204. The impedance of each line between 5V net is 10KΩ. On the reason of tiny space in parallel resistors pins, the system will has failure, once they are connected each other or short cut to GND. The 8 line of MST6151A's bus is:

Pin number	Net name	Pin number	Net name
PIN-72	DATA-0	PIN-68	INT
PIN-73	DATA-1	PIN-69	ALE
PIN-74	DATA-2	PIN-70	READ
PIN-75	DATA-3	PIN-71	WIRTE

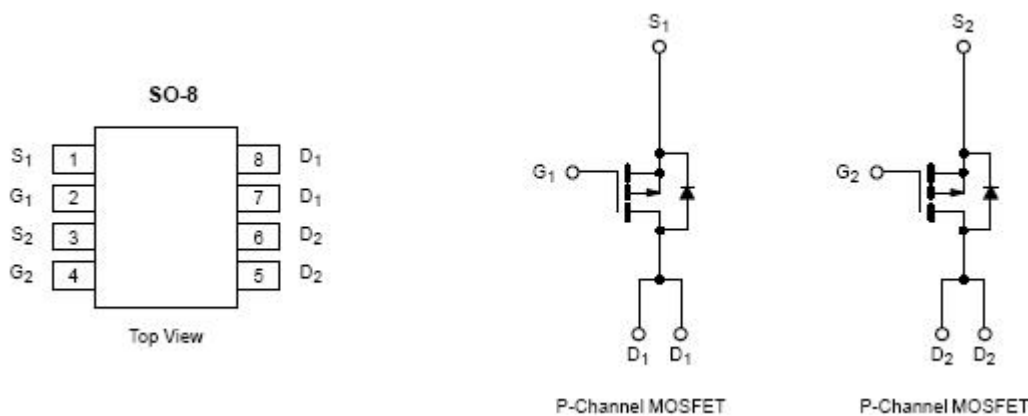
By the way, Pin-67 is REST pin of MST6151A. The pin's level is LOW in normal mode, it will be pull up HIGH several mini seconds to rest the chip in the beginning of AC power on..

5) The logic control signal output by MST6151A:

The CPU not has so many IO ports, and MST6151A has many pins could be used as GPIO(General Programmable IO Port). Many of the system's logic control signals were connect to GPIO pins and controlled by CPU indirectly. There are 5 control signal total:

Pin Number	Net name	Function explanation
PIN-51	BK-ON/OFF	Q507 as a buffer and inverter, to INVERTOR switch(control back light on/off)
PIN-52	V-SELECT	For FSAV330 select pin (RGB or Y PbPr)
PIN-76	HDCP-PLUG	Q101 as a buffer and inverter, to control DVI's HOT-PLUG function
PIN-78	PANEL-ON/OFF	Q507 as a buffer and inverter, to control P-MOS switch of panel's power
PIN-200	BK-ADJ	Q506 as a buffer and inverter, adjust INVERTOR output voltage(control back light brightness)

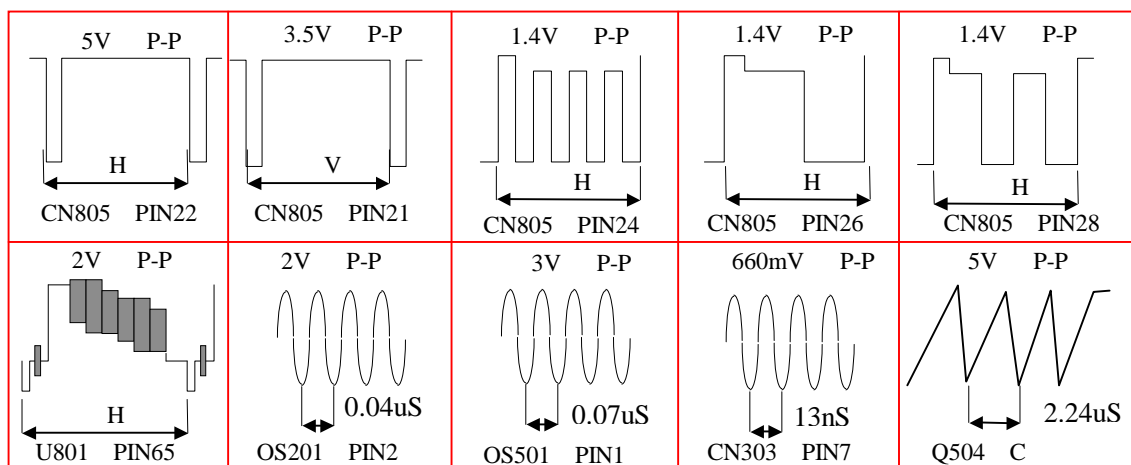
Q507,Q506 were used as the buffer and inverter of MST6151A's GPIO Pin-51, Pin-200. the output signals were connected to panel's inverter through CN502's Pin-1,Pin-2. The 2 logic signal control the panel's back light on/off and brightness. If the panel's lights are not bright, the failures in 2 nets should be checked and fixed first. SI9933 is a double P-MOS packaged as SO-8. the 2 P-MOS were paralleled and used as a large current switch in the PANEL-ON/OFF net. The insight of chip was shown below:



SI9933's Pin-5,6,7,8 will all output 5V when the TV in normal mode. The working condition of all pix on panel was relative on the chip working regular.

appendix:

The waveform of each test point:



For more detailed information about the chips in system, the following documents could be used as references. They are

include:

《The datasheet of SI993 》；

《The datasheet of FSAV330》；

《The specification of TPA3008》；

《The datasheet of LM358》；

all this documents cloud be download form internet.