



# SERVICE MANUAL

HF TRANCEIVER  
**IC-78**

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## INTRODUCTION

This service manual describes the latest service information for the **IC-78 HF TRANSCEIVER** at the time of publication.

**To upgrade quality, all electrical or mechanical parts and internal circuits are subject to change without notice or obligation.**

VERSION NO.	VERSION	SYMBOL
#01	Commercial	OTH
#02	Commercial (w/alarm)	OTH-1
#03	Marine	OTH-2
#04	Marine (w/alarm)	OTH-3

## DANGER

**NEVER** connect the transceiver to an AC outlet or to a DC power supply that uses more than 16 V. This will ruin the transceiver.

**DO NOT** expose the transceiver to rain, snow or any liquids.

**DO NOT** reverse the polarities of the power supply when connecting the transceiver.

**DO NOT** apply an RF signal of more than 20 dBm (100 mW) to the antenna connector. This could damage the transceiver's front end.



## ORDERING PARTS

Be sure to include the following four points when ordering replacement parts:

1. 10-digit order numbers
2. Component part number and name
3. Equipment model name and unit name
4. Quantity required

### <SAMPLE ORDER>

1110004080 S.I.C.  $\mu$ PC2709T IC-78 MAIN UNIT 1 piece  
8810009130 Screw PH B0 M3  $\times$  12 NI-ZU IC-78 CHASSIS 6 pieces

Addresses are provided on the inside back cover for your convenience.

## REPAIR NOTES

1. Make sure a problem is internal before disassembling the transceiver.
2. **DO NOT** open the transceiver until the transceiver is disconnected from its power source.
3. **DO NOT** force any of the variable components. Turn them slowly and smoothly.
4. **DO NOT** short any circuits or electronic parts. An insulated tuning tool **MUST** be used for all adjustments.
5. **DO NOT** keep power ON for a long time when the transceiver is defective.
6. **DO NOT** transmit power into a signal generator or a sweep generator.
7. **ALWAYS** connect a 50 dB or 60 dB attenuator between the transceiver and a deviation meter or spectrum analyser when using such test equipment.
8. **READ** the instructions of test equipment thoroughly before connecting equipment to the transceiver.

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# SECTION 1      SPECIFICATIONS

## ■ GENERAL

- Frequency coverage :  
Receive 0.030–29.999999 MHz<sup>\*1</sup>  
Transmit 1.600–29.999999 MHz<sup>\*2</sup>  
<sup>\*1</sup> Guaranteed range: 0.5–29.999999 MHz  
<sup>\*2</sup> Guaranteed range: 1.600–1.999999 MHz  
3.500–3.999999 MHz  
5.000–7.999999 MHz  
10.000–29.999999 MHz
- Mode : USB, LSB, CW, AM, RTTY (FSK)
- Channel : 100 channel
- Frequency stability : Less than ±200 Hz from 1 min. to 60 min. after power ON. After that rate of stability less than ±30 Hz/hr at +25°C (+77°F). Temperature fluctuations 0°C to 50°C (+32°F to +122°F) less than ± 350 Hz.
- Power supply requirement: 13.8 V DC ±15 % (negative ground)
- Current consumption :

Transmit	max. power	20.0 A
Receive	stand-by	1.3 A
	max. audio	2.0 A
- Usable temp. range : –10°C to +60°C (14°F to 140°F)
- Antenna connector : SO-239 (50 Ω)
- Dimensions : 240 (W) × 95(H) × 239(D) mm  
(projection not included)  
97/16(W) × 33/4(H) × 913/32(D) in
- Weight : 3.8 kg (8 lb 6 oz)
- ACC connector : 13-pin
- REMOTE connector : 2-conductor 3.5(d) mm (1/8")

## ■ RECEIVER

- Receive system : Double-conversion superheterodyne
- Sensitivity (10 dB S/N)  
SSB, CW, RTTY  
AM :  
0.16 µV<sup>\*1</sup> (1.8–29.999999 MHz)  
13 µV (0.5–1.599999 MHz)  
2.0 µV<sup>\*1</sup> (1.6–29.999999 MHz)  
<sup>\*1</sup> Pre-amp 1 ON
- Squelch sensitivity : Less than 5.6 µV (SSB)
- Selectivity :

SSB, CW, RTTY	More than 2.1 kHz/–6 dB
AM	Less than 4.5 kHz/–60 dB
AM	More than 6.0 kHz/–6 dB
AM	Less than 20.0 kHz/–40 dB
- Spurious and image rejection ratio:  
More than 70 dB  
(1.6–29.999999 MHz)
- Audio output power : More than 2.0 W  
(at 13.8 V DC)  
at 10 % distortion with an 8 Ω load
- RIT variable range : ±1200 Hz
- PHONES connector : 3-conductor 6.5(d) mm (1/4")
- EXT SP connector : 2-conductor 3.5(d) mm (1/8") 8 Ω

## ■ TRANSMITTER

- Modulation system :

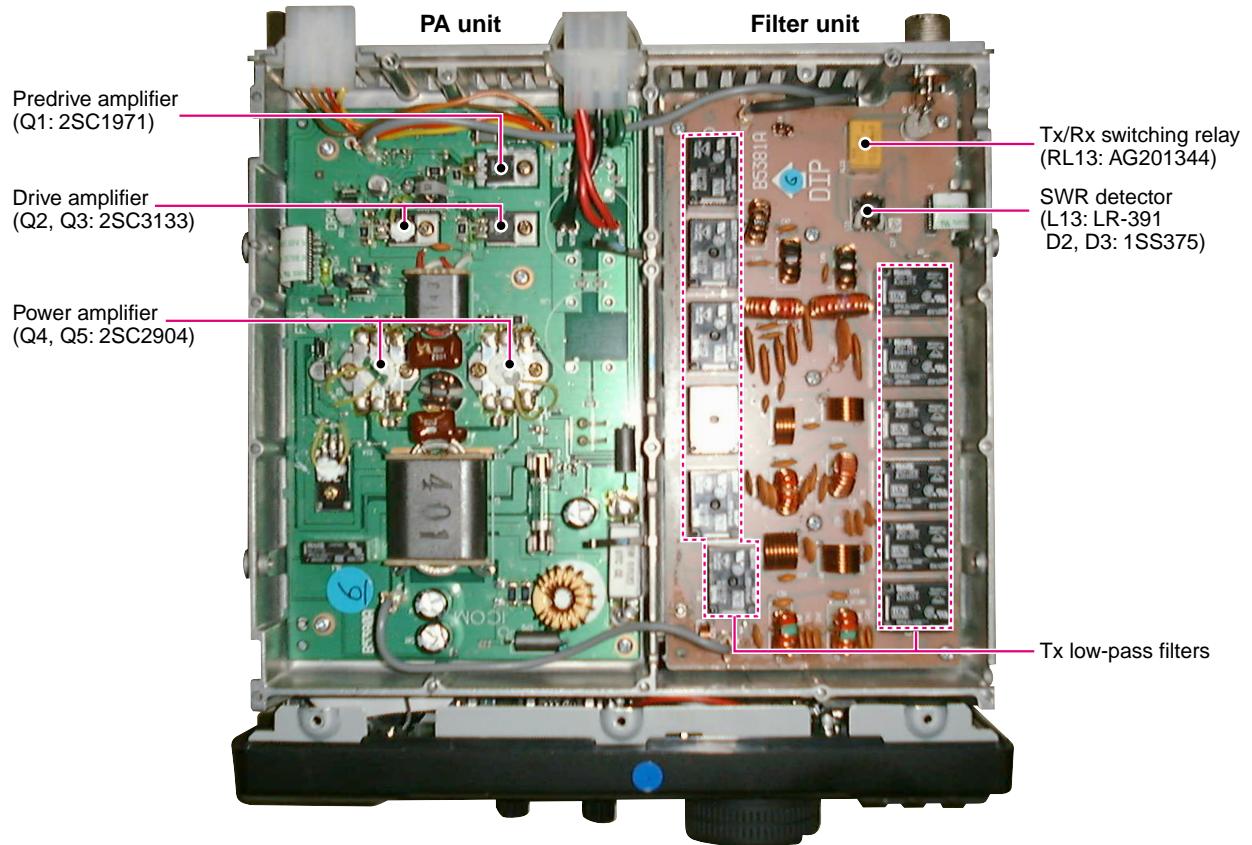
SSB	Balanced modulation
AM	Low level modulation
- Output power :

SSB/CW/RTTY/FM	2–100 W
AM	2–40 W
- Spurious emission : Less than –46 dB below peak output power  
\* spurious frequency ; below 30 MHz: –50 dB,  
above 30 MHz: –60 dB
- Carrier suppression : More than 40 dB
- Unwanted sideband suppression:  
More than 50 dB
- Mic. connector : 8-pin connector (600 Ω)
- KEY connector : 3-conductor 6.5(d) mm (1/4")
- SEND connector : Phono (RCA)
- ALC connector : Phono (RCA)

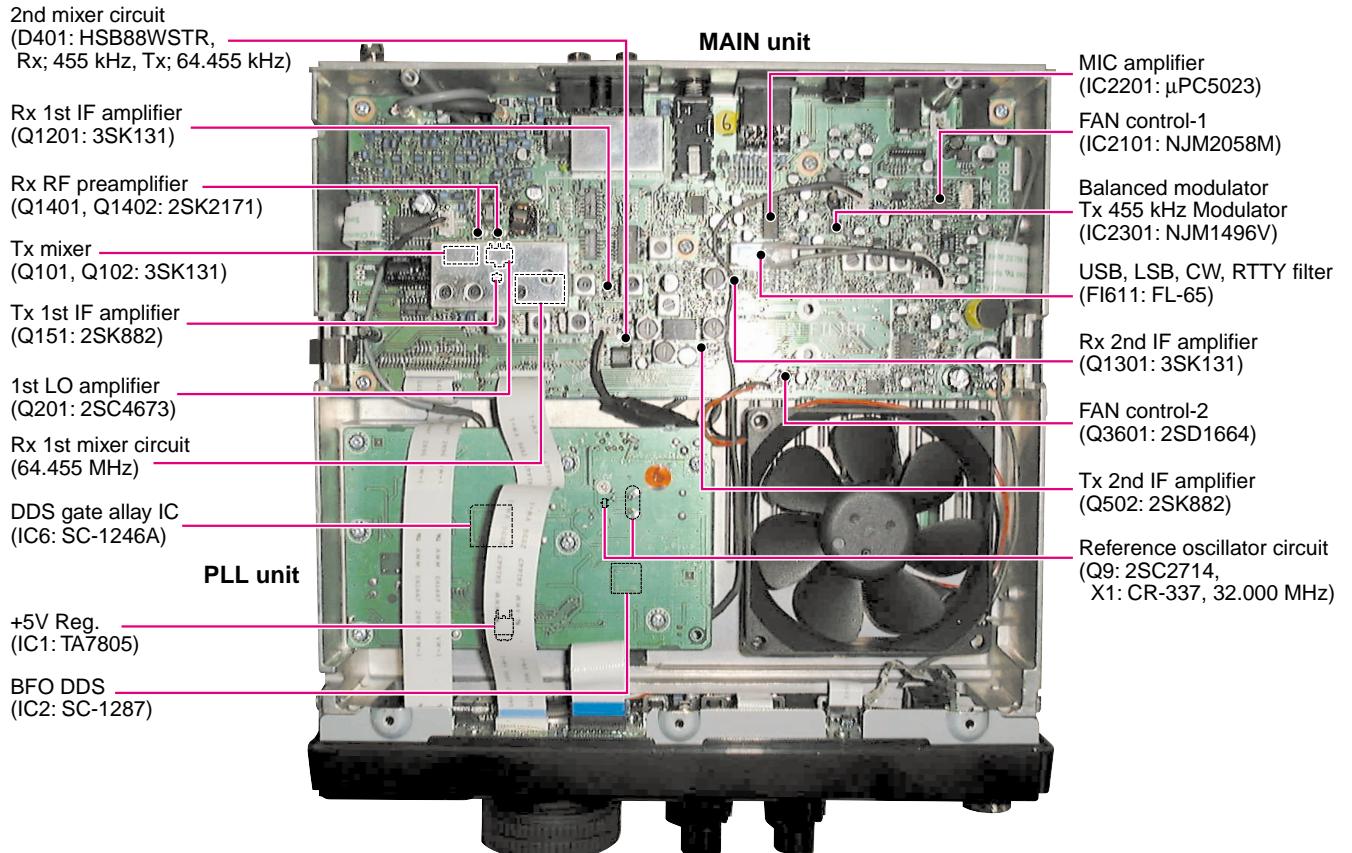
All stated specifications are subject to change without notice or obligation.

## SECTION 2 INSIDE VIEWS

### • Top view (PA AND FILTER UNITS)



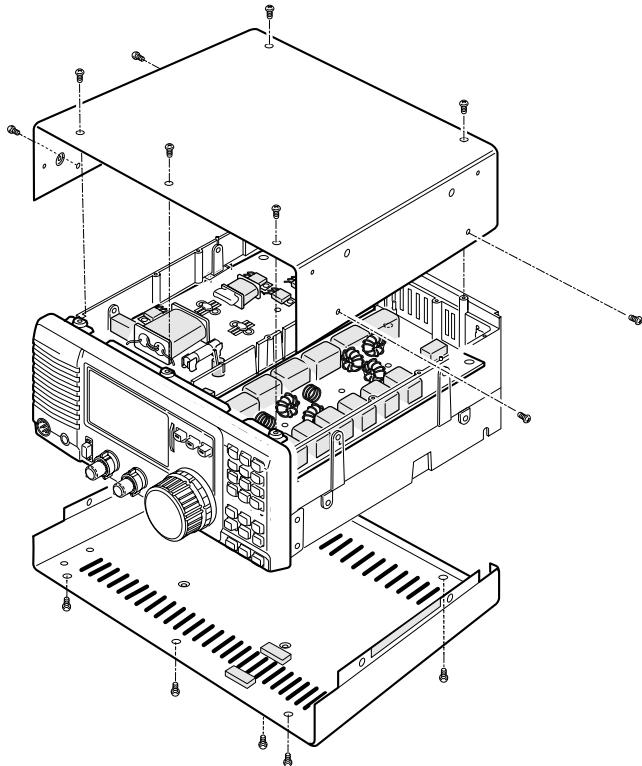
### • Bottom view (MAIN AND PLL UNITS)



## SECTION 3 DISASSEMBLY INSTRUCTIONS

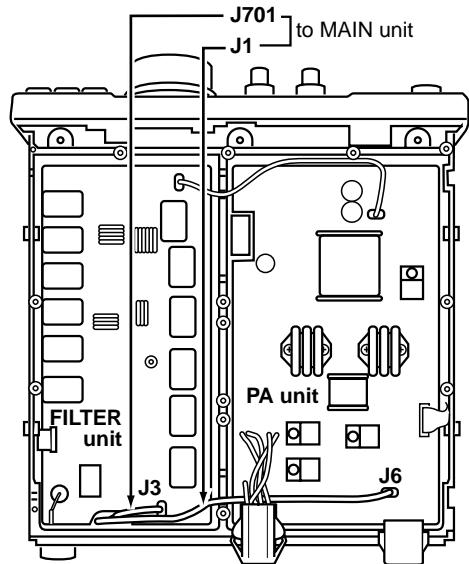
### • Removing the covers

Remove 14 screws from the top and bottom covers.



### • How to connect the coaxial cable

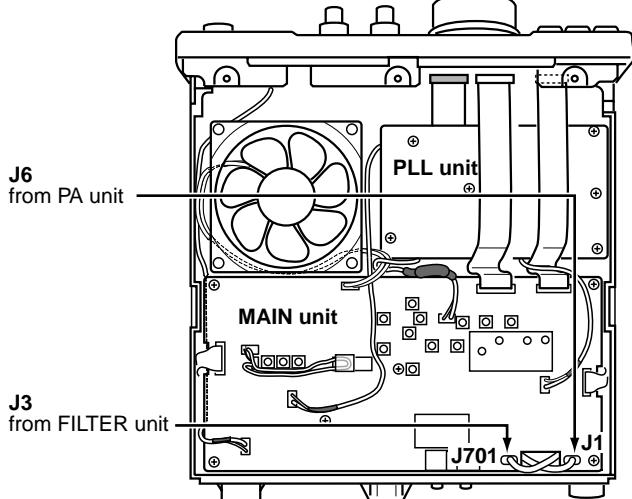
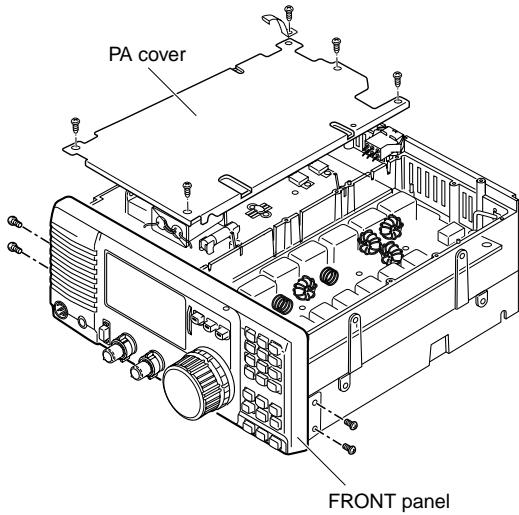
Connect the coaxial cable as shown below.



### • Removing the Front unit and PA cover

Remove 4 screws from the front panel.

Remove 5 screws from the PA cover.



## SECTION 4 CIRCUIT DESCRIPTION

### 4-1 RECEIVER CIRCUITS

#### 4-1-1 RF SWITCHING CIRCUIT (FILTER AND MAIN UNITS)

The RF switching circuit leads receive signals to bandpass filters from the antenna connector while receiving. While transmitting, this circuit leads signals from the RF power amplifier to the antenna connector. This circuit includes a 20 dB RF attenuator circuit to prevent distortion from very strong signals.

RF signals from the antenna connector pass through the transmit/receive switching relay (RL13), and low-pass filter (L14, C14–C16), and are then applied to the MAIN unit via J3 (MAIN unit; J701).

The signals from the FILTER unit are either bypassed or are attenuated at the 20 dB attenuator (D701, R703). The signals are then applied to RF filters.

#### 4-1-2 RF BANDPASS FILTER CIRCUIT (MAIN UNIT)

RF bandpass filters pass only the desired band signals and suppress any undesired band signals.

The RF circuit has 7 RF bandpass filters (BPF) for signals above 1.6 MHz and 1 low-pass filter (LPF) for signals and suppress any undesired band signals.

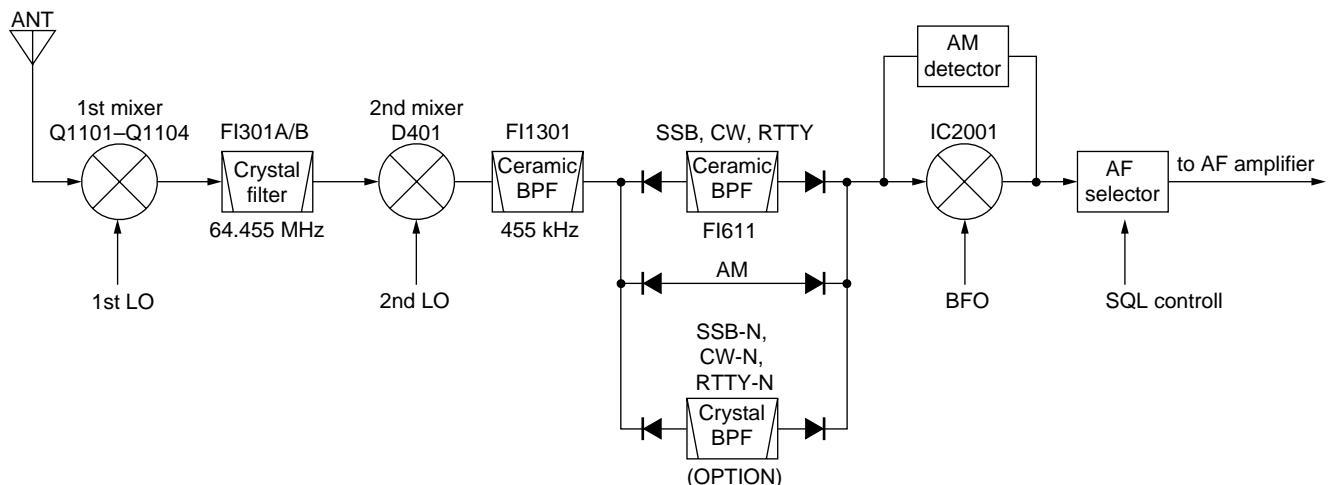
##### (1) 0.03–1.6 MHz

The signals pass through the low-pass filter (L821, L822, C822–C824) to suppress unwanted frequencies. The filtered signals are bypassed a pre-amplifier by a BPF control signal (B0) and preamp control signal (PROF), and are then applied to the 1st mixer circuit (Q1101–Q1104).

##### (2) 1.6–2.0 MHz

The signals pass through a bandpass filter (L831–L833, L835, L836, C831–C834, C837–C840) to suppress unwanted frequencies. The filtered signals are then applied to the pre-amplifier circuit.

#### • RECEIVER CONSTRUCTION



##### (3) 2.0–30.0 MHz

The signals pass through a high pass filter (L811–L814, C811–C817) to suppress excessively strong signals below 2.0 MHz, such as from broadcasting stations. The filtered signals are applied to a low-pass filter or one of 5 bandpass filters depending on their frequencies and are then applied to the pre-amplifier circuit.

##### • Used RF filter

Band	Control signal	Input diode	Band	Control signal	Input diode
0.03–1.6 MHz	B0	D802½	8–11 MHz	B4	D804
1.6–2 MHz	B1	D802½	11–15 MHz	B5	D811
2–4 MHz	B2	D803	15–22 MHz	B6	D805
4–8 MHz	B3	D810	22–30 MHz	B7	D812

#### 4-1-3 PRE-AMPLIFIER CIRCUIT (MAIN UNIT)

The pre-amplifier circuit uses two 2SK2171s to obtain 10 dB of gain over a wideband frequency range. When the preamplifier is turned ON, the signals above 1.6 MHz are applied to the pre-amplifier circuit.

Q1401 and Q1402 are connected in parallel to easily match the impedance to 50 Ω. IC3003 (pins 11, 12) switches the signals from a bandpass filter, either to be bypassed, or to be applied to the pre-amplifier, depending on the [PREAMP] switch condition.

Amplified or bypassed signals are applied to the 1st mixer circuit (Q1102–Q1104)

#### 4-1-4 1ST MIXER CIRCUIT (MAIN UNIT)

The 1st mixer circuit mixes the receive signals with the 1st LO signal to convert the receive signal frequencies into a 64.455 MHz 1st IF signal.

The signals from the pre-amplifier circuit, or signals which bypass the pre-amplifier, pass through a low-pass filter (L902, L903, C904–C907). This low-pass filter suppresses signals above 30 MHz to eliminate direct receiving of signals at 64.455 MHz and image interference at 130–160 MHz. The signals are then applied to the 1st mixer (Q1102–Q1104).

The 1st LO signal (64.485–94.455 MHz) enters the MAIN unit from the PLL unit via J201 (PLL unit; J4). The LO signal is amplified at Q201 and then applied to the 1st mixer.

The 1st mixer (Q1101–Q1104) uses four 2SK1740s to produce high level mixing with a high intercept point.

#### 4-1-5 1ST IF CIRCUIT (MAIN UNIT)

The 1st IF circuit filters and amplifies the 1st IF signals. The 1st IF signals from the 1st mixer circuit are applied to MCF (Monolithic Crystal Filter: FI301) to suppress out-of-band signals. The passband width of FI301 is  $\pm 7.5$  kHz/–6 dB. The filtered signals are applied to the 1st IF amplifier (Q1201). AGC voltage is supplied to the 2nd gate of Q1201.

- Exact 1st IF frequency

Mode	Frequency (MHz)
LSB	64.4535
USB	64.4565
CW	64.4541
AM, CW-N	64.4550

#### 4-1-6 2ND MIXER CIRCUIT (MAIN UNIT)

The 2nd mixer circuit mixes the amplified 1st IF signals and 2nd LO signal (64.00 MHz) to convert the 1st IF signals into a 2nd IF signal.

The amplified 1st IF signals from Q1201 are converted into 455 kHz 2nd IF signal at the 2nd mixer (D401). D401 is a DBM (Double Balanced Mixer). The 2nd LO level is approx. 0 dBm.

The 2nd IF signals are applied to FI1301 to suppress undesired signals such as the 2nd LO signal, and are then applied to the NB circuit.

- Exact 2nd IF frequency

Mode	Frequency (kHz)
LSB	453.5
USB	456.5
CW	454.1
AM, CW-N	455.0

#### 4-1-7 NOISE BLANKER CIRCUIT (MAIN UNIT)

The noise blanker circuit detects pulse type noise, and turns OFF the signal line when noise appears.

The 2nd IF signals from FI1301 are applied to the noise blanker gate (D1301, D1302). A portion of the signals from

FI1301 is amplified at the noise amplifiers (Q1501, Q1502, Q1503), then detected at the noise detector (D1501). The detected signal from the noise detector is applied to the noise blanker control (Q1508, Q1509).

A portion of the detected signals from the noise detector is applied to the noise AGC circuit (Q1504, Q1505, R1514, R1516, C1512) to control the bias voltage of the noise amplifier (Q1501, Q1502).

The threshold level of the noise blanker switch (Q1508) is set at 0.9 V. When the detected voltage exceeds the threshold level, Q1509 outputs a blanking signal to close the noise blanker gate (D1301, D1302), depending on the pulse noise period. When the operating frequency is changed, the "DN" signal line becomes "LOW", turning Q1509 ON through D1503. In this case, the noise blanker gate prevents PLL click noise.

#### 4-1-8 2ND IF CIRCUIT (MAIN UNIT)

The signals passed through the noise blanker gate (D1301, D1302) are amplified at Q1301. AGC voltage is supplied to the 2nd gate of Q1301.

When SSB, CW or RTTY mode is selected, the amplified signals pass through FI611 (FL-65). When an optional CW narrow filter is installed and CW-N mode is selected, the signals pass through the CW narrow filter. When AM mode is selected, the signals bypass the 2nd IF filter.

The filters are selected with mode selecting signals (SSB/CW, AM, CW-N) and the "T8V" voltage line.

The filtered signal is amplified at Q1603–Q1601 to obtain a detectable level. AGC voltage is supplied to the 2nd gate of Q1603. Two thermistors (R1612, R1617), connected to the gate of Q1602, improves the temperature characteristics of the receiver gain. R1614 adjusts the receiver gain.

While in SSB, CW or RTTY mode, output signal from Q1601 is applied to the product detector (IC2001). In AM mode, output signals from Q1601 are shared between the AM detector (D1901) and AGC detector (D1803).

#### 4-1-9 BFO CIRCUIT (PLL UNIT)

BFO (Beat Frequency Oscillator) frequency is used at the SSB/CW detector and the balanced modulator. The IC-78 uses a DDS IC for the BFO circuit.

Output signals from the DDS IC (IC2) are filtered by the low-pass filter (L14, L15, C50–C54), and applied to the product detector (MAIN unit; IC2001) for receive demodulation.

- BFO frequency in each mode

Mode	Frequency (kHz)	
	Receive	Transmit
LSB	453.5	453.5
USB	456.5	456.5
CW	454.1	455.0
CW-N	455.0	455.0
AM	No output	455.0

## 4-1-10 SSB/CW DEMODULATOR CIRCUITS (MAIN UNIT)

In SSB or CW mode, the 2nd IF signal from the IF amplifier (Q1601) is mixed with the BFO signal from the PLL unit at the product detector (IC2001) to demodulate the 2nd IF signal into AF signals. The detected signals (AF) from IC2001 (pin 1) are applied to the AF input mode selector switch (IC2102, pin 7).

## 4-1-11 AM DEMODULATOR CIRCUITS (MAIN UNIT)

In AM mode, the 2nd IF signal from the buffer amplifier (Q1601) passes through C1905 and is detected at D1901. The detected signal (AF) is then applied to the AF input mode selector switch (IC2102, pin 6).

## 4-1-12 AF INPUT MODE SELECTOR SWITCH (MAIN UNIT)

The AF signal from one of the detector circuits is applied to the AF input mode selector switch (IC2102). IC2102 consists of analog switches which are selected with a mode signal and the squelch control signal. The AF signal is output from IC2102 (pin 1) and then applied to the AF amplifier circuit.

## 4-1-13 AGC CIRCUIT (MAIN UNIT)

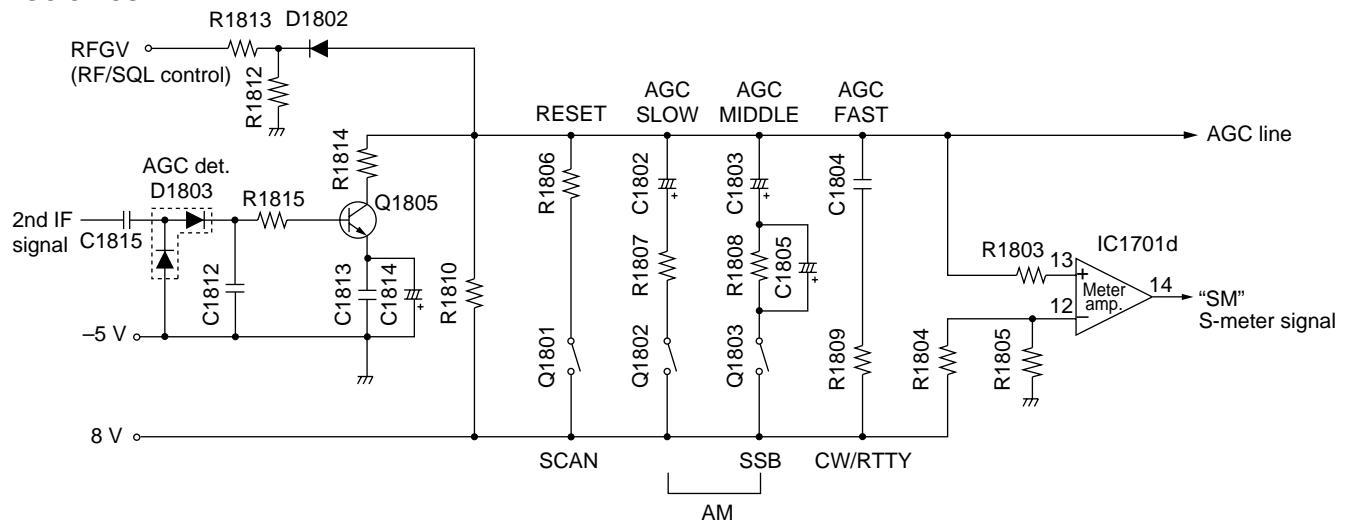
The AGC (Automatic Gain Control) circuit reduces IF amplifier gain to keep the audio output at a constant level.

The voltage on the AGC line (Q1805, collector) determines the receiver gain. The voltage is usually set by D1803 and the resistance ratio of R1812 and R1813.

The 2nd IF signal from the buffer amplifier (Q1601) is detected at the AGC detector (D1803) and is then applied to the DC amplifier (Q1805). -5 V is applied to the Q1805 emitter to activate the AGC line with minus voltage.

When receiving strong signals, the detected voltage increases and the voltage of the AGC line decreases via the DC amplifier (Q1805). As the AGC line is used for the bias voltage of the IF amplifiers (Q1301, Q1201, Q1603), IF amplifier gain is decreased.

### • AGC CIRCUIT



When the strong signal disappears, C1804 and R1809 release the AGC line voltage in CW or RTTY mode to obtain a fast AGC release time. While in SSB or AM mode, C1803, C1805, R1808 and C1802, R1807 are connected in parallel to obtain appropriate AGC characteristics (middle or slow AGC release time), respectively.

## 4-1-14 S-METER CIRCUIT (MAIN UNIT)

The S-meter circuit indicates the relative received signal strength while receiving by utilizing the AGC voltage which changes depending on the received signal strength.

The AGC bias voltage (time constant line) is applied to a differential amplifier (IC1701d, pin 13) where the difference between the bias and reference voltage is detected.

The S-meter signal is applied to the A/D converter section in the CPU (LOGIC unit; IC1, pin 98) and the S/RF indicator displays the relative signal strength.

## 4-1-15 SQUELCH CIRCUIT (MAIN UNIT)

The squelch circuit mutes audio output when the S-meter signal is lower than the [SQL] control setting level.

The S-meter signal from IC1701d (pin 14) is applied to the CPU (LOGIC unit; IC1) to be compared with the threshold level set by the [SQL] control.

When the S-meter signal is lower than the threshold level, the CPU outputs control signal to the AF input mode selector switch (IC2102, pin 5) via the D/A converter (IC3006). This cuts the AF signal OFF. The CPU also controls turning OFF the [RX] indicator, and CPU (pin 43) outputs "SQLS" signal to the [MIC] connector (pin 6) and [ACC] connector (pin 13).

## 4-1-16 AF AMPLIFIER CIRCUIT (MAIN UNIT)

The AF amplifier amplifies the AF input signal to a suitable driving level for the speaker.

The AF signal from the AF input mode selector switch is applied to the AF pre-amplifier (IC2101a). The CW side tone signal is also applied to IC2101a.

The amplified signal is applied to the VCA (IC2701), and then volume controlled AF signal is power-amplified at the AF power amplifier (IC2901) to drive the speaker. The AF signal is applied to the speaker.

## 4-2 TRANSMITTER CIRCUITS

### 4-2-1 MICROPHONE AMPLIFIER CIRCUIT (MAIN UNIT)

The microphone amplifier circuit amplifies microphone-input signals and outputs the amplified signal to the balanced modulator.

Audio signals from the [MIC] connector are applied to the MIC amplifier IC (IC2201). IC2201 consists of the microphone amplifier, microphone gain controller, speech compressor and VOX circuit. External modulation input from the [ACC] socket (pin 11) is also applied to IC2201. The microphone bias voltage is supplied from the 8V line via R2225 and R2201.

In AM mode, the ALC circuit (IC2351b, D2381) limits maximum level of the IC2201 output. The maximum modulation level is set by R2385.

### 4-2-2 BALANCED MODULATOR (MAIN UNIT)

The balanced modulator converts the AF signal from the microphone amplifier into a 455 kHz IF signal with a BFO signal.

Output signals from the microphone amplifier or the CW keying signal are applied to the balanced modulator (IC2301, pin 1). The BFO signal from the PLL unit is applied to IC2301 (pin 10) as a carrier signal.

C2301 is a doubled balanced mixer IC and outputs a double side band (DSB) signal with -40 dB carrier suppression.

R2303 adjusts the balanced level of IC2301 for maximum carrier suppression. In CW mode, the CW keying signal upsets the balance to create a carrier signal. In AM mode, Q2302 and R2321 upset the balance to create an AM carrier signal.

### 4-2-3 CW KEYING CIRCUIT (MAIN UNIT)

When the CW key is closed, control signal is output from CPU (LOGIC unit) and controls break-in operation, the side tone signal.

The input signal (DOT or DAS) from CW keyer is applied to the CPU (LOGIC unit; IC1, pins 71, 70) and then CPU outputs CW control signal (KDS) from pin 77. The CW control signal is applied to the balanced modulator (IC2301) via Q3701, Q3702, D3701 to unbalance the IC2301 input bias voltage and create a carrier signal. R3703 determines the transmit delay timing.

### 4-2-4 IF AMPLIFIER (MAIN UNIT)

The SSB/CW/RTTY 455 kHz IF signal passes through FI611 (FL-65) to suppress unwanted sideband signals, then the signal is applied to a transmit IF amplifier (Q502). The optional CW narrow filter is not used in transmitting.

The amplified signal from Q502 is mixed with the 2nd LO signal and converted to a 64.455 MHz IF signal at D401. D401 is used in receiving and transmitting. The AM signal bypasses FI611, and is amplified at Q502 and is then applied to D401.

The 64.455 MHz IF signal is filtered at FI301, and amplified at the IF amplifier (Q151) and is then converted into the displayed frequency at the balanced mixer (Q101, Q102) with the 1st LO signal.

The gates of the IF amplifiers (Q151, Q502) are controlled by ALC bias voltage from the ALC circuit. A thermistor (R508), connected to the gate of Q502, improves the temperature characteristics of the transmitter gain. R503 adjusts the total transmitter gain.

### 4-2-5 RF CIRCUIT (MAIN AND PA UNITS)

The displayed frequency signal converted at the balanced mixer (MAIN unit; Q101, Q102) is applied to the bandpass filter (L100–L103, C101–C107) where unwanted LO signal emission is reduced. The filtered signal is attenuated at R5–R7 and amplified at IC1, and is then applied to the PA unit via the attenuator (R1–R3).

The signals from the MAIN unit are amplified at the predrive amplifier (Q1), drive amplifier (Q2, Q3) and power amplifier (Q4, Q5) in the PA unit to obtain a stable 100 W of RF output power.

The predrive amplifier is a class-A amplifier with a VCC of 13.8 V. The drive amplifier is a class-AB push-pull amplifier with a VCC of 13.8 V. D1 controls bias voltage to the drive amplifier.

The impedance of the signal from the drive amplifier is converted at L2, and then the signal is applied to the power amplifier (Q4, Q5). The power amplifier is a class-AB push-pull amplifier and amplifies the input signal to 100 W. D2 and D3 control bias voltage to the power amplifier. The signal from the power amplifier is applied to one of the low-pass filters in the FILTER unit.

### 4-2-6 LOW-PASS FILTER CIRCUIT (FILTER UNIT)

The low-pass filter circuit consists of 6 Chebyschev low-pass filters to suppress the higher harmonic components. The signal from the power amplifier (Q4, Q5) is applied to one of the low-pass filters (depending on its frequency). The filter switching voltage from the MAIN unit (J4001) is applied to the FILTER unit via J1.

The filtered signal passes through the SWR detector circuit (L13) and is then applied to the antenna connector.

### 4-2-7 ALC CIRCUIT (MAIN UNIT)

The ALC (Automatic Level Control) circuit controls the gain of IF amplifiers in order for the IC-78 to output a constant RF power set by the [RF PWR] control even when the supplied voltage shifts, etc.

The "FOR" voltage from the FILTER unit is applied to IC1701c (pin 9) in the MAIN unit. The "POCV" voltage from the D/A converter (IC3301, pin 2), determined by the RF power setting, is applied to IC1701c (pin 10) as the reference voltage.

When the "FOR" voltage exceeds the "POCV" voltage, ALC bias voltage from IC1701c (pin 8) controls the IF amplifiers (Q151, Q502). This adjusts the output power to the determined level by the RF power setting until the "FOR" and "POCV" voltages are equalized.

In AM mode, Q1705 turns ON and C1707, C1708 are connected to the "FOR" voltage line to obtain an averaging ALC operation. Q1706 turns ON and the "POCV" voltage is shifted for 40 W AM output power (maximum) through R1730.

An external ALC input from the [ACC] socket or the [ALC] jack is applied to the buffer amplifier (Q1703). External ALC operation is identical to that of the internal ALC.

#### 4-2-8 APC CIRCUIT (MAIN UNIT)

The APC (Automatic Power Control) circuit protects the power amplifiers on the PA unit from high SWR and excessive current.

A reflected wave signal appears and increases on the antenna connector when the antenna is mismatched. D3 of the SWR detector circuit (L13, D2, D3) in the FILTER unit detects the signal and applies it to IC1701b in the MAIN unit as the "REF" signal. When the "REF" signal level increases, IC1701b decreases the ALC line voltage via R1716 to activate the ALC.

For the current APC, the power transistor current is obtained by detecting the voltage ("ICH" and "ICL") which appear at both terminals of a 0.012 Ω resistor (PA unit; R25). The detected voltage is applied to the differential amplifier (IC1701a, pins 2, 3). When the current of the final transistors is more than 22 A, IC1701a controls the ALC line via D1705 to prevent excessive current flow.

#### 4-2-9 TEMPERATURE PROTECTION CIRCUIT (MAIN UNIT)

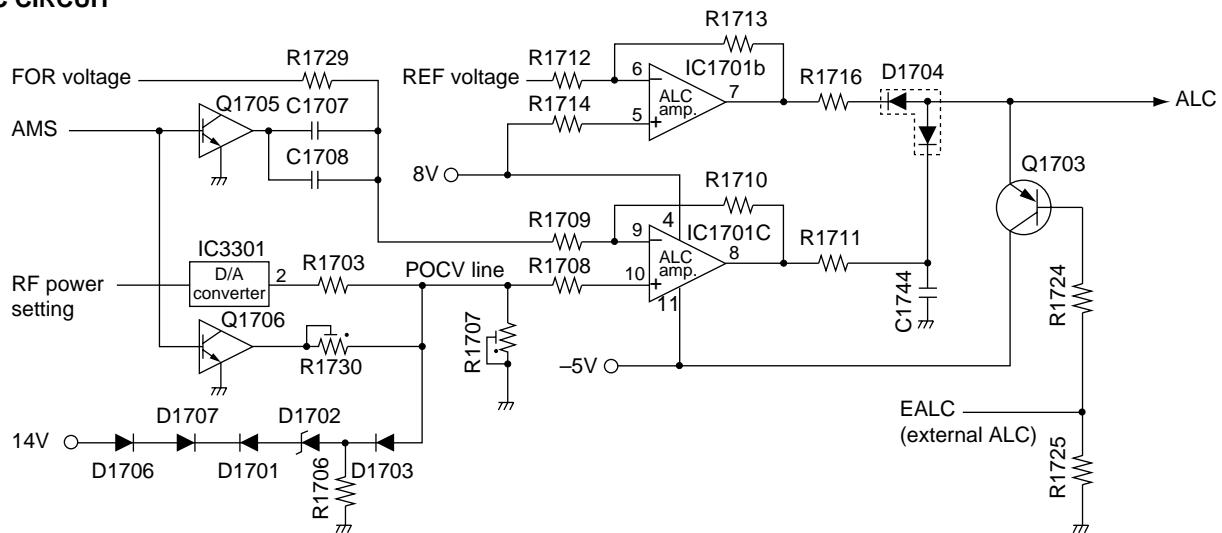
A cooling fan (CHASSIS; MF1) is activated while transmitting or if the temperature of Q4 (PA unit) exceeds the preset value.

While transmitting, PAT8 voltage is provided to MF1 via R30. Thermistor R30 on the PA unit detects the temperature of Q4. If the Q4 temperature is more than 50°C (122°F), R30 becomes very low impedance. Then TEMP signal from PA unit is applied to the A/D converter section of the CPU (IC1, pin 94) in the LOGIC unit as PATL signal. And the CPU outputs control signal to rotate the cooling fan at high speed via the I/O expander (IC3301, pin 8) as FANV signal – even when the transceiver condition has changed from transmit to receive.

#### 4-2-10 RF METER CIRCUIT (MAIN UNIT)

The "FOR" voltage from the FILTER unit is applied to the RF meter amplifier (IC1751a, pin 2) via the ALC amplifier (IC1701c). The amplified voltage is output from pin 1 (IC1751a) and then applied to the A/D converter section of the CPU (IC1, pin 99) in the LOGIC unit.

#### • ALC CIRCUIT



## 4-3 PLL CIRCUITS

### 4-3-1 GENERAL DESCRIPTION

The PLL unit contains 2 DDS circuits for generating a 1st LO signal (64.485–97.455 MHz variable) and a BFO frequency (453.5–456.5 kHz). The 1st LO PLL employs a 1 loop DDS PLL whose reference oscillator is also used as the 2nd LO signal (64.00 MHz fixed). The DDS (Direct Digital Synthesizer) circuit performs signal-sampling, generation of digital sine wave and digital phase detection.

### 4-3-2 1ST LO CIRCUIT (PLL UNIT)

The PLL contain one VCO circuit (Q18, D4) for all HF band coverage within 1 Hz step. The VCO oscillation signal is buffer-amplified at Q26 and is then amplified at Q29, Q32 and Q30. The resulting signal is applied to the DDS IC (IC6).

The DDS IC outputs pulse-type signals. The signals are applied to the loop filter to be converted into DC voltage (lock voltage).

The lock voltage is applied to the varactor diode (D4) in the VCO circuit to change the capacitance of this diode and control the oscillation frequency.

The VCO oscillating signal is then buffer-amplified at the buffer amplifier (Q26), and amplified at the LO amplifier (Q28), and finally applied to the MAIN unit as a 1st LO signal.

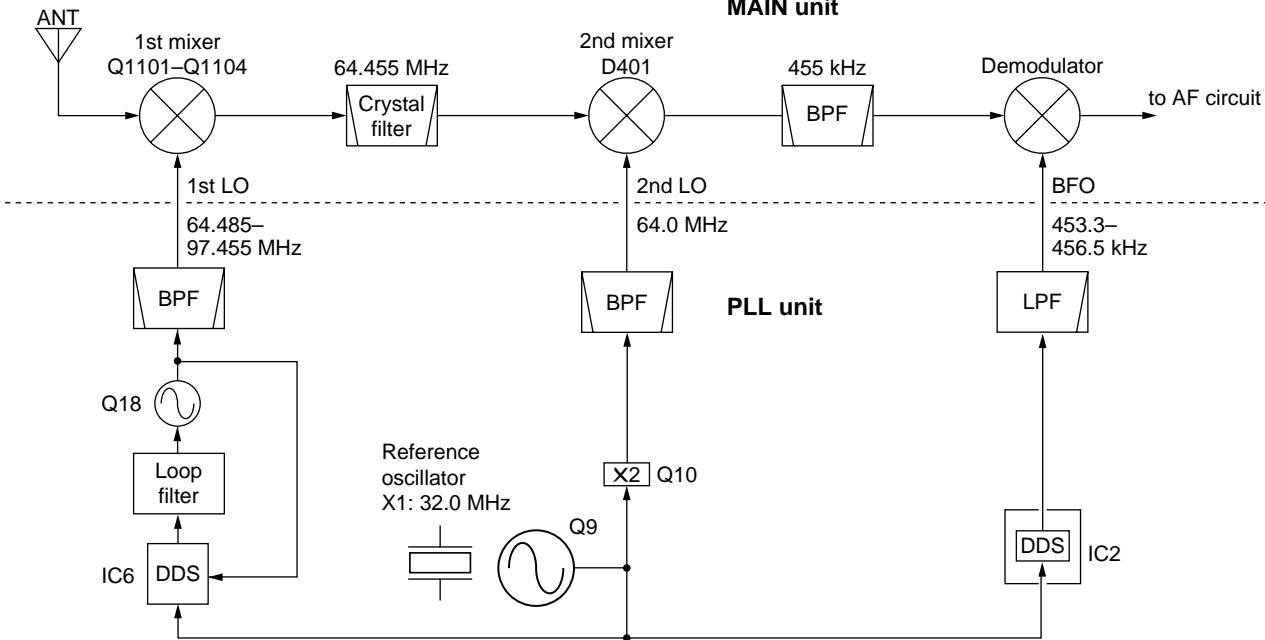
### 4-3-3 REFERENCE OSCILLATOR CIRCUIT

#### (PLL UNIT)

The reference oscillator circuit consists of Q9 and X1. A 32.00 MHz reference frequency is oscillated to produce a 2nd LO signal, DDS reference frequency and BFO DDS clock signal.

The 32.00 MHz reference frequency is doubled at Q10 to obtain the 2nd LO signal. The resulting 64.00 MHz signal is filtered at the bandpass filter and is then applied to the MAIN unit via J1 as the 2nd LO signal.

#### • FREQUENCY CONSTRUCTION



## 4-4 LOGIC CIRCUITS

### 4-4-1 BAND SELECTION DATA (MAIN UNIT)

To select the correct bandpass filter and low-pass filter, the CPU outputs the following band selection data from the I/O expander (MAIN unit; IC3001) depending on the displayed frequency.

The band voltage is produced at the D/A converter (IC3301) and IC2101c.

#### • Band selection data

Band	BPF	Band voltage	LPF
0.03–1.59999 MHz	B0	7.4 V	L1
1.6–1.99999 MHz	B1		
2.0–3.99999 MHz	B2	6.0 V	L2
4.0–7.99999 MHz	B3	5.0 V	L3
8.0–10.99999 MHz	B4	0 V	L4
11.0–14.99999 MHz	B5	4.0 V	
15.0–21.99999 MHz	B6	3.1 V	L5
22.0–30.00000 MHz	B7	2.2 V	L6

### 4-4-2 RIT CONTROL (FRONT UNIT)

The [RIT] control shifts the "RITL" voltage in order to shift the receive frequency. The voltage is applied to the A/D converter section of the CPU (IC1, pin 92). The CPU shifts the N-data for the DDS IC.

#### 4-4-3 CPU (LOGIC UNIT)

The CPU (IC1) contains an 8-bit CMOS CPU, a 60 k-byte ROM, a 2 k-byte RAM. A 9.8304 MHz clock is used for rapid operation. The CPU controls the operating frequency, mode, function display, etc. The memory channel information is stored in the EEPROM (IC2).

The Icom CI-V network system allows the IC-78 to be remotely controlled by a personal computer using an RS-232C I/O port.

#### • PORT ALLOCATIONS (LOGIC unit; IC1)

Pin number	Port name	Description
1	AVXL	Input port for the anti-VOX voltage.
11, 13	SEN1, SEN2	Input port for [MAIN DIAL] up/down signals.
15–17	CON0–CON2	Output control bit signals for the 1st LO DDS circuit (PLL unit; IC6).
18	DRES	Output reset signal for the DDS circuits (PLL unit; IC2, IC6) and D/A converters (MAIN unit; IC3001, IC3004, IC3006), etc.
19	PCK	Outputs serial clock signal for the DDS circuits (PLL unit; IC2, IC6).
21	PDAT	Outputs serial data signals for the DDS circuits (PLL unit; IC2, IC6).
22	DSTB	Outputs strobe signals for the 1st LO DDS circuit (PLL unit; IC6).
23	PSTB	Outputs strobe signals for the BFO DDS circuit (PLL unit; IC2).
24	BSTB	Outputs strobe signals for the D/A converter (MAIN unit; IC3001).
25	FSTB	Outputs strobe signals for the D/A converter (MAIN unit; IC3004).
26	MSTB	Outputs strobe signals for the D/A converter (MAIN unit; IC3006).
41, 42	P55, P56	Output LCD backlight control signals for the dimmer circuit (Q70–Q72).
43	SQLS	Outputs squelch mute control signal, applied to the AF selector switch (MAIN unit; IC2102). High : Squelch opens
52	ALMS	Outputs control signal for the alarm circuit (MAIN unit; Q2201).
54	MCK	Outputs serial clock signal for the I/O expander (MAIN unit; IC3301) and D/A converters (MAIN unit; IC3001, IC3004, IC3006).
55	MDAT	Outputs serial data signals for the I/O expander (IC3301) and D/A converters (IC3001, IC3004, IC3006) on the MAIN unit.
57	STAT	Outputs start signal for the optional antenna tuner.
58	KEY	Input port for transmit control signal from the optional antenna tuner CPU.

#### LOGIC unit; IC1

Pin number	Port name	Description
60	ECS	Outputs chip select signal for EEPROM (IC2).
61	ESI	Input port for serial signal from EEPROM (IC2).
62	ESO	Outputs serial signal to EEPROM (IC2).
63	ESCK	Outputs serial clock signal to EEPROM (IC2)
70	DASK	Input port for [KEY] jack, dash signal. Low : During key down.
71	DOTK	Input port for [KEY] jack, dot signal. Low : During key down.
77	POWS	Outputs switching relay (PA unit; RL1) control signal.
79	BEEP	Outputs beep/CW side tone/alarm audio signals.
80	RXS	Outputs R8V regulator (MAIN unit; IC3005) control signal. Low : While receiving.
81	TXS	Outputs T8V regulator (MAIN unit; IC3005) T13V regulator (MAIN unit; Q3801, Q3802) control signal. Low : While transmitting.
82	PWRK	Input port for the [POWER] switch. Low : While [POWER] is pushed.
85	ASTB	Outputs strobe signals for the I/O expander (MAIN unit; IC3301).
86	P41	Input port for the CI-V control signals.
87	P42	Outputs CI-V control signals.
88	SEND	Input port for connected microphone's PTT switch and SEND signal from the [ACC] jack. Low : While the PTT is pushed or activated from an external unit.
90	AFGL	A/D input port for the [AF] control.
91	RFGL	A/D input port for the [RF/SQL] control.
92	RITL	A/D input port for the [RIT] control.
93	SFTL	A/D input port for the [SHIFT] control.
95	UD	A/D input port for the microphone up/down signal.
96	FORL	A/D input port for the SWR detector circuit (FILTER unit; D2).
97	REFL	A/D input port for the SWR detector circuit (FILTER unit; D3).
98	SML	A/D input port for the S-meter amplifier circuit (MAIN unit; IC1701d).
99	ALML	A/D input port for the ALC meter amplifier circuit (MAIN unit; IC1751a).
100	VOXL	A/D input port for the VOX voltage.

## 4-5 POWER SUPPLY CIRCUITS

### 4-5-1 PA UNIT

LINE	DESCRIPTION
HV	The voltage from an external power supply passed through a fuse (F1).
14 V	The same voltage as the HV line passed through the switching relay (RL1).

### 4-5-2 LOGIC UNIT

LINE	DESCRIPTION
H5V	Common 5 V converted from the HV line and regulated by the H5V regulator circuit (IC5).
5 V	Common 5 V converted from the 14 V line and regulated by the 5V regulator circuit (IC6).

### 4-5-3 MAIN UNIT

LINE	DESCRIPTION
8V	Common 8 V converted from the 14 V line and regulated by the 8V regulator circuit (IC3005).
T8V	8 V for transmitter circuits converted from the 14 V line using TX signal and regulated by the T8V regulator circuit (IC3005).
R8V	8 V for receiver circuits converted from the 14 V line using RX signal and regulated by the R8V regulator circuit (IC3005).
-5V	Common -5 V converted from the 14 V line and converted by the -5V DC-DC converter circuit (IC3501, D3502). The voltage is applied to the AGC (Q1805, D1803), ALC (IC1701) and AF selector (IC2102), etc.
PAT8	8 V for transmitter circuits converted from the 8 V line and regulated by the PAT8 regulator circuit (IC3005).
T13V	13 V for transmitter circuits converted from the 14 V line using TX signal and regulated by the T13V regulator circuit (Q3801, Q3802). The voltage is applied to the TX/RX switching relay (FILTER unit; RL13).
R13V	13 V for receiver circuits converted from the 14 V line using R8V signal and regulated by the R13V regulator circuit (Q1001, Q1002). The voltage is applied to the receive 1st mixer circuit (Q1101–Q1104).

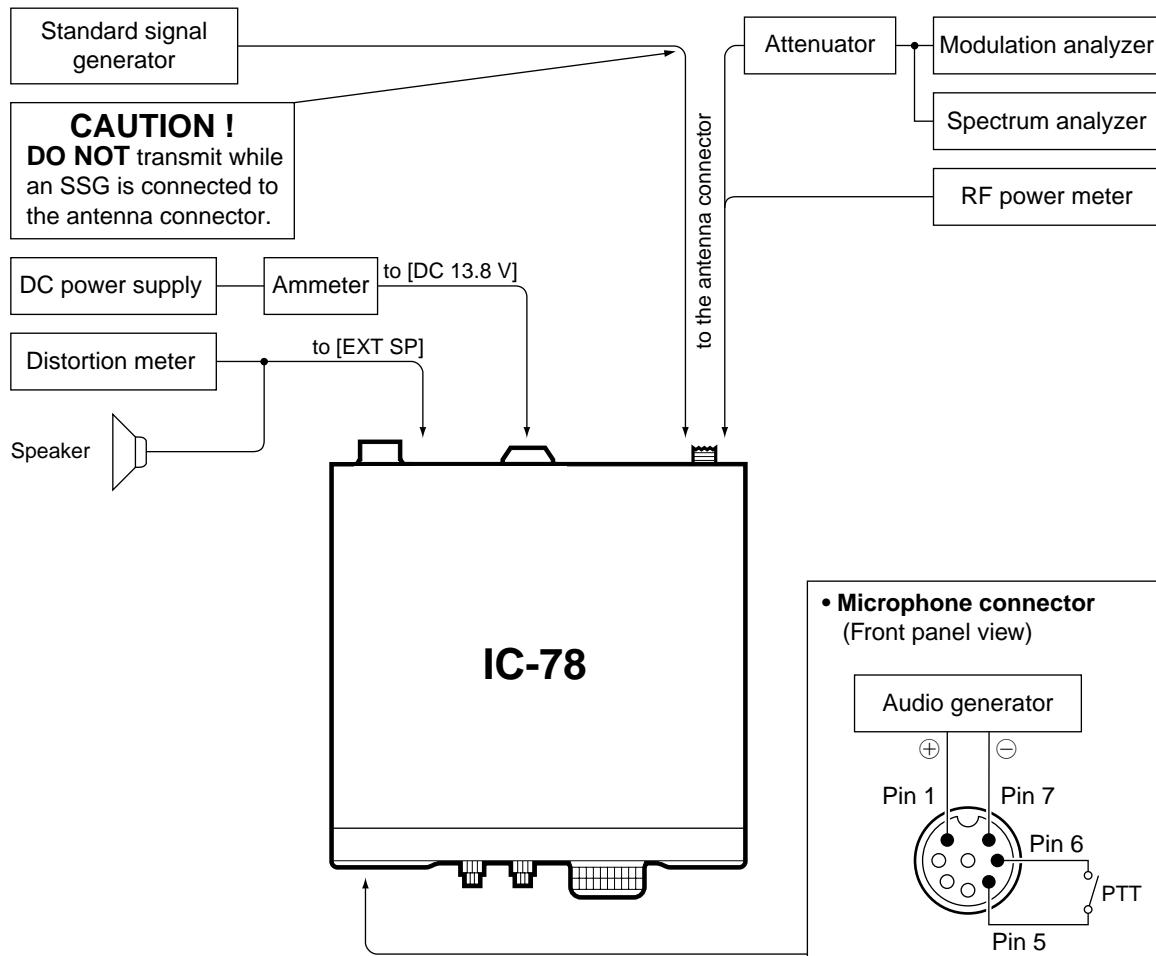
## SECTION 5 ADJUSTMENT PROCEDURES

### 5-1 PREPARATION BEFORE SERVICING

#### ■ REQUIRED TEST EQUIPMENT

EQUIPMENT	GRADE AND RANGE	EQUIPMENT	GRADE AND RENGE
DC power supply	Output voltage : 13.8 V DC Current capacity : 30 A or more	Spectram analyzer	Frequency range : At least 90 MHz Spectraum bandwidth : 100 kHz or more
RF power meter (terminated type)	Measuring range : 10–200 W Frequency range : 1.8–30 MHz Impedance : 50 Ω SWR : Less than 1.2 : 1	Standard signal generator (SSG)	Frequency range : 0.1–100 MHz Output level : 0.1 μV–32 mV (−127 to −17 dBm)
	AC millivoltmeter	Measuring range : 10 mV–10 V	
Frequency counter	Frequency range : 0.1–100 MHz Frequency accuracy : ±0.5 ppm or better Sensitivity : 100 mV or better	DC voltmeter	Input impedance : 50 kΩ/V DC or better
	DC ammeter	Measurement capability: 1 A and 30 A	
	RF voltmeter	Audio generator	Frequency range : 300–3000 Hz Measuring range : 1–500 mV
Modulation analyzer	Frequency range : At least 30 MHz Measuring range : 0–100 %	Attenuator	Power attenuation : 50 or 60 dB Capacity : 150 W or more
Distortion meter	Frequency range : 1 kHz ±10 % Measuring range : 1–100 %	External speaker	Input impedance : 8 Ω Capacity : 5 W or more
Oscilloscope	Frequency range : DC–20 MHz Measuring range : 0.01–10 V	Terminator	Resistance : 50 and 150 Ω Capacity : 150 W or more
Digital multimeter	Imput impedance : 10 MΩ/DC or beter		

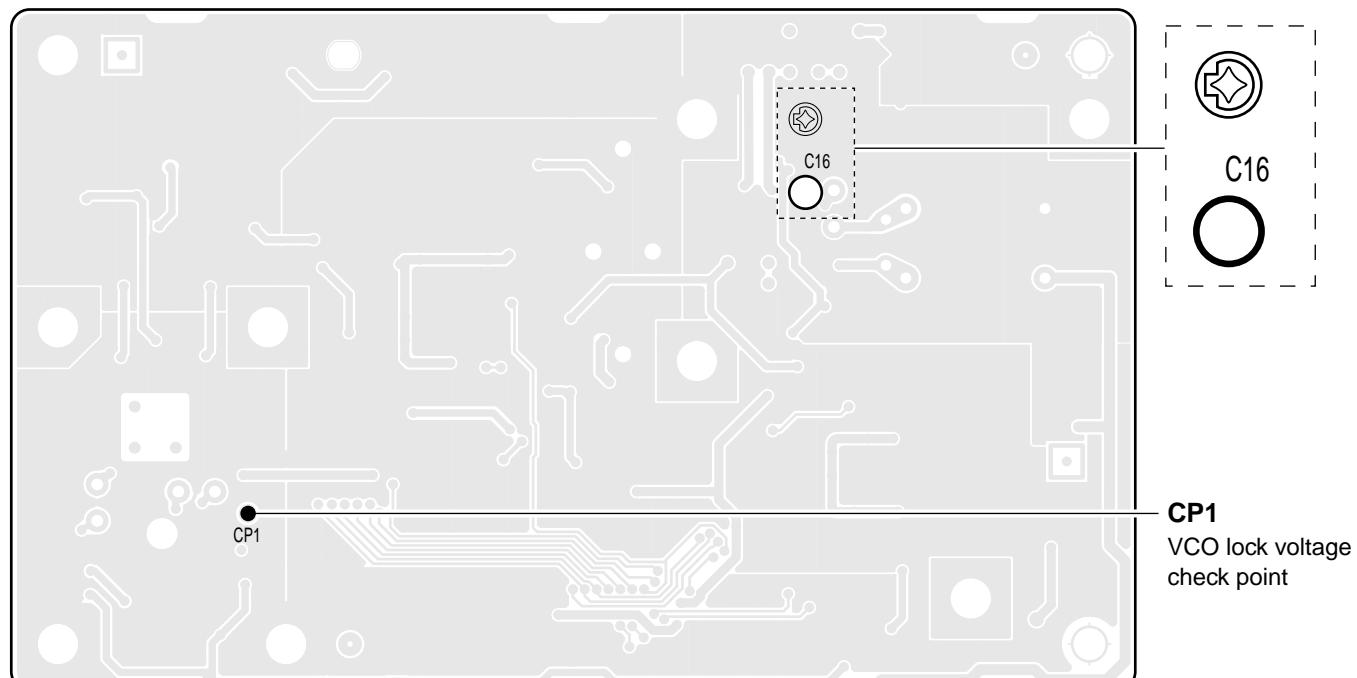
#### ■ CONNECTIONS



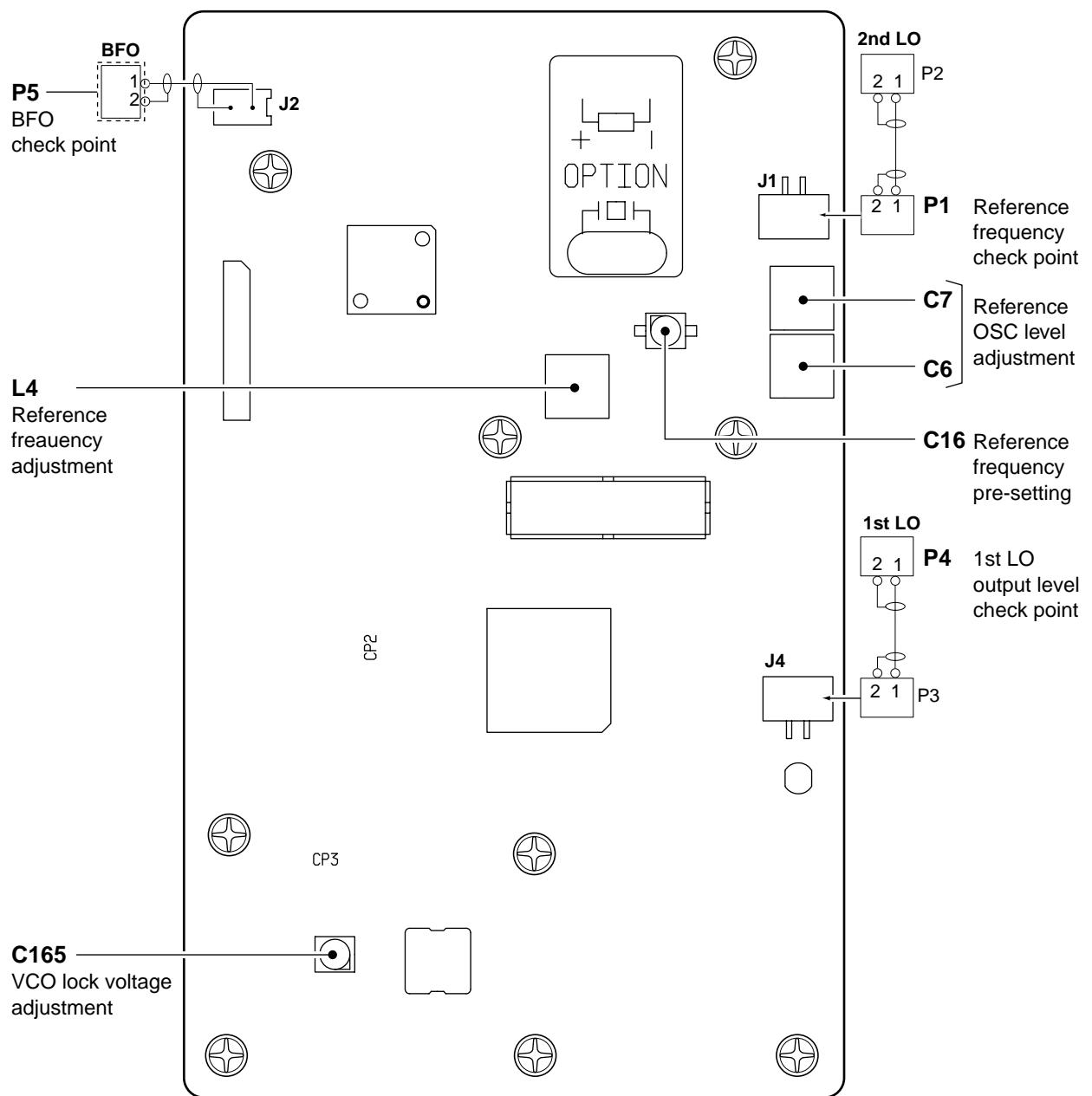
## 5-2 PLL ADJUSTMENTS

ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE	ADJUSTMENT POINT	
		UNIT	LOCATION		UNIT	ADJUST
REFERENCE FREQUENCY	1	<ul style="list-style-type: none"> <li>Display frequency: Any</li> <li>Set C16 as illustration at below.</li> <li>Receiving</li> </ul>	PLL	Connect a frequency counter to check point P1.	Turn L6, L7 on the PLL unit to downside for presetting until the frequency counter reads frequency.	L4
	2			64.00000 MHz		
	3		PLL	Connect an RF voltmeter to check point P1.	Maximum level	L6, L7
VCO LOCK VOLTAGE	1	<ul style="list-style-type: none"> <li>Display frequency: 29.99999 MHz</li> <li>Receiving</li> </ul>	PLL	Connect a digital multimeter or oscilloscope to check point CP1.	4.15 V	C165
	2				More than 0.8 V	
1ST LO OUTPUT LEVEL	1	<ul style="list-style-type: none"> <li>Display frequency: 29.99999 MHz</li> <li>Mode : USB</li> <li>Receiving</li> </ul>	PLL	Connect an RF voltmeter to check point P4.	-3 dBm to +3dBm	Verify
	2					
2ND LO OUTPUT LEVEL	1	<ul style="list-style-type: none"> <li>Display frequency: 14.10000 MHz</li> <li>Mode : USB</li> <li>Receiving</li> </ul>	PLL	Connect an RF voltmeter to check point P1.	-2 dBm to +4 dBm	Verify
BFO OUTPUT	1	<ul style="list-style-type: none"> <li>Display frequency: 14.10000 MHz</li> <li>Mode : USB</li> <li>Receiving</li> </ul>	PLL	Connect an RF voltmeter to check point P5.	-18 dBm to -12 dBm	Verify
	2			Connect a frequency counter to check point P5.	456.5 kHz	
	3				No output	

### • PLL unit (bottom view)



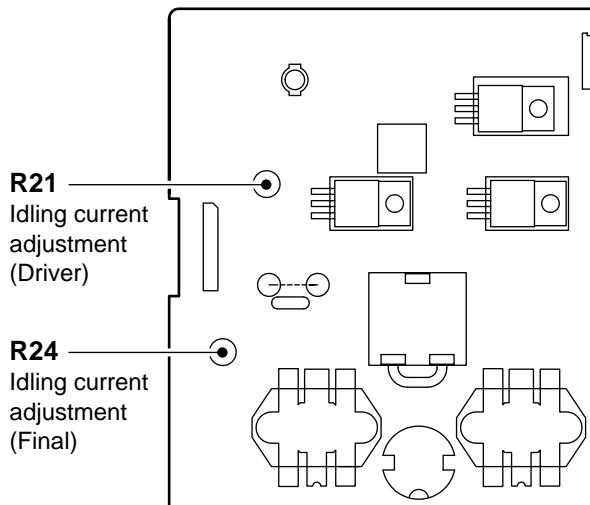
• PLL unit



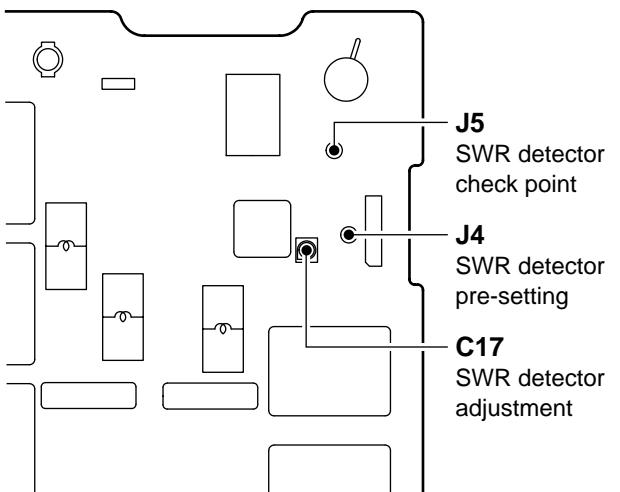
### 5-3 TRANSMITTER ADJUSTMENTS

ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE	ADJUSTMENT POINT	
		UNIT	LOCATION		UNIT	ADJUST
IDLING CURRENT (for driver)	1 • Display frequency: 12.23000 MHz • Mode : USB • RF power : Minimum (L) • Mic gain : Minimum (0) • Disconnect J3601 (MAIN unit) and preset R21, R24 (PA unit) to max. counter clockwise. • Transmitting	PA	Connect an ammeter (3 A) between power supply and the IC-78.	At the point where the Tx current Increases 200 mA.	PA	R21
(for final amplifier)	2 • Transmitting					R24
After adjustment, connect J3601 on the MAIN unit.						
SWR DETECTOR	1 • Display frequency: 12.23000 MHz • Mode : USB • RF power : Maximum (H) • Connect J4 (FILTER) unit to GND. • Connect an audio generator to [MIC] connector and set as: Frequency : 1.5 kHz Level : 30 mVrms • Transmitting	Rear panel	Connect an RF power meter to [ANT] connector.	100 W	Front panel	Mic gain control in the quick set mode
	2 • Transmitting	FILTER	Connect a digital multimeter or oscilloscope to J5.	Minimum voltage	FILTER	C17
	After adjustment, disconnect J4 on the FILTER unit from GND.					
TRANSMITTER TOTAL GAIN	1 • Display frequency: 12.23000 MHz • Mode : USB • RF power : Maximum (H) • Mic gain : Center (50) • R2701 (MAIN unit): Center • Connect an audio generator to [MIC] connector and set as: Frequency : 1.5 kHz Level : 3 mVrms • Transmitting	Rear panel	Connect an RF power meter to [ANT] connector.	Maximum output power	MAIN	L106, L151, L301, L302, L303, L501
	2 • Transmitting			50 W		R503
OUTPUT POWER	1 • Display frequency: 12.23000 MHz • Mode : USB • RF power : Maximum (H) • MIC gain : Center (50) • Connect an audio generator to [MIC] connector and set as: Frequency : 1.5 kHz Level : 30 mVrms • Transmitting	Rear panel	Connect an RF power meter to [ANT] connector.	100 W	MAIN	R1707
Ic APC	1 • Display frequency: 3.55000 MHz • Mode : USB • Connect CP4002 (MAIN unit) to GND. • RF power : Maximum (H) • Mic gain : Center (50) • Connect an audio generator to [MIC] connector and set as: Frequency : 1.5 kHz Level : 30 mVrms • Transmitting	Rear panel	Connect an ammeter (30A) between power supply and the IC-78.	22 A	MAIN	R1720
After adjustment, disconnect CP4002 on the MAIN unit from GND.						

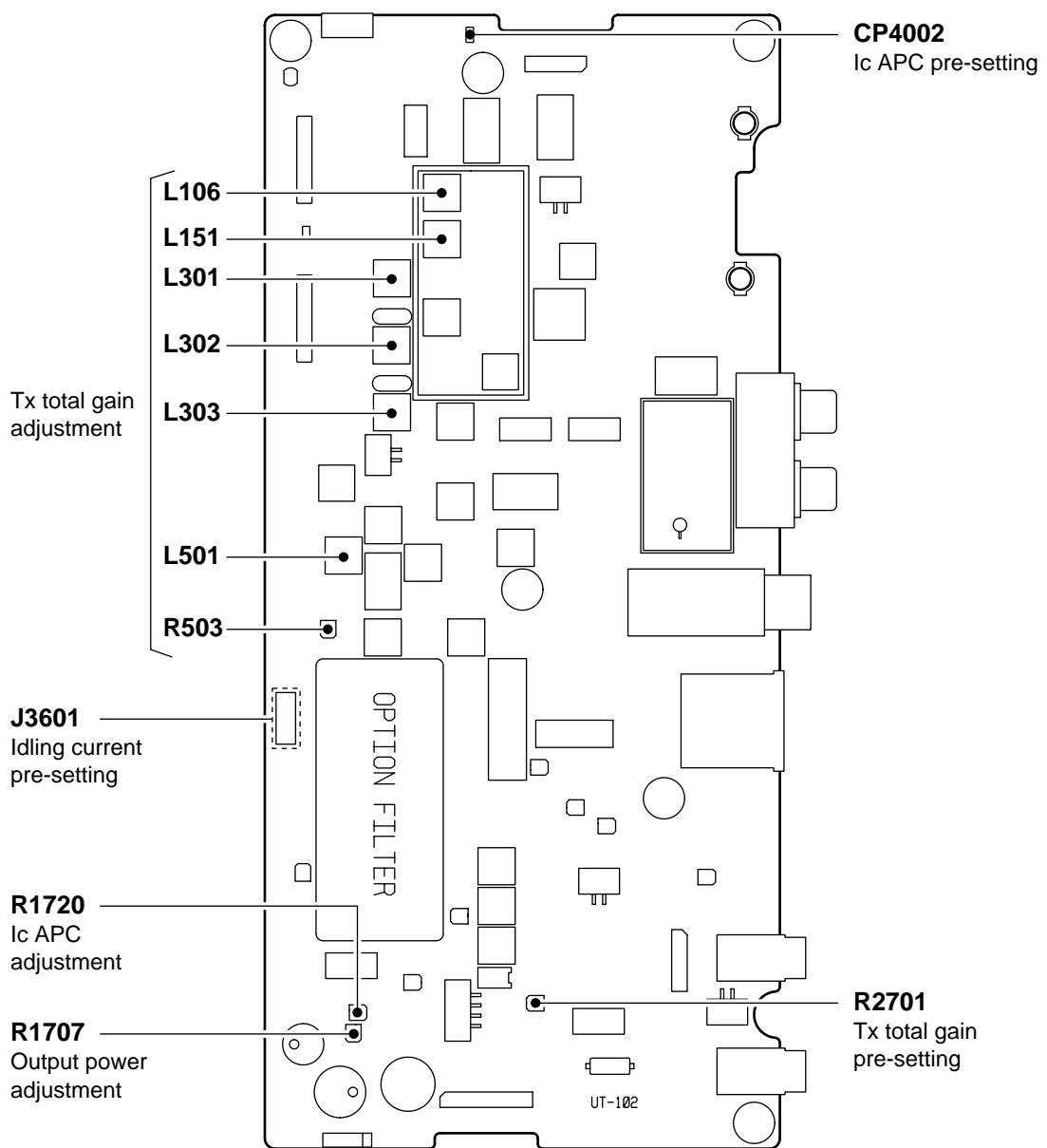
• PA unit



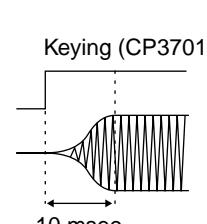
• FILTER unit



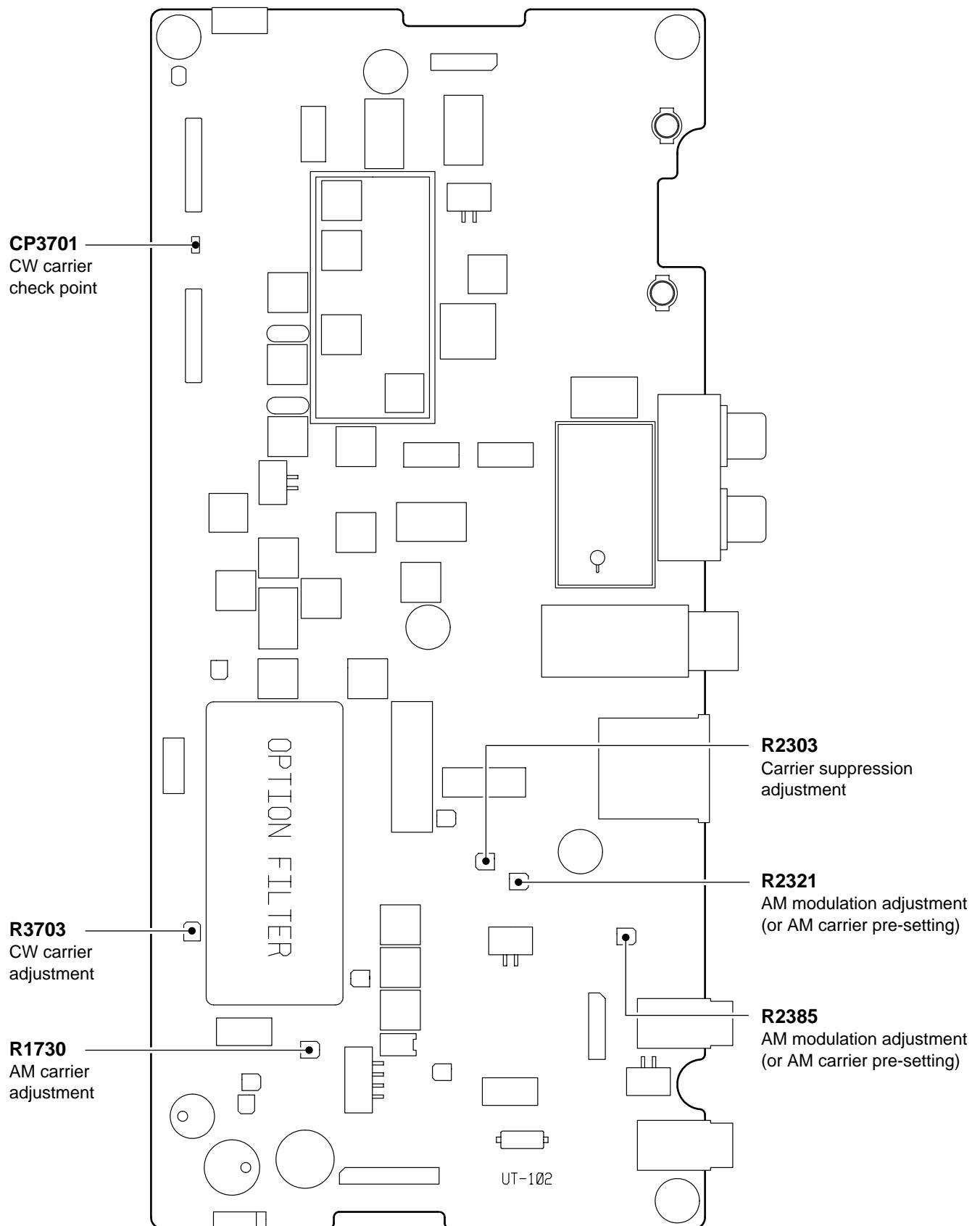
• MAIN unit



## TRANSMITTER ADJUSTMENTS—continued

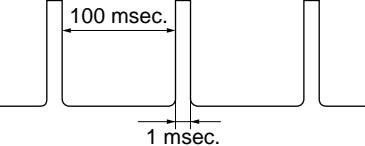
ADJUSTMENT		ADJUSTMENT CONDITION	MEASUREMENT		VALUE	ADJUSTMENT POINT	
			UNIT	LOCATION		UNIT	ADJUST
CARRIER SUPPRESSION	1	<ul style="list-style-type: none"> <li>• Display frequency: 12.23000 MHz</li> <li>• Mode : USB</li> <li>• Mic gain : Minimum (0)</li> <li>• Apply no audio signals to [MIC] connector.</li> <li>• Transmitting</li> </ul>	Rear panel	Connect a spectrum analyzer to the [ANT] connector through an attenuator.	Minimum carrier level	MAIN	R2303
AM CARRIER	1	<ul style="list-style-type: none"> <li>• Display frequency: 12.23000 MHz</li> <li>• Mode : AM</li> <li>• RF power : Maximum (H)</li> <li>• Mic gain : Minimum (0)</li> <li>• R2321 (MAIN unit): Center</li> <li>• R2385 (MAIN unit): Center</li> <li>• Apply no audio signals to [MIC] connector.</li> <li>• Transmitting</li> </ul>	Rear panel	Connect an RF power meter to [ANT] connector.	40 W	MAIN	R1730
AM MODULATION	1	<ul style="list-style-type: none"> <li>• Display frequency: 12.23000 MHz</li> <li>• Mode : AM</li> <li>• RF power : Maximum (H)</li> <li>• Mic gain : Center (50)</li> <li>• R2385 (MAIN unit): 9 o'clock</li> <li>• Connect an audio generator to [MIC] connector and set as:           <ul style="list-style-type: none"> <li>Frequency : 1 kHz</li> <li>Level : 30 mVrms</li> </ul> </li> <li>• Transmitting</li> </ul>	Rear panel	<ul style="list-style-type: none"> <li>• Connect a modulation analyzer to the [ANT] connector through an attenuator.</li> </ul>	70% modulation	MAIN	R2321
	2	<ul style="list-style-type: none"> <li>• Set an AG as:           <ul style="list-style-type: none"> <li>Frequency : 1 kHz</li> <li>Level : 3 mVrms</li> </ul> </li> <li>• Transmitting</li> </ul>			90% modulation		
CW CARRIER	1	<ul style="list-style-type: none"> <li>• Display frequency: 12.23000 MHz</li> <li>• Mode : CW</li> <li>• RF power : Maximum (H)</li> <li>• Connect a keyer to the [KEY] jack.</li> <li>• Key down (transmitting)</li> </ul>	MAIN	Connect an oscilloscope to CP3701 and [ANT] connector.	Adjust as follows: 	MAIN	R3703

• MAIN unit



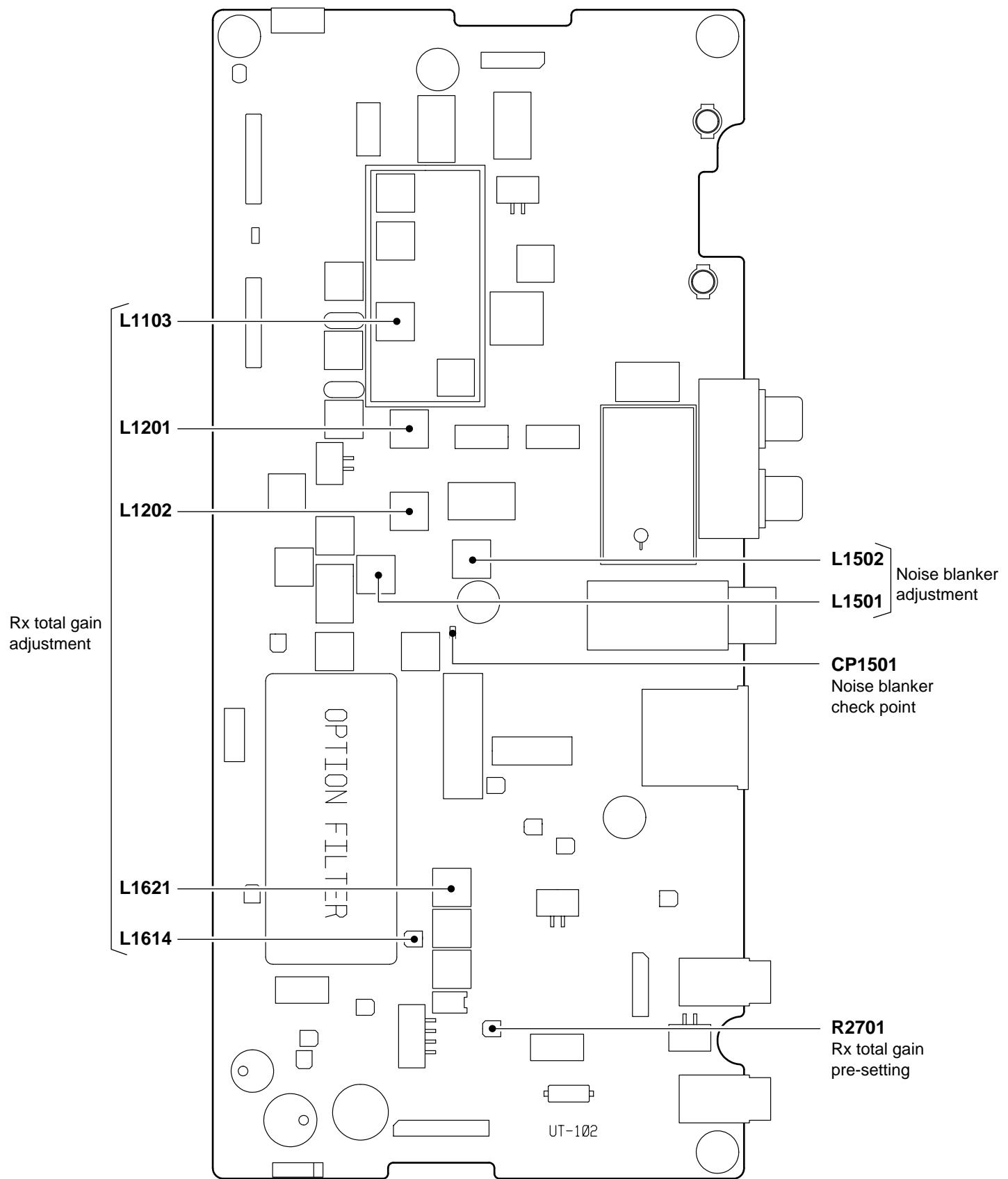
## 5-4 RECEIVER ADJUSTMENTS

Receiver total gain adjustment must perform after transmitter total gain adjustment.

ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE	ADJUSTMENT POINT		
		UNIT	LOCATION		UNIT	ADJUST	
RECEIVER TOTAL GAIN	1	<ul style="list-style-type: none"> <li>• R2701 (MAIN unit): Center</li> <li>• Turn R1614 (MAIN unit) to 90° counter clockwise from center position.</li> <li>• Display frequency: 14.10000 MHz</li> <li>• Mode : USB</li> <li>• [RIT] : OFF (Center)</li> <li>• [NB] : OFF</li> <li>• [P.AMP] : ON</li> <li>• [ATT] : OFF</li> <li>• Connect a standard signal generator to [ANT] connector and set as:           <ul style="list-style-type: none"> <li>Frequency : 14.10150 MHz</li> <li>Level : 1.0 <math>\mu</math>V* (-107 dBm)</li> <li>Modulation: OFF</li> </ul> </li> <li>• Receiving</li> </ul>	Rear panel	<p>Connect an AC millivolt meter to [EXT SP] connector with an 8 <math>\Omega</math> load.</p>	Maximum audio output level	MAIN	Adjust in sequence L1103, L1201, L1202, L1621 several times.
	2						
NOISE BLANKER	1	<ul style="list-style-type: none"> <li>• Display frequency: 14.10000 MHz</li> <li>• Mode : USB</li> <li>• [P.AMP] : ON</li> <li>• [NB] : OFF</li> <li>• Connect an SSG to [ANT] connector and set as:           <ul style="list-style-type: none"> <li>Frequency : 14.10150 MHz</li> <li>Level : 3.2 <math>\mu</math>V* (-97 dBm)</li> <li>Modulation: OFF</li> </ul> </li> <li>and apply following signal to [ANT] connector.</li>  <li>• Receiving</li> </ul>	MAIN	<p>Connect an oscilloscope to check point CP1501.</p>	Maximum noise waveform	MAIN	L1501, L1502
	2						

\*This output level of a standard signal generator (SSG) is indicated as SSG's open circuit.

• MAIN unit



## 5-5 SET MODE ADJUSTMENT

ADJUSTMENT		ADJUSTMENT CONDITION	DISPLAY	OPERATION
ENTERING SET MODE ADJUSTMENT FOR RX	1	<ul style="list-style-type: none"> <li>Enter set mode adjustment for RX:           <ul style="list-style-type: none"> <li>Turn power OFF.</li> <li>Terminate the [REMOTE] jack with a 3.5(d) mm mini-plug.</li> <li>While pushing [MODE] and [TONE] keys, turn power ON.</li> </ul> </li> </ul>	--RX--	<p>Push [SET] key to enter the RX setting. Or push [UP] key to skip the set mode adjustment for RX.</p>
VOLUME CENTER	1	<ul style="list-style-type: none"> <li>Set the [RIT] and [SHIFT] controls to center.</li> </ul>	RIT/SIFT	Push and hold [SET] key to set the volume center positions.
	2		GooD	Verify the display shows "GooD", then push [UP] key to enter the "SMETER" adjustment.
S METER	1	<ul style="list-style-type: none"> <li>Connect a standard signal generator to [ANT] and set as :           <ul style="list-style-type: none"> <li>Frequency : 14.15150 MHz</li> <li>Level : OFF</li> </ul> </li> <li>Receiving</li> </ul>	SO LEVEL	Push [SET] key to set the "S0 level".
	2	<ul style="list-style-type: none"> <li>Set an SSG as :           <ul style="list-style-type: none"> <li>Level : 50 µV (-73 dBm)</li> <li>Modulation : OFF</li> </ul> </li> <li>Receiving</li> </ul>	S9 LEVEL	Push [SET] key to set the "S9 level".
	3	<ul style="list-style-type: none"> <li>Set an SSG as :           <ul style="list-style-type: none"> <li>Level : 50 mV (-13 dBm)</li> <li>Modulation : OFF</li> </ul> </li> <li>Receiving</li> </ul>	+60LEVEL	<p>Push [SET] key to set the "+60 dB level". Push [UP] key to return the set mode adjustment for RX.</p>
SET MODE ADJUSTMENT FOR TX	1	<ul style="list-style-type: none"> <li>Push [UP] to enter the set mode adjustment for TX.</li> </ul>	-- TX --	Push [SET] key to enter the TX setting.
FILTER CALIBRATION	1	<ul style="list-style-type: none"> <li>Connect an RF power meter to [ANT] connector.</li> </ul>	FIL CAL	<p>Push [SET] key to make the calibration. • Transceiver transmits for a while.</p>
POWER METER	1	<ul style="list-style-type: none"> <li>Connect an RF power meter to [ANT] connector.</li> <li>Connect an audio generator to [MIC] jack and set as:           <ul style="list-style-type: none"> <li>Frequency : 1.5 kHz</li> <li>Level : 30 mVrms</li> </ul> </li> </ul>	Po 90W	<p>Push [SET] key to transmit. • Transceiver transmits automatically. Set to 90 W using [MAIN DIAL], then push [SET] key while transmitting.</p>
	2		Po 50W	Set to 50 W using [MAIN DIAL], then push [SET] key while transmitting.
	3		Po 10W	Set to 10 W using [MAIN DIAL], then push [SET] key while transmitting. Push [UP] key to enter the "ALC METER" adjustment.
ALC METER	1	<ul style="list-style-type: none"> <li>Connect an RF power meter to [ANT] connector.</li> <li>Connect an audio generator to [MIC] jack and set as:           <ul style="list-style-type: none"> <li>Frequency : 1.5 kHz</li> <li>Level : 30 mVrms</li> </ul> </li> </ul>	ALC -M SET	<p>Push [SET] key to set ALC reference level. • Transceiver transmits automatically.</p>
			ALC ST-ET	Push [UP] key to enter the "SWR METER" adjustment.

## SET MODE ADJUSTMENT —continued

ADJUSTMENT		ADJUSTMENT CONDITION	DISPLAY	OPERATION
SWR METER	1	• Connect a $50 \Omega$ dummy load or power meter to [ANT] connector.	SWR SET	Transmit using an external PTT switch to set SWR reference level after pushing [SET].
			SWR 1 Ld	
	2	• Connect a $100 \Omega$ dummy load or power meter to [ANT] connector.	SWR 2 Ld	<p>Transmit using an external PTT switch to set SWR2 level after pushing [SET].</p> <p>• The display returns to the same as the set mode adjustment for TX.</p>

# SECTION 6 PARTS LIST

## [FRONT UNIT]

REF NO.	ORDER NO.	DESCRIPTION	
SP1	2510000670	SPEAKER	VS-50-0827
W3	8900008930	CABLE	OPC-885 (P=1 N=10 L=39)
W4	8900008930	CABLE	OPC-885 (P=1 N=10 L=39)
W5	8900006990	CABLE	OPC-683 (N:10 L:110)
WS1	8970023720	E.OTHER	SX2241 ICOM SHIELD (1) /FR
EP2	6450001230	E.OTHER	HLJ0999-01-480

## [LOGIC BOARD]

REF NO.	ORDER NO.	DESCRIPTION	
X1	6050009870	S.XTAL	CR-567 (9.8304 MHz)
L1	6200001830	S.COIL	NL 322522T-100J
L2	6200001830	S.COIL	NL 322522T-100J
L40	6200003260	S.COIL	NL 322522T-101J
L41	6200002040	S.COIL	NL 252018T-101J
L42	6200002040	S.COIL	NL 252018T-101J
L43	6200003950	S.COIL	HF50ACC 322513-T
L44	6200009300	S.COIL	ELJPA 100KF 10U
L47	6200003950	S.COIL	HF50ACC 322513-T
L48	6200003950	S.COIL	HF50ACC 322513-T
L49	6200003950	S.COIL	HF50ACC 322513-T
L100	6200003260	S.COIL	NL 322522T-101J
L101	6200003950	S.COIL	HF50ACC 322513-T
L102	6200003950	S.COIL	HF50ACC 322513-T
L103	6200003950	S.COIL	HF50ACC 322513-T
L104	6200003950	S.COIL	HF50ACC 322513-T
R1	7030003800	S.RESISTOR	ERJ3GEYJ 105 V (1 MΩ)
R2	7030003600	S.RESISTOR	ERJ3GEYJ 223 V (22 kΩ)
R3	7030003560	S.RESISTOR	ERJ3GEYJ 103 V (10 kΩ)
R4	7030003560	S.RESISTOR	ERJ3GEYJ 103 V (10 kΩ)
R5	7030003560	S.RESISTOR	ERJ3GEYJ 103 V (10 kΩ)
R7	7030003600	S.RESISTOR	ERJ3GEYJ 223 V (22 kΩ)
R8	7030003560	S.RESISTOR	ERJ3GEYJ 103 V (10 kΩ)
R9	7030003560	S.RESISTOR	ERJ3GEYJ 103 V (10 kΩ)
R10	7030003680	S.RESISTOR	ERJ3GEYJ 104 V (100 kΩ)
R11	7030003680	S.RESISTOR	ERJ3GEYJ 104 V (100 kΩ)
R12	7030003680	S.RESISTOR	ERJ3GEYJ 104 V (100 kΩ)
R13	7030003680	S.RESISTOR	ERJ3GEYJ 104 V (100 kΩ)
R14	7030003680	S.RESISTOR	ERJ3GEYJ 104 V (100 kΩ)
R15	7030003680	S.RESISTOR	ERJ3GEYJ 104 V (100 kΩ)
R16	7030003680	S.RESISTOR	ERJ3GEYJ 104 V (100 kΩ)
R17	7030003680	S.RESISTOR	ERJ3GEYJ 104 V (100 kΩ)
R18	7030006220	S.RESISTOR	ERJ12YJ470U (47 Ω)
R19	7030007190	S.RESISTOR	ERJ12YJ220U (22 Ω)
R20	7030003640	S.RESISTOR	ERJ3GEYJ 473 V (47 kΩ)
R21	7030003630	S.RESISTOR	ERJ3GEYJ 393 V (39 kΩ)
R22	7030003440	S.RESISTOR	ERJ3GEYJ 102 V (1 kΩ)
R24	7030003640	S.RESISTOR	ERJ3GEYJ 473 V (47 kΩ)
R25	7030003640	S.RESISTOR	ERJ3GEYJ 473 V (47 kΩ)
R26	7030003640	S.RESISTOR	ERJ3GEYJ 473 V (47 kΩ)
R27	7030003640	S.RESISTOR	ERJ3GEYJ 473 V (47 kΩ)
R30	7030003640	S.RESISTOR	ERJ3GEYJ 473 V (47 kΩ)
R31	7030003640	S.RESISTOR	ERJ3GEYJ 473 V (47 kΩ)
R32	7030003640	S.RESISTOR	ERJ3GEYJ 473 V (47 kΩ)
R33	7030003640	S.RESISTOR	ERJ3GEYJ 473 V (47 kΩ)
R34	7030003640	S.RESISTOR	ERJ3GEYJ 473 V (47 kΩ)
R35	7030003640	S.RESISTOR	ERJ3GEYJ 473 V (47 kΩ)
R36	7030003640	S.RESISTOR	ERJ3GEYJ 473 V (47 kΩ)
R37	7030003640	S.RESISTOR	ERJ3GEYJ 473 V (47 kΩ)
R38	7030003640	S.RESISTOR	ERJ3GEYJ 473 V (47 kΩ)
R39	7030003640	S.RESISTOR	ERJ3GEYJ 473 V (47 kΩ)
R40	7030003640	S.RESISTOR	ERJ3GEYJ 473 V (47 kΩ)
R41	7030003640	S.RESISTOR	ERJ3GEYJ 473 V (47 kΩ)
R42	7030003640	S.RESISTOR	ERJ3GEYJ 473 V (47 kΩ)
R43	7030003640	S.RESISTOR	ERJ3GEYJ 473 V (47 kΩ)
R44	7030003200	S.RESISTOR	ERJ3GEYJ 100 V (10 kΩ)
R49	7030003680	S.RESISTOR	ERJ3GEYJ 104 V (100 kΩ)
R54	7030003680	S.RESISTOR	ERJ3GEYJ 104 V (100 kΩ)
R55	7030003640	S.RESISTOR	ERJ3GEYJ 473 V (47 kΩ)
R56	7030003640	S.RESISTOR	ERJ3GEYJ 473 V (47 kΩ)
R59	7030003560	S.RESISTOR	ERJ3GEYJ 103 V (10 kΩ)
R62	7030003480	S.RESISTOR	ERJ3GEYJ 222 V (2.2 kΩ)
R63	7030003480	S.RESISTOR	ERJ3GEYJ 222 V (2.2 kΩ)
R70	7030003370	S.RESISTOR	ERJ3GEYJ 271 V (270 Ω)
R71	7030003410	S.RESISTOR	ERJ3GEYJ 561 V (560 Ω)
R72	7030003430	S.RESISTOR	ERJ3GEYJ 821 V (820 Ω)
R73	7030003510	S.RESISTOR	ERJ3GEYJ 392 V (3.9 kΩ)
R74	7030003440	S.RESISTOR	ERJ3GEYJ 102 V (1 kΩ)
R75	7030009670	S.RESISTOR	ERJ1WYJ390U (39 Ω)
R100	7030003680	S.RESISTOR	ERJ3GEYJ 104 V (100 kΩ)
R101	7030003680	S.RESISTOR	ERJ3GEYJ 104 V (100 kΩ)
R102	7030003680	S.RESISTOR	ERJ3GEYJ 104 V (100 kΩ)

S.=Surface mount

























**[FILTER UNIT]**

REF NO.	ORDER NO.	DESCRIPTION	
C71	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C72	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C73	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C74	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C75	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C76	4030006880	S.CERAMIC	C1608 JB 1H 472K-T-A
C78	4030014460	S.CERAMIC	GRM42-6 CH 820J 500PT
C80	4010005930	CERAMIC	HM11SJ SL 391J 500V
C81	4010005930	CERAMIC	HM11SJ SL 391J 500V
C104	4030014460	S.CERAMIC	GRM42-6 CH 820J 500PT
C107	4030011170	S.CERAMIC	GRM42-6 CH 180J 500PT
C108	4030011550	S.CERAMIC	GRM42-6 CH 680J 500PT
RL1	6330001470	RELAY	AJS1311
RL2	6330001470	RELAY	AJS1311
RL3	6330001470	RELAY	AJS1311
RL4	6330001470	RELAY	AJS1311
RL5	6330001470	RELAY	AJS1311
RL6	6330001470	RELAY	AJS1311
RL7	6330001470	RELAY	AJS1311
RL8	6330001470	RELAY	AJS1311
RL9	6330001470	RELAY	AJS1311
RL10	6330001470	RELAY	AJS1311
RL11	6330001470	RELAY	AJS1311
RL12	6330001470	RELAY	AJS1311
RL13	6330001330	RELAY	AG 201344
J1	6510021980	CONNECTOR	10FMN-BTRK
J2	6510007020	CONNECTOR	TMP-J01X-V6
J3	6510007020	CONNECTOR	TMP-J01X-V6
J4	6910001040	CONNECTOR	IPS-1136
J5	6910001040	CONNECTOR	IPS-1136
W3	6910001030	JUMPER	IPS-1041-4
W4	6910001030	JUMPER	IPS-1041-4
W5	7030008240	S.JUMPER	ERJ12YJ0R00U
W72	7030003860	S.JUMPER	ERJ3GE JPW V
W73	7030003860	S.JUMPER	ERJ3GE JPW V
EP1	0910052046	PCB	B 5381F

**[CHASSIS PARTS]**

REF NO.	ORDER NO.	DESCRIPTION	
J1	6510000370	CONNECTOR	MR-DS
MF1	2710000520	FAN	SB0812H-ICOM-00
W1	8900009501	CABLE	OPC-939A
W2	8900009511	CABLE	OPC-940A
W3	8900009511	CABLE	OPC-940A
W4	8900009521	CABLE	OPC-941A
W5	8900009531	CABLE	OPC-942A
WS1	8970023670	E.OTHER	SX2241 1.5D COAXIAL A (1)/CH
WS2	8970023680	E.OTHER	SX2241 1.5D COAXIAL B (1)/CH
WS3	8970023690	E.OTHER	SX2241 1.5D COAXIAL C (1)/CH
EP1	8930021010	PLUG	DOMED PLUG DP-500
EP2	6910000310	PLATE	B312D INSULATION WASHER
EP3	6910000340	SHEET	P101 KD INSULATION SHEET

S.=Surface mount

## SECTION 7 MECHANICAL PARTS AND DISASSEMBLY

### [FRONT UNIT]

REF NO.	ORDER NO.	DESCRIPTION	QTY.
SP1	2510000670	Speaker VS-50-0827	1
EP2	6450001230	Snap plate HLJ0999-01-480	1
MP1	8210016620	2241 front panel	1
MP2	8930050940	2241 21-key	1
MP3	8930050930	2241 3-key	1
MP4	8930050960	2241 power key	1
MP5	8930050950	2241 lock key	1
MP6	8010018050	2241 sub chassis assembly	1
MP9	8610010420	Knob N261	1
MP10	8610010420	Knob N261	1
MP11	8610010710	Knob N272	1
MP12	8610010710	Knob N272	1
MP15	8610010800	Knob N278	1
MP16	8930050990	2241 plate	1
MP22	8810008660	Screw PH BT M3 × 8 NI-ZU	5
MP23	8810009130	Screw PH BT M3 × 12 NI-ZU	6
MP24	8930049930	Non-woven sheet CC	2
MP25	8930036870	Sponge (DZ)	1

### [CHASSIS PARTS]

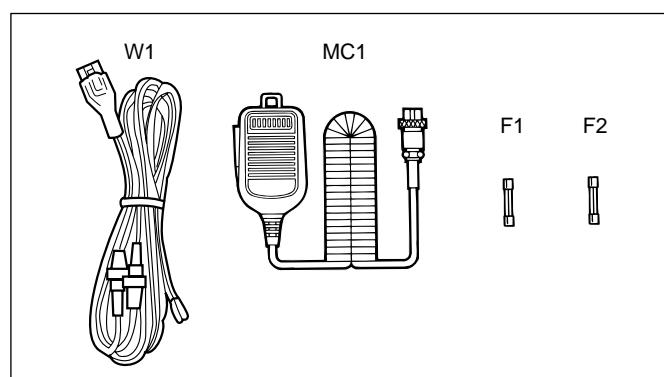
REF NO.	ORDER NO.	DESCRIPTION	QTY.
J1	6510000370	ANT connector MR-DS	1
MF1	2710000520	Fan SB0812H-ICOM-00	1
EP1	8930021010	Domed plug DP-500	1
EP2	6910000310	B312D insulation washer	1
EP3	6910000340	P101 KD insulation sheet	1
MP1	8110007050	Bottom cover 2241 L-cover	1
MP2	8110007060	Top cover 2241 U-cover	1
MP3	8010018020	2241 chassis	1
MP4	8930037001	1691 grounding plate-1	1
MP6	8930002900	Rubber foot (A) SK1912A	2
MP7	8010001520	Stand (C)	1
MP8	8930005790	Color foot (A) for stand	1
MP9	8930005800	Color foot (B) for stand	1
MP10	8930018520	TR clip (A)	1
MP11	8930018520	TR clip (A)	1
MP12	8810009650	Screw FH BT M3 × 8 NI-ZU	4
MP13	8810008660	Screw PH BT M3 × 8 NI-ZU	2
MP14	8810008660	Screw PH BT M3 × 8 NI-ZU	5
MP15	8810008660	Screw PH BT M3 × 8 NI-ZU	7
MP16	8810008660	Screw PH BT M3 × 8 NI-ZU	6
MP17	8810008660	Screw PH BT M3 × 8 NI-ZU	9
MP18	8810008660	Screw PH BT M3 × 8 NI-ZU	4
MP19	8810008660	Screw PH BT M3 × 8 NI-ZU	1
MP20	8810003170	Set screw A M3 × 8	8
MP21	8820000550	Cap bolt M4 × 8 ZK	4
MP22	8810005770	Bind M3 × 8 ZK	14
MP23	8820000530	Frangé bolt M4 × 8 NI	1
MP24	8850000140	Flat washer M4 NI BS	2
MP25	8850000430	Spring washer M4 NI	1
MP26	8930052550	2241 sheet	2
MP28	8810009130	Screw FH BT M3 × 12 NI-ZU	2
MP29	8930052080	2241 grounding spring	2
MP31	8930007120	Non-woven sheet B	2
MP33	8930004070	Grounding spring (C)	1
MP34	8810008660	Screw PH B0 3 × 8 NI-ZU	5
MP35	8510013470	2241 PA cover	1

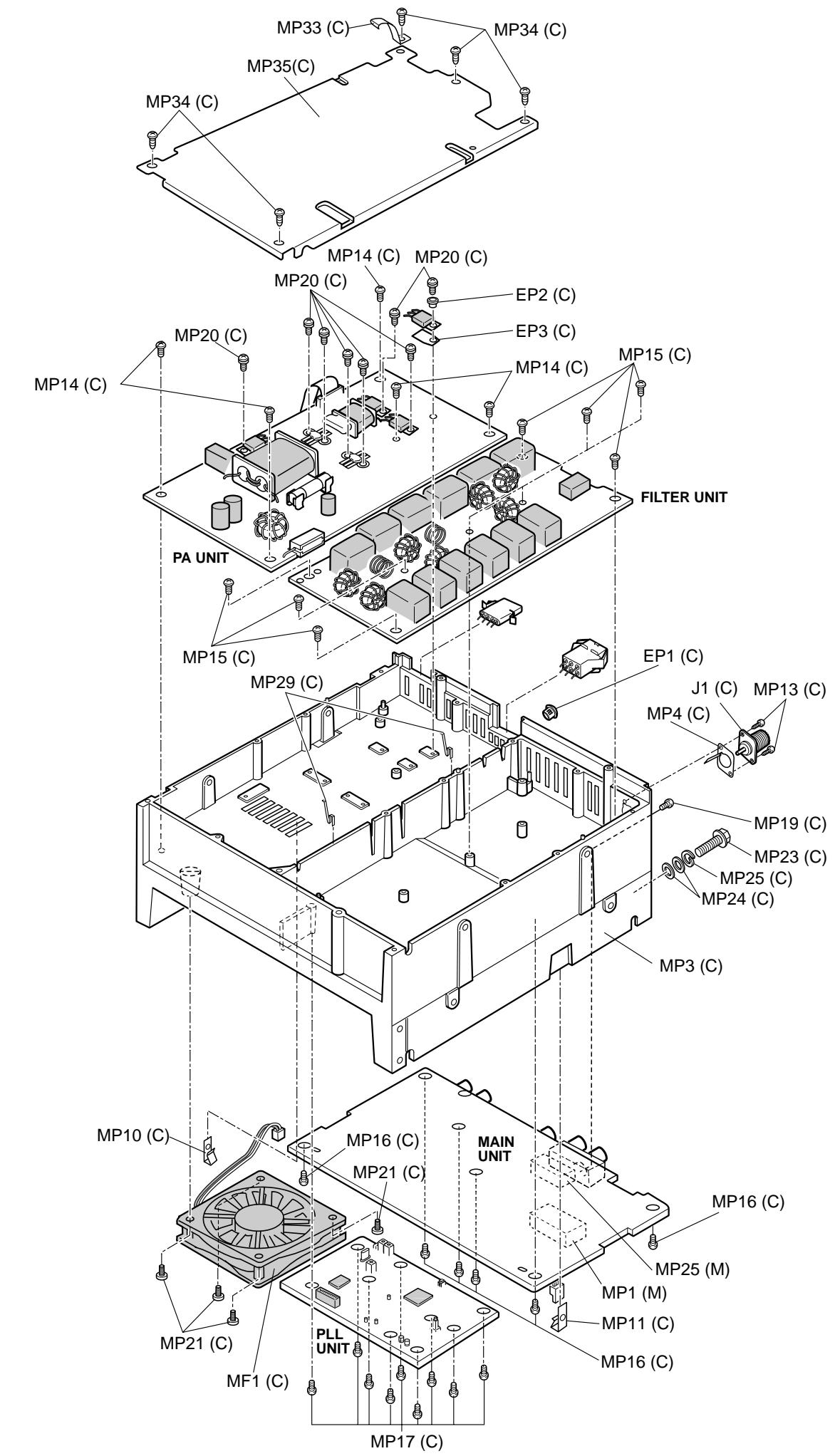
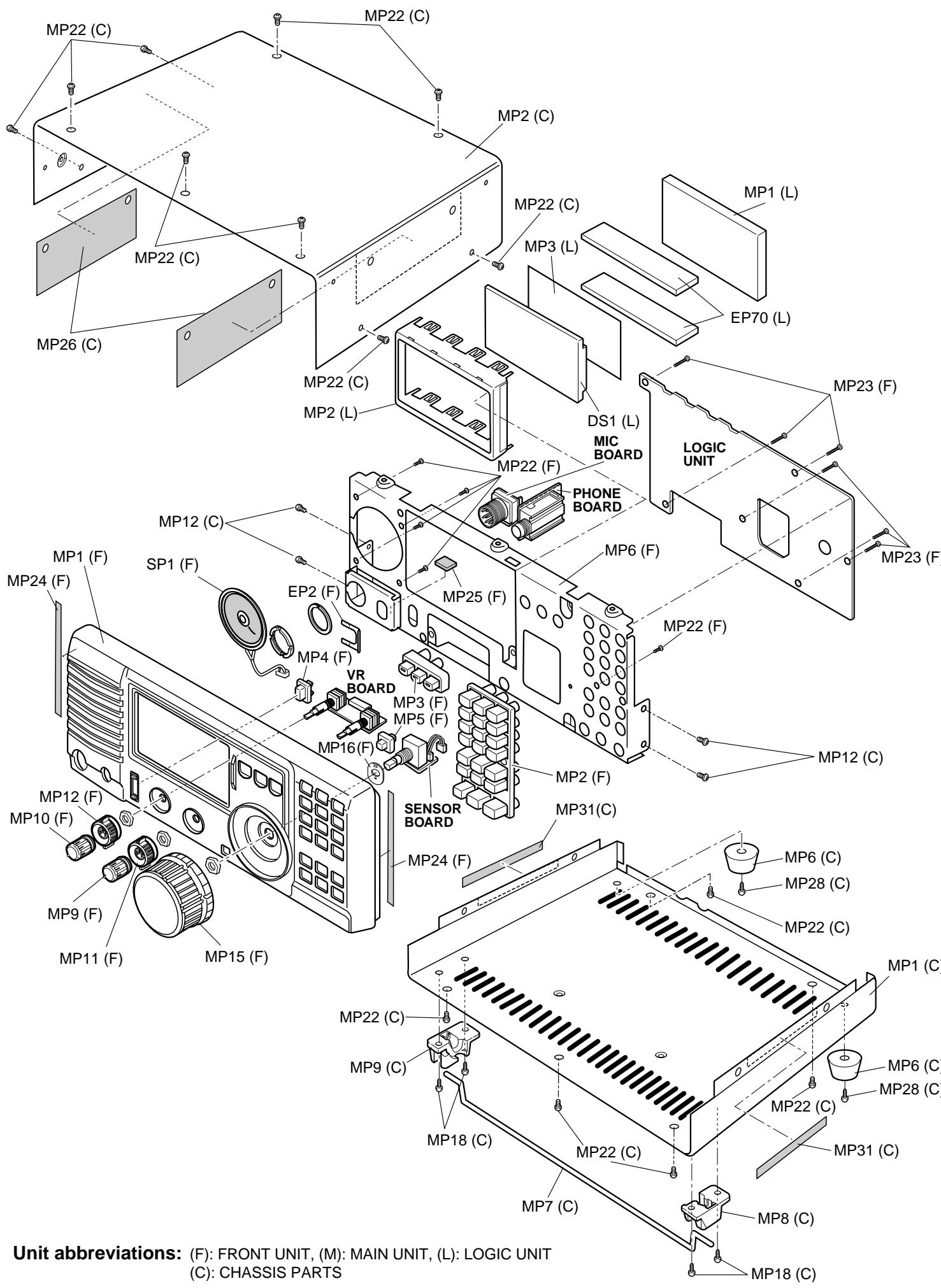
**Screw abbreviations:** PH: Pan head FH: Flat head  
 BT, A0: Self-tapping ZK: Black  
 NI-ZU: Nickel-Zinc

### [LOGIC UNIT]

REF NO.	ORDER NO.	DESCRIPTION	QTY.
DS1	5030001820	LCD A0087	1
EP70	8930051450	LCD contact SRCN-2241-SP-N-W	2
MP1	8210016610	2241 reflector	1
MP2	8930050970	2241 LCD holder	1
MP3	8930051090	2241 LCD filter	1

REF NO.	ORDER NO.	DESCRIPTION	QTY.
F1	5210000080	Fuse FGB 20A	1
F2	5210000130	Fuse FGB 4A	1
W1	Optional product	DC power cable OPC-025 A	1
MC1	Optional product	Microphone HM-36	1





**Unit abbreviations:** (F): FRONT UNIT, (M): MAIN UNIT, (L): LOGIC UNIT  
(C): CHASSIS PARTS

## SECTION 8 SEMI-CONDUCTOR INFORMATIONS

### 8-1 TRANSISTORS

NAME	SYMBOL	INSIDE VIEW
2SA1576A R	FR	
2SC1971 2SC3133	None None	
2SC2714-O 2SC4081 R	QO BR	
2SC2904	None	
2SC4673D-TD	CO	
2SD1585K	None	
2SD1619-T-TD 2SD1664 T100Q	DB DA	
2SK508 2SK1740-TA	K52 IJ	

NAME	SYMBOL	INSIDE VIEW
2SK882-GR	TG	
2SK2171-4	KM	
3SK131-T2 MAS	V11	
DTA114EE TL DTA114EUA T106	14 16	
DTC114EE TL DTC114EUA UN9211 (TX)	24 24 8A	
UMD6N TR	D6	
XP4311 (TX)	7X	
XP4601 (TX)	5C	

### 8-2 DIODES

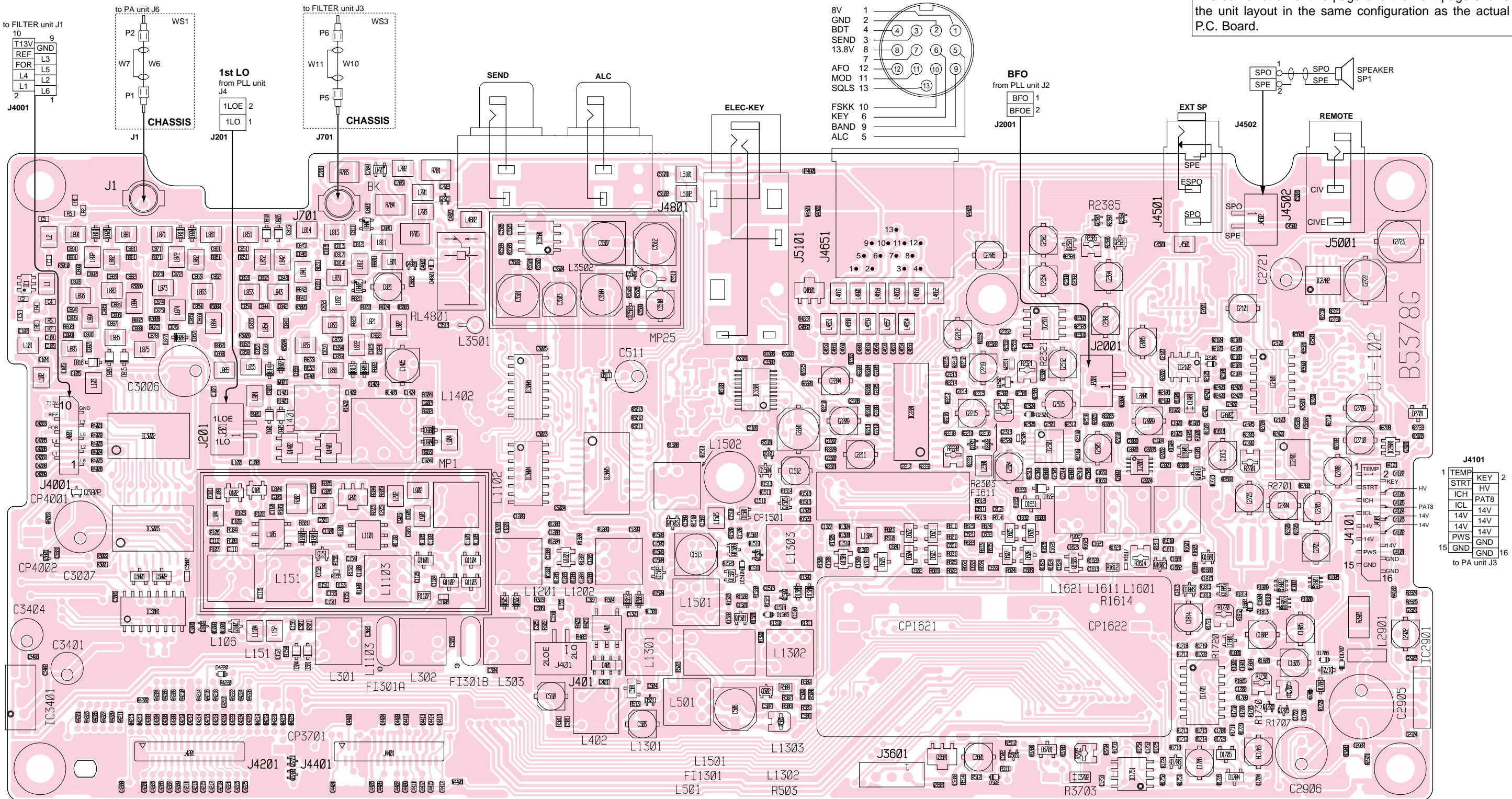
NAME	SYMBOL	INSIDE VIEW
1SS184 DAN202K	B3 N	
1SS226 1SS375-TL DA221 TL MA742	C3 FH K M1U	
1SS355 MA2S111 MA2S728	A A B	
1SV312	BB	
DAP202K T146 DAP222 TL	P P	
HSB88WSTR	Silver line	
KV1470TL	F7	

NAME	SYMBOL	INSIDE VIEW
MA29B	Y	
MA77	4B	
MA8043-H MA8051-M (TX)	4^3 5-1	
NNCD6.2G-T1	62G	
RD10M-T2B3	103	

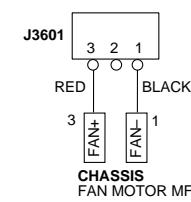
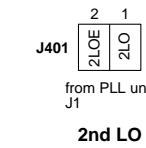
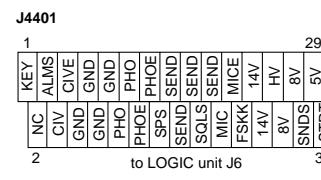
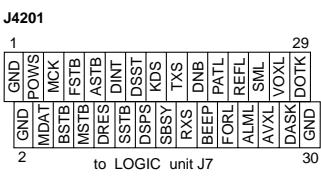
## SECTION 9 BOARD LAYOUTS

### 9-1 MAIN UNIT

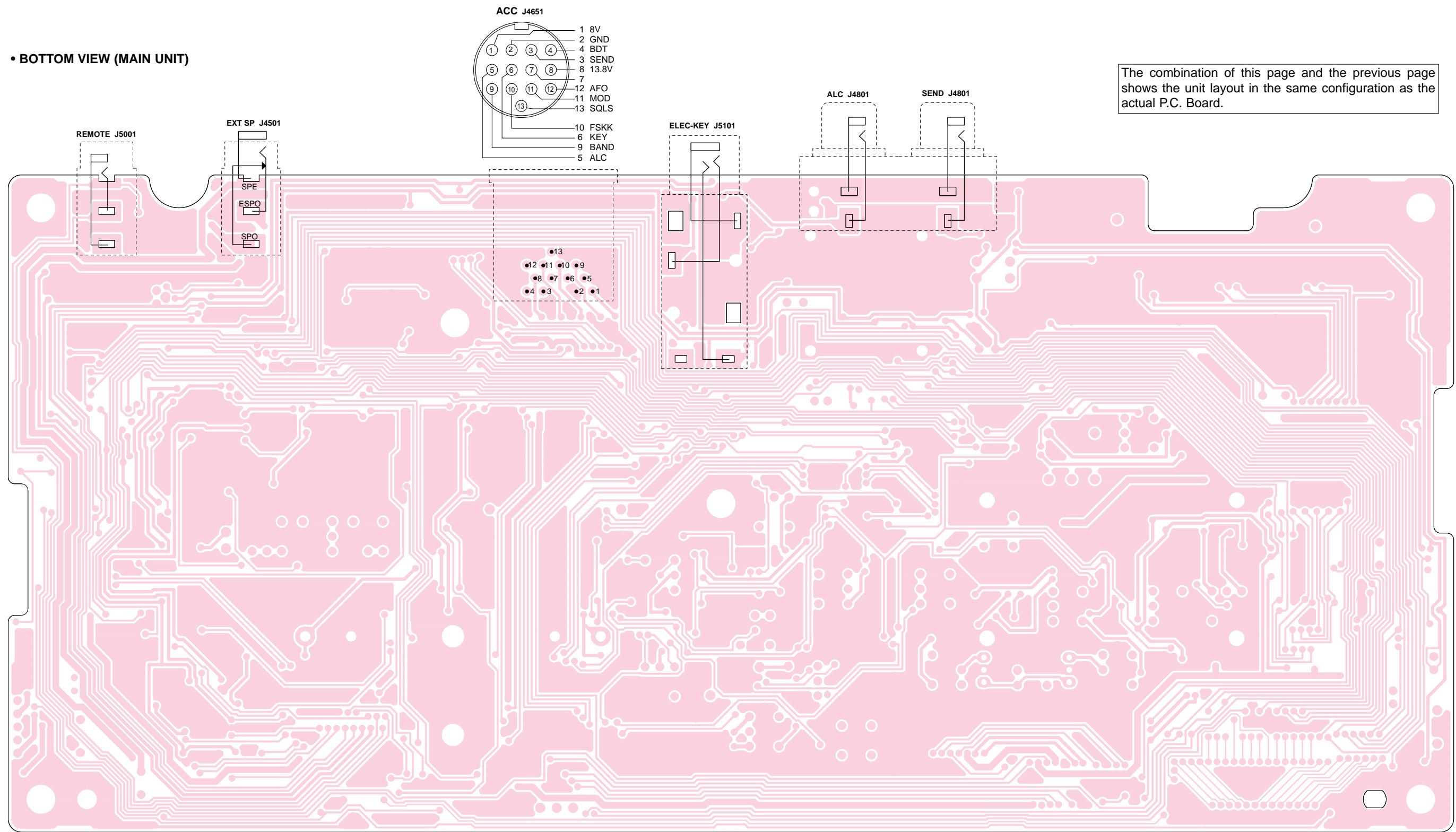
#### • TOP VIEW



The combination of this page and the next page shows the unit layout in the same configuration as the actual P.C. Board.

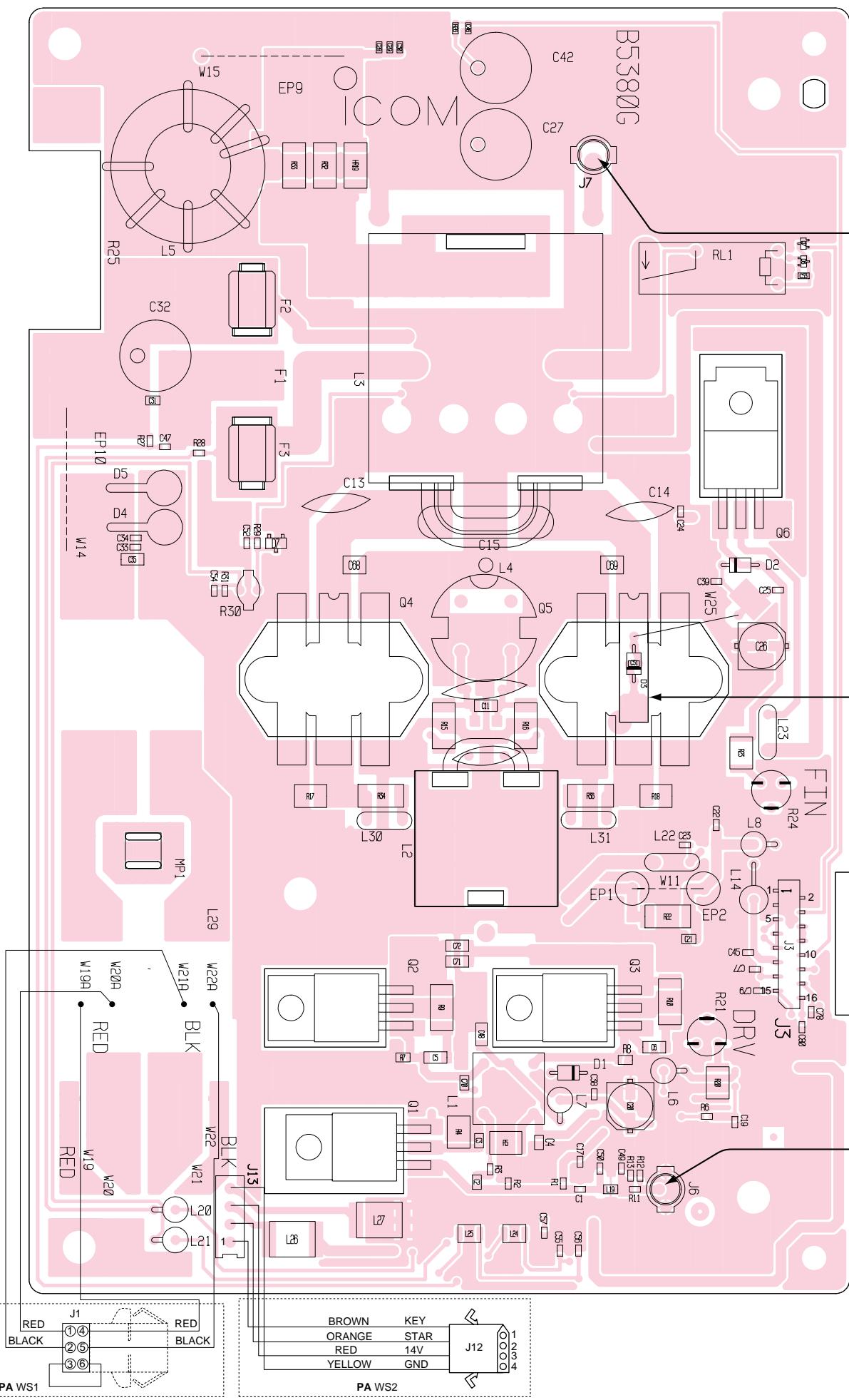


• BOTTOM VIEW (MAIN UNIT)



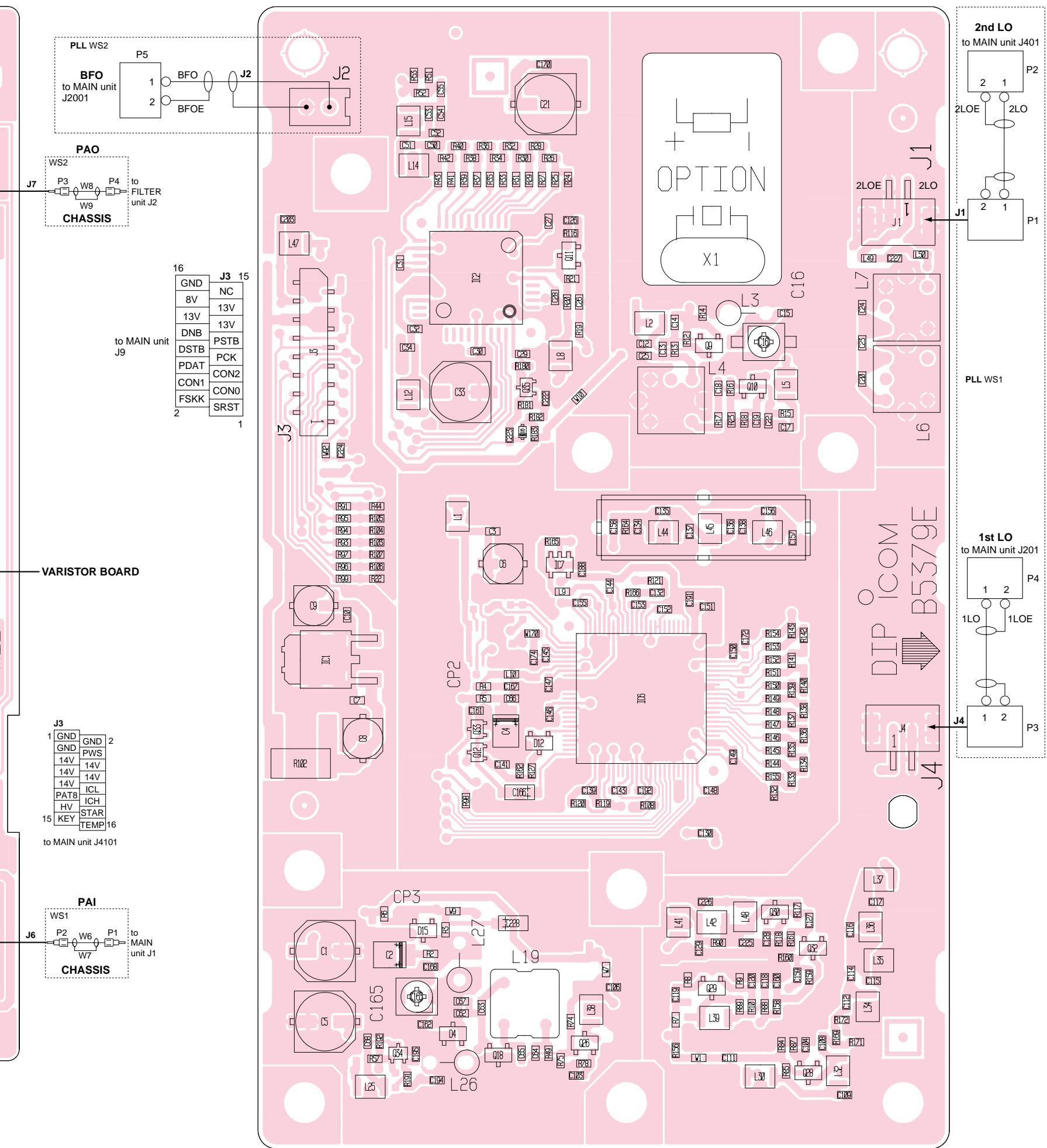
## 9-2 PA UNIT

• TOP VIEW



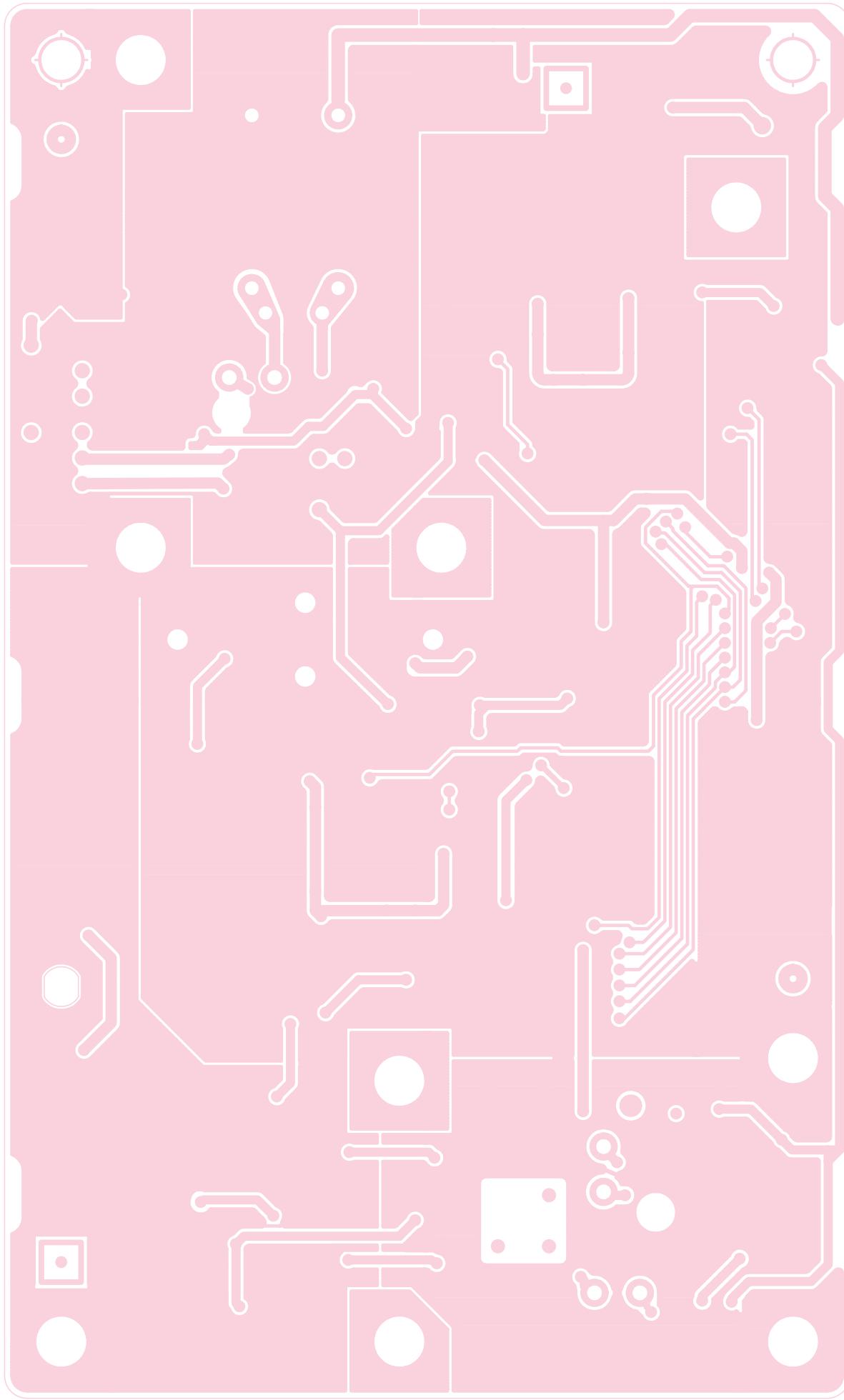
## 9-3 PLL UNIT

• TOP VIEW

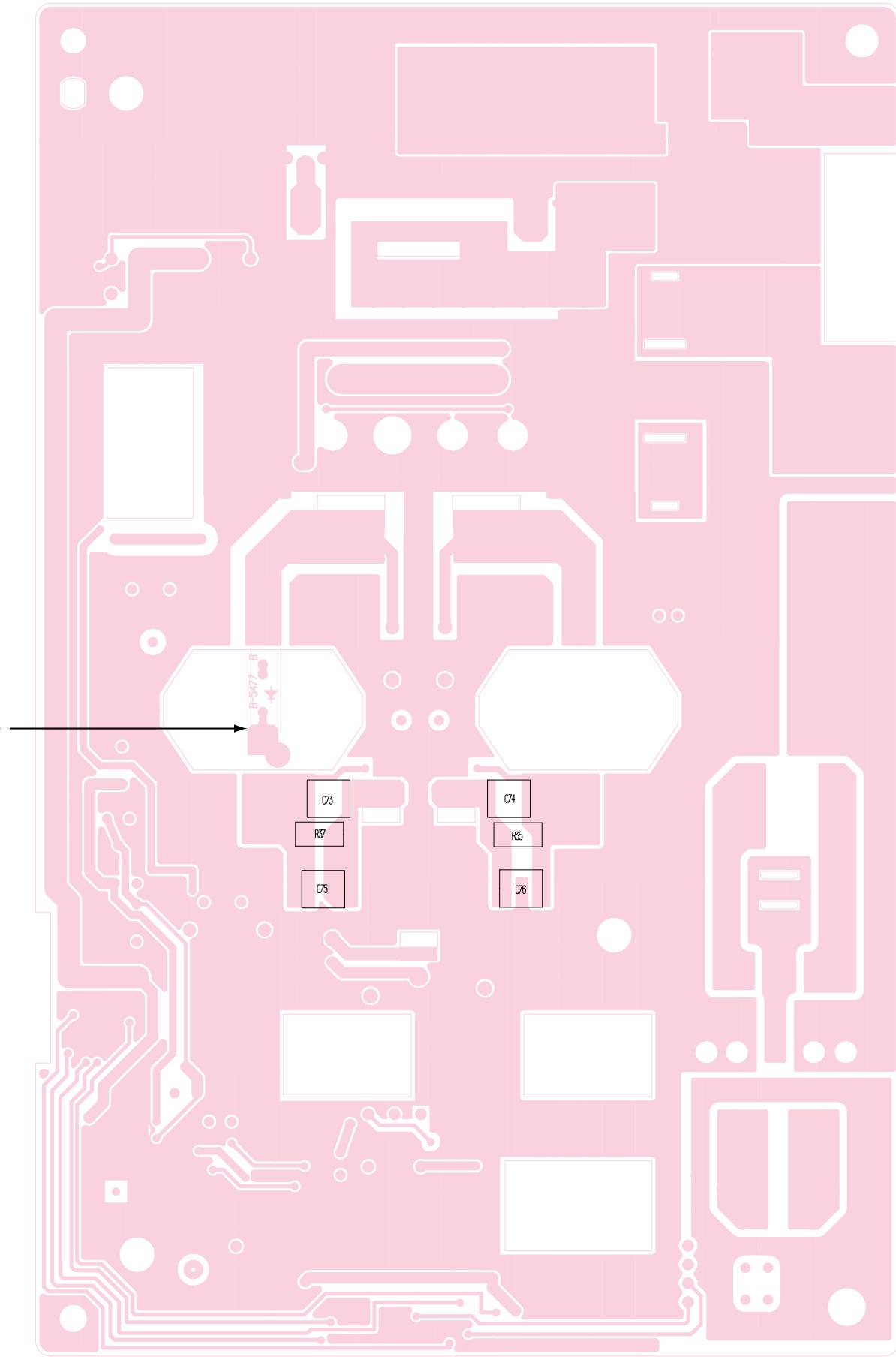


The combination of this page and the previous page shows the unit layout in the same configuration as the actual P.C. Board.

• BOTTOM VIEW (PLL UNIT)



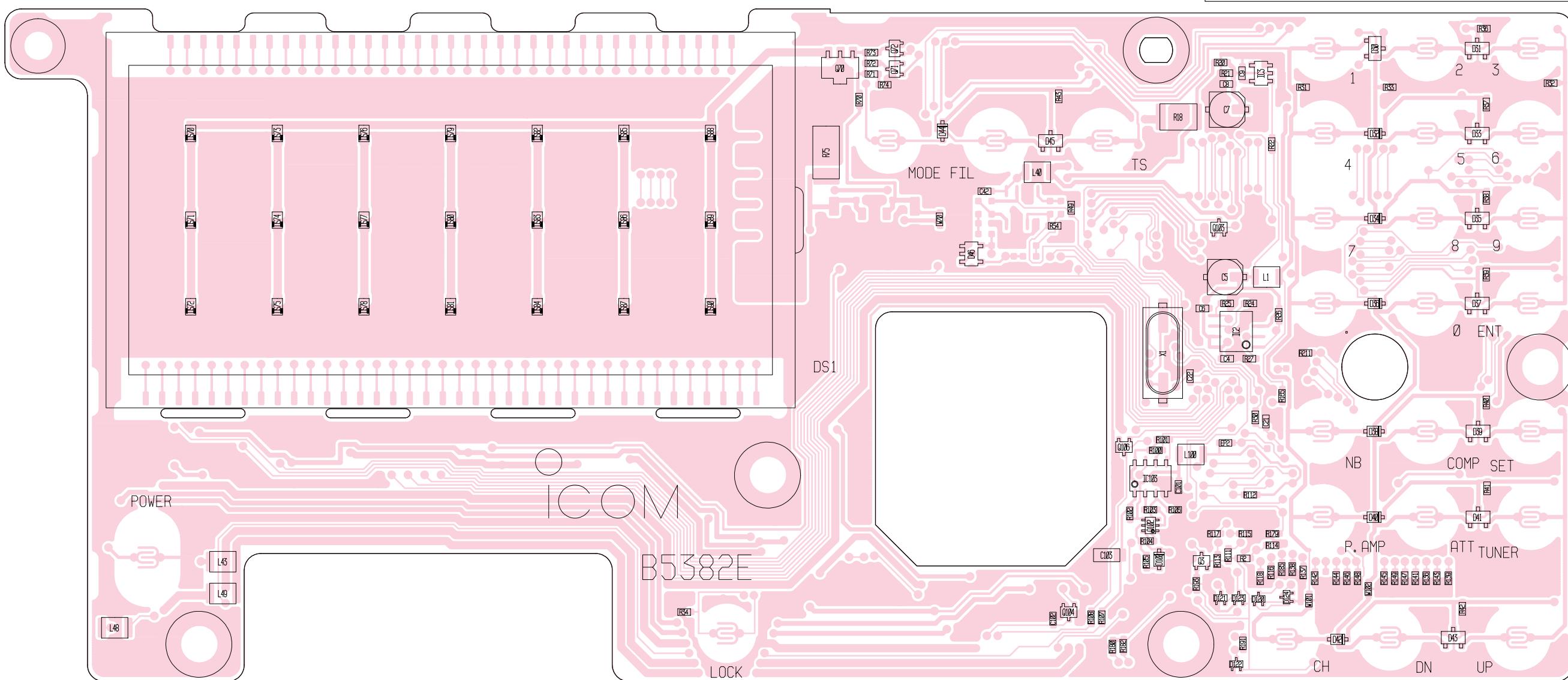
• BOTTOM VIEW (PA UNIT)



#### 9-4 LOGIC BOARD

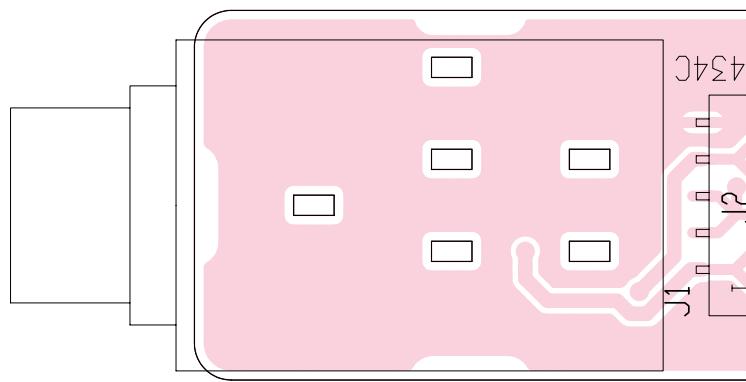
• TOP VIEW

The combination of this page and the next page shows  
the unit layout in the same configuration as the actual  
P.C. Board.



#### 9-5 PHONE BOARD

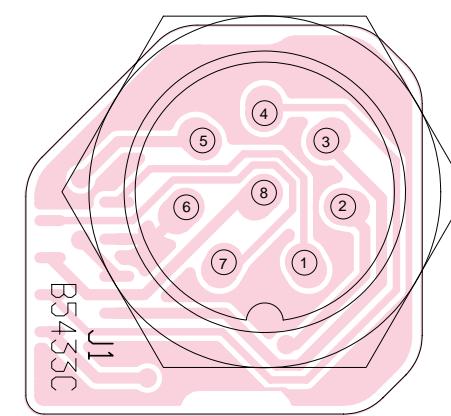
• TOP VIEW



to LOGIC  
unit J5

#### 9-6 MIC BOARD

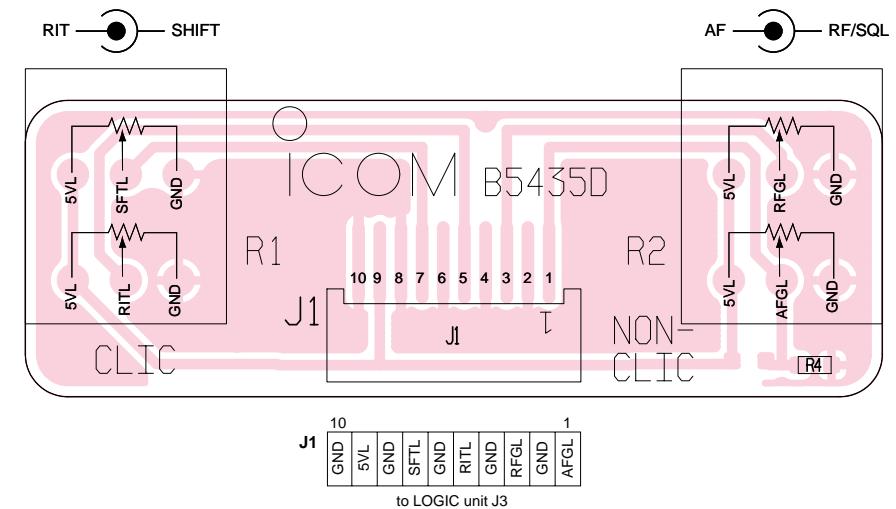
• TOP VIEW



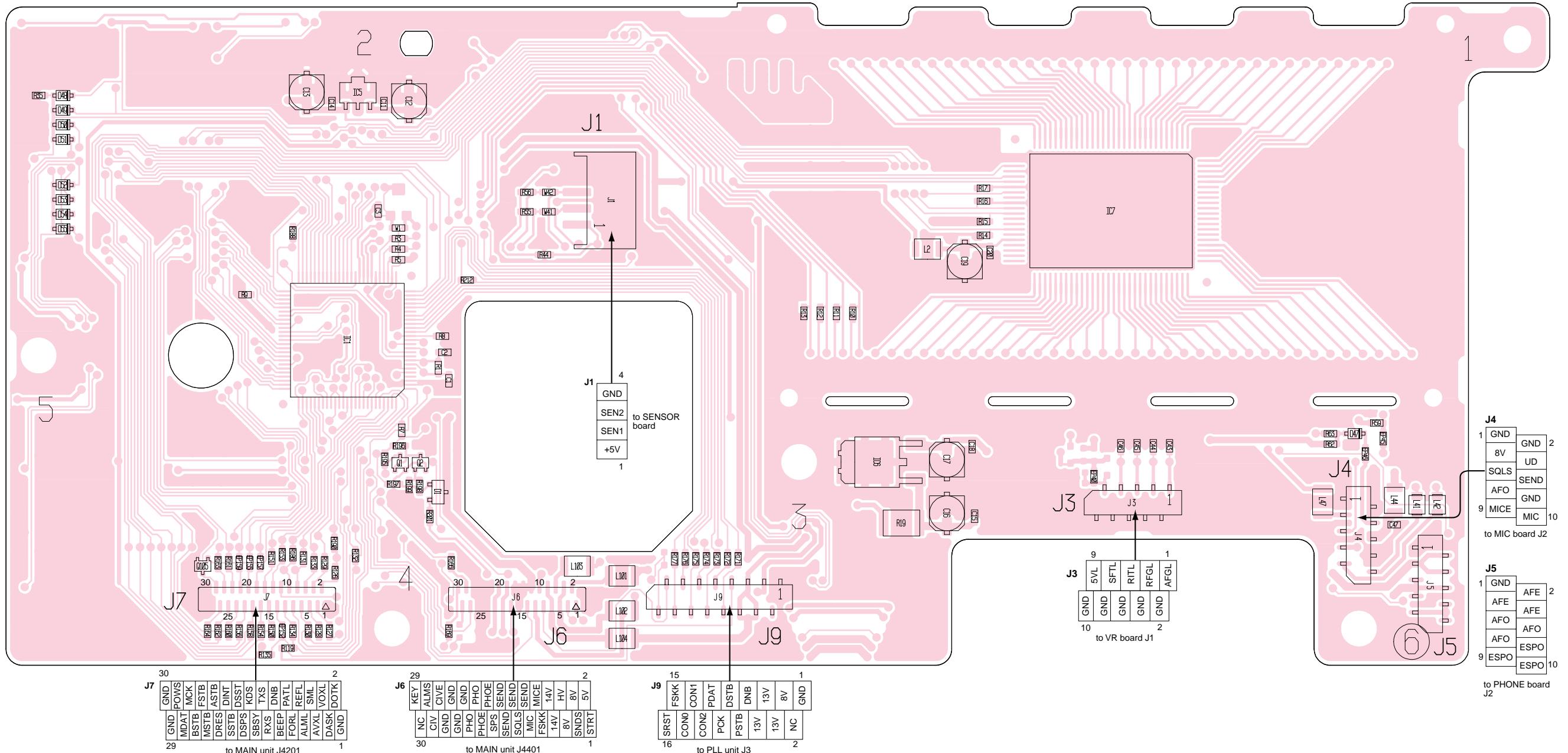
J1

#### 9-7 VR BOARD

• TOP VIEW



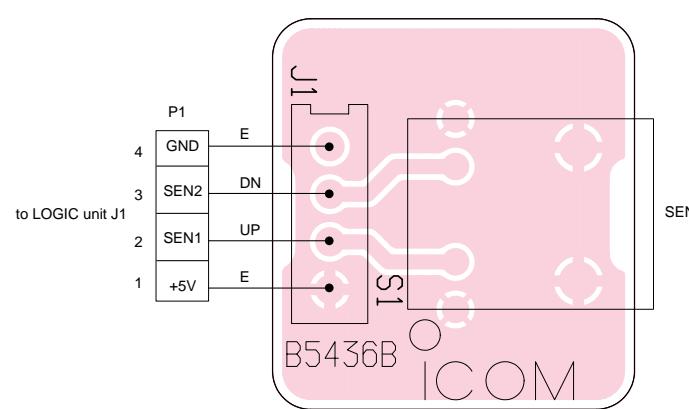
• BOTTOM VIEW (LOGIC UNIT)



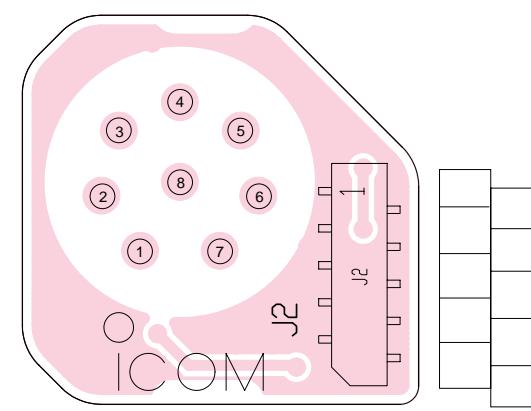
The combination of this page and the previous page shows the unit layout in the same configuration as the actual P.C. Board.

9-8 SENSOR BOARD

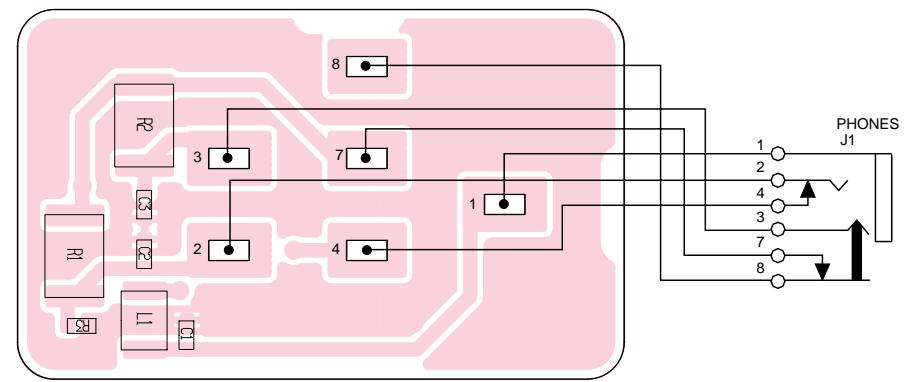
• TOP VIEW



• BOTTOM VIEW (MIC BOARD)

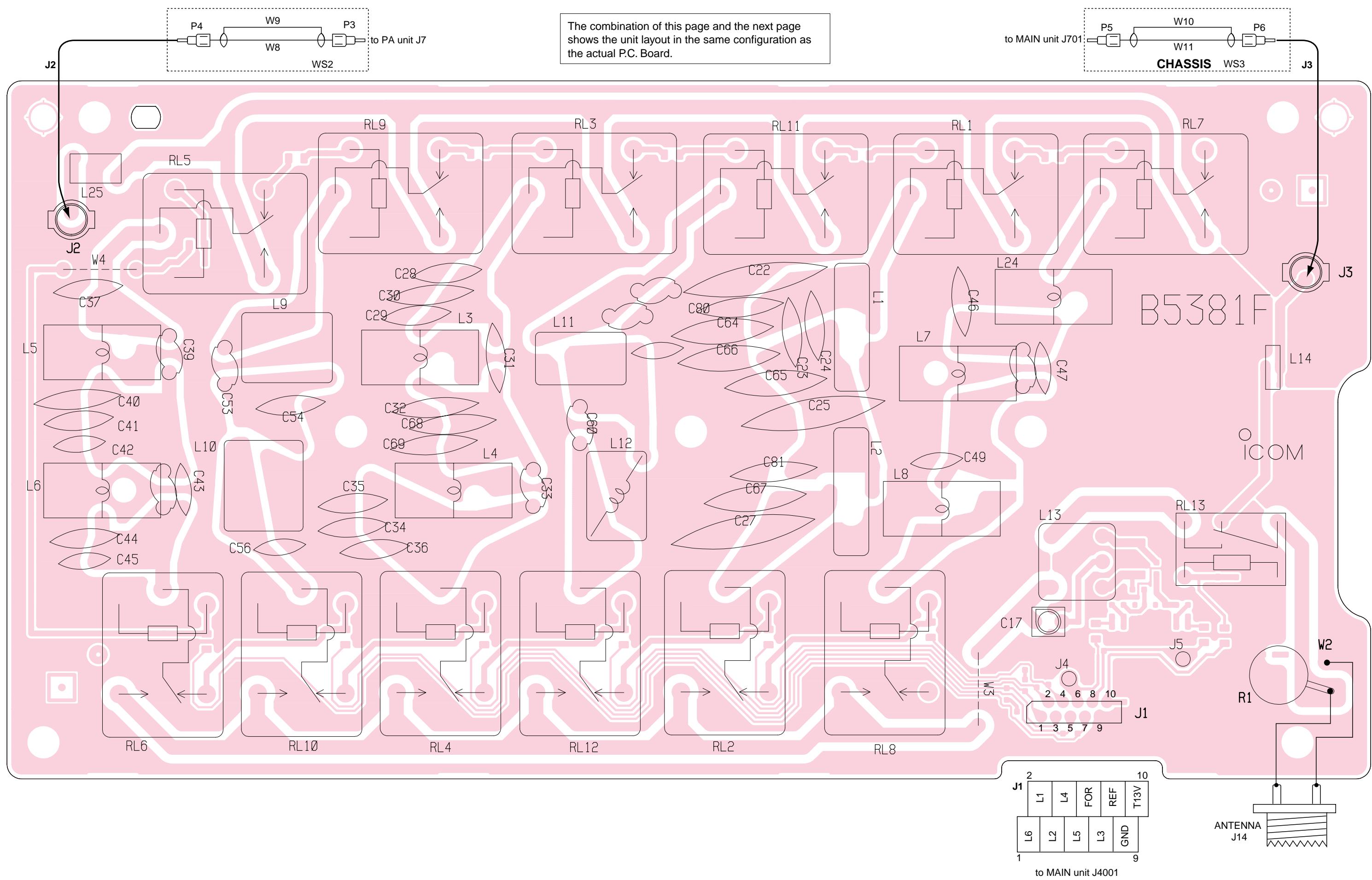


• BOTTOM VIEW (PHONE BOARD)



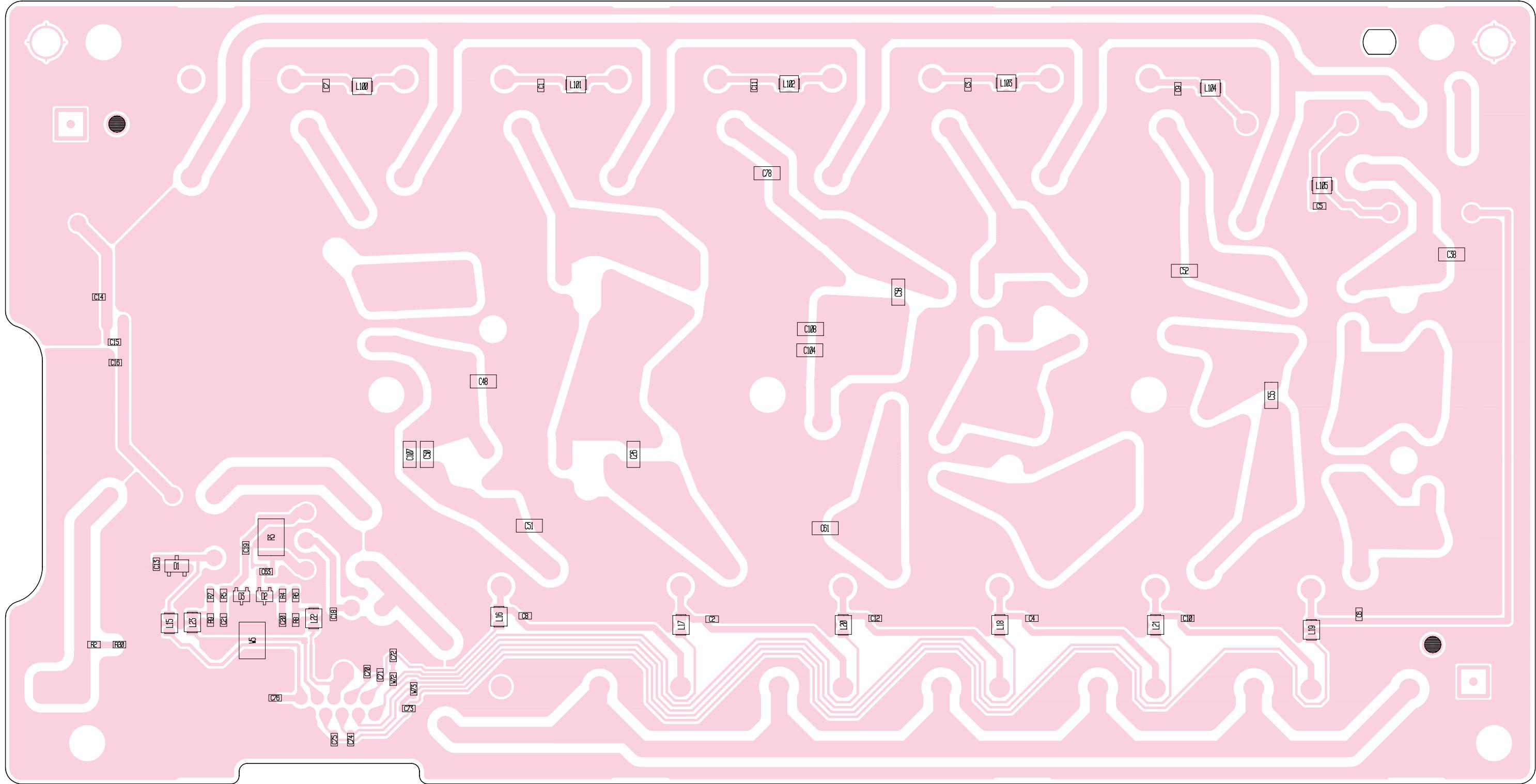
## 9-9 FILTER UNIT

• TOP VIEW



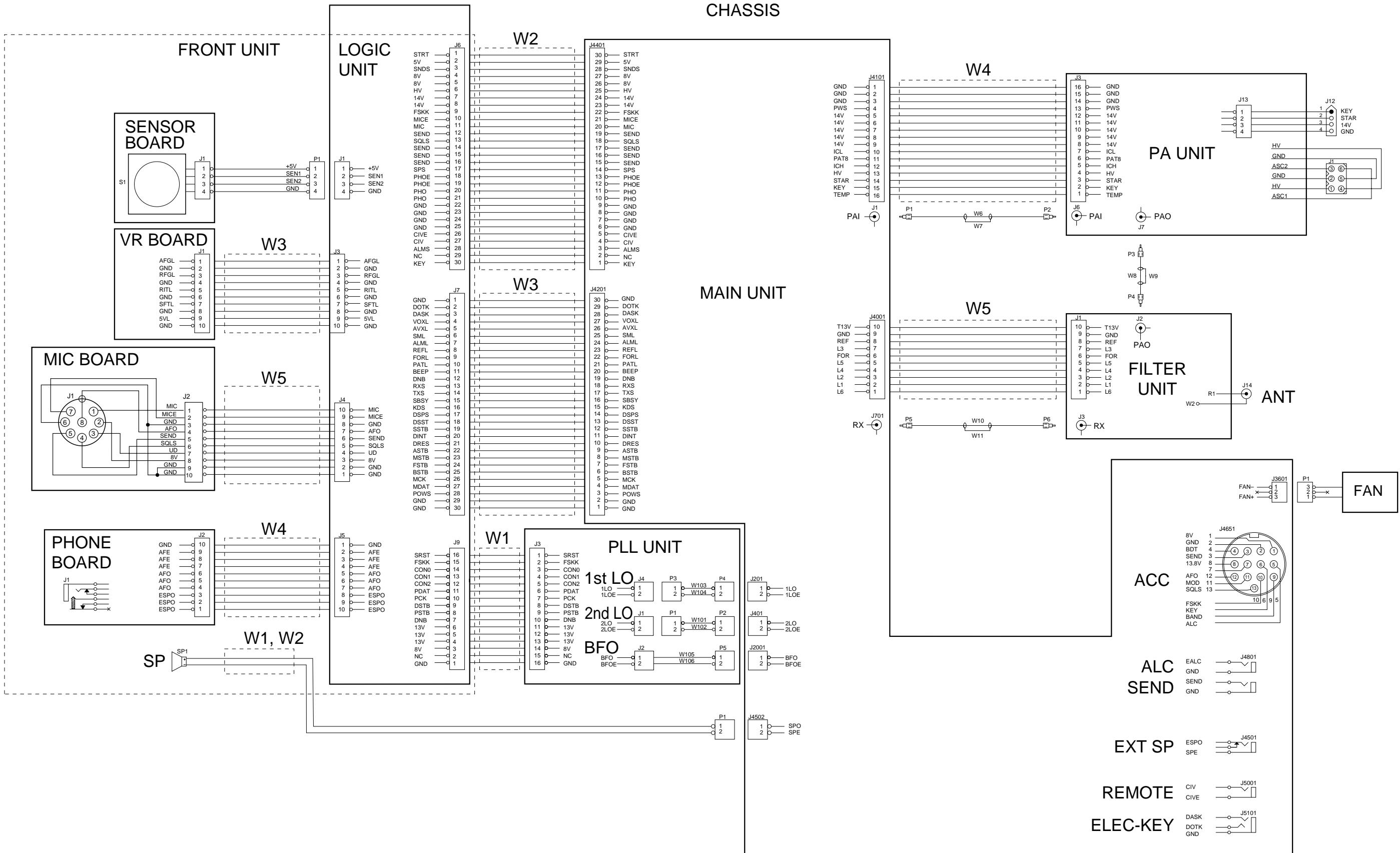
The combination of this page and the previous page shows the unit layout in the same configuration as the actual P.C. Board.

• BOTTOM VIEW (FILTER UNIT)



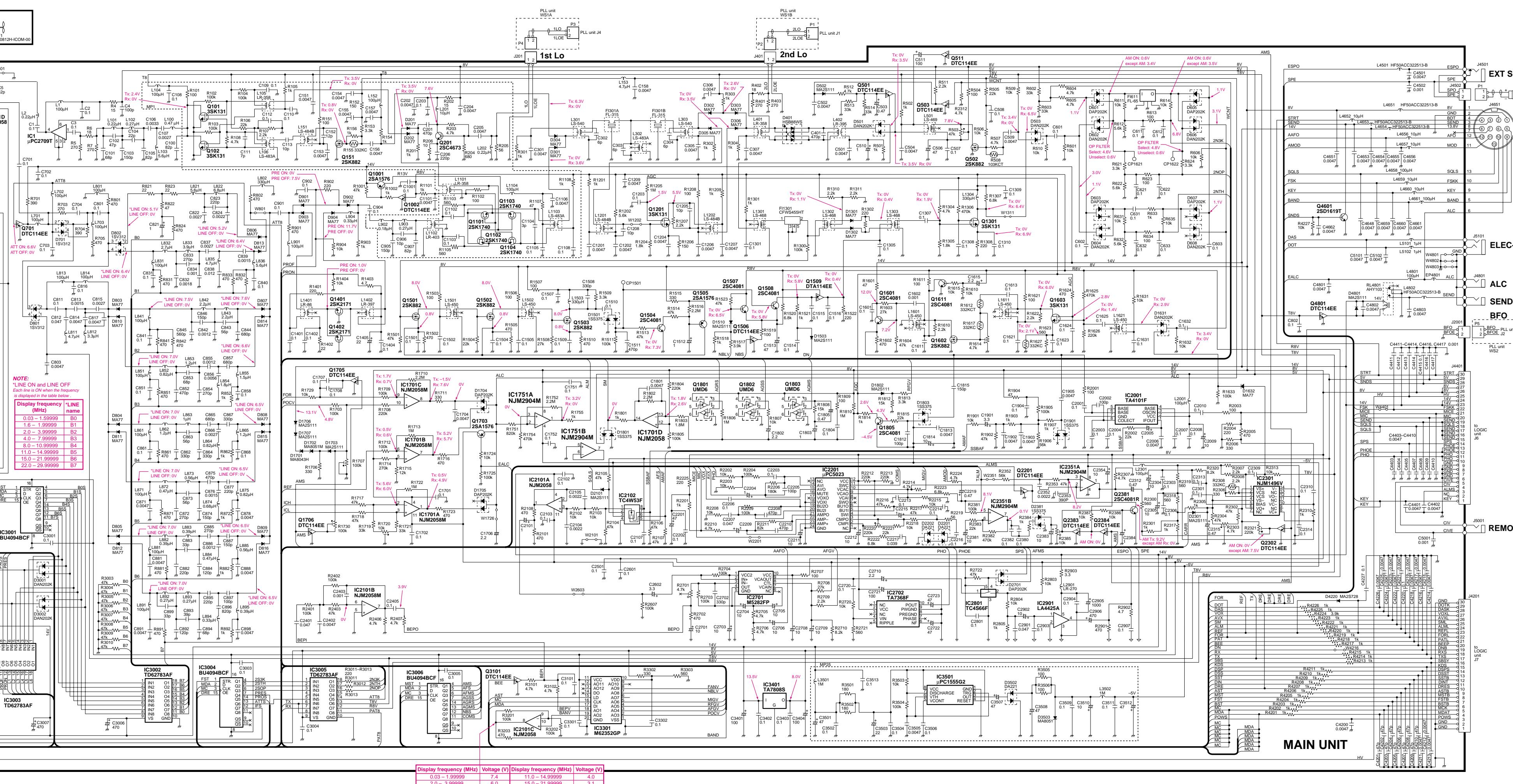
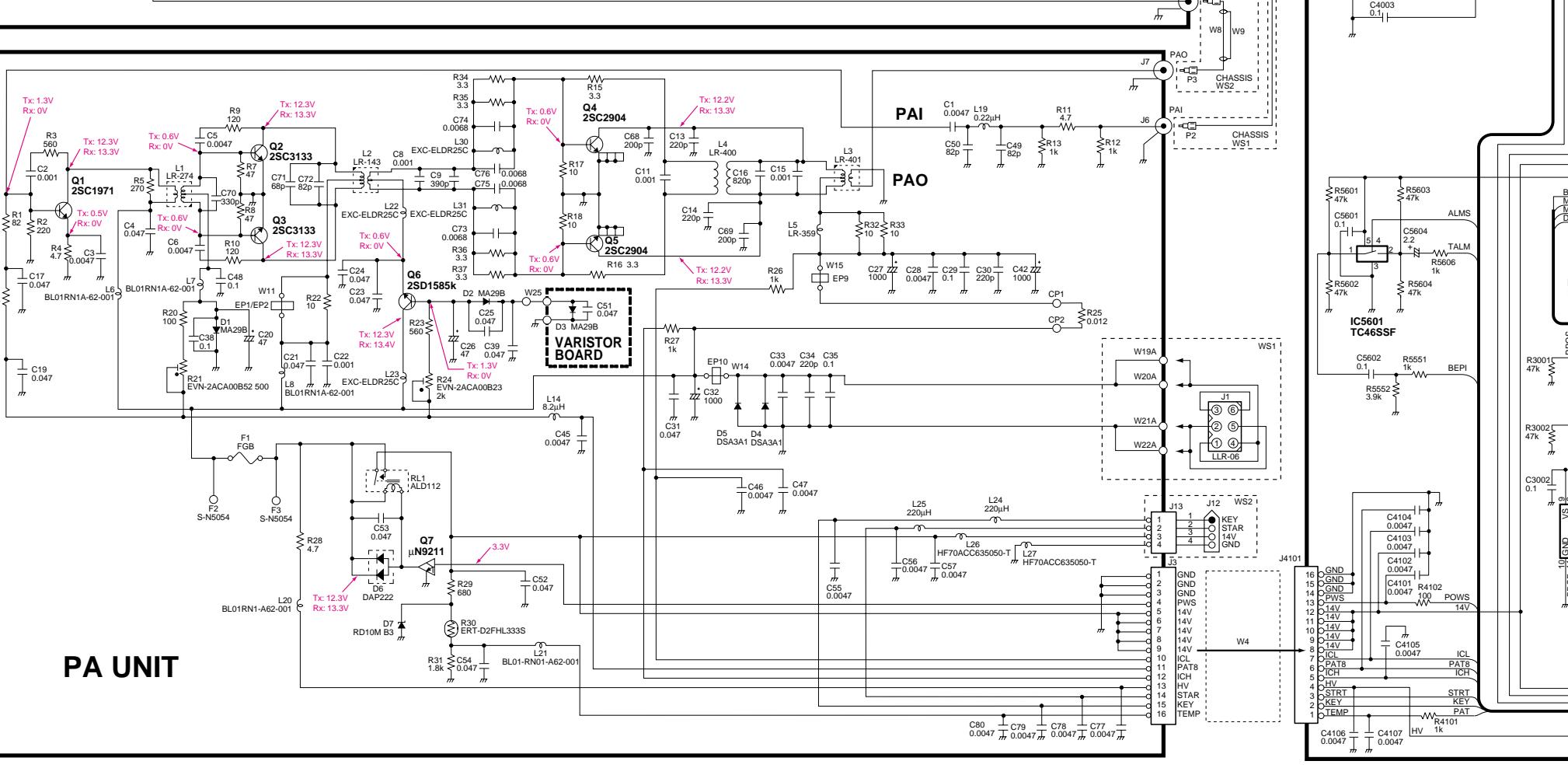
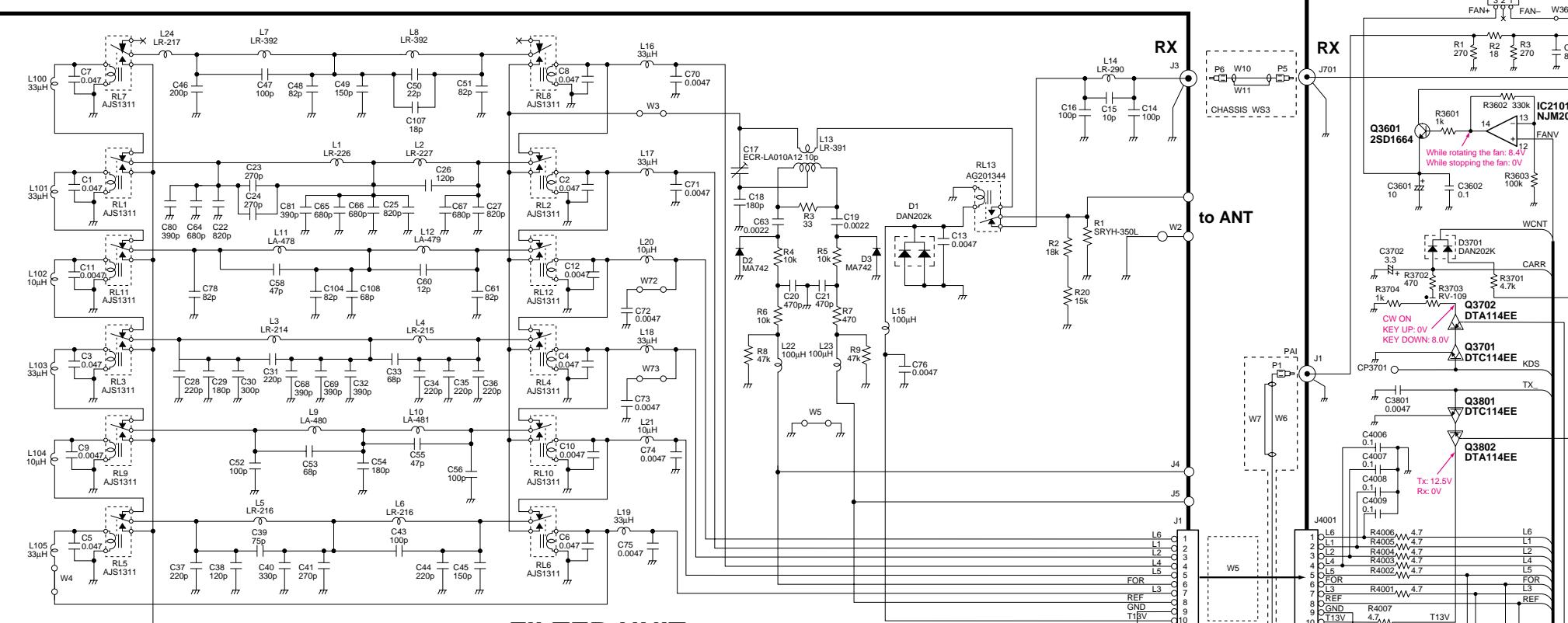


## SECTION 11 WIRING DIAGRAM

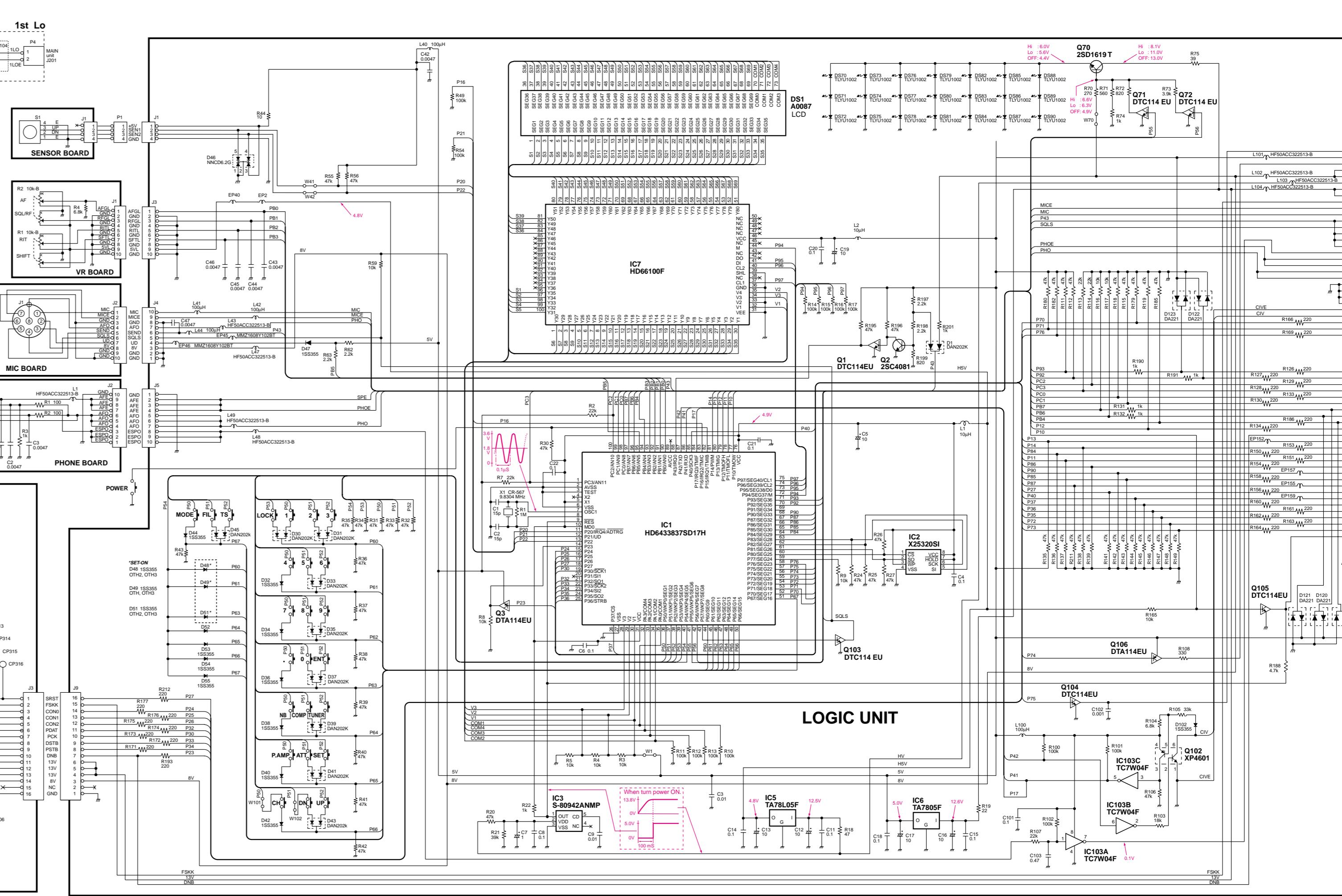
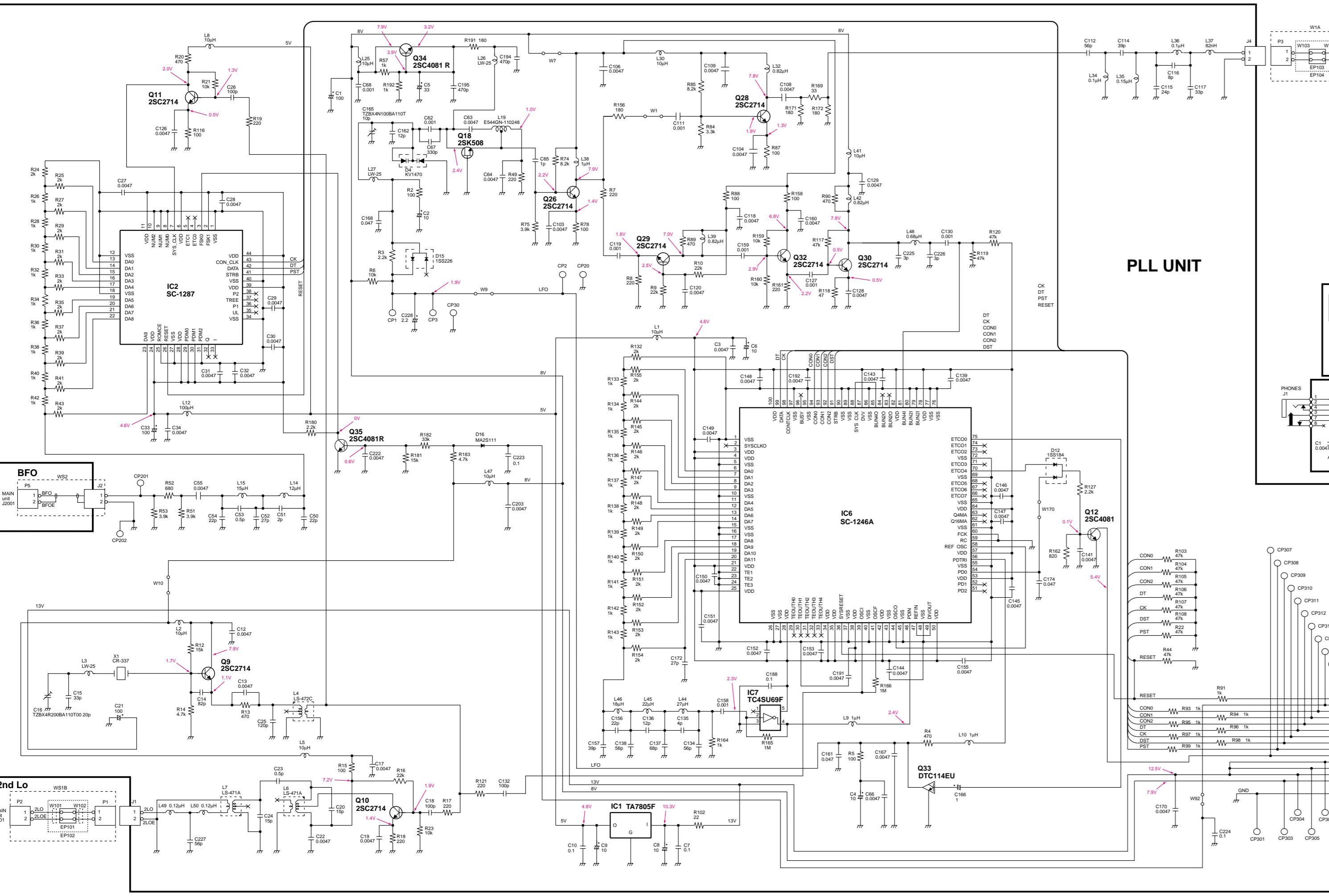


## SECTION 12 VOLTAGE DIAGRAM

### 12-1 FILTER, PA and MAIN units



## 12-2 PLL and LOGIC units



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