NTDPJTV04

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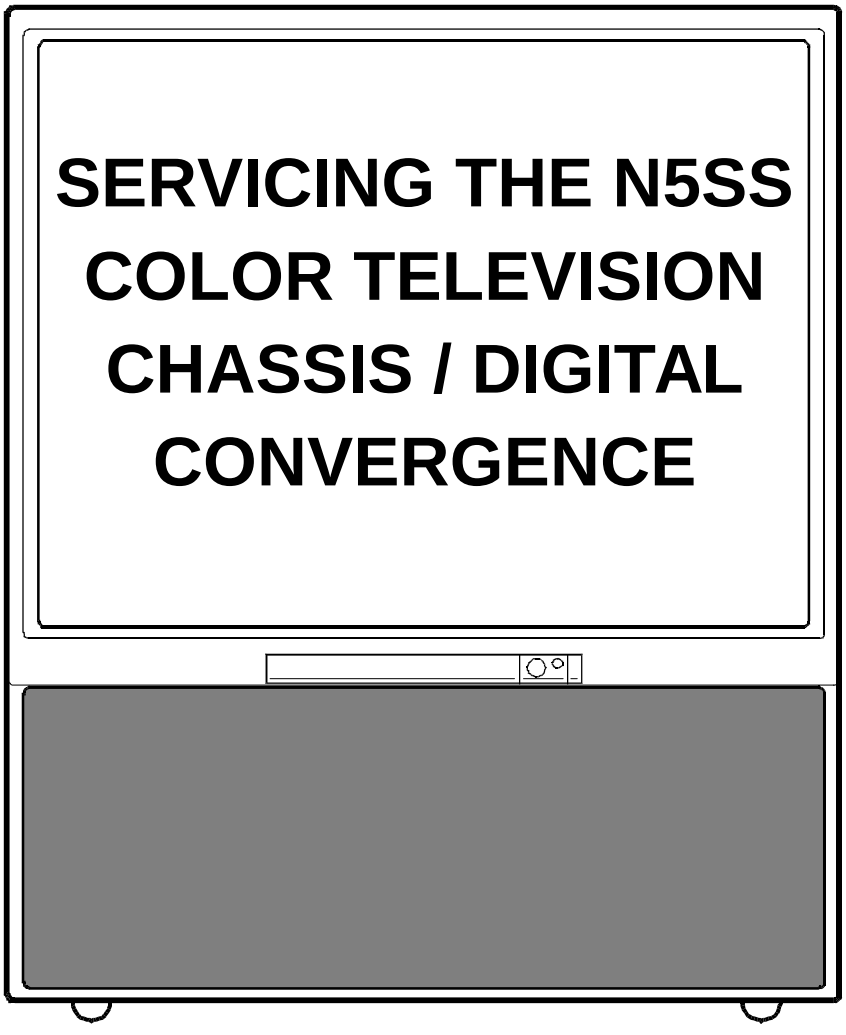

SERVICING THE N5SS COLOR TELEVISION CHASSIS / DIGITAL CONVERGENCE

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FOREWORD

The material presented in this manual is provided for the technical training of TACP employees and qualified service personnel only.

The specific circuit reference designations, pin numbers, etc., are taken from the TP48E50/60 Service Manual, File Number 020-9508. The diagrams in this manual are simplified for training and should be used as a reference guide only when servicing the N5SS CTV Chassis. Refer to the applicable service data for detailed adjustment and servicing procedures.

NTDPJTV04

SERVICING TOSHIBA'S N5SS TELEVISION CHASSIS

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SECTION I
OVERALL UNIT CHARACTERISTICS BLOCK DIAGRAMS LABS 1 & 2

SECTION I

OVERALL UNIT CHARACTERISTICS

1. MAIN FEATURES

The main feature of Toshiba's projection television model TP48E60, is the use of the N5SS (TG-1C) chassis. This chassis utilizes a bus control system, developed by PHILIPS Corporation, called the I^2C (or IIC) bus. IIC stands for Inter-Integrated Circuit control. This bus co-ordinates the transfer of data and control between ICs inside the Television. It is a bi-directional serial bus consisting of two lines, namely SDA (Serial DATA), and SCL (Serial CLOCK).

Digital data which is passed along the bus is received by individual devices and can be either command or data. Digital-to analog converters are also found within some of the ICs, allowing them to be addressed and controlled by strings of digital instructions, replacing those functions which were previously implemented by external potentiometers.

2. MERITS OF THE BUS SYSTEM

2-1. Improved Serviceability

Most of the adjustments previously made by resetting variable resistors and/or capacitors can be made on the new chassis by operating the remote control and seeing the results on the television screen. This allows adjustments to be made without removing covers on the unit thus increasing servicing speed and efficiency.

2-2. Reduction of Parts Count

The use of digital-to-analog converters built into the ICs, allowing them to be controlled by software, has eliminated or reduced the requirement for many discrete parts such as potentiometers and trimmers, etc.

2-3. Quality Control

The central control of adjustment data makes it easier to understand, analyze, and review the data, thus improving the quality of the product.

3. COMPARISON/DIFFERENCES OF TG-1 CHASSIS

Toshiba's concept for the TG-1 chassis was to create a sort of universal chassis which, with minimal changes, could be used as a standard throughout the entire Toshiba color television lineup starting in 1995. TG-1 stands for "Toshiba Global 1". The TG-1 chassis can be found in several different models and varies in both complexity and features.

Root Chassis	TG-1 Chassis	Typical Sizes	Picture and Features
N5E	A1	13, 19	Less
N5ES	A2	20, 32	
N5S	A2 - LEM	20, 32	
N5S	B	27, 32	
N5SS	C	27 thru 35	More

Typical Chassis Examples	
Model	TG-1
CF13E22,23	A1
CF19E22	A1
CF20E30	A1
CF20E40	A1
CN27E55	A2
CF30E50	A2
CF32E50	A2
CF32E55	A2
CX32E60	B
CX32E60	B
CN27E90	C
CX32E70	C
CN32E90	C
CN35E15	C
TP48E50,51	C
TP48E60,61	C
TP55E50,51	C
TP55E80.81	C
TP61E80	C
TP48E90	C

4. SPECIFICATIONS

	CHASSIS	C	C	C	C	C	C
	MODEL Nbr / SPECIFICATION	TP48E50 TP48E51	TP48E60 TP48E61	TP48E90	TP55E50 TP55E51	TP55E80 TP55E81	TP61E80 STEP-UP
* GENERAL	1 Picture Size#	48"-D/S	48"-D/S	48"-D/S	55"-D/S	55"-D/S	61"-D/S
	2 Channel Capacity	181ch	181ch	181ch	181ch	181ch	181ch
	3 C. Caption	●	●	●	●	●	●
	4 MTS with dbx	●	●	●	●	●	●
	5 Bass, Tre/Balance	●	●	●	●	●	●
	6 Sub-Audio-Program	●	●	●	●	●	●
	7 Remote Control	*A-Uni (42k	A-Uni (42k	*Intelig+EZ	A-Univ (42k	A-Univ (43k	A-Univ (43k
	8 Picture-in-Picture	* ● (1TN)	● (2TN)	● (2TN)	● (1TN)	● (2TN)	● (2TN)
	9 LED Indicator (RED)	● (P)	● (P)	● (P)	● (P)	● (P)	● (P)
	10 Local Key	8key	8key	8key	8key	8key	8key
* SOUND	11 Dolby Surround	—	—	●(Prolo)	—	●	●
	12 Dig-Sound Processor	—	—	● (DSP4ch)	—	● (DSP4ch)	● (DSP4ch)
	13 Front Surround	●	●	—	●	—	—
	14 Cyclone ABX	—	—	—	—	—	—
	15 Sub-Bass-System	●	●	●	●	●	●
	16 Audio Output	14Wx2	14Wx2	14Wx2, 10Wx2 & 10Wx2	14Wx2	14Wx2 & 10Wx2	14Wx2 & 10Wx2
	17 Speaker Size & Nbr	160Rx2	160Rx2	160Rx2 & REAR SPK	160Rx2	160Rx2 & REAR SPK	160Rx2 & REAR SPK
* PICTURE	18 Comb Filter	● (DIG)	● (DIG)	● (DIG)	● (DIG)	● (DIG)	● (3D-Y/C)
	19 Dynamic Focus #	●	●	●	●	●	●
	20 Scan Velocity Modu	● (RGB)	● (RGB)	● (RGB)	● (RGB)	● (RGB)	● (RGB)
	21 Vert Contour Corre	—	—	—	—	—	—
	22 Black Level Expand	●	●	●	●	●	●
	23 Flesh Tone Correct	●	●	●	●	●	●
	24 Dynamic Noise Reduc	●	●	●	●	●	●
	25 Picture Preference	●	●	●	●	●	●
	26 Digital-Convergence	●	●	●	●	●	●
	27 Horiz Resolution	800	800	800	800	800	800
* OTHER	28 Parental-Ch Lock	●	●	●	●	●	●
	29 Channel Label (32ch)	●	●	●	●	●	●
	30 3-Language Display	●	●	●	●	●	●
	31 Clock/Off-Timer	● / ●	● / ●	● / ●	● / ●	● / ●	● / ●
	32 Favorite Channel	●	●	●	●	●	●
	33 Extended-Data-Servi	●	●	●	●	●	●
	34 Star-Sight-Decoder	—	—	—	—	—	—
* TERMS	35 S-Video In-Term	● (1+1)	● (1+1)	● (1+1)	● (1+1)	● (1+1)	● (1+1)
	36 Audio, Video-In/Out	1+2/1	1+2/1	1+2/1	1+2/1	1+2/1	1+2/1
	37 Front AV Jack	●	●	●	●	●	●
	38 Variable Audio Out	●	●	●	●	●	●
	39 2-RF Input	*—	●	●	—	●	●
	40 Ext Speaker Term	●	●	●	●	●	
	41 PIP Audio Out Jack	—	—	●	—	—	—
	42 Center-Ch-Aud-Input	—	—	—	—	●	●
AC	43 Speaker-Box	—	—	● (SS-SR94	—	● (SS-SR94	● (SS-SR94
	*Cabinet	NEW	NEW	NEW	NEW	NEW	NEW
	PARTS SUPPLY (ISO)	—	—	—	—	—	—

5. FRONT AND REAR CONTROL VIEWS

5-1. Front View

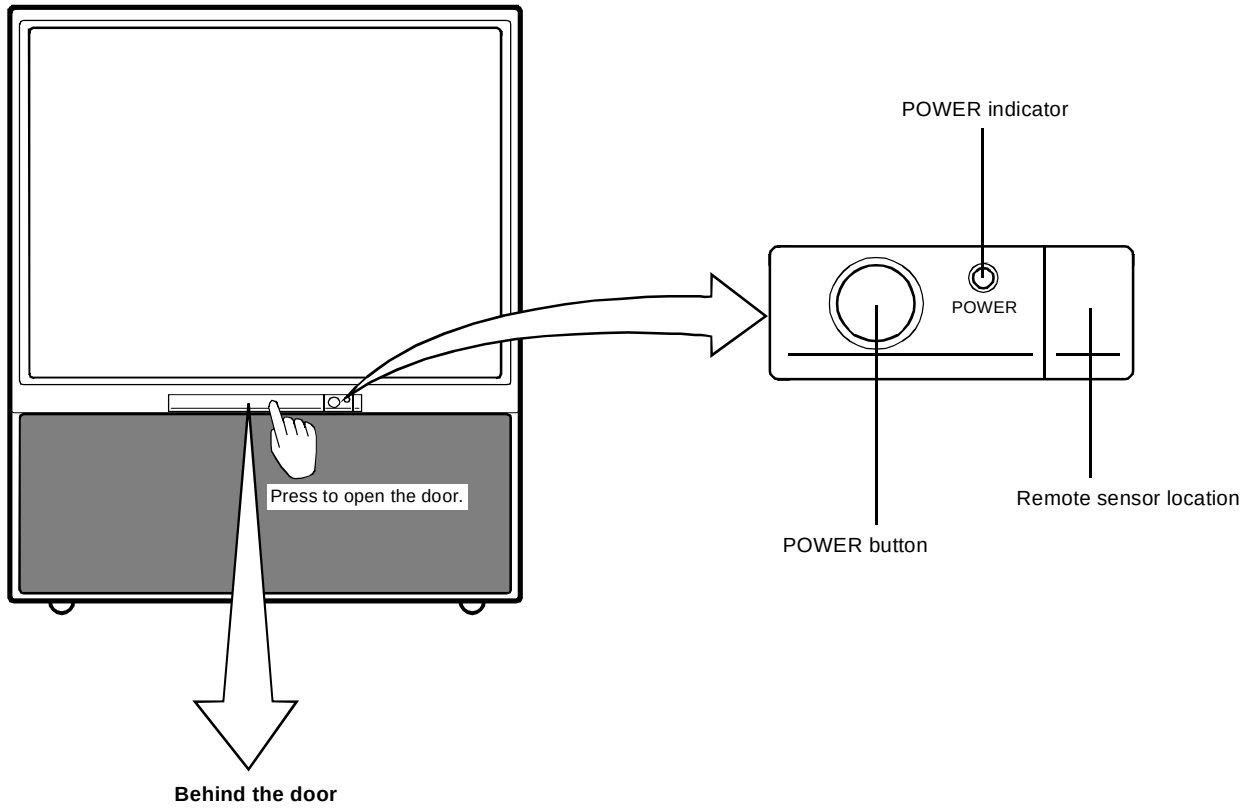
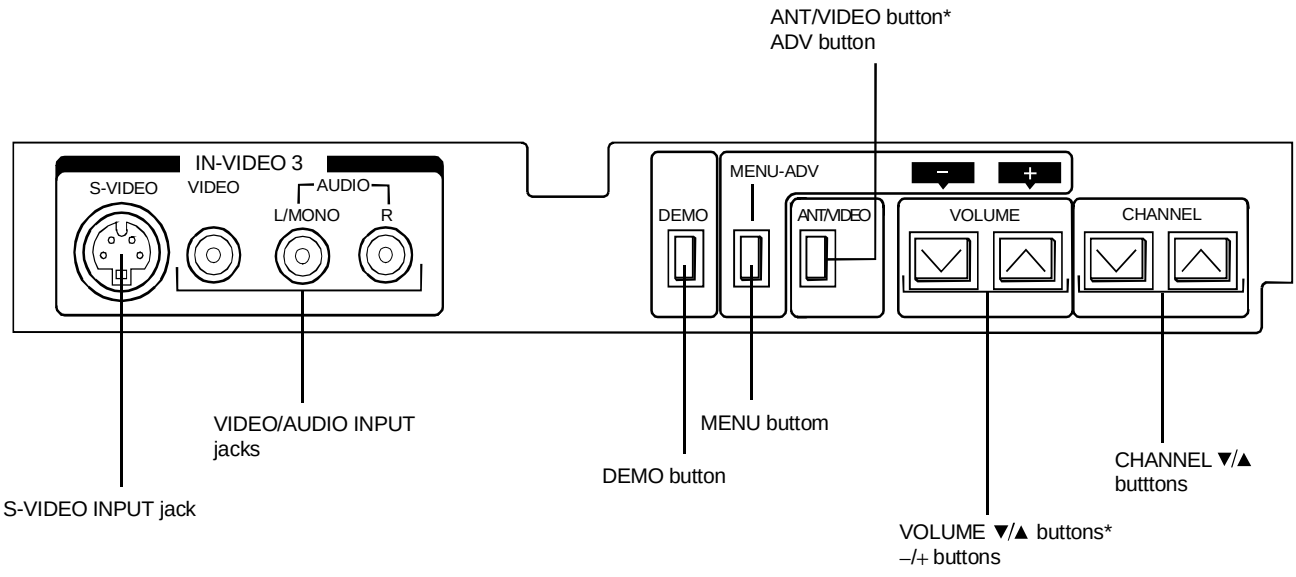


Fig. 1-1



* These buttons have dual functions.

Fig. 1-2

5-2. Rear View

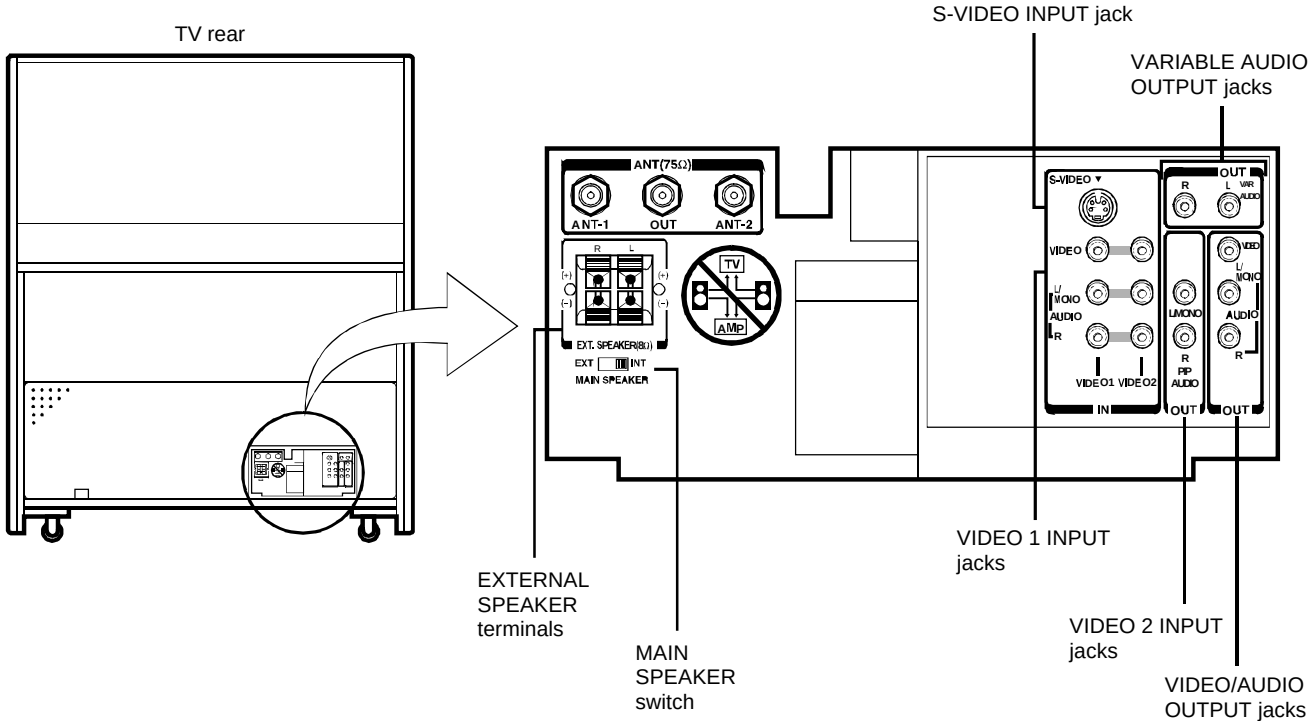


Fig. 1-3

5-3. Remote Control View

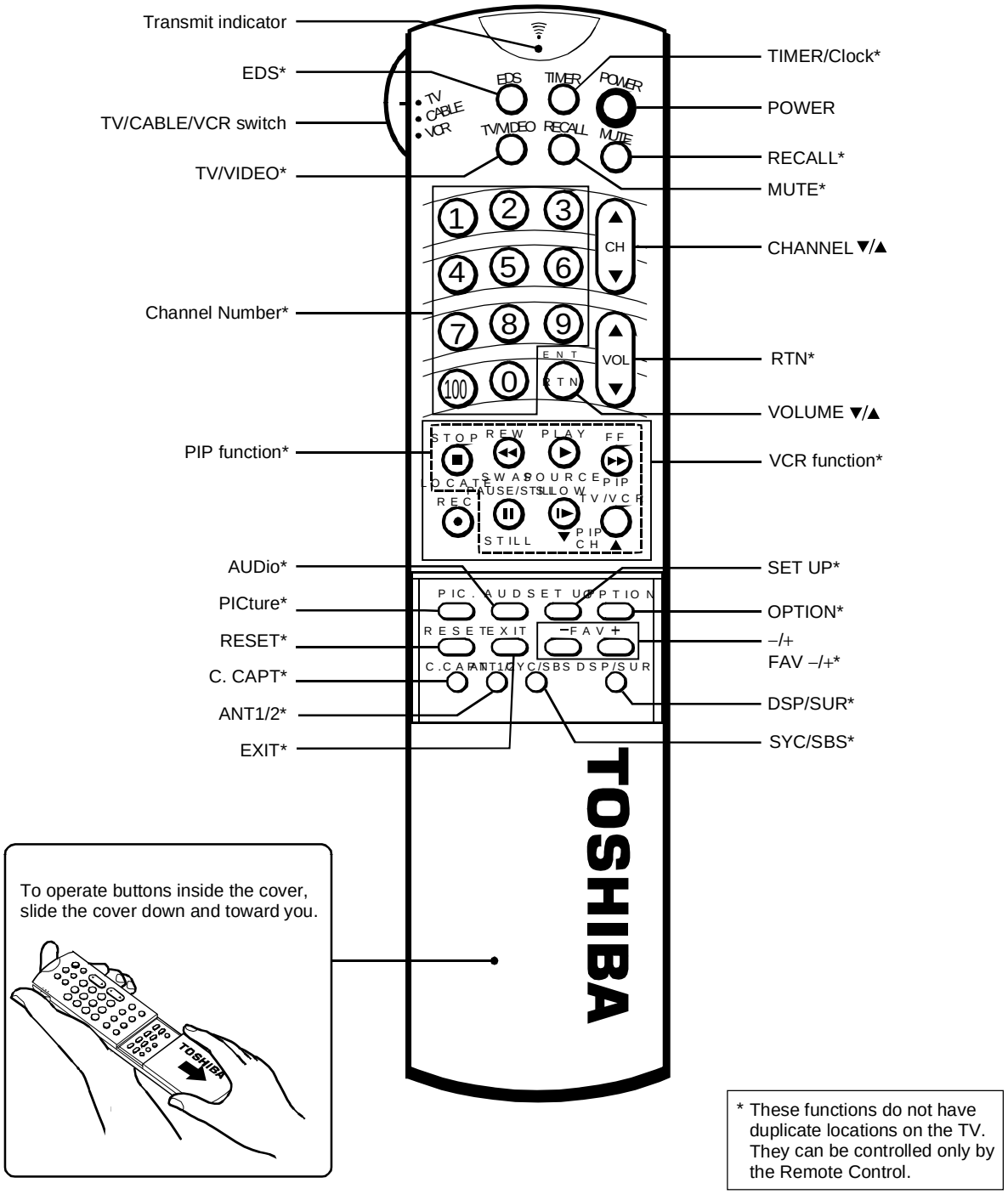


Fig. 1-4

6. PJTV CHASSIS LAYOUT

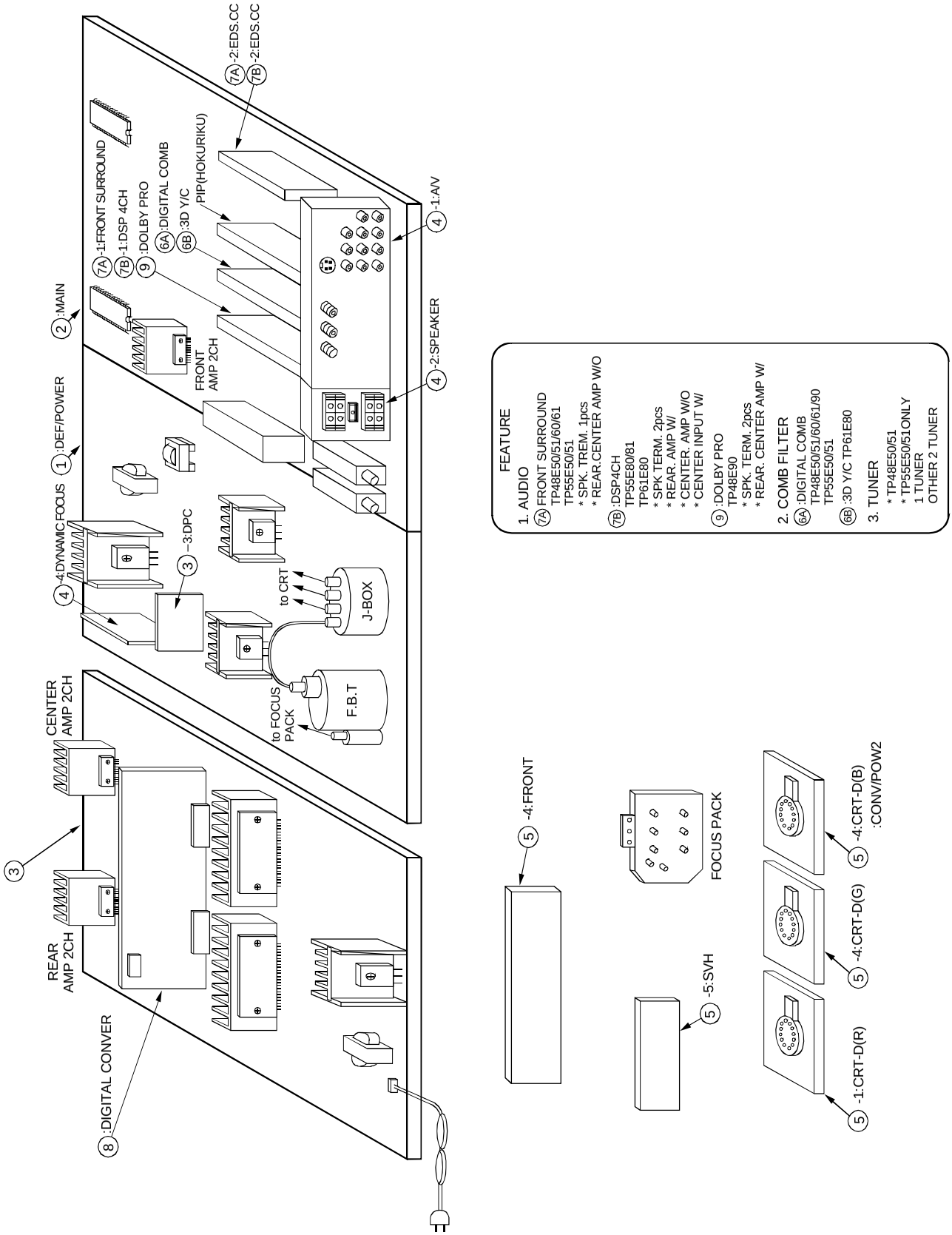
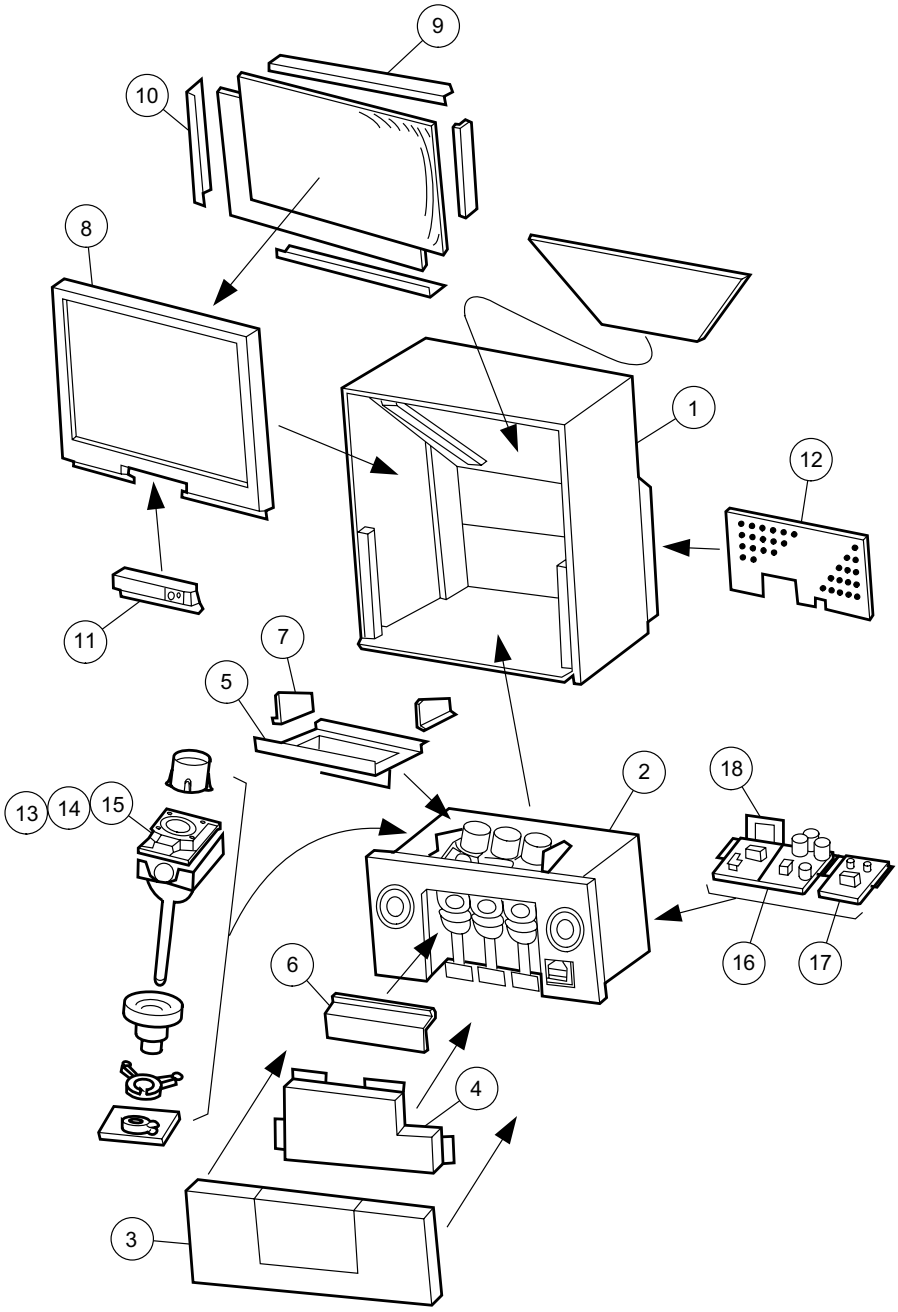


Fig. 1-5

7. CONSTRUCTION OF CHASSIS



1. WOOD CABINET
2. LIGHT BOX
3. SPEAKER GRILLE
4. FRONT COVER
5. CRT MOUNTING
6. SHIELD FRONT
7. SHIELD SIDE
8. SCREEN BEZEL
9. SCREEN BRACKET L
10. SCREEN BRACKET S
11. CONTROL PANEL
12. BACK BOARD
13. COUPLING R
14. COUPLING G
15. COUPLING B
16. CHASSIS FRAME MAIN
17. CHASSIS FRAME POWER
18. AV TERMINAL BOARD

Fig. 1-6

8. VIDEO SIGNAL FLOW BLOCK DIAGRAM

Basic Circuit Operation

The basic operation of the TG-1 chassis is illustrated in the block diagrams, figures 1-7 through 1-12. Although these diagrams focus on the TP48E60, the video and audio signal flow diagrams can be applied to any TG-1 chassis with minor modifications.

Video Signal Flow

Figure 1-7 illustrates the video signal flow through the TG-1 chassis. The Antenna 1 (ANT 1) and Antenna 2 (ANT 2) inputs allow two separate RF signals to be connected to the RF switcher. When the switch, which is controlled by the microcomputer, QA01, is in the up position the ANT 1 signal is connected to the HY01 PIP Tuner/IF and the H001 Main Tuner. Moving the switch down connects the ANT 2 signal to the H001 Tuner. Due to the RF Switch the ANT 2 signal can't be used as the PIP source, but when ANT 2 is selected the ANT 1 signal is available at RF OUT. The PIP Tuner/IF produces a composite video (CV) signal and sends it to the AV Switcher, QV01. An IF signal produced by the Main Tuner is sent to H002, which produces a composite video signal and sends it to the AV Switcher.

Three video inputs, video 1 through 3, are applied to the AV Switcher. The video 1 input can be composite video, Y/C video, or the test signal from QA01. Video 2 is composite video only, and video 3 is either composite video or Y/C video. A mechanical switch on the video 1 input defaults to the test signal, so a video connector must not be plugged into the video 1 input jack when the internal test signals are used.

The selected video signal is output as composite video and applied to the video output jack, the EDS/CC/RGB SW., and the Digital Comb Filter or the 3D - Y/C circuit. After processing the video signal is sent back to the AV Switcher as separate luminance (Y) and chrominance (C) signals. The Y and C signals are then sent to Q501 the Video Chroma Deflection Processing IC. A sync signal is tapped off the Y signal and applied to Q501. Q501 processes the video signal and sends separate R, G, and B signals to the CRT drives and the CRTs.

If the PIP feature is selected, composite video from AV Switcher is sent to the PIP circuit, ZY01. After processing, the PIP signal is sent to Q501 as R, G, B, and YS where it is mixed with the main video.

On screen display (OSD) R, G, and B signals produced by the Microcomputer, QA01, are mixed with the Extended Data Service (EDS) and Closed Caption (CC) data in UM01. These new signals are applied to an OR gate, QB91, and combined with the convergence signals from the digital convergence circuit. The convergence signals can be either the customer convergence cross hairs, or the service cross hatch pattern. All of these signals are sent to Q501 where they are mixed with the main video signal.

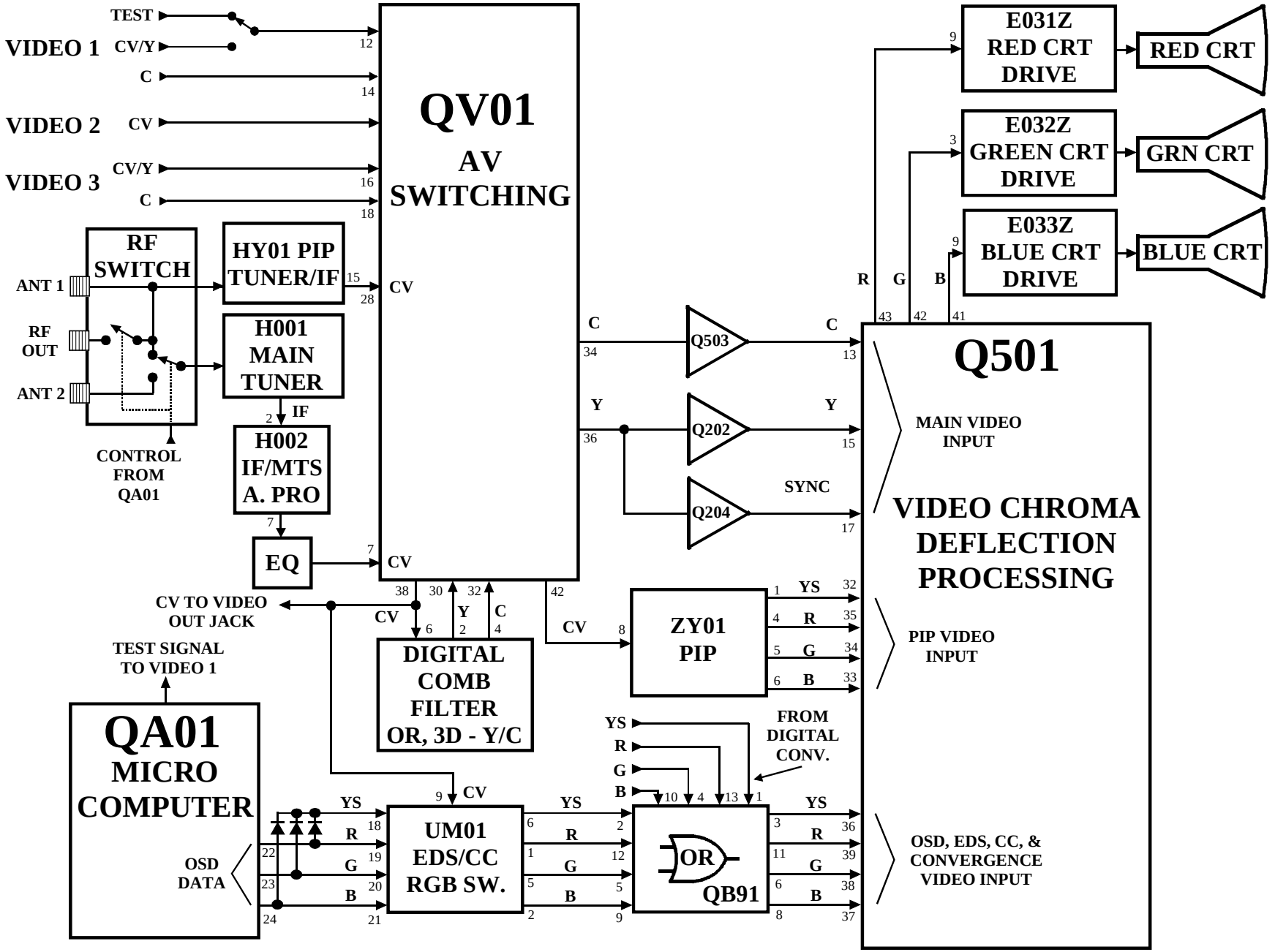


Figure 1-7 Video Signal Flow Block Diagram

9. AUDIO SIGNAL FLOW BLOCK DIAGRAM

Audio Signal Flow

Audio signals are applied to the AV Switcher from the three video jacks, H002, and the PIP Tuner, as shown in Figure 1-8. Like the video signal, there must not be a connector in the video 1 jack for the audio test signal to be applied to the AV Switcher. In the TP48E90, PIP audio is applied to the PIP output jack. The main audio signals are applied to the audio output jacks and to the Front Surround circuit, the DSP/Dolby circuit, or the Dolby Pro Logic circuit. Afterprocessing, the left and right audio signals are applied to the audio processor in H002 where the volume, balance, treble, and bass are controlled. Next, the audio signals are amplified by QS101 and applied to the variable output jacks, and Q601. If the sub bass system (SBS) is selected, a signal is mixed with the left and right signals just before Q601 to increase the signals bass response. In TP55E80/81 and TP61E80 models, the jumper is removed so a center signal can be switched in to replace the main left and right signals. The amplified left and right audio signals are applied to the internal/external speaker switch and routed to the desired speakers.

Sets equipped with Dolby or Dolby Pro Logic have a surround audio signal that is sent to the audio processor in H002 from the Dolby circuit. The surround signal is then sent to the rear amplifier, Q641, amplified, and applied to the rear speakers. In the TP48E90 the surround signal is routed through an amplifier in Q690 before it is applied to Q641. Also, the TP48E90 is equipped with Dolby Pro Logic, and has a center channel. The center channel is amplified by the Center Amplifier, Q621, and applied to the front speakers through the internal/external speaker switch.

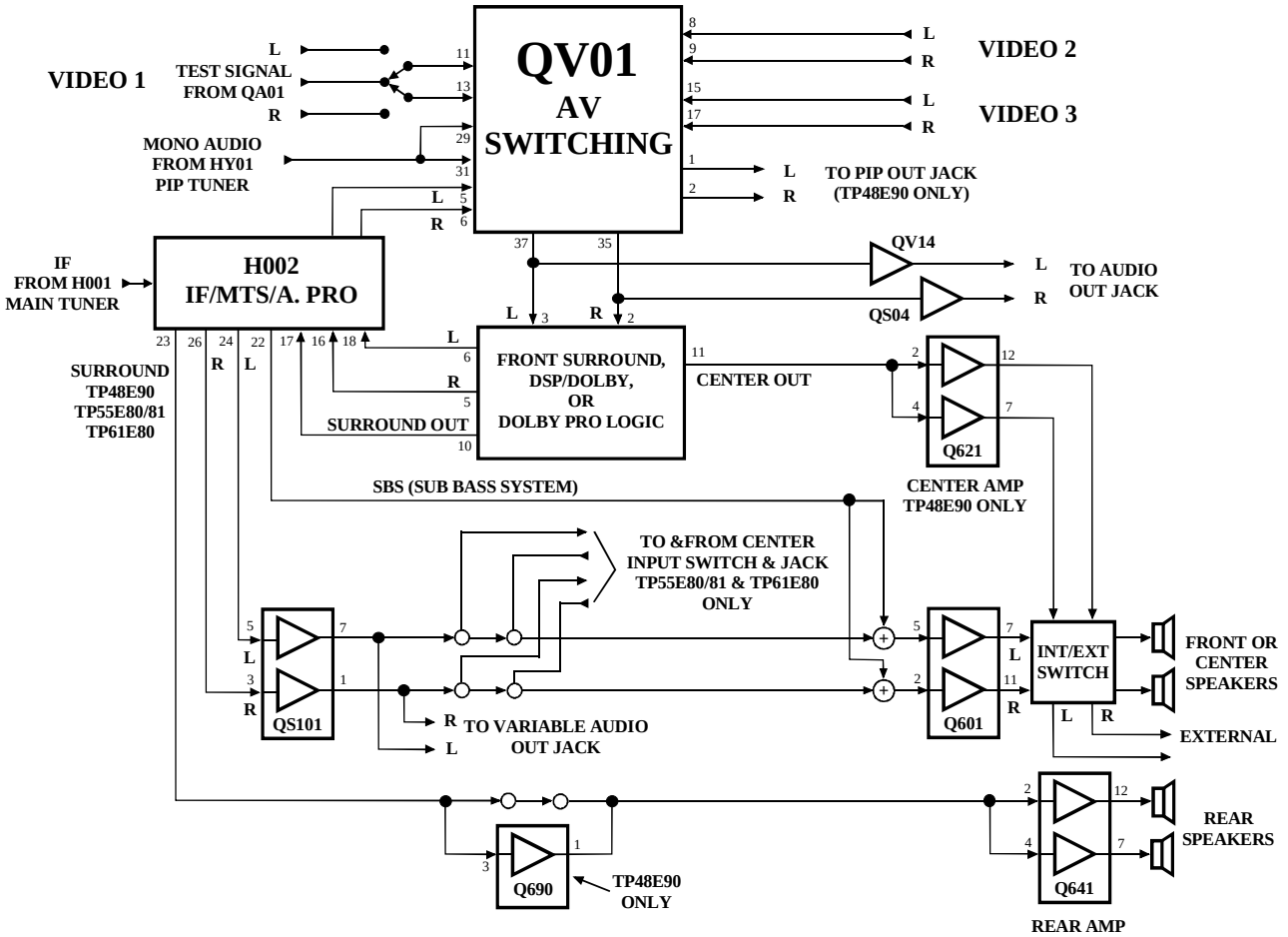


Figure 1-8 Audio Signal Flow Block Diagram

10. POWER SUPPLY AND PROTECTION BLOCK DIAGRAM

The E model PTVs actually have three separate power supplies as shown in Figure 1-9. These supplies consist of the Standby Supply, the Main Switch Mode Supply, and the Sub Switch Mode Supply. The Standby Supply provides the 5 VDC needed to run the microcomputer and the customer interface controls, such as the key pad and the IR receiver. When the set is turned on, the switch closes to activate the two switch mode supplies and provide the numerous DC voltages needed to operate the set.

The Control/Protection circuit, Z801, has two functions. The first is to regulate the Main Switch Mode Supply, and the second is to monitor over current, over voltage, and under voltage sensors throughout the set. If any one of these sensors activates the protection circuit, Z801 turns off the switch powering the two switch mode supplies thus turning off the set. If this occurs, a red LED on the front panel flashes at half second intervals, and the set must be unplugged to reset Z801.

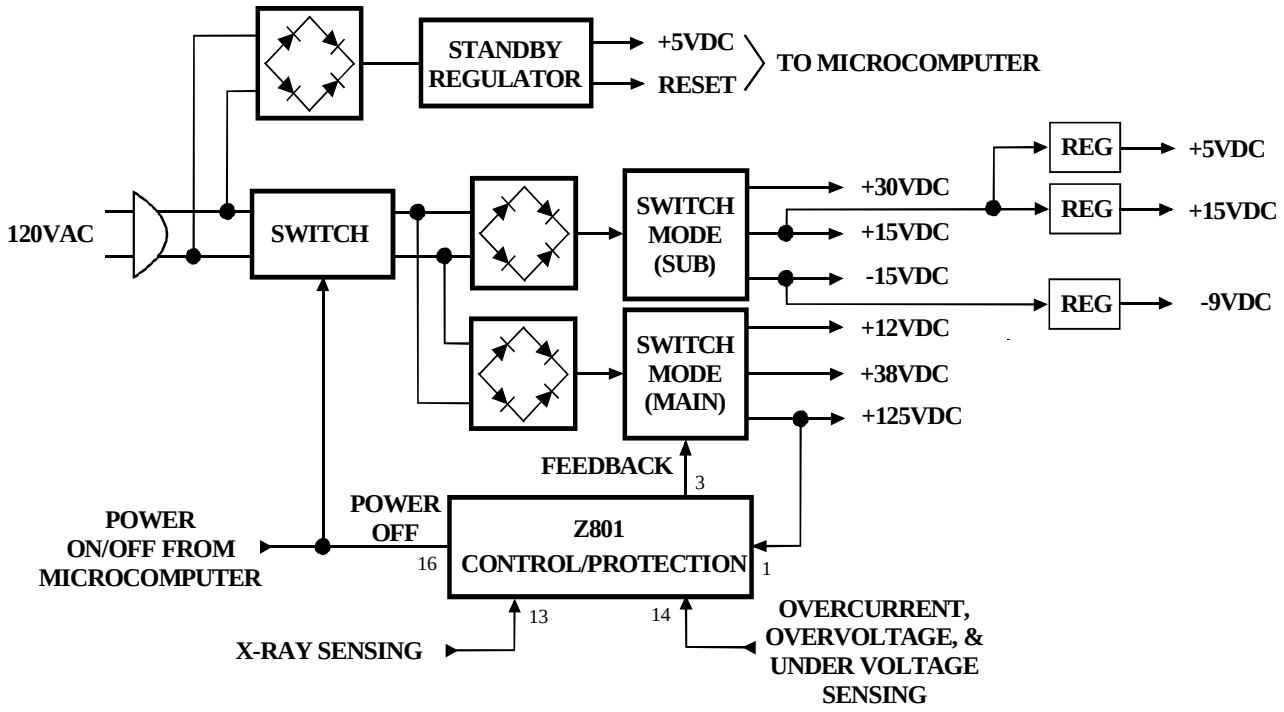


Figure 1-9 Power Supply/Protection Block Diagram

11. HORIZONTAL AND VERTICAL DEFLECTION

Deflection circuitry in the E model PTV's is rather straight forward as show in Figure 1-10. The horizontal pulse from Q501 drives the horizontal drive circuitry, which in turn drives the Horizontal Yokes and the Flyback Transformer, T461. Numerous low voltage DC supplies are produced by the Flyback, as well as the high voltages for the anode, focus, and screen drives. To prevent excessive high voltages, a sample X-Ray protection voltage is monitored by the over voltage protection circuits.

Vertical drive (VD) is applied to the DPC circuit, U421, to correct any distortions before it's sent to the Vertical Drive circuit, Q301. Then the vertical drive circuit supplies the signals required by the yokes for deflection.

To enhance horizontal transitions between dark and light areas of the picture, a Velocity Scan Modulation (VSM) signal is produced by Q501. This signal is sent to the SVM circuit, E036Z, which in turn drives the SVM coils on the CRTs.

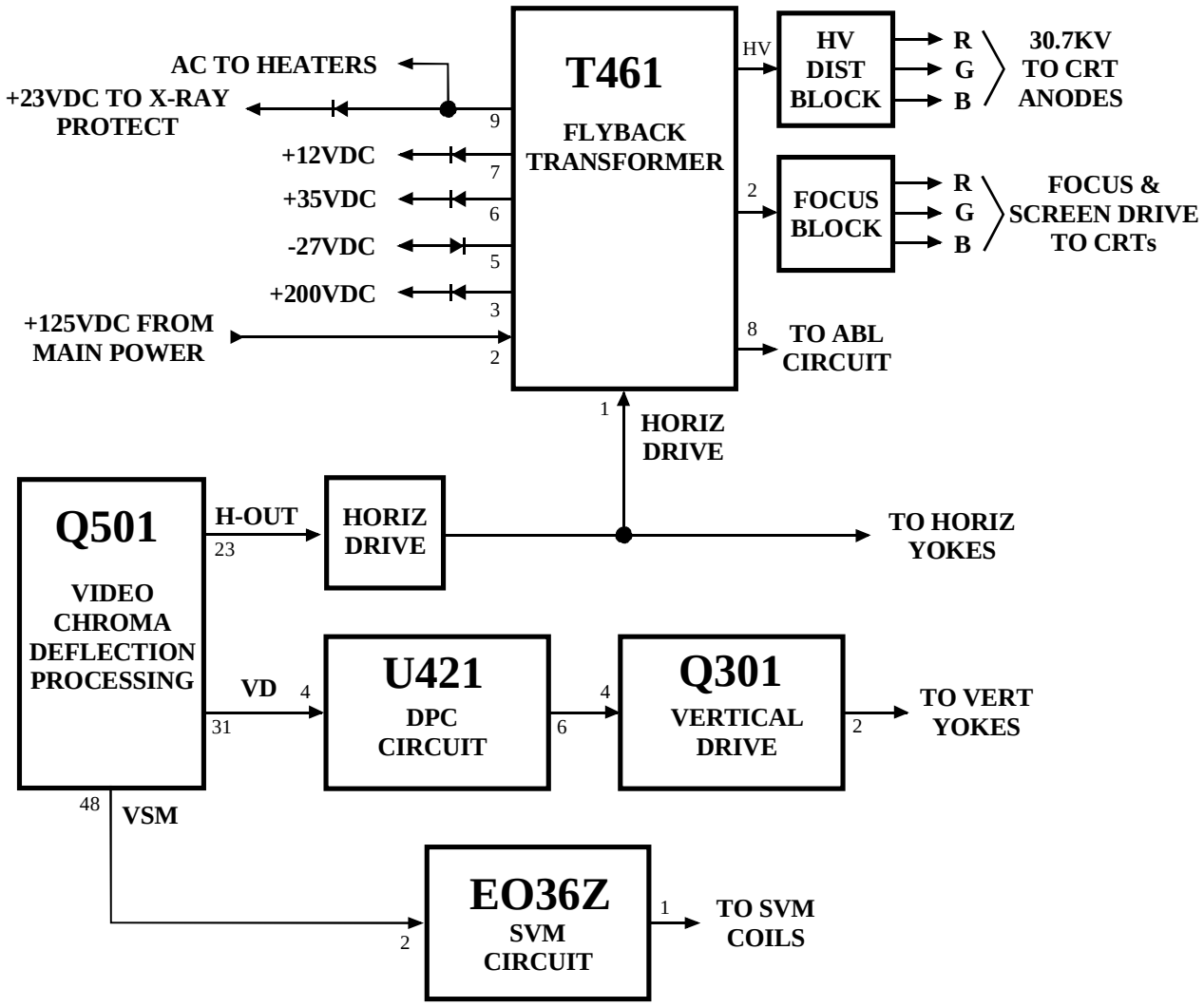


Figure 1-10 Horizontal and Vertical Deflection Block Diagram

12. I²C Communications

The TG-1 chassis uses I²C data communications to control all customer features and most of the service adjustments that where previously done with discrete devices, refer to Figure 1-11. All communications are controlled by the Microcomputer, QA01 through serial data lines (SDA) and serial clock lines (SCL). Memory settings for customer controls and service adjustments (except convergence data) are stored in the E²PROM Memory, QA02, and communicated to QA01 by the SCL0 and SDA0 lines. Data and clock lines SDA1 and SCL1 communicate with most of the circuits in the set. However, there are three plug in circuits where the data and clock signals are buffered by QB90 to provide isolation.

All customer functions and most services adjustments are implemented through the Key Pad and the Remote Sensor. The RMT OUT signal on the microcomputer drives the IR Transmitter on the front panel, but it's only used in the manufacturing process. Figure 1-12 shows the Service Registers and their default values used for making adjustments in the set.

REG	ADJUSTMENT	PRESET
RCUT	RED CUTOFF	40
GCUT	GREEN CUTOFF	40
BCUT	BLUE CUTOFF	40
RDRV	RED DRIVE	40
BDRV	BLUE DRIVE	40
CNTX	SUB-CONTRAST MAX	7F
BRTC	SUB-BRIGHT CENTER	80
COLC	SUB-COLOR CENTER	50
TNTC	SUB-TINT CENTER	40
SCOL	SAP-COLOR	15
SCNT	SUB-CONTRAST	15
HPOS	HORIZ. POSITION	16
VPOS	VERTICAL POSITION	00
HIT	VERTICAL HEIGHT	D1
GMPS	GMPS	00
VLIN	VERTICAL LINEARITY	12
VSC	A-S CORRECTION	08
VPS	VERTICAL SHIFT	15
VCP	V-COMPENSATION	03
WID	PICTURE WIDTH	25
TRAP	TRAPEZIUM	10
HCP	H-COMPENSATION	02
VFC	V-F CORRECTION	0F
STRH	HORIZ. START POSITION	82

Figure 1-12 Service Register Default Values

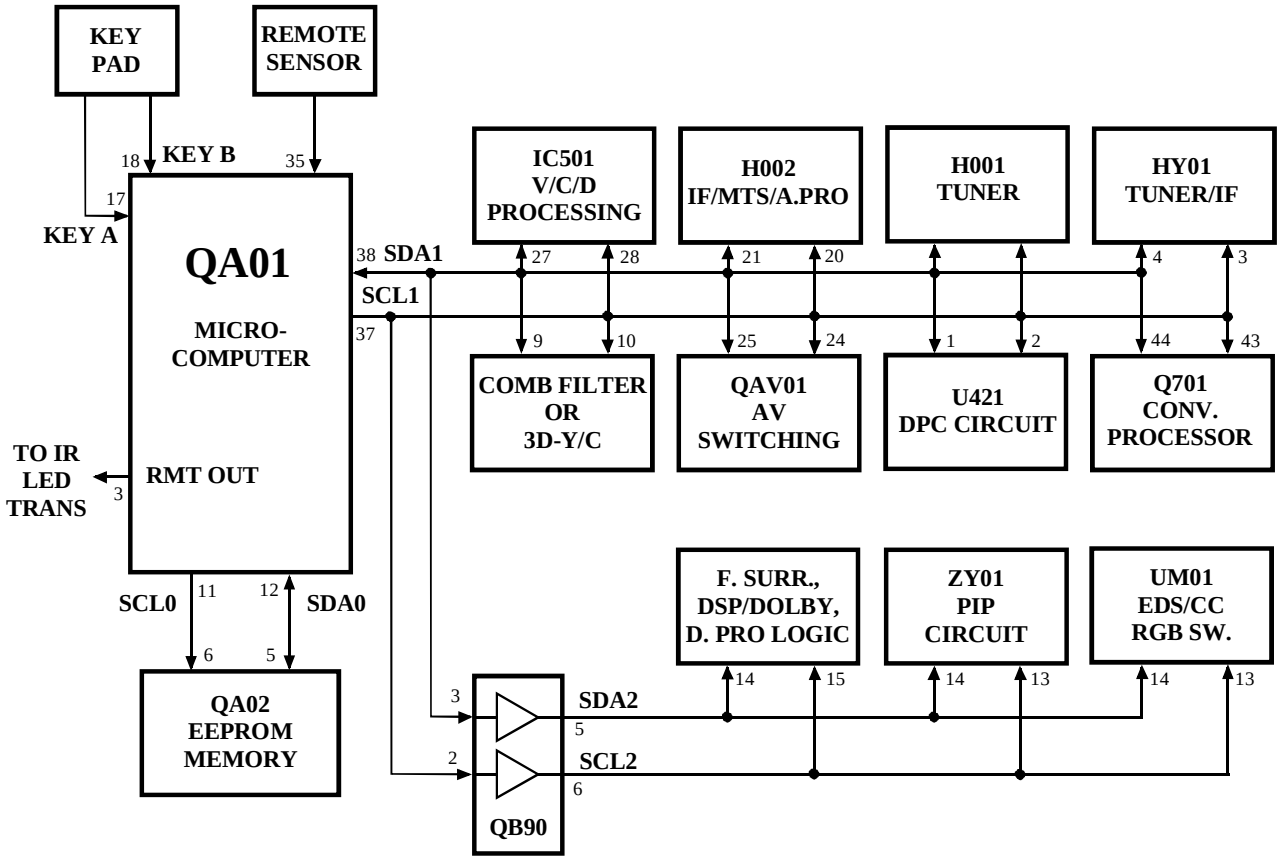


Figure 1-11 I²C Communication Block Diagram

13. Digital Convergence

The TG-1 model PTV's are equipped with a new digital convergence circuit shown in Figure 1-13. This circuit allows servicers to set the convergence with the remote control. Q701, the Digital Convergence Processor aligns the convergence from data received from the remote, and saves the settings in the E^2PROM, Q713. The digital convergence signals are converted to analog by the D/A Converters Q703, Q704, and Q705. Then they are amplified by the pre amps (Q715, Q717, & Q719) and power amps (Q751 & Q751) before being applied to the convergence yokes. The Power Amps Q752 and Q751 dissipate allot of heat because of their current draw, so the supplies to these amps have a number of sensors for over current conditions. Most of the convergence circuit is on a shielded board, but the power amps are easily accessible for service.

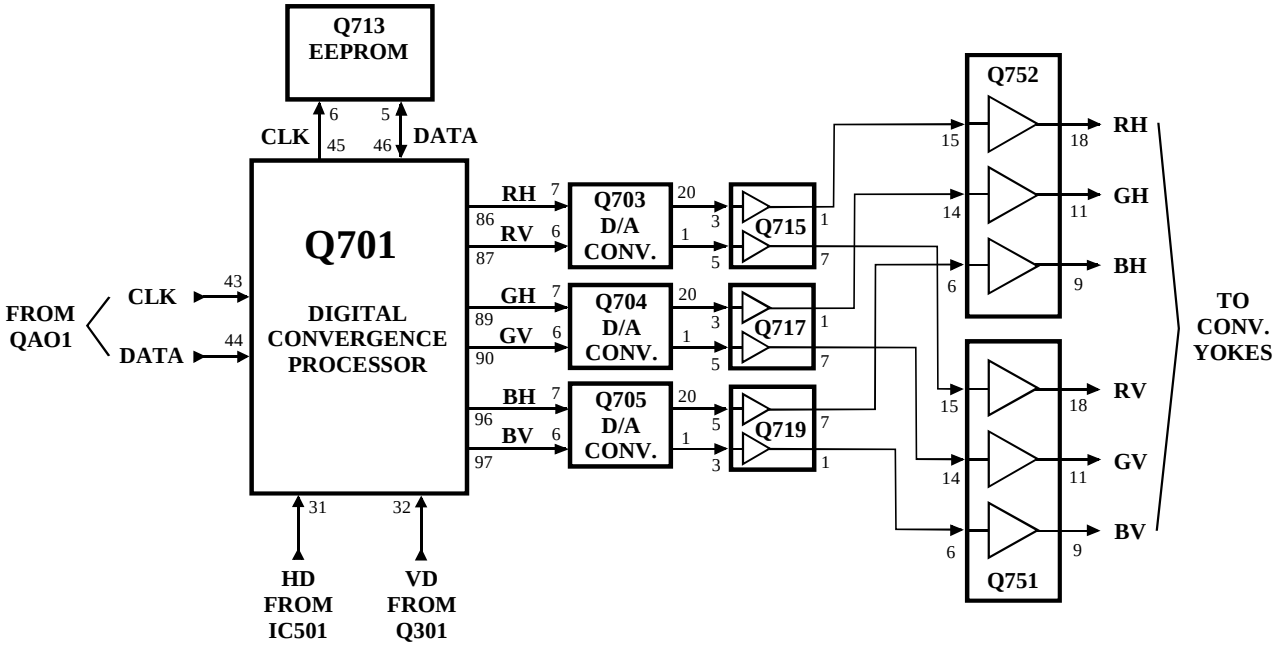


Figure 1-13 Convergence Block Diagram

LAB 1

BASIC OPERATION AND UNIT UNDERSTANDING

As a servicer, it is important now, more than ever, to fully understand the operation and functions of a television set before proceeding with a repair. This is because many of the problems encountered by a customer today can be caused by an incorrect menu selection or improper setup.

Therefore, the purpose of this lab is to familiarize you with menus and features of the television from the customer's point of view.

SECTION ONE
BASIC OPERATION

1. Verify that the unit is connected to an AC supply, and that a signal is connected to the ANT 1 input. While verifying signal connections, take time to examine all of the inputs on the rear and front (behind door) of the unit.

2. Turn on the set with the remote control and tune to an active channel. Refer to page 9 of the service manual provided and familiarize yourself with all of the keys on the remote paying, particular attention to the following keys:

   - ☐ **EDS**
   - ☐ **TIMER**
   - ☐ **PIP Functions**

Open the bottom door on the remote control by sliding it down. Try each key starting with the upper row. Each of these buttons brings up another menu and/or sub-menus.

3. In the ***Picture Menu***, What is Color Temperature?

   _____

   _____

4. In the ***Audio Menu***, Where can the speakers be turned off by the user?

   _____

   _____

5. In the ***Setup Menu***, What is Favorite Channel?, What is Channel Lock?

   _____

   _____

6. Refer to page 16 of the Service Manual and perform the *User Convergence Adjustments.* How is this different from previous Toshiba PJTVs?

_____

_____

7. In the ***Option Menu***, How many different languages are there? What are they used for? What is Channel Label Used for?

_____

_____

_____

_____

NOTES:

_____

_____

_____

_____

_____

_____

SECTION TWO
DISASSEMBLY & SERVICE POSITION

Follow the procedure listed below to gain access to the tubes and circuit boards.

1. Remove the speaker grill by holding the sides and pulling straight out.

2. Take out the four screws holding the plastic shield in place. Then remove the shield.

3. Remove the control wires from the holder on the metal shield in front of the CRTs.

4. Remove the 4 screws holding the metal shield in place. The shield is notched, so slide it to the right then down to remove it.

5. Remove the two screws holding the front control panel. Then release the tabs on either side and let it hang down out of the way.

6. Remove the 4 screws holding the bottom of the screen. Then lift up on the top of the screen and pull it away from the cabinet.

7. Remove the 5 screws holding the back panel. Then remove the back panel.
8. Reattach the control panel to the light box.
9. Remove the six screws on the front of the light box.
10. Remove the three screws on the back of the cabinet.
11. Remove the one screw holding the back of the light box to the cabinet.
12. From the front of the set, lift the light box up just a little, and pull it towards you.
13. Pull the light box all the way out of the cabinet and turn it on its side.

CAUTION: the light box weighs about 85 pounds, so get help if you need it.

SECTION THREE
IDENTIFICATION

1. Identify each of the board assemblies and note their locations. Use Figure 1-5 to help you identify the various boards.

   - ☐ **Convergence/Output/Power Board**
   - ☐ **Deflection/Power Board**
   - ☐ **Main PCB**
   - ☐ **Front Surround Board**
   - ☐ **Digital Comb Filter Board**
   - ☐ **PIP Board**
   - ☐ **EDS/CC Board**

2. Is there a convergence board in this unit?
   If so, where?

   _____

   _____

3. How does this convergence setup differ from previous models?

   _____

   _____

4. Examine the Flyback and HV lead assemblies. What is different about this area from earlier models?

   _____

   _____

5. Is it possible for one technician to perform a service call on this type of unit?

   _____

   _____

6. Put the lightbox in the cabinet, but don't screw it in. Then replace the screen and control panel. Use a few screws to hold the screen and control panel in place.

SUMMARY

In this lab, the operation and function of the unit was determined, and the unit was set up for service on the bench. Common user type problems in addition to overall serviceability was also discussed.

END OF LAB 1

LAB 2

TEST SIGNALS, SELF DIAGNOSTICS, & SERVICE REGISTERS

OBJECTIVES: After completing this lab you will be able to:

1. Enter and exit the set's internal video and audio test signals.
2. Use the test signals for troubleshooting.
3. Use the set's self diagnostic feature.
4. Make adjustments in the set with the service registers via the remote control.

SECTION ONE
VIDEO TEST SIGNALS

1. Verify that the unit is connected to an AC supply, and that a signal is connected to the ANT 1 input.
2. Enter the service mode by pressing mute on the remote. Press and hold mute a second time while pressing menu on the control panel. An S appears in the upper right corner of the screen indicating that the set is in the service mode. Press menu and the RCUT register appears in the upper left corner of the screen.
3. Push the TV/VIDEO button on the remote once to enter the internal test pattern mode. The screen should be red.
4. Slowly cycle through the test signals with the TV/VIDEO button until the white cross hairs on a black background appear. (If the TV/VIDEO button is pushed in rapid succession, the set will jump out of the test signal mode to one of the inputs - ANT 1, VIDEO 1, VIDEO 2, or VIDEO 3. The set is still in the service mode, so if this occurs, push the menu button then the TV/ VIDEO button to get back into the test signal mode.)
5. Plug a video cable into the VIDEO 1 input jack (make sure the other end of the cable is not plugged into a video source)
6. What happened to the cross hairs?

   _____

   _____

7. If something did happen to the cross hairs, why did it happen?

   _____

   _____

8. Is there video on the screen?

_____

_____

9. If there is video on the screen, where does it come from?

_____

_____

10. Unplug the video cable.

SECTION TWO
AUDIO TEST SIGNALS

1. Push the 8 button on the remote to activate the audio test signal. (**NOTE:** The internal test pattern mode must be activated for this feature to work.)

2. Push the mute button twice. Now you can control the volume of the signal.

3. Select AUD on the remote control.

4. Select BALANCE and adjust it from left to right with the + and - buttons.

5. Select SPEAKERS and turn them off then on. (**NOTE:** The speakers are turned off at Q601, refer to Figure 1-8, while the volume, bass, treble, and balance are controlled in H002. This means you can troubleshoot most of the audio system with the speakers off.)

6. Plug an audio cable into the left AUDIO 1 input jack (make sure the other end of the cable is not plugged into an audio source)

7. What happened to audio?

_____

_____

8. If something did happen to the audio, why did it happen?

_____

_____

9. Push the 8 button to turn off the audio test signal.

10. Cycle the video test signals back to the ANT 1 signal with the TV/VIDEO button.

SECTION THREE
SELF DIAGNOSTICS

1. Push the 9 button to activate the self diagnostic feature.
2. What does POWER indicate?

   _____

   _____

3. What does BUS LINE indicate?

   _____

   _____

4. What does BUS CONT indicate?

   _____

   _____

5. What does BLOCK indicate?

   _____

   _____

6. Push the EXIT button to exit the self diagnostic feature.
7. Select the VIDEO 1 input with the TV/VIDEO button. (Make sure there is no signal applied to VIDEO 1)
8. Push MENU on the control panel to display the registers.
9. Push 9 to activate the self diagnostic feature.
10. Is the display different from the previous display. _____
11. If it is, explain why.

    _____

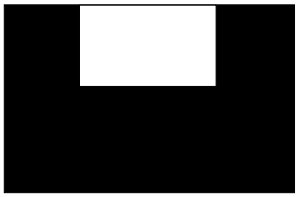
    _____

12. Push the EXIT button to exit the self diagnostic feature.
13. Push MENU on the control panel to display the registers.

SECTION FOUR
SERVICE REGISTERS

NOTE: In each of the following exercises write down the register's value before adjusting it. Then restore the register to its original value before proceeding to the next exercise.

1. Enter the internal test pattern mode and select the test signal that has a white window in the upper center of a black background as shown below.



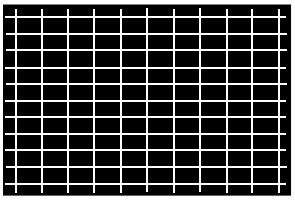
2. Increase the RCUT register value and describe its effect on the picture.

   RCUT_____

   _____

   _____

3. Change the test signal to the white on black cross hatch pattern as shown below.



4. Select the HPOS register and vary its value between 00 and 1F. Describe its effect on the picture. What happens if you increase the register to 20?

   HPOS_____

   _____

   _____

5. Select the VPOS register and vary its value between 00 and 07. Describe its effect on the picture. What happens if you increase the register to 08?

   VPOS_____

   _____

   _____

6. Select the HIT register and vary its value 5 steps above and below the recorded value. Describe its effect on the picture.

   HIT_____

   _____

   _____

7. Select the VLIN register and vary its value 8 steps above and below the recorded value. Describe its effect on the picture.

   VLIN_____

   _____

   _____

8. Select the WID register and vary its value 8 steps above and below the recorded value. Describe its effect on the picture.

   WID_____

   _____

   _____

9. Select the STRH register and vary its value 8 steps above and below the recorded value. Describe its effect on the picture.

   STRH_____

   _____

   _____

SUMMARY

Now that you have completed Lab 2, you should be able to use the internal video and audio test signals, the self diagnostic feature, and the service registers for making adjustments.

END OF LAB 2

SECTION II
TUNER, IF/MTS/S.PRO MODULE

1. CIRCUIT BLOCK

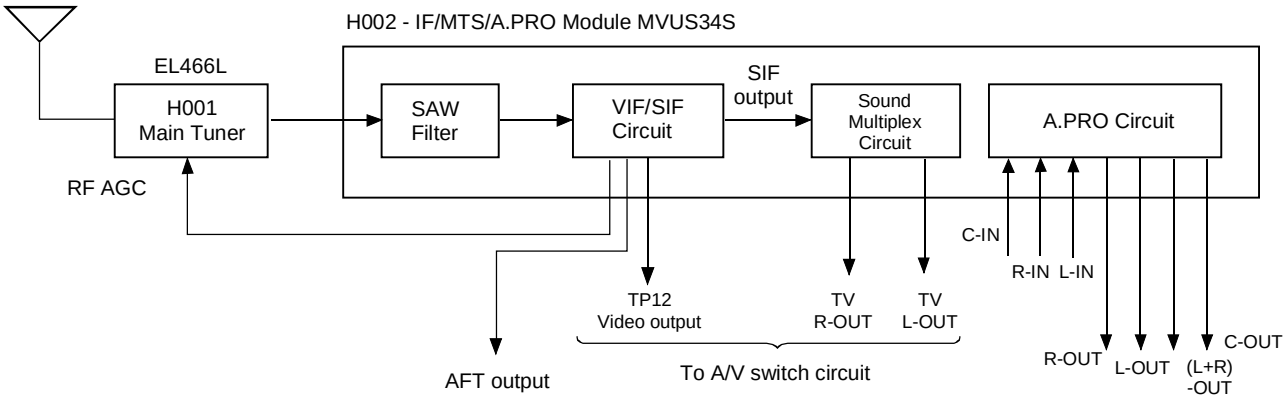


Fig. 2-1 Block diagram

1-1. Outline

(1) RF signals sent from an antenna are converted into intermediate frequency band signals (video: 45.75 MHz, audio: 41.25 MHz) in the tuner. (Hereafter, these signals are called IF signals.)
(2) The IF signals are band-limited in passing through a SAW filter.
(3) The IF signals band-limited are detected in the VIF circuit to develop video and AFT signals.
(4) The band-limited IF signals are detected in the SIF circuit and the detected output is demodulated by the audio multiplexer, developing R and L channel outputs. These outputs are fed to the A/V switch circuit.
(5) A sound processor (S.PRO.) is provided.

1-2. Major Features

(1) The VIF/SIF circuit is fabricated into a small module by using chip parts considerably.
(2) As the tuner, EL466L that which contains an integrated PLL circuit is employed.
(3) Wide band double SAW filter F1802R used.
(4) FS (frequency synthesizer) type channel selection system employed.
(5) VIF/SIF circuit uses PLL sync detection system to improve performances shown below:
  • Telop buzz in video over modulation
  • DP, DG characteristics (video high-fidelity reproduction)
  • Cross color characteristic (coloring phenomenon at color less high frequency signal objects)
(6) HIC SBX1637A-22 is used in the audio multiplexer circuit to minimize the size with increased performance.
(7) As a sound control processor, TA1217N is used. I^2C-bus data control the DAC inside the IC to perform switching of the audio multiplexer modes.

1-3. Audio Multiplex Demodulation Circuit

The sound multiplex composite signal FM-detected in the PIF circuit enters pin 12 of HIC (hybrid IC) in passing through the separation adjustment VR RV2 and amplified. After the amplification, the signal is split into two: one enters a de-emphasis circuit, and only the main signal with the L-R signal and a SAP signal removed enters the matrix circuit. At the same time, the other passes through various filters and trap circuits, and the L-R signal is AM-demodulated, and the SAP is FM-demodulated.

Then, both are fed to the matrix circuit. At the same time, each of the stereo pilot signal fH and the SAP pilot signal 5fH is also demodulated to obtain an identification voltage. With the identification voltage thus obtained and the user control voltage are used to control the matrix.

The audio signals obtained by demodulating the sound multiplex signal develop at pin 10 and 11 of HIC and develop the terminals of 12 and 14 of the module.

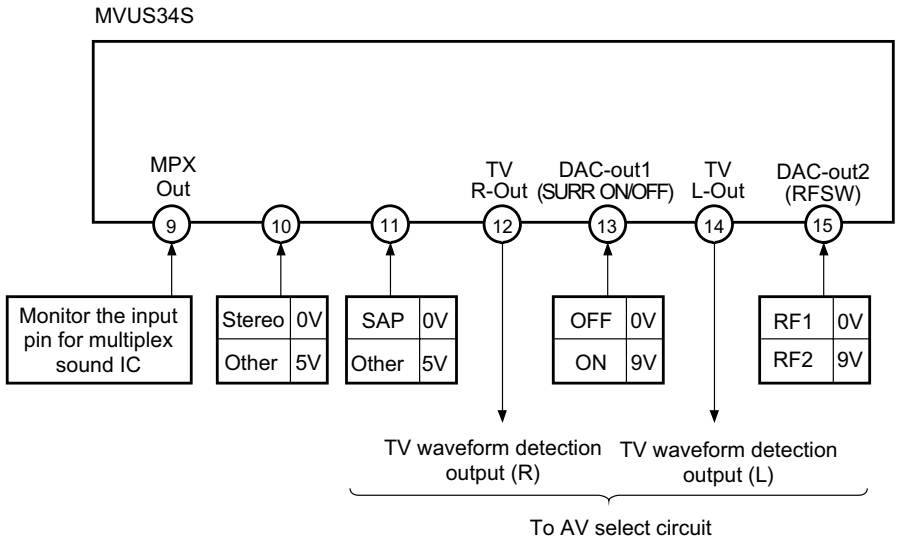


Fig. 2-2 Block diagram of MVUS34S

Table 2-1 Matrix for broadcasting conditions and reception mode

Broad-casted	Switching mode	Output		OSD display	
		12 pin (R)	14 pin (L)	Stereo	SAP
Stereo	STE	R	L	Y	N
	SAP	R	L	Y	N
	MONO	L+R	L+R	Y	N
Mono	STE	L+R	L+R	N	N
	SAP	L+R	L+R	N	N
	MONO	L+R	L+R	N	N
Stereo + SAP	STE	R	L	Y	Y
	SAP	SAP	SAP	Y	Y
	MONO	L+R	L+R	Y	Y
Mono + SAP	STE	L+R	L+R	N	Y
	SAP	SAP	SAP	N	Y
	MONO	L+R	L+R	N	Y

Note:
Of the mode selection voltages, switching voltages for STE, SAP, MONO do not output outside the module.
They are used inside the module to control the BUS.

1-4. A.PRO Section (Audio Processor)

The S.PRO section has following functions.

(1) Woofer processing (L+R output)
(2) High band, low band, balance control
(3) Sound volume control, cyclone level control
(4) Cyclone ON/OFF

All these processing are carried out according to the BUS signals sent from a microcomputer.

Fig. 2-3 shows a block diagram of the A.PRO IC.

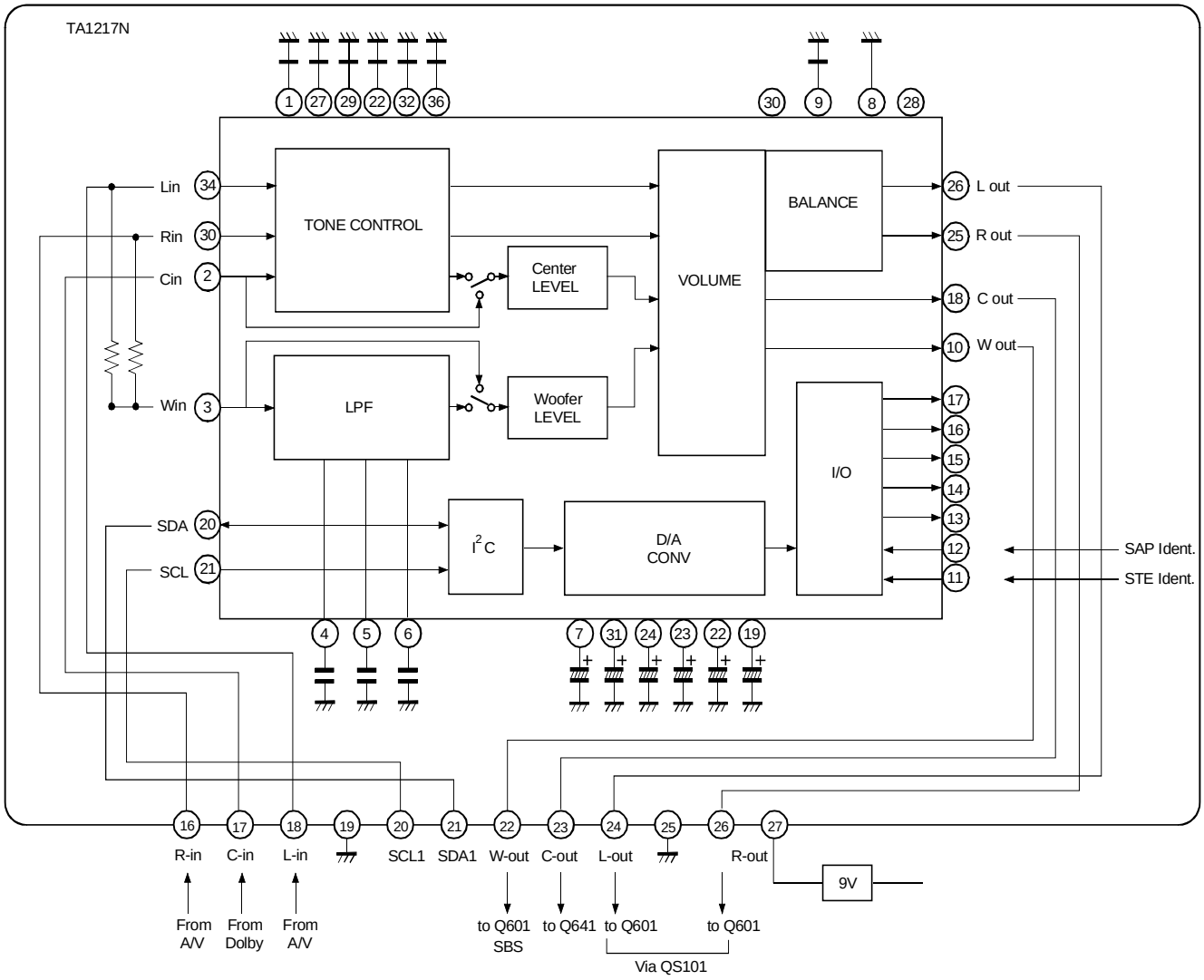


Fig. 2-3 A.PRO block diagram

Configuration of the audio circuit and signal flow are given in Fig. 2-4

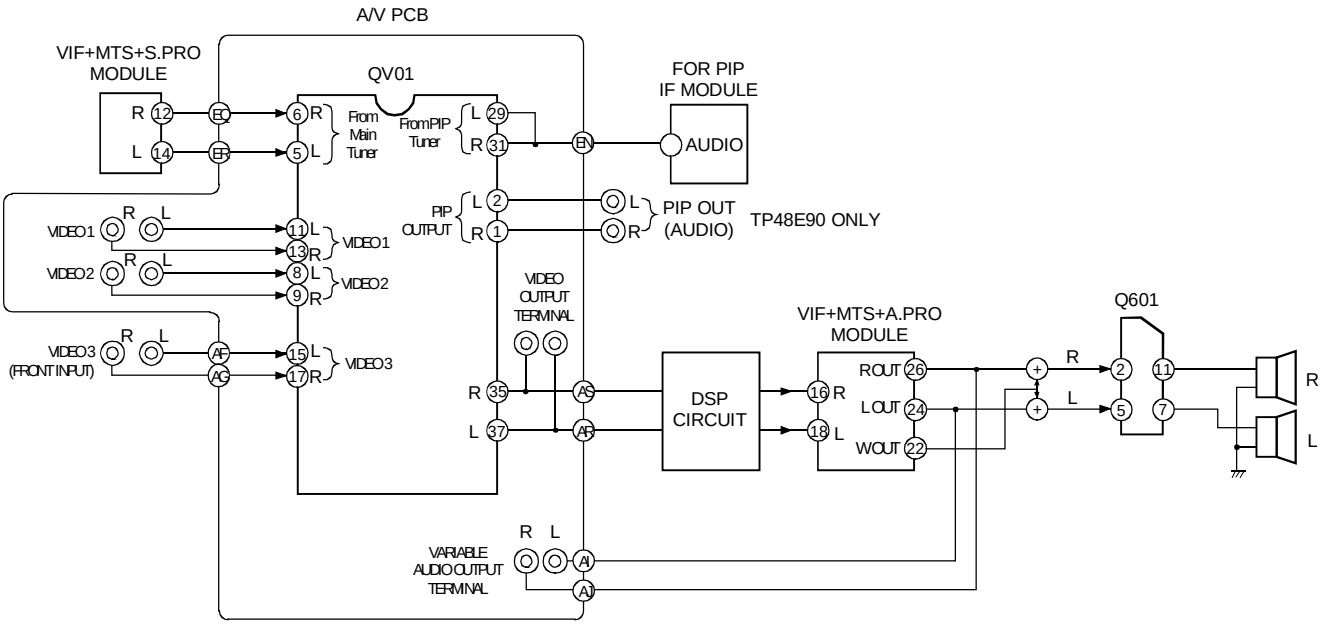


Fig. 2-4

2. PIP TUNER

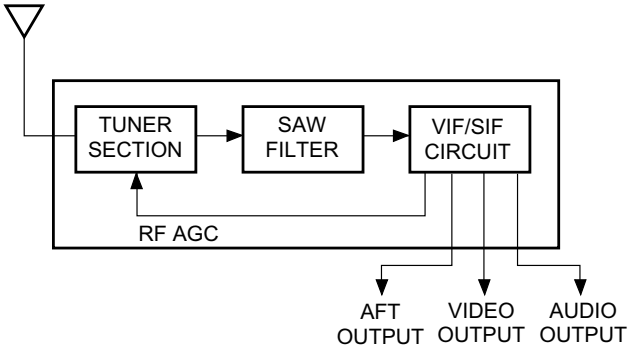


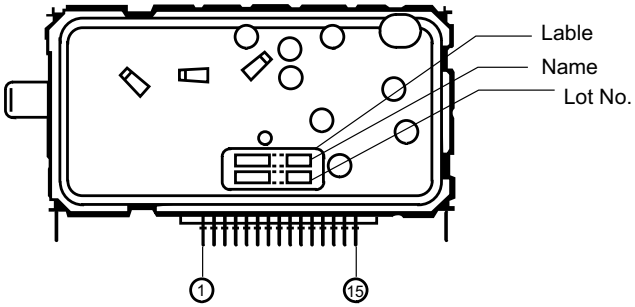
Fig. 2-5

2-1. Outline

The PIP tuner (EL922L) consists of a tuner and an IF block integrated into one unit. The tuner receives RF signals induced on an antenna and develops an AFT output, video output, and audio output.

The tuner has receive channels of 181 as in the tuner for the main screen and it is also controlled through the I2C-bus.

As the IC for the IF, a PLL complete sync detection plus audio inter carrier system are employed.



Terminal No.	Name
1	NC
2	32V
3	S-CLOCK
4	S-DATA
5	NC
6	ADDRESS
7	5V
8	RF AGC
9	9V
10	AUDIO
11	GND
12	AFT
13	NC
14	GND
15	VIDEO

Fig. 2-6 Tuner terminal layout

SECTION III
CHANNEL SELECTION CIRCUIT

1. OUTLINE OF CHANNEL SELECTION CIRCUIT SYSTEM

The channel selection circuit in the N5SS chassis employs a bus system which performs central control by connecting a channel selection microcomputer to a control IC in each circuit block through control lines called a bus. This bus system herin referred to as the I^2C bus system (two line bus) is licensed from and was developed by Philips.

Integrated circuits controlled by the I^2C bus system are : QN06 for audio signal processing, Q501 for V/C/D signal processing , QV01 for A/V switching, QA02 for non volatile memory, main and sub U/V tuners (H001, HY01), Q302 for deflection distortion correction, QY04 for PIP signal processing, QM01 for DSP, and Q701 for closed caption control.

Differences from the previous N5SS chassis include;

1. On-screen display generation now originates within ICA01. A separate IC is no longer used.
2. The microcomputer does not perform the closed caption function, but instead controls a separate IC for this purpose.
3. The system uses two sperate channels of I^2C bus. One of these is dedicated for communication with the non-volatile memory.

2. OPERATION OF CHANNEL SELECTION CIRCUIT

An 8 bit, Toshiba microcomputer (series TLCS-870) is used within the television as ICA01. Part number TMP87CS38N-3152 or similar is employed.
With this microcomputer, each IC and circuit shown below are controlled.

(1) CONTROL OF AUDIO SIGNAL PROCESS IC (QN06 Toshiba TA1217N)
- Adjustments for volume, treble, bass and balance
- Selection between surround mode and DSP mode, and level adjustment
- Level adjustment of BAZOOKA (Sub-Bass) system
- Audio muting during channel selection or no signal reception.

(2) CONTROL OF VIDEO/CHROMA/DEF SIGNAL PROCESS IC (Q501 Toshiba TA1222N)
- Adjustments for uni-color, brightness, tint, color gain, sharpness and PIP uni-color
- Setting of adjustment memory values for sub-brightness, sub-color and sub-tint, etc.
- Setting of memory values for video parameters such as white balance (RGB cutoff, GB drive) and g correction, etc.
- Setting of video parameters of video modes (Standard, Movie, Memory)

(3) CONTROL OF A/V SWITCH IC (QV01 Toshiba TA1218N)
- Preforms source switching for main screen and sub screen
- Performs source switching for TV and up to three video inputs

(4) CONTROL OF NON-VOLATILE MEMORY IC (QA02 Microchip 24LC08BI/P)
- Memorizes data for video and audio signal adjustment values, volume and woofer adjustment values, external input status, etc.
- Memorizes adjustment data for white balance (RGB cutoff, GB drive), sub-brightness, sub color, sub tint, etc.
- Memorizes deflection distortion correction value data adjusted for each unit.

(5) CONTROL OF U/V TUNER UNIT (H001 Matsushita EL466L, HY01 Toshiba EL922L)
- A desired channel can be tuned by transferring a channel selection frequency data (divided ratio data) to the I^2C bus type frequency synthesizer equipped in the tuner, and by setting a band switch which selects the UHF or VHF band.

(6) CONTROL OF DEFLECTION DISTORTION CORRECTION IC (Q302 Toshiba TA8859P)
- Sets adjustment memory value for vertical amplitude, linearity, horizontal amplitude, parabola, corner, trapezoid distortion.

(7) CONTROL OF PIP SIGNAL PROCESS IC (QY04 Toshiba TC9083F)
- Controls ON/OFF and position shift of PIP.

(8) CONTROL OF DIGITAL SOUND PROCESSOR IC (QM04 Yamaha YSS238-D)
- Performs mode switching of DSP.

(9) CONTROL OF CLOSED CAPTION/EDS (QM01 Motorola XC144144P)
- Controls Closed Caption/EDS.

3. MICROCOMPUTER

The main Microcomputer TMP87CS38N-3152 has 60k byte of ROM capacity and is equipped with an internal OSD function.

The specification is as follow.

- Type name : TMP87CS38N-3152
- ROM : 60k byte
- RAM : 2k byte
- Processing speed : 0.5μs (at 8MHz with Shortest command)
- Package : 42 pin shrink DIP
- I^2C-BUS : two channels
- PWM : 14 bit x 1, 7 bit x 9
- ADC : 8 bit x 6 (Successive comparison system, Conversion time 20ms)
- OSD

  Character kinds : 256
  Character display : 24 characters x 12 lines
  Character dot : 14 x 18 dots
  Character size : 3 kinds (Selected by line)
  Character color : 8 colors (Selected by character)
  Display position : Horizontal 128 steps, Vertical 256 steps

This microcomputer performs the functions of an Analog to Digital converter, reception of U/V TV and OSD display in one chip.

IIC device controls through I^2C bus. (Timing chart : See fig. 3-1)

- Pin 8, (LED) is used to source current and is an output only.
- For clock oscillation, an 8MHz ceramic oscillator is used.
- I^2C has two channels. One is for EEPROM only.
- A Self diagnosis function which utilizes the ACK function of I^2C is employed
- Function indication is added to service mode.
- Operation by remote control is possible, and controls and adjustments can be made with no physical contact is possible. (Bus connector in the conventional bus chassis is deleted.)
- Substantial self diagnosis function
  (1) B/W composite video signal generating function (inside micon, green crossbar added)
  (2) Generating function of audio signal equivalent to 1kHz (inside micon)
  (3) Detecting function of power protection circuit operation
  (4) Detecting function of abnormality in I^2C bus line
  (5) Functions of LED blink indication and OSD indication
  (6) Block diagnosis function which uses new VCD and AV SW

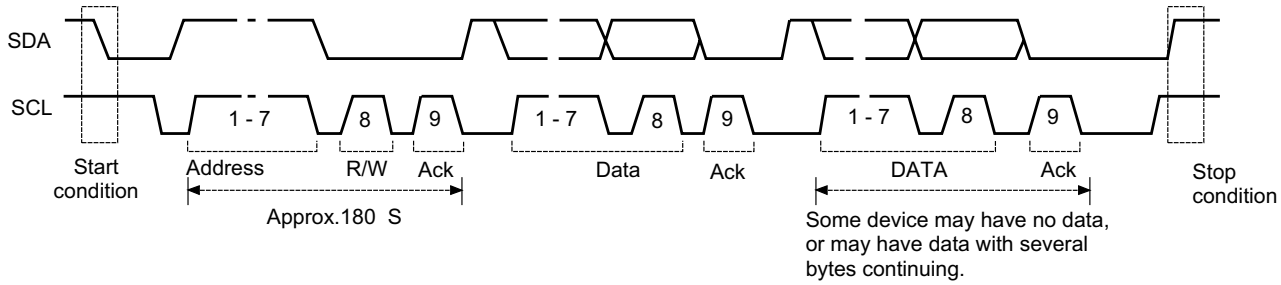


Fig. 3-1

4. MICROCOMPUTER TERMINAL FUNCTION

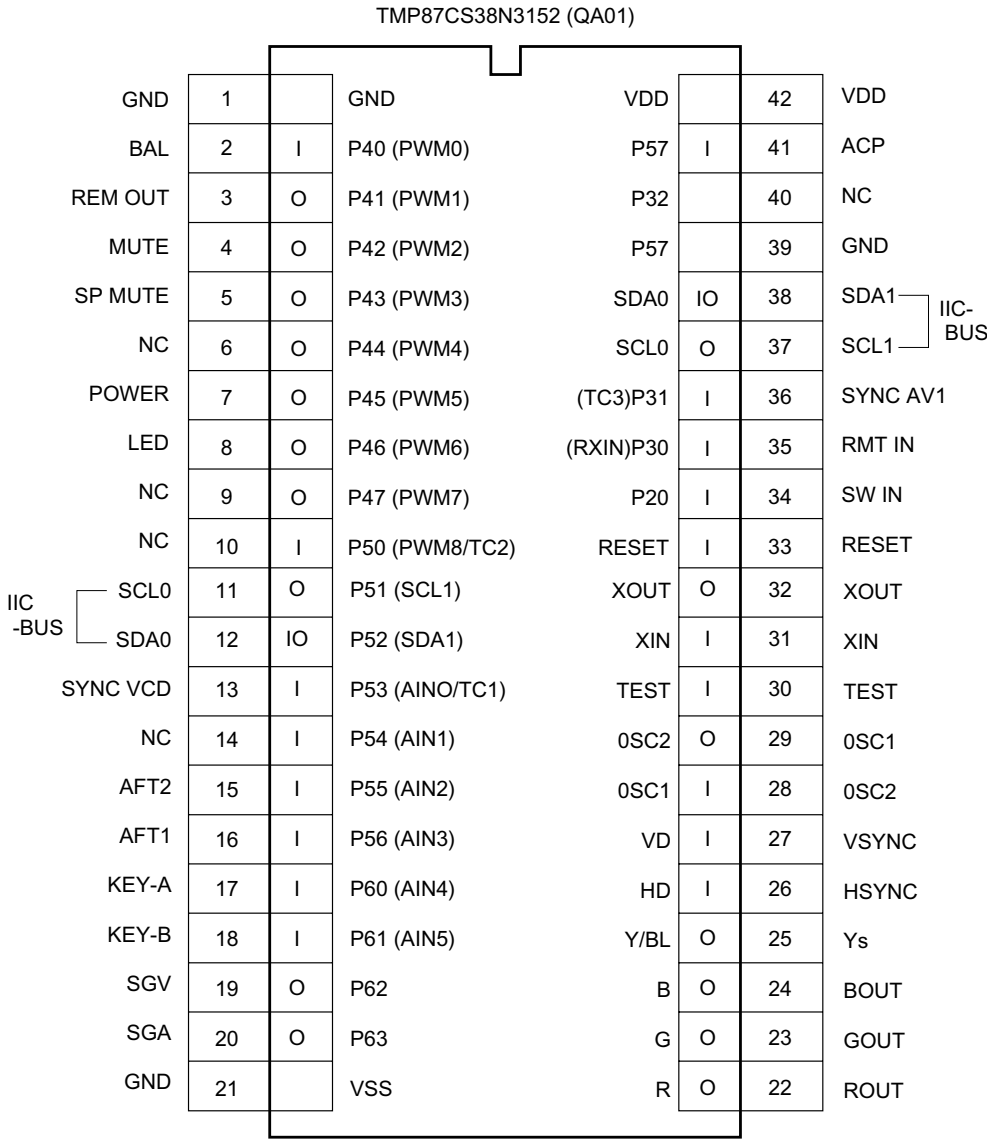


Fig. 3-2

<< MICROCOMPUTER TERMINAL NAME AND OPERATION LOGIC >>

No.	Terminal Name	Function	In/Out	Logic	Remarks
1	GND				0V
2	BAL	INPUT BALANCE	Out	PWM out	
3	REM OUT	REMOTE CONTROL SIGNAL OUT	Out	Remote control output	
4	MUTE	SOUND MUTE OUT	Out	Sound mute output	
5	SP MUTE	SPEAKER MUTE	Out	In muting = H	
6	DEF POW		Out		
7	POWER	POWER ON/OFF OUT	Out	Power control In ON=H	
8	LED	POWER LED OUTPUT	Out	Power LED on-control LED lighting=L	
9	POWER LNB		Out		0V
10	LNB DET		In		0V
11	SCL()	IIC BUS CLOCK OUT	Out	IIC bus clock output 0	
12	SDA()	IIC BUS DATA IN/OUT	In/Out	IIC bus data input/output 0	
13	SYNC VCD	H SYNC INPUT	In	Main picture H. sync signal input	
14					
15	AFT2 IN		In	Sub tuner AFT S-curve input	
16	AFT1	UV MAIN S-CURVE SIGNAL	In	Main tuner AFT S-curve signal input	
17	KEY A	LOCAL KEY INPUT	In	Local key detection: 0 to 5V	
18	KEY B	LOCAL KEY INPUT	In	Local key detection: 0 to 5V	
19	SGV	TEST SIGNAL OUT	Out	Test signal output In normal=L	0V
20	SGA	TEST AUDIO OUT	Out	Test audio output In normal=L	0V
21	VSS	POWER GROUNDING	—	0V: Gounding voltage	0V
22	R	R	Out		At display on:Pulse
23	G	G	Out		At dispaly on:Pulse
24	B	B	Out		At dispaly on:Pulse
25	Y/BL	BL	Out		At dispaly on:Pulse
26	HSYNC		In	HSYNC for OSD display	Pulse
27	VSYNC		In	VSYNC for OSD display	Pulse
28	OSC1	DISPLAY CLOCK	Out	4.5MHz	Pulse
29	OSC2	DISPLAY CLOCK	In		Pulse
30	TEST	TEST MODE	In	GND fixed	0V
31	XIN	SYSTEM CLOCK	In	System clock input	8MHz pulse
32	XOUT	SYSTEM CLOCK	Out	System clock output 8MHz	8MHz pulse
33	RESET	SYSTEM RESET	In	System reset input (In reset=L)	5V
34	SW IN				
35	RMT IN	REMOTE CONTROL SIGNAL INPUT	IN	In remote control pulse input=L	In reception of remote pulse
36	SYNC AV1	HSYNC INPUT	In	External H. sync signal input	Pulse
37	SCL1	IIC BUS CLOCK OUT	Out	IIC bus clock output 1	Pulse
38	SDA1	IIC BUS DATA IN/OUT	In/Out	IIC bus data input/output 1	Pulse
39	GND				0V
40	NC				
41	ACP	NSYNC INPUT	In	AC pulse input	
42	VDD	POWER	—	5V	5V

5. EEPROM (QA02)

EEPROM (Non volatile memory) has function which, in spite of power-off, memorizes the such condition as channel selecting data, last memory status, user control and digital processor data. The capacity of EEPROM is 8k bits. Type name is 24LC08BI/P or ST24C08CB6, and those are the same in pin allocation and function, and are exchangeable each other. This IC controls through I²C bus. The power supply is common to the EEPROM and the main MICOM. Pin function of EEPROM is shown in Fig. 3-3.

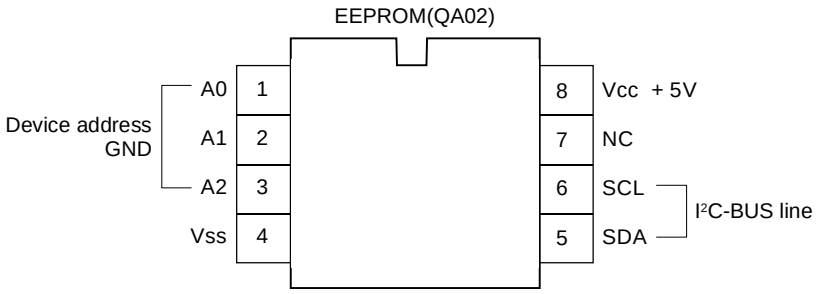


Fig. 3-3

6. ON SCREEN FUNCTION

ON SCREEN FUNCTION indicates data like channel, volume. Formerly, exclusive use of OSD IC was used, but in N5SS, the OSD function is within the main microcomputer. Pin function concerning on-screen data generation is shown in Fig. 3-4. Oscillation clock of OSD is approx. 4.5MHz. 9MHz which becomes multiplied by two to become the dot clock i slocated within the microcomputer. For oscillation, a coil TRF1160D (LA02) is used.

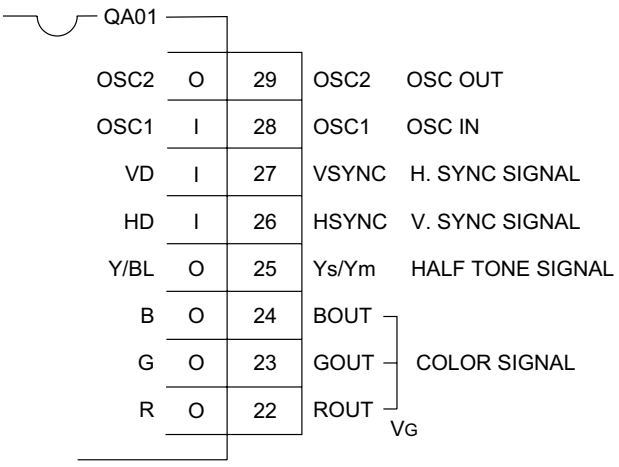


Fig. 3-4

7. SYSTEM BLOCK DIAGRAM

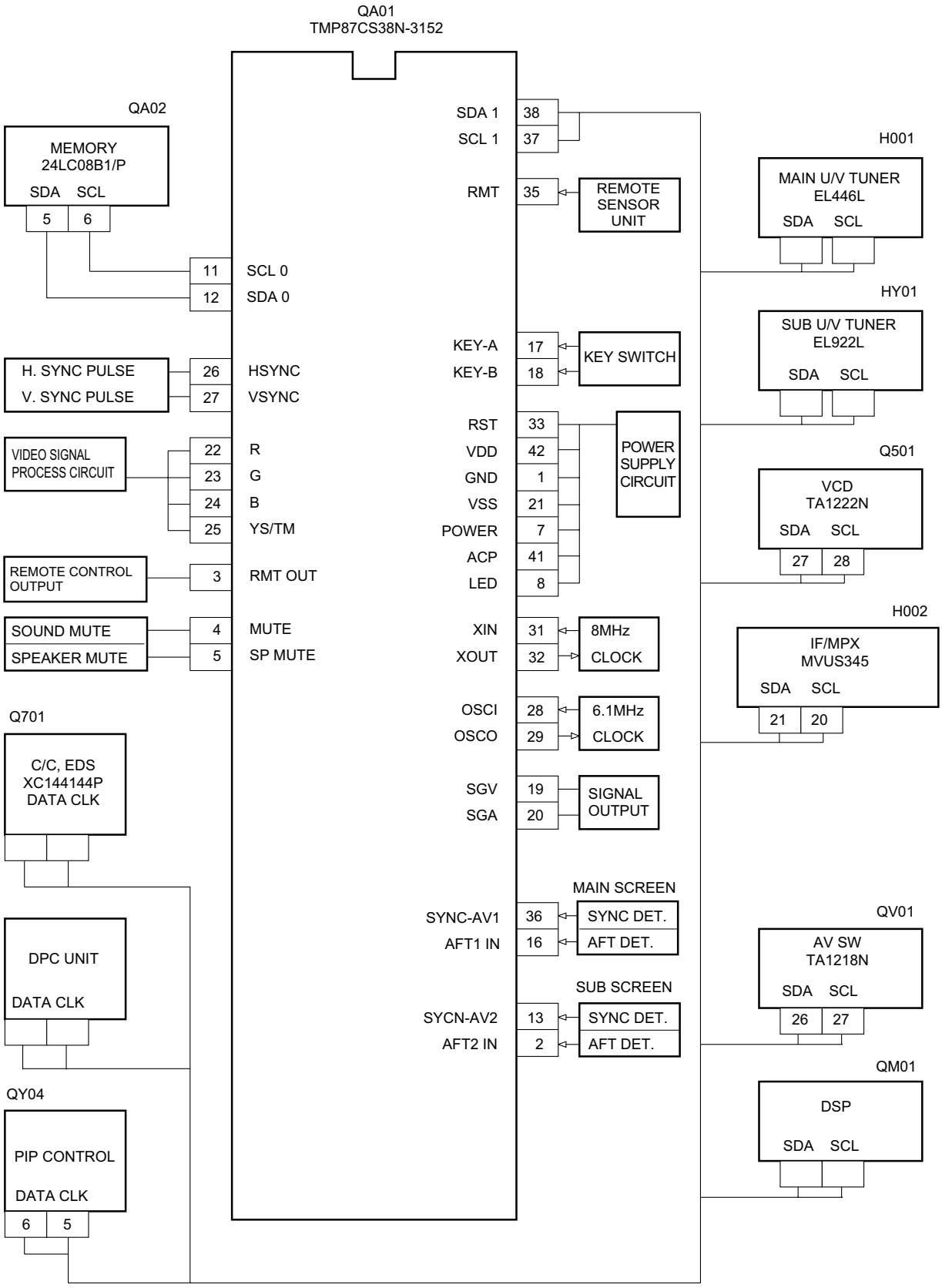


Fig. 3-5

8. LOCAL KEY DETECTION METHOD

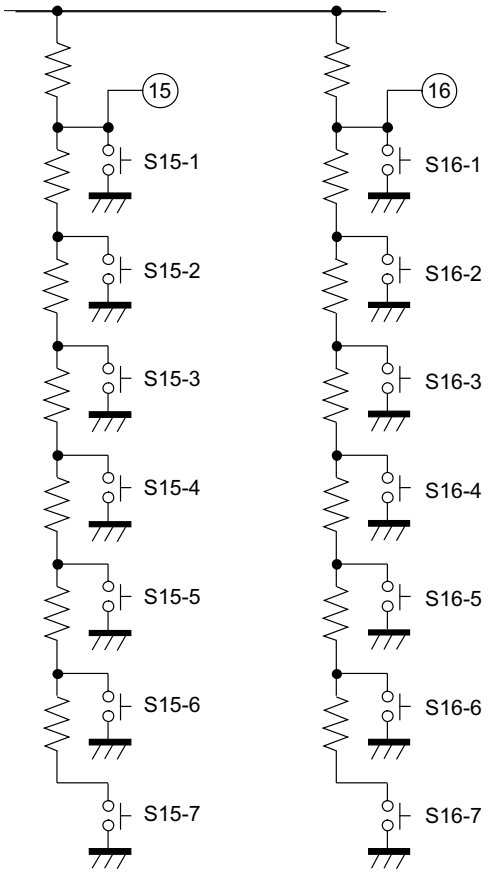


Fig. 3-6. Local key assignment

Local key detection in the N5SS chassis is carried out by using an analog voltage divider-like method which detects a voltage appearing at the local key input terminals (pins 17, 18) of the microcomputer whenever a key is depressed. Using this method, a maximum of 14 keys can be interpreted.

The circuit diagram shown at the left is a representation of the local key circuit. As can be seen from the diagram, when one of keys among SA-01 to SA-08 is pressed, each of two input terminals (pins 17, 18) develops a voltage (Vin) corresponding to the key pressed. (The voltage measurement and key identification are carried out by an A/D converter inside the microcomputer along with interpreting software.

Table 3-1 Local key assinment

Key No.	Function	Key No.	Function
SA-02	POWER	SA-01	DEMO START/STOP
SA-03	CH UP		
SA-04	CH DN		
SA-05	VOL UP		
SA-06	VOL DN		
SA-07	ANT/VIDEO, ADV		
SA-08	MENU		

9. ENTERING THE SERVICE MODE

1. PROCEDURE
   (1) Press once MUTE key on the remote hand unit to indicate MUTE on screen of the television.
   (2) Press the MUTE key of remote hand unit again and keep depressed while depressing the MENU key on the front of the unit.

2. During service mode, indication S is displayed at upper right corner on screen.

10. TEST SIGNAL SELECTION

1. In OFF state of test signal, SGA terminal (Pin 20) and SGV terminal (Pin 21) are kept at a "L" condition.
2. The function of VIDEO test signal selection is cyclically changed with each depression of the VIDEO key (on the remote control unit).

Table 3-2

Test Signal No.	Name of Pattern
0	Signal OFF
1	All black signal + R single color (OSD)
2	All black signal + G single color (OSD)
3	All black signal + B single color (OSD)
4	All black signal
5	All white signal
6	W/B
7	Black cross bar
8	White cross bar
9	Black cross hatch
10	White cross hatch
11	White cross dot
12	Black cross dot
13	H signal (bright area)
14	H signal (dark area)
15	Black cross + G

   (3) SGA (audio test signal) output should be square wave of 1kHz.

11. SERVICE ADJUSTMENT

1. ADJUSTMENT MENU INDICATION ON/OFF, MENU key (on TV set)
2. During display of the adjustment menu, the following functions are possible:
   a) Selection of adjustment item :
      POS UP/DN key (on TV/remote unit)
   b) Adjustment of each item :
      VOL UP/ DN key (on TV / remote unit)
   c) Direct selection of adjustment item
      R CUTOFF : 1 POS (remote unit)
      G CUTOFF : 2 POS (remote unit)
      B CUTOFF : 3 POS (remote unit)
   d) Data setting for PC unit adjustment
      SUB CONTRAST : 4 POS (remote unit)
      SUB COLOR : 5 POS (remote unit)
      SUB TINT : 6 POS (remote unit)
   e) Horizontal line ON/OFF : VIDEO (TV)
      (**NOTE: applies only to direct view)**
   f) Test signal selection : VIDEO (remote unit)
   * In service mode, serviceable items are limited.

3. Test audio signal ON / OFF : 8 POS (remote unit)
   * Test audio signal : 1kHz

4. Self check display : 9 POS (remote unit)
   * Cyclic display (including ON/OFF)

5. Initialization of memory :
   CALL (remote unit) + POS UP (TV)
6. Initialization of self check data :
   CALL (remote unit) + POS DN (TV)
7. BUS OFF :
   CALL (remote unit) + VOL UP (TV)

12. FAILURE DIAGNOSIS PROCEDURE

The N5SS chassis is equipped with a self diagnosis function inside, used for troubleshooting.

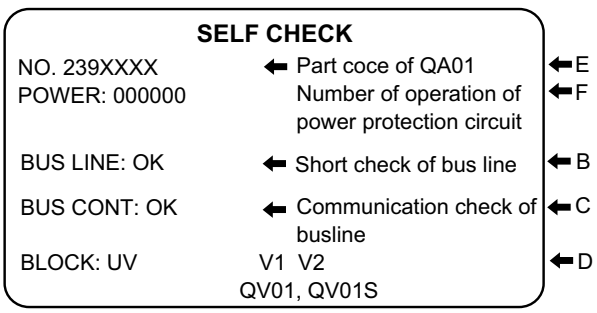
1. CONTENTS TO BE CONFIRMED BY CUSTOMER BEFORE SERVICE CALL IS MADE

Table 3-3

Contents of self diagnosis	Display items and actual operation
A. DISPLAY OF FAILURE INFORMATION IN NO PICTURE (Condition of display) 1. When power protection circuit operates; 2. When I2C-BUS line is shorted;	Power indicator lamp blinks and picture does not come. 1. Power indicator red lamp blinks. (0.5 seconds interval) 2. Power indicator red lamp blinks. (1 seconds interval) If these indication appears, repairing work is required.

2. CONTENTS TO BE CONFIRMED BY SERVICER (Check in self diagnosis mode)

Table 3-4

Contents of self diagnosis	Display items and actual operation
Contents of self diagnosis <Countermeasure in case that phenomenon always arises.> B. Detection of shortage in BUS line C. Check of comunication status in BUS line D. Check of signal line by sync signal detection E. Indication of part code of microcom.(QA01) F. Number of operation of power protection circuit	Display items and actual operation (Example of screen display) 

3. EXECUTING SELF DIAGNOSIS FUNCTION [CAUTION]

(1) When executing block diagnosis, select first the desired input signal source (U/V BS VIDEO1,2,3) screen, and then enter the self diagnosis mode.

(2) When diagnosing other input modes, repeat the diagnosis routines after source selection. The test signals and/or routines apply only to the video source selected at the time of testing.

(PROCEDURE)

(1) Place the unit in the service mode.

(2) Press the “9” key on the remote control will display the self diagnosis results on screen.
With each key press the mode will change as shown below.

(3) To exit from the service mode, turn the power off via the front panel or remote control.

4. UNDERSTANDING THE RESULTS OF THE SELF DIAGNOSIS FUNCTION
See Fig. 3-7 .

(Example of screen display)

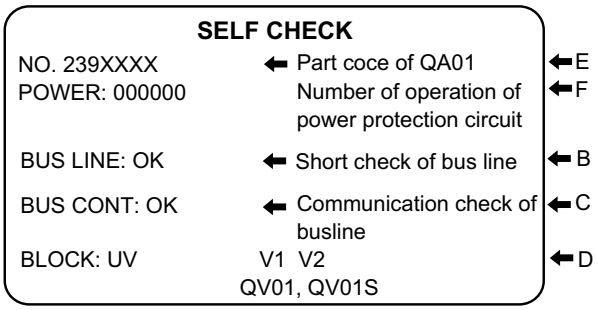


Fig. 3-7

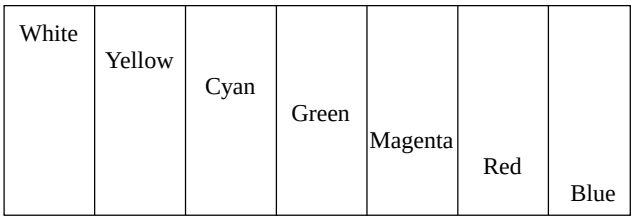
Table. 3-5

Item	Contents	Instruction of results
BUS LINE	Detection of bus line short	Indication of OK for normal result, NG for abnormal
BUS CONT	Communication state of bus line	Indication of OK for normal result Indication of failure place in abnormality (Failure place to be indicated) QA02 NG, H001 NG, Q501 NG, H002 NG QV01 NG, Q302 NG, QY02 NG, HY01 NG QD04 NG, QM01 NG, Q701 NG Note 1. The indication of failure place is only one placet though failure places are plural. When repair of a failure place finishes, the next failure place is indicated. (The order of priority of indication is left side.)
BLOCK: UV1 UV2 V1 V2	The sync signal part in each video signal supplied from each block is detected. Then by checking the existence or non of sync part, the result of self diagnosis is displayed on screen. Besides, when “9” key on remote unit is pressed, diagnosis operation is first executed once.	*Indication by color • Normal block :Green • Non diagnosis block :Cyan

<Clearing the self diagnosis results>
While the error count state is displayed upon the screen, press the “CHANNEL DOWN” button on TV set pressing “DISPLAY” button on remote unit.

[CAUTION]
All ways observe the following caution, when in the service mode screen.

- Do not press the **“CHANNEL UP”** button. This will cause initialization of the memory IC. (Replacement of memory IC is required.
- Do not initialize self diagnosis result. This will change user adjusting contents to factory setting value. (Adjustment is required.)



(COLOR BAR SIGNAL)
Color elements are positioned in sequence of high brightness.

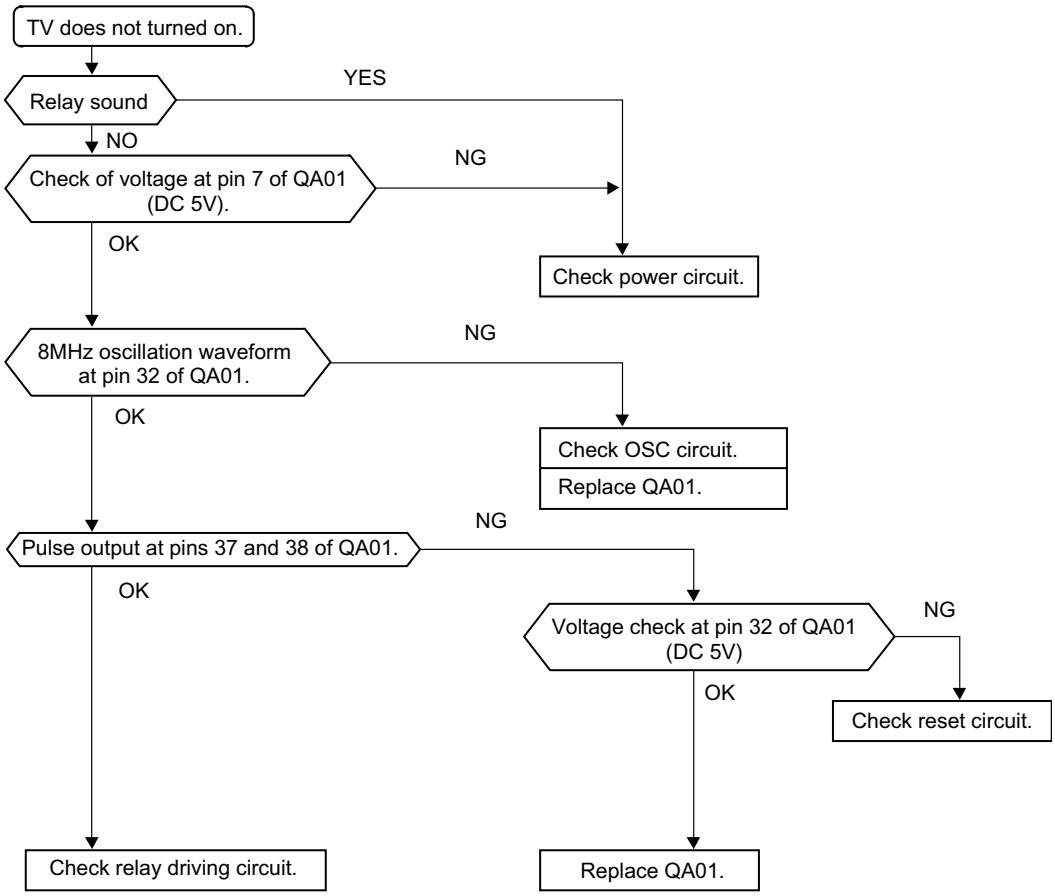
<Troubleshooting method utilizing internal test signal> (VIDEO INPUT 1 terminal should be open.)

(1) With service mode screen, press VIDEO button on remote unit. If inner video signal can be received, QV01 and after are normal.
(2) With service mode screen, press “8” button on remote unit. If sound of 1kHz can be heard, QV01 and after are normal.

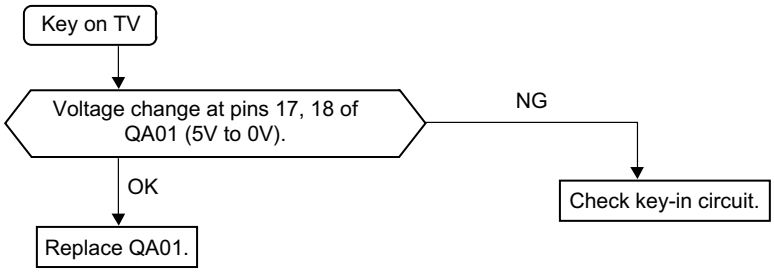
* By utilizing signal of VIDEO input terminal, each circuit can be checked. (Composite video signal, audio signal)

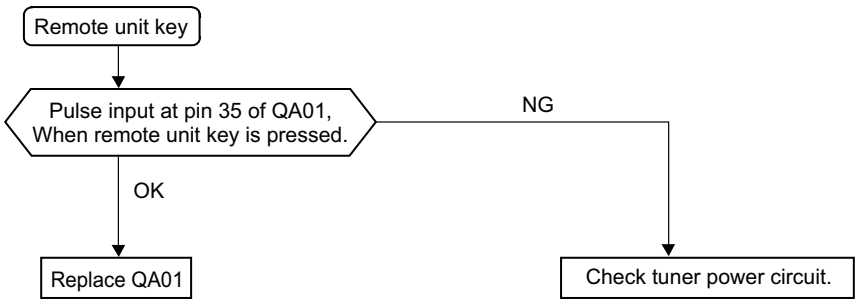
13. TROUBLE SHOOTING CHARTS

(1) TV DOES NOT TURNED ON

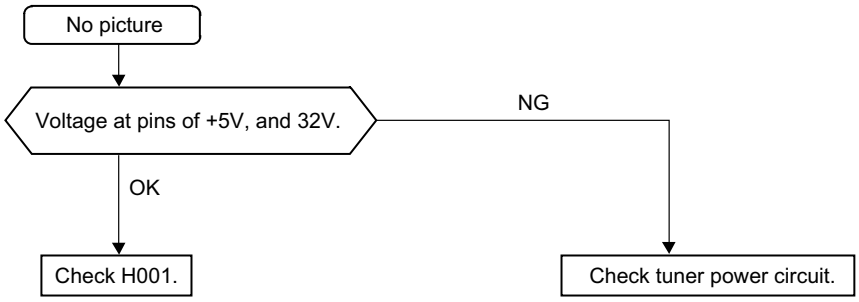


(2) NO ACCEPTION OF KEY-IN

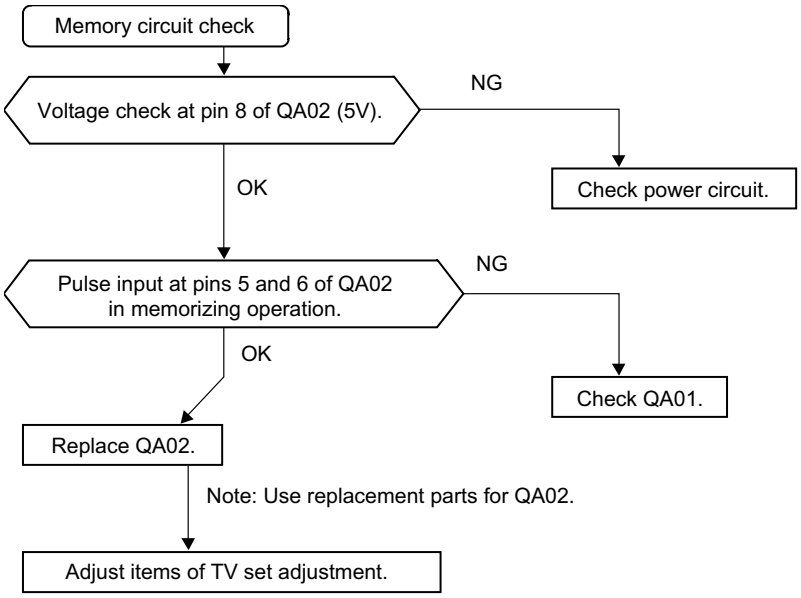




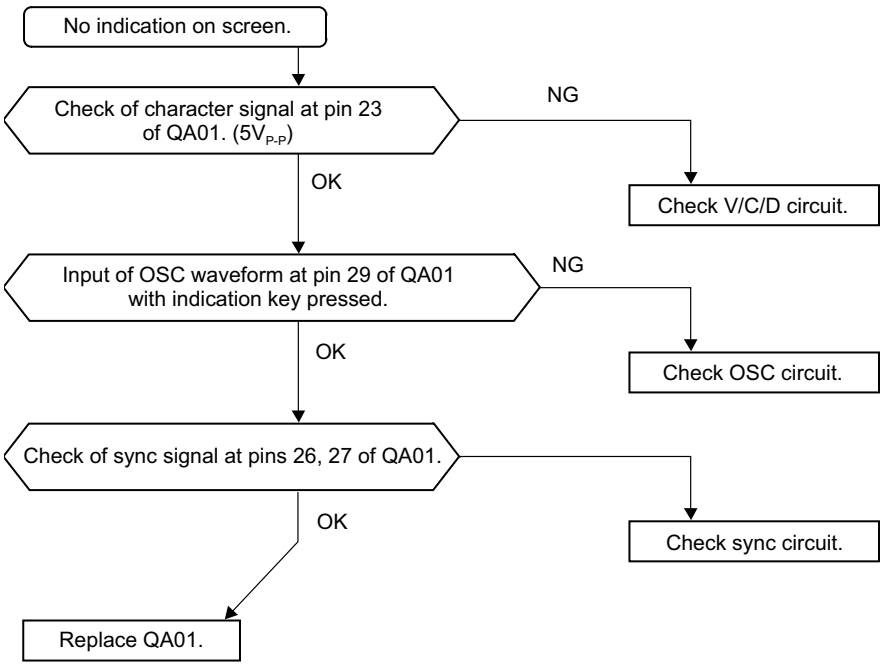
(3) NO PICTURE (SNOW NOISE)



(4) MEMORY CIRCUIT CHECK



(5) NO INDICATION ON SCREEN



NOTES

SECTION IV
AUDIO OUTPUT CIRCUIT

1. OUTLINE

The main amplifiers and woofer output amplifiers use a bipolar IC (TA8256H) and develop output powers of 10Wx2 + 13W.

2. THEORY OF OPERATION

2-1. Operation of TA8256H

The TA8256H is a modified version of the TA8128AH which was used in the N4SS chassis as an audio ouput IC. In the TA8256H, one channel has been added and up to 3 channels can be used. Performance for each channel is the same as that of the TA8218H. Fig. 4-1 shows a block diagram of the IC.

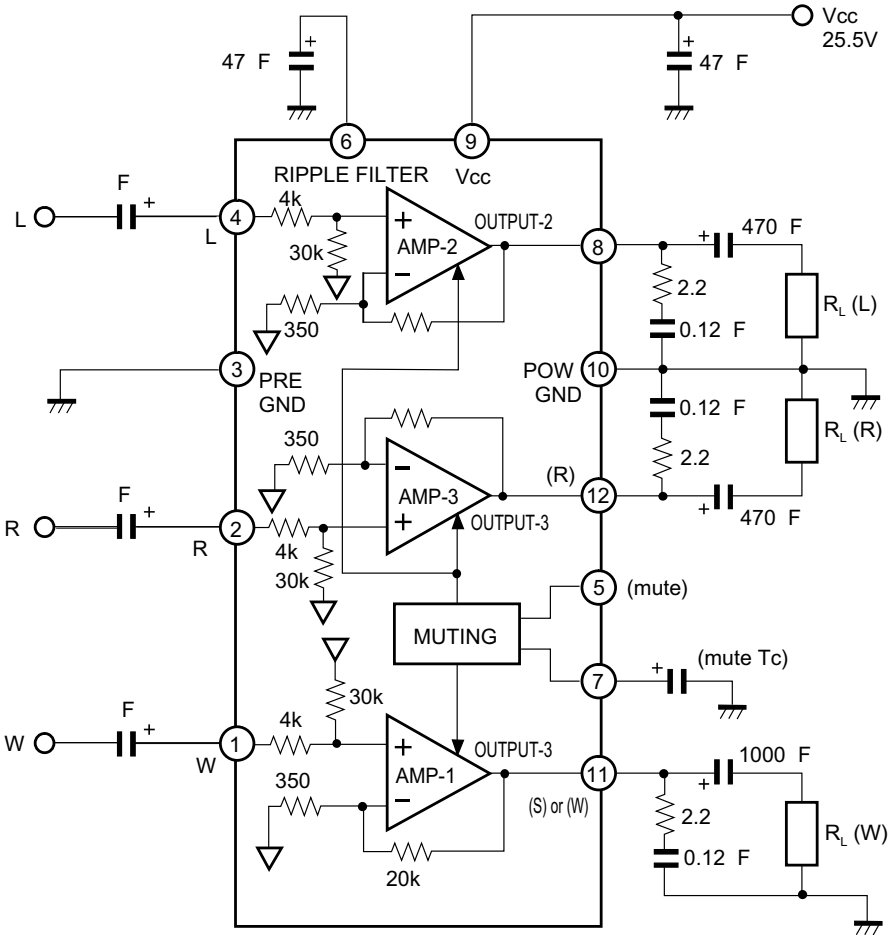


Fig. 4-1

SECTION V
DSP CIRCUIT

1. ORIGINS OF DOLBY SURROUND

Dolby Stereo movies and Dolby Surround video and television programs include an additional sonic dimension over conventional stereo productions. They are made using a Dolby MP (Motion Picture) Matrix encoder, which combines four channels of audio into a standard two-channel format, suitable for recording or transmitting the same as regular stereo programs. To recapture the dimensional properties brought by the additional channels, a Dolby Surround decoder is used. In the theatre, a professional decoder is part of the Dolby Stereo cinema processor used to play 35 mm stereo optical prints. The decoder recovers the left, center, and right signals for playback over three front speakers, and extracts the surround signal for distribution over an array of speakers wrapped around the sides and back of the theater. (These same speakers may also be driven from four of the six discrete tracks on 70 mm Dolby Stereo magnetic prints, but in this case no decoder is needed.)

Home viewing of movies on video has become extremely popular, and with the advent of stereo VCR's, stereo television and digital video discs, the audio side of the video presentation has improved considerably, inviting the use of full-range sound reproduction. The ability to deliver high quality audio in these formats made it easy to bring MP Matrix-encoded soundtracks into the home as well, thus establishing the foundation for Dolby Surround.

2. THE DOLBY MP MATRIX

One of the original goals of the MP Matrix was to enable Dolby Stereo soundtracks to be successfully played in theaters equiped for mono or two-channel stereo sound. This allows movies to be distributed in a single optical format, and furtheremore results in complete compativility with home video media without requiring separate soundtrack mixes. Since the three front channels of the MP Matrix are assembled in virtually the same way as a conventional stereo mix --- left into left, center equally into left and right, and right into right- playing a Dolby Stereo soundtrack over two speakers reproduces the entire encoded soundtrack. There is but one exception: the surround signal, though audible, is not reproduced in its proper spatial perspective. When the first home decoder was developed in 1982, its goal was to restore this lone missing dimension.

Before we discuss decoders, it is necessary to see how the MP Matrix encoder works. Referring to the conceptual diagram in Fig. 5-1, the encoder accepts four separate input signals; left, center, right, and surround (L, C, R, S), and creates two final outputs, left-total and right-total (Lt and Rt).

The L and R inputs go straight to the Lt and Rt outputs without modification, and the C input is divided equally to Lt and Rt with a 3 dB level reduction (to maintain constant acoustic power). The S input is also divided equally between Lt and Rt, but it first undergoes three additional processing steps:

a. Frequency bandlimiting from 100 Hz to 7 kHz.
b. Encoding with a modified from of Dolby B-type noise reduction.
c. Plus and minus 90-degree phase shifting is applied to create a 180-degree phase differential between the components feeding Lt and Rt.

It is clear there is no loss of separation between the left and right signals; they remain completely independent. Not so obvious is that there is also no theoretical loss of separation between the center and surround signals. Since the surround signal is recovered by taking the difference between Lt and Rt, the identical center channel components in Lt and Rt will exactly cancel each other in the surround output. Likewise, since the center channel is derived from the sum of Lt and Rt, the equal and opposite surround channel components will cancel each other in the center output.

The ability for this cancellation technique to maintain high separation between center and surround signals requires the amplitude and phase characteristics of the two transmission channels to be as close as possible. For instance, if the center

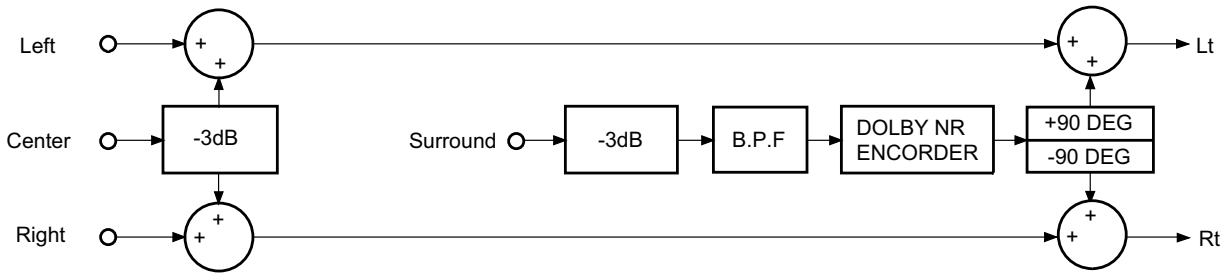


Fig. 5-1 Conceptual Dolby Stereo/Dolby Surround encoder

channel components in Lt are not identical to the ones in Rt as a result of a channel balance error, center information will come out of the surround channel in the form of unwanted crosstalk.

3. THE DOLBY SURROUND DECODER

This leads us to the original Dolby Surround decoder. The block diagram in Fig. 5-2 shows how the decoder works. Except for level and channel balance corrections, the Lt input signal passes unmodified and becomes the left output. The Rt input signal likewise becomes the right output. Lt and Rt also carry the center signal, so it will be heard as a "phantom" image between the left and right speakers, and sounds mixed anywhere across the stereo soundstage will be presented in their proper perspective. The center speaker is thus shown as optional since it is not needed to reproduce the center signal.

The L-R stage in the decoder will detect the surround signal by taking the difference of Lt and Rt, then passing it through a 7 kHz low-pass filter, a delay line, and complementary Dolby noise reduction. The surround signal will also be reproduced by the left and right speakers, but it will be heard out-of-phase which will diffuse the image.
Since the heart of the decoding process is a simple L-R difference amplifier, it is referred to generically as a "passive" decoder. This is to distinguish it from decoders using active processes to enhance separation which are known as "active" decoders.

4. DSP CIRCUIT

A surround component (L-R) is extracted from L, R audio signals coming through the AV SW in the matrix circuit as shown in Fig. 5-3. The surround component enters the DSP circuit through the LPF.
The signal is A/D converted, delayed by an arbitrary time of 0~100 msec (every 3.2 msec) by digital process and then D/A converted and outputs from the DSP IC. The DSP IC develops two outputs; (LO) for FRONT (LO) and (RO) for REAR and each output is controlled by the microcomputer for each surround mode. The output signal (LO) for FRONT is added and subtracted with the input signal in a matrix circuit and output from the front speaker in passing through the audio processor and main amplifiers.
At the same time, the output signal (RO) for REAR is fed to the Dolby NR circuit, but switched to "Dolby surround" mode, and then output from the rear speaker in passing through audio processors and rear main amplifiers.
In this case, the DSP stands for not only a simple digital surround processor but also a digital surround field processor. That is, it works to give a simple surround effect but to give effect as if the listener can feel reality suitable for the programs. For example, it aims to give the listeners a reality matching to each program they are enjoying in their home listening room so that they can obtain reality of big concert hall or feel as if they are watching a move at a reserved seat in a movie theater.

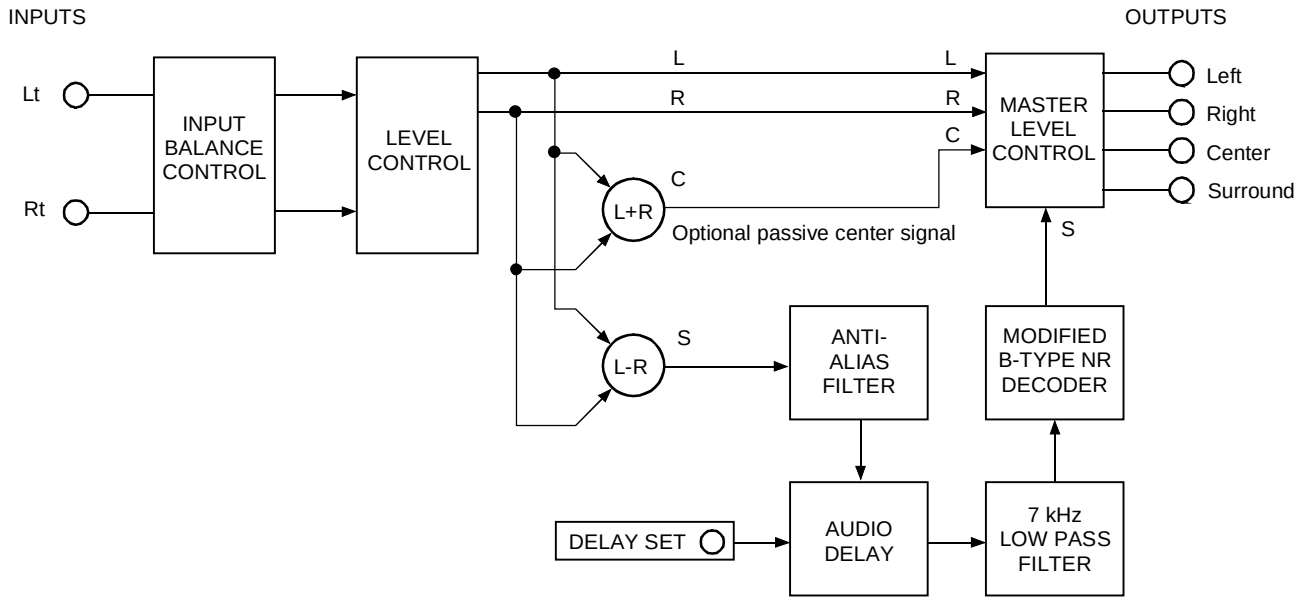


Fig. 5-2 Passive surround decoder block diagram

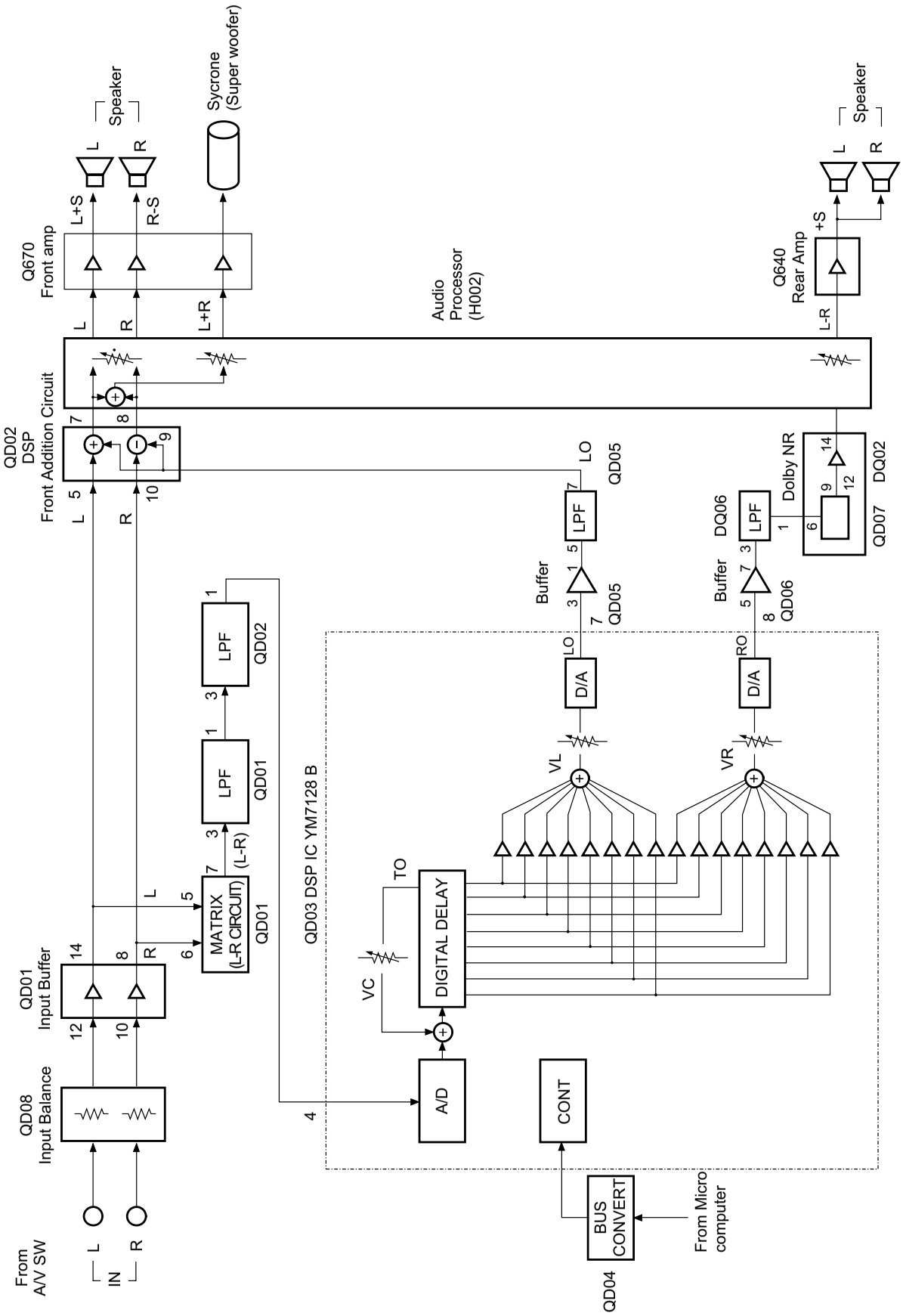


Fig. 5-3 Block diagram of DSP circuit

As shown in Fig. 5-4, a sound emitted in a sound field can be classified as a direct sound which directly reaches ears of a listener, and reflected sound which comes after collision with a wall as shown by dotted line or comes after several times of collision as shown by double dotted lines. The listeners are determining that they are listing in what type of location by perceiving time difference and volume level difference between the direct sound and the reflected sound.

For more detail, this situation can be expressed with the direct sound, initial reflection sound coming after one time of reflection, and trains of reverberation sound in later period as shown in Fig. 5-5.

The DSP circuit develops these initial reflection sound and the reverberation sound artificially and add them to the original sounds, thereby creating rhe effect that allows the listeners in the home listening room to feel as if they are listening in an original location.

The DSP IC YM7128B has eight separate output taps and their delay time and the output levels can be specified separately, so, various sound fields can be selected by varying the initial reflection sound. Moreover, the IC has an internal feedback loop which controls the delay time and the output level in considering the later time reverberation sound.

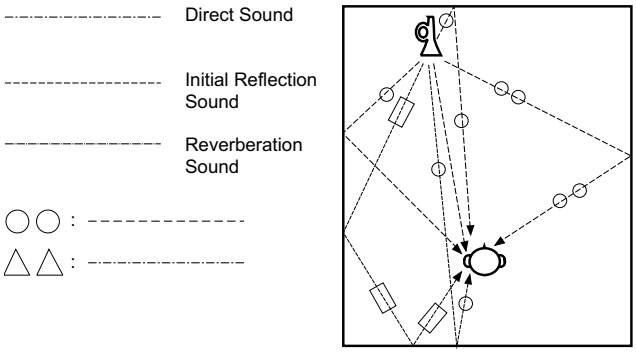


Fig. 5-4

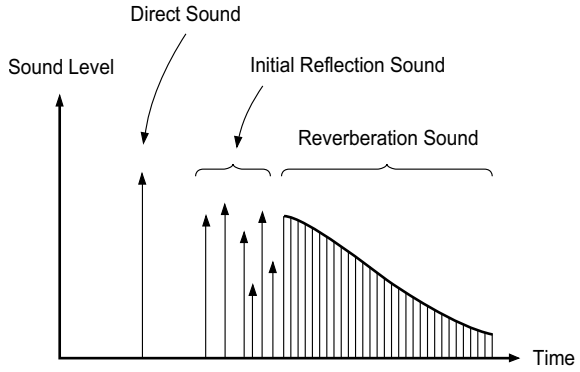


Fig. 5-5

5. DSP (Digital Surround Processor) IC

Input signal entered into analog input pin 4 of DSP IC QD03 (YM7128B) is converted to 14 bit digital signal with the sampling frequency 23.6 kHz by A/D converter of 14 bit floating system, and enters digital delay circuit through digital attenuator VM and doubler.

The digital delay circuit has nine output taps, and the delay time of each tap can be controlled independently, also each tap position can be switched by T0 to T8 register.

In a minute, the T0 output passes through the primary FIR (Finite Impulse Response) type low pass filter, and reduction processing is performed by VC, then it feed-backed to the delay input after it is added to the doubler described above.

The output of eight taps T1 to T8 is added after performing reduction processing by GL1~GL8, GR1~GR8, and reduction processing is performed by the digital attenuator VL or VR, and an analog output is created by D/A converter after passing through digital filter, comes out from pin 7 or 8.

The digital attenuated value, delay time and the coefficient of FIR type low pass filter are set by writing the data on the register.

This process is performed by loading three data from sub microcomputer to microcomputer interface.

This unit has four modes as surround mode. The setting values are described in Table 5-1.

Table 5-1 DSP control factor

Mode	OFF Control	DOLBY SURROUND	THEATER	STADIUM	NIGHT CLUB HALL HALL	CONCERT	UNIT
-VM (IN)	-¥	P-0	P0 ¥	P0	P0	P0	dB
VL (LO)		-¥	P0~-•	P0~-¥•	P0~--¥•	P0~--¥•	
VR (RO)		P0	P0	P0	P0	P0	
VC (Echo)		-¥	-¥	M-6	M-10	M-8	
GL1			P-4	M-2	M-2	P-2	
2			M-6	-¥	P-4	P-10	
3			P-12		P-6	P-16	
4			P-12		M-10	-¥	
5			-¥		-¥		
6							
7							
8		▼					
GR1		P0		▼			
2		-¥		P0			
3				P-18			
4			▼	-¥	▼	▼	
5			P-2		P-6	P-4	
6			M-2		M-6	P-8	
7			P-8		M-10	P-8	
8	▼	▼	P-10	▼	P-12	P-14	▼
T0 (Delay)	0	0	0	100.0	19.4	51.6	msec
1		19.4	12.9	93.6	12.9	71.0	
2		0	38.7	100.0	19.4	83.9	
3			71.0	100.0	22.6	100.0	
4			87.1	0	29.0	0	
5			29.0		6.5	64.5	
6			45.2		9.7	80.7	
7			83.9		25.3	90.4	
8			100.0	▼	35.5	100.0	▼
C0 (Filter)			0	0.71875	0.59375	0.875	—
1	▼	▼	▼	0.28125	0.40625	0.125	—

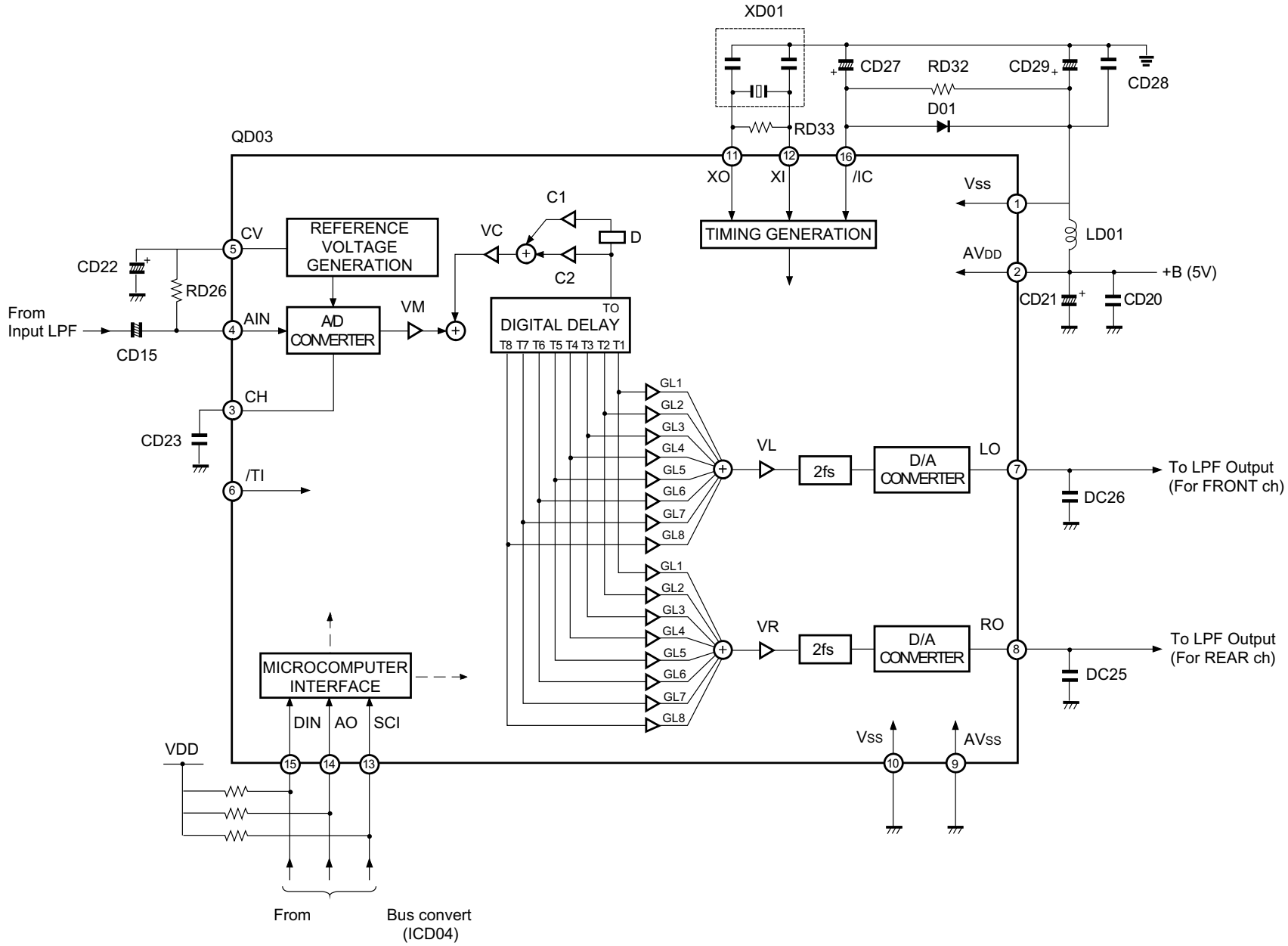

XD01
CD27
RD32
CD29
CD28
D01
RD33
QD03
11
12
16
XO
XI
/IC
TIMING GENERATION
Vss
1
LD01
AVDD
2
+B (5V)
CD21
CD20
C1
D
C2
VC
CV
5
REFERENCE VOLTAGE GENERATION
CD22
RD26
From Input LPF
CD15
AIN
4
A/D CONVERTER
VM
TO
DIGITAL DELAY
T8 T7 T6 T5 T4 T3 T2 T1
CH
3
CD23
/TI
6
GL1
GL2
GL3
GL4
GL5
GL6
GL7
GL8
VL
2fs
D/A CONVERTER
LO
7
To LPF Output (For FRONT ch)
DC26
VR
RO
8
To LPF Output (For REAR ch)
DC25
MICROCOMPUTER INTERFACE
DIN
AO
SCI
VDD
15
14
13
Vss
10
AVss
9
From
Bus convert (ICD04)

Fig. 5-6

NOTES

SECTION VI
A/V SWITCHING CIRCUIT

1. OUTLINE

The A/V switching circuit selects the desired video and audio signals from the various inputs. It is controlled by the microcomputer through IIC bus.

2. IN/OUT TERMINALS

TUNER INPUT	U/V Tuner (Main)
	U/V Tuner (PIP)
EXTERNAL INPUT	VIDEO 1 With S-terminal
	VIDEO 2
	VIDEO 3 (Front) With S-terminal
OUTPUT	VIDEO OUTPUT (V, L, R)
	AUDIO ON SUB-PICTURE

3. CIRCUIT OPERATION

This circuit consists of A/V SW IC; TA1218N (QV01), and selects signals from U/V tuner (Main), U/V tuner (PIP), E1, E2 and E3.

3-1. Composite Video Signal

The selected video signal is output to pin 38 of QV01, and separated by comb filter into Y an C. The resulted signal is input to pins 30 and 32 of QV01, and is output to pins 36 and 34 to be supplied to Q501 (V/C/D).
Video signal for PIP is output to pin 42 of QV01, and is supplied to PIP unit (ZY01).

3-2. S-Video Signal

When a cable is connected to S-VIDEO terminal, inner switch of S-VIDEO terminal is shorted to ground to turn off the transistor (QV05 for VIDEO1 input) for S-VIDEO terminal detection. Then chroma input terminal (Pin 14 for VIDEO1 input) of QV01 turns on.

AV SW CIRCUIT

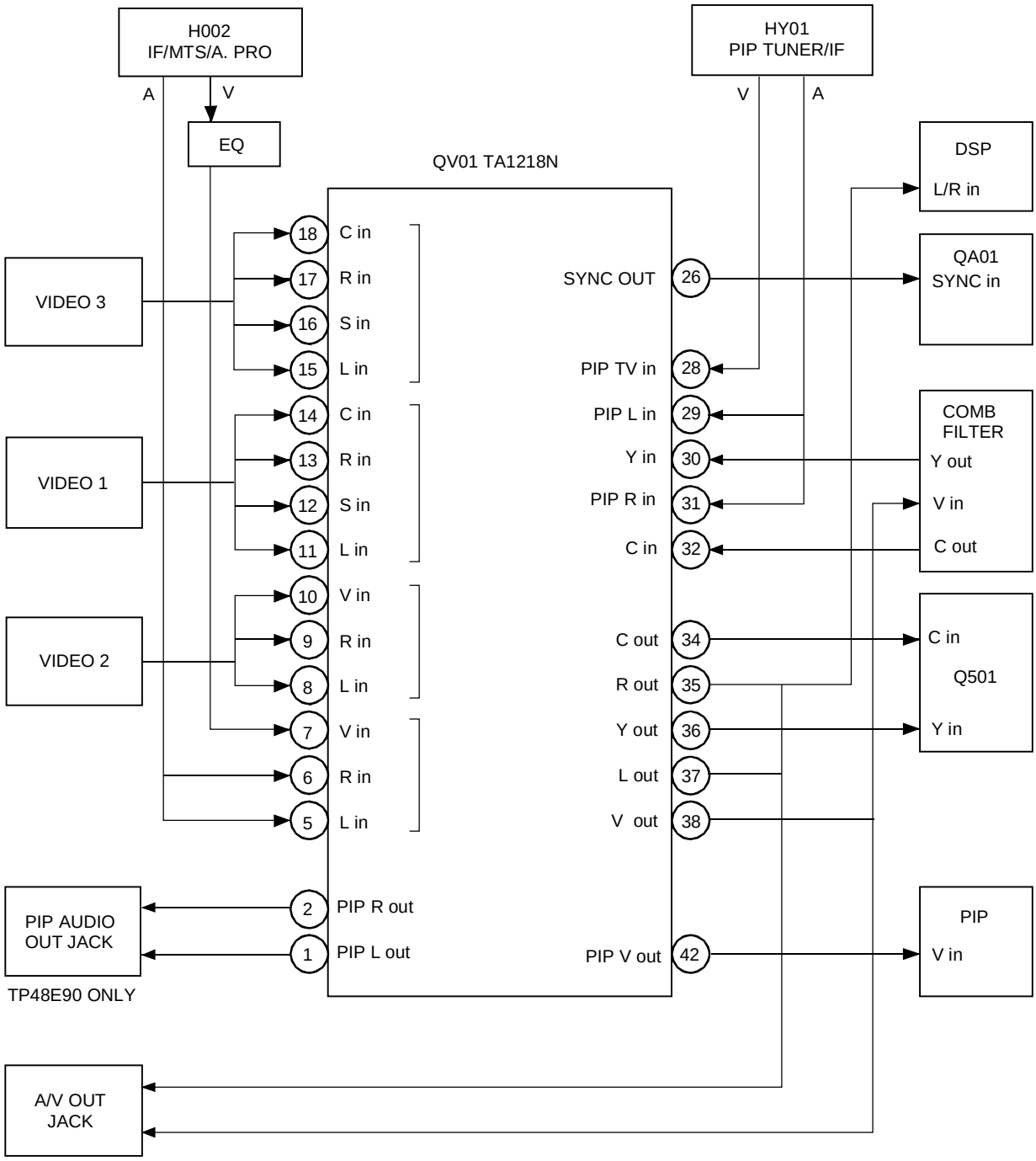


Fig. 6-1

NOTES

SECTION VII
VIDEO PROCESSING CIRCUIT

1. OUTLINE

This circuit converts and amplifies video signal (Luminance and chroma signals) separated into Y/C, to original color signal, and is supplied to CRT Drive circuit.

2. SIGNAL FLOW

Signal flow chart is shown in figure 6-1 Block diagram.

(1) Luminance signal is input to pin 15 of Q501, and enters into delayline inside Q501 to be output to pin 4.

(2) Chroma signal is input to pin 13, and I/Q signal which is demodulated in color, is output to pins 5 and 6, and next supplied to pins 51 and 52.

(3) The signal is processed on luminance and chroma signals, and is converted to original color signal (R,G,B) by RGB matrix. Next the signal is superimposed with OSD signal to be output to pins 41, 42 and 43, and is supplied to CRT Drive circuit.

(4) The signal for Scan Modulation is processed with differential in Q501 to be output to pin 48 Besides, at terminal for adjustment TP501, luminance and chroma signals are automatically output according to the selected items of service mode.

3. CIRCUIT OPERATION

All processing operation of video signal are done inside Q501. The outline of Q501 (TA1222N) is explained in the next section. Here, major terminals excepting input/output terminals of Q501 are described.

Table 7-1

Pin No.	Name	Description
Pin 1	CW output	3.58MHz synchronized with burst is output. This is used for clock of comb filter.
Pin 10	Xtal 1	Terminal for 3.58MHz OSC crystal
Pin 11	APC filter	Terminal for phase detection of color sync (OSC frequency control)
Pin 18	SYNC	Sync-separated sync signal is output. It is used for detecting no signal in microcomputer.
Pin 30	HD	Terminal for output of HD pulse syncronized with horizontal sync., and for input of black expading mask pulse. It is used for timing pulse of OSD, C.C (Closed Caption) in micro- computer.
Pin 32	Ys	OSD change-over pulse input: Ys of OSD is input.
Pin 45	ABL	Terminal for ABL control input
Pin 47	Ym	Input of pulse for half tone control: It is supplied from microcomputer.
Pin 49	APL DET	Detecting average level of video signal for correction of DC transmission
Pin 50	BLACK DET	Detecting black area of video signal for black expading circuit
Pin 54	COL	Terminal for peak-hold of color limiter
Pin 55	DAC1	Test point (TP501): Functioning test point in service mode

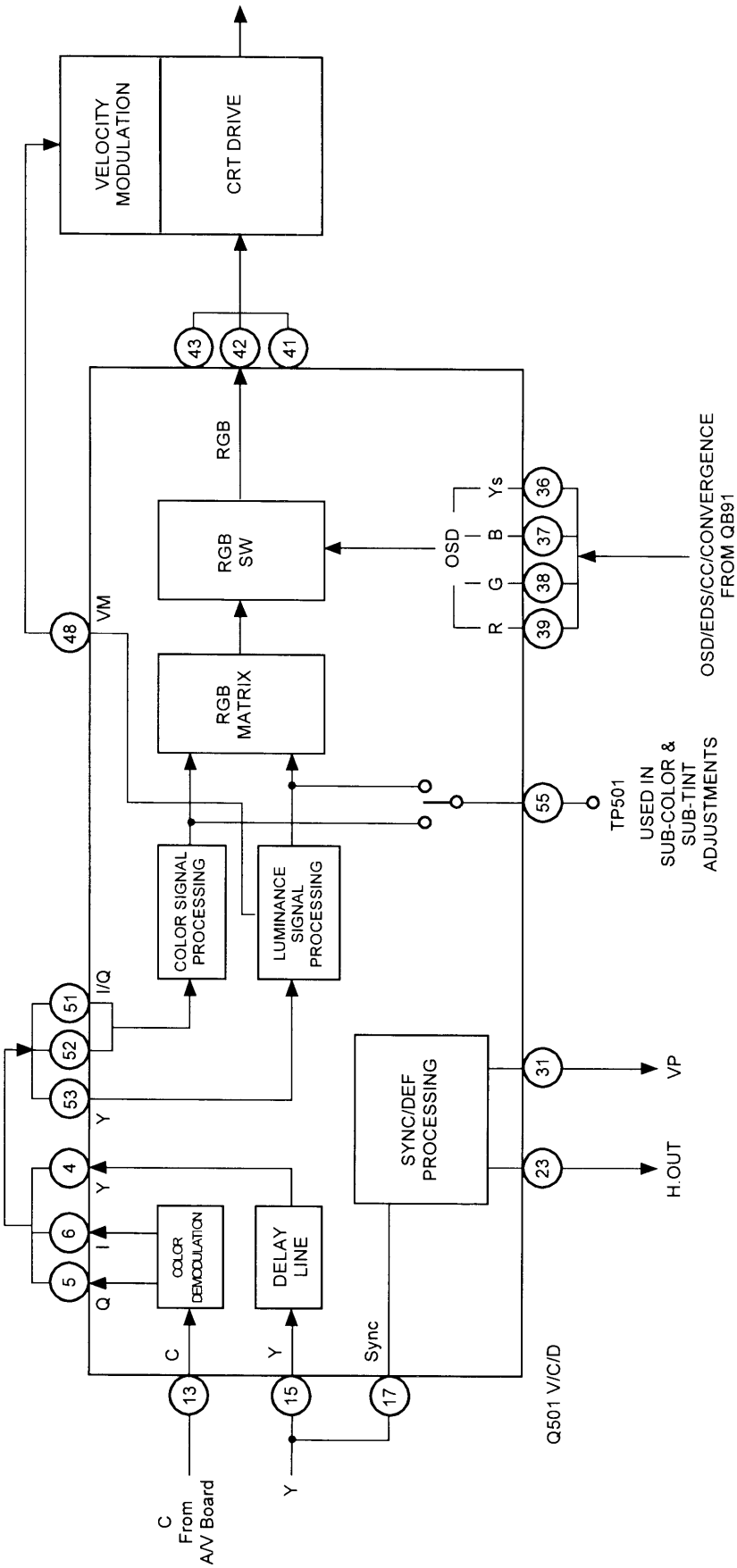


Fig. 7-1 Block diagram of Video Processing circuit

NOTES

SECTION VIII
V/C/D/IC

1. OUTLINE

This IC enables more precise picture setting than that of former IC (TA8845N) by means of large scale employment of IIC bus, and reduces many peripheral components by containing filters inside.
The main features (comparing TA8845) are as follows.

2. LARGE SCALE EMPLOYMENT OF BUS CONTROL OF PARAMETER FOR PICTURE CONTROLS

Soft method of picture making

Table 8-1

	Former/TA8845N	TA1222N
* Black expanding start point	External constant	BUS control
* DC transmission correction quantity point	External constant	BUS control
* Black level correction quantity	External constant	BUS control
* Each ABCL characteristic	External constant	BUS control

3. EMPLOYMENT OF CONTAINING EACH VIDEO BAND FILTER INSIDE

Employment of automatic adjustment circuit by Fsc to absorb deviation / Employment of deviation aborbing method by high S/N filter and mask triming using fixed CR

Table 8-2

	Former/TA8845N	TA1222N
* Y-DL	Apa-con DL inside	Inside
* Chroma TO/BPF	External	Inside
* Velocity modulation processing circuit	External	Inside
* Fsc trap for chroma demodulation output	External	Inside

4. EMPLOYMENT OF CONTAINING EACH FILTER (FOR S/H) INSIDE

Circuit operation by extremely low current / Employment of leak current cancel circuit Employment of detection circuit which does not suffer from influence of stray capacity

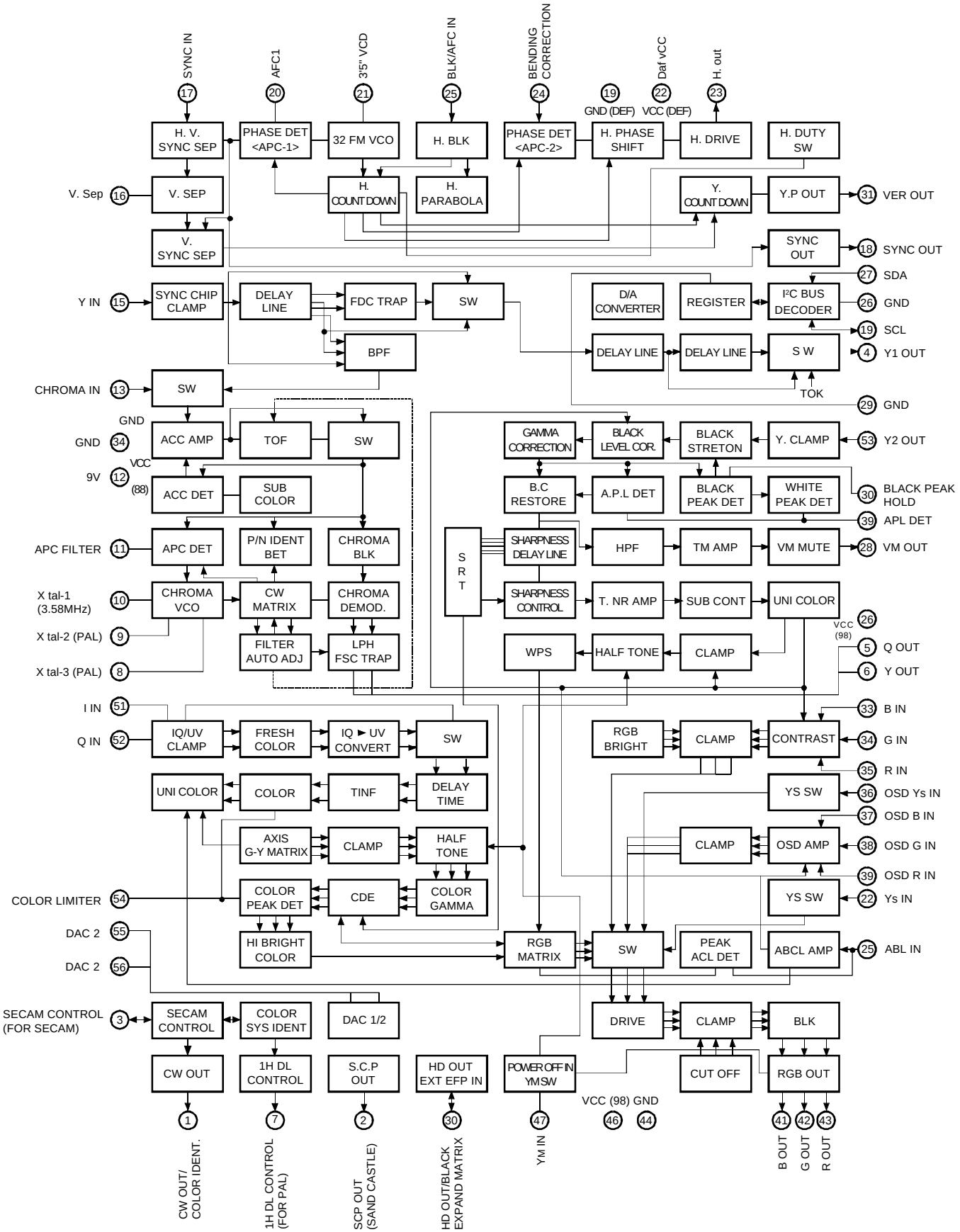
Table 8-3

	Former/TA8845N	TA1222N
* Chroma ACC / killer filter	External	Inside
* Y / color difference clamp filter	External	Inside
* Filter for filter automatic adjustment	External	Inside
* AFC 2 filter	External	Inside

5. LOW COST OF IC

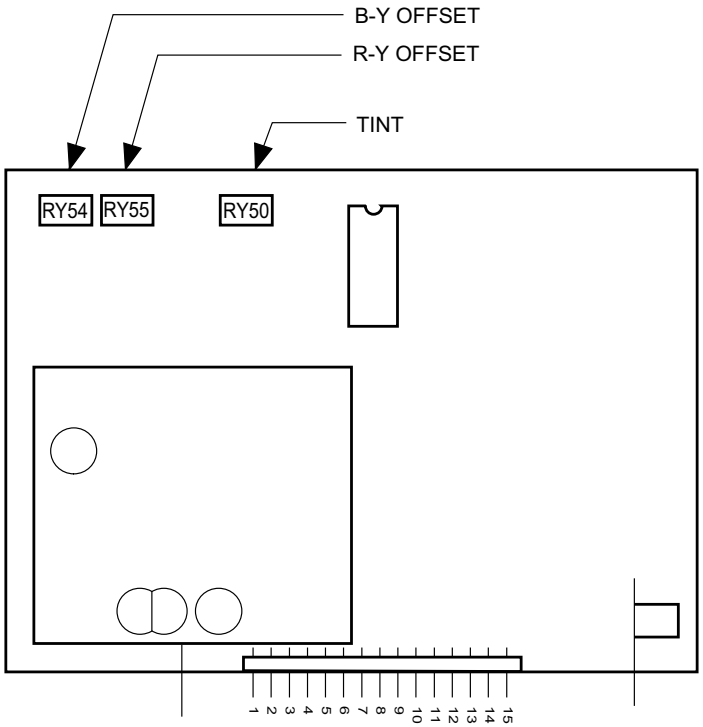
* Involving peripheral components inside ——> Down sizing of chip ——> Newly employment (NPN Tr area ratio to former : -25%) of miniature process (PLAS-1 S process)
* Involving peripheral components inside——>Increasing of power consumption——>2 power supply system (5V / 9V used)
* Involving peripheral components inside ——> Reducing of number of elements ——> Employment of new circuit
  (1) Reducing of gate (change of preset method) of register for IIC decoder
  (2) Reducing of DAC elements (employment of rudder type DAC + temperature compensation circuit)
  (3) Deletion of chroma CW, ACC (employment of 90 degree shift phase circuit with automatic adjustment)

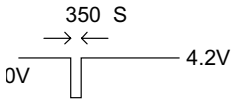
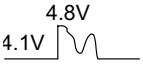
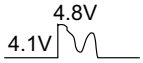
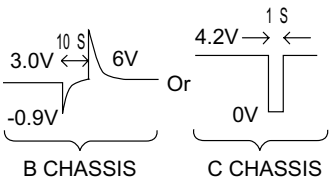
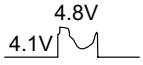
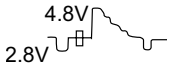
VCD BLOCK DIAGRAM (TA1222N)



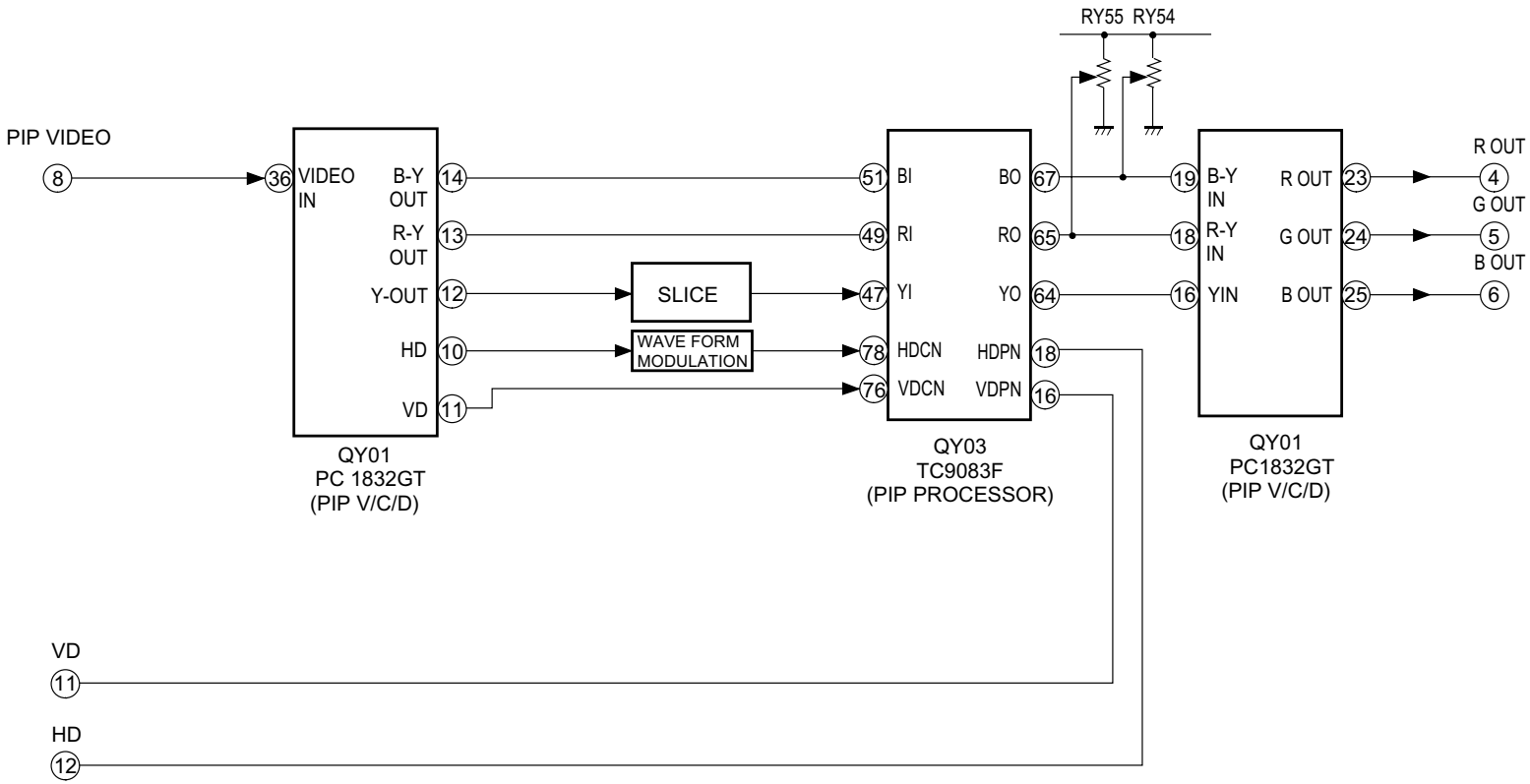
SECTION IX
PIP MODULE

PMUS 02H (SN:23148232)



PIN	I/O	NAME	PIN	I/O	NAME
1	0	YS 	9	I	5V
2	-	NC	10	I	GND
3	I	GND	11	I	VD 
4	O	R OUT 	12	I	HD
5	O	G OUT 	13	I/O	SCL 
6	O	B OUT 	14	I/O	SDA
7	I	GND	15	-	NC
8	I	PIP VIDEO 			

PMUS02H
<BLOCK DIAGRAM OF PIP MODULE>



NOTES

SECTION X
SYNC SEPARATION, H-AFC, H-OSCILLATOR CIRCUITS

1. SYNC SEPARATION CIRCUIT

The sync separation circuit separates a sync signal from a video signal and feeds it to an H and V deflection circuits.
The separation circuit consists of an amplitude separation (H and V sync separation circuit) and a frequency separation circuit (V sync separation circuit) which performs the separation by using a frequency difference between H and V.
In the N5SS chassis, all these sync separation circuits are contained in a V/C/D IC (TA1222N).
Fig. 10-1 shows a block diagram of the sync separation circuit.

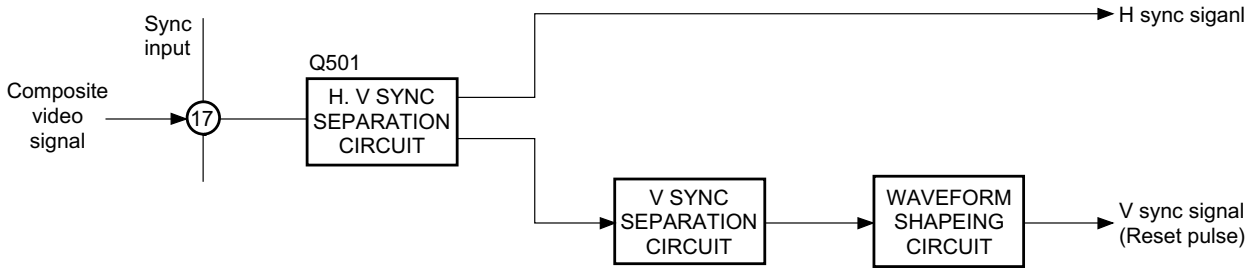


Fig. 10-1 Sync separation circuit block diagram

1-1. Theory of Operation

1-1-1. Auto slicer type synchronous separation circuit

When a synchronizing signal is separated, synchronous separation is made from the beginning with constant voltage in the conventional synchronous separation circuit. The auto slider type circuit employed in this time makes synchronous separation at a constant rate against the synchronizing signal amplitude. (See Fig. 10-2)
In this method, even if an abnormal signal with small amplitude is applied, stable synchronizing performance can be obtained without separating pedestal.

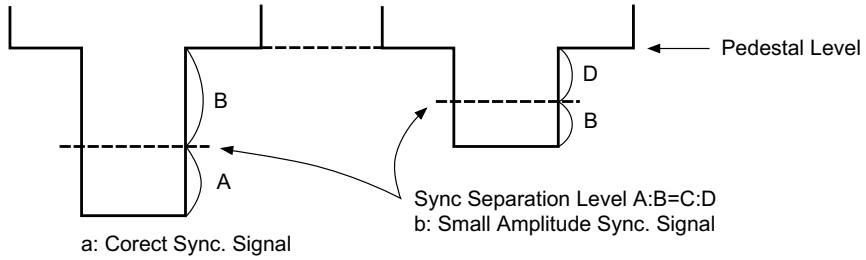


Fig. 10-2 Synchronous separation by auto slider system

1-1-2. V Sync Separation Circuit

To separate a V sync signal from the composite sync signal consisting of V and H sync signals mixed, two stages of integration circuits are provided inside the IC. The circuit consists of a differential circuit and a Miller integration circuit, and has following functions.

(1) Removes H sync signal component.
(2) Maintain stable V sync performance for a tape recorded with a copy guard.
(3) Stabilized V sync performance under special field conditions (poor field, ghost, sync depressed, adjacent channel best).

The V sync signal separated in this stage is processed in a waveform shape circuit and then used as a reset pulse in the V division circuit as stated later.

2. H AFC (Automatic Frequency Control) CIRCUIT

A sync system which performs synchronization with each waveform of the sync signal as performed in a sync system in the V circuit is called a direct type sync system. However, if the synchronization for the H oscillator is carried out with this method, the H oscillator synchronizes with external noises and the H synchronization will be disturbed. To prevent this, an output of the H oscillator is compared with a reference H sync signal to detect deviations of frequency and phase. The H oscillator is automatically controlled with the detected output averaged. This circuit is called an AFC circuit.

In the N4SS chassis, a conventional AFC circuit is not employed but a new double AFC circuit built-in the TA1222N is used. Fig. 10-3 shows the AFC circuit and the block diagram of the circuit.

First, phases of a 32 fH counted-down signal and a H sync signal contained in broadcasting signal are compared in the AFCI loop and the loop develops an H pulse signal for the AFCII loop. That is, when a phase deference 01 exists in comparison of the phase of fH signal developed by counting down the 32 fH signal and the phase of H sync signal of the broadcasting signal, an error signal corresponding to the phase different is detected and a correction voltage V_1 corresponding to the error output is generated. With this correction voltage, the 32 fH oscillator circuit is controlled. The correction (control) voltage for the oscillator varies in direction of positive or negative corresponding to phase lead or lag of the fH pulse (developed by counting down) from the H sync signal. As the H oscillator (32 x fH), a voltage controlled oscillator (VCO), oscillation frequency and phase of which can be controlled with the control voltage is used.

Next, an H pulse signal is created from the fH signal counted down, and the pulse is used instead of the H sync signal in the AFCII circuit. The AFCII circuit differs in the loop of the count down circuit and H output circuit.

The AFCII circuit compares phase of a H BLK pulse created by waveform shaping a AFC pulse from the FBT and a phase of the H pulse, and detects an error component corresponding to the phase difference 02 (if exist) and develops a correction voltage V2 corresponding to the error, thereby controlling the phase of Q501 H out.

The H output control voltage varies in a positive or negative direction corresponding to the phase lead or lag of the H BLK pulse from that of the H pulse. The phase of H out is varied with the control voltage to make synchronization with the H pulse phase.

The purpose of the double AFC circuit employed this time

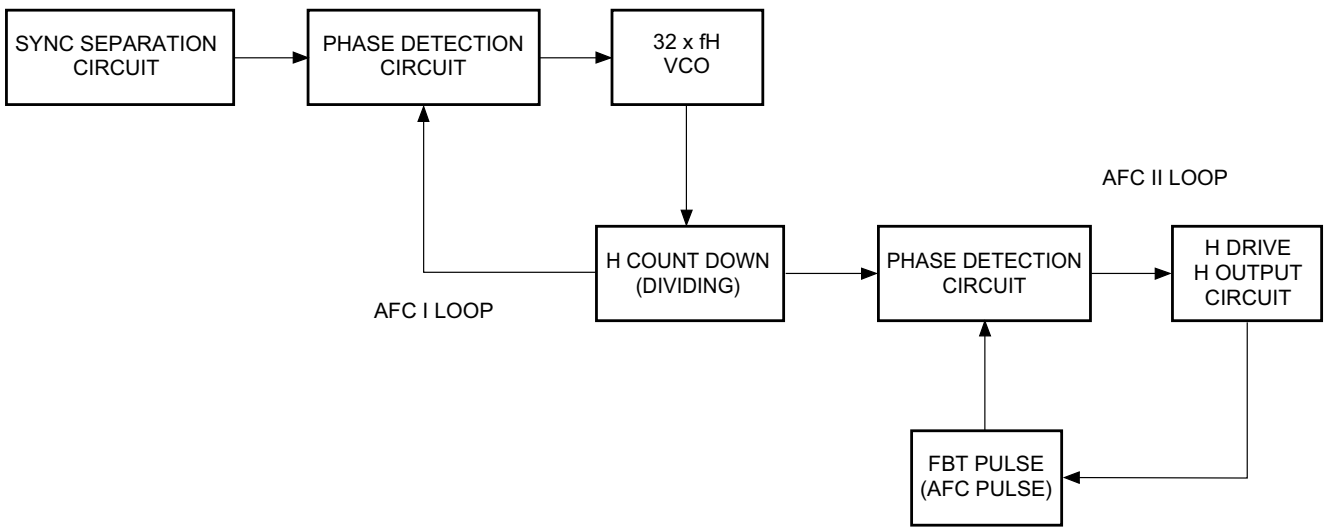


Fig. 10-3 H AFC circuit block diagram

is to improve horizontal jitter under signal reception in a poor electrical field. The jitter in the poor field strength and distortion due to phase difference are incompatible. That is,to improve the jitter under poor field strength, response speed must be slowed by lowering the AFC sensitivity. On the other hand, to improve distortion due to the phase difference, the response must be increased by increasing the AFC sensitivity.

In a conventional AFC circuit, setting of the sensitivity is carried out at one part only, so an compromise point for both characteristics must be found. However, with the double AFC circuit employed this time, for the jitter the AFCI loop works best with decreasing the sensitivity and for the phase distortion the AFCII loop works with increasing the sensitivity.

3. H OSCILLATOR CIRCUIT

3-1. Outline

A 503 kHz (32 x fH) voltage controlled type oscillator with a ceramic oscillation element is used to generate a clock pulse and the clock is counted down, thereby obviating the need of adjustments for both the H and V deflection process circuit.

3-2. Theory of Operation

(1) The H sync signal used as a reference signal enters from the sync separation circuit to the AFCI circuit. At the same time, the fH pulse created by counting down the 32 x fH pulse generated in the ceramic oscillator enters the H AFCI circuit. Phase difference between these two signals enters an integration circuit (low pas

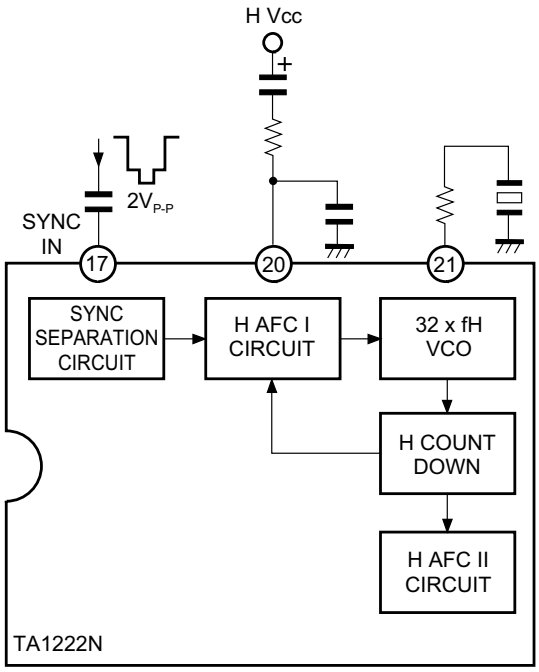


Fig. 10-4

filter) connected to pin 4 and converted into a DC voltage (AFC voltage).

(2) The AFC voltage controls frequency (32 x fH) of the oscillator (VCO).
Fig. 10-5 shows the control characteristics of the VCO.

(3) The H output is obtained by dividing the 32 x fH (503 kHz) of the oscillator with flip-flops. Fig. 10-6 shows the block diagram of this count down circuit.

(4) The V output is created by dividing the 32 x fH oscillator output into 1/8, and then by counting the 4 x fH pulse with a vertical counter which is reset with a V reset pulse (V sync output signal stated under sync separation).

(5) That is, the V output is not created by simply counting down the H by performing V synchronization with a V reset pulse entering within a window provided for V synchronization --- called direct type sync system, thus, the circuit can work for non standard signals.

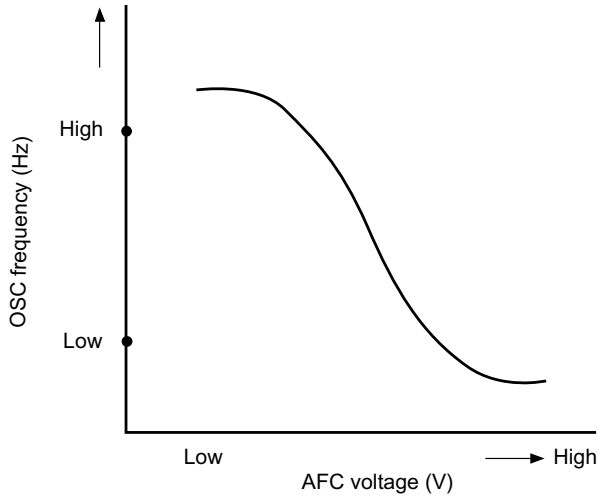


Fig. 10-5

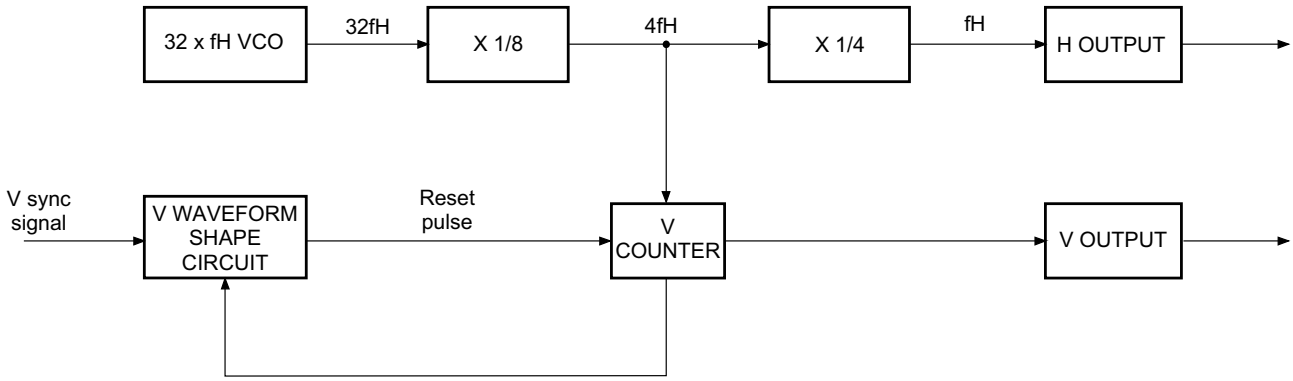


Fig. 10-6 Block diagram of H, V count down circuits

NOTES

SECTION XI
VERTICAL OUTPUT CIRCUIT

1. OUTLINE

As can be seen from the block diagram, the sync circuit and the V trigger circuit are contained in Q501 (TA1222N), and the sawtooth generation circuit and amplifier (V drive circuit) contained in Q302 (TA8859AP). The output circuit and pump-up circuit circuits are included in Q301 (TA8427K).

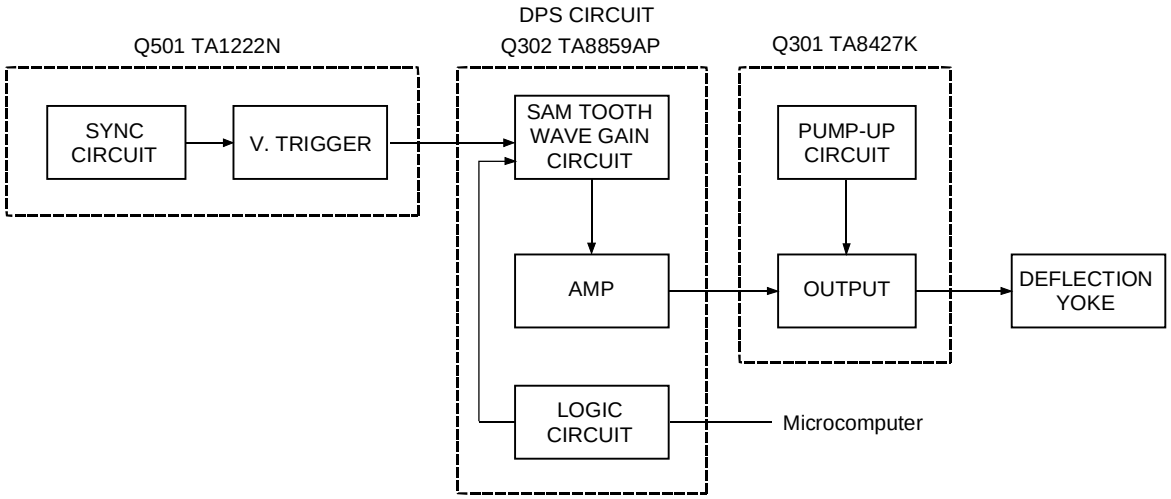


Fig. 11-1 Block diagram of V deflection circuit

1-1. Theory of Operation

The purpose of the V output circuit is to provide a sawtooth wave signal with good linearity in V period to the deflection yoke.

When a switch S is opened, an electric charge charged up to a reference voltage VP discharges in an constant current rate, and a reference sawtooth voltage generates at point a. This voltage is applied to (+) input (non-inverted input) of an differential amplifier, A. As the amplification factor of A is sufficiently high, ⓐ deflection current flows so that the voltage V2 at point ⓒ becomes equal to the voltage at point ⓐ.

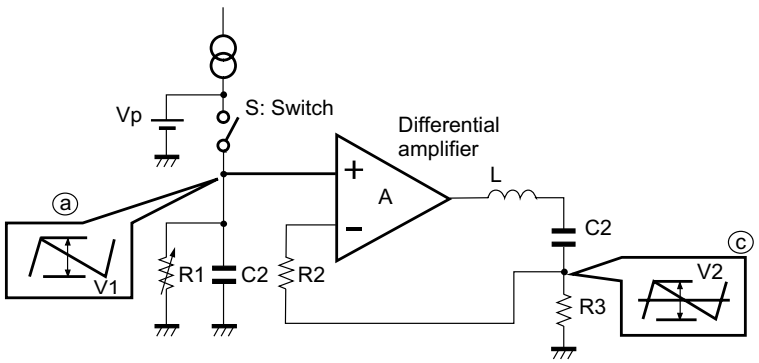


Fig. 11-2

2. V OUTPUT CIRCUIT

2-1. Actual Circuit

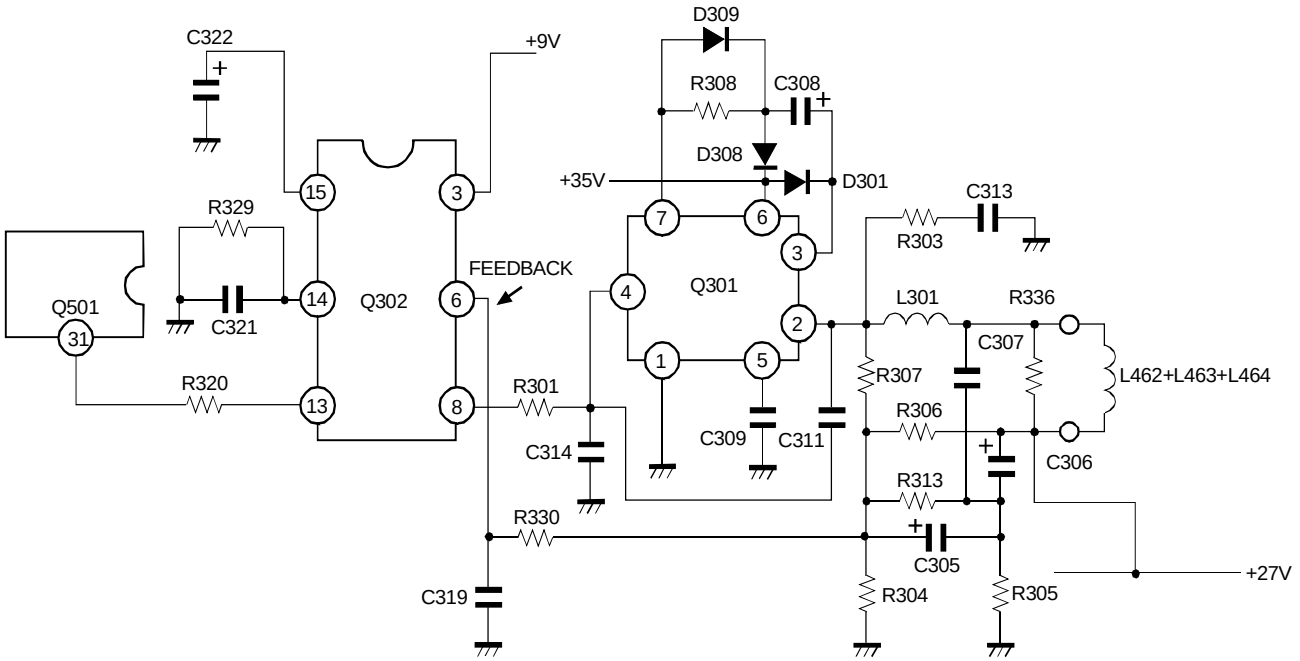


Fig. 11- 3

2-2. Sawtooth Waveform Generation

2-2-1. Circuit Operation

The sawtooth waveform generation circuit consists of as shown in Fig. 11-4. When a trigger pulse enters pin 13, it is differentiated in the waveform shape circuit and only the falling part is detected by the trigger detection circuit, to the waveform generation circuit is not susceptible to variations of input pulse width.

The pulse generation circuit also works to fix the V ramp voltage at a reference voltage when the trigger pulse enters, so it can prevent the sawtooth wave start voltage from variations by horizontal components, thus improving interlacing characteristics.

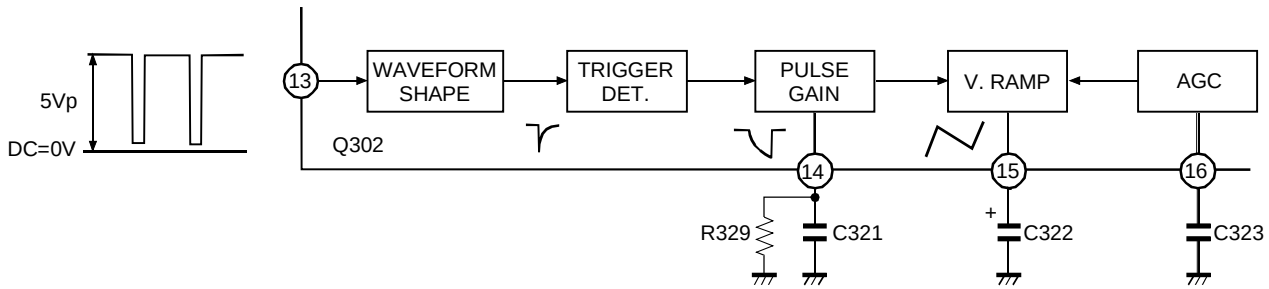


Fig. 11-4

2-3. V Output

2-3-1. Circuit Operation

The V output circuit consists of a V driver circuit Q302, Pump-up circuit and output circuit Q301, and external circuit components.

(1) Q2 amplifies its input fed from pin 4 of Q301, Q3, Q4 output stage connected in a SEPP amplifies the current and supplies a sawtooth waveform current to a deflection yoke. Q3 turns on for first half of the scanning period and allows a positive current to flow into the deflection yoke (Q3➡DY➡C306➡R305➡GND), and Q4 turns on for last half of the scanning period and allows a negative current to flow into the deflection yoke (R305➡C306➡DY➡Q4). These operations are shown in Fig. 11-5.

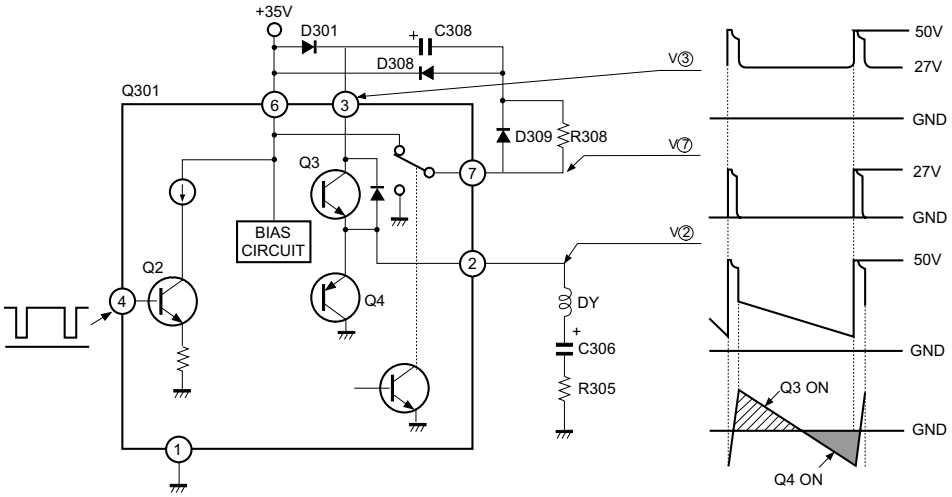


Fig. 11-5 V output circuit

(2) In Fig. 11-6 (a), the power Vcc is expressed as a fixed level, and the positive and negative current flowing into the deflection yoke is a current (d) = current (b) + (c) in Fig. 11-6, and the emitter voltage of Q3 and Q4 is expressed as (e).

(3) Q3 collector loss is i1 x Vce1 and the value is equal to multiplication of Fig. 11-6 (b) and slanted section of Fig. 11-6 (e), and Q4 collector loss is equal to multiplication of Fig. 11-6 (c) and dotted section of Fig. 11-6 (e).

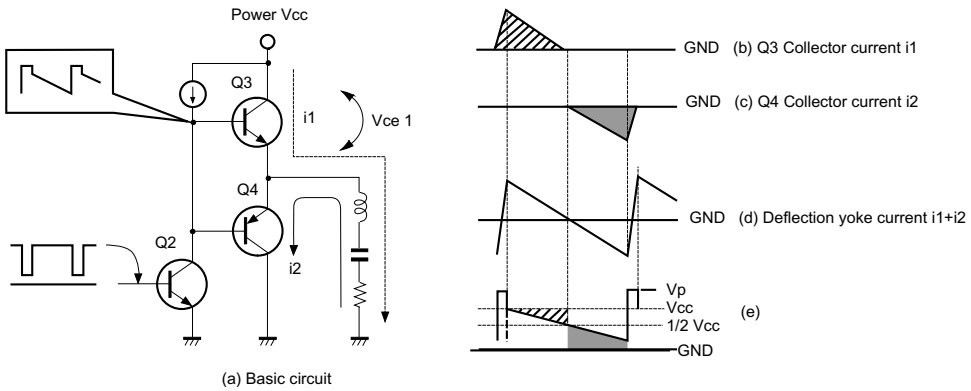


Fig. 11-6 Output stage operation waveform

(4) To decrease the collector loss of Q3, the power supply voltage is decreased during scanning period as shown in Fig. 11-7, and VCE1 decreases and the collector loss of Q3 also decreases.

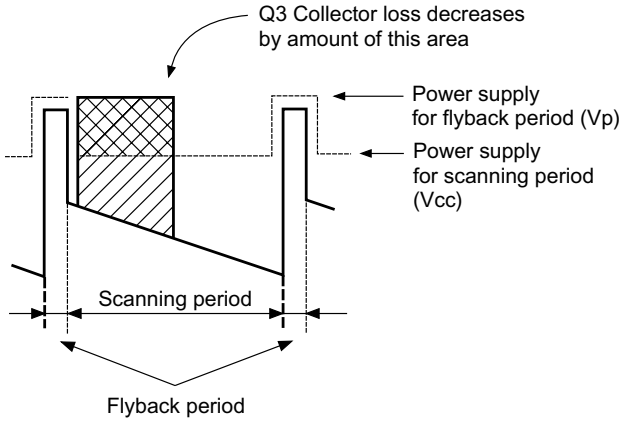


Fig. 11-7 Output stage power supply voltage

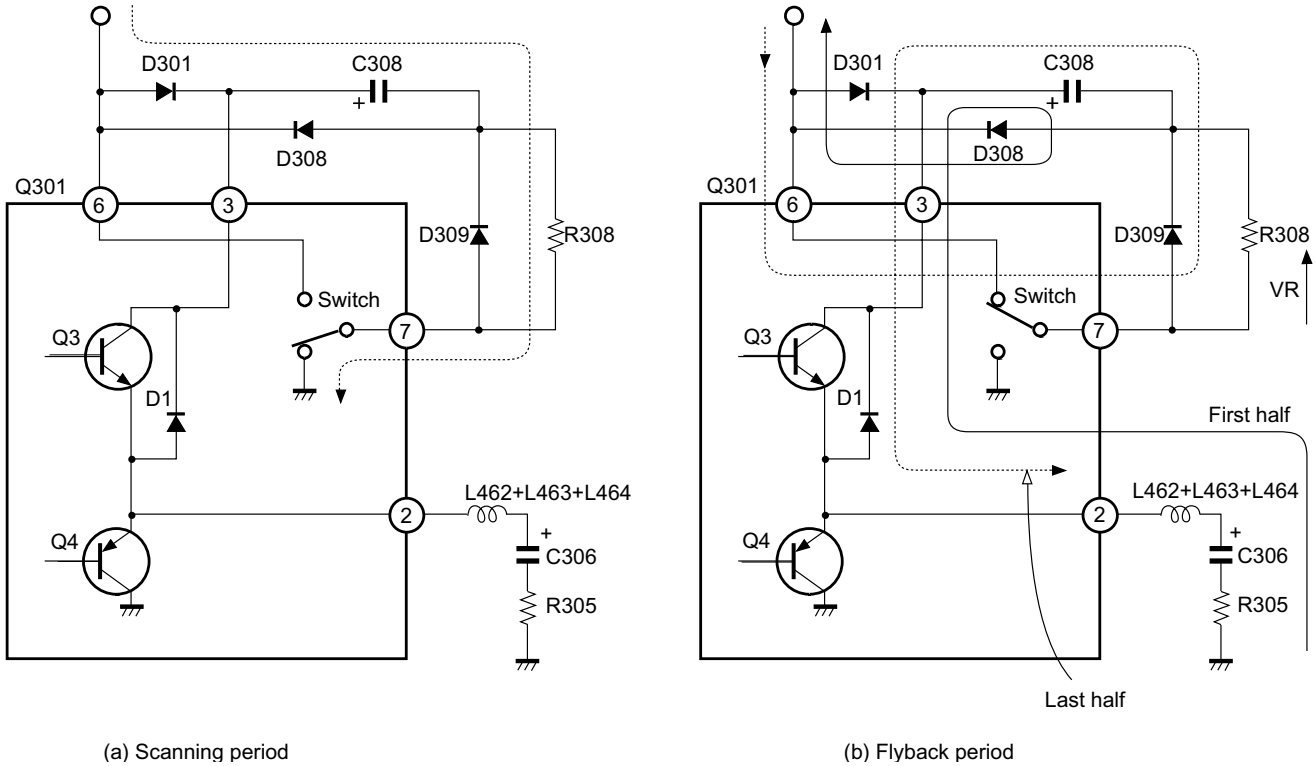
(5) In this way, the circuit which switches power supply circuit during scanning period and flyback period is called a pump-up circuit. The purpose of the pump-up circuit is to return the deflection yoke current rapidly for a short period (within the flyback period) by applying a high voltage for the flyback period. The basic operation is shown in Fig. 11-8.

(6) Since pin 7 of a transistor switch inside Q301 is connected to the ground for the scanning period, the power supply (pin 3) of the output stage shows a voltage of (VCC-VF), and C308 is charged up to a voltage of (VCC-VF--VR) for this period.

(7) First half of flyback period
Current flows into L462➡D1➡C308➡D308➡VCC (+35V)➡GND➡R305➡C306➡L462+L463+L464 in this order, and the voltage across these is:
VP=VCC+VF+(VCC-VF-VR)+VF about 50V is applied to pin 3. In this case, D301 is cut off.

(8) Last half of flyback period
Current flows into VCC ➡ switch➡ D309 ➡C308 ➡ Q301(pin3)➡Q3➡L462+L463+L464➡C306➡R305 in this order, and a voltage of VP=VCC-VCE (sat)-VF+(VCC-VF-VR)-VCE (sat), about 40V is applied to pin 3.

(9) In this way, a power supply voltage of about 27V is applied to the output stage for the scanning period and about 50V for flyback period.



(a) Scanning period

(b) Flyback period

Fig. 11-8

2-4. V Linearity Characteristic Correction

2-4-1. S-character Correction

(Up-and Down-ward Extension Correction)

A parabola component developed across C306 is integrated by R306 and C305, and the voltage is applied to pin 6 of Q302 to perform S-character correction.

2-4-2. Up-and Down-ward Linearity Balance

A voltage developed at pin 2 of Q301 is divided with resistors R307 and R303, and the voltage is applied to pin 6 of Q301 to improve the linearity balance characteristic. Moreover, the S-character correction, up- and down-ward balance correction, and M-character correction are also performed through the bus control.

3. PROTECTION CIRCUIT FOR V DEFLECTION STOP

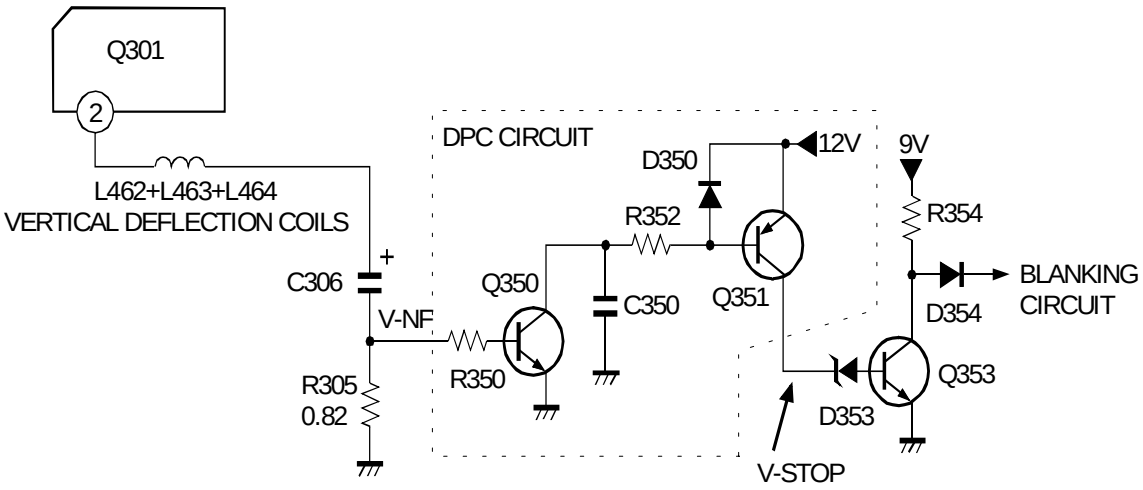


Fig. 11-9

When the deflection current is not supplied to the deflection coils, one horizontal line appears on the screen. If this condition is not continued for a long time, no trouble will occur in a conventional TV. But in the projection TV, all the electron beams are directly concentrated at the fluorescent screen because of no shadow mask used, and burns out the screen instantly.

To prevent this, the stop of the V deflection is detected when the horizontal one line occurs, and the video signals are blanked out so that the electron beams are not emitted.

When the V deflection circuit is operating normally, a sawtooth wave voltage is obtained across (R305), so Q350 repeats on-off operation in cycle of V sync. In this case, the collector voltage of Q35 is set to develop less than (12V-V_{BE} (Q351)) with R352 and C350 as shown in Fig. 4-8. Accordingly, Q351 and Q353 are continuously turned on. As a result, diode D354 is turned off, giving no influence on the blanking operation.

Next, when the V deflection stops, the voltage across (R305) does not develop, so Q350 turns off, and both the Q351 and Q353 are turned off. Then, the picture blanking terminal pin 13 of ICA05 is set to high through R354 and D354 connected to 90V power line, BLANKING CIRCUIT ON thus cutting off the projection tubes.

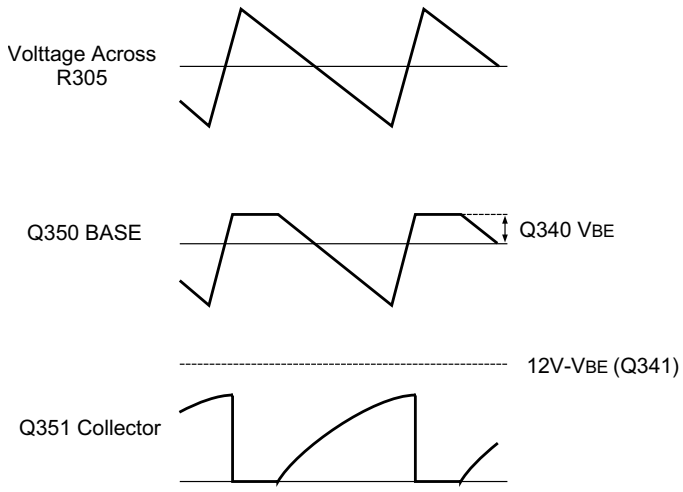


Fig. 11-10

3-1. +35V Over Current Protection Circuit

The over current protection circuit cuts off the power supply relay when it detects abnormal current increased in the +35V power line due to failure of the vertical deflection circuit.

3-1-1. Theory of operation

Fig. 11-11 shows the circuit diagram of the over current protection circuit. When the load current of the +35V line increases, the voltage across a resistor of T370 will also increase. When the voltage increases across R370. and the voltage developed across R371 becomes higher than the Vbs of Q370, Q370 turns on and a voltage develops across R374 due to the collector current flowing. When this voltage increases to a value higher than about 13V, Z801 operates, thus cutting off the power relay. When the circuit operates, a power LED provided will turn on and off in red.

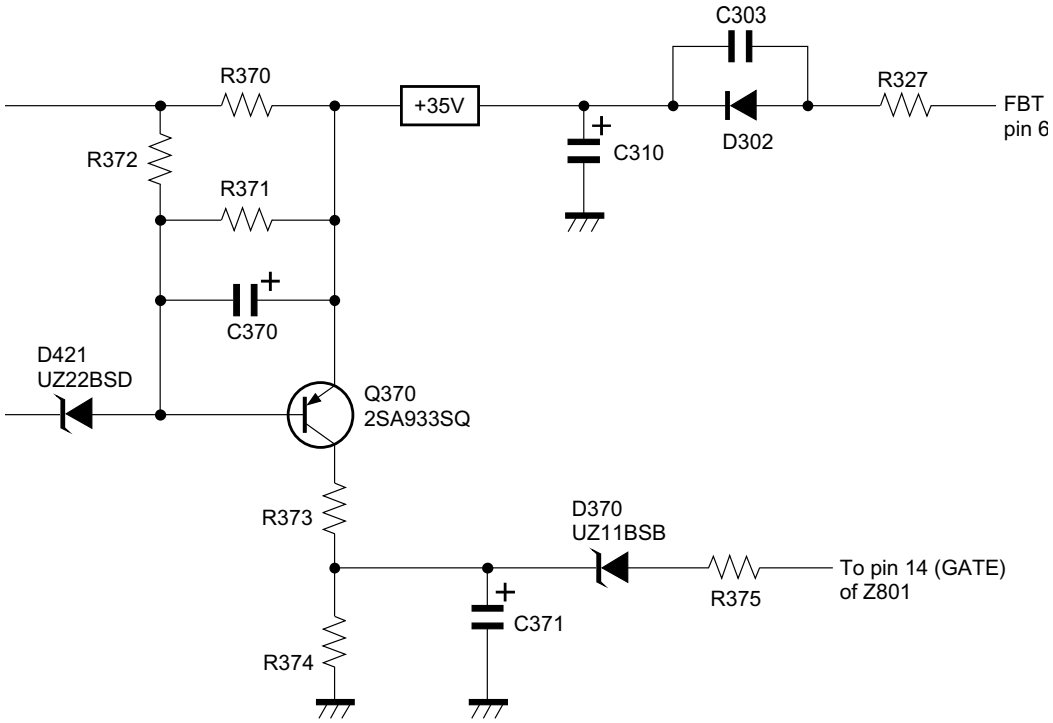


Fig. 11-11

SECTION XII
HORIZONTAL DEFLECTION CIRCUIT

1. OUTLINE

The H deflection circuit works to deflect a beam from left to right by flowing a sawtooth waveform of 15.734 kHz into the DY H deflection coil.

2. HORIZONTAL DRIVE CIRCUIT

The H drive circuit works to start the H output circuit by applying HVCC (Q501 DEF power source) to pin 22 of Q501 (TA1222N) and a bias to the H drive transistor Q402 at the main power on.

2-1. Theory of Operation

(1) When the power switch is on, the main power supply of 125V starts to rise. At the same time, AF power supply 25V also rises.

(2) With 25V line risen, Q430 base voltage which is created by dividing the audio power with R433 and D430 also rises. Then, the transistor Q430 turns on and the HVCC is applied from the audio power line through R432 and D431 to pin 22 of Q501.

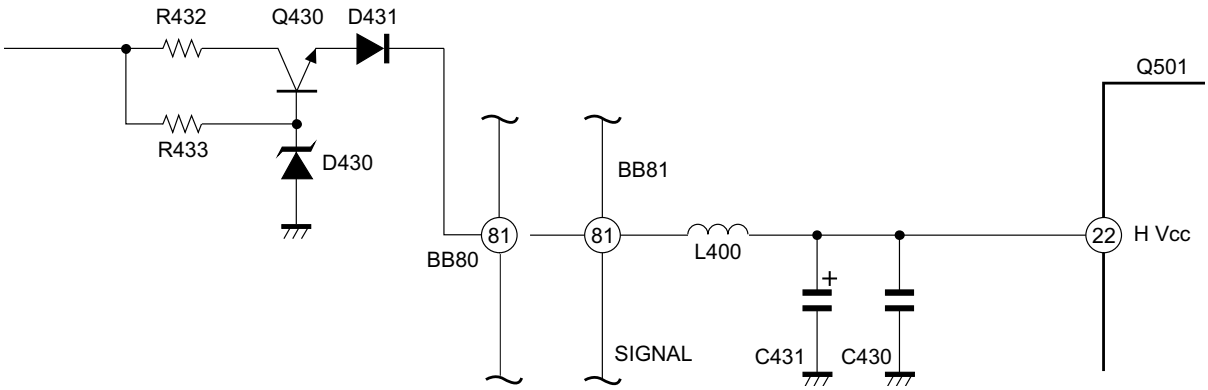


Fig. 12-1 H drive circuit block diagram

3. BASIC OPERATION OF HORIZONTAL DRIVE

A sufficient current must flow into base of the horizontal output transistor to rapidly make it into a saturated (ON) condition or a cut off (OFF) condition. For this purpose, a drive amplifier is provided between the oscillator circuit and the output circuit to amplify and to waveshape the pulse voltage.

3-1. Theory of Operation

(1) The horizontal drive circuit works as a so called switching circuit which applies a pulse voltage to the output transistor base and makes the transistor on when the voltage swings in forward direction and off in reverse direction.

(2) To turn on the output transistor completely and to make the internal impedance low, a sufficiently high, forward drive voltage must be applied to the base and heavy base current ib must be flown. On the contrary, to completely turn off the transistor, a sufficiently high, reverse voltage must be applied to the base.

(3) When the transistor is on (collector current is maximum) condition with the sufficiently high forward voltage applied to the base, the transistor can not be turned off immediately, if a reverse base bias is applied to the base because minority carriers storaged in the base can not be reduced to zero instantly. That is, a reverse current flows through an external circuit and gradually reduces to zero. The time lag required for the base current to disappear is called a storage time and falling time.

(4) To shorten the storage time and the falling time, a sufficiently high reverse bias voltage must be applied to allow a heavy reverse current to flow. This operation also stabilizes operation of the horizontal output transistor.

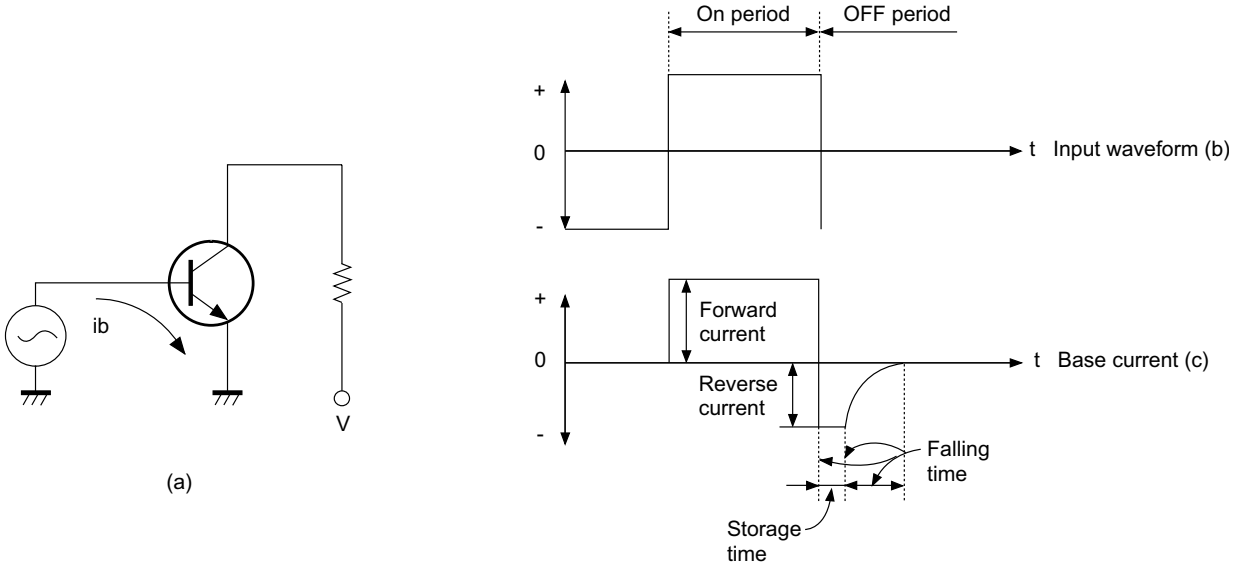


Fig. 12-2

3-2. Drive System

3-2-1. ON drive system

When the drive transistor is on, the horizontal output transistor also turns on.

Merit:

- The base current can be precisely controlled without being affected by variation of pulse width which is caused by the horizontal oscillator circuit and the drive circuit.

Demerit:

- It is difficult to flow a reverse bias current to the horizontal output transistor to eliminate its storage carrier for transient period of on to off period for the horizontal output transistor.

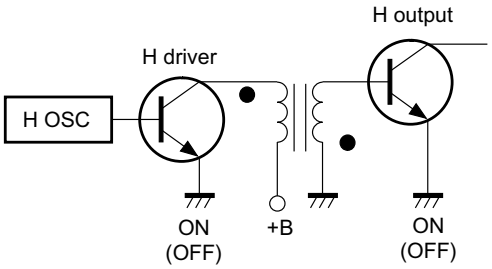


Fig. 12-3

3-2-2. OFF drive system

When the drive transistor is on, the horizontal output transistor is off.

Merit:

- Energy balance between on and off periods of the drive circuit is better, and the circuit can be simplified.
- Reverse base current of the horizontal output transistor can be controlled easily.

Demerit:

- Base-emitter forward current flowing into the horizontal output transistor is susceptible to on-period variation of the drive transistor.

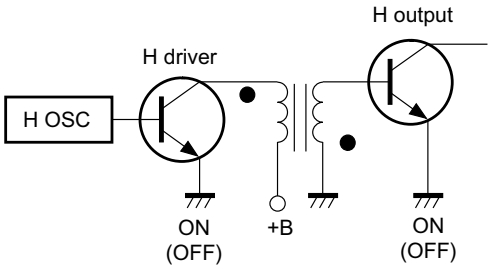


Fig. 12-4

3-3. Circuit Description

In the N5SS chassis, the off drive system is employed.

(1) When Q1 inside Q501 is turned on, Q402 base is forward biased through 9 V ➡ pin 22 of Q501 (H. VCC)➡pin 23 of Q501 (H. Out) ➡ R411/R410 resistor divider, and then, Q402 collector current flows through 125V➡R416➡T401. In this case, the H output transistor Q404 turns on with the base-emitter reverse biased because of the off drive system employed.

(2) On the contrary, when Q1 inside IC501 is off (pin 8 is 0V), base-emitter bias of Q402 becomes 0V and Q402 turns off, and a collector pulse as shown in Fig. 12-5 develops at the collector.
The voltage is stepped down and Q404 is forward biased with this voltage, thus turning on Q404.

(3) In this way, by stepping down the voltage developed at primary winding of the drive transformer and by applying it to Q404, a sufficient base current flows into Q404 base, thereby switching the Q404.

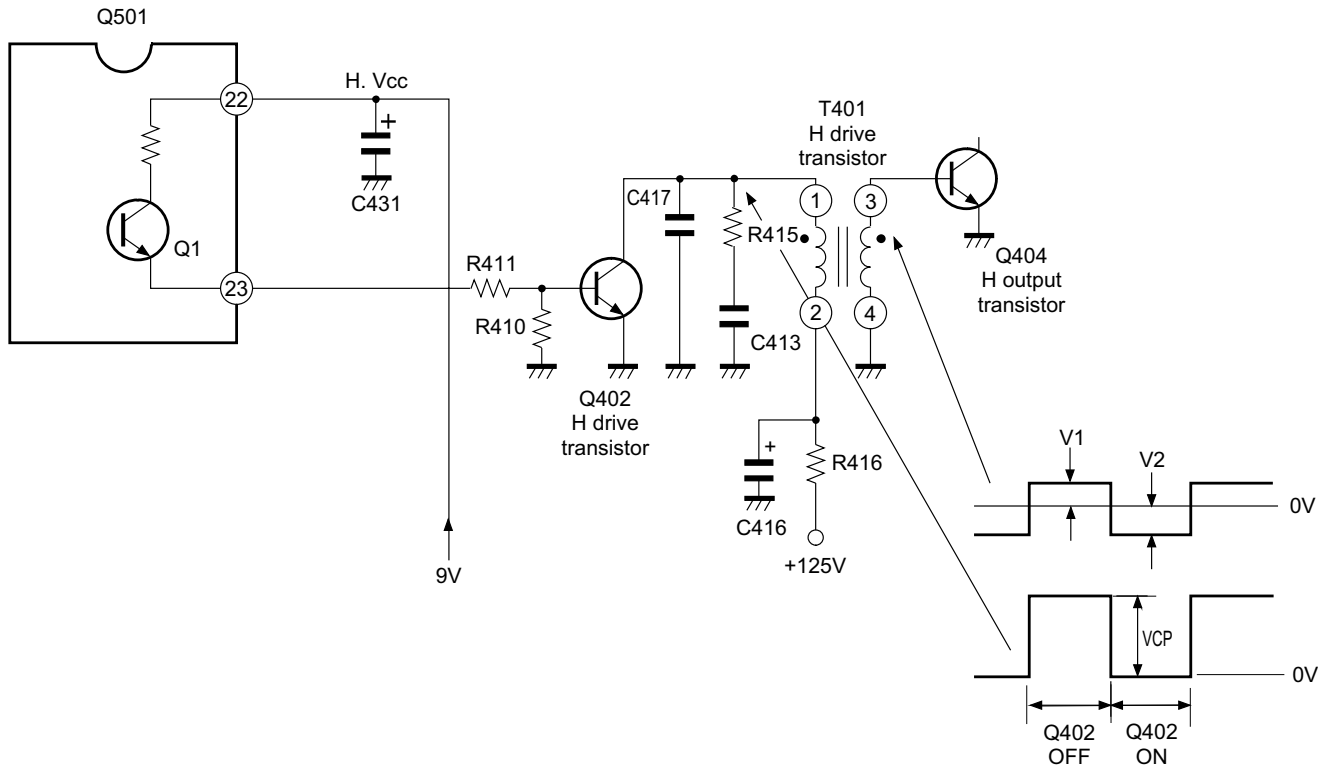


Fig. 12-5

4. HORIZONTAL OUTPUT CIRCUIT

The horizontal output circuit applies a 15.734 kHz sawtooth wave current to the deflection coil with mutual action of the horizontal output transistor and the damper diode, and deflects the electron beam from left to right in horizontal direction.

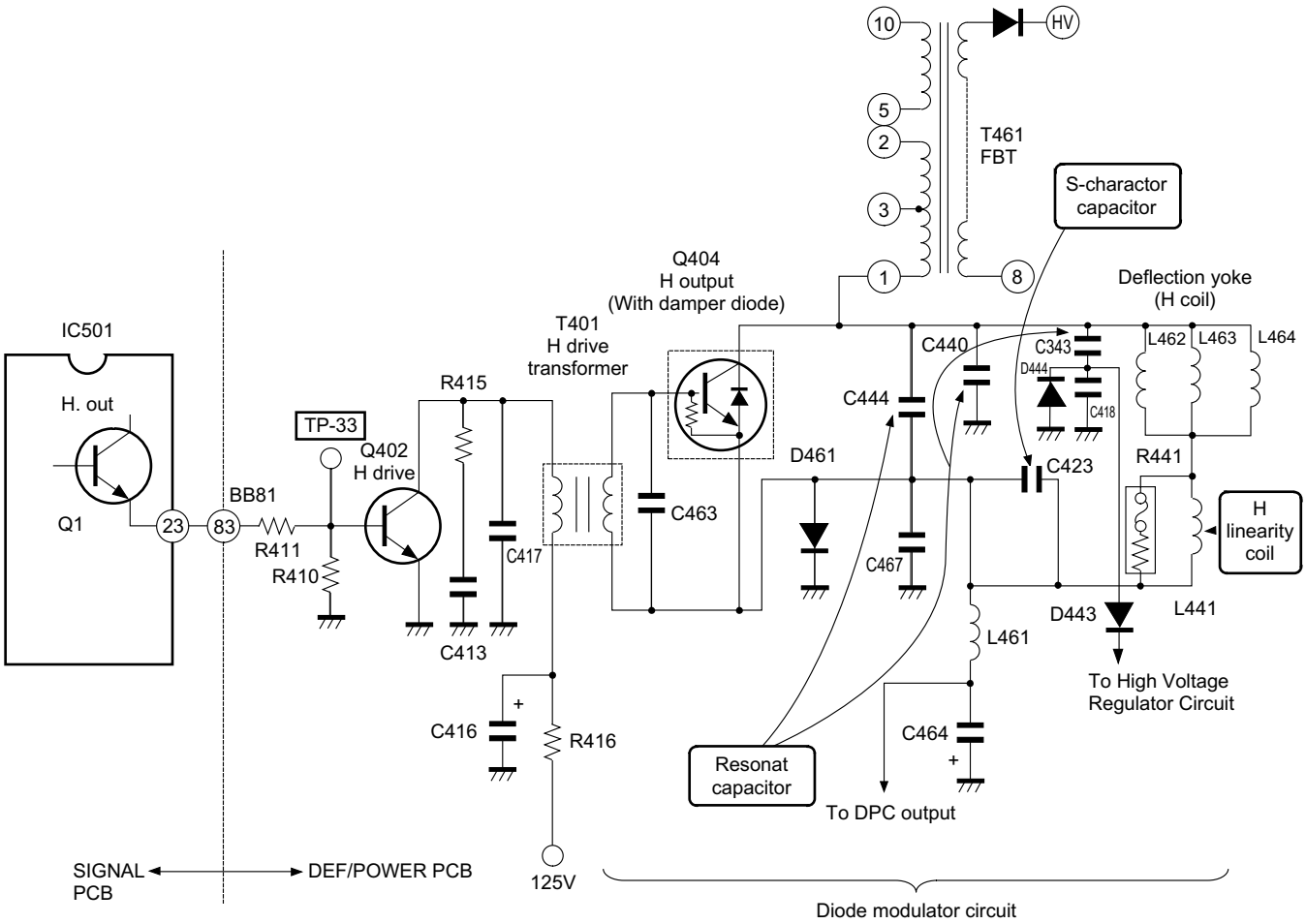


Fig. 12-6

4-1. Theory of Operation

4-1-1. Operation of Basic Circuit

(1) To perform the horizontal scanning, a 15.734 kHz sawtooth wave current must be flown into the horizontal deflection coil. Theoretically speaking, this operation can be made with the circuit shown in Fig. 12-7 a and b.

(2) As the switching operation of the circuit can be replaced with switching operation of a transistor and a diode, the basic circuit of the horizontal output can be expressed by the circuit shown in Fig. 12-7 a. That is, the transistor can be turned on or off by applying a pulse across the base emitter. A forward switching current flows for on-period, and a reverse switching current flows through the diode for off-period. This switching is automatically carried out. The diode used for this purpose is called a damper diode.

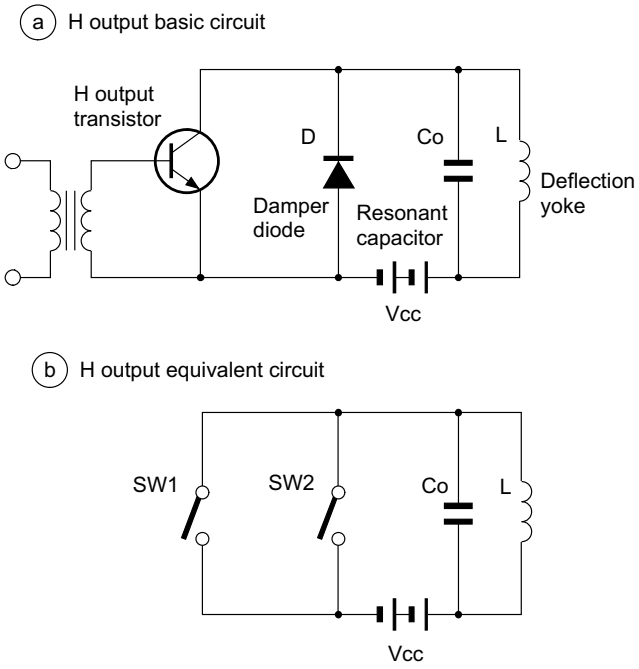


Fig. 12-7

Description of the basic circuit

1. t1~t2:

A positive pulse is applied to base of the output transistor from the drive circuit, and a forward base current is flowing. The output transistor is turned on in sufficient saturation area. As a result, the collector voltage is almost equal to the ground voltage and the deflection current increases from zero to a value in proportionally. (The current reaches maximum at t2, and a right half of picture is scanned up to this period.)

2. t2:

The base drive voltage rapidly changes to negative at t2 and the base current becomes zero. The output transistor turns off, collector current reduces to zero, and the deflection current stops to increase.

3. t2~t3:

The drive voltage turns off at t2, but the deflection current can not reduce to zero immediately because of inherent nature of the coil and continues to flow, gradually decreasing by charging the resonant capacitor C0. At the same time, the capacitor voltage or the collector voltage is gradually increases, and reaches maximum voltage when the deflection current reaches zero at t3. Under this condition, all electro-magnetic energy in the deflection coil at t2 is transferred to the resonant capacitor in a form of electrostatic energy.

4. t3~t4:

Since the charged energy in the resonant capacitor discharges through the deflection coil, the deflection current increases in reverse direction, and voltage at the capacitor gradually reduces. That is, the electrostatic energy in the resonant capacitor is converted into a electromagnetic energy in this process.

5. t4:

When the discharge is completed, the voltage reduces to zero, and the deflection current reaches maximum value in reverse direction. The t2~t4 is the horizontal flyback period, and the electron beam is returned from right end to the left end on the screen by the deflection current stated above. The operation for this period is equivalent to a half cycle of the resonant phenomenon with L and C0, and the flyback period is determined by L and C0.

6. t4~t6:

For this period. C0 is charged with the deflection current having opposite polarity to that of the deflection current stated in "3.", and when the resonant capacitor voltage exceeds VCC, the damper diode D conducts. The deflection current decreases along to an exponential function (approximately linear) curve and reaches zero at t6. Here, operation returns to the state described under "1.", and the one period of the horizontal scanning completes. For this period a left half of the screen is scanned.

In this way, in the horizontal deflection scanning, a current flowing through the damper diode scans the left half of the screen; the current developed by the horizontal output transistor scans the right half of the screen; and for the flyback period, both the damper diode and the output transistor are cut off and the oscillation current of the circuit is used. Using the oscillation current improves efficiency of the circuit. That is, about a half of deflection current (one fourth in terms of power) is sufficient for the horizontal output transistor.

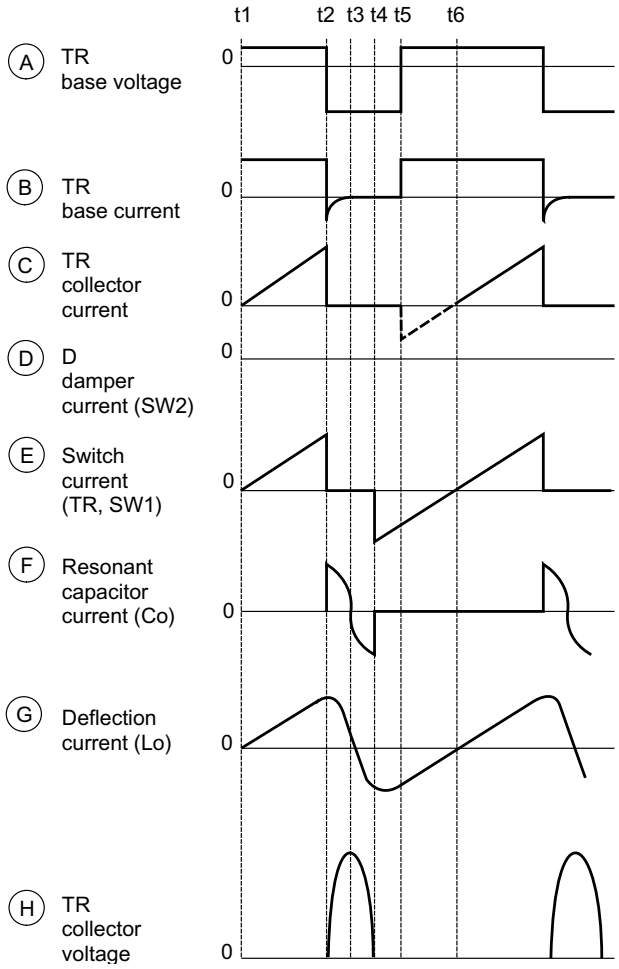


Fig. 12-8

Amplitude Correction

To vary horizontal amplitude, it is necessary to vary a sawtooth wave current flowing into the deflection coil. These are two methods to vary the current; a method which varies L_H by connecting a variable inductance L in series with the deflection yoke, and a method which varies power supply voltage (across S-character capacitor) for the deflection yoke.

As the DPC circuits is used in the this chassis, the later method which varies the deflection yoke power supply voltage by modifying the bus data is used.

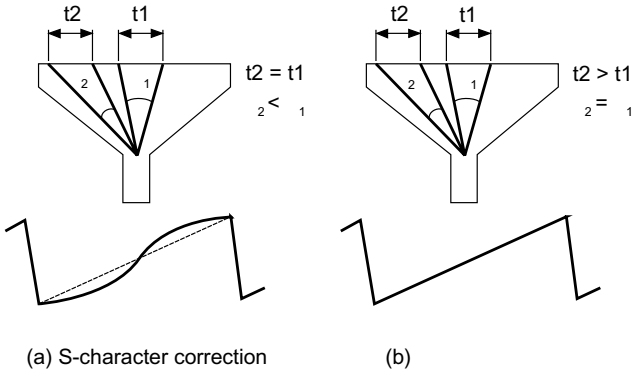


Fig. 12-9

4-1-2. Linearity Correction (LIN)

(1) S-curve Correction (S Capacitor)

Pictures are expanded at left and right ends of the screen even if a sawtooth current with good linearity flows in the deflection coil when deflection angle of a picture tube increases. This is because projected image sizes on the screen are different at screen center area and the circumference area as shown in Fig. 12-9. To suppress this expansion at the screen circumference, it is necessary to set the deflection angle q_1 to a large value (rapidly deflecting the electron beam) at the screen center area, and to set the deflection angle q_2 to a small value (scanning the electron beam slowly) at the circumference area as shown in Fig. 12-9.

In the horizontal output circuit shown in Fig. 12-10, capacitor CS connected in series with the deflection coil LH is to block DC current. By properly selecting the value of CS and by generating a parabolic voltage developed by integrating the deflection coild current across the S capacitor, and by varying the deflection yoke voltage with the voltage, the scanning speed is decreased at beginning and end of the scanning, and increased at center area of the screen. The S curve correction is carried out in this way, thereby obtaining pictures with good linearity.

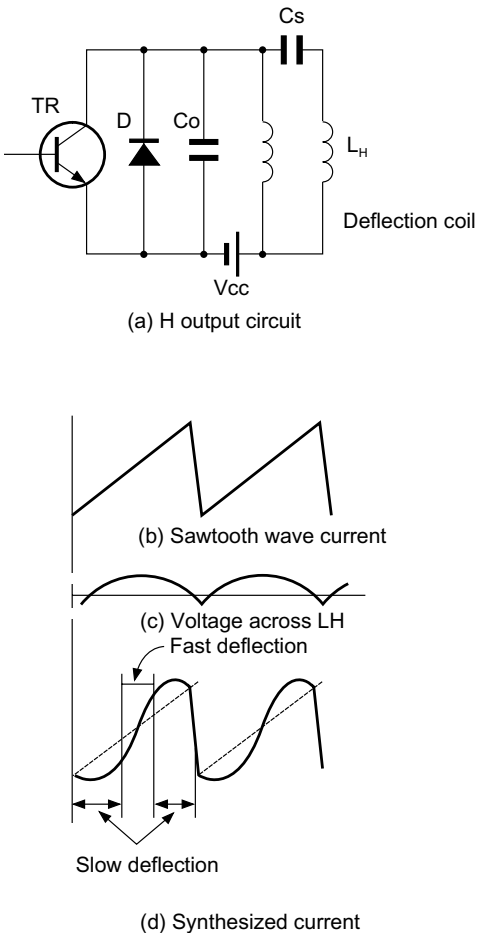
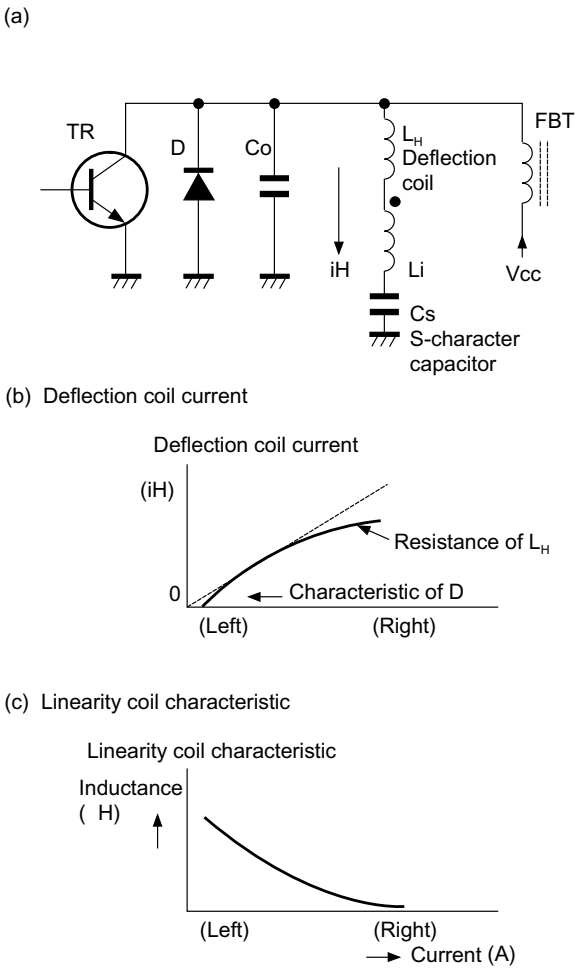


Fig. 12-10

(2) Left-right Asymmetrical Correction (LIN coil)

In the circuit shown in Fig. 12-11 a, the deflection coil current iH does not flow straight as shown by a dotted line in the figure b if the linearity coil does not exist, by flows as shown by the solid line because of effect of the diode for a first scanning (screen left side) and effect of resistance of the deflection coil for later half period of scanning (screen right side). That is, the deflection current becomes a sawtooth current with bad linearity, resulting in reproducing of asymmetrical pictures at left and right sides of the screen (left side expanded, right side compressed).

When a horizontal linearity oil L1 with a current characteristic as shown in figure c is used, left side picture will be compressed and right side picture will be expanded because the inductance is high at the left side on the screen and low at the right side. The left-right asymmetrical correction is carried out in this way, and pictures with good linearity in total are obtained.



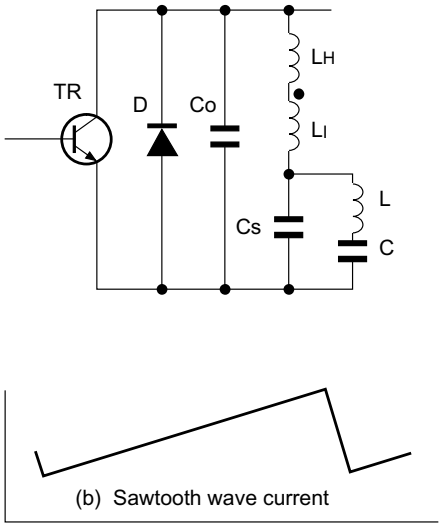


Fig. 12-12

Fig. 12-11 Linearity coil

4-2. White Peak Bending Correction Circuit

4-2-1. Outline

White peak area in screen picture may sometimes cause bending in picture. See figure below.

In TP48E60 series, correction signal which consists of video signal and video ripple in video output circuit power supply 200V is input to pin 24 (Bending correction terminal) of Q501. This corrects white peak bending.

4-2-2. Operation theory

Fig. 12-13 shows circuit diagram. From R, G and B output (pins 41, 42 and 43 of Q501), video signal is taken in the dividing ratio of resistor R375 and R378. After that, it suffers DC cut by C360 and integration by R369 and C415, then is input to pin 24 of Q501. On the other hand, video ripple in video output circuit power supply 200V suffers DC cut by C475, and is inverted in Q470, then input to pin 24 of Q501 via C481. Pin 24 of Q501 is a bending correction terminal. The voltage which is applied to this terminal, controls phase of video signal to correct white peak bending.

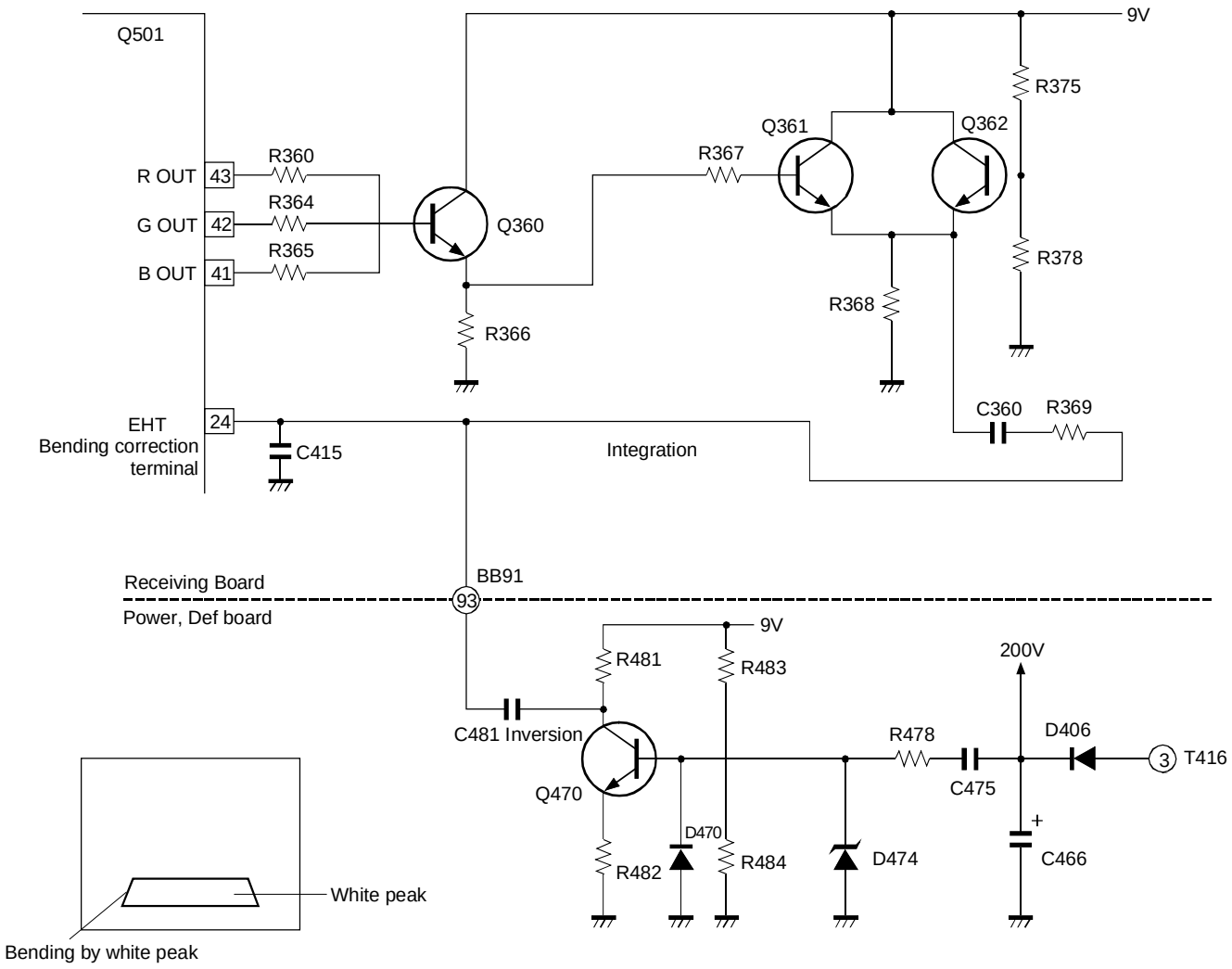


Fig. 12-13 White peak bending correction circuit

4-3. H Blanking

4-3-1. Outline

The H blanking circuit applies a blanking precisely for the horizontal flyback period so that undesirable pictures folding does not appear at screen ends.

This unit allows the users to adjust an horizontal amplitude adjustment, so, picture quality at screen ends will be improved. This is one of the purposes of the blanking circuit.

4-3-2. Theory of Operation

The H blanking circuit determines the flyback period precisely from the AFC pulse in the FBT and applies the period to emitter of the video output stage transistor on the CRT-D PC board.

4-3-3. Circuit Operation

As can be seen from Fig. 12-14, the flyback period of the AFC pulse in the FBT starts at a negative side from 0V. To detects this, the DC component is cut with C493. This is, C493 is always charged through D487 with a negative side (about -17V) of the AFC pulse. As a result, a voltage at point A in the waveform rises from the ground level. This waveform is sliced in a circuit (R410, C492, D486) to detect the flyback period. Thus obtained voltage is applied to Q901, Q903, and Q905 through D912 ~ D914 and cuts off them thereby blanking the resters.

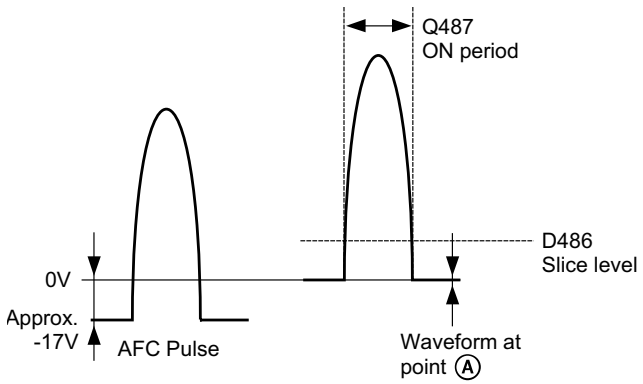


Fig. 12-14

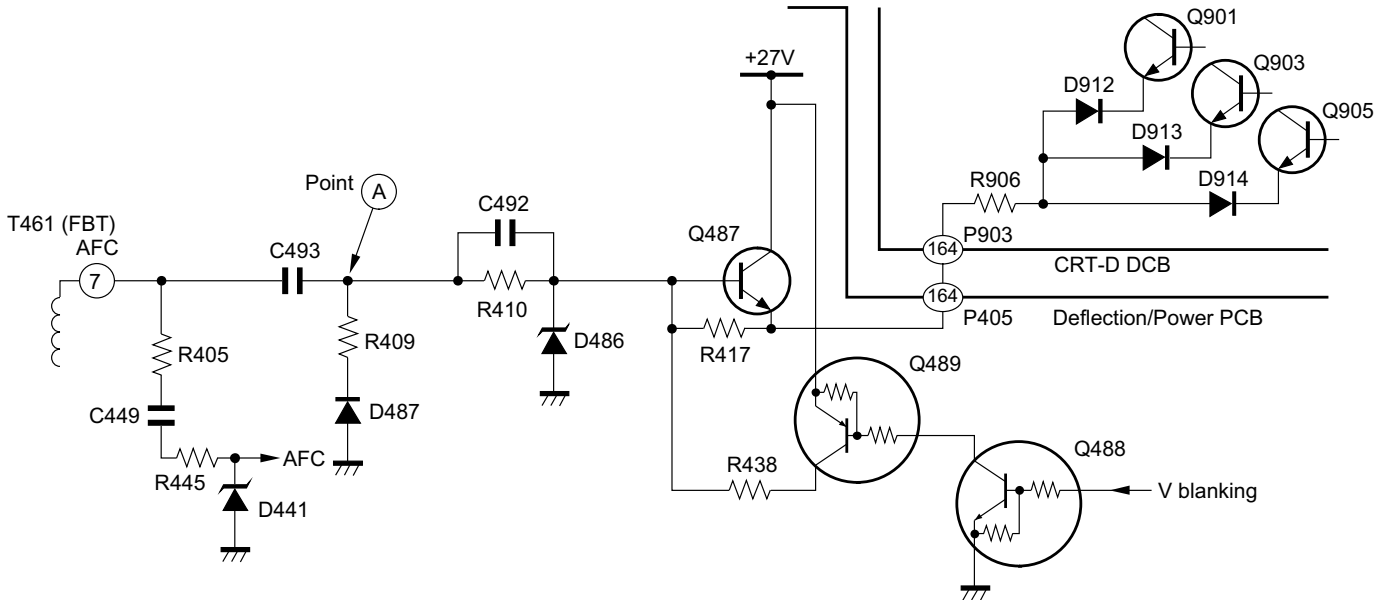


Fig. 12-15

4-4. 200V Low Voltage Protection

4-4-1. Outline

CPT. To prevents this, a 200V low voltage protection circuit is provided.

4-4-2. Theory of Operation

Fig. 12-16 shows a connection diagram.

Under a normal condition Q340 is always on because of about 210V supplied from the 200V line. Accordingly Q340 collector is kept at about 6.2V or the zener voltage of D341 and Q341 is turned off.

If some abnormality occurs and 200V line voltage lowers by less than about 160V. Q340 turns off and its collector voltage rises. So Q341 turns on. With Q341 turned on the voltage at pin 14 of Z801 (expander) exceeds a threshold voltage and pin 16 of Z80 is high level and makes the power relay turn off.

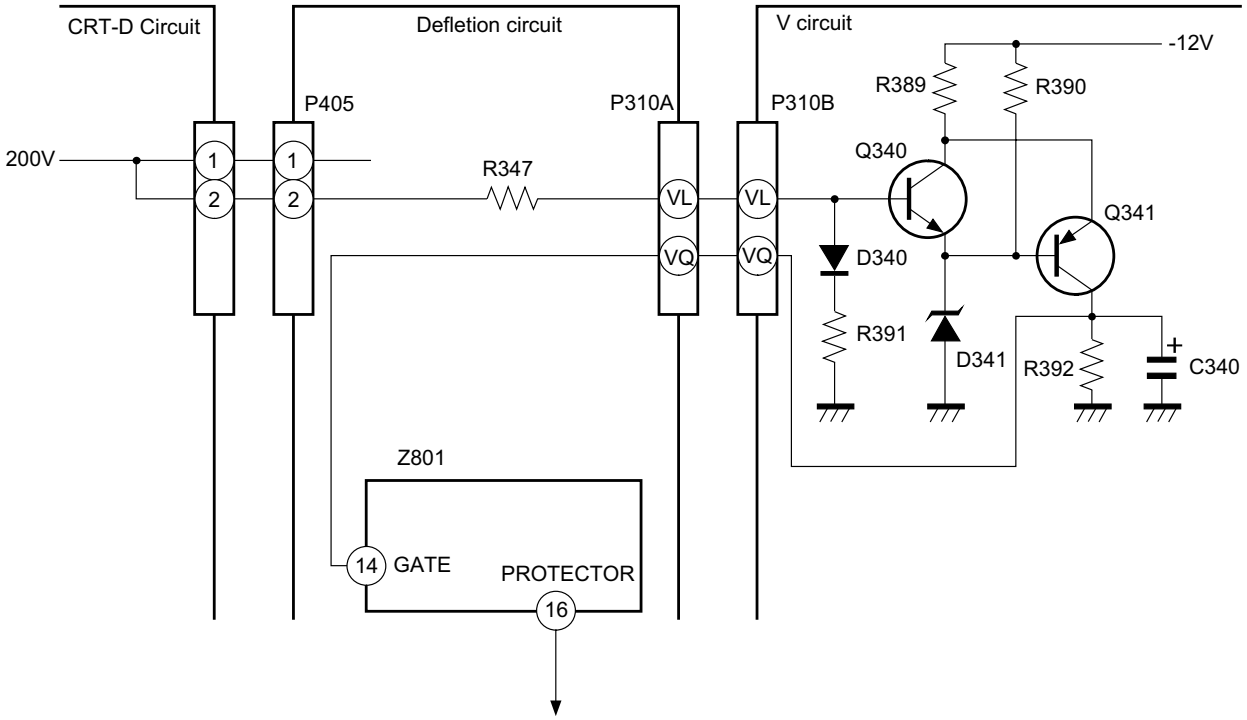


Fig. 12-16

5. HIGH VOLTAGE GENERATION CIRCUIT

The high voltage generation circuit develops an anode voltage for the picture tube, focus, screen, CRT heater, video output (210V) and so on by stepping up the pulse voltage developed for flyback period of the horizontal output circuit with the FBT, and supplies the power to various circuit.

5-1. Theory of Operation

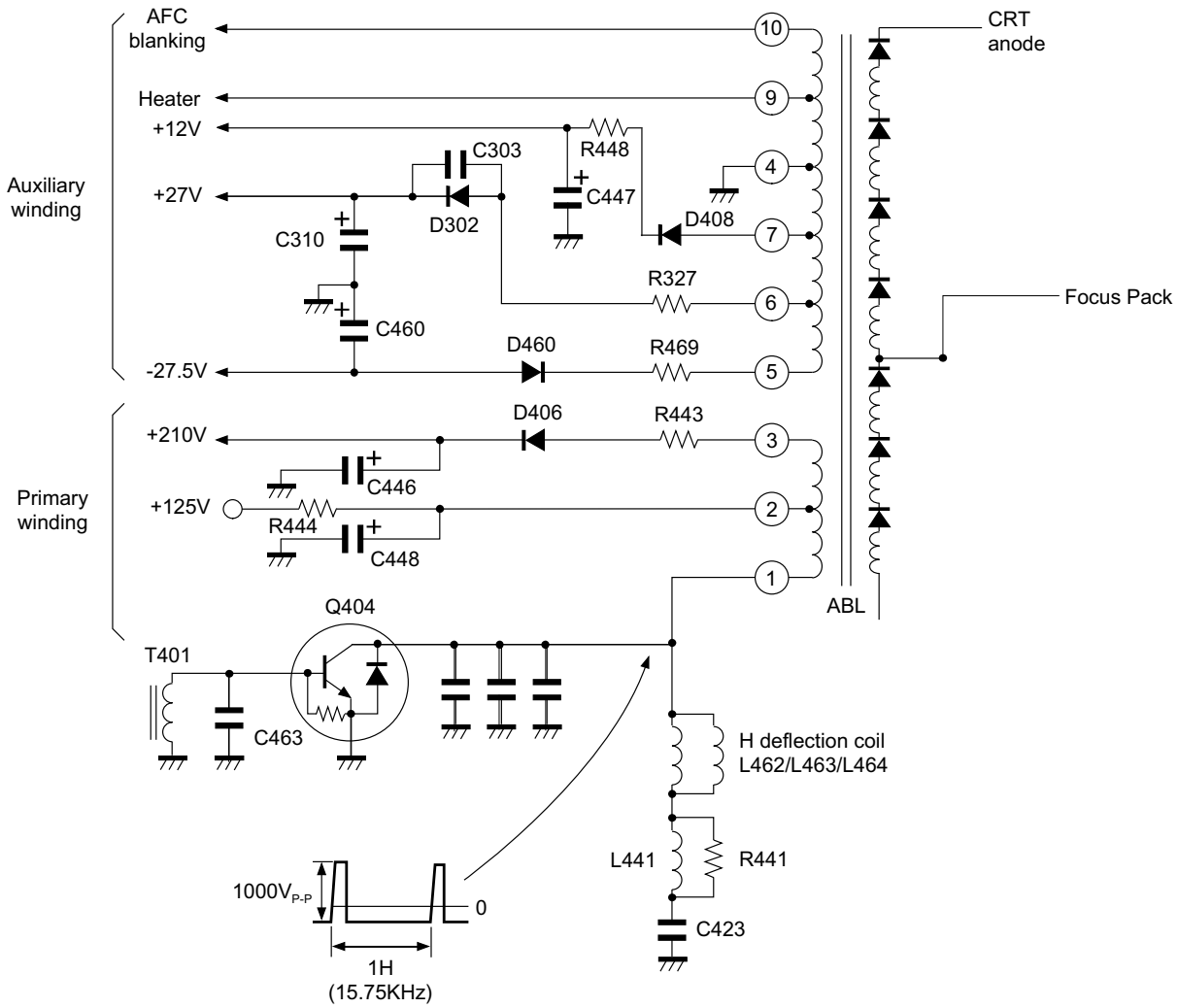


Fig. 12-17

5-1-1. +210V

For the flyback period, pulses are stacked up to DC +125V with FBT, and the voltage is rectified by D406 and filtered by C446.

5-1-2. +35V, 12V

Pin 4 of the FBT is grounded and the shaded area of negative pulse developed for opposite period of the flyback period is rectified, thus developing better regulation power supply.

5-1-3. -27V

As a power for the DPC circuit, a negative pulse signal is rectified by D460 and filtered with C460, thus developing the -27V.

5-1-4. High voltage

Singular rectification system which uses a harmonics non-resonant type FBT is employed and a better high voltage regulation is obtained, so amplitude variation of pictures becomes low.

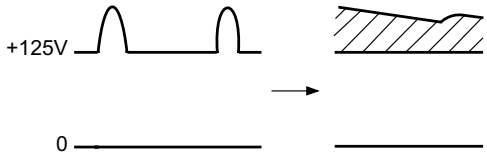


Fig. 12-18

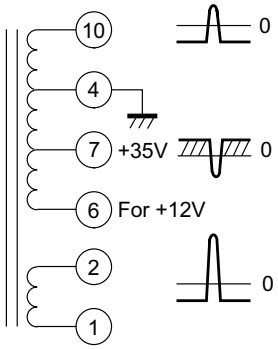
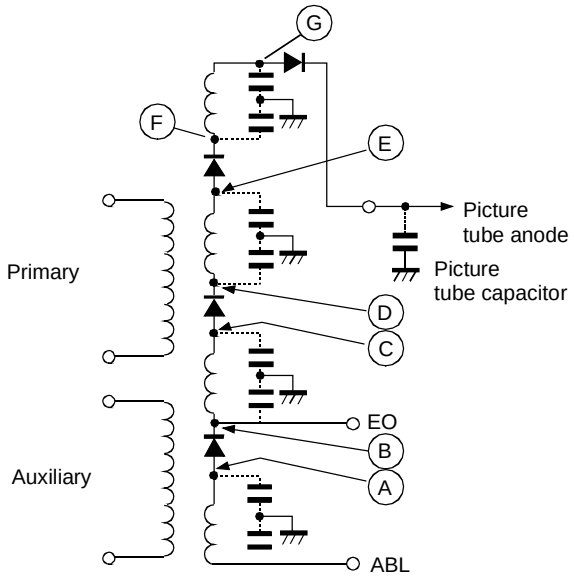


Fig. 12-19



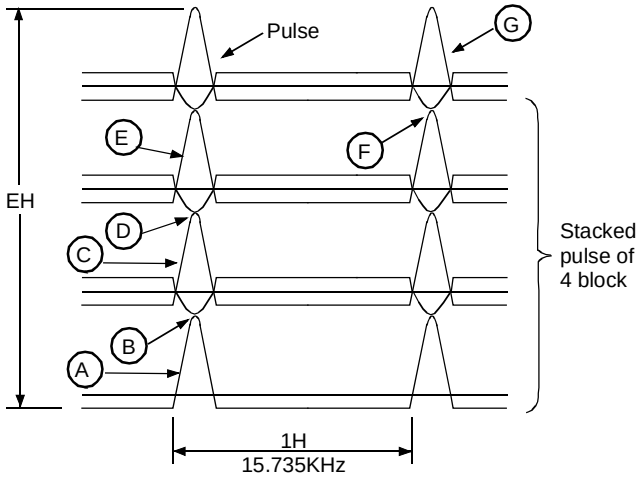


Fig. 12-20

5-2. Operation Theory of the Harmonic Non-Resonant System and Tuned Waveforms

The high voltage coil is of film multi-layer winding type and the coils are isolated into seven blocks. Each block is connected through a diode.

The basic operation is described in the case of 4 blocks construction for simplification. Positive or negative pulse determined by stray capacitance of each coil develops at terminal points (Ⓐ, Ⓑ, Ⓒ, Ⓓ, Ⓔ, Ⓕ, Ⓖ) of each coil as shown in Fig. 12-20, and these pulses are stacked as shown, thus developing the high voltage.

Moreover, a capacitance between the internal and external coatings of the picture tube works as a smoothing capacitor. Focus voltage is obtained at point EO.

The FBT is turned to a harmonic of 15 times the fundamental frequency, and the turned waveform is shown in Fig. 12-21.

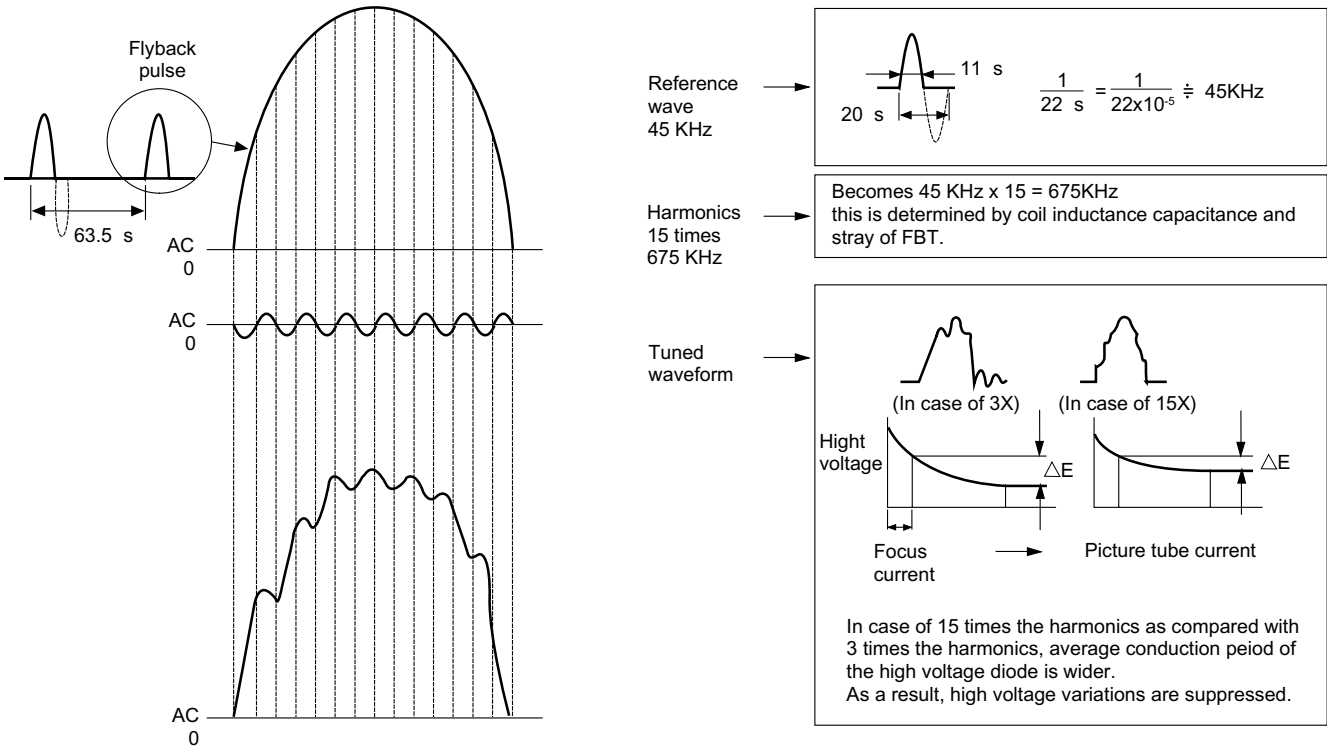


Fig. 12-21 Tuned waveforms

6. HIGH VOLTAGE CIRCUIT

6-1. High Voltage Regulator

6-1-1. Outline

Generally, four kinds of methods exist to stabilize a high voltage in high voltage output circuits using the FBT:

(1) Stabilization by varying the power supply voltage.
(2) Stabilization by varying L value with a saturable reactance connected in series with the primary winding of the FBT.
(3) Stabilization by varying equivalent capacitance of the resonant capacitor C0.
(4) Stabilization by superimposing a DC or pulse (this varies the high voltage) on a lower voltage side of the high voltage winding of the FBT.

In this unit, pulse transformer is eliminated and the regulator circuit using the method (3) is employed. The block diagram is shown in Fig. 12-22.

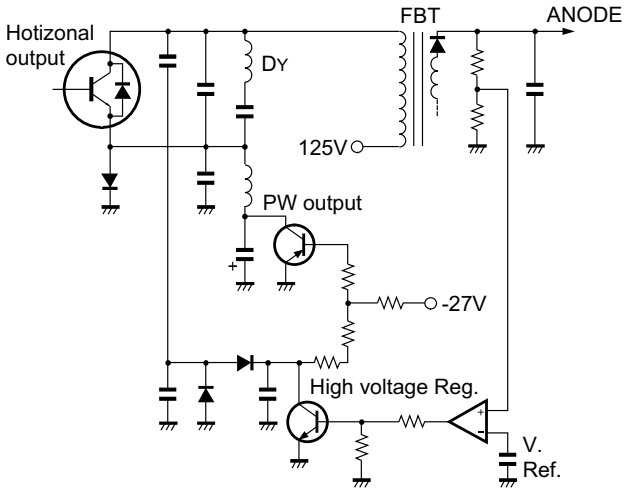


Fig. 12-22 Basic circuit for high voltage regulator emplyed in the unit

6-1-2. Theory of Operation

Fig 12-23 shows a basic circuit of the high voltage regulator used in the unit.

The high voltage regulator circuit splits a resonant capacitor C0 to C1 and C2. thereby dividing the collector voltage (V_{CP}) of the H output transistor with C1 and C2.

Here, assume each voltage developed across C1 and C2 as V_{CP1} and V_{CP1}, respectively,

$$V_{CP1} = \frac{C2}{C_1+C_2} V_{CP} \quad \text{①}$$

$$V_{CP2} = \frac{C2}{C_1+C_2} V_{CP} \quad \text{②}$$

$$V_{CP} = \frac{C2}{C_1+C_2} V_{CP2} \quad \text{③}$$

each relation can be expressed by the above equations ①~③.

The V_{CP2} developed across C2 is DC-clamped with a diode D1 and the resultant voltage is smoothed with a diode D2 and a capacitor C3. Thus processed voltage is obtained at the point Ⓑ. This voltage is used to provide a base current for the transistor Q1 or to flow the collector current. The voltage at the point Ⓑ decreases with the circuit impedance and finally lowers up to a V_{CE} saturation voltage of Q1.

Then, V_{CP2} is not clamped by D2 with the voltage at the point B. Since the V_{CP} is expressed as a sum of V_{CP1} and V_{CP2} as shown by equation ③, V_{CP} decreases by amount the V_{CP2} is decreased. This varies the high voltage.

Q1 collector current is controlled by Q1 base current which is an output of the comparison inverted amplifier. That is, the Q1 base current is controlled by a voltage obtained by comparing a detection voltage of the top breeder of the FBT (9.1V) and a DC voltage of 9V.

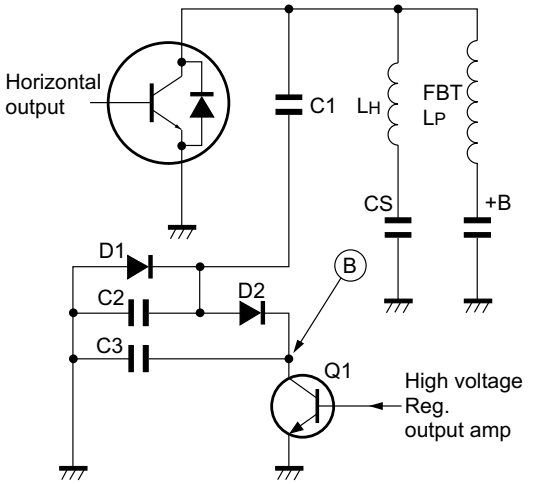


Fig. 12-23

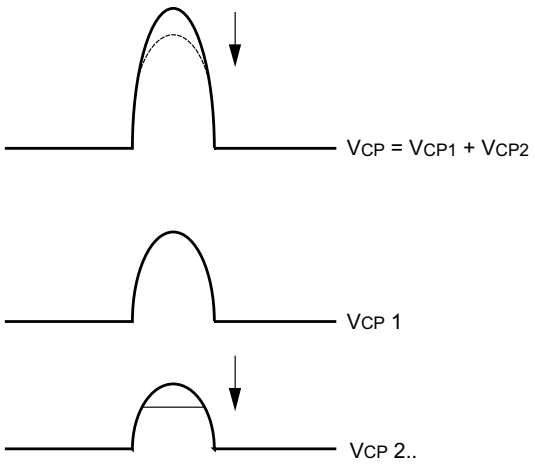


Fig. 12-24

6-1-3. Actual

Fig 12-25 shows the actual circuit used in the unit.

A resonant capacitor C0 is also split into two capacitors C443 and C444 in this circuit. The high voltage regulator cirucits is structured by splitting the C443 to two capacitors of C443 and C448.

Here, assume a high voltage increases and the detection voltage E_D' obtained by dividing the high voltage also increases in proportional to the high voltage. This makes the voltage E_D increase at pin 7. (The voltage is impedance transformed by a voltage follower circuit consisting of op amplifier Q483 at pin 7.)

The voltage E_D and a 9V reference voltage developed by a 3-terminal regulator Q420 are compared. When the E_D increases, the voltage at pin 2 of Q483 differential amplifier also increases, and the base current I_B of the high voltage transistor Q480 increases.

As a result, Q480 collector current increases and Q480 collector voltage (at the point Ⓑ) decreases. Then, a peak value of V_{CP2} across C418 is clamped by the diode D443 at the collector voltage lowered, and the collector voltage V_{CP} of Q404 (H output transistor) obtained as a sum of the voltage V_{CP1} across C443 and V_{CP2} across L418 decreases. Then, the high voltage also decreases.

When the high voltage lowers, the corrective operation is carried out in reverse order.

* Resustors R451, R452, R453 and R455 are used to correct undersirable influence (H amplitude increase at minimum I_H) by the H amplidude regulator.

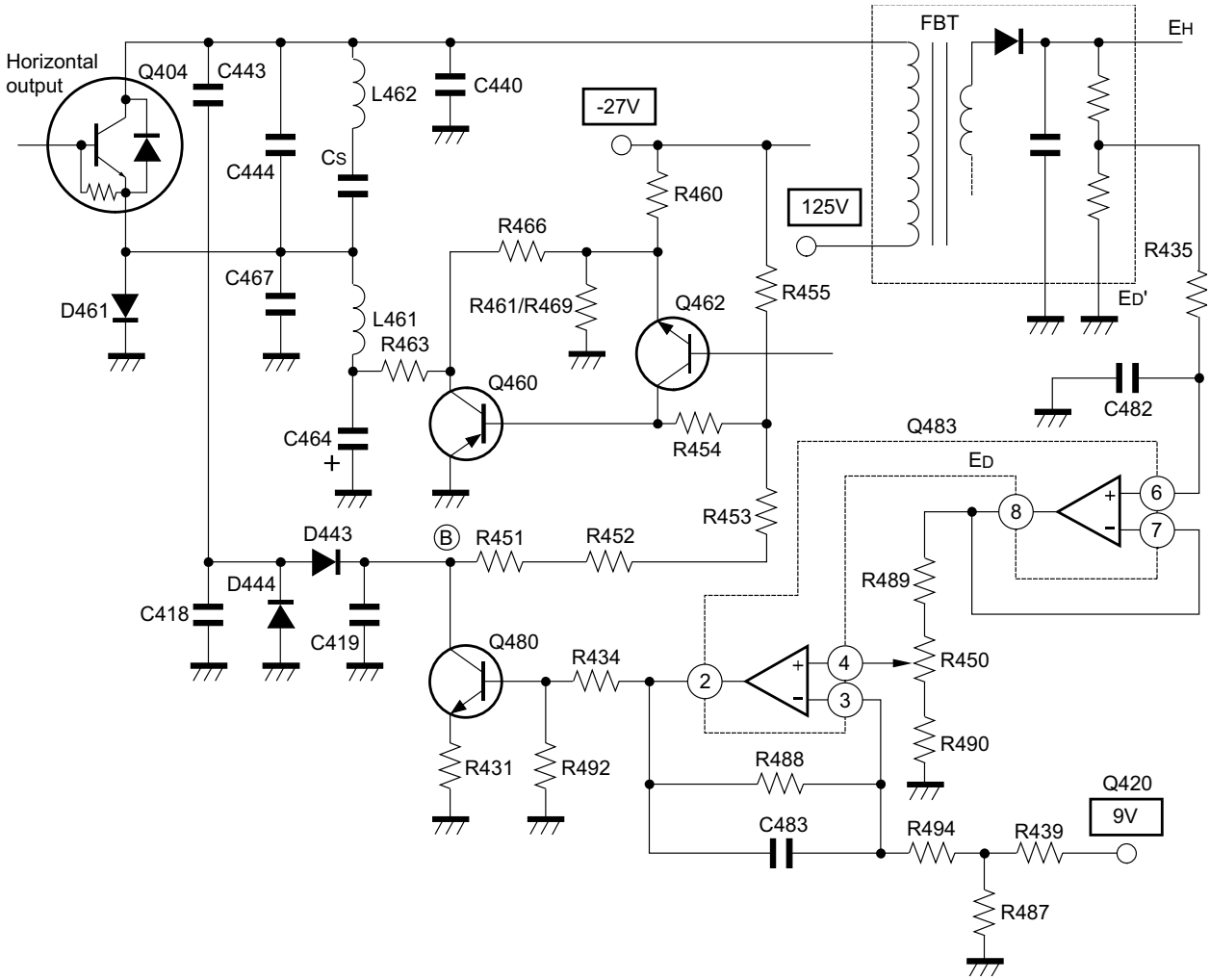


Fig. 12-25 Actual high voltage regulator circuit

7. X-RAY PROTECTION CIRCUIT

7-1. Outline

In case picture tube using high voltage, when high voltage rises abnormally due to components failure and circuit malfunction, there is possible danger that X-RAY leakage increases to affect human body. To prevent it, X-RAY protection circuit is equipped.

7-2. Operation

Figure 10-18 shows the circuit diagram. Supposing high voltage rises abnormally due to some reason, pulse at pin 9 of T461 also rises, and detection voltage Eb rectified by D471 and C471 in X-RAY protection circuit rises. When Eb rises, emitter voltage of Tr10 divided by R25 and R26 in protector module becomes higher than [zener voltage (6.2V) of ZD6 + Tr10 VBE]. This causes Tr10 turns on to supply base current to Tr9. Then Tr9 turns on. By this Tr6 and Tr6 turn on to make ON/OFF pulse at pin 7of QA01 in low level, QB30 and Q843 turns off, then relay SR81 turns off. Tr6 and Tr7 are in thyristor-connection, and 5V of power holds protection operation until main power switch is turned off. During circuit operation, power LED near main power switch blinks turn on and off in red.

Caution : To restart TV set, repair failure first.

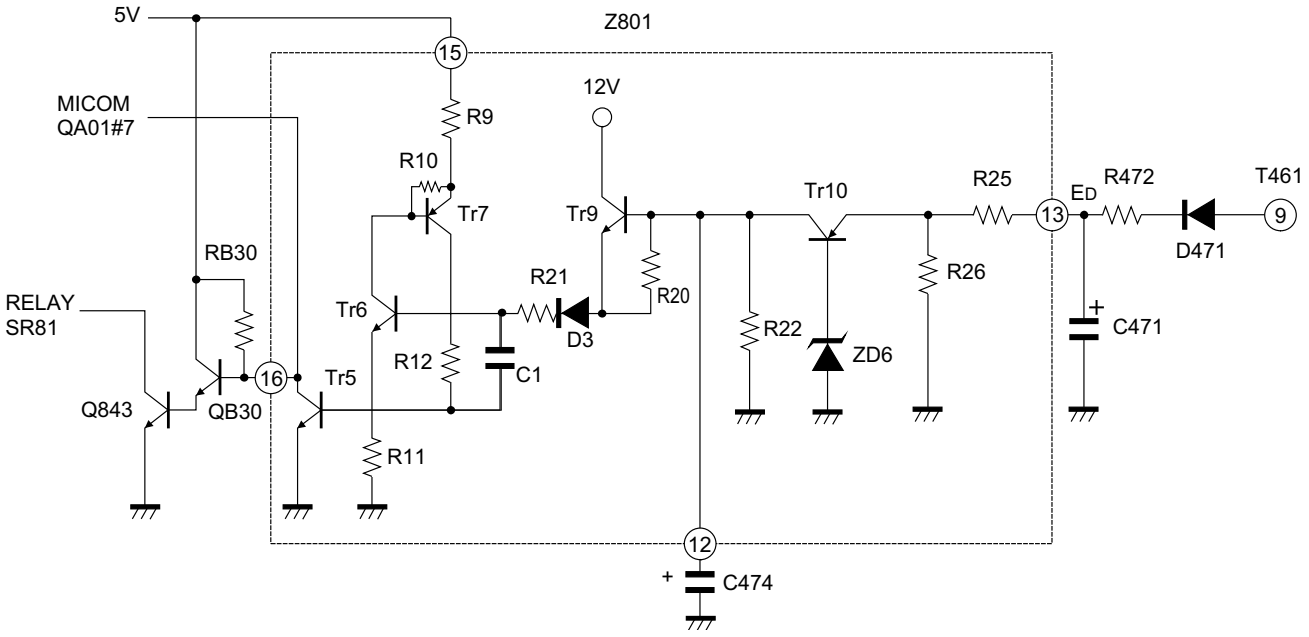


Fig. 12-26 X-RAY protection circuit

8. OVER CURRENT PROTECTION CIRCUIT

8-1. Outline

If main power (125V) current increases abnormally due to components failure, there is possible danger of the secondary damage like failure getting involved in other part failure, and abnormal heating. To prevent this, over current protection circuit is equipped, which detects current of main B line to turn off power relay in abnormal situation.

8-2. Operation

Fig. 12-27 shows over current protection circuit. When the current of main B line increases abnormally due to the shortage in load of main B line, voltage drop arises across R470. By this voltage drop, when base-emitter voltage of Tr 8 in protector module (Z801) becomes appprox. 0.7V or more, Tr 8 turns on, and the voltage by divided ratio of R15 and R16 is applied to cathode of ZD4. When this voltage becomes higher than zener voltage of ZD4, ZD4 turns on to supply base current to base of Tr 6 via R14. This causes Tr 5 ON and voltage at pin 16 of Z801 becomes Low. Therefore, QB30 and Q843 turns off to set SR81 OFF. Tr 6 and Tr 7 in Z801 are in thyristor- connection, and power 5V-1 supplied at pin 15 keeps protection operation for standby power until main power switch is turned off. During circuit operation, power LED near main power switch blinks in red.
Caution : To restart TV set, repair failure first.

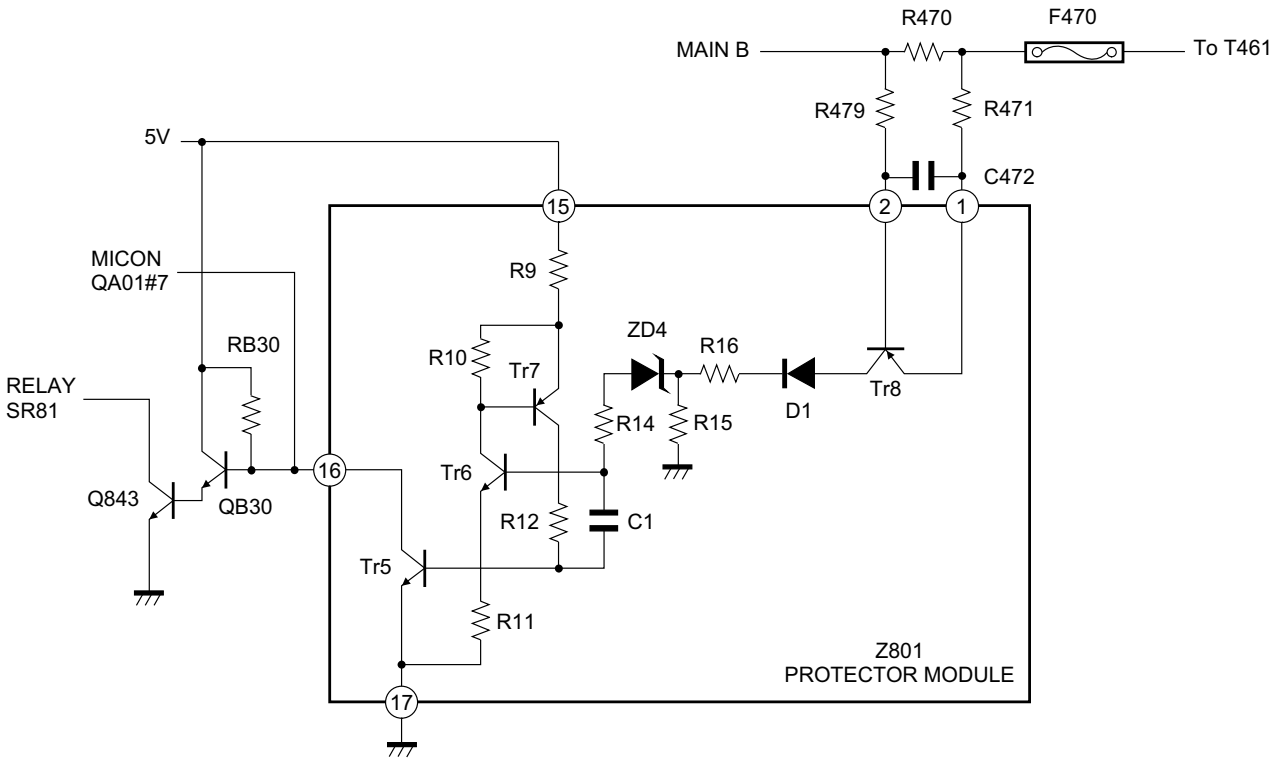


Fig. 12-27 Over current protection circuit

NOTES

SECTION XIII
DEFLECTION DISTORTION CORRECTION CIRCUIT
(DPC Circuit)

1. DEFLECTION DISTORTION CORRECTION IC (TA8859P)

1-1. Outline

The deflection distortion correction IC (TA8859AP), in combination with a V/C/D IC (TA1222N) which has a V pulse output, performs correction for various deflection distortions and V output under I²C bus control. All the I²C bus controls are carried out by a microcomputer and can be controlled with the remote control.

1-2. Functions and Features

The IC has functions of V RAMP voltage generation, V amplitude automatic switching (50/60 Hz), V linearity correction, V amplification, EHT correction, side pincushion correction, I²C bus interface, etc. and controls following items through the I2C bus lines.

(1) V amplitude
(2) V linearity
(3) V S-character correction
(4) V picture position (neutral voltage setting)
(5) V M-character correction
(6) V EHT correction
(7) H amplitude
(8) L and R pin-cushion distortion correction I (entire area)
(9) L and R pin-cushion distortion correction II (corner portions at top and bottom)
(10) H trapezoid distortion correction
(11) H EHT correction
(12) V AGC time constant switching

1-3. Block Diagram

Fig. 13-1 shows a block diagram of the basic circuit.

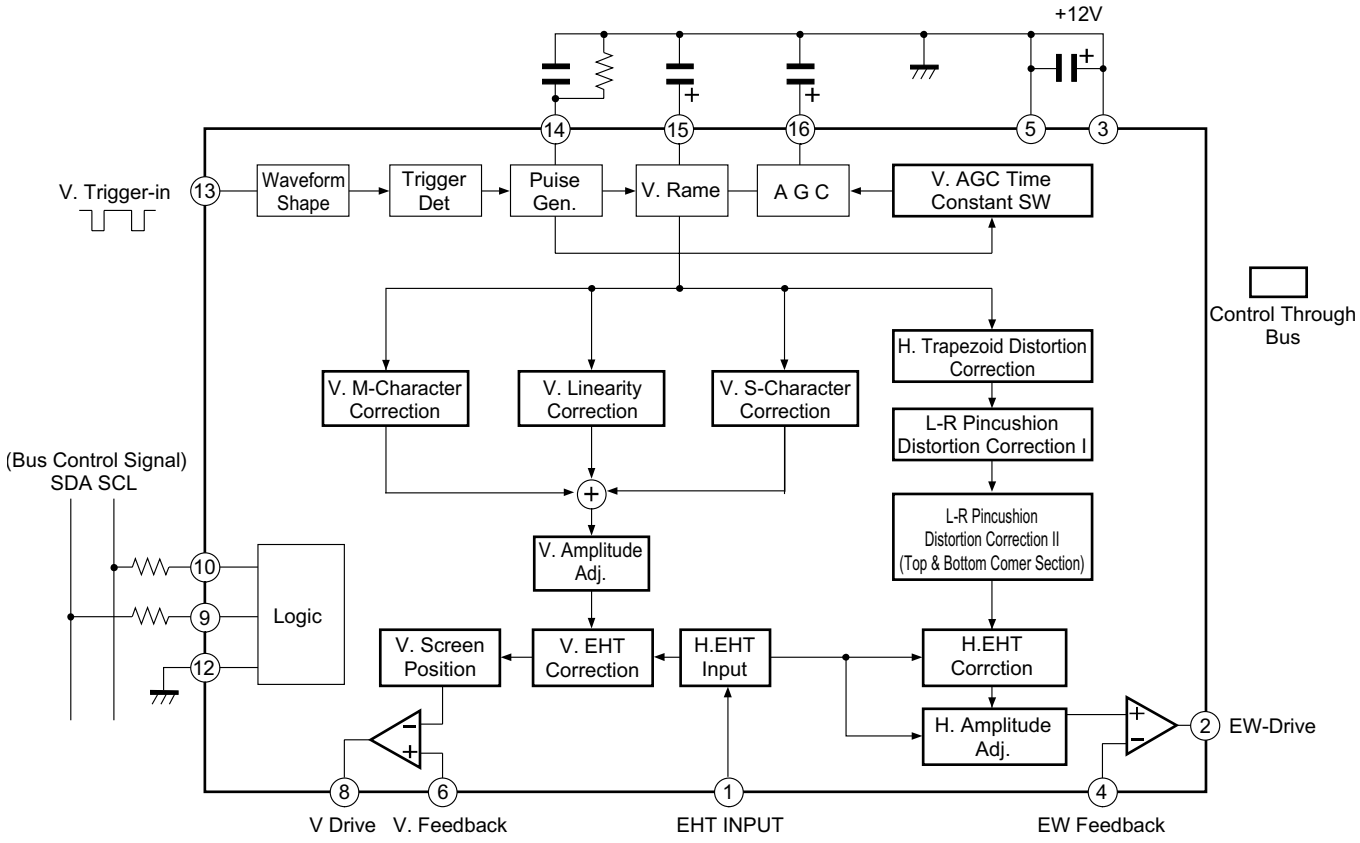


Fig. 13-1

2. DIODE MODULATOR CIRCUIT

Fig. 13-2 shows a basic circuit of the diode modulator used in the N5SS chassis.
A key point in the modulation circuit shown in Fig. 13-2 is the development of a negative pulse at point B.
In this circuit, a current loop of the resonant circuit for flyback period is shown by an arrow, and the energy stored in LDY is transferred to resonant capacitors Cr, Crm in passing through Cr, Crm, Cs when the scanning completes. As a result, a positive, horizontal pulse as shown in Fig. 13-3 Ⓐ will appear at Cr, and the current flows into Crm with the direction as shown. Then a pulse as shown in Fig. 13-3 Ⓑ develops at the point B.
On the other hand, since constant amplitude pulses across Cr, as shown in Fig. 13-3, are applied to the primary winding, the high voltage of the FBT is also constant.

When the negative pulse developed at point B is integrated with Lm and Csm, the average value appears at Csm as a negative voltage.

By modulating this voltage to have a parabolic curve with Q460, a waveform of Vm is obtained as shown in Fig. 13-4. As a result, the voltage Vs which is the sum of the power supply voltage VB and Vm, is applied across the S-curve capacitor Cs. Vs becomes a power source for the deflection yoke, and the modulated parabolic waveform, as shown in Fig. 13-3 Ⓑ, is applied to the horizontal deflection yoke and corrects the left-right pin-cushion distortion.

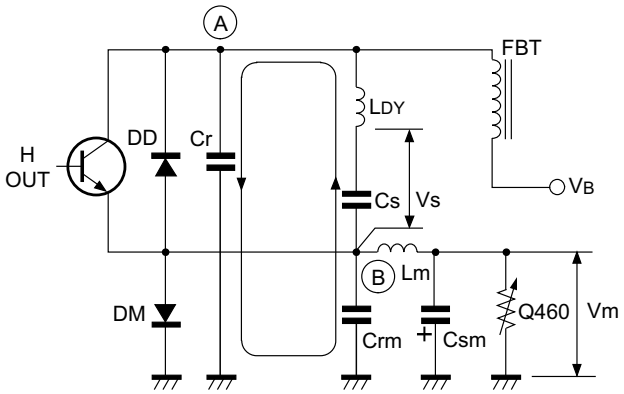


Fig. 13-2

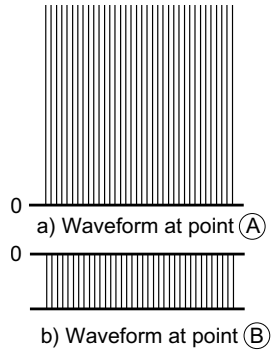


Fig. 13-3

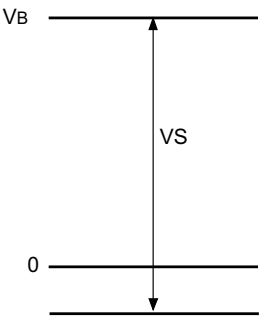


Fig. 13-4

3. ACTUAL CIRCUIT

In the actual circuit, the resonant capacitor is split into two as shown in Fig. 13-7. One, C440, is inserted between the collector of the H. OUT transistor and ground. The second one, C444, is inserted between the collector and emitter. In Fig. 13-5, C440 is expressed as C1 and C444 as C2, and the resonant current path for the flyback period is shown by arrows.

In a conventional circuit, when the brightness of a picture tube varies, high voltage current and high voltage also vary. As a result, horizontal amplitude is affected.

However, in this circuit, the horizontal amplitude variation can be suppressed to near zero if the high voltage current varies with variation of the high voltage.

When the scanning period completes, the energy stored in the deflection yoke LDY is transferred to the resonant capacitor in a form of current Iy. In this case, the current is split into two; Iy1 passing through C1, C3 and Iy2 passing through C2. In the same way, the energy stored in the primary winding of the FBT is transferred to the resonant capacitor in the form of Ip. In this case, the current (path) is also split into two; Ip1 passing through C1 and Ip2 passing through C2, C3. Concequently, the current differences between Iy1 and Ip2 (Iy1-Ip2) passes through C3.

When the high voltage current IH reduces with a dark picture, the current Ip in the primary circuit decreases, so Ip1 and Ip2 also decrease. However, a current flowing into (Iy1-Ip2) increases as Ip2 decreases. As a result, the pulse developing at the point B increases and the voltage Vm at Csm also increases as shown in Fig. 13-8. That is, when a dark picture appears, the voltage across S-curve capacitor Cs increases as shown in Fig. 13-8, the high voltage rises, and the horizontal amplitude is going to decrease. But, as Vs increases, the deflection yoke current increases and this works to increase the horizontal amplitude. Accordingly, if the brightness of a picture changes, the horizontal amplitude is maintained at a constant value.

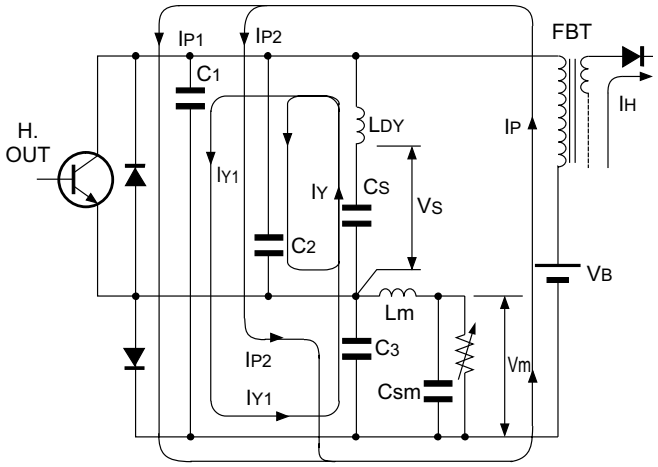


Fig. 13-5

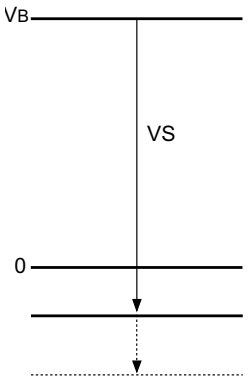


Fig. 13-6

3-1. Basic Operation and Current Path

3-1-1. Later Half Scanning Period

When the power is turned on, the power supply voltage VB is applied to Cs and Csm, and the Cs acts as a power source for a later half of the scanning period for which the H. OUT transistor is turned on, and the deflection current Iy flows in the path as shown below

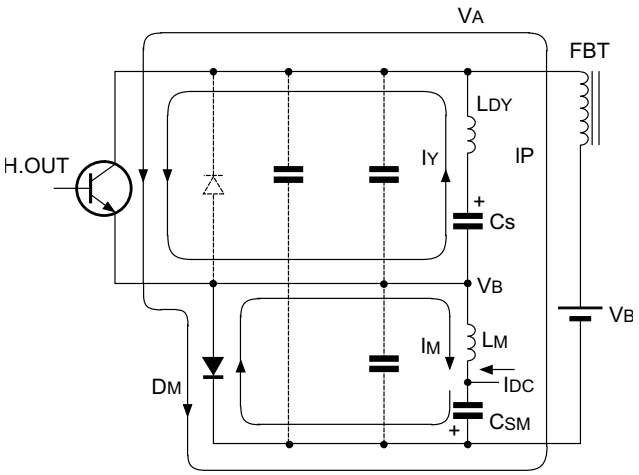


Fig. 13-7

Voltage & current waveform in H period.

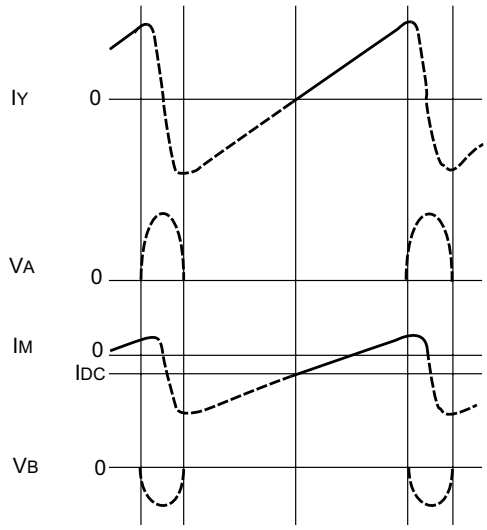


Fig. 13-8

3-1-2. First Half Scanning Period

When the base drive current decreases and the H. OUT transistor is turned off, each of the energies stored in LDY, Lm, Lp of FTB is transferred to C1, C2 and C3, respectively, and the resonant current becomes zero at a center of the flyback period. Then, VA and VB pulses show a maximum amplitude.

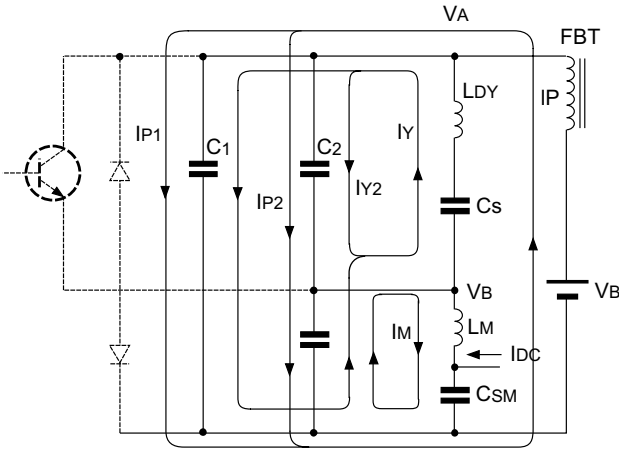


Fig. 13-9

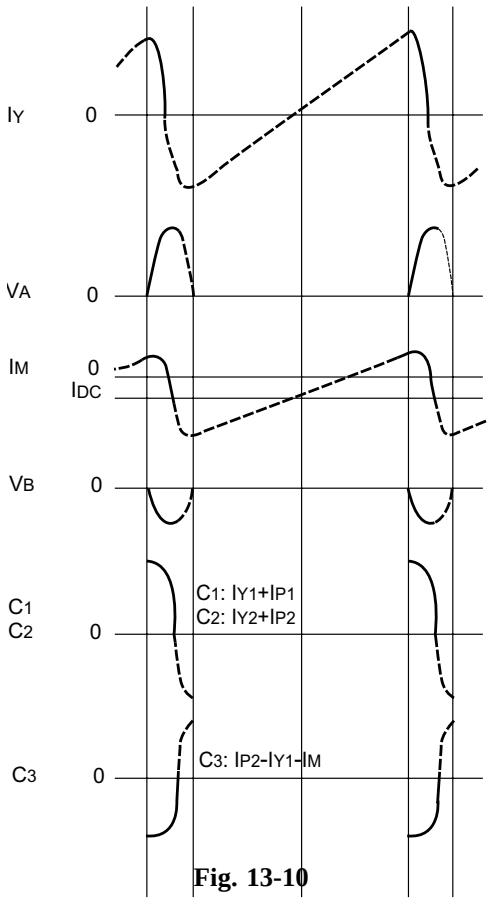


Fig. 13-10

3-1-3. Later Half of Flyback Period

All energy in the coil has been transferred to the resonant capacitors at the center of the flyback period, and the voltage shows the maximum value. However, during next half of the flyback period, the energy of the resonat capacitor is discharged as a reverse current through respective coil. When the discharge has been completed, VA and VB becomes zero, and the deflection current in reverse direction becomes the maximum.

3-1-4. First Half of Scanning Period

When the flyback period completes, the damper diode DD and the modulation diode DM turn on, and the Iy and Im proportionally decrease from the maximum value to zero. The H. OUT transistor is turned on just preceding at the center of the scanning period, and repeats the steps 3-1-1 through 3-1-4 stated above.

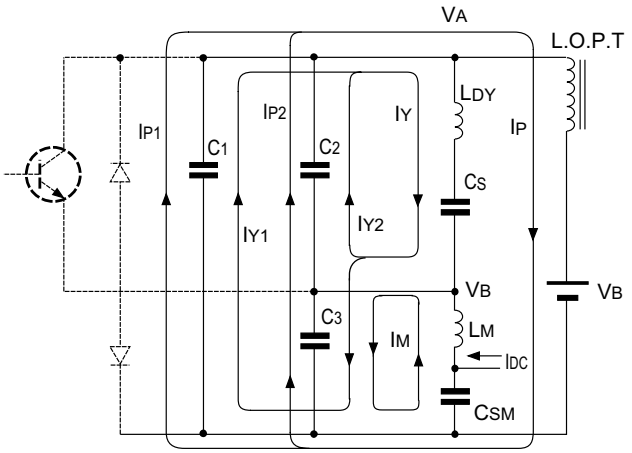


Fig. 13-11

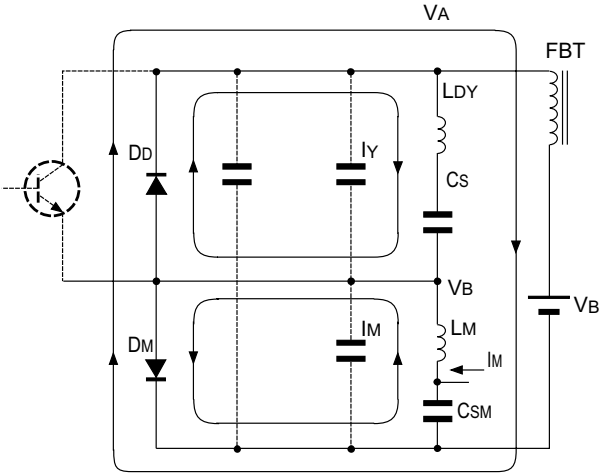


Fig. 13-13

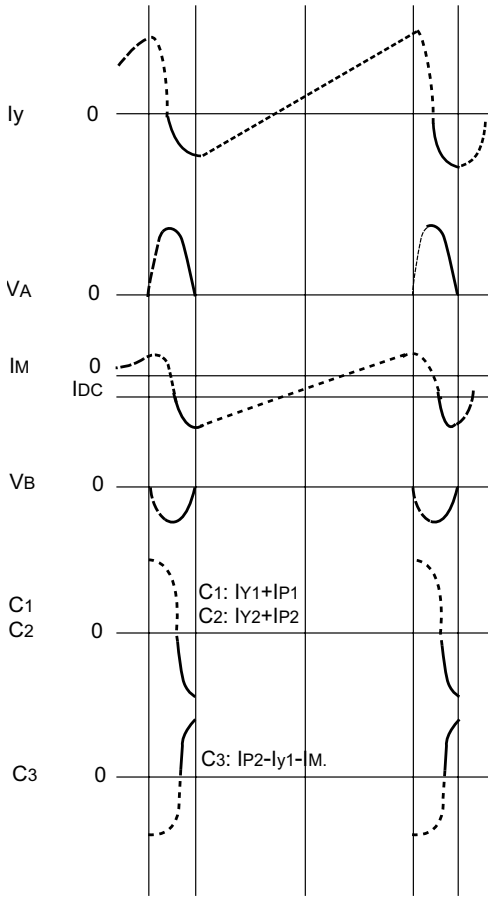


Fig. 13-12

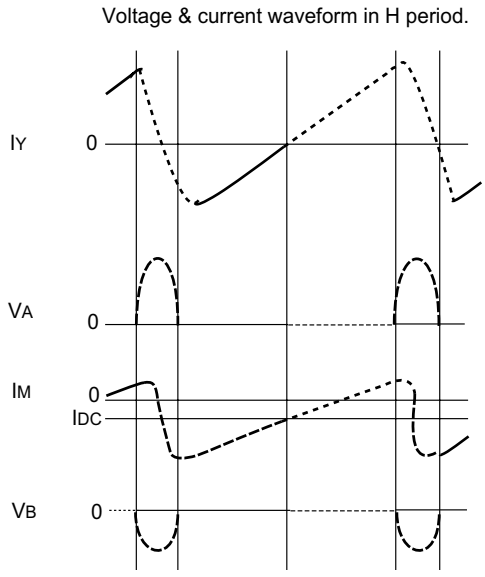


Fig. 13-14

SECTION XIV
CLOSED CAPTION/EDS CIRCUIT

1. OUTLINE

The CC (Closed Caption) and EDS (Extended Data Services) circuits extract data from from the incoming video signal and decode them to generate displayable text information. Major features of the CC/EDS circuit found in the TG1-C chassis are as follows:

(1) All decoding performed in 1 chip

(2) Capable of processing field 2 data (CAPTION 3, 4 TEXT 1, 2 EDS) as well as field 1 data (CAPTION 1, 2 TEXT 1, 2)
(3) Display of text mode extended from 8 rows to 15 rows.
(4) 64 extended characters to handle Spanish and the like.
(5) Background attribute capability (8 colors + transparent)

2. DATA TRANSMISSION FORMAT

The CC/EDS data is transmitted having been superimposed on line 21, field 1 (21H) and field 2 (284H). Waveform of line 21
is shown in Fig. 14-1. Line 21 signal is composed of data of 7 cycle clock-run-in, start bit and 16 bit (8bits x 2 bytes).

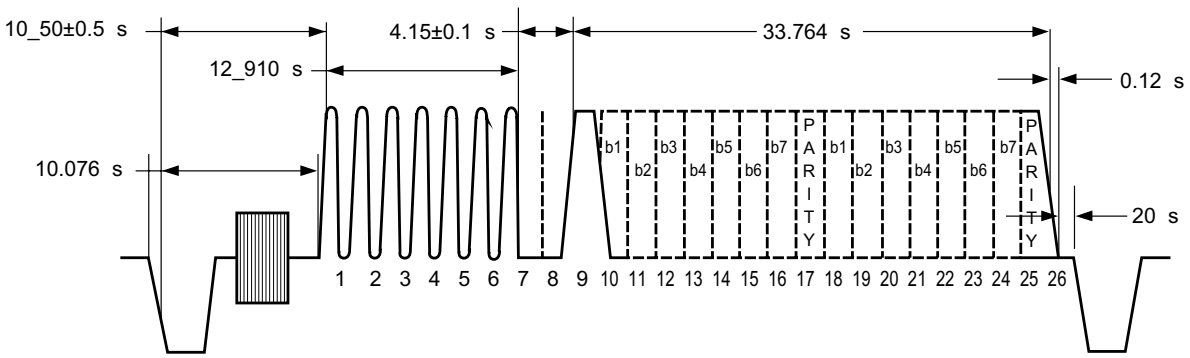


Fig. 14-1 Line 21 waveform

3. DISPLAY FORMAT

The character display area of caption mode and text mode consists of 32 characters x 15 rows as shown in Fig. 14-2. On the front and back of each row, 1 character blank area is respectively added. In caption mode, up to 15 rows can be displayed at the same time. Characters viewed while in text mode are displayed in a black rectangular box of 34 characters x 15 rows. EDS display format is shown in Fig. 14-3. CC or EDS can be displayed only when data of that type has been transmitted.

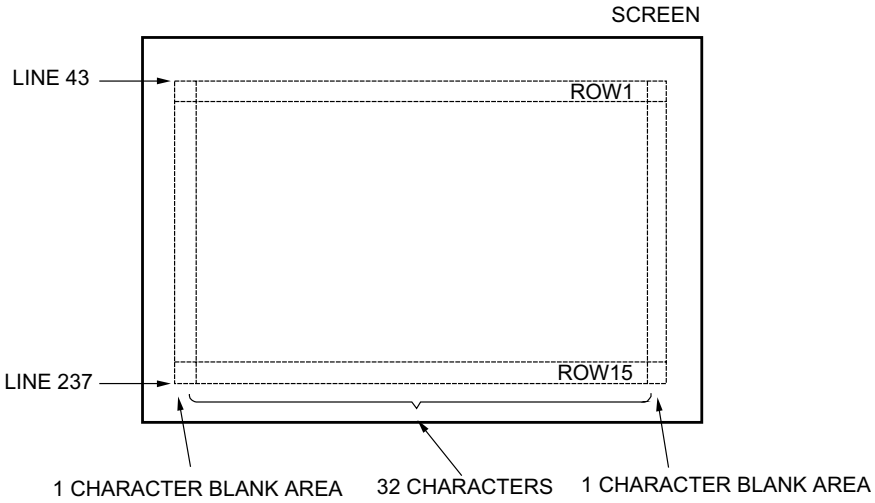


Fig. 14-2 Caption / Text display area

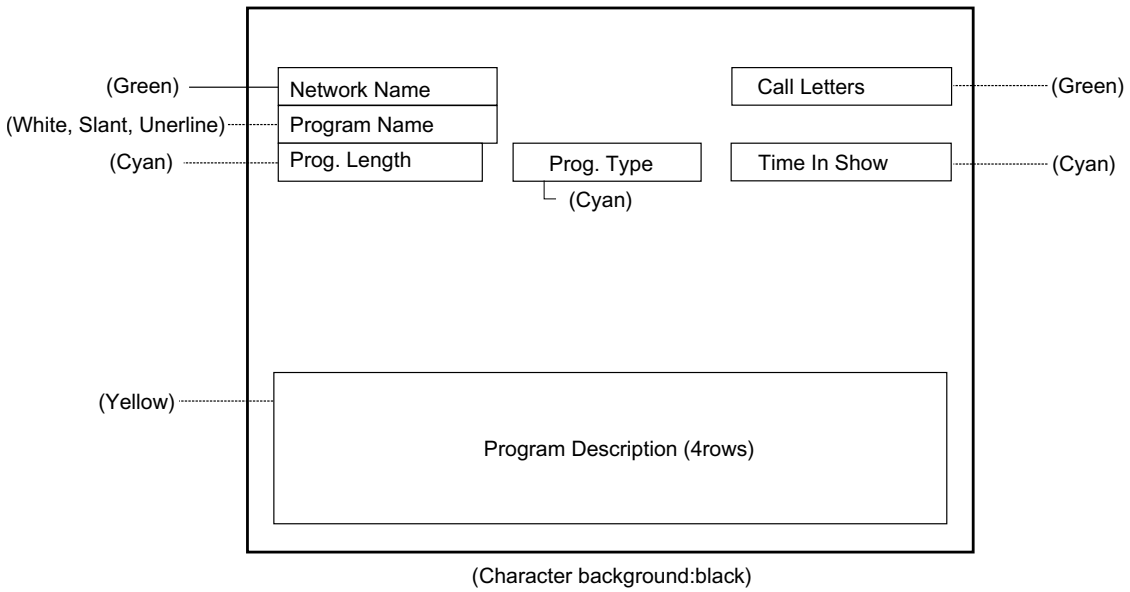


Fig. 14-3 EDS display format

4. CIRCUIT OPERATION

A block diagram of the CC / EDS circuit is shown in Fig. 14-4, and block diagram of QM01 is shown in Fig. 14-5.

The video signal which is input to pin 9 of UM01 is changed to 1 Vp-p signal which is band-limited to 600kHz by the input circuit, and it is supplied to pin 7 of QM01.

Inside QA01, line 21 signal information is extracted from the input video signal, and is recovered on clock and data. Recovered data is decoded by the command processor and converted to a display signal of R, G, B, Ys in Output Logic section.

The display signal is output at pins 18, 2, 3 and 17 in the CMOS level of positive polarity. The display output and OSD are switched by QR01 in UM01, and the selected signal is sent to the V/C/D IC.

When CC/EDS and OSD are displayed concurrently, OSD has the highest priority.

H. sync signal with negative CMOS level is input to pin 5 of QM01. This signal becomes the standard signal of a PLL circuit in the IC. The loop filter for the PLL circuit is connected to pin 9. QM01 is controlled by the I^2C bus connected to pins 14 and 15.

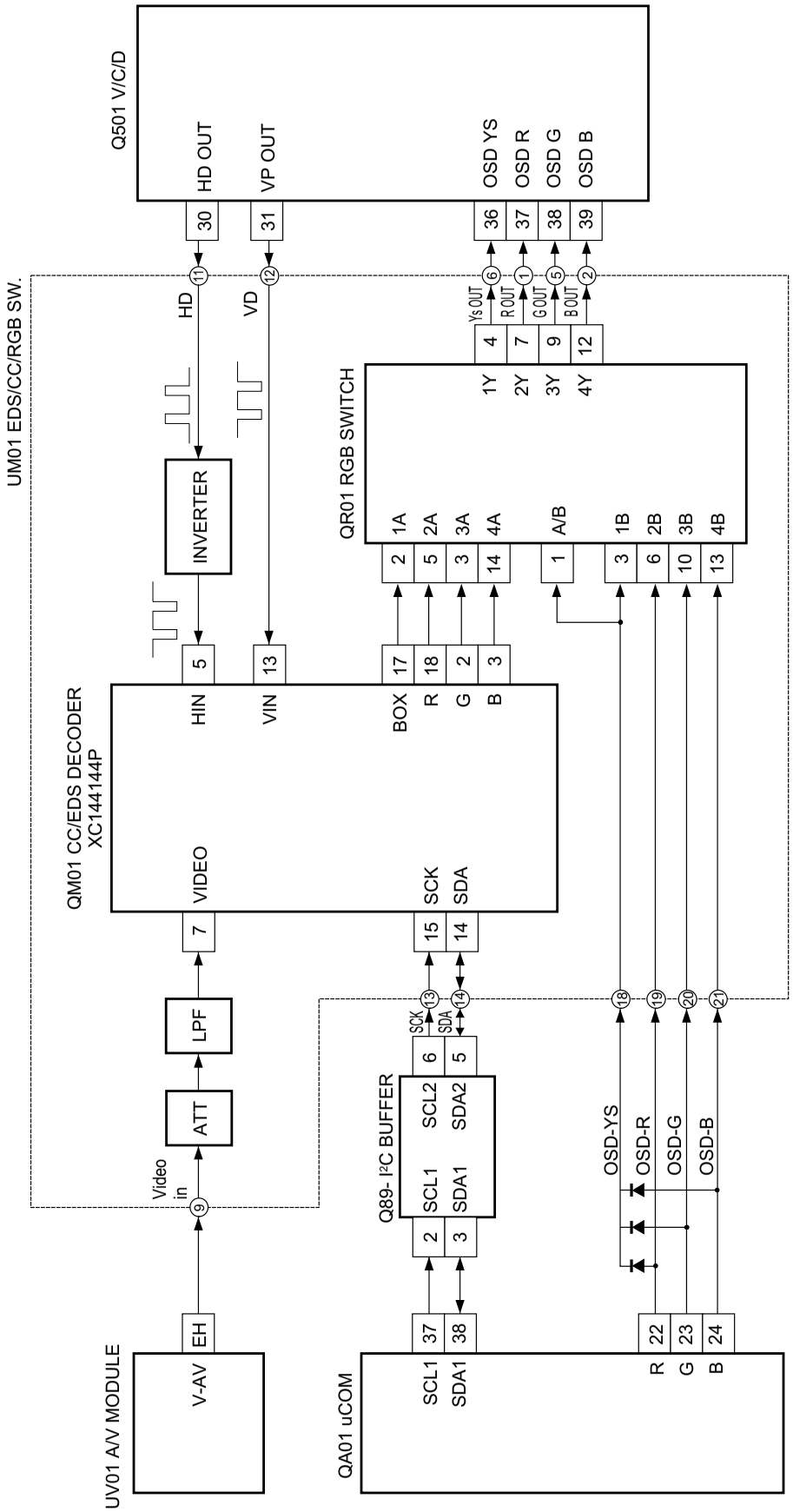


Fig. 14-4 CC /EDS circuit block diagram

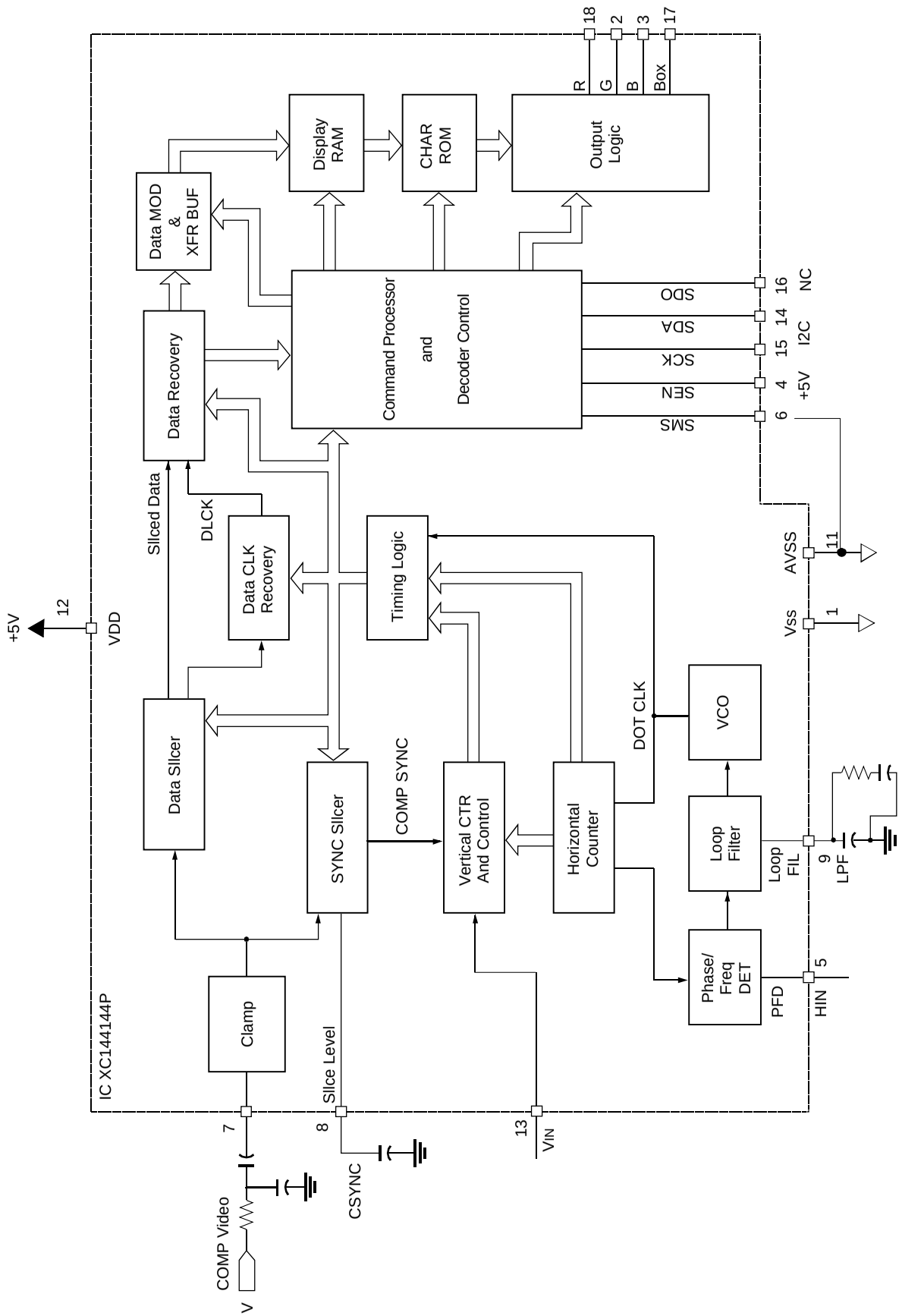


Fig. 14-5 XC144144P QM01 block diagram

SECTION XV
DIGITAL CONVERGENCE CIRCUIT

1. OUTLINE

The Digital Convergence circuit developes the correction signals to eliminate geometric distortions in the red, green, and blue CRTs. This new digital design is smaller than previous convergence circuits, more accurate, and adjusted via the remote control. Once adjusted, the data is saved in an E^2PROM and retrieved every time the set is powered up. Memory capacity for one full screen of data is 4k.

2. CIRCUIT DESCRIPTION

2-1 Configuration

Figure 15-1 shows the circuit block diagram for the digital convergence board. The digital convergence circuit consists of the convergence processor (Q701), the PLL circuit (Q707), the E^2PROM memory (Q713), D/A converters (Q703, Q704, & Q705), and pre amplifiers (Q715, Q717, & Q719).

Convergence waveforms from the D/A converters are amplified and shaped by Q715, Q717 and Q719, filtered, and output from unit. The PLL clock is adjusted by L719, to a basic frequency of 32MHz with no sync signal. Q701 generates a customer convergence test pattern and a service convergence test pattern, and outputs them as R, G, B and YS signals.

2-2 Circuit Operation

(1) When power is applied to the set, C711 resets the unit. Vertical (VD) and horizontal (HD) sync signals are applied to Q701 and Q707. These signals lock the PLL (Q707) to 32 MHz, which is counter down in Q701 to provided the clock.

(2) Q701 down loads the data in Q713 to RAM.

(3) Q701 processes the data, and sends it in serial form to the D/A converters (Q703, Q704, & Q705).

(4) Onced processed, the comvergence wave forms are amplified by Q715, Q717, and Q719.

(5) Next, the waveforms are filtered before they are output from the digital convergence board.

BLOCK DIAGRAM

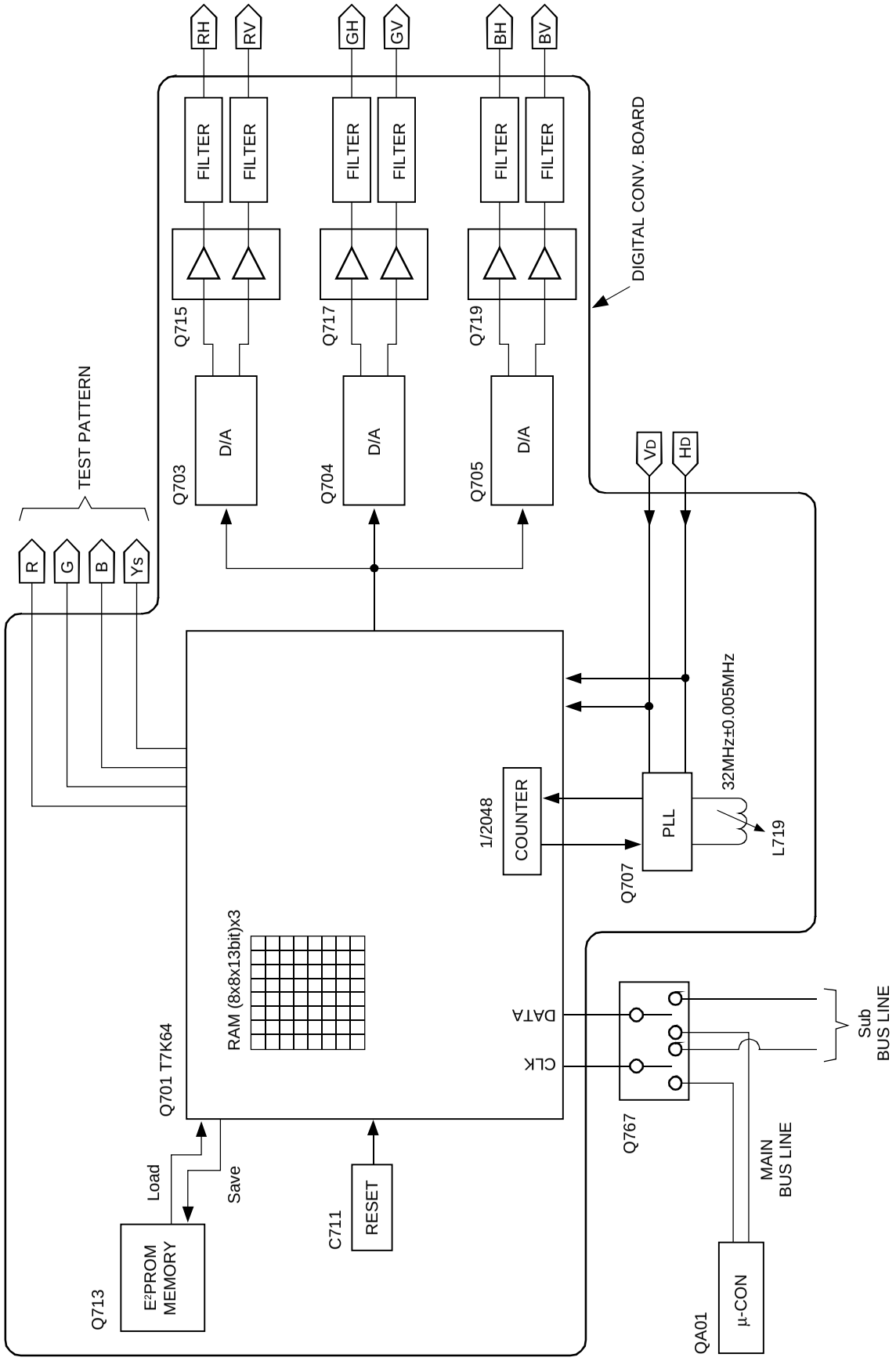


Fig. 15-1

3. PICTURE ADJUSTMENT

The adjustment is done on 60Hz mode (NTSC).

3-1 Change of Memory (E^2PROM)

Memory of Q713 E^2PROM is nonvolatile, and adjusted data is stored. Since data in RAM of Q701 is eliminated with power OFF, the RAM is set by soft command of microcomputer QA01 at every power ON. The adjusted data which is obtained from screen-watching is once stored in RAM inside QA01. The whole data in RAM which is corrected on each adjusting point and is changed, is saved into E2PROM (Q713) as a fixed data. The data capacity per one screen requires 4k for 60Hz mode (NTSC).

3-2 Service Mode

3-2-1 Outline

Service mode is controlled by software of microcomputer QA01, and is one of function of set.

This mode is designed so that ordinary user cannot use this, and special operation is required to use this.

Data change is done by direct shift (cursor display) of adjusting points ; 60Hz mode (NTSC) 8x8 /1 color.

3-2-2 To enter and to exit

Press MUTE key on remote hand unit twice and keep pressing the key, press MENU key of set console.

Then service data will be displayed on top left of screen. Under the condition, Press “7” key on remote hand unit, and the screen shows crosshatch picture (Later, the first picture). Press again “7” key, and the screen changes to crosshatch + data display (Later, second picture). This time changed data are automatically saved.

Further, press “7” key on remote, the screen returns to original picture.

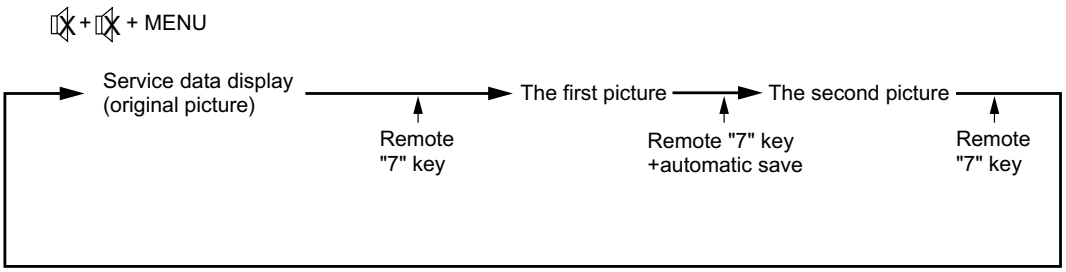


Fig. 15-2

3-2-3. Picture

60Hz mode (NTSC) ..... Correcting point Horizontal 8 x Vertical 8 (Arrow marks denote correcting point)

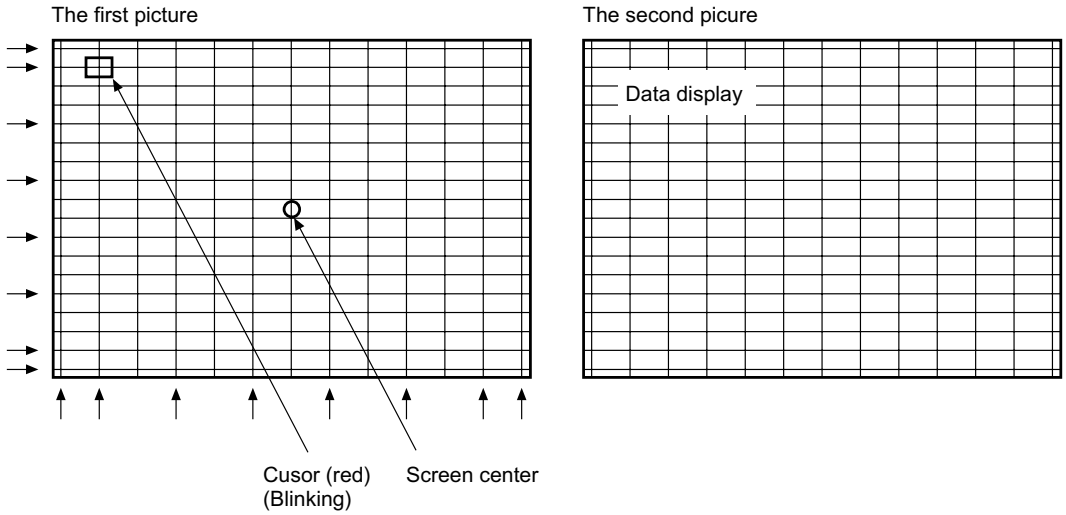


Fig. 15-3

The first picture
Crosshatch pattern. Pattern colors are three color display. Cursor is blinking in red. When changed, condition is last memory state.
Cursor is ..... Data change mode in lighting,
Cursor shifting mode in blinking.
Display color shows the color that data change is possible.

The second picture
When entering from the first picture to the second picture, correcting wave of convergence is muted for one second. During this period, the changed data is transferred from RAM Q701 to E2PROM Q713, and saved.
The second picture is indicated with data on top left of the first picture, therefore, convergence cannot be adjusted by this picture.

(CAUTION)
Receive suitable signal for adjustment. Decide the center by cross pattern of static convergence in menu, and adjust convergence from center to circumference.

4. ADJUSTING PICTURE DIMENSION (Green picture)

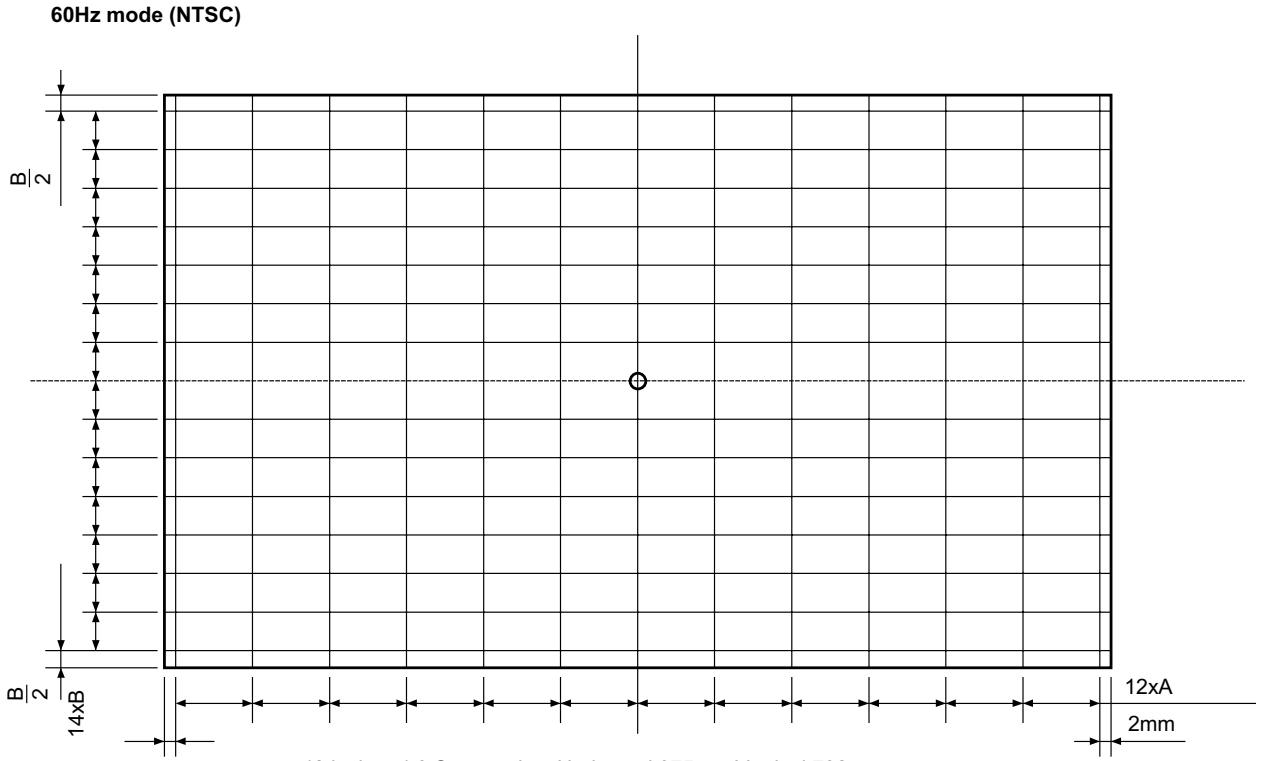


Fig. 15-4

5. KEY FUNCTION OF REMOTE CONTROL UNIT

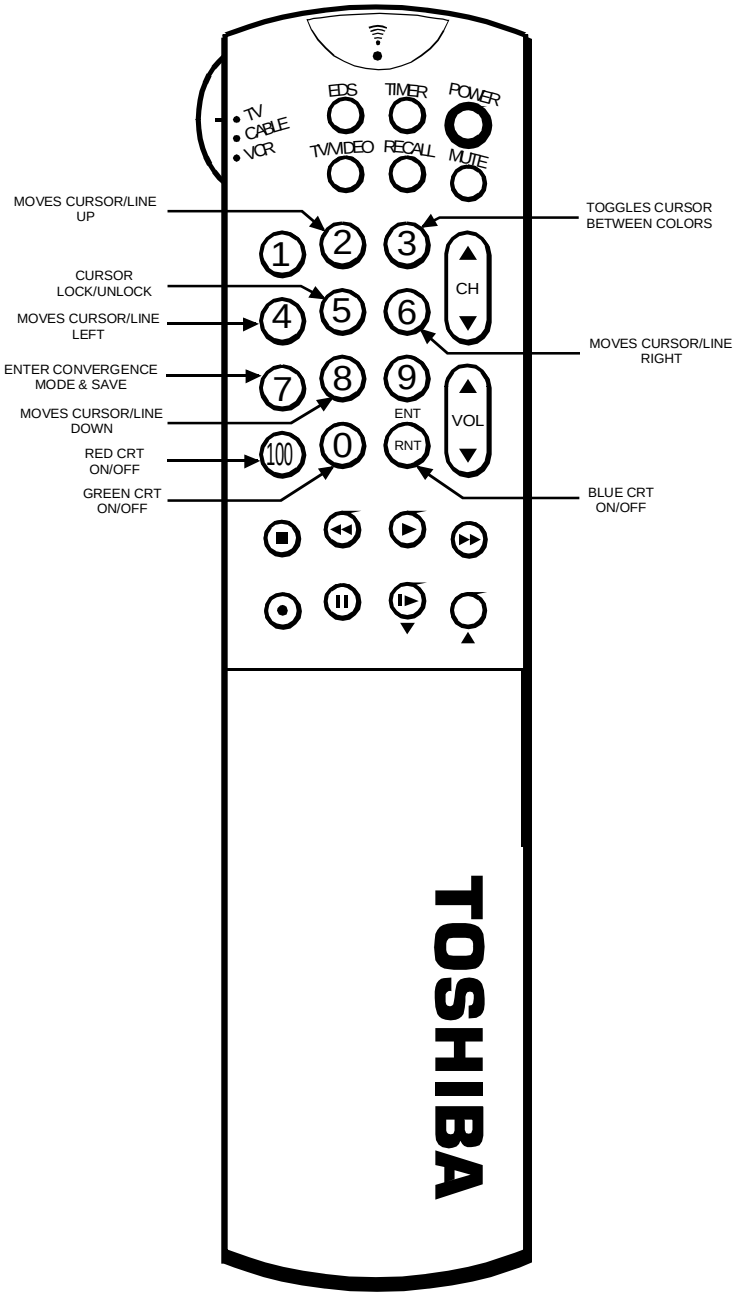


Fig. 15-5

6. CONVERGENCE OUTPUT CIRCUIT

6-1 Outline

This circuit current-amplifies digital convergence correction signal at output circuit, and drives by convergence yoke to perform picture adjustment.

Digital convergence output signal 6ch adjustment is done.

(H-R/G/B) (V-R/G/B)

6-2 Circuit Description

6-2-1. Signal flow

Signal which is corrected by digital convergence, is output to P708 (V, H R/G/B);

is input to Q751 (V) R/G/B, and is output to P713, P714 and P715;

is input to Q752 (H) R/G/B, and is output to P713, P714 and P715.

6-2-2. Over current protection circuit

All currents of Power supply, -15V, +15V and +30V are detected to protect CONV-OUT IC from damage due to output short of CONV-OUT.

Current value: Normal ± 15V approx. 700mA

+30V approx. 200mA

Detecting curren ±15V approx. 1.8A or more

+30V approx. 700mA or more protecting operation

6-2-3. Pump-up source

CONV-OUT IC Q752 (H)

Pin 10 (+15V/H,PV)

Pin 5 (+30V)

By HD input signal, pump-up is done only in horizontal retracing time.

6-2-4. CONV-OUT mute

In power-on operation, transistors Q765 and Q766 are made turned ON, and -15V is applied to pin 3 of CONV- OUT IC. These cause mute operation on CONV-OUT.

6-2-5. Operation of IC

1) Q764 (TC74HC4050AP)

Sync signal which is input from P711 1 VD, 2 HD, is, through buffer, supplied to digital convergence P708.

2) 3-terminal source

Q754 (+5V) Q755(+9V) Q756(-9V)

Source for digital convergence

3) Q767 (TC4066BP)

P711 4 SDAM, 5 SCLM : microcomputer. Busline, through Q767, is input to Digital Convergence P709, and is controlled.

4) To adjust from outside of digital convergence :

Put adjusting jig into 6P socket of P720. Iscs turns from H to L, switch of Q767 is changed over. Then busline from microcomputer is cut off.

P720 3 SCLU, 4 SDAU

Controlled by external adjusting jig.

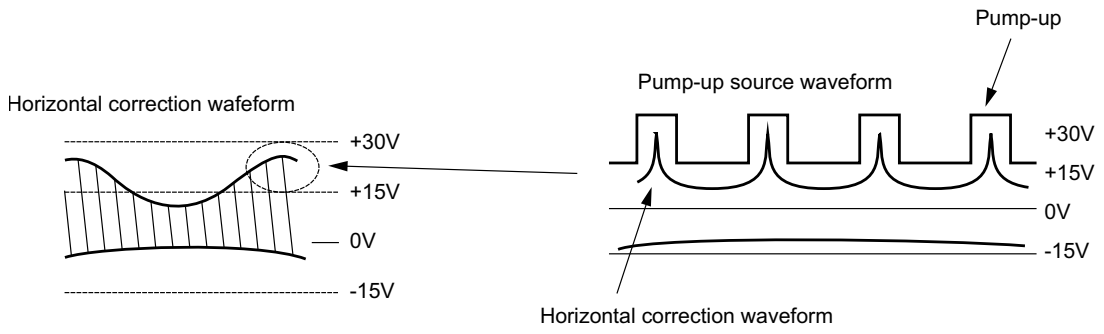
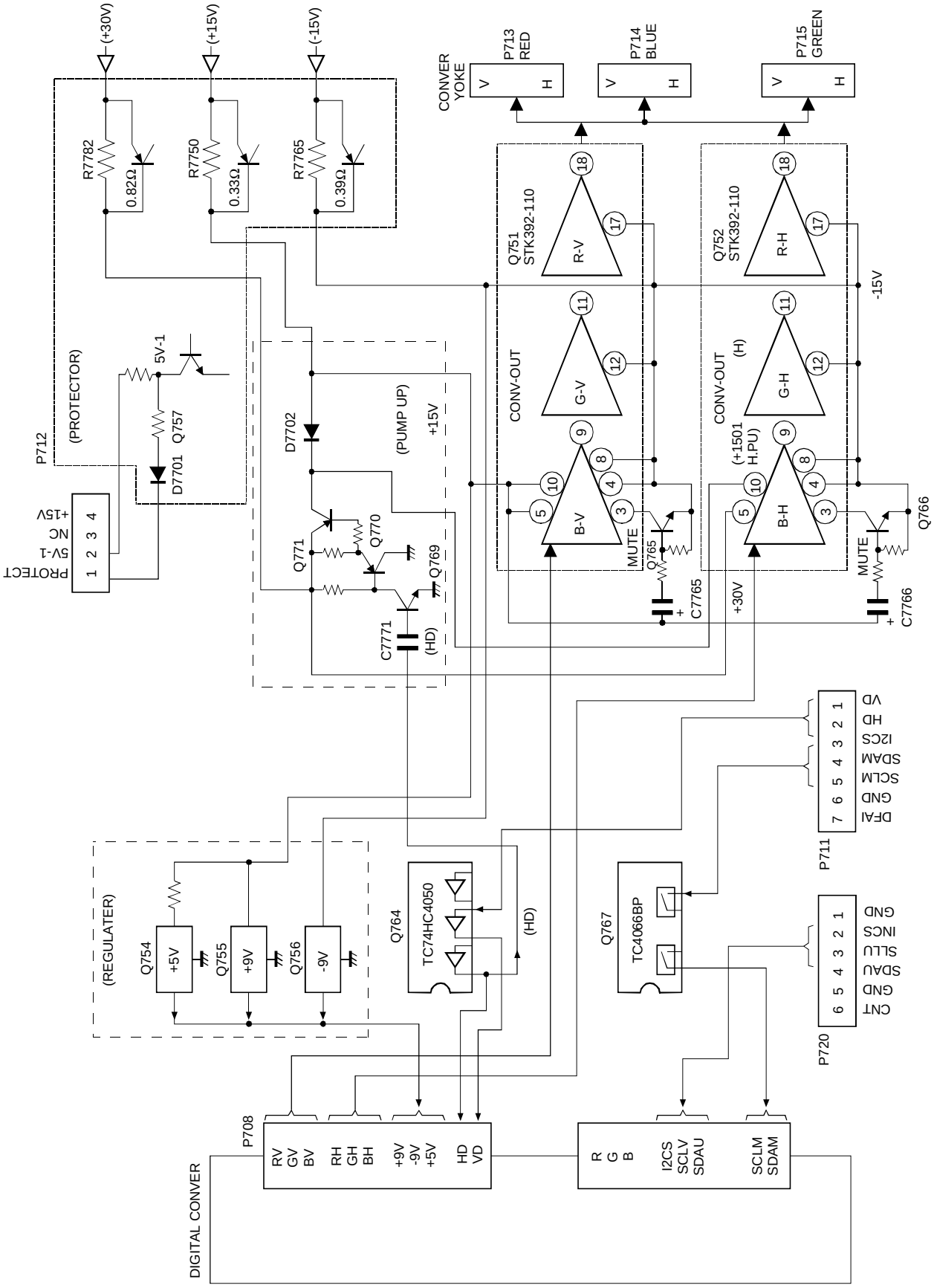
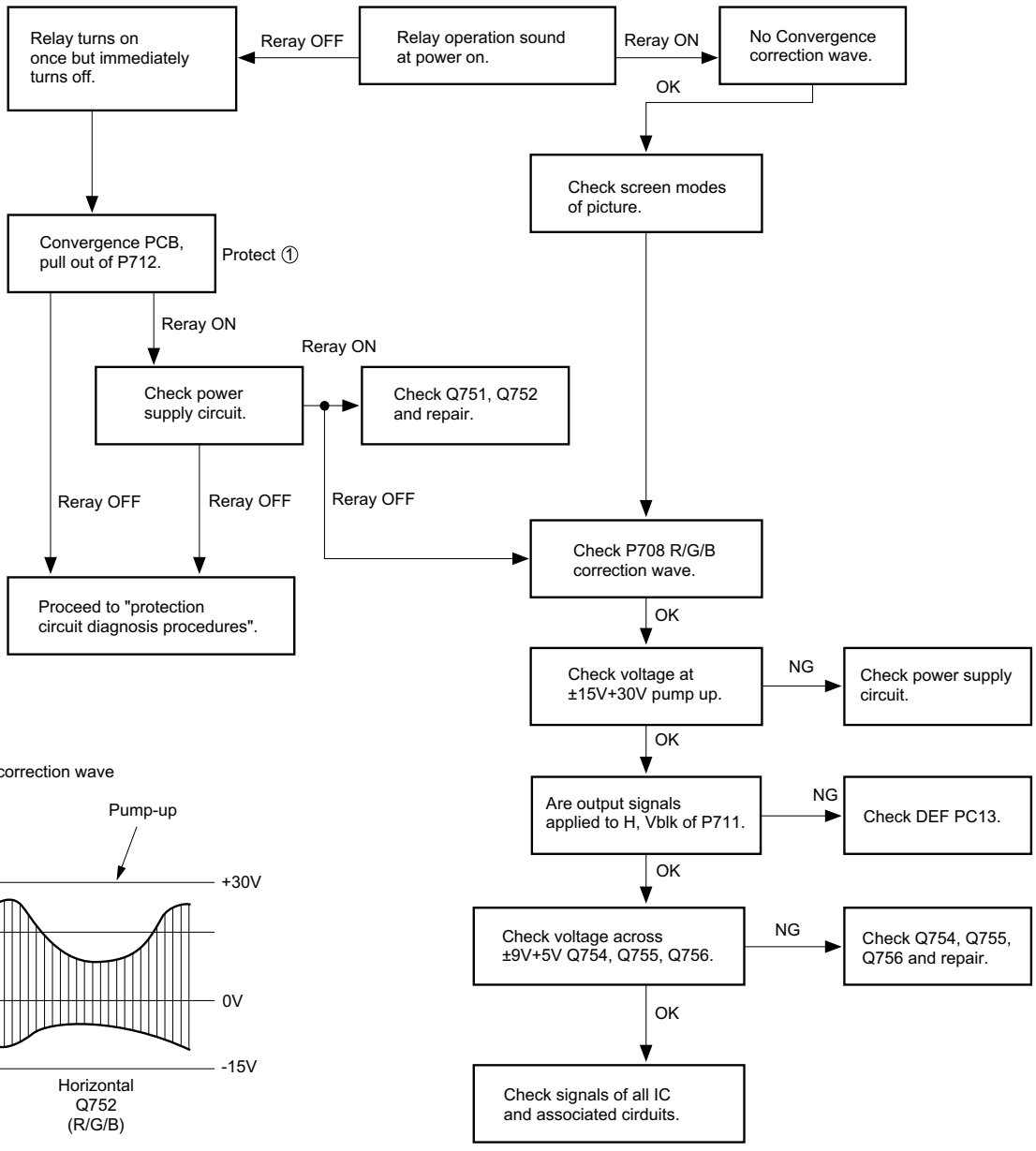


Fig. 15-6

CONVERGENCE (BLOCK DIAGRAM)



7. CONVERGENCE TROUBLESHOOTING CHART



Convergence output signals correction wave

LAB 3

DIGITAL CONVERGENCE

GREEN GEOMETRY

1. Put the set in the service mode and bring up the convergence cross hatch.
2. Push the 100 button to turn off the red tube, and RTN to turn off the blue tube.
3. Place the convergence template on the screen and align the center cross hairs with the tabs in the bezel.
4. Use low tack masking tape to attach the template to the bezel. Try to get the template flat against the screen to reduce parallax errors.
5. Push the 3 button on the remote until the blinking cursor in the upper left corner of the screen turns green.
6. Move the blinking cursor to the right with the 6 button, then down with the 8 button until it's one line to the right of center. The 4 button moves the cursor to the left, and the 2 button moves it up.
7. Push the 5 button to lock the cursor in place.
8. Use the 2, 6, 8, and 4 buttons to align the intersection of the cross hairs with those on the template.
9. Push the 5 button to unlock the cursor.
10. Move the cursor to another location and repeat steps 7 and 8. Moving the cursor in a counter clockwise spiral to the various locations works best. Normally, you need to repeat the procedure a second time to make fine adjustments.

RED CONVERGENCE

1. Remove the template and press the 100 button to turn on the red tube.
2. Press the 3 button until the red cursor appears.
3. Align the red cross hatch pattern to the green cross hatch pattern the same way you aligned the green with the cross hatch pattern on the template.

BLUE CONVERGENCE

1. Push the 100 button to turn off the red tube, and RTN to turn on the blue tube.
2. Push the 3 button until the blue cursor appears.
3. Align the blue cross hatch pattern to the green cross hatch pattern in the same manner.
4. Push the 100 button to turn on the red tube and check the convergence with all three tubes on. The cross hatch pattern should be white with no red, green, or blue present. However, depending on how much the blue tube is defocused, a slight blue halo may show.

5.Push the 7 button then the power button to save the settings and exit the service mode.

ELECTRICAL CENTERING

1. Disconnect all video cables in the video 1 input.

2. Put the set in the service mode.

3. Push the TV/VIDEO button on the remote until the white cross hair pattern on a black background is displayed.

4. Check the centering of the cross hair pattern with the centering tabs in the bezel.

5. If the horizontal position is off, push the channel up button until the HPOS register appears. Use the volume button to center the pattern.

6. If the vertical position is off, push the channel up button until the VPOS register appears. Use the volume button to center the pattern.

7. Push the TV/VIDEO button until the TV picture is displayed, then turn the power off.

8. Turn the set on and check the picture quality with a live video signal.

END OF LAB 3

SECTION XVI
OPTICAL SECTION

1. NECK COMPONENTS

NOTES:

1-1. Outline of Components Around Neck of The Projection Tube

Fig. 16-1 shows names and mounting locations of neck components around the projection tube.

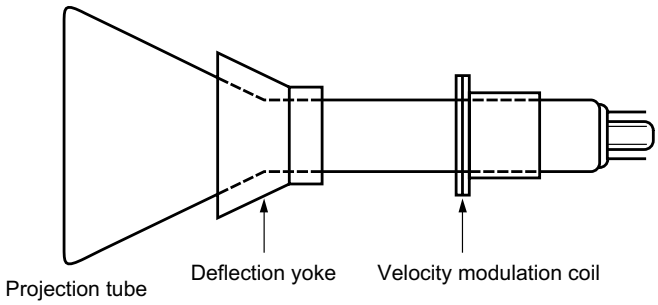


Fig. 16-1

1-2. Theory of Operation

The neck components consist of, a deflection yoke assembly ① (which consists of a main yoke, a sub-yoke, and a centering magnet), and a velocity modulation coil ②.

The main yoke of the deflection yoke assembly consists of a horizontal and vertical deflection coil, and deflects electron beams in horizontal and vertical directions.

The sub-yoke is called a convergence yoke and also consists of a horizontal and vertical coils. The sub-yoke performs distortion correction and color registration according to correction currents supplied from the convergence output circuits.

Moreover, a centering magnet consisting of two 2-pole magnets is provided at end of the deflection yoke to adjust the raster position.

1-3. Projection Tube

TP4688J, TP4880A

• Fluorescent screen: flat

TP48E60/61 TW56D90

• Fluorescent screen: inverted R 350mm

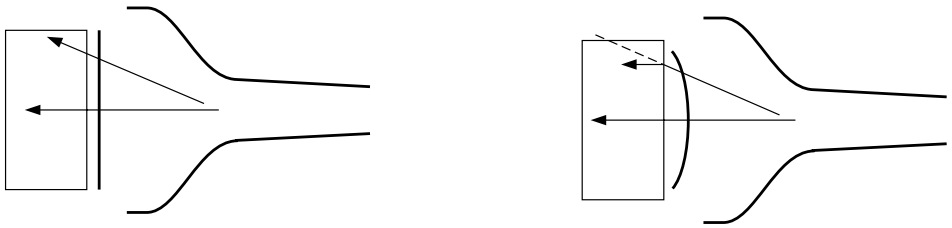


Fig 16-2

Electrons around the peripheral of the CRT screen come into collision with the A/B lenses and are not used, thus lowering contrast, etc.

Light beams around the peripheral of the CRT screen are focused towards the center, thus increasing the amount of light emitted towards the screens.

• Electromagnetic Focus

Electromagnetic focusing with magnets mounted around the CRT neck.

• Electrostatic Focus

High unipotential focus

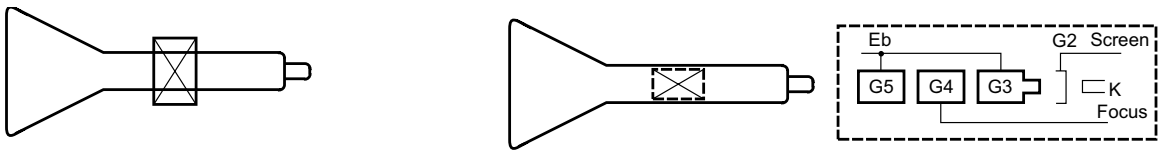


Fig 16-3

Since the deflection is carried out by using a magnetic field applied from the outside of the neck, high deflection power is obtained and focusing quality is high. Moreover, since the coils are mounted on the outside of the neck, the configuration of the deflection fields created inside the neck has less distortion, thus the best beam pattern will be obtained.

The best beam pattern is obtained at screen center and screen edges by applying parabolic voltages for H and V periods to the focus terminals.

This also assures a flat focusing characteristic across the entire screen.

To obtain clearer pictures, a velocity modulation circuit is also provided.

2. FUNCTION OF KEY COMPONENTS

2-1. Outline

The optical system of the TP48C60/61 consists of a screen, mirror and lens assembly. A description will be given for each block.

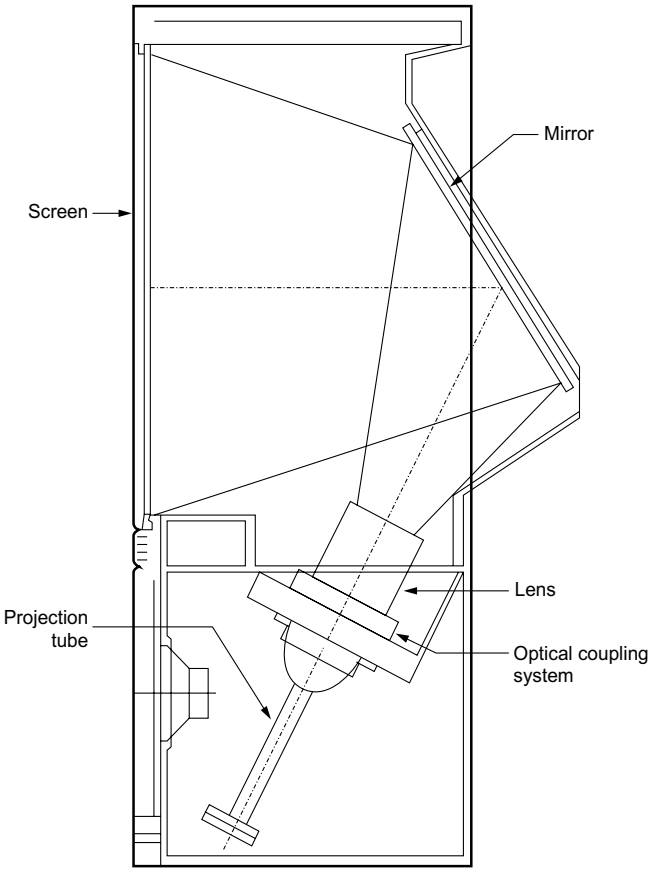


Fig. 16-4

2-2. Theory of Operation

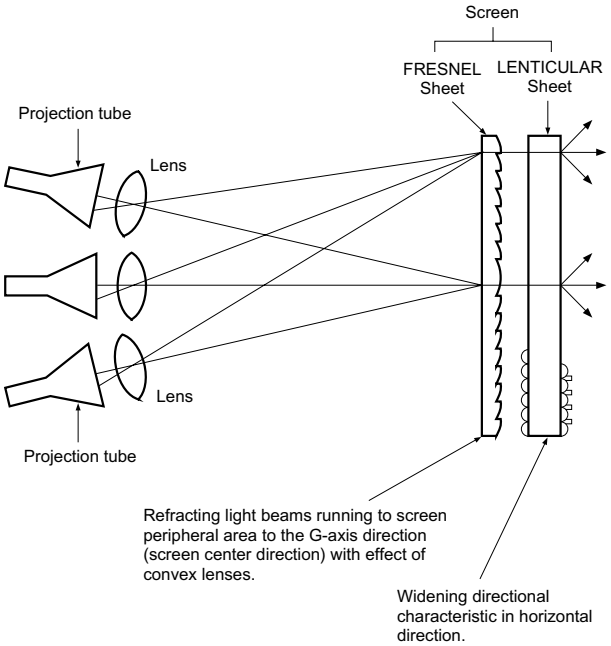


Fig. 16-5

2-3-1. Effect of Fresnel Sheet

The shape of the lens has been changed to reduce focal length.
(This allows the product size to be reduced, specifically in the distance from front to rear.)

2-3-2. Appearance of LENTICULAR Sheet

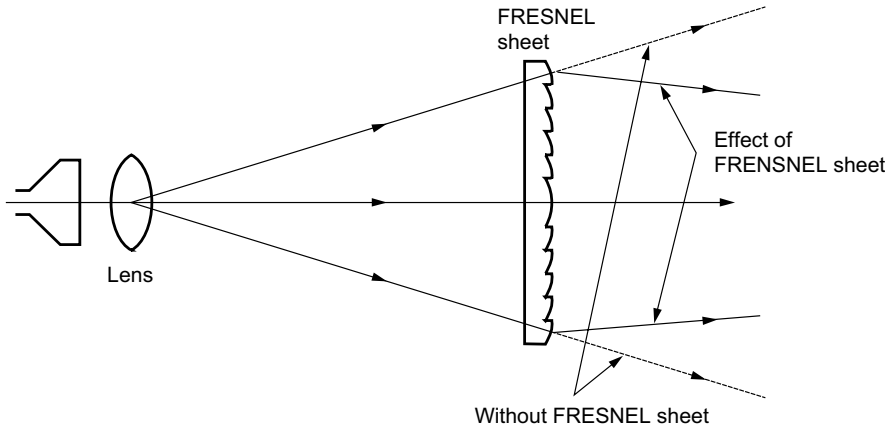


Fig. 16-6

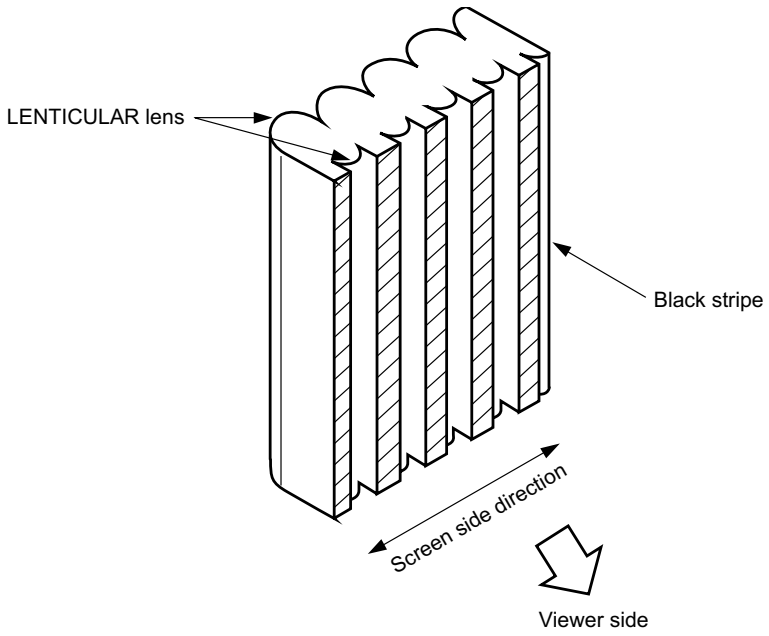


Fig. 16-7

LENTICULAR sheet

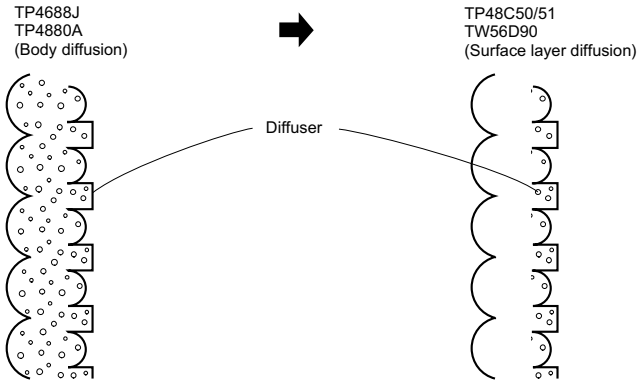


Fig. 16-8

Light beams will be effectively used by collecting the diffuser at surface of the layer, thus increasing the brightness by about 10%.

	SCREEN GAIN
TP48C60/61	5.6
TW56D90	6.2

2-3-3. Effect by LENTICULAR Sheet

If the light enters the front lenticular screen on the diagonal, the light will be diffused in the same way as parallel light incidence when viewed from the front of the TV.

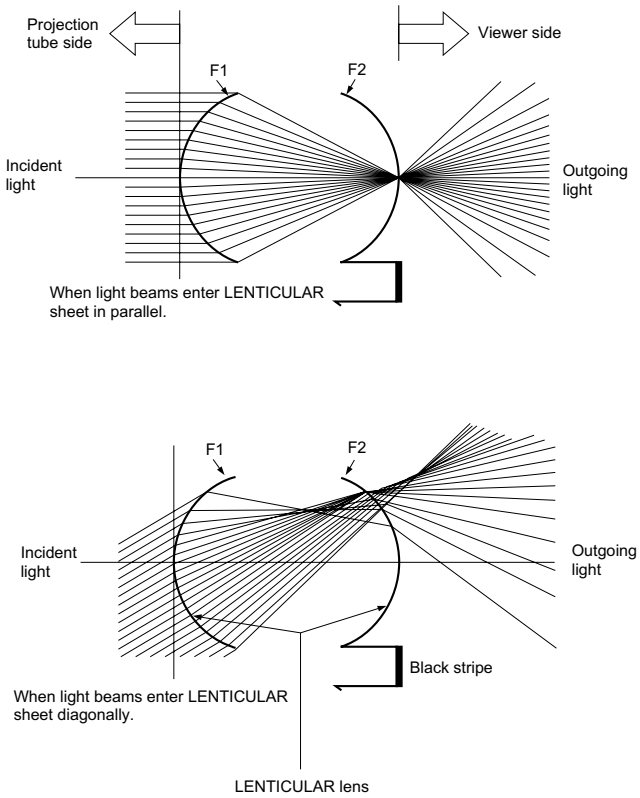


Fig. 16-9

2-4. Optical Coupling Effect

An liquid with a refraction index near that of glass is filled between the projection tube and lens to suppress:

(1) total reflection from the tube, thereby improving the contrast

(2) interfacial reflection to reduce loss of light. Moreover, with the cooling effect of the liquid, the power output of the projection tube can be safely increased.

2-4-1. Optical Coupling Effect

(1) Light beams ①, ② emitted from the fluorescent surface A advance up to the lens, but light beam ③ returns to the fluorescent surface due to the total reflection.

(2) This extremely lowers the contrast at the fluorescent surface.

Assuming that the reflection index of air is 1.0 and that of glass 1.5, the angle which causes the total reflection is 41.8° That is, the light beams with an angle of q higher than 41.8° can not exit from the projection tube. The light beams returned to the fluorescent surface reaches 56% of the total beams coming out from A.

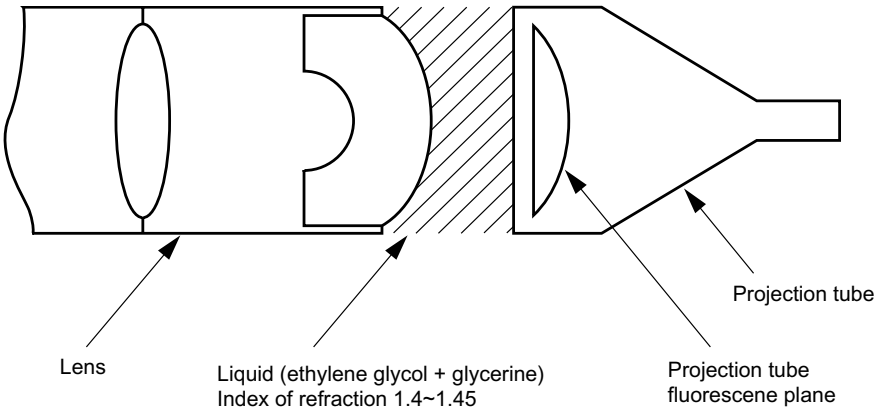


Fig. 16-10

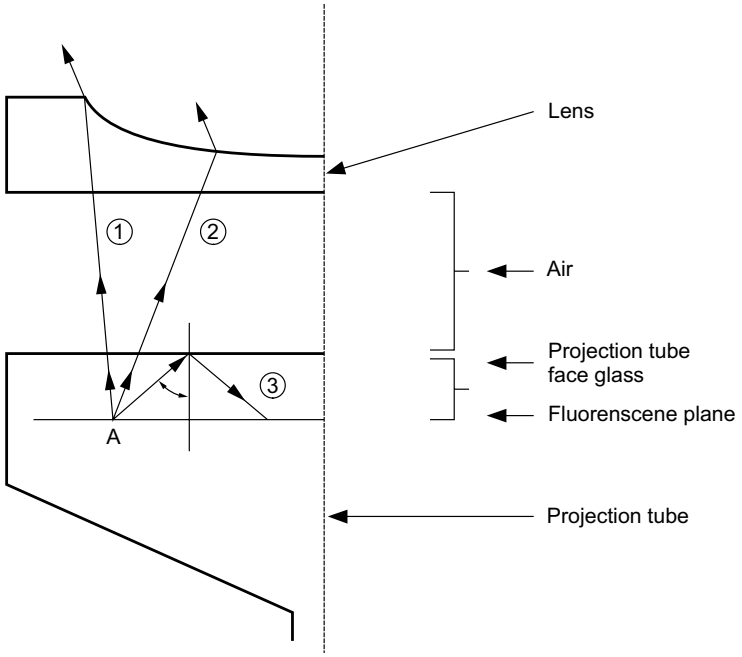


Fig. 16-11

2-5. Lens

The lens system consists of a main lens (3 pieces of lens), C lens, and the face plate of inverted gCRT (used as a lens), and realizes a short focus optical lens system with less quantity of lens.

With the short focus optical system employed, the depth of the unit is reduced by about 30%, thus making the unit slim and compact.

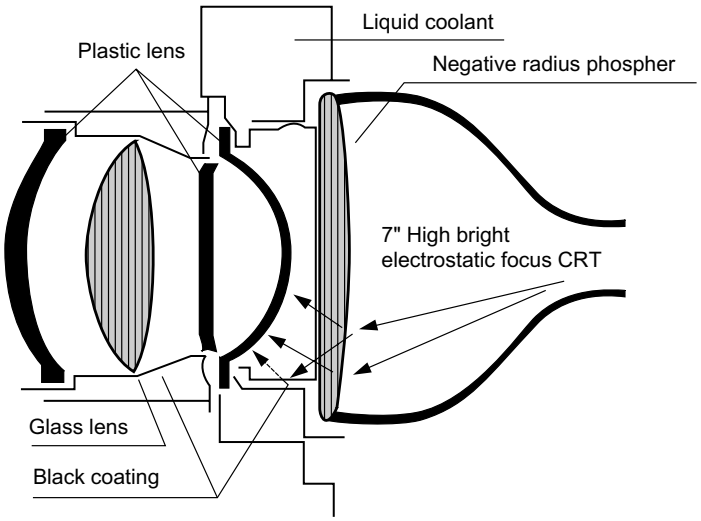


Fig. 16-12

	LENSES
TP48C60/61	USPL DELTA 77
TW56D90	USPL DELTA 79

2-5-1. Optical Coupling Effect

Note: When making adjustments on the neck components, it is always best to use dedicated drivers made of non magnetic material to avoid any distortion while making adjuctments.

Optical focus will be made according to the procedures shown below. After completion of the electrical and optical focus adjustments, convergence adjustments should be made.

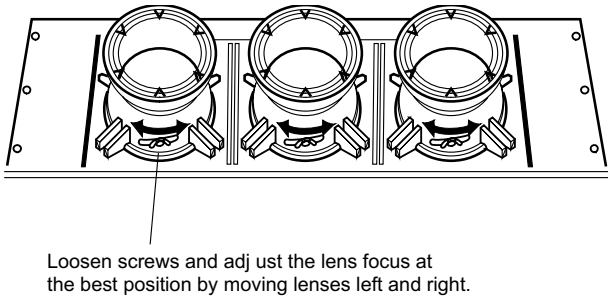


Fig. 16-13 Lens focus adjustment

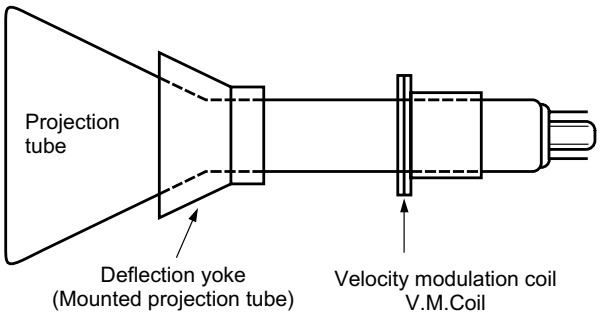


Fig. 16-14 Mounting position of deflection yoke and V.M coil

2-6. Focus Adjustment

(1) Turn on the static convergence switch and receives a cross character signal.
(2) For easy adjustment, project one color to be adjusted at a time on the screen. (Other colors can be interrupted by putting caps on the lens.)
(3) Turn the electrical focus volume for the color to be adjusted clockwise or counterclockwise so that the focus at center of the cross character shows the best.
(4) Loosen screws securing the lens and move the lens toward left and right until the best focus is obtained at center of the cross character.
(5) repeat steps 3 and 4 to obtain the best focus. Finally, secure the screws.
(6) Perform the convergence adjustment according to the convergence adjustment method.

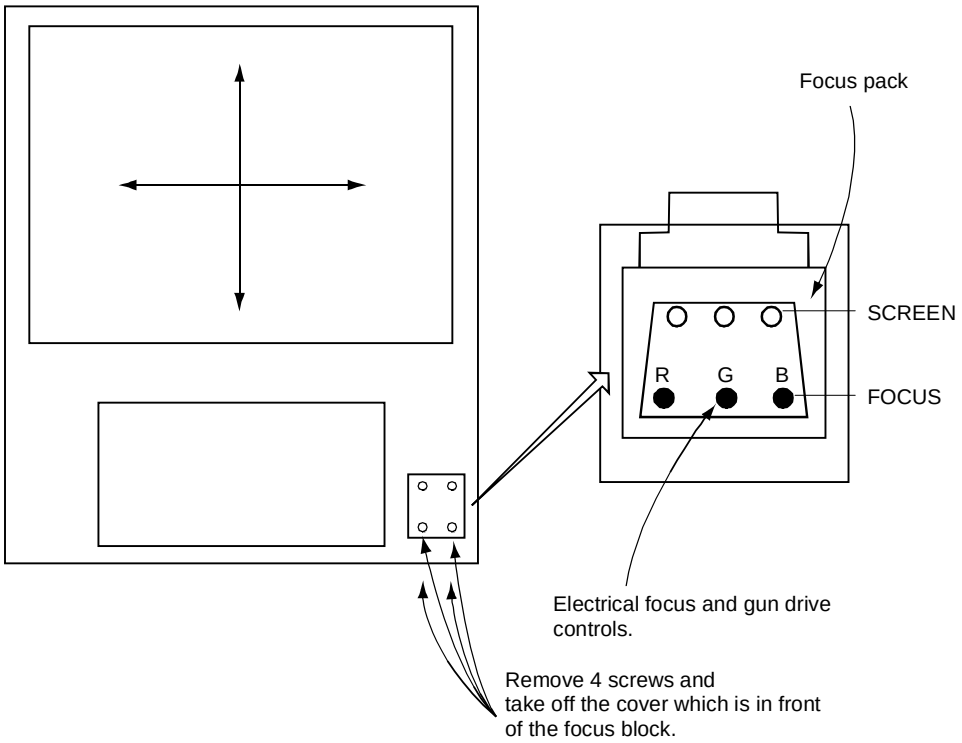


Fig. 16-15

NOTES

Chapter XVII
Power Supply

Notes:

1. Power Supply Overview

A block diagram of the power circuit is shown in fig. 17-1. The power circuit consists of the following:

1) Standby Supply, which supplies the +5V-1 Standby to the microcomputer and +12V Standby to the On/Off Relay (SR81).

2) Main Supply which supplies HORIZONTAL OUTPUT B+ (+125V) and AUDIO OUTPUT Vcc (+38V). The signal process circuits are supplied by +5V-3, +5V-2, and +9V-2 via regulators from the 12V source of the Main Supply.

3) Sub Supply which supplies +30V, +15V and -15V for the convergence output board.

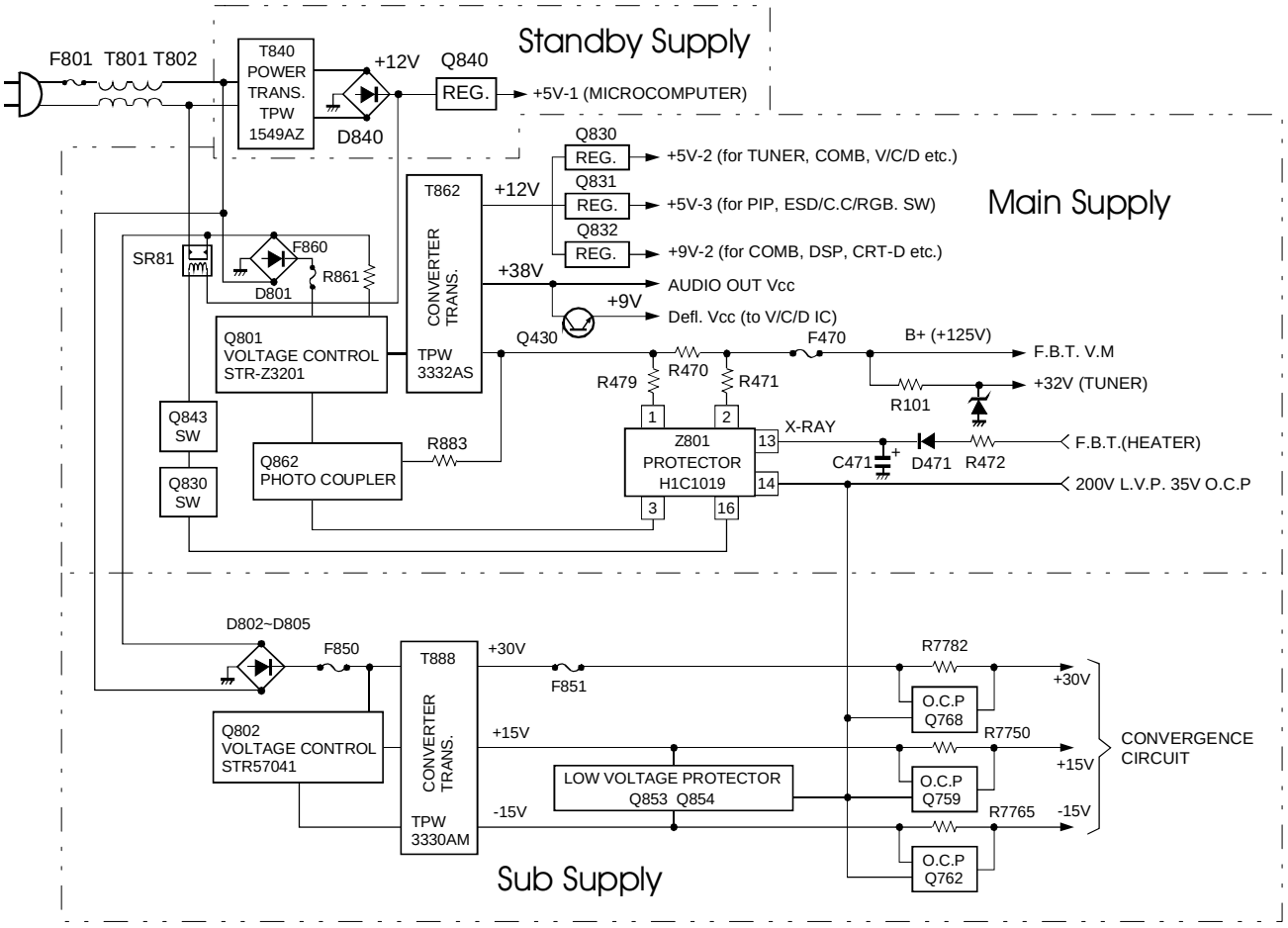


Figure 17-1 Power Supply Block Diagram

2. Rectifying circuit and standby power supply

The rectifying circuit generates dc voltage sources from the 117 Vac input. D899 is a metal oxide varistor used to absorb surges due to line spikes, lightning, etc. The arrow in fig. 17-2 indicates the path in which the surge is bypassed. C801, T801 and T802 are filters for abnormal radiation or line noise. For direct view sets the degaussing circuit, using a thermistor, is supplied after SR81 (not shown). R810 is used to suppress surge current during switch-on. D801, along with C810, output a rectified and smoothed DC voltage. T840 is the standby power transformer. D840 along with C840 output a rectified and smoothed 12V signal for driving relay SR81 and for supplying the +5V regulator, Q840. Q840 supplies the standby +5V-1 and the reset signals for the microcomputer as well as other circuits. When the power is switched on, QA01 (ICA01), the Main Microcomputer, sends a high signal from pin 7 to the base of QB30, turning it on. This causes the base of Q843 to go high and thereby turn it on. When Q843 turns on, current flows through the coil of SR81, activating the relay and thereby switching the main power on.

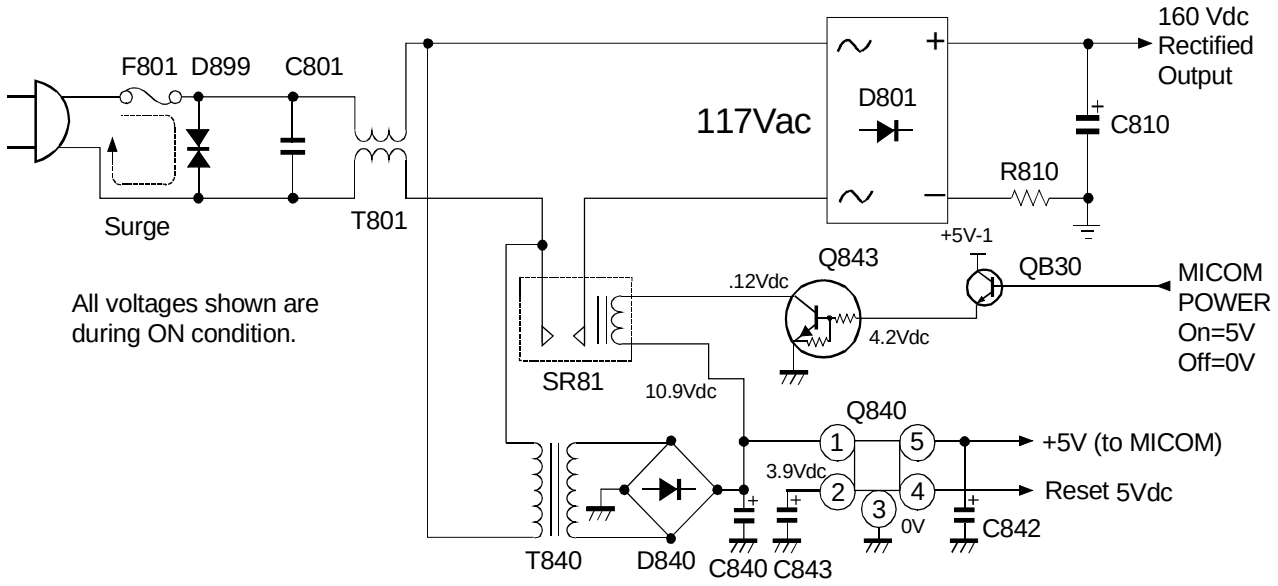


Figure 17-2 Standby Supply

3. Main Supply Circuit

The circuit in fig. 17-3 is a current resonant switching type power supply that incorporates a hybrid IC, Q801 (STR-Z3201). The current resonant power circuit is highly efficient in that it operates with very low power consumption and very little noise. In the case of a short on the load side of T862, the AUDIO OUTPUT, Low B, and B+ circuits are protected with F899, F890 and F470 respectively. F860 is used to protect the primary side of T862.

4. Outline of Current Resonant Type Supply

Fig. 17-3 shows the configuration for the Current Resonant type power supply. A start-up voltage is sent to Pin 10 to begin operation. VIN source voltage of 160V is applied to Pin 1. Pin 14 is tied to ground for the negative phase of the MOS-FET configuration. The Primary winding of T862 and C870 are connected in series to form an LC Series Resonant Circuit. The converter transformer, which is driven by a push-pull MOSFET configuration located inside Q801, operates in forward mode.

The automatic voltage control operation is performed by the detection of the B+ voltage (125V) fed into the error amp, Pin 5, of IC Z801, then output through Pin 3 to the photo coupler. Next this signal is fed into the primary Oscillating (OSC) circuit, located inside IC Q801 (Pin 6) which controls the frequency of the ON/OFF time, via an internal logic IC, for the MOS FET configuration.

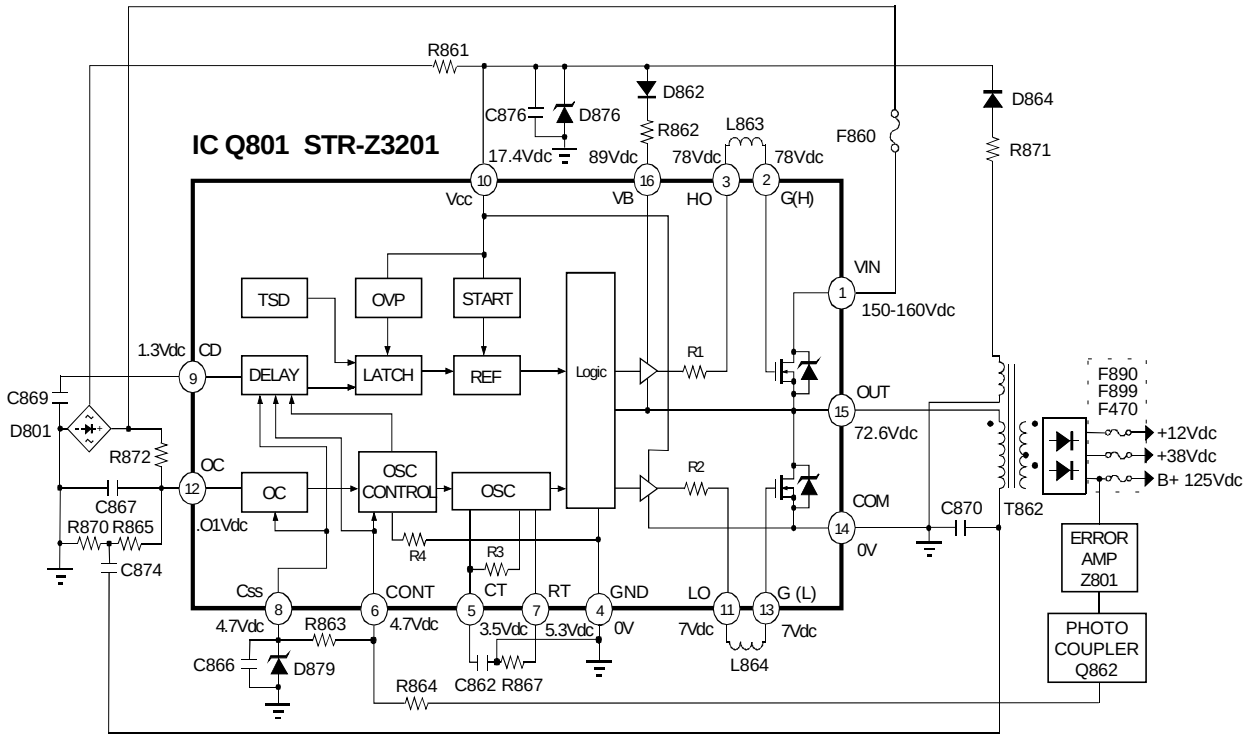


Figure 17-3 Current Resonant Supply (Main)

5. Fundamental Theory of LC Series Resonant Circuit

The LC series resonant switch mode power supply is a frequency regulated power supply operating above resonance (see figures 17-3 and 17-4). The LC series resonant circuit is composed of the primary winding of T862 and C870. A negative feedback circuit is used to control the output of the transformer. The feedback circuit, which monitors the 125Vdc source, is composed of the error amp inside Z801 and the photo coupler (Q862). This feedback is applied to the CONT input (Pin 6) of IC801 to control the frequency of the internal oscillator (OSC). When the load increases on the secondary side of the transformer, the frequency decreases (operates closer to resonance) and the current increases. Conversely, when the load decreases, the frequency increases and the current decreases. Table 17-1 shows the voltages developed on T862 secondaries.

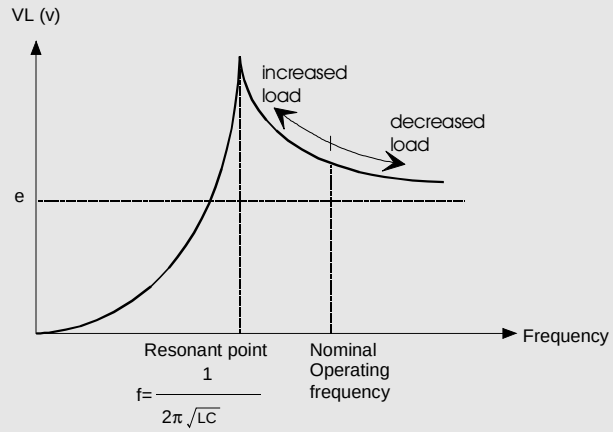


Fig. 17-4 Resonance Curve

Table 17-1 T862 Voltage Chart

T862 Pin #	Voltage
Pin 2*	47 Vp-p
Pin 3 Ground	Hot Side*
Pins 4, 5*	148 Vp-p
Pins 6, 7*	127 Vp-p
Pin 9	27 Vp-p
Pin 10	27 Vp-p
Pin 11, 12, 15	Ground, Signal Side
Pin 13	256 Vp-p
Pin 14	256 Vp-p
Pin 16	81 Vp-p
Pin 17	81 Vp-p

* Reference Hot Side Ground (T862, Pin 3) when measuring Pins 2, 4, 5, 6, and 7. **CAUTION, USE ISOLATION TRANSFORMER**.

6. Main Supply Actual operation

Refer to Figure 17-5 diagram and waveforms.

1. **Start-up**

   When power is applied to the set, a start-up voltage of 16V is applied to pin 10 of IC Q801. At the same time, charging of C869 (pin 9) induces a delay to the internal latch circuit to prevent the Over Voltage Protect (OVP) circuit from shutting the set down.

2. **Output switching element**

   Two power MOSFETs operating in push-pull mode are used for switching. The on-off timing of each is controlled by the logic inside Q801. To avoid a short circuit from occuring a delay is used between the turn off of one MOSFET to the turn on of the next.

3. **CT terminal (Pin 5) - basic oscillation**

   The frequency of the internal oscillator is controlled by the Oscillator Control block. The frequency is determined by the charge and discharge of capacitor C862 connected to CT terminal. The oscillator generates a ramp waveform at Pin 5. The ramp waveform charges up to 4 V (typical) and discharges to about 2.5 V. The charging time is the output-on period, and discharging time is the off period (see OSC OUT SIGNAL waveform of Figure 17-5). The lowest oscillation frequency is determined by capacitor C862 and resistor R867.

4. **CONT (Pin 6) - frequency control**

   Current flowing out of the CONT terminal (Pin 6) varies the charging current of oscillator capacitor C862, which in turn controls the frequency of the Output (Pin 15) signal. The control current is determined by the Photocoupler. The Photocoupler phototransister side current is determined by the feedback current of the photodiode side. The photodiode current is determined by the Error Amp inside of Z801, which is monitoring the +125V source. Thus, the terminal current (CONT) corresponds to the feedback from the +125V output.

5. **Css terminal (Pin 8) - soft start**

   When power is first applied, the switching frequency is set high by capacitor C866 and resistor R863, resulting in soft start of the switching supply. Thus, current (surge) in the POWER MOSFET output is limited to provide stable starting of the supply sources. After initial start-up, the circuit operates at its nominal frequency (70-80 kHz).

6. **CD terminal (Pin 9) - Latch Delay**

   The Latch circuit shuts the power supply off (shut-down) when a fault is detected. Shut-down occurs by detecting errors from the following:

   • Over voltage protection (OVP) circuit

   • Thermal shock detection (TSD) circuit

   • Over current protection (OCP) circuit

   • Loss of and no recovery of Main B+

   The charging time of capacitor C869 connected to the CD terminal (Pin 9) is used to delay the operation of the Latch circuit when power is initially applied. If the unit goes into shut-down, temporarily remove ac power to reset the latch circuit.

7. **OC terminal (Pin 12) - Over Current Detect**

   This is to detect over-current in the LC series resonant circuit.

8. **Over voltage protection (OVP) circuit**

   If the Vcc terminal (Pin 10) exceeds 22V (typical), the Latch circuit is engaged (shutdown) .

9. **Thermal shock detection (TSD) circuit**

   This is to make the Latch circuit operate when the IC's internal temperature exceeds 150°C.

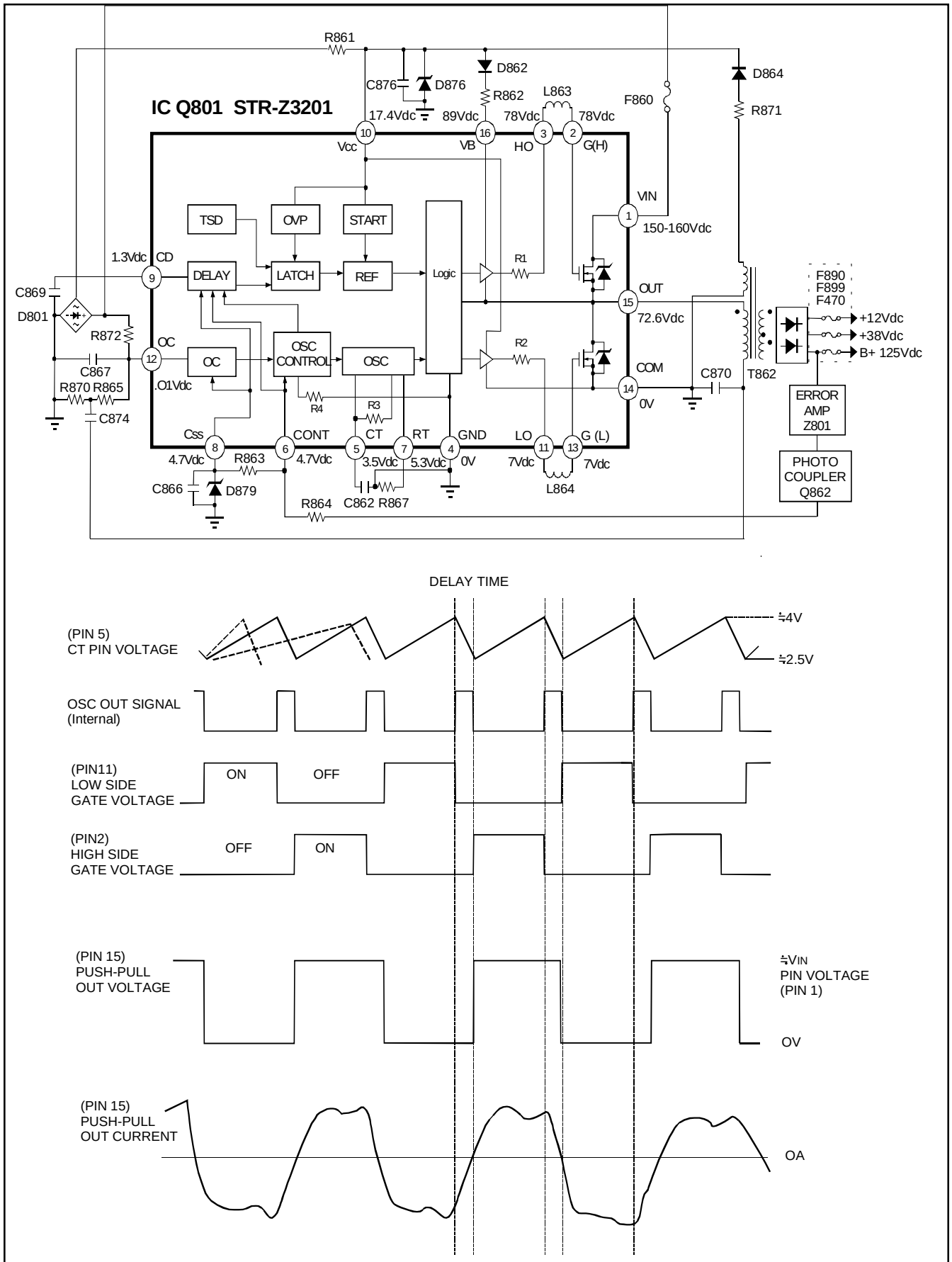


Figure 17-5 Current Resonant Supply with Wavefoms

7. Scan-Derived Voltages (FBT)

Figure 17-6 shows the voltages derived from the FBT of the Horizontal Deflection circuit. The FBT derives 200V for the Video Output circuit from pin 3, +35V for the Fail Safe, H.V. Regulator, Blanking, Dynamic Pin Cushion (DPC), and Vertical Deflection (V.D.) circuits from pin 6, and -27V for the side DPC circuit from pin 5, Heater voltage from pin 9, Automatic Frequency Control (AFC) and blanking signal from pin 10, and the Automatic Black Level (ABL) signal from pin 8. A 12Vdc source is also derived, via pin 7 and D408, to supply the SVM and DPC circuit boards. In addition, the 12Vdc source is used to develop the +9V-1 source via a 9 Volt regulator made up of Q420, Q421, and D427. High voltage is supplied from the secondary along with Focus and Screen voltage sources developed from a tap on the high voltage secondary of T461.

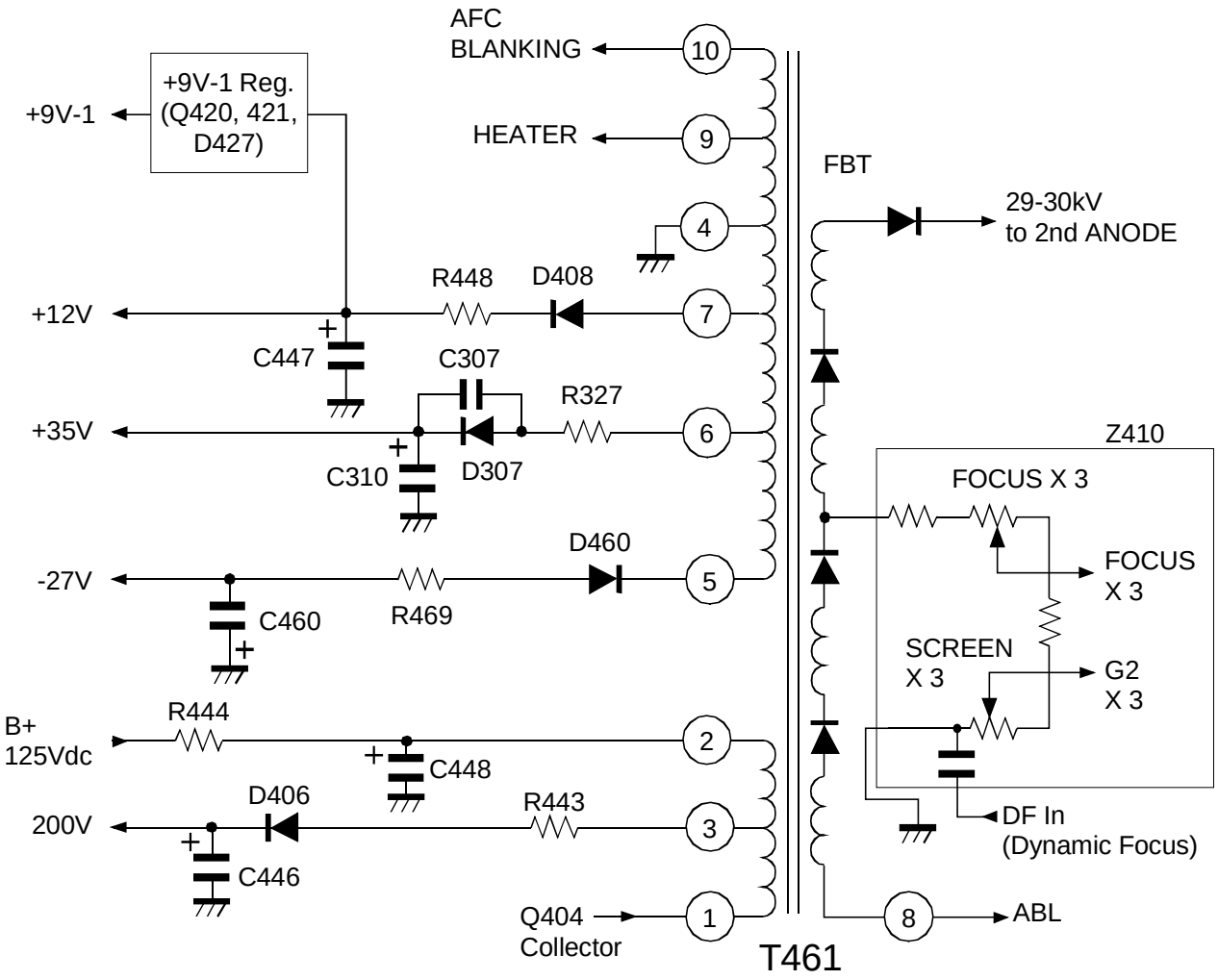


Figure 17-6 Scan Derived Sources

8. Protector Module (Z801)

Figure 17-7 shows the standardized protector module (Z801). The following are the four different sections within the Protector Module: Error Amp, Switch/Latch, B+ OCP, and X-Ray Protect. In addition the Over Current Protect (OCP), Over Voltage Protect (OVP), and Under Voltage Protect (UVP) circuits are routed through the internal Switch/Latch circuit to trigger the unit off through the Protect output (Pin 16).

The **Error Amp circuit** monitors the B+, 125V line, via Pin 1. The Error Amp controls the current through the photodiode of photocoupler Q862. When the B+ voltage decreases Q862 conducts less and when it increases, Q862 conducts more.

The **Switch/Latch circuit** is used to turn off SR81 relay in case of over current, over voltage or under voltage. In shutdown mode, Pin 16 (Protect) latches low, which turns QB30 off. When QB30 turns off Q843 turns off. This causes the relay (SR81) to open and thereby disconnect the power.

In the **B+ Over Current Protect (OCP) circuit**, the current is being compared across R470, which is applied through Pins 1 and 2. The resistance of R470 is so small that changes in voltage equate to larger changes in current. When a large enough change in voltage occurs the internal latch circuit outputs a low on Pin 16, which shuts the unit down.

In the **X-Ray Protect circuit,** Pin 11 provides a reference voltage of +25V. If the High Voltage increases abnormally, Pin 9 of T461 senses the increase and increases the voltage through R472. This increased voltage is applied to D471, which rectifies AC to DC. The increase in Vdc is applied to Pin 13, which will trigger the internal latch circuit and output a Low on Pin 16. As long as +5v-1 is applied to pin15, the remote control hand unit will not recover the power. The AC power line must be disconnected to reset the latch.

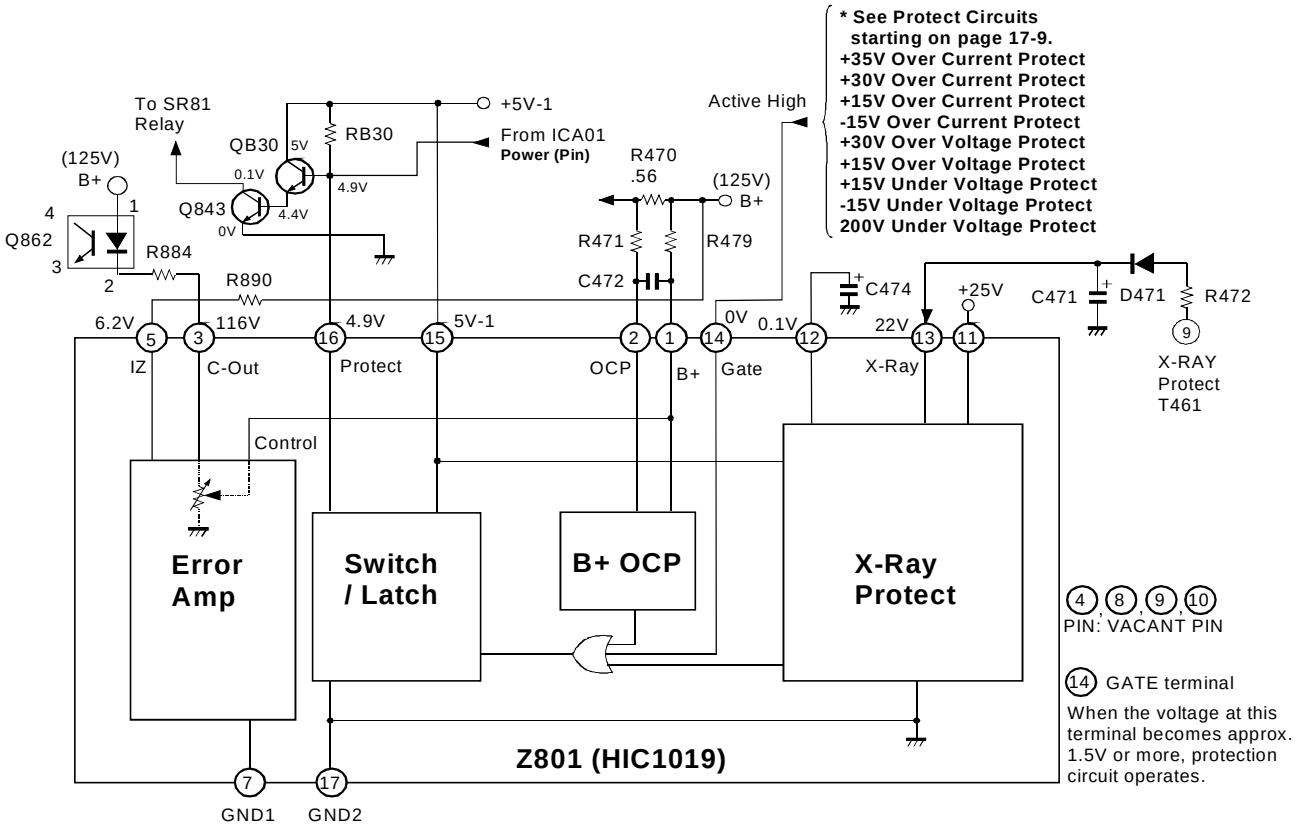


Figure 17-7 Protector Module Circuit

9. Sub Supply

The Sub Supply is located on the Convergence Out/Power2 board. Figure 17-8 shows that the Sub Supply is a ringing choke converter, using hybrid IC STR57041. Operation begins with a start-up voltage that is applied through R852. This provides a trickle base current to Q1 (internal to the IC, Pin 2 of Q802), which causes it to turn on. When Q1 turns on, the collector current begins to flow. During this start-up time the current is flowing through the primary winding of T888 through Pins 2 and 5. At the same time current will flow through Pins 7 and 8, which create the detection winding, as well as Pins 8 and 9, which create the base drive winding. During the first half cycle of the AC pulse no current flows through the detection winding because of the reversed polarity of D856. Pin 9, however, provides positive feedback for the base, as the electromagnetic inductance increases, to rapidly turn Q1 on. As Q1 becomes saturated the current through the primary winding decreases.

This decrease in current through the primary winding, reduces the electromagnetic inductance across the base drive winding, which decreases the voltage to the base of Q1 and thereby rapidly turns Q1 off.

T888 uses a detection type winding through Pins 7 and 8. The secondary windings are proportional to the detection winding. Subsequently, any fluctuation in voltage across the secondary windings is sensed across the detection winding which is fed back through Vo sense (Pin 1). This feedback is used to regulate the On/Off time of the internal switching transistor Q1.

R846, C845, R852 and D848 create a voltage clamping circuit that allow the collector voltage of Q1 to stay within a specified level. R847, C855, R848 and D849 filter the base voltage. Q850, Q851, Q852, C856, D855, R857 and R859 create the Slow-start circuit. C856 determines the rate of the start-up time.

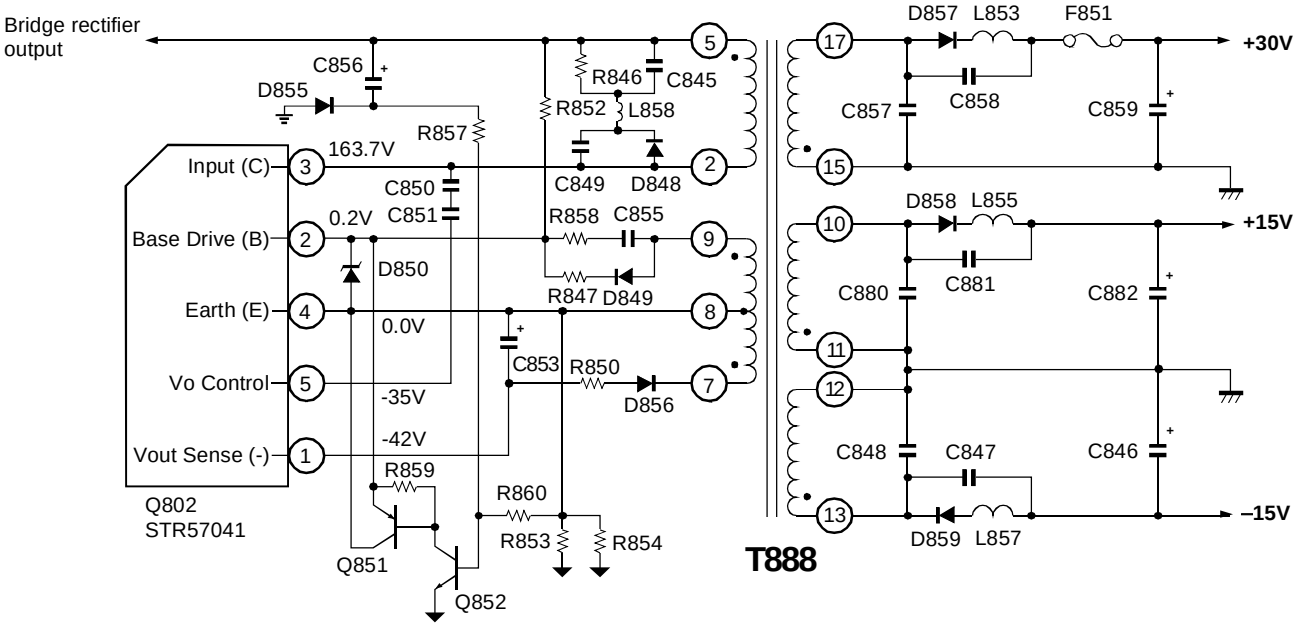
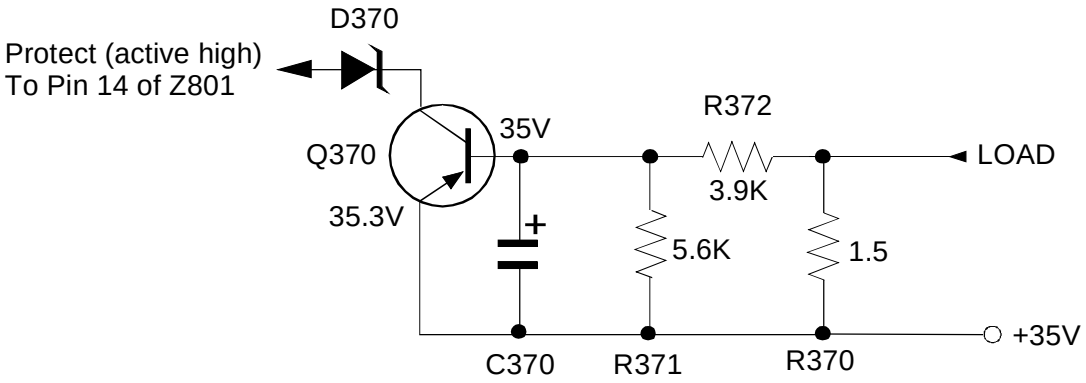


Figure 17-8 Sub Supply

10. Protect Circuits



+35V OVER CURRENT PROTECT CIRCUIT
(Located on Deflection/Power board)

Figure 17-9 +35V Over Current Protect Circuit
(Located on Deflection/Power Board)

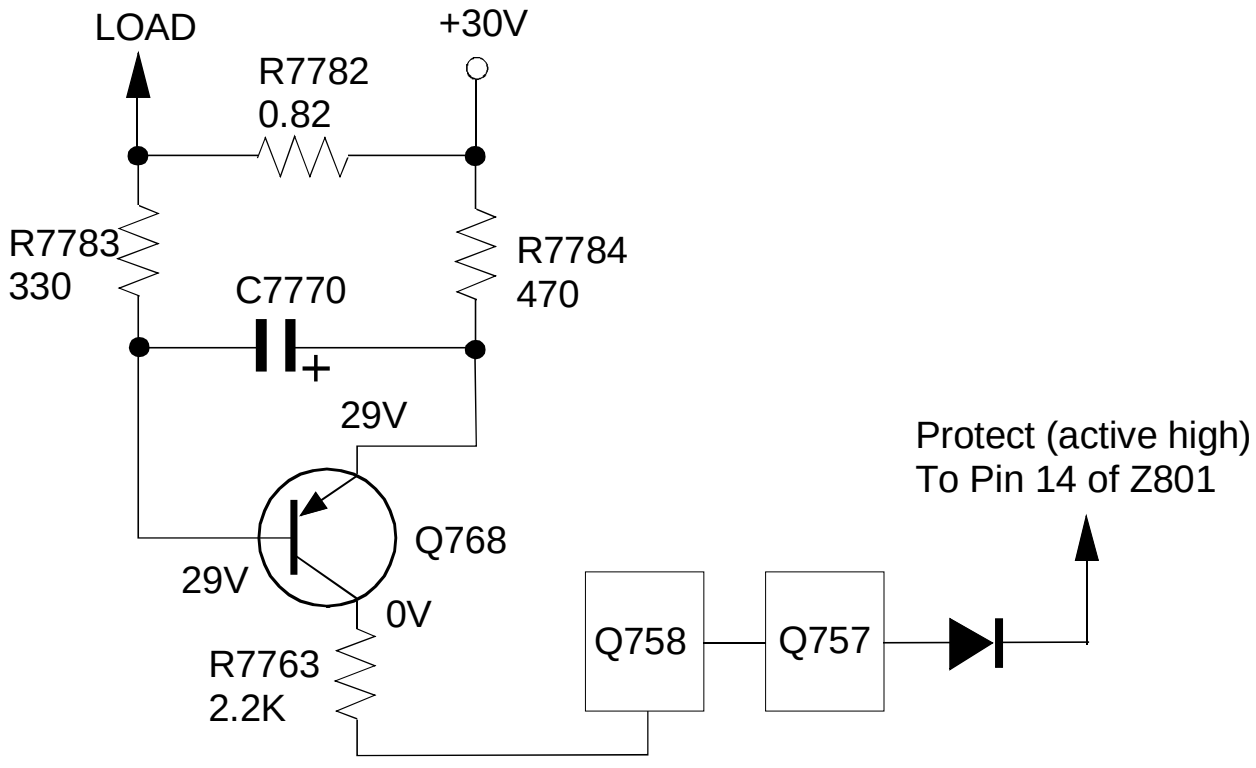


Figure 17-10 +30V Over Current Protect Circuit
(Located on Convergence Out/Power2 Board)

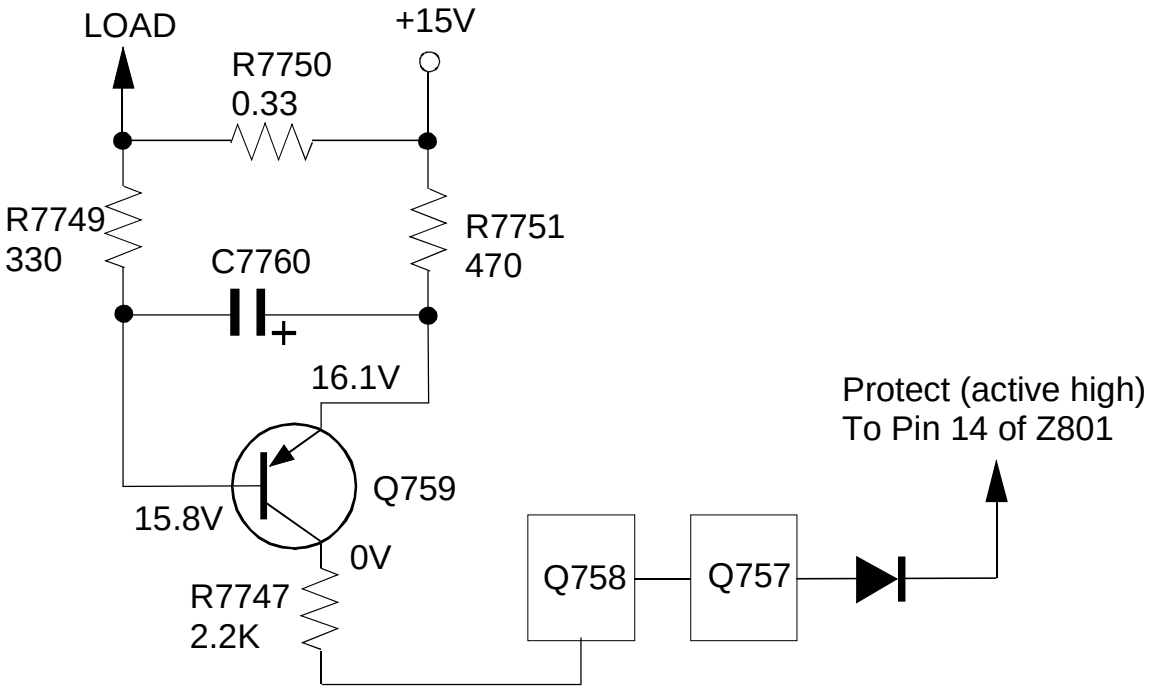


Figure 17-11 +15V Over Current Protect Circuit
(Located on Convergence Out/Power2 Board)

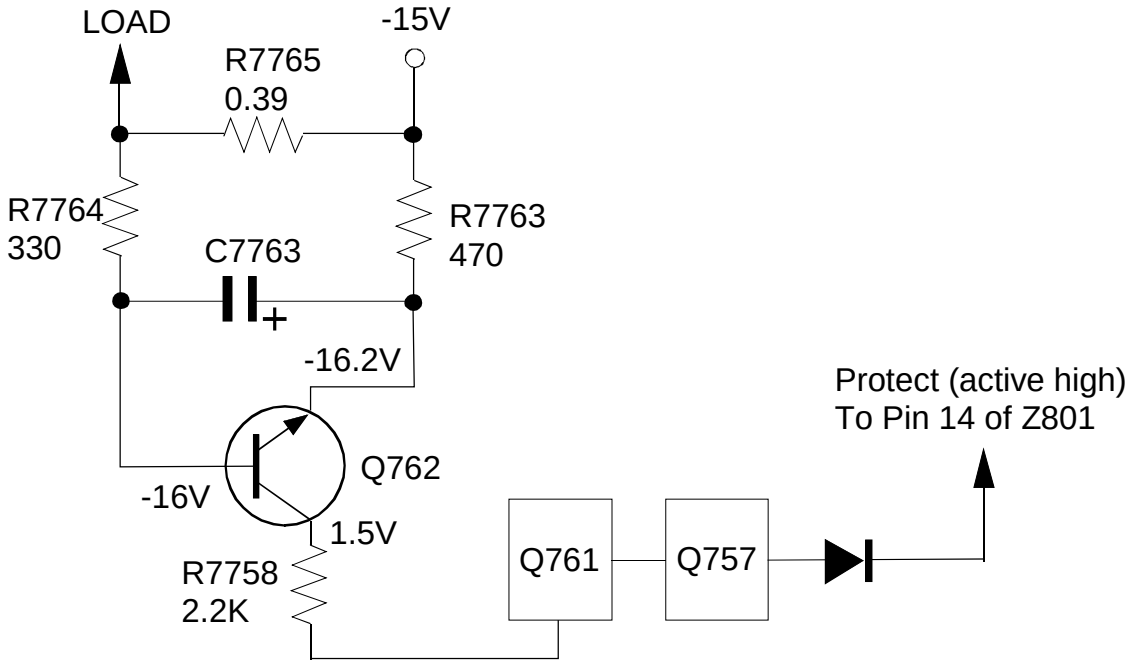


Figure 17-11 -15V Over Current Protect Circuit
(Located on Convergence Out/Power2 Board)

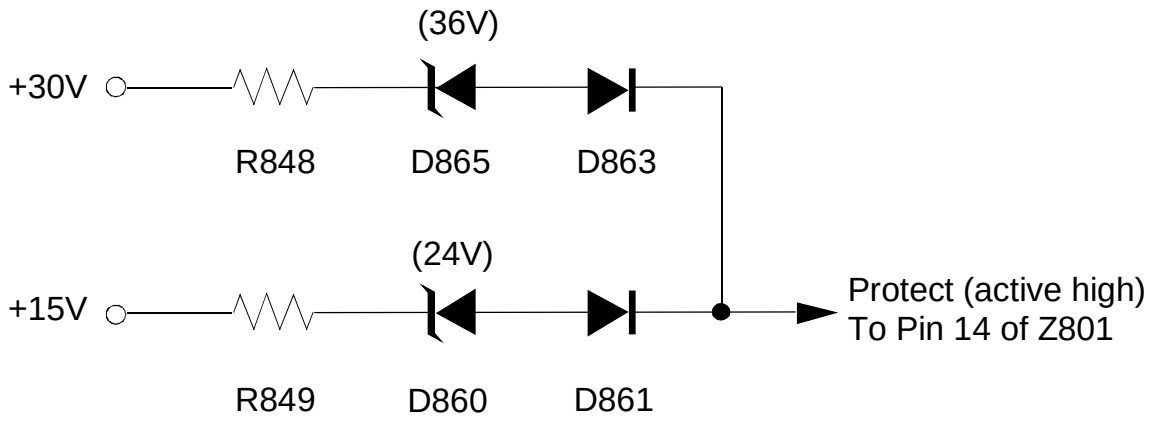


Figure 17-12 +30V/+15V Over Voltage Protect Circuit
(Located on Convergence Out/Power2 Board)

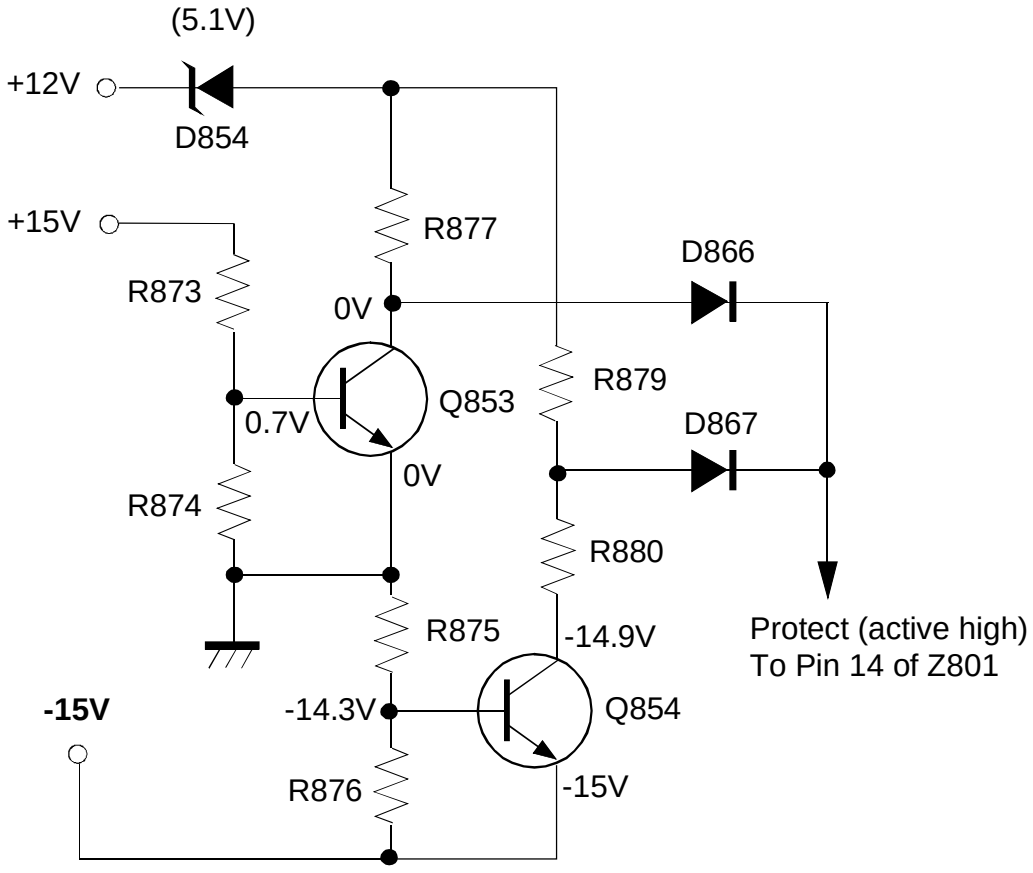


Figure 17-13 +15V/-15V Under Voltage Protect Circuit
(Located on Convergence Out/Power2 Board)

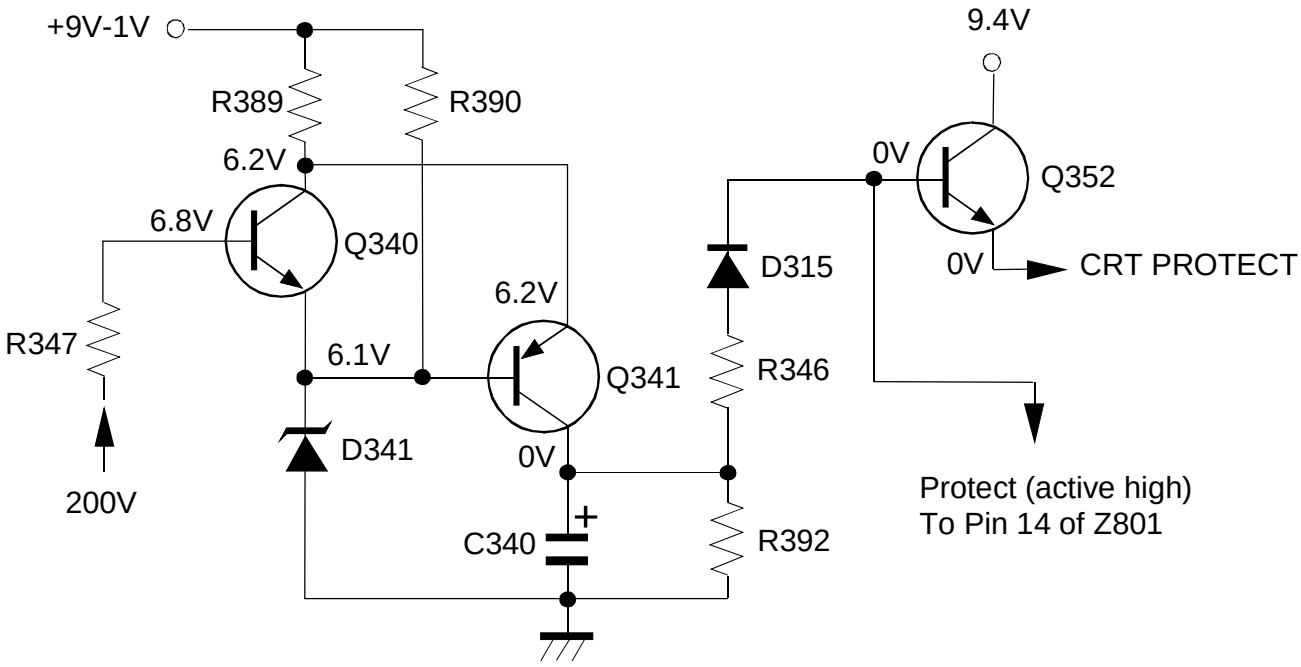


Figure 17-14 200V Under Voltage Protect Circuit
(Located on Convergence Out/Power2 Board)

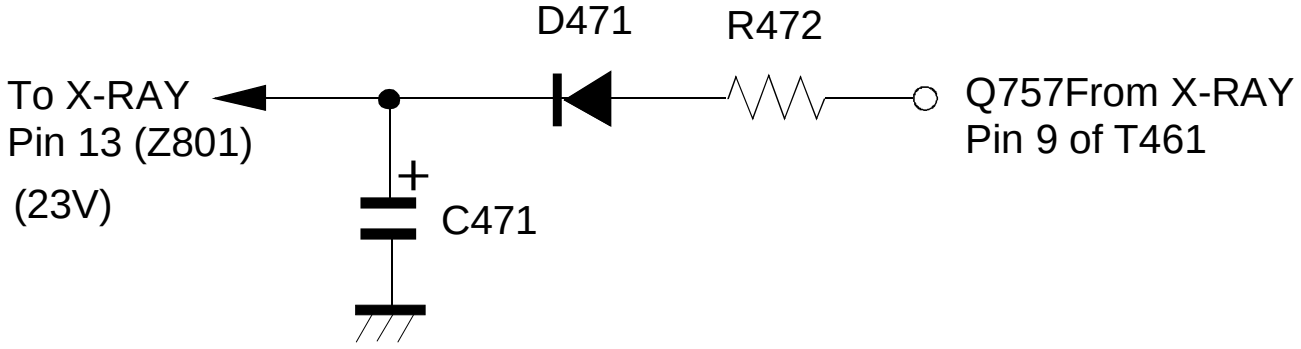


Figure 17-15 X-Ray Protect Circuit
(Located on Deflection/Power Board)

LAB 4

POWER SUPPLY SHUTDOWN CIRCUITS

SECTION 1
VOLTAGES UNDER NORMAL CONDITIONS

Place the unit in the service position by removing the chassis light box and place it on its side in an upright position with the power cord up. (See FIG. 17-16) Connect a signal to the ANT1 input. You may want to refer to the actual schematic diagram for a clearer understanding of the circuitry.

PROTECT CIRCUIT MEASUREMENTS:

1. Connect the (-) lead of the peak/hold meter to pin 17 of Z801 (See FIG. 17-16, #1) and record the DC voltages on the following pins:

   PIN 11)_____
   PIN 13)_____
   PIN 14)_____
   PIN 15)_____
   PIN 16)_____

RELAY CONTROL CIRCUIT MEASUREMENTS:

2. Locate Q843. (See FIG. 17-16, #2) Record the voltages on the following:

   C_____
   B_____
   E_____

3. What does Q843 control, and how does it control it?

   _____

   _____

   _____

OVER CURRENT, OVER VOLTAGE, AND UNDER VOLTAGE PROTECT CIRCUIT MEASUREMENTS:

4. Connect the (-) lead of the p/h meter to the (-) side of C882 (See FIG.17-16, #3).

5. Measure the voltage on the anode side of D865. (See FIG.17-16, #4)

   Anode D865_____

6. Measure the voltage on the anode side of D860. (See FIG. 17-16, #5)

   Anode D860_____

7. Measure the voltage on the collector of Q853. (See FIG. 17-16, #6)

   Collector Q853_____

8. Measure the voltage on the anode side of D867. (See FIG. 17-16, #7)

   Anode D867_____

9. Measure the voltage on the collector of Q757. (See FIG. 17-16, #8)

   Collector Q757_____

10. Connect the (-) lead of the p/h meter to the (-) side of C310 (see FIG. 17-16, #9).

11. Measure the voltage on the collector of Q370. (See FIG. 17-16, #10)

    Collector Q370_____

SECTION 2
VOLTAGES UNDER SHUTDOWN CONDITION

1. Locate the (X) pin (P415) and the (R) pin (P416) (See FIG. 17-16, #11)

2. While monitoring pins 13 and 16 of Z801 on the p/h meter, jumper pins (X) and (R) together.

3. After the shutdown, record the voltages on pins 13 and 16 of Z801. (See FIG. 17-16, #1)

   PIN 13)_____

   PIN 16)_____

The above exercise allows you to see what happens when the X-Ray protect circuit shuts down the set.

4. How is this determined?

   _____

   _____

   _____

NOTE: SHUTDOWN OCCURS WHEN THE VOLTAGE INCREASES TO APPROXIMATELY 25V.

5. While shorting the base of Q853 (See FIG. 17-16, #6) to ground, monitor and record the collector voltage using the p/h meter.

   Collector Q853_____

6. What have you simulated by shorting the base to ground?

   _____

   _____

   _____

7. Why does a change occur on the collector and where is this change sensed?

   _____

   _____

   _____

8. Look on the schematic diagram labeled “Convergence Out/Power2”, in the upper right side. Find D865 (zener diode) on the +30V supply line. How would you determine what the peak voltage would be before the over voltage protect circuit would operate?

   _____

   _____

   _____

9. Look on the schematic diagram labeled “Convergence Out/Power2”, in the upper right side. Find D860 (zener diode) on the +15v supply line. How would you determine what the peak voltage would be before the over voltage protect circuit would operate?

   _____

   _____

   _____

10. Remember when you measured the anode sides of D865 and D860 earlier? Well, if the set, your working on, is in shutdown mode, how would you determine if it was caused by over voltage on the +30v or +15v lines?

    _____

    _____

    _____

11. While shorting the base of Q757 (See FIG. 17-16, #8) to ground, monitor and record the collector voltage using the p/h meter.

    Collector Q757_____

12. What have you simulated by shorting the base to ground?

    _____

    _____

    _____

13. Measure the voltage drop across R7750 (See FIG. 17-16, #12), R7782 (See FIG. 17-16, #13) and R7765 (See FIG. 17-16, #14).

    R7750_____

    R7782_____

    R7765_____

14. List a procedure of how would you determine which one of the over current protect circuits were causing the shutdown?

    _____

    _____

    _____

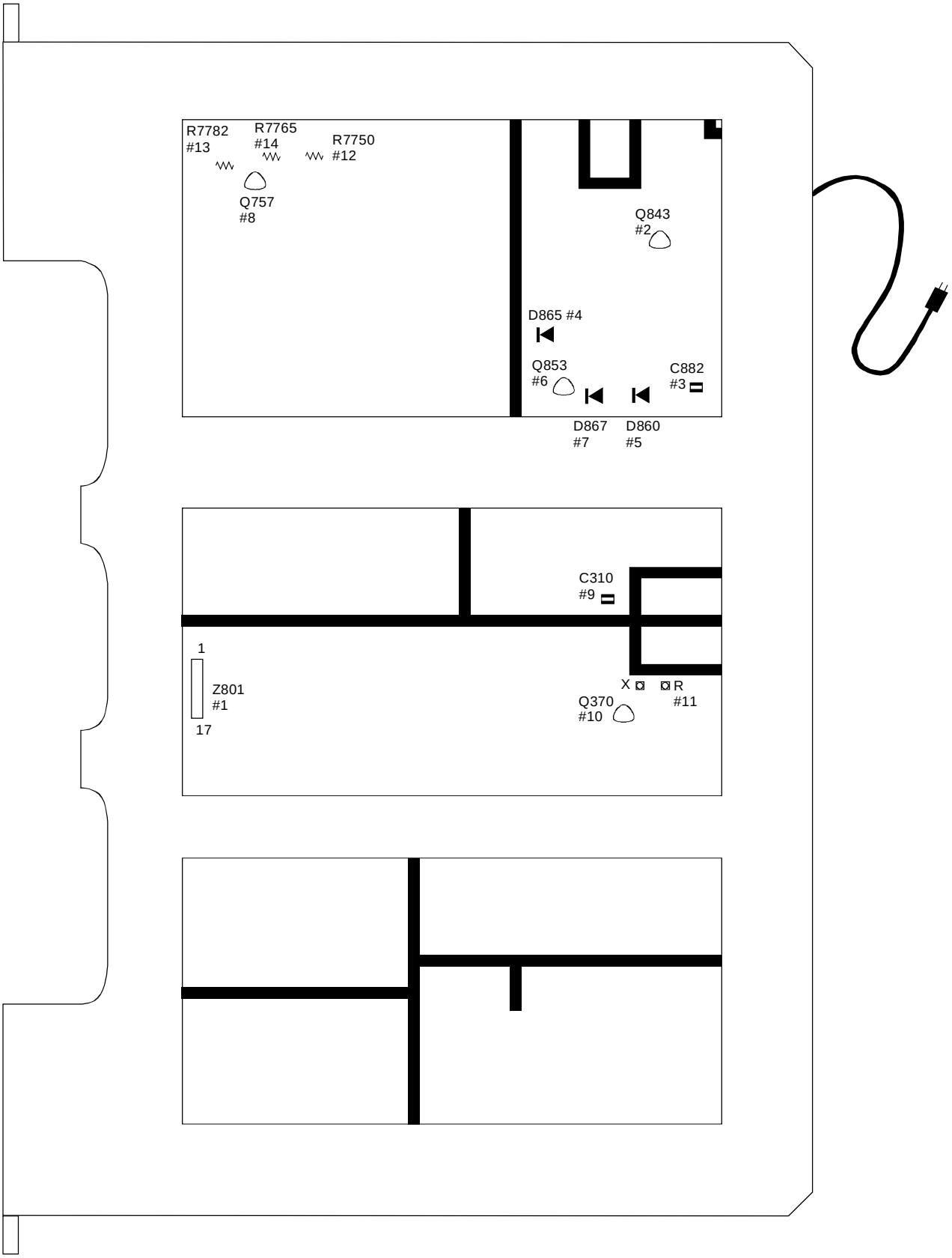

R7782
#13
R7765
#14
R7750
#12
Q757
#8
Q843
#2
D865 #4
Q853
#6
C882
#3
D867
#7
D860
#5
C310
#9
1
Z801
#1
17
X
R
Q370
#10
#11

Figure 17-16

NOTES

SECTION XVIII
DYNAMIC FOCUS CIRCUIT

1. OUTLINE

In TP48C51, a static focus system is employed in the projection tube.
Degradation of the focus quality at peripheral screen is improved by applying focus correction voltages (parabola voltages in H/V periods).
The dynamic focus circuit creates this focus correction voltage and consists of an H and a V dynamic focus circuit.

To obtain a flat focus characteristics at center and peripheral of the screen, the focus correction is carried out by applying the H sync parabola correction voltage (efH=700 Vp-p) and the V sync parabola correction voltage (eifv=300 Vp-p) to the focus electrode in addition to the focus DC voltage of Ef (=EHx0.27~0.29).

2. H DYNAMIC FOCUS CIRCUIT

2-1. Theory of Operation

Fig. 18-1 shows a block diagram of the circuit which develops an H parabora correction voltage.

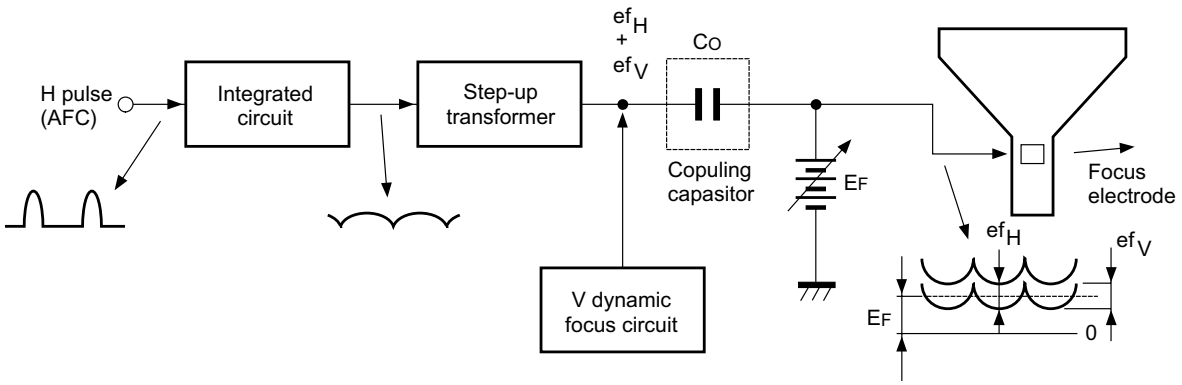


Fig. 18-1 Block diagram of H dynamic focus circuit

2-2. Circuit Operation

The H pulse developed at pin 10 of the pulse transformer T461 enters the integration circuit consisting of L450 and C_1. The C_1 does not exist in the actual circuit as shown in a dotted line. The C_1 is an equivalent capacitance of the stray capacitance of Cs in secondary side of the step-up transformer T405 converted into the primary side and can be expressed as:

$$C_1=n^2Cs$$

The H pulse is integrated with L450 and C_1, and a sawtooth wave current of IC_1 flows into C_1.

Accordingly, a parabora voltage V_1 integrated is developed across C_1 and this is used as the input voltage (primary side voltage) for the step-up transformer. A parabora voltage V_2 stepped-up and inverted is obtained at secondary side (F, P terminals) of T400. This parabola voltage is mixed with the V parabola voltage described under the V dynamic focus circuit, and the mixed voltage is superimposed with the focus DC voltage (about 9kV) through a coupling capacitor Co, and supplied to the focus electrodes of three R, G, B tubes.

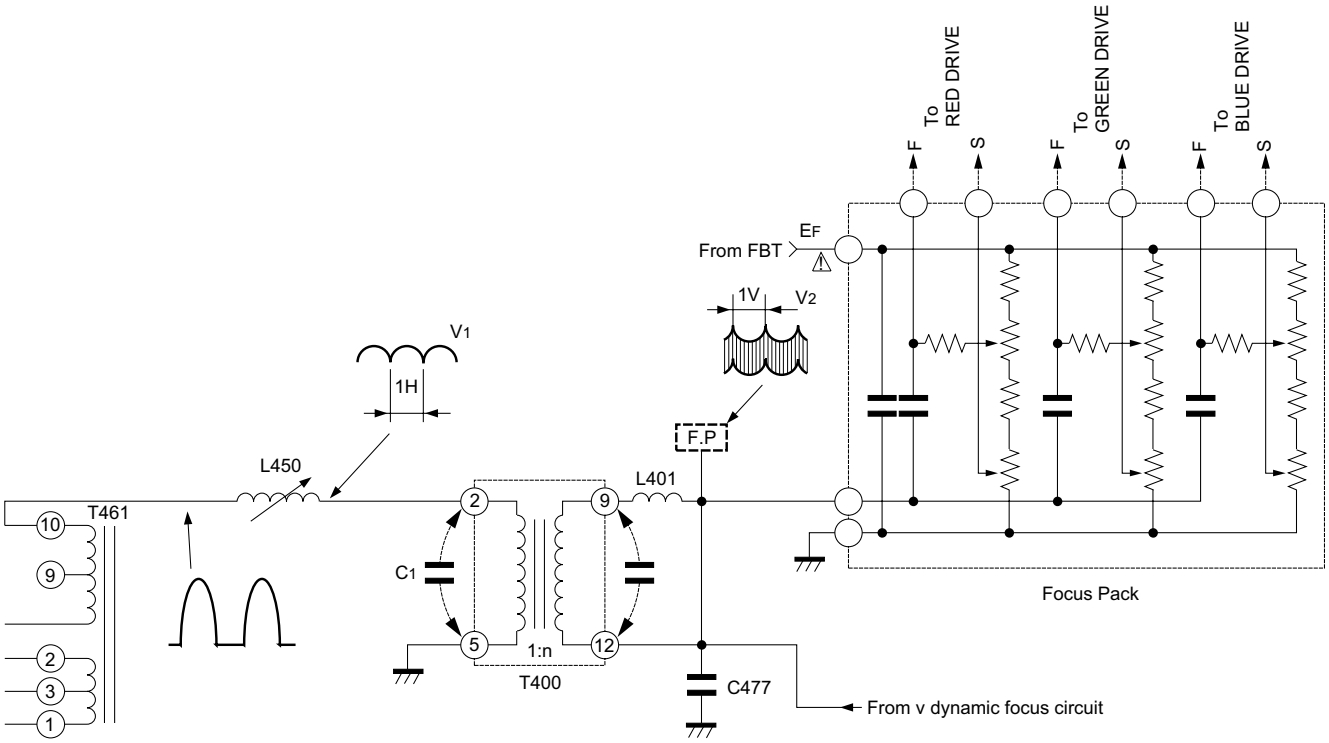


Fig. 18-2

3. V DYNAMIC FOCUS CIRCUIT

3-1. Theory of Operation

Fig. 18-3 shows the circuit which develops the V parabola correction voltage.

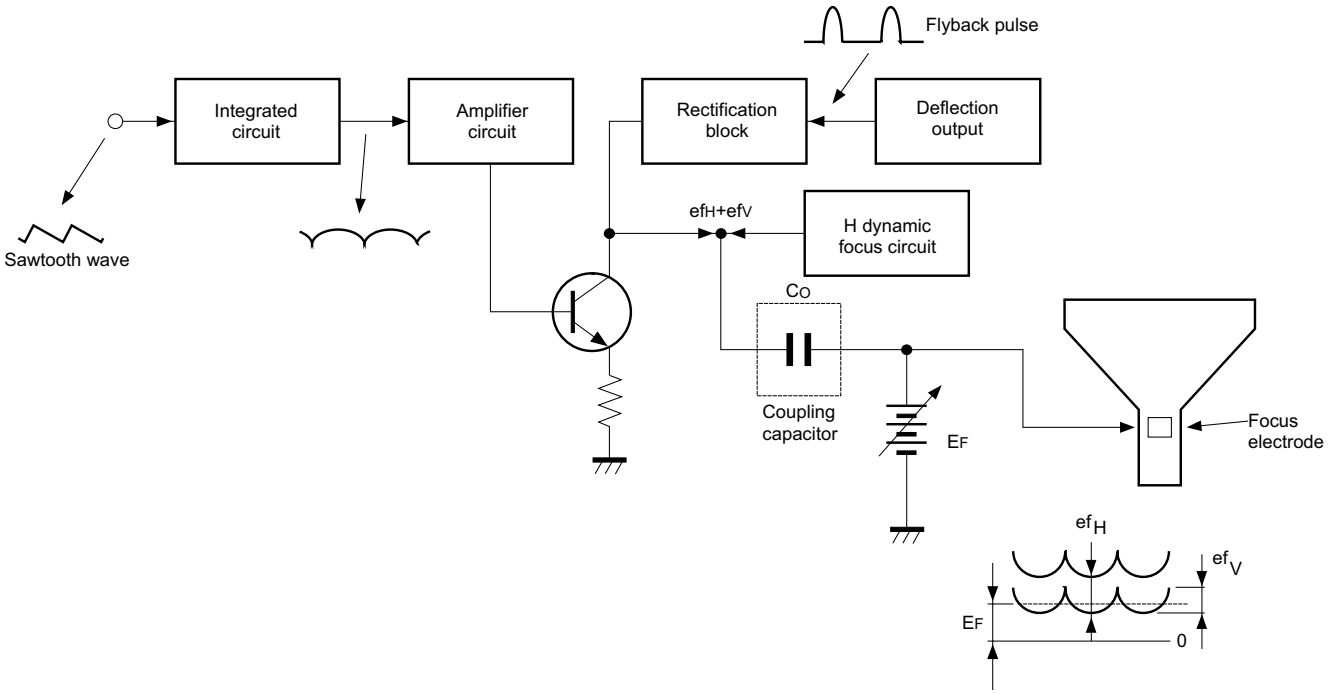


Fig. 18-3 Block diagram of V dyanamic focus circuit

3-2. Circuit Operation

A sawtooth wave voltage developed across (R305) in the V output circuit is cut in its DC component and the AC components of the voltage is integrated into a parabola form by a mirror integrator in the first stage and amplified with a specified gain level set by R362/R361. The amplified parabola wave enters an op. amplifier in the next stage and again amplified. The op. amplifier works as an inverting amplifier and the gain is determined by (R368/R369)/R366. The parabola voltage amplified in this way enters base of Q361, amplified in an inverted form, and developed as the V focus parabola voltage (300 Vp-p, DC component 60V). This voltage is mixed with the H focus parabola voltage in passing through R483, resulting in mixed parabora voltage consisting of a H component of 700 Vp-p and a V component of 300 Vp-p. Thus obtained mixed output is fed to the focus electrodes of R, G, B projection tubes through the coupling capacitor stated under 2-2.

The parabola level of the V focus parabola output voltage can be adjusted by varying R369 and the DC voltage level by varying R354.

The power for Q361 is obtained by rectifying collector pulse of the deflection output circuit with the rectification circuit Z470. The rectification circuit Z470 is assembled as a separate block in considering safety because of its high rectified output voltage of about 1000V.

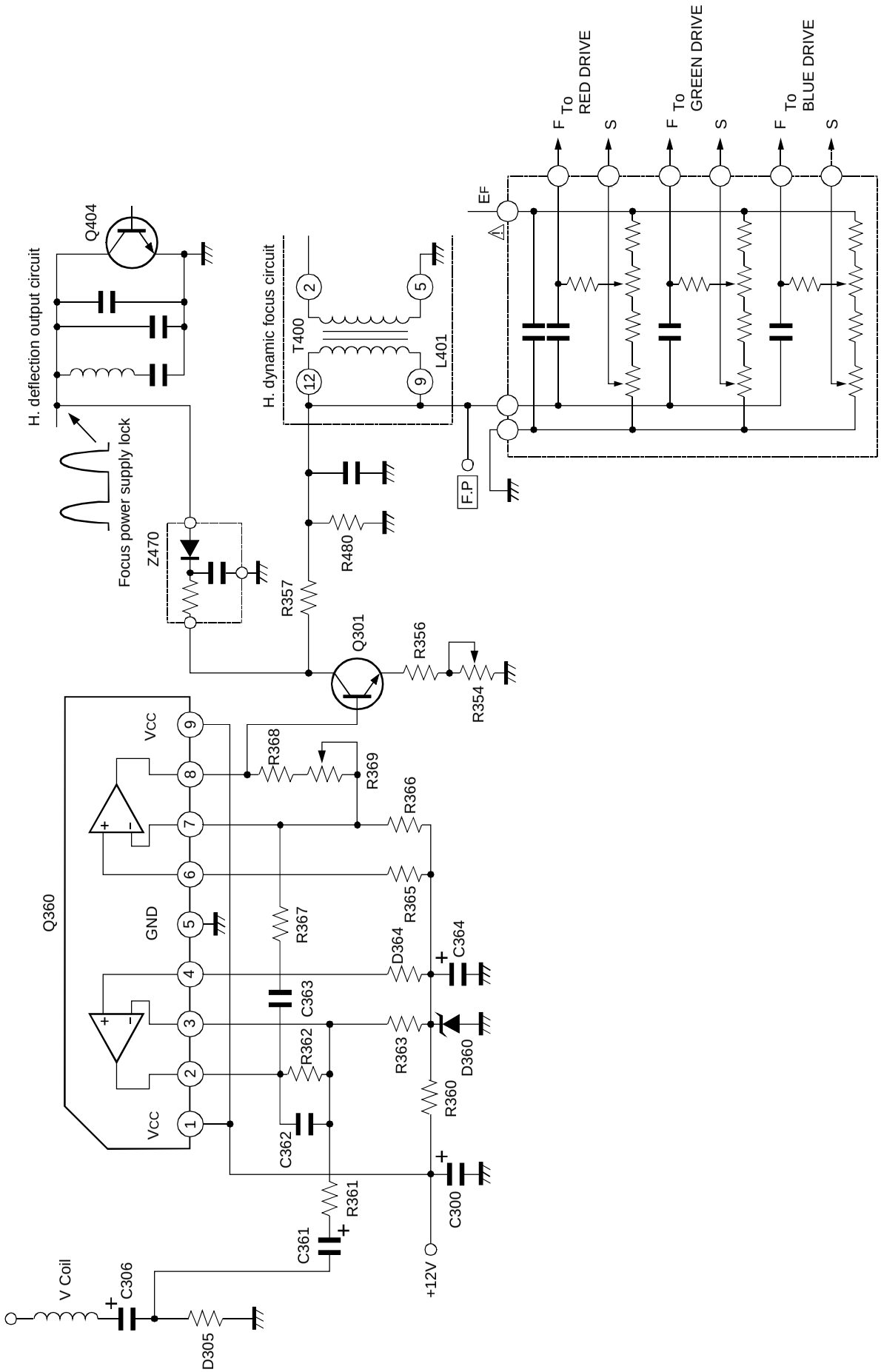


Fig. 18-4 V output circuit