42” Plasma Color Television
Model: PLA-4200M

Service Manual

Polaroid

Contents

Notice: This service manual is only read and used by professionals. The repairman should review the part of safety precaution before work.

1.Safety instruction

TO PREVENT POSSIBLE DANGER,DAMAGE, AND BODILY HARM, PLEASE CONSIDER AND OBSERVE ALL CAUTIONS CONTAINED IN THIS PARAGRAPH.

A.Warning

If you don't consider the following warning before maintenance, it could result in death or serious injury.

(1) The PDP module is controlled by voltage about 350V. If you need to handle the module during operation or just after power-off, you must take proper precautions against electric shock and never touch the drive circuit portion and metallic part of PDP module.

The capacitors in the drive circuit portion remain temporarily charged even after the power off. After turning off the power, you must be sure to wait at least one minute before touching the module. If the remainder of voltage is strong enough, it could result in electric shock.

(2) Do not use any other power supply voltage than the specified voltage in this product specifications. If you use deviated power voltage from the specifications, it could result in fire hazard or product failure.

(3) Do not operate or install under the deviated surrounding from the environmental specification such as in moisture or rain; near water-for example, bath tub, laundry tub, kitchen sink; in a wet basement; or near a swimming pool; and also near fire or heater for example, near or over radiator heat resistor; or where it is exposed to direct sunlight; or somewhere like that. If you use the PDP module in places above, it could result in electric shock, fire hazard or product failure.

(4) If any foreign objects (e.g. water, liquid and metallic chip or dust) entered the PDP module, the power supply voltage to the PDP module must be turned off immediately. Also never push objects of any kind into the PDP module as they may touch dangerous voltage point or make short circuits that could result in fire hazard or electric shock.

(5) If smoke, offensive smell or unusual noise should come from the PDP module, the power supply voltage to the PDP module must be turned off immediately.

Also, when the PDP screen cannot display any picture after the power-on or during operation, the power supply must be turned off immediately. Never continue to operate the PDP module under these conditions.

（6） Do not disconnect or connect the PDP module's connector while the power supply is on, or just after power off. Because the PDP module is operated by high voltage, and the capacitors in drive circuit remain temporarily changed even after the power is turned off. If you need to disconnect it, you have to wait at least one minute after power off.

（7）Do not disconnect or connect the power connector by wet hands. The voltage of the product may be strong enough to cause an electric shock..

（8） Do not damage the power cable of the PDP module, also do not modify it.
（９） When the power cable or connector is damaged or frayed, do not use it.
（１０）When the power connector is covered with dust, please wipe it with a dry cloth before the power on.

Ｂ． Caution

If you don’t consider the following cautions, it may result in personal injury or damage to the product.

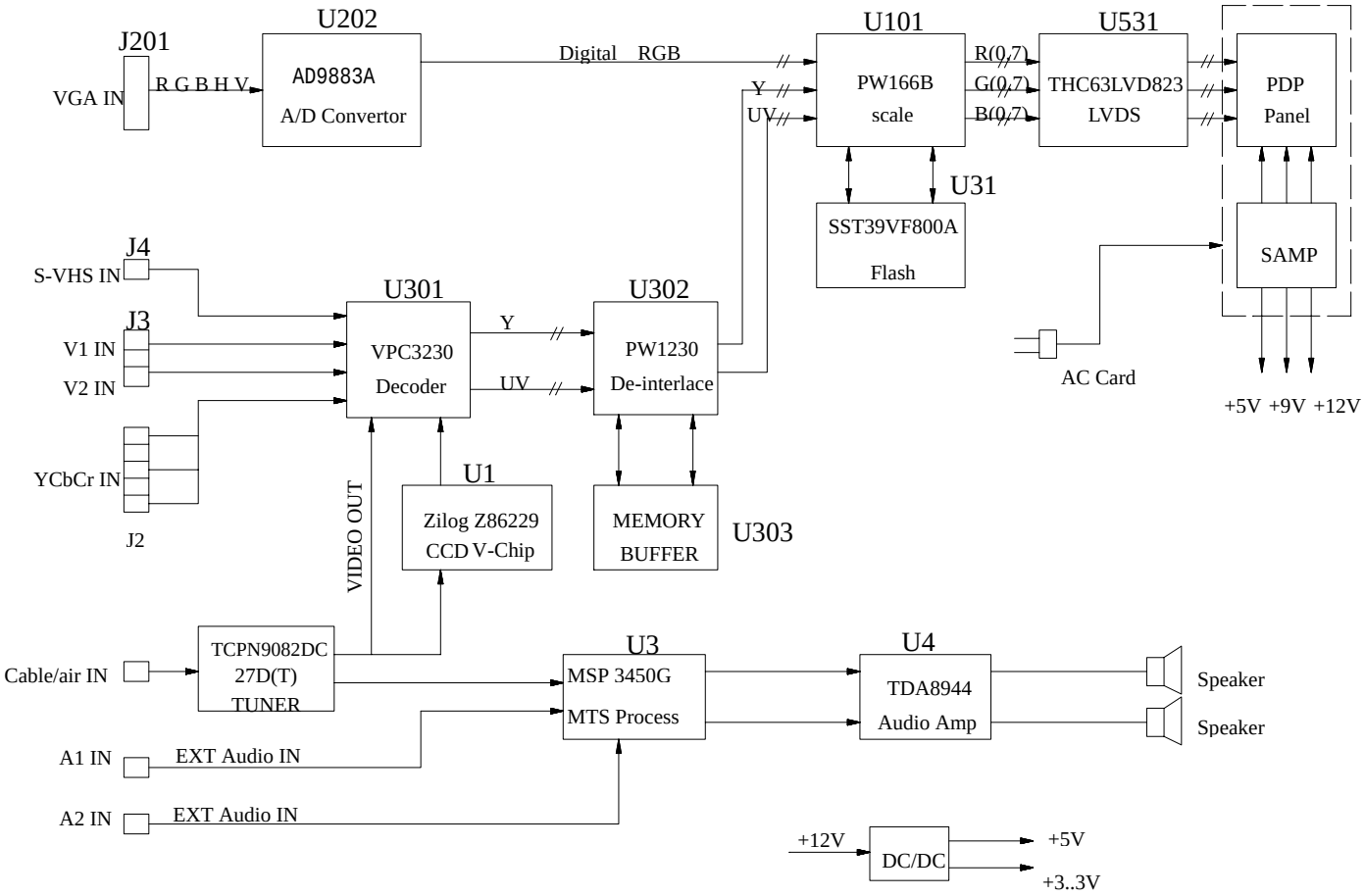
（１） Do not set the PDP module on an unstable place, vibrating place or inclined place. The PDP module may fall or drop, and it may cause serious injury to a person, and serious damage to the product.
（２） If you need to remove the PDP module to another place, you must turn off the power supply and detach the interface cable and power cable from the PDP module, and watch your steps during the work. If the cable has a damage, it may result in fire hazard or electric shock. Also if the PDP module drop or fall, it may result in personal injury.
（３） When you draw or insert the PDP’s cable, you must turn off the power supply and do it with holding the connector. If you draw the cable, the electric wire in the cable could be exposed or broken. It may result in fire hazard or electric shock.
（４） To carry the PDP module, it be done by two workers in order to avoid unexpected accidents.
（５） The PDP module has a glass-plate. If the PDP module is inflicted with excessive stress for example; shock, vibration, bending and heat-shock, the glass plate could break. It may result in personal injury. And also, do not press or strike the glass surface.
（６） If the glass plate was broken, do not touch it with bare hand. It may result in a cut injury.
（７） Do not place any object on the glass plate. It may scratch or break the glass plate.
（８） Do not place any object on the PDP module. It may result in personal injury due to its fall or drop.

2.Specifications

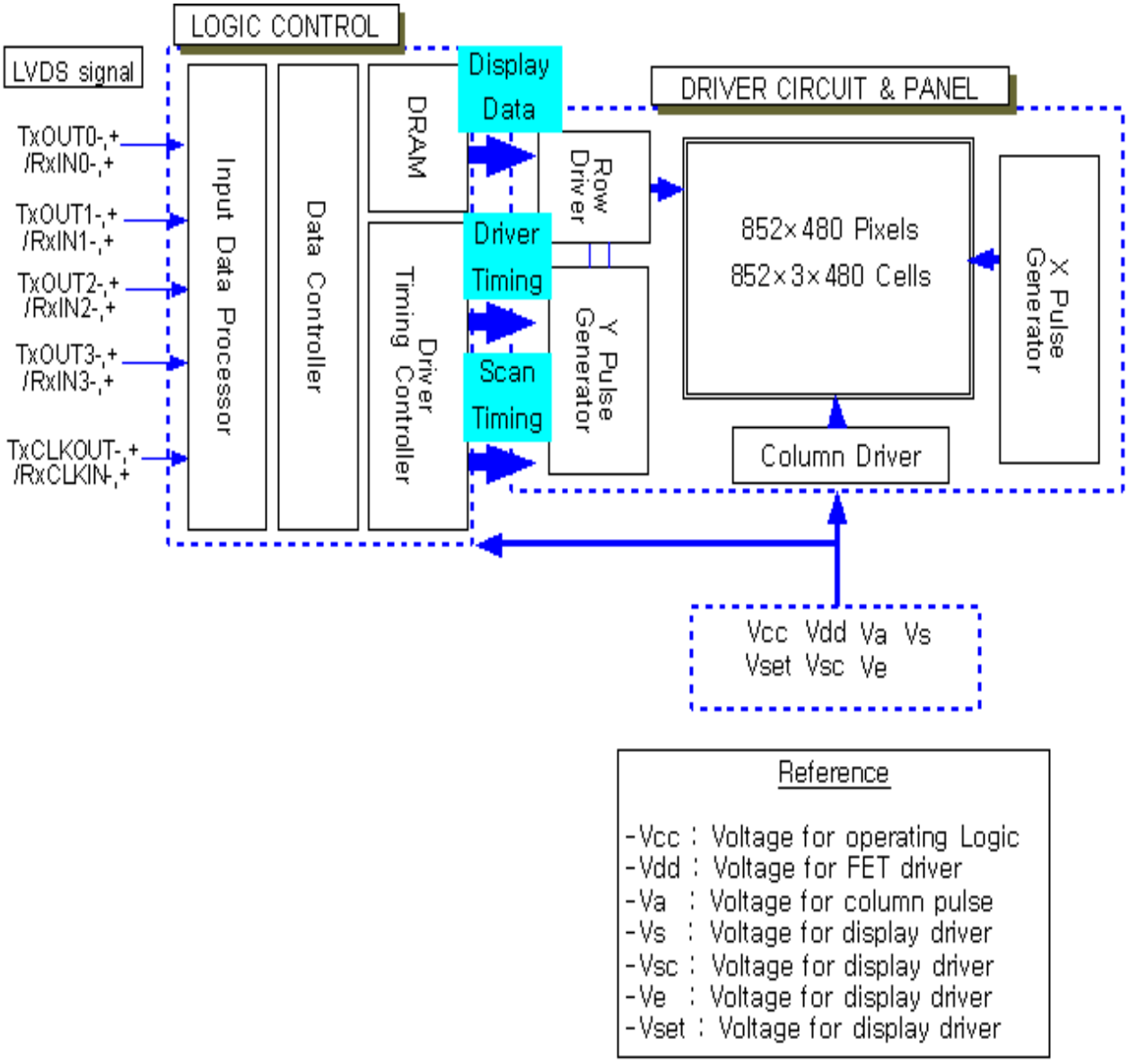
Type	PLA-4200M
System of the broadcasting	NTSC-M
System of the video signal	PAL/NTSC/SECAM
Number of stored programs	125
Scope of the channel	Air: CH2 to CH69, Cable: CATV1 to CATV125
Signal intensity	70dB
Audio input	Input impedance>10kΩ, Input voltage 0.1-0.5 V(rms)
Speaker output	2*5W
Visual angle (Max)	160°
Resolution	852*480
Power supply	AC 100V-240V (50Hz/60Hz)
Energy consumption	350W(typ).3W (stand by)
Dimensions (W*H*D)	46.1*29.1*5.2 inch
Size of screen	42 inch
Aspect ration	16:9
Weight	110 lb.
Ambient temperature	0-35℃
Ambient humidity	20%-70%RH
Ambient air pressure	86-106Kpa

3.Signal processing and system block diagram

A. Image signal processing block diagram



B. PDP DISPLAY SCREEN BLOCK DIAGRAM



4.Part list

Part Number	Description	Qty.
SPW5.069.166	Polaroid PLA-4200M YPbPr Circuit Board	1
SPW5.969.003	Polaroid PLA-4200M Remote Control Circuit Board	1
A920008	Polaroid PLA-4200M Zinnia PDP Control Circuit Board	1
B135011	Polaroid PLA-4200M 5W-8Ω Speaker	8
SPW8.339.008	Polaroid PLA-4200M Main Power Button	1
E143221JF	Polaroid PLA-4200M Tapping Screw ST3*8F	2
E143222JH	Polaroid PLA-4200M Tapping Screw ST3*8 (black)	6
E143461	Polaroid PLA-4200M Tapping Screw ST4*16	16
E143463	Polaroid PLA-4200M Tapping Screw ST4*16 (black)	6
E144231	Polaroid PLA-4200M Tapping Screw ST3*10	30
E144431	Polaroid PLA-4200M Tapping Screw ST4*10	3
E690220	Polaroid PLA-4200M SEMS Screw M3*8	16
E690221	Polaroid PLA-4200M SEMS Screw M3*8 (black)	6
E690223	Polaroid PLA-4200M SEMS Screw M3*8 (black)	15
E690230	Polaroid PLA-4200M SEMS Screw M3*10	2
E690420	Polaroid PLA-4200M SEMS Screw M4*8	14
E690660	Polaroid PLA-4200M SEMS Screw M6*16 (black)	10
E690670	Polaroid PLA-4200M SEMS Screw M6*20 (black)	4
S070183	Polaroid PLA-4200M Power Switch KDC-A04-1	1
G330170	Polaroid PLA-4200M Remote Control	1

4.Part list

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4.Part list

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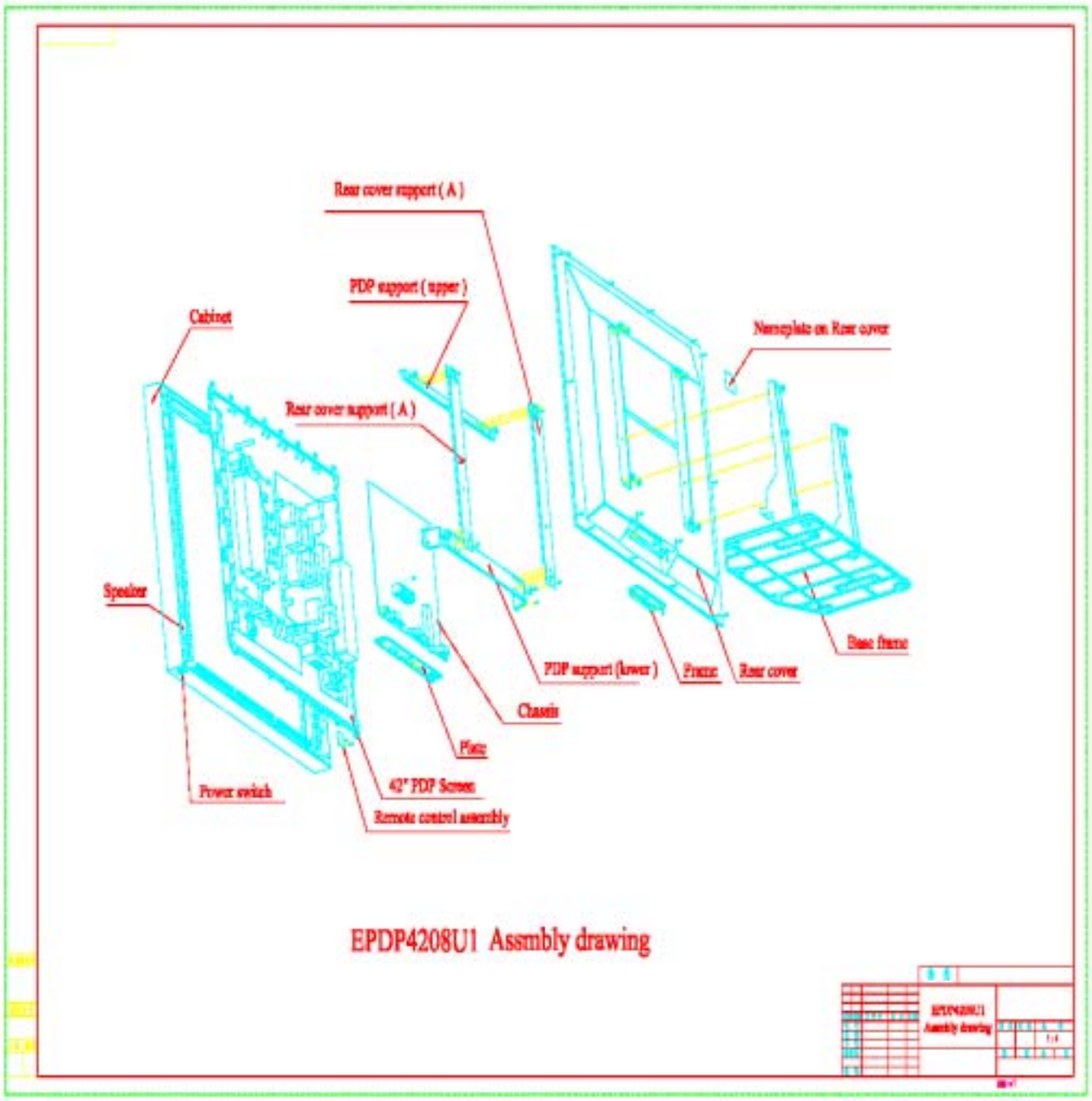
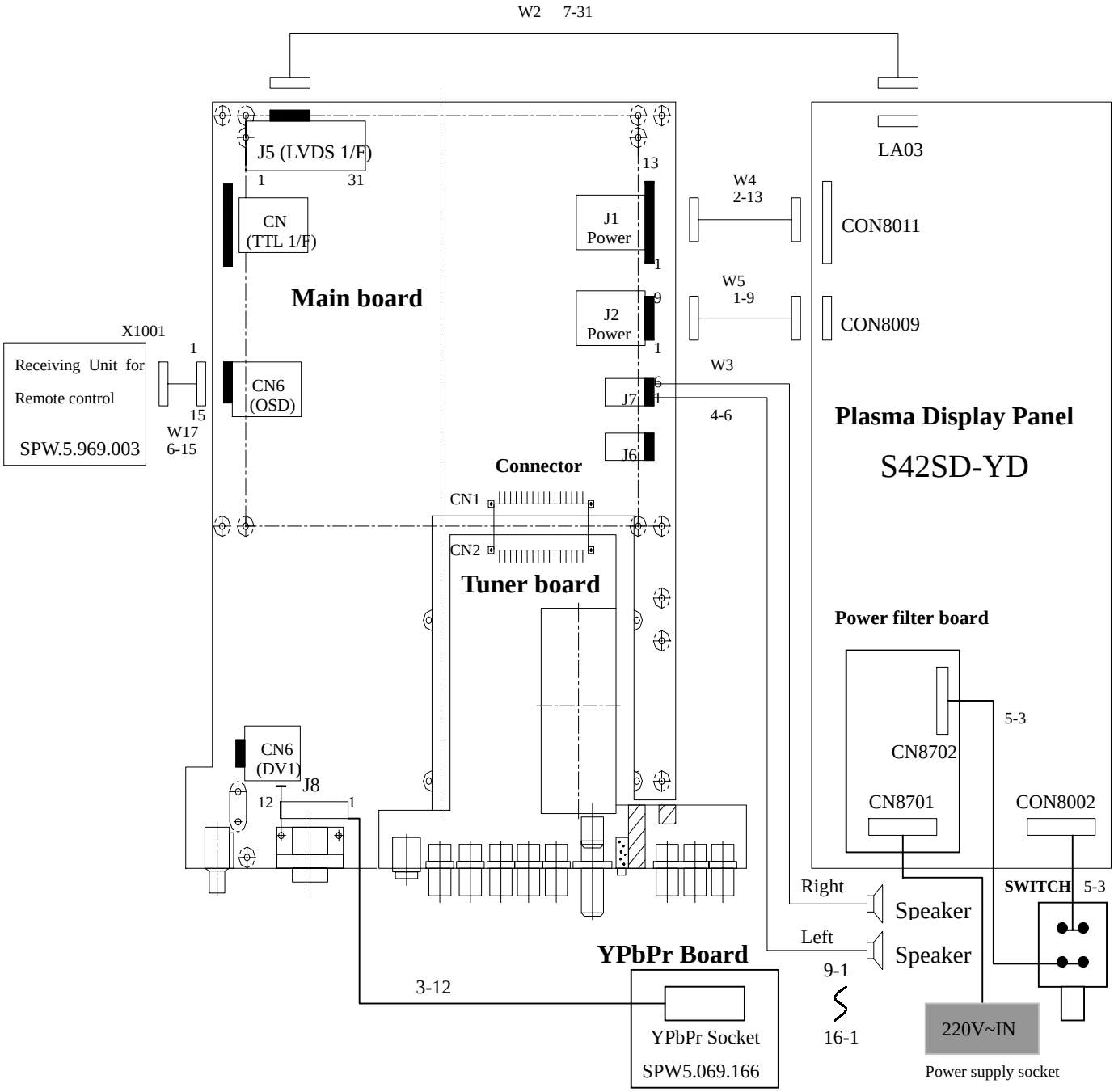
5.General assembly drawing



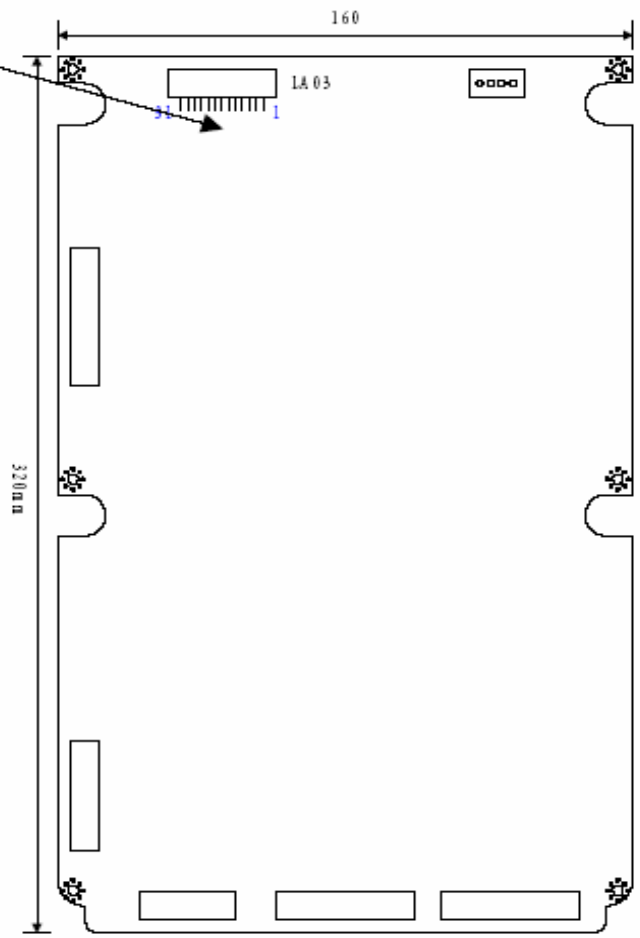
6.General connection diagram



A. Specifications for the data signal of Plasma display panel

Input signal name and Pin assignment

Pin No.	Pin Name(LA03)
1	GND
2	GND
3	TxOUT0-/RxIN0-
4	TxOUT0+/RxIN0+
5	GND
6	GND
7	TxOUT1-/RxIN1-
8	TxOUT1+/RxIN1+
9	GND
10	GND
11	TxOUT2-/RxIN2-
12	TxOUT2+/RxIN2+
13	GND
14	GND
15	TxCLKOUT-/RxCLKIN-
16	TxCLKOUT+/RxCLKIN+
17	GND
18	GND
19	TxOUT3-/RxIN3-
20	TxOUT3+/RxIN3+
21	GND
22	GND
23	GND
24	GND
25	NC
26	GND
27	NC
28	GND
29	NC
30	GND
31	NC



B. Input Power Voltage Source and Pin Assignment

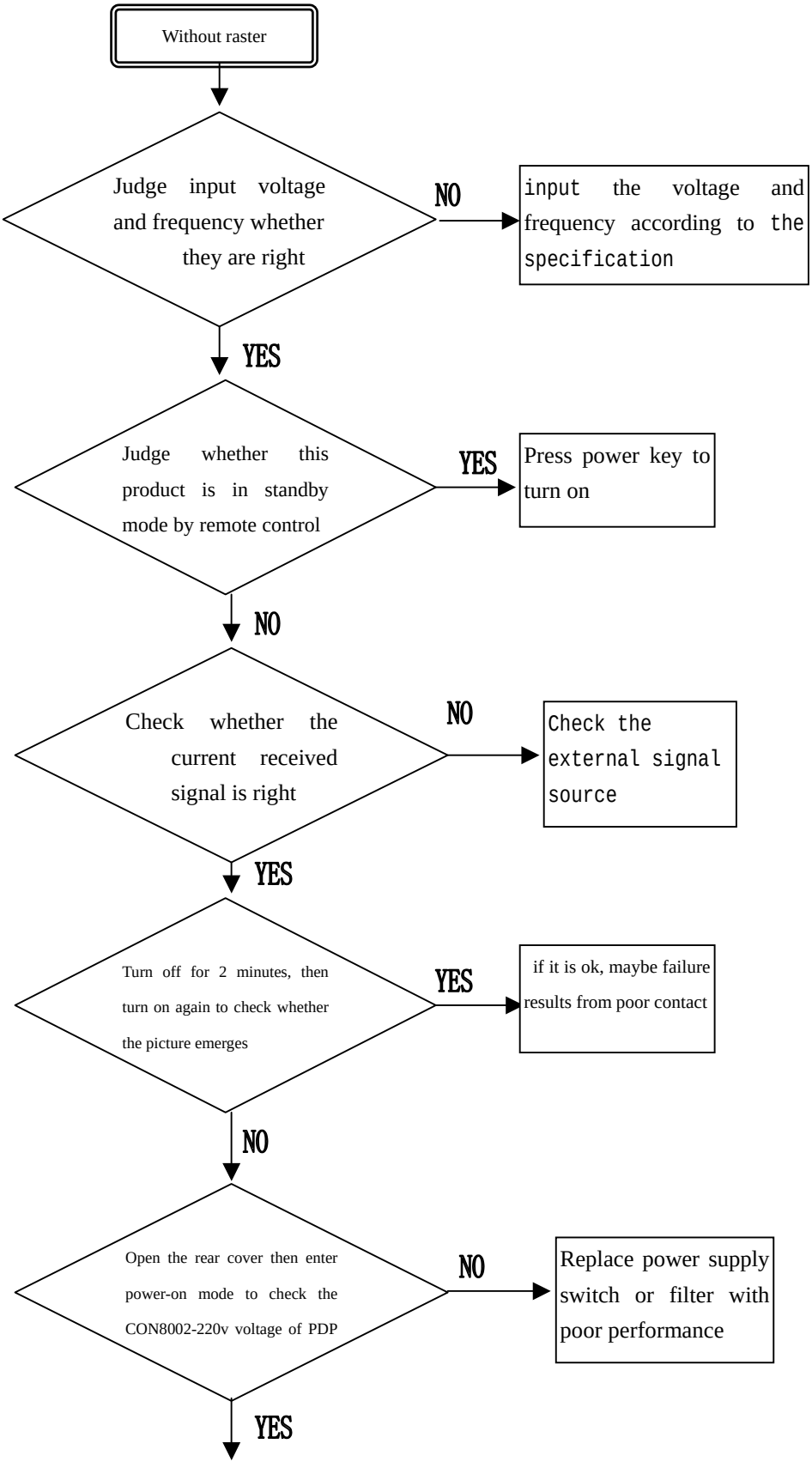
Connector Name: SA→J1(W4)		
to The Image Board		
Pin no	Voltage Source	Usage
1	5Vsb	Vcc5-SB-PDP
2	GND	GND
3	GND-D	GND
4	B5d1	NC
5	RELAY	PDP-RELAY
6	TH-DET	NC
7	FAN-DET	NC
8	GND-A	GND
9	GND-A	GND
10	NC	NC
11	V12A	NC
12	V5a	Vcc5-PDP
13	NC	NC

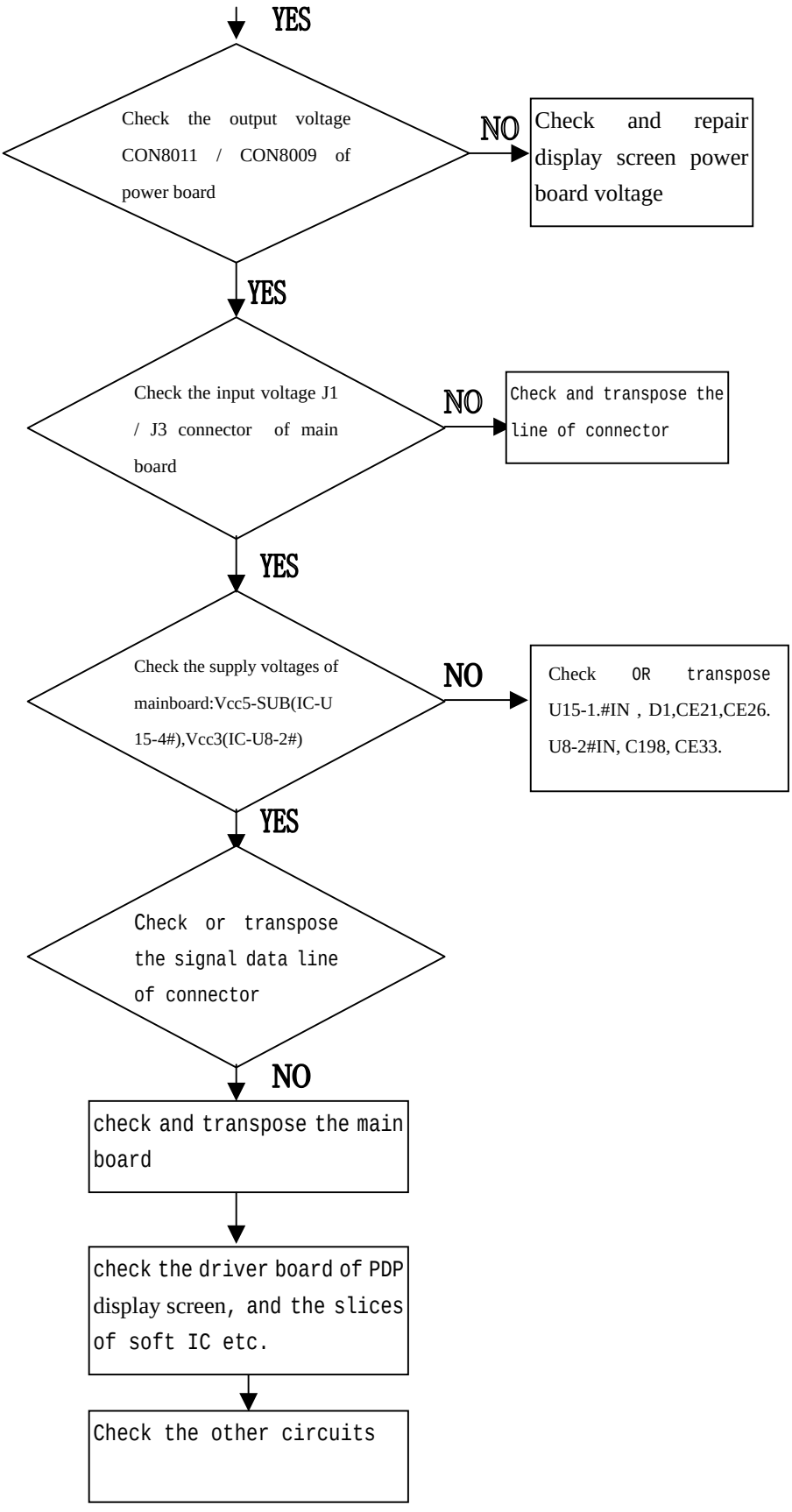
Connector Name: AUDIO→J2(W5)		
to The Audio Amp Board		
Pin no	Voltage Source	Usage
1	V5A	Vcc5-PDP
2	GND-A	GND
3	12VCC	Vcc12-FAN
4	V9A	Vcc9-PDP
5	GND-A	GND
6	24Vsp	Vcc12-AUD-PDP
7	24Vsp	Vcc12-AUD-PDP
8	GNDS	GND-AUD
9	GNDS	GND-AUD

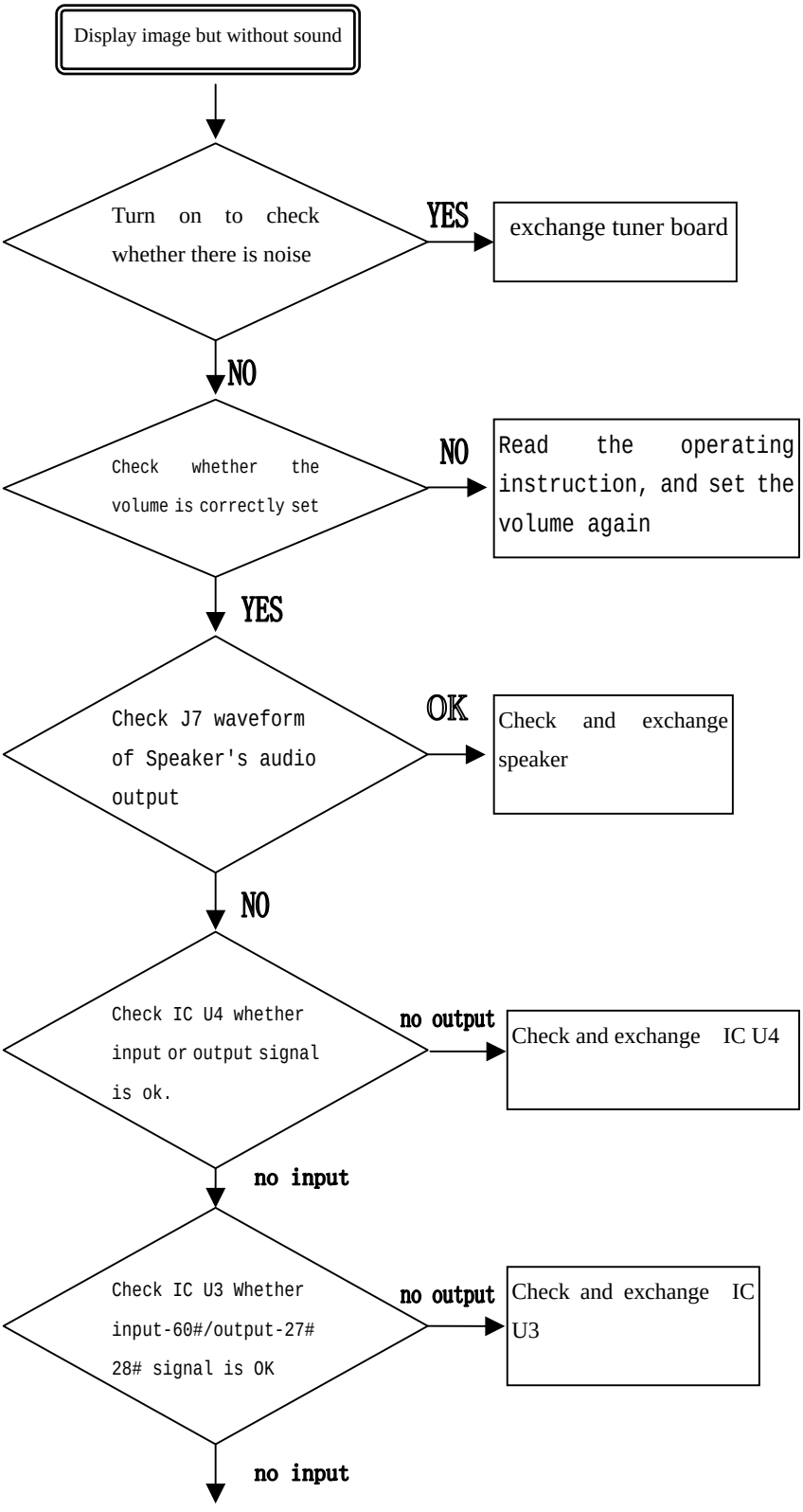
Connector Name: OSD(W17)	
Pin no	Usage
1	Vcc5
2	KPAD0
3	KPAD1
4	KPAD2
5	KPAD3
6	LED-RED
7	LED-GREEN
8	Vcc5-SB
9	GND
10	POWER-SW
11	IR
12	KPAD4
13	KPAD5
14	KPAD6
15	KPAD7

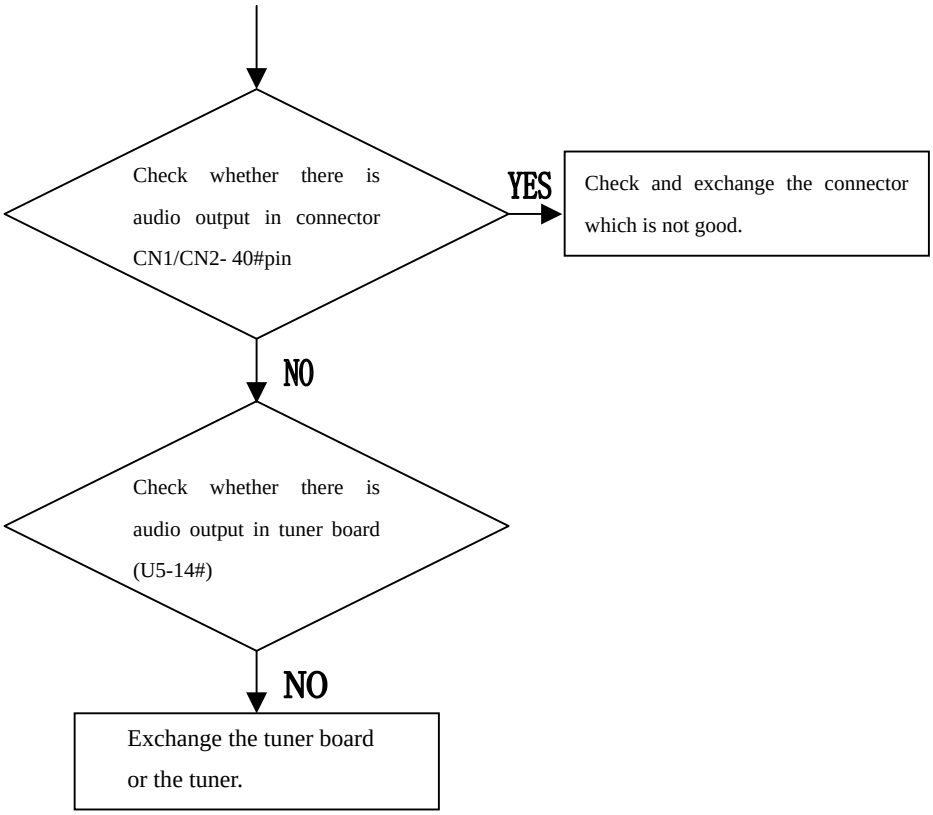
Connector Name: SPEAKER(W3)	
Pin no	Usage
1	SPEAKER-SW
2	SPK-OUT1-
3	SPK-OUT1+
4	GND
5	SPK-OUT2-
6	SPK-OUT2+

7.Failures analysis




YES
Check the output voltage CON8011 / CON8009 of power board
NO
Check and repair display screen power board voltage
YES
Check the input voltage J1 / J3 connector of main board
NO
Check and transpose the line of connector
YES
Check the supply voltages of mainboard:Vcc5-SUB(IC-U 15-4#),Vcc3(IC-U8-2#)
NO
Check OR transpose U15-1.#IN , D1,CE21,CE26. U8-2#IN, C198, CE33.
YES
Check or transpose the signal data line of connector
NO
check and transpose the main board
check the driver board of PDP display screen, and the slices of soft IC etc.
Check the other circuits


Display image but without sound
Turn on to check whether there is noise
YES
exchange tuner board
NO
Check whether the volume is correctly set
NO
Read the operating instruction, and set the volume again
YES
Check J7 waveform of Speaker's audio output
OK
Check and exchange speaker
NO
Check IC U4 whether input or output signal is ok.
no output
Check and exchange IC U4
no input
Check IC U3 Whether input-60#/output-27# 28# signal is OK
no output
Check and exchange IC U3
no input


Check whether there is audio output in connector CN1/CN2- 40#pin
YES
Check and exchange the connector which is not good.
NO
Check whether there is audio output in tuner board (U5-14#)
NO
Exchange the tuner board or the tuner.

8.Description of main ICs and components

(1) M52790SP/FP

AV SWITCH with I^2C BUS CONTROL

DESCRIPTION

The M52790 is AV switch semiconductor integrated circuit with I^2C bus control .

This IC contains 2-channels of 4-input audio switches and 2-channels of 4-input video switches. Each channel can be controled independently .

The video switches contain amplifiers can be controled a gain of

output 0dB or 6dB .

FEATURES

•Video and stereo sound switches in one package

•Wide frequency range (video switch) DC-20MHz

•High separation (video switch).....Crosstalk -60dB (typ.) at 1MHz

•Two types of packages are provided : SDIP with a lead pitch of 1.778mm (M52790SP) ; and SSOP with a lead pitch of 0.8mm (M52790FP) .

APPLICATION

Video equipment

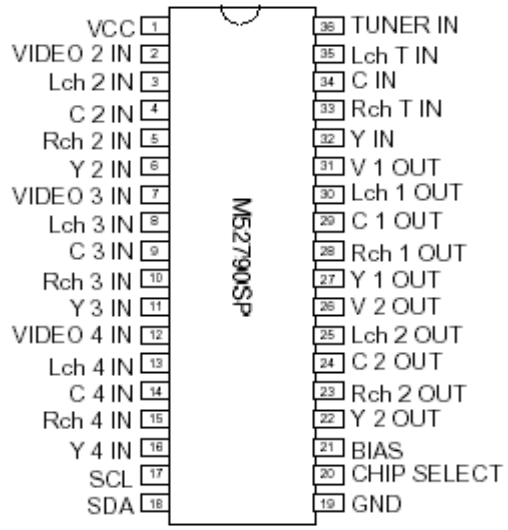
RECOMMENDED OPERATING CONDITION

Supply voltage 4.7V ~ 9.3V

Rated supply voltage 5V,9V

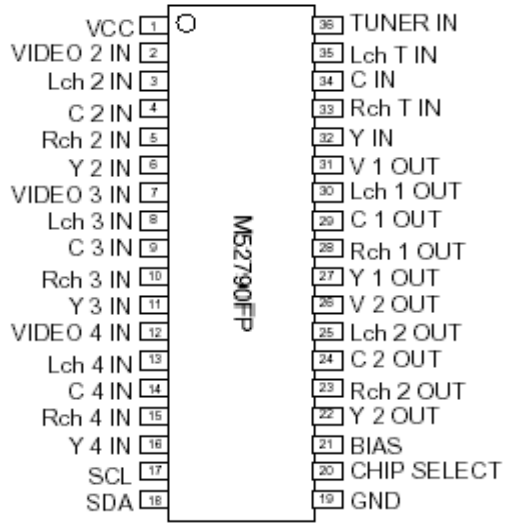
Maximum output current 63mA(at 9V)

PIN CONFIGURATION (TOP VIEW)



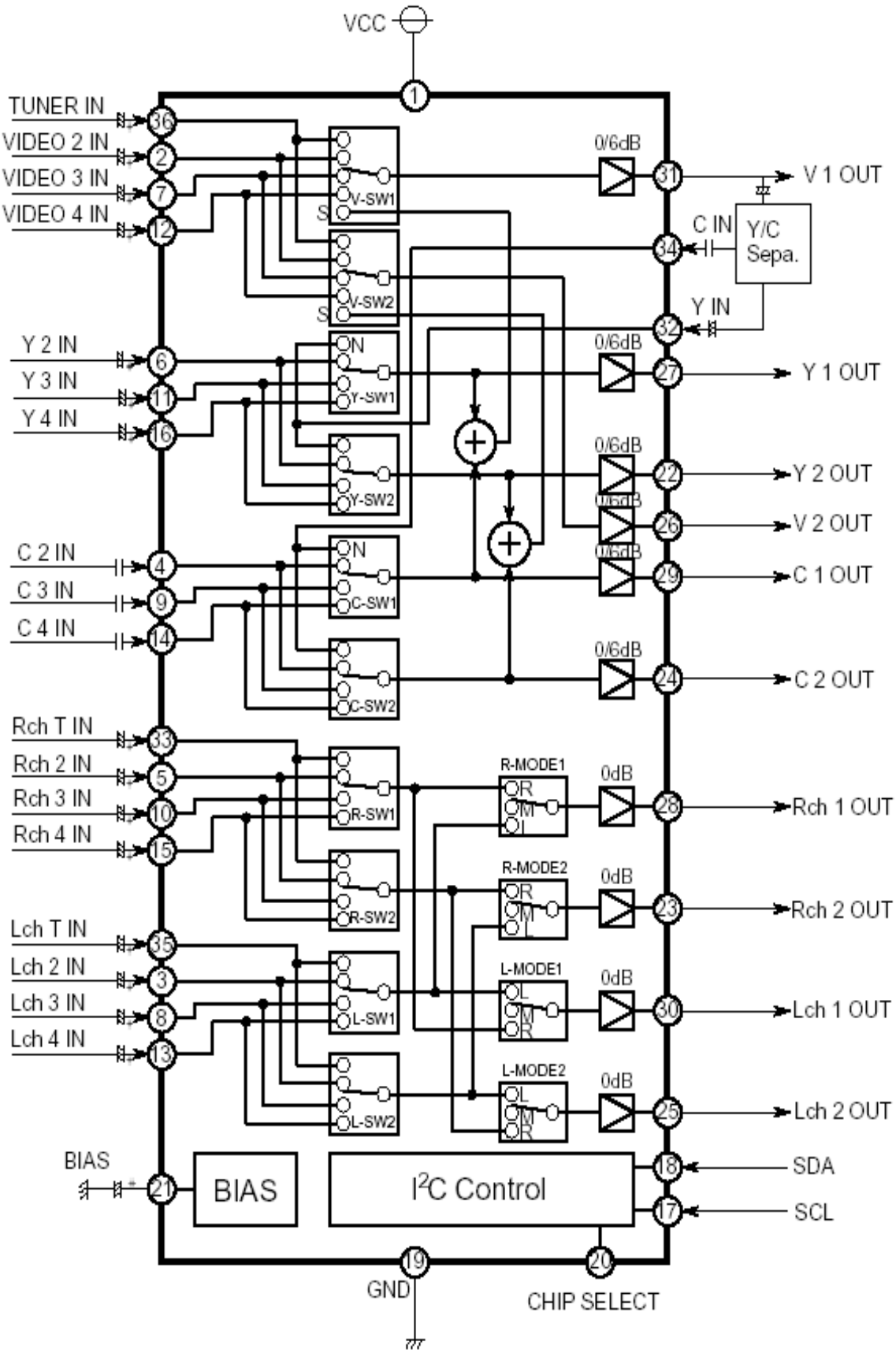
Outline 36P4E
(Lead pitch :1.778mm)

PIN CONFIGURATION (TOP VIEW)



Outline 36P2R-D
(Lead pitch :0.8mm)

BLOCK DIAGRAM



(2) MSP3450G

Multistandard Sound Processor Family

Release Note: Revision bars indicate significant changes to the previous edition. The hardware and software description in this document is valid for the MSP 3450G version B5 and following versions.

Introduction

The MSP 3450G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip. Figure4 shows a simplified functional block diagram of the MSP 3450G.

This new generation of TV sound processing ICs now includes versions for processing the multichannel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, MICRONAS Noise Reduction (MNR) is performed alignment free.

Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard.

Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J. The MSP 3450G has optimum stereo performance without any adjustments.

All MSP 3450G versions are pin and software downward-compatible to the MSP 3450D. The MSP 34x0G further simplifies controlling software. Standard selection requires a single I2C transmission only.

The MSP 34x0G has built-in automatic functions: The IC is able to detect the actual sound standard automatically (Automatic Standard Detection). Furthermore, pilot levels and identification signals can be evaluated internally with subsequent switching between mono/ stereo/bilingual; no I2C interaction is necessary (Automatic Sound Selection).

The ICs are produced in submicron CMOS technology. The MSP 34x0G is available in the following packages: PLCC68, PSDIP64, PSDIP52, PQFP80, and PLQFP64.

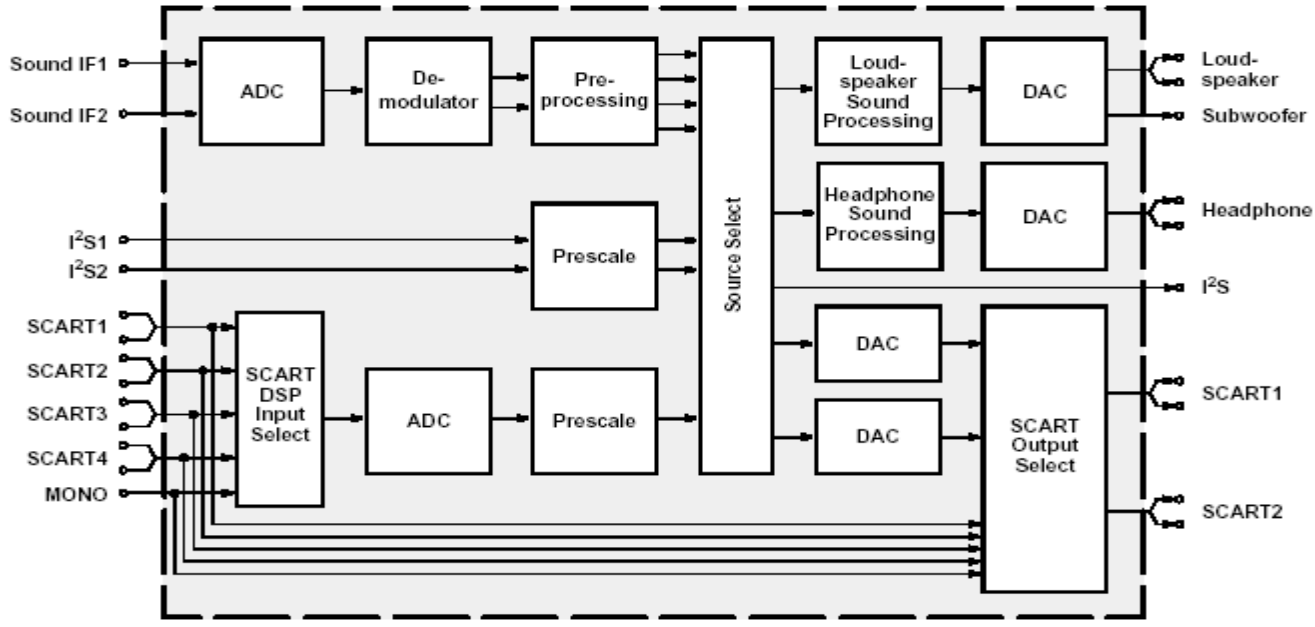


Fig. 4: Simplified functional block diagram of the MSP 3450G

(3) VPC323OD

PRELIMINARY DATA SHEET

Comb Filter Video Processor

Introduction

The VPC 3230D is a high-quality, single-chip video front-end, which is targeted for 4:3 and 16:9, 50/60-Hz and 100/120 Hz TV sets. It can be combined with other members of the DIGIT3000 IC family (such as DDP 331x) and/or it can be used with 3rd-party products.

The main features of the VPC 3230D are

– high-performance adaptive 4H comb filter Y/C separator with adjustable vertical peaking
– multi-standard color decoder PAL/NTSC/SECAM including all substandards
– four CVBS, one S-VHS input, one CVBS output
– two RGB/YC_rC_b component inputs, one Fast Blank (FB) input
– integrated high-quality A/D converters and associated clamp and AGC circuits
– multi-standard sync processing
– linear horizontal scaling (0.25 ... 4), as well as non-linear horizontal scaling ‘Panoramavision’
– PAL+ preprocessing
– line-locked clock, data and sync, or 656-output interface
– peaking, contrast, brightness, color saturation and tint for RGB/YC_rC_b and CVBS/S-VHS
– high-quality soft mixer controlled by Fast Blank
– PIP processing for four picture sizes (1/4,1/9,1/16, or1/36 of normal size) with 8-bit resolution
– 15 predefined PIP display configurations and expert mode (fully programmable)
– control interface for external field memory
– I^2C-bus interface
– one 20.25-MHz crystal, few external components
– 80-pin PQFP package

System Architecture

Fig.5 shows the block diagram of the video processor

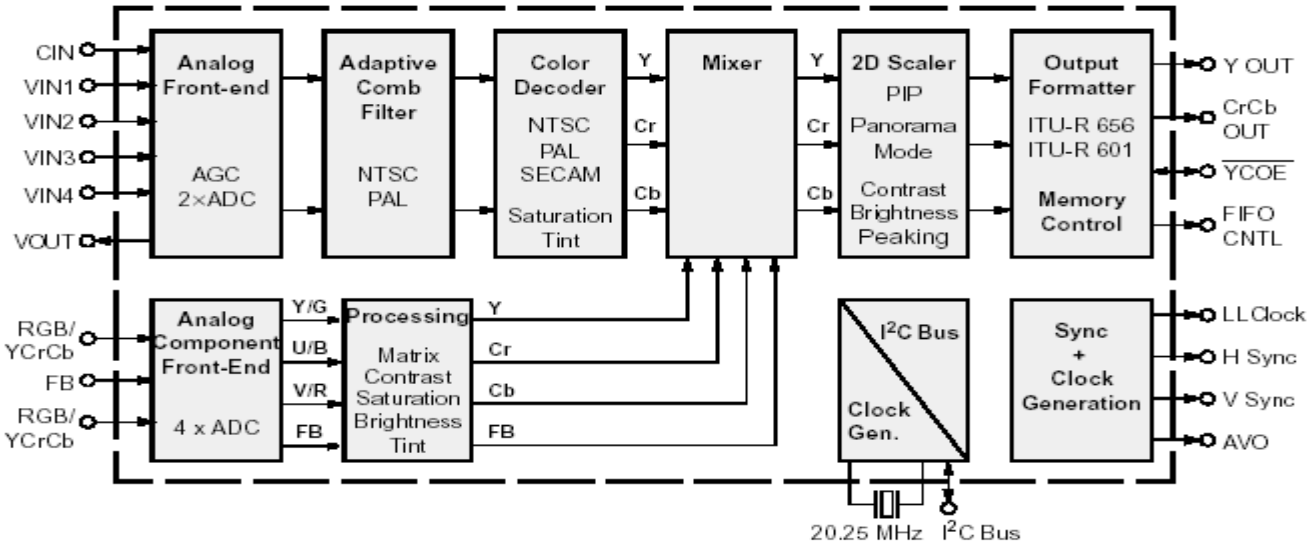


Fig. 5: Block diagram of the VPC 3230D

Pin Configuration

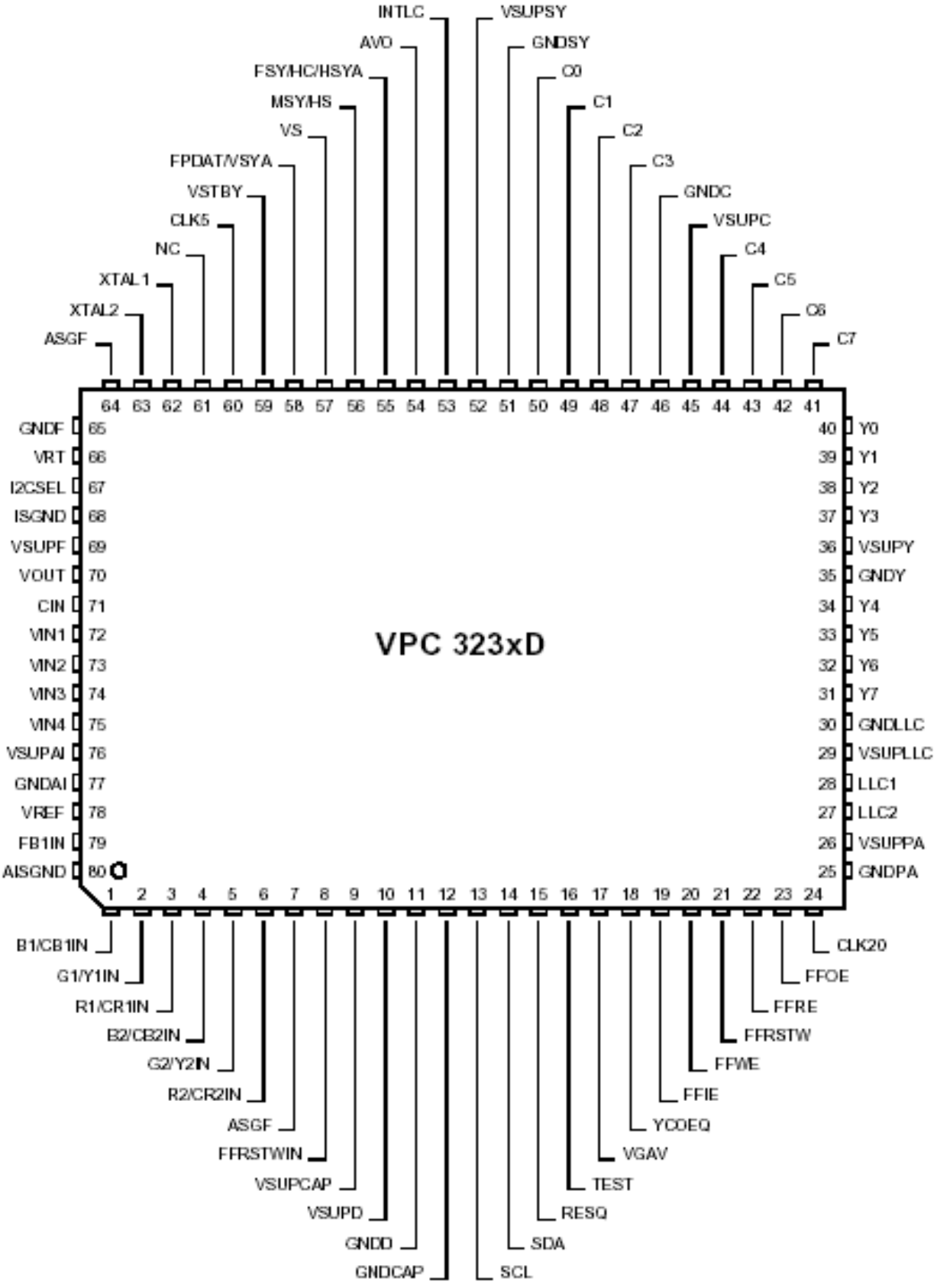


Fig.6: 80-pin PQFP package

(4) Z86229

NTSC LINE 21 CCD DECODER

FEATURES

Devices	Speed (MHz)	Pin Count/ Package Types	Standard Temp. Range	On-Screen Display & Closed Captioning	Automatic Data Extraction: Program Rating	Automatic Data Extraction: Time of Day
Z86229	12	18-Pin DIP, SOIC	0°C to +70°C	Yes	Yes	Yes

- Complete Stand-Alone Line 21 Decoder for Closed-Captioned and Extended Data Services (XDS)
- Preprogrammed to Provide Full Compliance with EIA–608 Specifications for Extended Data Services
- Automatic Extraction and Serial Output of Special XDS Packets (Time of Day, Local Time Zone, and Program Blocking)
- Programmable XDS Filter for a Specific XDS Packet
- Cost-Effective Solution for NTSC Violence Blocking inside Picture-in-Picture (PiP) Windows
- Minimal Communications and Control Overhead Provide Simple Implementation of Violence Blocking, Closed Captioning, and Auto Clock Set Features
- Programmable, On-Screen Display (OSD) for Creating Full Screen OSD or Captions inside a Picture-in-Picture (PiP) Window
- User-Programmable Horizontal Display Position for easy OSD Centering and Adjustment
- I^2C Serial Data and Control Communication
- Supports 2 Selectable I^2C Addresses

GENERAL DESCRIPTION

Capable of processing Vertical Blanking Interval (VBI) data from both fields of the video frame in data, the Z86229 Line 21 Decoder offers a feature-rich solution for any television or set-top application. The robust nature of the Z86229 helps the device conformto the transmission format defined in the Television Decoder Circuits Act of 1990, and in accordance with the Electronics Industry Association specification 608 (EIA–608).

The Line 21 data streamcan consistof data fromseveral data channels multiplexed together. Field 1 consists of four data channels: two Captions and two Texts. Field 2 consists of five additional data channels: two Captions, two Texts, and Extended Data Services (XDS). The XDS data structure is defined in EIA–608. The Z86229 can recover and display data transmitted on any of these nine data channels.

The Z86229 can recover and output to a host processor via the I2C serial bus. The recovered XDS data packet is further defined in the EIA–608 specification. The on-chip XDS filters in the Z86229 are fully programmable, enabling recovery of only thoseXDSdata packets selected by the user. This functionality allows the device to extract the required XDS information with proper XDS filter setup for compatibility in a variety of TVs, VCRs, and Set-Top boxes.

In addition, the Z86229 is ideally suited to monitor Line 21 video displayed in a PiP window for violence blocking, CCD, and other XDS data services.

PIN DESCRIPTION

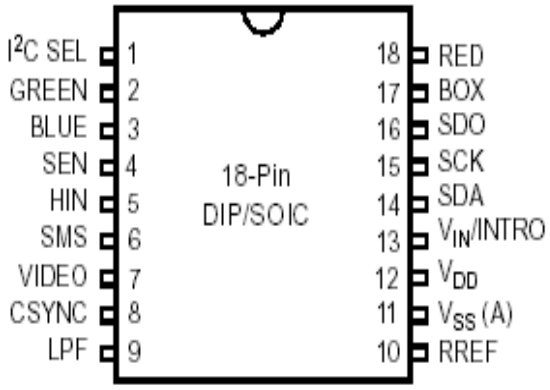


Figure 2. Z86229 Pin Configuration

Table 1. Z86229 Pin Identification*

No.	Symbol	Function	Direction
1	I^2C SEL	I^2C Address Selection	Input
2	GREEN	Video Output	Output
3	BLUE	Video Output	Output
4	SEN	Serial Enable	Input
5	HIN	Horizontal In	Input
6	SMS	Serial Mode Select	Input
7	VIDEO	Composite Video	Input
8	CSYNC	Composite Sync	Output
9	LPF	Loop Filter	Output
10	RREF	Resistor Reference	Input
11	V_{SS} (A)	Pwr. Supply (Analog) GND	
12	V_{DD}	Power Supply	
13	V_{IN}/INTRO	Vertical In/Interrupt Out	In/Output
14	SDA	Serial Data	In/Output
15	SCK	Serial Clock	Input
16	SDO	Serial Data Out	Output
17	BOX	OSD Timing Signal	Output
18	RED	Video Output	Output

Note: *DIP and SOIC pin configurations are identical.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	–0.5 to 6.0	V
V_{IN}	DC Input Voltage	–0.5 to V_{DD} +0.5	V
V_{OUT}	DC Output Voltage	–0.5 to V_{DD} +0.5	V
I_{IN}	DC Input Current per Pin	+10	mA
I_{OUT}	DC Output Current per Pin	+20	mA
I_{DD}	DC Supply Current	+30	mA
P_D	Power Dissipation per Device	300	mW
T_{STG}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

Notes:
*Voltages referenced to V_{SS} (A). Values beyond the maximum ratings listed above may cause damage to the device. Functional operation should be restricted to the limits specified in the DC and AC Characteristics tables or Pin Description section.

(5) HY57V641620HG

DRAM

DESCRIPTION

The Hynix HY57V641620HG is a 67,108,864-bit CMOS Synchronous DRAM, ideally suited for the Mobile applications r which require low power consumption and extended temperature range. HY57V641620HG is organized as 4banks of 1,048,576x16.

HY57V641620HG is offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTL.

Programmable options include the length of pipeline (Read latency of 2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or Full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipelined design is not restricted by a `2N` rule.)

FEATURES

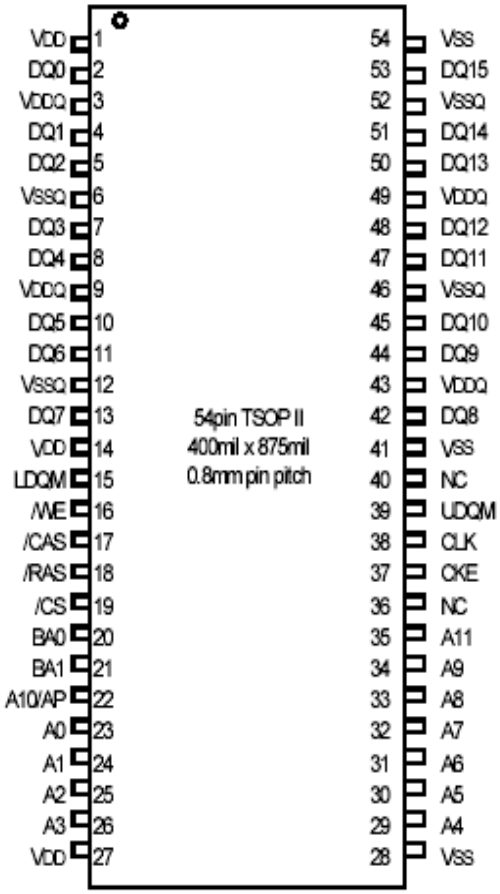
- Single 3.3±0.3V power supply Note)
- All device pins are compatible with LVTTL interface
- JEDEC standard 400mil 54pin TSOP-II with 0.8mm of pin pitch
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by UDQM or LDQM
- Internal four banks operation
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 or Full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Programmable $\overline{CAS}$ Latency ; 2, 3 Clocks

ORDERING INFORMATION

Part No.	Clock Frequency	Power	Organization	Interface	Package
HY57V641620HGT-5I/55I/6I/7I	200/183/166/143MHz	Normal	4Banks x 1Mbits x16	LVTTL	400mil 54pin TSOP II
HY57V641620HGT-KI	133MHz				
HY57V641620HGT-HI	133MHz				
HY57V641620HGT-8I	125MHz				
HY57V641620HGT-PI	100MHz				
HY57V641620HGT-SI	100MHz				
HY57V641620HGLT-5I/55I/6I/7I	200/183/166/143MHz	Low power			
HY57V641620HGLT-KI	133MHz				
HY57V641620HGLT-HI	133MHz				
HY57V641620HGLT-8I	125MHz				
HY57V641620HGLT-PI	100MHz				
HY57V641620HGLT-SI	100MHz				

Note : VDD(Min) of HY57V641620HG(L)T-5I/55I/6I is 3.135V

PIN CONFIGURATION



PIN DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
$\overline{CS}$	Chip Select	Enables or disables all inputs except CLK, CKE and DQM
BA0,BA1	Bank Address	Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during $\overline{CAS}$ activity
A0 ~ A11	Address	Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
LDQM, UDQM	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ15	Data Input/Output	Multiplexed data input / output pin
VDD/VSS	Power Supply/Ground	Power supply for internal circuits and input buffers
VDDQ/VSSQ	Data Output Power/Ground	Power supply for output buffers
NC	No Connection	No connection

(6) TDA8944J

STEREO AUDIO AMPLIFIER

1. General description

The TDA8944J is a dual-channel audio power amplifier with an output power of 2 × 7 W at an 8 Ω load and a 12 V supply. The circuit contains two Bridge Tied Load (BTL) amplifiers with an all-NPN output stage and standby/mute logic. The TDA8944J comes in a 17-pin DIL-bent-SIL (DBS) power package. The TDA8944J is printed-circuit board (PCB) compatible with all other types in the TDA894x family. One PCB footprint accommodates both the mono and the stereo products.

2. Features

- Few external components
- Fixed gain
- Standby and mute mode
- No on/off switching plops
- Low standby current
- High supply voltage ripple rejection
- Outputs short-circuit protected to ground, supply and across the load
- Thermally protected
- Printed-circuit board compatible.

3. Applications

- Mains fed applications (e.g. TV sound)
- PC audio
- Portable audio.

4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		6	12	18	V
I_q	quiescent supply current	V_{CC} = 12 V; R_L = ∞	-	24	36	mA
I_{stb}	standby supply current		-	-	10	µA

Table 1: Quick reference data...*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_o	output power	THD = 10%; R_L = 8 Ω; V_{CC} = 12 V	6	7	-	W
THD	total harmonic distortion	P_o = 1 W	-	0.03	0.1	%
G_v	voltage gain		31	32	33	dB
SVRR	supply voltage ripple rejection		50	65	-	dB

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
TDA8944J	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

6. Block diagram

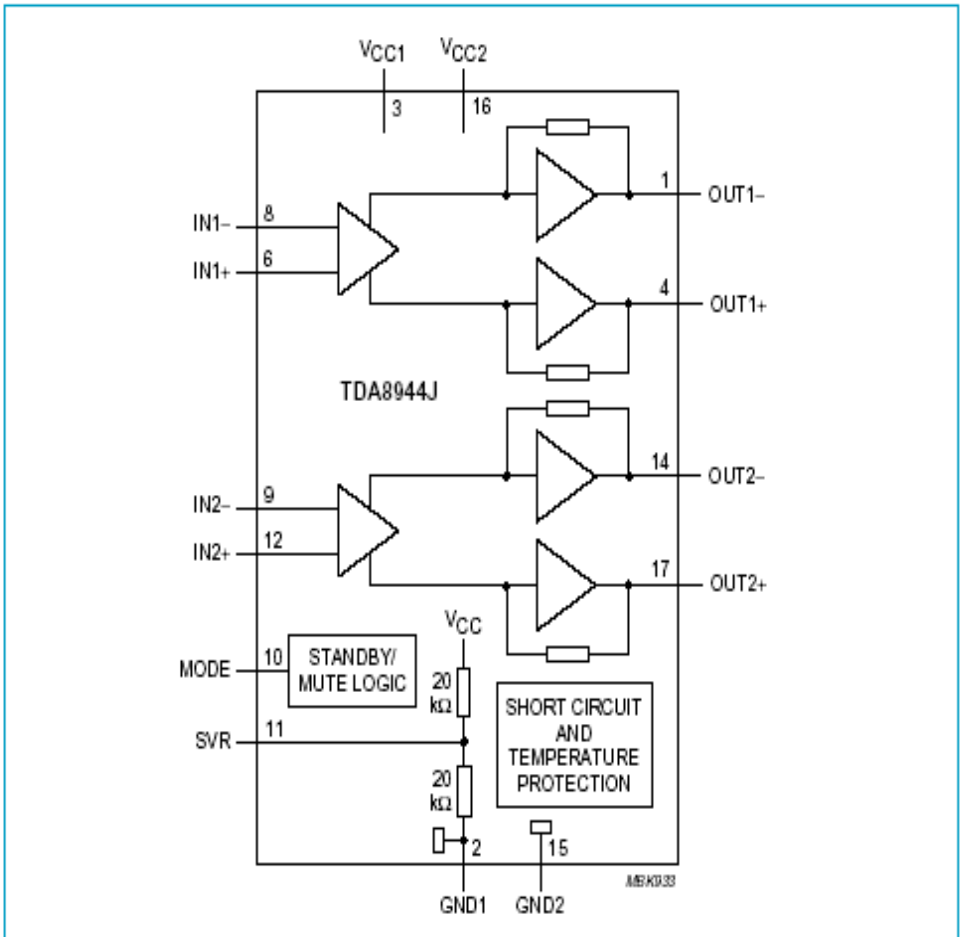


Fig 9. Block diagram

(7) PW166 ImageProcessor

XGA/SXGA Flat Panel Display Controller IC

General

The PW166/PW166B ImageProcessor is a highly integrated "system-on-a-chip" that interfaces analog, digital, and video inputs in virtually any format to a digital projection system or multimedia display. The PW166/PW166B is pin-compatible with the PW164.

An embedded SDRAM frame buffer and memory controller perform frame rate conversion. Computer images from VGA to UXGA at almost any refresh rate can be resized to fit on a fixed-frequency target display device with any resolution up to SXGA with full 24-bit color.

The PW166/PW166B includes advanced second generation image scaling that provides completely programmable, horizontal and vertical image scaling. Keystoning allows vertical keystoning effects. In addition, non-linear scaling is supported for precise scaling control, with 16:9 aspect ration sources and displays.This high-quality scaling—coupled with Auto Image Optimization circuitry—provides sharp, full-screen images, centered on the screen, with no manual adjustments required.

The PW166/PW166B also includes advanced second-generation sync decoding which provides full support for a wide variety of sync types. This includes interlaced, progressive, sync-on-green, and TMDS DE (Data Enable) only.

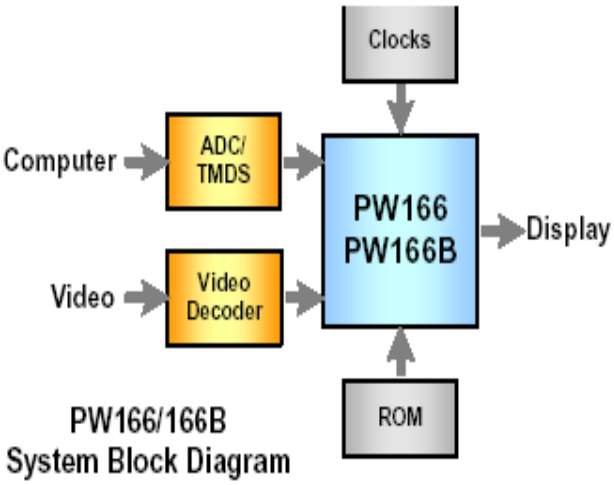
The PW166/PW166B ImageProcessor supports NTSC or PAL video data with a 4:3 aspect ratio and 16:9 aspect ratio sources, such as DVD or HDTV. Nonlinear scaling and separate horizontal and vertical scalers allow these inputs to be resized optimally for the native resolution and aspect ratio of the display device.

The PW166B uses an integrated PLL to synchronize the display interface timing to the input timing. This requires only a single external crystal to generate all necessary clocks for the system (PW166B only).

An integrated OSD controller provides bit-mapped based OSDs with 16 colors from a 64K color palette. The OSD controller supports transparent and translucent functions.

The PW166/PW166B provides a Pulse Width Modulation (PWM) output for low cost backlight or audio control.

With reference source code and an on-chip microprocessor, manufacturers can develop feature-rich products with rapid time-to-market. Programmable features include the user interface, custom start-up screen, all automatic imaging features, and special screen effects.



PW166/166B
System Block Diagram

Features

- Second-Generation Image Scaling
- Second-Generation Automatic Image Optimization
- Video Processing
- Picture-in-Picture (PIP)
- Frame Rate Conversion
- Multi-region, non-linear scaling
- Color Matrix for improved color temperature adjustment
- On-board PLLs to generate MCLK and DCLK (PW166B only)
- On-Screen Display
- On-Chip Microprocessor
- JTAG Debugging Port
- Hardware PWM Output

Applications

- Flat Panel Monitors
- Digital Projection Systems
- Multimedia Displays

Device	Application	Package
PW166-10T PW166B-10T	Up to SXGA in, SVGA/XGA out, no keystone	256 PBGA
PW166-10TK PW166B-10TK	Up to SXGA in, SVGA/XGA out, with keystone	
PW166-20T PW166B-20T	Up to UXGA in, SXGA out, no keystone	
PW166-20TK PW166B-20TK	Up to UXGA in, SXGA out, with keystone	

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y
20	GBE6	GGO2	GGO3	GGO7	GGE2	G COAST	GPEN SOG	GGE4	GGE6	GRO0	GRO4	GRE0	GRE4	GRE5	GRE7	DRE1	VDD 3.3	DRE7	DGE2	DGE4
19	GBE4	GBE5	GGO1	GGO6	GGE1	GBLK SPL	GHS	GCLK	GGE5	GGE7	GRO3	GRO7	GRE1	GRE6	DRE0	VSS	DRE5	DGE1	DGE3	DBE0
18	GBE1	GBE3	VDD 3.3	GBE7	GGO4	GGE0	VDD 2.5	GREF	GGE3	VDD 2.5	GRO2	GRO5	GRE2	VDD 2.5	DRE2	DRE4	DGE0	VDD 3.3	DGE7	DBE1
17	GBO5	GBO7	GBE2	VSS	GGO0	GGO5	VSS	GFBK	GVS	VSS	GRO1	GRO6	GRE3	VSS	DRE3	DRE6	VSS	DGE5	VSS	VDD 3.3
16	GBO1	GBO4	GBO6	GBE0													DGE6	DBE2	DBE6	DBE4
15	V FIELD	GBO0	GBO2	GBO3													DBE3	DBE5	DBE7	DEN
14	VVS	VHS	VDD 2.5	VSS													VSS	VDD 2.5	VSS	VDD 2.5
13	MODE 0	VB7	VPEN	CPU TMS													DHS	DVS	MCK EXT	DCK EXT
12	VSS	VDD 2.5	VB6	VCLK													VSS	VDD 3.3	DCLK	DRO0
11	VB5	VSS	VDD 2.5	VB4													VSS	VDD 2.5	DRO1	DRO2
10	VB3	VB2	VDD 2.5	VSS													DRO3	DRO4	DRO5	DRO6
9	VB1	VB0	VG6	VG5													VSS	VDD 3.3	DRO7	DGO0
8	VG7	VG4	VG1	VG0													DGO3	DGO2	DGO1	DGO4
7	VG3	VG2	VDD 3.3	VSS													VSS	VDD 2.5P	DGO6	DGO5
6	CPU TCK	MODE 2	PORT B5	PORT B2													DBO1	DBO0	VSS	VDD 3.3
5	PORT B7	PORT B6	PORT B1	PORT A5													MODE 1	DBO4	DBO2	DGO7
4	PORT B4	PORT B3	PORT A4	VSS	IR RCVR0	D0	VSS	D8	D13	VSS	VSS	WR	A3	XTAL OUT	A11	A16	VSS	DBO6	VSS	DBO3
3	PORT B0	PORT A6	VDD 2.5	TXD	RESET	D1	VDD 2.5	D9	D14	VDD 3.3	VDD 2.5	RD	A2	XTAL IN	A8	A12	A17	VDD 3.3	CPU TDO	DBO5
2	PORT A7	PORT A2	PORT A0	IR RCVR1	EXT INT	D3	D5	D10	D12	RAM WE	ROM WE	CS0	BHEN	A1	A5	A7	A10	A15	A19	DBO7
1	PORT A3	PORT A1	RXD	NMI	D2	D4	D6	D7	D11	D15	RAM OE	ROM OE	CS1	A0	A4	A6	A9	A13	A14	A18

Fig11.PW166 Pin Diagram - Top View

ImageProcessor Pin Descriptions

<table>
<tr><th>Name</th><th>Pin(s)</th><th>Type</th><th>Function</th></tr>
<tr><th colspan="4">Graphics Port</th></tr>
<tr><td>GCLK</td><td>H19</td><td>ID</td><td>Graphics port pixel clock input. Typically driven by an external PLL GPort Clock. The GCLK pin can be selected to be the source for the internal GCLK that is used for GPort image capture and for the PLL divider (see GCKPOL & GCKSRC bits).</td></tr>
<tr><td>GPENSOG</td><td>G20</td><td>ID</td><td>Graphics port pixel enable input. Used for external flow control when EXTFCE=1. When GPENSOG is high, input RGB pixel is valid. Using GPENSOG allows capture of non-contiguous data.When EXTFCE=0, this is the Graphics port Sync-On-Green (SOG) input. Driven by external sync stripper circuit, this pin is monitored (SOGACT status bit) and can supply composite sync information (depending on SOGEN & COMPEN bits).</td></tr>
<tr><td>GVS</td><td>J17</td><td>ID</td><td>Graphics port vertical sync input. Indicates start of next field or frame of input data. GVS can be either active-high or active-low as determined by VPOL and VSOK. GVS is not used when a composite digital sync source is used (SOGEN=1 or COMPEN=1).</td></tr>
<tr><td>GHS</td><td>G19</td><td>ID</td><td>Graphics port horizontal sync input. Indicates the start of the next line of input data. This signal is internally polarity corrected and monitored for composite sync content (HSOK, HPOL, & COMP status bits). GHS can supply horizontal sync information or digital composite sync information (depending on COMPEN bit). GHS is also used as the input to the clock phase delay circuit that produces the GREF signal.</td></tr>
<tr><td>GFBK</td><td>H17</td><td>I/O</td><td>Graphics port PLL feedback / line advance input. This pin has three different functions depending on the register settings for EXTFBK and EXTFCE:
<table>
<tr><th>EXTFBK</th><th>EXTFCE</th><th>GFBK Function</th></tr>
<tr><td>0</td><td>X</td><td>GFBKOUT: An output from the internal PLL divider.</td></tr>
<tr><td>1</td><td>0</td><td>GFBKIN: An input to the feedback pulse from an external PLL divider. In free running capture mode this signal is used to define the horizontal capture region (along with CAPL and CAPW), and advances the GPort capture controller to the next input line. The LAVPOL bit is used to select the polarity of GFBKIN.</td></tr>
<tr><td>1</td><td>1</td><td>GLAV: An input to the graphics port line advance. Used in external flow control capture mode. When GLAV transitions (depending on LAVPOL bit), the GPort capture controller advances to the next input line.</td></tr>
</table></td></tr>
<tr><td>GRE0</td><td>M20</td><td>ID</td><td rowspan="8">Graphics port red even data sub-pixel input. Red channel data for single pixel mode or even red pixel data for dual pixel input mode. Pr channel data for YPbPr inputs.</td></tr>
<tr><td>GRE1</td><td>N19</td><td>ID</td></tr>
<tr><td>GRE2</td><td>N18</td><td>ID</td></tr>
<tr><td>GRE3</td><td>N17</td><td>ID</td></tr>
<tr><td>GRE4</td><td>N20</td><td>ID</td></tr>
<tr><td>GRE5</td><td>P20</td><td>ID</td></tr>
<tr><td>GRE6</td><td>P19</td><td>ID</td></tr>
<tr><td>GRE7</td><td>R20</td><td>ID</td></tr>
<tr><td>GGE0</td><td>F18</td><td>ID</td><td rowspan="8">Graphics port green even data sub-pixel input. Green channel data for single pixel mode or even green pixel data for dual pixel input mode. Y channel data for YPbPr inputs.</td></tr>
<tr><td>GGE1</td><td>E19</td><td>ID</td></tr>
<tr><td>GGE2</td><td>E20</td><td>ID</td></tr>
<tr><td>GGE3</td><td>J18</td><td>ID</td></tr>
<tr><td>GGE4</td><td>H20</td><td>ID</td></tr>
<tr><td>GGE5</td><td>J19</td><td>ID</td></tr>
<tr><td>GGE6</td><td>J20</td><td>ID</td></tr>
<tr><td>GGE7</td><td>K19</td><td>ID</td></tr>
</table>

ImageProcessor Pin Descriptions (continued)

Name	Pin(s)	Type	Function
GBE0	D16	ID	Graphics port blue even data sub-pixel input. Blue channel data for single pixel mode or even blue pixel data for dual pixel input mode. Pb channel data for YPbPr inputs.
GBE1	A18	ID	
GBE2	C17	ID	
GBE3	B18	ID	
GBE4	A19	ID	
GBE5	B19	ID	
GBE6	A20	ID	
GBE7	D18	ID	
GRO0	K20	ID	Graphics port red odd data sub-pixel input. Not used for single pixel mode, odd red pixel data for dual pixel input mode.
GRO1	L17	ID	
GRO2	L18	ID	
GRO3	L19	ID	
GRO4	L20	ID	
GRO5	M18	ID	
GRO6	M17	ID	
GRO7	M19	ID	
GGO0	E17	ID	Graphics port green odd data sub-pixel input. Not used for single pixel mode, odd green pixel data for dual pixel input mode.
GGO1	C19	ID	
GGO2	B20	ID	
GGO3	C20	ID	
GGO4	E18	ID	
GGO5	F17	ID	
GGO6	D19	ID	
GGO7	D20	ID	
GBO0	B15	ID	Graphics port blue odd data sub-pixel input. Not used for single pixel mode, odd blue pixel data for dual pixel input mode.
GBO1	A16	ID	
GBO2	C15	ID	
GBO3	D15	ID	
GBO4	B16	ID	
GBO5	A17	ID	
GBO6	C16	ID	
GBO7	B17	ID	
GREF	H18	O	Graphics port PLL reference output. Delayed version of internal sync separated GHS. Typically connected to the REF input of PLL. Changing the PHASE bits changes the amount of delay between GHS and GREF.
GBLKSPL	F19	O	Graphics port black sample clamp pulse output. Used as part of an external DC restoration circuit to clamp the black level of the GPort analog RGB data to ground. This pulse occurs after HSync and is programmable (BKSPOL, BKSCEN, BKSBEG, & BKSWID).
GCOAST	F20	O	Graphics port PLL coast control output. Used to enable PLL coasting (ignore GREF and GFBK) during vertical blanking. Used to prevent the PLL from reacting to extra or missing HS pulses during vertical blanking. Coast enable and duration is programmable (PLLCM, PLLCB & PLLCE).
Video Port			
VCLK	D12	ID	Video port pixel clock. Controls video port image capture. Typically driven by external video decoder.
VPEN	C13	ID	Video port pixel enable input. Used for external flow control when EXTFCE=1. When VPEN is high, input pixel data is valid. Using VPEN allows capture of non-contiguous data.
VVS	A14	ID	Video vertical sync. Indicates start of next field or frame of data from external video decoder. VVS can be either active-high or active-low as determined by VPOL. VVS is not used when a composite digital sync source is used (COMPEN).
VHS	B14	ID	Video horizontal sync. Indicates start of next line of data input from external video decoder. VHS can be either active-high or active-low as determined by HPOL. Indicates composite sync when COMP = 1.
VFIELD	A15	ID	Video odd/even field indicator. Indicates whether odd or even field of interlaced input is being captured as determined by FLDINV and FLDSEL. Field information can also be derived from VVS and VHS, so VFIELD is not needed in some applications.

ImageProcessor Pin Descriptions (continued)

Name	Pin(s)	Type	Function
VY0	D8	ID	Video Port Y Pixel Data. Can operate in three different modes: Y Data in YUV 4:2:2 mode; U Data in YUV 4:4:4 mode; Green Data in 24-bit RGB mode.
VY1	C8	ID	
VY2	B7	ID	
VY3	A7	ID	
VY4	B8	ID	
VY5	D9	ID	
VY6	C9	ID	
VY7	A8	ID	
VUV0	B9	ID	Video Port UV Pixel Data. Can operate in three different modes: UV Data in YUV 4:2:2 mode; V Data in YUV 4:4:4 mode; Blue Data in 24-bit RGB mode.
VUV1	A9	ID	
VUV2	B10	ID	
VUV3	A10	ID	
VUV4	D11	ID	
VUV5	A11	ID	
VUV6	C12	ID	
VUV7	B13	ID	
Display Port			
DCKEXT	Y13	ID	Display clock input. Not needed when using on-chip PLL (PW166B only).
DCLK	W12	O	Display pixel clock output. Enabled when DCLKEN=1. Polarity is inverted when DCPOL=1. Runs at ½ pixel rate when DCK2EN=1.
DVS	V13	O	Display vertical sync output. Polarity and timing controlled by VSPOL, VPLSE, and VDLY.
DHS	U13	O	Display horizontal sync output. Polarity and timing controlled by HSPOL, HPLSE.
DEN	Y15	O	Display pixel enable.
DRE0	R19	O	Display red even data sub-pixel out in dual pixel output mode. Display red data sub-pixel out in single pixel output mode.
DRE1	T20	O	
DRE2	R18	O	
DRE3	R17	O	
DRE4	T18	O	
DRE5	U19	O	
DRE6	T17	O	
DRE7	V20	O	
DGE0	U18	O	Display green even data sub-pixel out in dual pixel output mode. Display green data sub-pixel out in single pixel output mode.
DGE1	V19	O	
DGE2	W20	O	
DGE3	W19	O	
DGE4	Y20	O	
DGE5	V17	O	
DGE6	U16	O	
DGE7	W18	O	
DBE0	Y19	O	Display blue even data sub-pixel out in dual pixel output mode. Display blue data sub-pixel out in single pixel output mode.
DBE1	Y18	O	
DBE2	V16	O	
DBE3	U15	O	
DBE4	Y16	O	
DBE5	V15	O	
DBE6	W16	O	
DBE7	W15	O	

ImageProcessor Pin Descriptions (continued)

Name	Pin(s)	Type	Function
DRO0	Y12	O	Display red odd data sub-pixel out in dual pixel output mode. Unused in single pixel output mode.
DRO1	W11	O	
DRO2	Y11	O	
DRO3	U10	O	
DRO4	V10	O	
DRO5	W10	O	
DRO6	Y10	O	
DRO7	W9	O	
DGO0	Y9	O	Display green odd data sub-pixel out in dual pixel output mode. Unused in single pixel output mode.
DGO1	W8	O	
DGO2	V8	O	
DGO3	U8	O	
DGO4	Y8	O	
DGO5	Y7	O	
DGO6	W7	O	
DGO7	Y5	O	
DBO0	V6	O	Display blue odd data sub-pixel out in dual pixel output mode. Unused in single pixel output mode.
DBO1	U6	O	
DBO2	W5	O	
DBO3	Y4	O	
DBO4	V5	O	
DBO5	Y3	O	
DBO6	V4	O	
DBO7	Y2	O	
Microprocessor Interface			
WR	M4	O	Write Enable. Low indicates a write to external RAM or other devices.
RD	M3	O	Read Enable. Low indicates a read to external RAM or other devices.
ROMOE	M1	O	ROM Output Enable. Active low output indicates a read from external ROM.
ROMWE	L2	O	ROM Write Enable. Active low indicates a write to external ROM.
BHEN	N2	O	High-byte enable. Low indicates upper byte of data is valid.
RAMOE	L1	O	RAM output enable. Active low output indicates a read from external RAM.
RAMWE	K2	O	RAM write enable. Active low output indicates a write to external RAM.
CS0	M2	O	Miscellaneous Chip Select 0. Active low output selects external devices. Each Chip Select decodes a 256-byte block of CPU address space (location of block is programmable).
CS1	N1	O	Miscellaneous Chip Select 1. Active low output selects external devices. Each Chip Select decodes a 256-byte block of CPU address space (location of block is programmable).
EXTINT	E2	ID	External interrupt request 0. Can be programmed to be level or edge sensitive. This pin becomes CPUTDI input when the JTAG debugger is enabled.
NMI	D1	ID	Non-maskable interrupt. A high input triggers a non-maskable interrupt to the on-chip microprocessor.

ImageProcessor Pin Descriptions (continued)

Name	Pin(s)	Type	Function
A0	P1	O	Microprocessor address bus output bits (19:0).
A1	P2	O	
A2	N3	O	
A3	N4	O	
A4	R1	O	
A5	R2	O	
A6	T1	O	
A7	T2	O	
A8	R3	O	
A9	U1	O	
A10	U2	O	
A11	R4	O	
A12	T3	O	
A13	V1	O	
A14	W1	O	
A15	V2	O	
A16	T4	O	
A17	U3	O	
A18	Y1	O	
A19	W2	O	
D0	F4	I/O	Microprocessor 16-bit bidirectional data bus.
D1	F3	I/O	
D2	E1	I/O	
D3	F2	I/O	
D4	F1	I/O	
D5	G2	I/O	
D6	G1	I/O	
D7	H1	I/O	
D8	H4	I/O	
D9	H3	I/O	
D10	H2	I/O	
D11	J1	I/O	
D12	J2	I/O	
D13	J4	I/O	
D14	J3	I/O	
D15	K1	I/O	
Peripheral Interface Pins			
PORTA0	C2	I/O	General purpose IO port. PORTA7 can be selected as the PWM output.
PORTA1	B1	I/O	
PORTA2	B2	I/O	
PORTA3	A1	I/O	
PORTA4	C4	I/O	
PORTA5	D5	I/O	
PORTA6	B3	I/O	
PORTA7	A2	I/O	

ImageProcessor Pin Descriptions (continued)

<table>
<tr><th>Name</th><th>Pin(s)</th><th>Type</th><th>Function</th></tr>
<tr><td>PORTB0</td><td>A3</td><td>I/O</td><td rowspan="8">General Purpose I/O Port. Can operate in three different modes:
8 bits of GPIO in VPort YUV 4:2:2 mode;
Y Video Data in VPort YUV 4:4:4 mode;
Red Video Data in VPort 24-bit RGB mode.</td></tr>
<tr><td>PORTB1</td><td>C5</td><td>I/O</td></tr>
<tr><td>PORTB2</td><td>D6</td><td>I/O</td></tr>
<tr><td>PORTB3</td><td>B4</td><td>I/O</td></tr>
<tr><td>PORTB4</td><td>A4</td><td>I/O</td></tr>
<tr><td>PORTB5</td><td>C6</td><td>I/O</td></tr>
<tr><td>PORTB6</td><td>B5</td><td>I/O</td></tr>
<tr><td>PORTB7</td><td>A5</td><td>I/O</td></tr>
<tr><td>IRRCVR0</td><td>E4</td><td>IU</td><td>IR receiver input 0.</td></tr>
<tr><td>IRRCVR1</td><td>D2</td><td>IU</td><td>IR receiver input 1.</td></tr>
<tr><td>RXD</td><td>C1</td><td>ID</td><td>Receive data to the on-chip serial port.</td></tr>
<tr><td>TXD</td><td>D3</td><td>O</td><td>Transmit data from the on-chip serial port.</td></tr>
<tr><th colspan="4">Miscellaneous</th></tr>
<tr><td>RESET</td><td>E3</td><td>IU</td><td>Master reset. A high input initializes all internal logic.</td></tr>
<tr><td>MCKEXT</td><td>W13</td><td>ID</td><td>Memory system clock. Not needed when using on-chip PLL (PW166B only).</td></tr>
<tr><td>MODE2

MODE1

MODE0</td><td>B6

U5

A13</td><td>IU

ID

ID</td><td>
<table>
<tr><th colspan="3">Mode</th><th rowspan="2">Mode Description</th><th rowspan="2">JTAG</th><th rowspan="2">24-Bit</th><th rowspan="2">PLL</th><th rowspan="2">OSC</th></tr>
<tr><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Reserved</td><td>---</td><td>---</td><td>---</td><td>--</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Normal with PLL and OSC</td><td>Yes</td><td>No</td><td>Yes</td><td>Yes</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Normal</td><td>Yes</td><td>No</td><td>No</td><td>No</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>24-bit Addressing Mode</td><td>Yes</td><td>Yes</td><td>Yes</td><td>Yes</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Pin test mode
<table>
<tr><th>VG(7:0)</th><th>Output</th></tr>
<tr><td>0x80</td><td>Z</td></tr>
<tr><td>0x82</td><td>0</td></tr>
<tr><td>0x83</td><td>1</td></tr>
</table></td><td>---</td><td>---</td><td>---</td><td>--</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>PLL and OSC (PW166B only)</td><td>No</td><td>No</td><td>Yes</td><td>Yes</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>PW364 Emulation Mode</td><td>No</td><td>No</td><td>No</td><td>No</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>PLL only (PW166B only)</td><td>No</td><td>No</td><td>Yes</td><td>No</td></tr>
</table>
NOTE: Mode 101 is normal operating mode for PW166B.
</td></tr>
<tr><td>XTALIN</td><td>P3</td><td>ID</td><td>Crystal input for PLL or Clock input if OSC is disabled (PW166B only).</td></tr>
<tr><td>XTALOUT</td><td>P4</td><td>O</td><td>Crystal output (PW166B only).</td></tr>
<tr><th colspan="4">Microprocessor Debug Port</th></tr>
<tr><td>CPUTMS</td><td>D13</td><td>ID</td><td>JTAG input Test Mode Select. Active high to enable JTAG test port for CPU debugger.</td></tr>
<tr><td>CPUTCK</td><td>A6</td><td>ID</td><td>JTAG Test Clock for CPU debugger mode.</td></tr>
<tr><td>CPUTDO</td><td>W3</td><td>O</td><td>JTAG Test Data Output CPU debugger mode.</td></tr>
<tr><th colspan="4">Power and Ground</th></tr>
<tr><td>VDD2.5</td><td>B12,C3, C10, C11, C14, G3, G18, K18, L3, P18, V11, V14, Y14</td><td>P</td><td>2.5V digital power.</td></tr>
<tr><td>VDD2.5P</td><td>V7</td><td>P</td><td>2.5 PLL analog power. Connect to 2.5V supply through a 27 ohm resistor.</td></tr>
<tr><td>VDD3.3</td><td>C7, C18, K3, U20, V9,V12, V18, V3, Y6, Y17</td><td>P</td><td>3.3V digital power.</td></tr>
</table>

ImageProcessor Pin Descriptions (continued)

Name	Pin(s)	Type	Function
VSS	A12, B11, D4, D7, D10, D14, D17, G4, G17, K4, K17, L4, P17, T19, U4, U7, U9, U11, U12, U14, U17, W4, W6, W14, W17	P	Ground.