Model AD413A
Camac Quad 8K ADC
Operating and Service Manual

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Manual Revision E

1202

Advanced Measurement Technology, Inc.

a/k/a/ ORTEC®, a subsidiary of AMETEK®, Inc.

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SAFETY INSTRUCTIONS AND SYMBOLS

This manual contains up to three levels of safety instructions that must be observed in order to avoid personal injury and/or damage to equipment or other property. These are:

DANGER Indicates a hazard that could result in death or serious bodily harm if the safety instruction is not observed.

WARNING Indicates a hazard that could result in bodily harm if the safety instruction is not observed.

CAUTION Indicates a hazard that could result in property damage if the safety instruction is not observed.

Please read all safety instructions carefully and make sure you understand them fully before attempting to use this product.

In addition, the following symbol may appear on the product:

ATTENTION – Refer to Manual

DANGER – High Voltage

Please read all safety instructions carefully and make sure you understand them fully before attempting to use this product.

SAFETY WARNINGS AND CLEANING INSTRUCTIONS

DANGER	Opening the cover of this instrument is likely to expose dangerous voltages. Disconnect the instrument from all voltage sources while it is being opened.

WARNING	Using this instrument in a manner not specified by the manufacturer may impair the protection provided by the instrument.

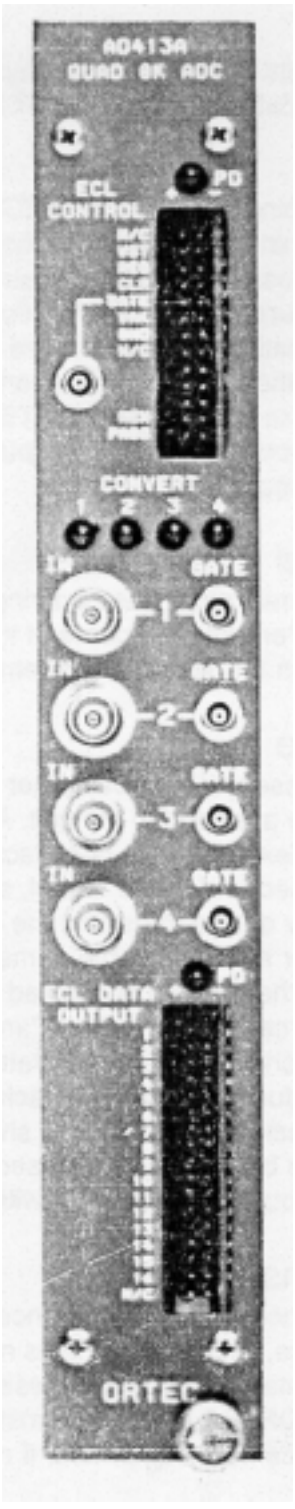
Cleaning Instructions

To clean the instrument exterior:

- Unplug the instrument from the ac power supply.
- Remove loose dust on the outside of the instrument with a lint-free cloth.
- Remove remaining dirt with a lint-free cloth dampened in a general-purpose detergent and water solution. Do not use abrasive cleaners.

CAUTION	To prevent moisture inside of the instrument during external cleaning, use only enough liquid to dampen the cloth or applicator.

- Allow the instrument to dry completely before reconnecting it to the power source.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QUAD 8K ADC
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PD
CONVERT
1 2 3 4
IN
GATE
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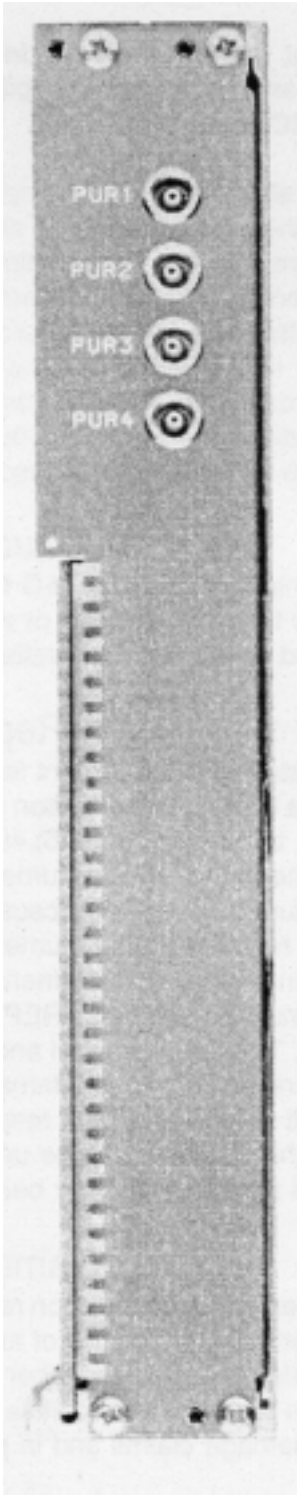
ECL DATA OUTPUT
ORTEC


PUR1
PUR2
PUR3
PUR4

ORTEC MODEL AD413A
CAMAC Quad 8K ADC

1. DESCRIPTION

1.1. GENERAL

The ORTEC Model AD413A CAMAC Quad 8K ADC is a multiplexed, four-input, 13-bit ADC with CAMAC and fast FERAbus readout. It is a very productive solution for high-multiplicity experiments with germanium detectors because it has a conversion time of 6 µs per active input, and a 100-ns-per-word FERAbus readout with the ability to skip ADCs with zero information in 3 ns. This 8064-channel ADC can also be used with surface barrier detectors, scintillation detectors, proportional counters, and ionization chambers.

Each of the four analog inputs has its own peak amplitude stretcher, and accepts pulses in the linear range from 0 to +10 V. The stretchers are multiplexed on a first-come, first-served basis to a 13-bit, successive-approximation ADC with sliding scale linearization. If two or more inputs receive coincident pulses, the pulse amplitudes are stored in their respective stretchers, so that the ADC can successively convert each input. The dc-coupled analog inputs accept unipolar and bipolar pulses from standard spectroscopy amplifiers with shaping times from 0.25 to 20 µs. Differential inputs are incorporated to suppress ground-loop noise when connected to systems with multiple power supplies and grounds.

Each analog input has its own gate input (GATE 1, 2, 3, 4) to suppress analysis of unrelated events when the master gate in the FERA (Fast Encoding and Readout ADC) ECL CONTROL bus is used to synchronize coincident events. The master gate is also available as a TTL input on a LEMO connector, for use with CAMAC readout in the coincidence mode. CAMAC commands permit enabling and disabling the module's response to any gate input. This is useful when selecting the coincidence mode or the singles mode for the AD413A under CAMAC control. Four LEMO connectors on the rear panel accept the pile-up rejector logic signals from the four spectroscopy amplifiers suppling the associated analog input pulses.

Additional modes selectable by CAMAC command are: CAMAC or FERAbus readout, zero suppression or no zero suppression during readout, overflow suppression, singles or coincidence analysis, and random access versus sequential access during CAMAC readout. Each analog input has its own lower-level discriminator, separately adjustable by CAMAC command over the range from 0 to 512 mV with 2 mV/bit resolution.

The AD413A is compatible with the standard LeCroy FERA control and data output busses. This system can provide very fast readout of the ADCs with non-zero events in a CAMAC crate full of ADCs. For both data acquisition and readout, the control bus synchronizes all the ADCs with the experiment's master trigger. This permits identification of all the ADC outputs from the same event and their subsequent assimilation into a common block of data. To the standard FERAbus features, ORTEC has added the ability to select the singles or coincidence analysis mode for any AD413A. This feature allows checking the functionality of a detector via the singles spectrum at any time during an experiment.

Normally, all the ADCs in the crate are connected to a LeCroy Model 4301 FERA Driver for control and readout (Fig. 1 on page 8). The FERA Driver, in turn, delivers the data to either a LeCroy Model 4302 Dual Port Fast Memory in CAMAC, or a CES Model HSM8170 High Speed Memory in VMEbus. Both memories operate in the list mode to assemble the block of coincident events for further processing by an event builder.

2. SPECIFICATIONS

2.1. PERFORMANCE

ADC ANALOG INPUTS Four inputs, each with its own peak amplitude stretcher, accept analog input pulses in the range from 0 to +10V. The stretchers are multiplexed to a single, successive-approximation ADC with sliding scale linearization.

RESOLUTION 8,064 channels (1.25 mV/channel).

CONVERSION TIME 6 µs per active channel input (5 µs for conversion plus 1 µs settling time for the multiplexer.).

INTEGRAL NONLINEARITY <±0.025% over the top 99% of the dynamic range.

DIFFERENTIAL NONLINEARITY <±1% over the top 99% of the dynamic range.

TEMPERATURE SENSITIVITY 0 to 50°C
Gain <50 ppm/°C.
Zero Offset <50 ppm of full scale per °C.

LOWER-LEVEL DISCRIMINATOR RANGE CAMAC controlled from 0 to 512 mV (2 mV/bit.)

UPPER-LEVEL DISCRIMINATOR RANGE Common to all channels and factory set to approximately +10.2 V.

CAMAC CONTROL OF READOUT MODES Selection of: CAMAC or FERAbus (ECL bus) readout, sequential readout of all ADCs or suppression of ADCs with zeros (zero-suppression mode), overflow-suppression option, singles or coincidence modes, random access or sequential CAMAC readout.

READOUT TIME
Zero-Suppressed Readout Mode Two to five words at 100 ns per word for FERAbus readout, or at 1 µs per word for CAMAC readout.
Sequential Readout Mode 0.8 µs for initialization plus four words at 100 ns per word for FERAbus readout, or at 1 µs per word for CAMAC readout.

2.2. CONTROLS AND INDICATORS

CONVERT 1, 2, 3, 4 Four front-panel red LEDs, one for each channel. Each LED blinks once for each pulse that is accepted for conversion.

PD Two front-panel red LEDs, one for the ECL CONTROL connector, and one for the ECL DATA OUTPUT connector. Turned on when the ECL pull-down resistors or termination resistors are installed for the respective connector.

STRETCHER ZERO OFFSET A 12-turn potentionmeter mounted on each of the stretcher printed circuit boards permits adjustment of the stretcher dc offset so that zero pulse amplitude is digitized into channel zero. Maximum input offset compensation is ±20mV.

2.3. INPUTS

IN 1, 2, 3, 4 Four separate front-panel BNC connectors accept analog pulses for pulse amplitude digitization in the linear range from 0 to + 10 V. Each input has its own peak amplitude stretcher multiplexed to the common ADC. Inputs accept positive unipolar pulses, positive gated integrator pulses, or bipolar pulses, with the positive lobe leading. Pulse shapes can be semi-Gaussian or triangular, with shaping time constants from 0.25 to 20 µs, or delay-line-shaped with widths >0.25 µs. Maximum input is ±12 V. No internal delay. Center conductor input impedance is 2000Ω to ground, dc-coupled. The floating BNC connector shield is used with a differential input amplifier to suppress common-mode input noise caused by ground loops. The common-mode rejection ratio is nominally 99:1 with a zero-impedance source, and nominally 22:1 with a 93-Ω signal source.

GATE 1, 2, 3, 4 Four front-panel LEMO connectors provide separate gating for each analog input. Inputs are compatible with TTL logic levels. A low logic level (0 to +0.8 V) prevents analysis of the analog signal at the associated IN connector; a high logic level (+2 to +5 V) permits analysis of the analog signal. With no input connected, the GATE input remains at the high logic level. The GATE signal must be at the desired logic level prior to the peak amplitude of the analog pulse, and must extend ≥0.5 µs beyond peak detection. Input impedance is 1000Ω. Response to each GATE connector can be enabled/disabled by CAMAC commands.

GATE Front-panel LEMO connector accepts the master gate signal for coincidence mode operation with CAMAC readout. See ECL GATE for function. A lot TTL logic level (0 to +0.8 V) prevents analysis, and a high TTL logic level (+2 to +5 V) permits analysis. With no input connected, the GATE input remains at the low logic level. Input impedance is 1000Ω.

PUR 1, 2, 3, 4 Four rear-panel LEMO connectors accept the pile-up rejector logic signals from the four spectroscopy amplifiers supplying the associated analog input pulses. The inputs are compatible with TTL logic levels. A high logic level (+2 to +5 V) causes rejection of the analog signal; a low logic level (0 to +0.8 V) permits analysis of the analog signal. The circuit defaults to a low logic level if no input is connected. The PUR signal must be at the desired logic level prior to the peak amplitude of the analog pulse, and must extend ≥0.5 µs beyond peak detection. Input impedance is 1000 Ω. Can be used as veto inputs.

2.4. ECL INPUTS/OUTPUTS

The fast FERAbus readout utilizes the front-panel ECL CONTROL bus and the ECL DATA OUTPUT bus.

ECL LOGIC LEVELS

Nominal differential ECL logic levels (into 100 Ω differential load) are:

	Left (+) Pin	Right (−) Pin
Logic 0	−1.8 V	−0.9 V
Logic 1	−0.9 V	−1.8 V

ECL DATA OUTPUT Front-panel 17- by 2-pin connector (AMP 1-103326-7) provides the digitized ADC outputs for connection to the FERA data readout bus. Differential ECL outputs are employed, with bit 1 assigned to the two pins in row 1, and bit 16 occupying the two pins in row 16. Row 17 is not connected. See READOUT FORMAT. Interconnection between ADC modules and FERA Driver (LeCroy 4301) requires construction of a 34-conductor ribbon cable (3M part number 3365/34) with 17- by 2-pin headers (3M 3414-6006 or AMP 499498-9) spaced to match the configuration of modules (Fig. 1). Only one module on the ECL DATA OUTPUT bus should have the pull-down resistors installed (See PD LED and Fig. 1).

ECL CONTROL BUS Front-panel 8- by 2- pin connector accommodates the control bus for synchronizing data acquisition among multiple ADCs, and for ECL readout. A row of two pins is assigned to each differential ECL input or output. Interconnection between ADC modules and the FERA Driver (LeCroy 4301) requires construction of a 16-conductor ribbon cable (3M part number 3365/16) with 8- by 2-pin headers (3M 3452-6006 or AMP 499497-3) spaced to match the configuration of modules (Fig.1**). Only one module on the ECL CONTROL bus should have the pull-down and termination resistors installed (See PD LED and Fig. 1**). The logic signals in the ECL CONTROL bus are listed below. Except where noted otherwise, the inputs to the AD413A are provided from the LeCroy 4301 FERA Driver connected to the bus.

N/C No connection.

WST The Write Strobe output indicates when each output word is valid on the ECL DATA OUTPUT connector. WST is released 15 ns after the Write Acknowledge (WAK) is received.

REQ The Request output indicates that the module has completed its conversions, and is ready to take control of the ECL DATA OUTPUT bus for readout. REQ can be asserted only if FERAbus readout is enabled.

CLR The Clear input clears stored data and conversions in progress for all ADCs connected to the ECL CONTROL bus. It is required in the coincidence mode at the end of readout to simultaneously release all ADCs for the next conversion. CLR is not required in the singles mode. The differential ECL input impedance is 100 Ω. Minimum width, 5 ns. Clear can also be initialed from the CAMAC interface. If Clear is asserted during ADC conversion, up to 5 µs are required to clear the module.

GATE The Gate input simultaneously provides the master gate signal to all ADCs connected to the ECL CONTROL bus for coincidence mode operation. This ECL GATE input is OR'ed with the TTL master gate input from the LEMO connector. The logic 1 state enables acceptance of the analog input signal for conversion, and forces all ADCs to wait for a common clear (CLR) after analyzing coincident events. With no signal connected, the GATE input remains in the logic 0 state. The GATE signal must arrive before the peak amplitude on the analog input signal, and extend ≥0.5 µs beyond peak amplitude detection. With termination resistors installed, the differential ECL input

impedance is 100 Ω. Response to the GATE input can be enabled/disabled by CAMAC commands.

WAK The Write Acknowledge input signal indicates through the readout controller (LeCroy 4301) that the associated memory has read the current word and that the next word may be sent. The differential ECL input impedance is 100 Ω. WAK minimum width is 30 ns.

GND Connected to Ground.

N/C No connection.

REN The Readout Enable input is a front-panel, 1- by 2-pin connector. It accepts the PASS output from a previous module, or the REO output from the LeCroy 4301, to enable readout of the AD413A. The ECL differential input impedance is 100 Ω. Interconnection requires construction of a 100-Ω, twisted-pair cable with a 2-pin socket and housing (AMP 1-87756-8 and AMP 5-87456-3) on each end.

PASS The PASS output is in provided on a front-panel, 1- by 2-pin connector. It indicates completion of the module's readout cycle on the ECL bus. The PASS output is normally connected to the REN input on the next module to enable readout of the next module (Fig. 1). In the zero suppression mode, the AD413A generates the PASS signal typically within 3 ns of receiving the REN signal if the AD413A has no data to read out. The PASS signal from the last AD413A in the readout loop is used to generate the CLR signal via the external master trigger logic for the experiment and/or the LeCroy 4301.

2.5. CAMAC COMMANDS

Z Initializes module. Clears the module, sets all bits of control registers 1 and 2 to zero, and sets all LLD registers to 36 (72 mV).

C Performs the same function as the CLR input on the ECL CONTROL bus.

I Inhibits subsequent conversion when present. Conversions and readouts already in progress are not affected. Used to start and stop data acquisition.

X Generated by the module for all valid functions.

Q Generated by the module if the function can be executed.

L LAM is set (if CAMAC readout is enabled, and if LAM is enabled) after the end of conversion, if there are data to be read. See CONTROL REGISTER FORMAT.

F(0)·A(0)	Read Control Register 1
F(0)·A(1)	Read Control Register 2
F(1)·A(0)	Read Channel 1 LLD setting
F(1)·A(1)	Read Channel 2 LLD setting
F(1)·A(2)	Read Channel 3 LLD setting
F(1)·A(3)	Read Channel 4 LLD setting
F(2)·A(0-3)	Read ADC conversions. When the Random Access mode is selected, A = 0, 1, 2, or 3 selects the ADC to be read (ADC 1, 2, 3, or 4, respectively). When the Sequential CAMAC readout mode is selected, the value given for A is ignored, and the command is issued four times to read the four ADCs in sequence. See B14 of Control Register 1. If zero suppression is active in the Sequential CAMAC readout mode, the command is issued 2 to 5 times until Q = 0. Q = 1 if valid data is available.
F(8)·A(0)	Test LAM. Q = 1 if LAM is present.
F(9)·A(0)	Clear Module. Performs the same function as the C command, except only for the single module being addressed through CAMAC.
F(10)·A(0)	Test and clear LAM. Q = 1 if LAM was set.
F(16)·A(0)	Write Control Register 1
F(16)·A(1)	Write Control Register 2
F(17)·A(0)	Write Channel 1 LLD Value
F(17)·A(1)	Write Channel 2 LLD Value
F(17)·A(2)	Write Channel 3 LLD Value

F(17)·A(3) Write Channel 4 LLD Value

CONTROL REGISTER 1 FORMAT

Bit	Function
B1 - B8	Virtual Station Number; Index Source for readout with zero suppression. (Lower eight bits of header word.)
B9	Zero-suppression enable; when B9 = 0, ADCs with zeroes for data are skipped during readout.
B10	ECL port enable; when B10 = 0, ECL port readout is enabled. When B10 = 1, CAMAC readout is enabled.
B11	Not used.
B12	Not used.
B13	Coincidence/Singles selection for all 4 inputs. When B13 = 0, the coincidence mode is selected. When B13 = 1, the singles mode is selected. When in the singles mode, the zero-suppression mode must be selected for all ADCs in the same FERAbus readout loop.
B14	CAMAC random access enable; when B14 = 1 and B10 = 1 and B9 = 1, random access CAMAC readout is enabled.
B15	CAMAC LAM enable; when B15 = 1, LAM is enabled.
B16	Overflow-suppression enable. When B16 = 0, overflows are converted to zeroes in the ADC output data. Readout will be suppressed only if the zero-suppression mode is selected.

CONTROL REGISTER 2 FORMAT

Bit	Function
B1	Enable GATE 1 (B1 = 0); When B 1 = 1, the GATE 1 input is ignored and all analog pulses in channel 1 are converted, unless gated by the master GATE in the ECL CONTROL bus, or by PUR 1.
B2	Enable GATE 2 (B2 = 0). Function similar to B1
B3	Enable GATE 3 (B3 = 0). Function similar to B1.
B4	Enable GATE 4 (B4 = 0). Function similar to B1.
B5	Enable master GATE (B5 = 0) for the coincidence mode. When B5 = 1, the master GATE signal in ECL CONTROL bus is ignored and all analog pulses are converted, unless gated by GATE 1, 2, 3, or 4, or by PUR 1, 2,3, or 4. B5 = 1 may be used only with the singles mode.

2.6. READOUT FORMAT

The readout format of the AD413A is identical in both the CAMAC and the FERAbus ECL readout modes

WITHOUT ZERO SUPPRESSION

B16	B15	B14	B13 . . . . . B1
0	0	0	CHANNEL 1 DATA
0	0	0	CHANNEL 2 DATA
0	0	0	CHANNEL 3 DATA
0	0	0	CHANNEL 4 DATA

WITH ZERO SUPPRESSION When zero suppression is enabled and valid data is received, two to five data words are output. The first is always a header word:

B16	B15	B14	B13. . .B12	B11	B10	B9	B8 . . B1
1	0	0	WRDCNT	0	0	0	VSN

Followed by 1 to 4 Data Records

B16	B15	B14	B13 . . . . . B1
0	SUBADDR		DATA

DEFINITIONS

WRDCNT The word count is a value from 0 to 3 which defines the number of data records that follow in the Readout. A value of 0 indicates that four data records follow.

VSN The Virtual Station Number (0 – 255) identifies the module number during zero-suppressed Readout. VSN is set via CAMAC command in the lower 8 bits of Control Register 1.

SUBADDR The Subaddress (0 – 3) indicates with which of the four input channels the data is associated. NOTE: The data records are in no particular order in the zero-suppression mode. Therefore, the subaddress should always be used to determine which channels are delivering data.

SUBADDR = 0 Channel 1 data
SUBADDR = 1 Channel 2 data
SUBADDR = 2 Channel 3 data
SUBADDR = 3 Channel 4 data

DATA Thirteen bits of ADC data. DATA over 8064 indicates overflow.

2.7. ELECTRICAL AND MECHANICAL

POWER REQUIRED The Model AD413A derives its power from a CAMAC crate supplying ±24 V and ±6 V. The power required is + 24 V at 380 mA, +6 V at 2 A,-6 V at 1.2A, and −24 V at 430 mA.

WEIGHT
Net 1.1 kg (2.5 lb).
Shipping 2.0 kg (4.5 lb).

DIMENSIONS CAMAC-standard double-width module, 3.42 X 22.15 cm (1.35 X 8.72 in.) front panel per IEEE/583-1975.

3. INSTALLATION

3.1. INSTALLATION IN CAMAC CRATE

The AD413A may be placed in any available slot in a CAMAC crate except for the slot which is reserved for the crate controller, usually slot 25. The power to the crate should *ALWAYS* be turned off when inserting and removing modules to prevent problems associated with momentary misalignment of the card edge connections.

With the power to the crate turned off, slide the module into any available slot and tighten the jack screw on the bottom front of the module to force the card edge connector into the CAMAC bus. The AD413A requires two CAMAC slots; however, the module responds only to CAMAC functions issued to the higher number slot. For example, if the AD413A occupies slots 10 and 11, the AD413A responds to commands issued to slot 11, but not slot 10.

3.2. AMPLIFIER CONNECTIONS

In a standard electronics setup, each of the four channels in the AD413A has two connections to an associated amplifier. The input, on the front panel of the AD413A, is normally connected to the output of the amplifier. The PUR input on the rear panel of the AD413A, which is used to reject pulses that are too close together to be properly processed with the selected pulse shaping time, is normally connected to the amplifier pile-up reject output, labeled PUR or INHIBIT. The following chart shows the normal connections to various ORTEC amplifiers.

AD413A Amplifier Connections

Amplifier	IN	PUR
ORTEC MODEL 572	UNI or BI	INH
ORTEC MODEL 671	UNI or BI	PUR
ORTEC MODEL 672	UNIPOLAR OR BIPOLAR	PUR
ORTEC MODEL 673	UNIPOLAR OR GI	INHIBIT
ORTEC MODEL 973	OUTPUT OR GI	PUR

If a transistor-reset preamplifier (TRP) is connected to the detector, PUR must be connected differently. If a Model 572 or 673 amplifier is used, connect PUR on the AD413A to the INHIBIT OUTPUT on the Model 132 inhibit generator, and connect INHIBIT on the amplifier to INHIBIT INPUT on the Model 132. If a Model 671, 672, or 973 amplifier is used, connect INHIBIT OUTPUT on Model 132 to INHIBIT INPUT on the amplifier, and connect PUR on the amplifier to PUR on the AD413A.

If a Model FG424 fine-gain and offset controller is in the system, the amplifier output connects to the FG424 input and the FG424 output connects to the AD413A input. The PUR connection is unchanged. Refer to the specification in Section 2 for further details concerning the INPUT and PUR inputs.

3.3. ECL BUS INSTALLATION

An ECL bus interface is provided on the AD413A for high-speed readout of ADC data. The ECL bus is designed to permit multiple ADCs to be connected to the bus in parallel for readout of a large number of channels. A wiring diagram for a multiple ADC system is shown in Fig. 1. Across the top of all modules is a control bus, which controls the readout process. The bus is formed from a 16-conductor ribbon cable with an 8- by 2-pin header mounted on it for each ADC. Located across the bottom of the modules is the ECL OUTPUT bus. This bus is formed with a 34-conductor ribbon cable with a 17- by 2-pin headers mounted on the cable for each ADC. REN and PASS are normally connected as shown in Fig 1. In the first module in the chain, REN is connected to REO on the FERA driver. On the remaining modules, REN is connected to PASS from the previous unit. The PASS output on the final unit is normally connected to the Clear input on the FERA driver to clear the ADCs in preparation for the next event. In experiments with an event master trigger, the PASS output from the final AD413A may be sent through the master trigger logic to generate the Clear input for the FERA driver. See Appendix A for information on cables.

3.3.1. ECL BUS RESISTOR PACKS

If an acquisition system makes use of multiple AD413A modules connected together with an ECL bus, the resistor packs must be removed from all except the last module in the chain of modules. The PD LEDs on the front panel of the AD413A are lit when the resistor packs are installed. Figure 1 indicates which module in a chain of modules should have the packs installed

To remove the resistor packs from a module do the following:

1. Turn off power to CAMAC crate and remove AD413A module after disconnecting all cables.
2. Slide the left side plate back approximately 4 inches to reveal the components near the front panel of the module.
3. Locate resistor packs labeled RA3, RA4, RA5, RA6, RA7, RA8, and RA9. Remove the resistor packs from their sockets.
4. Store the resistor packs in a safe location, so they can be found and replaced, if necessary.
5. Close the side panel and return the module to the CAMAC crate.

Should it become necessary to replace the resistor packs once they have been removed, refer to Table 3.1 to determine which types belong in each location. Make sure to orient the resistor packs correctly before insertion into the socket. In the Main Component Assembly Drawing. pin 1 is indicated with a bar across the pack and a small “1". On most resistor packs, pin 1 is indicated with a dot.

Table 3.1 Resistor Pack Values

Resistor Pack	Value(Ω)	No. of Pins
RA3, RA4 RA5, RA6	470	10
RA7	470	6
RA8	56	8
RA9	2200	6

NOTE: When reading values on resistor packs, 470 is often designated 471, 56 is often designated 560, and 2200 is usually designated 222.

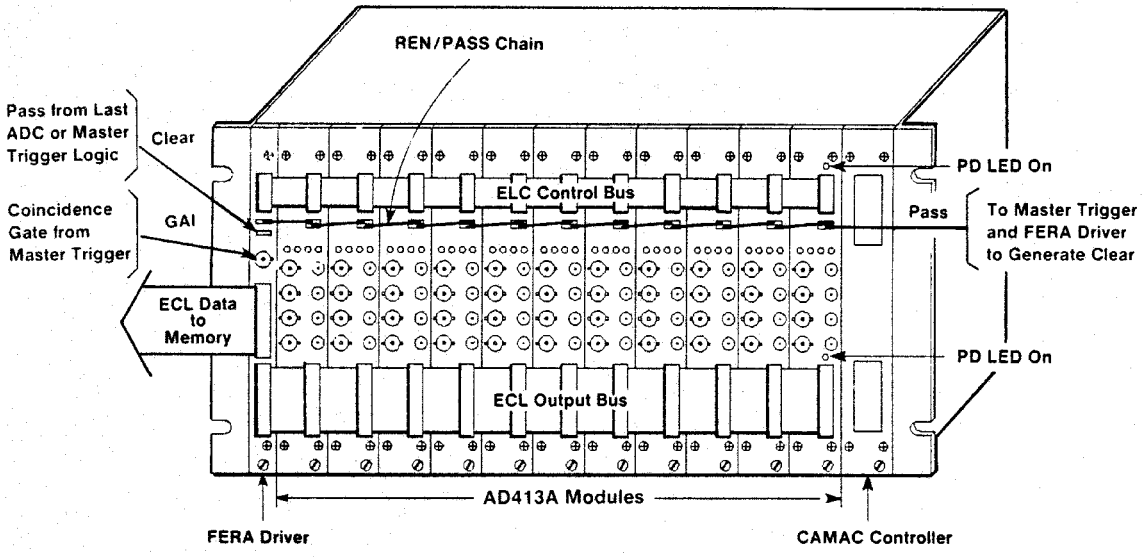


Fig. 1. Interconnection of Multiple AD413As and the LeCroy 4301 FERA Driver for FERAbus Readout.

4. OPERATION

4.1. LOWER-LEVEL DISCRIMINATOR

Each channel in the AD413A has a programmable lower-level discriminator (LLD) setting. This voltage level determines the minimum amplitude pulse that will be accepted by the ADC. Normally the lower-level is set just above the level of the noise in the system, so time is not wasted converting noise pulses.

The lower level in the AD413A is set with the CAMAC command F(17). The sub-addresses 0 through 3 specify which channel's lower level is to be set. For example, A = 0 sets channel 1, and A = 3 sets channel 4. An 8-bit value is written to the module during this CAMAC command specifying the voltage in units of 2 mV. A value of 50 in the lower-level register sets the voltage to 100 mV. The lower-level setting may be read with the F(1) CAMAC command. The returned value is also in units of 2 mV. When reading the lower-level setting, only the low 8 bits are valid. Any higher bits should be ignored. The high bits may be cleared by performing an AND function between the returned value and 255 decimal (e.g., in BASIC, INFO = INFO AND 255).

The CAMAC commands that change and report the lower levels are active only when the ADC is not busy. The ADC is not busy after a clear command and before the peak of the next acceptable pulse after the clear. No Q response is given if the ADC is busy when the commands are issued. To guarantee that the ADC is not busy, set the CAMAC inhibit line (I) and clear the module (C command).

The initial setting of all lower-level voltages on initialization (Z command) is 36, which corresponds to 72 mV.

4.2. GATING SIGNALS

Three input signals are available to select which pulses are to be converted by the ADC: PUR, GATE, and MASTER GATE. If any one of the signals indicates that the pulse is to be rejected, the pulse will be rejected. All three inputs are sampled approximately 100 ns after the peak of an input pulse; therefore, the gating signals should arrive before the peak of the pulse and extend at least 500 ns beyond the peak to ensure proper sampling.

PUR or pile-up reject is always active and is normally connected to the pile-up reject output on an amplifier associated with the channel. When the PUR input in high, pulses are not converted. The PUR input is pulled low, so if no connection is made, no pulses are rejected by PUR.

GATE 1, 2, 3, or 4 is an individual gate input for each channel in the AD413A. The individual gates can be used in addition to the master gate to ensure that each ADC accepts only pulses that are judged to be valid for the ADC input. GATE 1, 2, 3,

or 4 may be disabled by setting the appropriate bit in control word 2 (see Section 4.3). If the GATE is enabled, pulses are converted only if the gate signal is high. The GATE (1, 2, 3, 4) input assumes a high state when no connection is made to the GATE (1, 2, 3, 4) input.

The master GATE signal may be supplied via the ECL control bus or the LEMO connector on the front panel (see Sections 2.2 and 2.3). Normally, the master GATE is a gate signal that is applied to all channels in all the AD413A modules connected to a common ECL control bus. The master gate signal not only provides a gating function, it also determines which pulses are to be grouped together as a coincident event. When t he master gate is high, pulses are accepted into the AD413A. When the master gate returns low, no pulses are accepted in the ADC until a clear command is given, even if the master gate returns high. The master gate may be disabled in any AD413A by setting bit 5 in control word 2 (see Section 4.3). Disabling the master gate in not recommended for coincidence spectra experiments, because there is no signal to indicate which pulses belong in the coincident event. Disabling the master gate is useful only when collecting singles spectra.

4.3. CONTROL REGISTERS

Two control registers exist in the AD413A to set the various modes of operation. Control register 1 specifies the virtual station number of the module as well as the readout and operation modes. Control register 2 specifies which gating signals are to be enabled.

Control register 1 is loaded with the CAMAC function F(0)·A(0), and is queried with the CAMAC function F(16)·A(0). Control register 2 is loaded with the CAMAC function F(0)·A(1), and is queried with the CAMAC function F(16)·A(1). These CAMAC commands are active only when the ADC is not busy. The ADC is not busy after a clear command and before the peak of the next acceptable pulse after the clear. No Q response is given if the ADC is busy when the commands are issued. To guarantee that the ADC is not busy, set the CAMAC inhibit line (I) and clear the module (C command).

The lower 8 bits of control register 1 from the virtual station number for the module. The remaining bits in control register 1 have the following function:

Zero-Suppression Enable (Bit 9) Specifies zero-suppression readout mode as opposed to sequential mode (ECL PORT or CAMAC) or random access (CAMAC only).

= 0; Zero-suppression selected.
= 1; Sequential or random access selected. See Bit 14.

ECL Port Enable (Bit 10) Specifies which readout port is to be used; CAMAC or ECL.

= 0; ECL readout enabled.
= 1; CAMAC readout enabled.

Coincidence/Singles Mode Select (Bit 13) Specifies coincidence mode or singles mode.

= 0; Coincidence mode selected.
= 1; Singles mode selected. See Section 4.6

CAMAC Random Access Enable (Bit 14) Specifies random access mode as opposed to sequential readout mode when CAMAC readout without zero suppression is enabled. If ECL PORT is enabled (Bit 10 = 0) or zero suppression is enabled (Bit 9 = 0), this bit is ignored.

= 0; Sequential readout selected..
= 1; Random access selected.

CAMAC LAM Enable (Bit 15) Specifies whether or not LAM is to be asserted when data is ready to be readout on the CAMAC port.

= 0; LAM not asserted..
= 1; LAM is asserted if CAMAC readout is selected.

Overflow-Suppression Enable (Bit 16) Specifies overflow-suppression mode.

= 0; Overflow suppression enabled. When used in conjunction with zero-suppression mode, pulses above the upper-level discriminator are not reported. When not in zero-suppression mode, pulses above the upper-level discriminator are reported as zero.
= 1; Overflow-suppression disabled. All pulses above the upper-level discriminator are reported with a value between 8064 and 8191.

Control Register 2 contains 5 bits which determine which gate signals are enabled. If a gate signal is disabled, then a pulse is accepted regardless of the state of the gate signal. Control Register 2 has the following definition:

Enable Gate 1 (Bit 1)

= 0; Front-panel gate for channel 1 enabled.
= 1; Gate for channel 1 disabled.

Enable Gate 2 (Bit 2)

= 0; Front-panel gate for channel 2 enabled.
= 1; Gate for channel 2 disabled.

Enable Gate 3 (Bit 3)

= 0; Front-panel gate for channel 3 enabled.
= 1; Gate for channel 3 disabled.

Enable Gate 4 (Bit 4)

= 0; Front-panel gate for channel 4 enabled.
= 1; Gate for channel 4 disabled.

Enable Master Gate (Bit 5)

= 0; Master gate is enabled.
= 1; Master gate is disabled. This mode should not be selected while in the coincidence mode of operation because the master gate determines which pulses belong in a given event. This mode should be used only in the singles mode.

On power-up, the control registers have an undetermined value. If an initialize (Z) command is issued to the CAMAC crate, all bits of the control registers are set to zero.

4.4. MULTIPLEXER/CONVERTER OPERATION TIMING

Figure 2 illustrates the conversion and readout timing when a pulse is accepted into the module. The conversion process begins as soon as a peak detect occurs in any one of the four channels. The conversion phase then takes 6 µs per valid input. If an input happens to be greater than the upper-level discriminator setting. 1µs of dead time is required. If a channel is rejected by PUR, the individual gate, or the lower-level discriminator, no time is required during T1 for that channel.

When the conversion phase completes AND the master gate has returned low, the readout phase begins. The time required to read out depends on the readout method and the mode selected. See Fig. 2 for details.

Once readout completes, a clear command must be issued by the readout electronics. Following the clear command, and initialization sequence is performed in which the readout memory is loaded with zeros if zero-suppression is not used. The next pulse can be accepted after the initialize phase. If zero suppression is used, no time is required to initialize the readout memory.

4.5. READOUT PORT

Data from the AD413A can be read from either the CAMAC interface of the ECL BUS interface. The ECL BUS interface is designed for high-speed Readout, up to 10 MHz, and is suited for bussing many ADC modules together into a large system. However, additional external hardware (FERA drivers, FIFO memories, cables, etc.) is required to buffer the data and transfer it to permanent storage. When CAMAC readout is utilized, Readout occurs at speeds a factor of 10 or more slower; however, performing the readout via CAMAC does not require any extra hardware to get data out of the ADC and into a host computer.

When the AD413A is initialized, the default readout method is the ECL BUS. To select the CAMAC option, bit 10 of control register 1 should be set high.

4.5.1. CAMAC READOUT

When CAMAC readout is selected, data is read from the ADC via CAMAC operations. Three modes exist for reading data from the module via the CAMAC interface: “zero suppression,” “addressed,” and “sequential.”

In zero-suppression mode, non-zero data is sequentially available to the CAMAC dataway until all valid data have been read. At that time, a Q = 0 response is given when the read ADC data command is given (F(2)). The first output word in a readout cycle is the header word that identifies the AD413A, which is reporting data and indicates the number of data words which follow. The format of the header word is shown in Section 2.6. One to four data words follow the header in no particular order. The channel that converted the data must be determined from bits 14 and 15 of the data word

(see Section 2.6). Zero-suppression mode is enabled by setting bit 9 of control register 1 to 0.

In addressed readout mode, the various channels can be addressed in a random access fashion by selecting the ADC channel data to be red with CAMAC subaddresses. In this mode, four data words would have to be read from the module to ensure that all available data are read. Channels that had no pulse arrive during the gating time will report zero. If overflow suppression is enabled, zero will be reported for all overflows. If overflow suppression is disabled, a value greater than 8064 is reported for all overflows. Addressed readout mode is selected by setting bits 9 and 14 of control register 1 to 1.

When sequential readout mode is selected, there are always four data words to be read from the ADC after an event occurs. (Master Gate goes high then low.) The four data words are read by issuing the F(2)·A(0) CAMAC command four times in a row. After all four words have been read, Q = 0 occurs if the command is issued again. Channels that had no pulse arrive during the gating time will report zero. If overflow suppression is enabled, zero will be reported for all overflows. If overflow suppression is disabled, a value greater than 8064 is reported for all overflows. Sequential readout is selected by setting bit 9 of control register 1 to 1 and bit 14 to 0.

Regardless of the readout mode selected, the module must be cleared after readout is completed to permit new conversions. The clear can be initiated with the global CAMAC clear function, and addressed clear to a single module [F(9)], or a clear from the ECL bus on the front panel.

If bit 15 in control register 1 is set, a Look-At-Me (LAM) signal is asserted by the module when data is ready to be read. If zero-suppression or sequential mode is selected, the LAM will be removed when the last data word is read. In addressed readout mode, LAM remains asserted until the clear command is issued. The LAM may also be cleared with the F(10)·A(0) command.

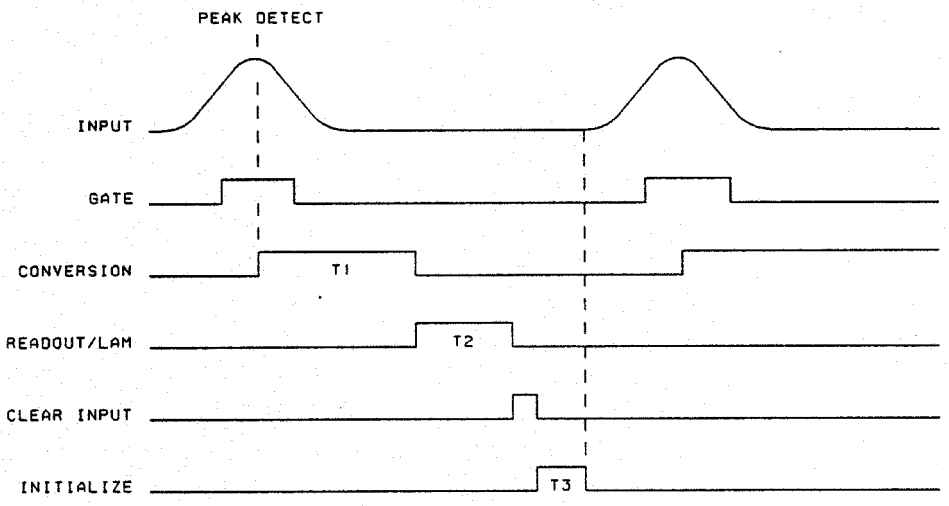


Fig. 2. Conversion Timing Diagram.

4.5.2. ECL PORT READOUT

When ECL readout is selected, data is read from the ADC via the front panel ECL DATA port. Multiple AD413A modules may be connected in parallet on the ECL bus for readout of a large number of channels. When multiple ADCs are connected to the ECL bus, a FERA driver module (LeCroy 4301 or CES 1570) is required to control the bus. Two readout modes exist for ECL readout: “sequential mode” and “zero suppression mode.”

In sequential mode, four data words are sequentially available to readout. When this mode is used, every ADC module in the system will always report four data words when an event occurs (mast gat is asserted). The format of the data words can be found in Section 2.6. If overflow suppression is enabled, a zero is output in place of the overflow. If overflow suppression is disabled, a value greater than 8064 is output in place of the overflow value. If a channel receives no pulse during the gating time, a zero is output during readout.

In zero-suppression mode, only non-zero data is output on the ECL port. If no non-zero data is available, no data is output onto the ECL bus. If there is data to be read, the module outputs a header word, which contains the virtual station number of the ADC and the number of the data words to follow. Therefore, when an ADC module receives non-zero data, two to five data words are output on the bus; no data is placed on the bus if the data is all zero. Zero-suppression mode is the mode of choice in most experiments, because time is not wasted reading zeros out of modules that did not receive a pulse during the event. The ECL readout passes by an ADC with zeros typically within 3 ns in the zero-suppression mode.

Regardless of the readout mode selected, the module must be cleared after readout to permit new conversions. The clear can be initiated with the global CAMAC clear function, an addressed clear to a single module [F(9)], or a clear from the ECL control bus on the front panel.

Five different control signals are used to control ECL PORT readout. A description of each follows, and their relationship can be observed in Fig. 3.

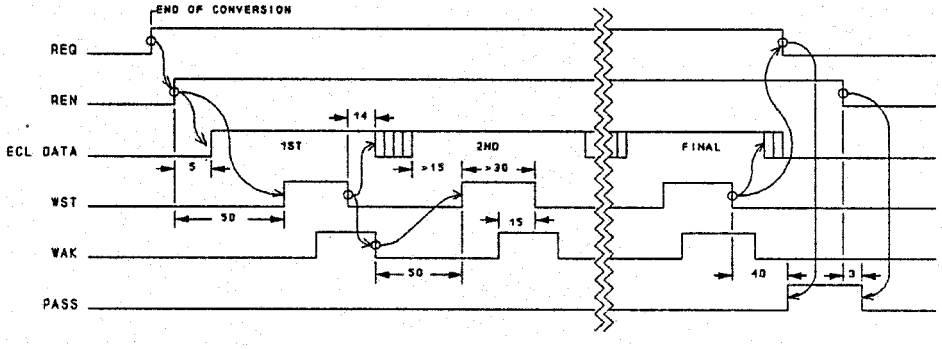


Fig. 3. ECL Port Readout Timing Diagram.

REQ (Output) The readout request signal is asserted by the AD413A as soon as data are ready for readout. REQ is removed when the last datum has been read or a clear command is given.

REN (Input) The readout enable input causes an AD413A to begin readout if it has data ready to be output. Once REN is asserted, it must remain active throughout the entire readout cycle.

PASS (Output) The pass output is asserted by the AD413A if REN is asserted, if the module is not busy converting, and if the module does not have any data to output. The AD413A will not generate a PASS signal as long as it is busy converting new data. This feature allows ADCs with different conversion times to be placed in the same FERA readout loop without additional hardware.

WAK (Input) The write acknowledge input is asserted by the readout controller when the data on the ECL port output has been accepted.

WST (Output) The write strobe output is asserted by the AD413A when a data word is available on the ECL port output. The data is stable on the output a minimum of 15 ns before the write strobe occurs, and the write strobe continues to be asserted a minimum of 15 ns after the write acknowledge signal has occurred.

WAK should be removed after WST has been released. WST is not reasserted after WAK has been released until 50 ns have elapsed.

4.6. SINGLES MODE

Although this module is designed with coincidence experiments in mind, a mode exists for collection of singles data. When bit 13 is set in control register 1 (see Section 2.5), the module behaves in a fashion that can be used to collect a singles spectrum for a particular input or several inputs. The major distinction of singles mode is that no clear is required to reset the module once readout has completed. The module performs its own clear. This enables one module to be read out and cleared without affecting any other modules in the chain. A second distinction of the singles mode is that data is read out after each conversion completes unless another channel within the module has a pulse ready to convert. If another channel has data ready, it is also converted before readout occurs. In coincidence mode, readout will not occur until the master gate has returned low; however, when the singles mode is enabled, the master gate has no "grouping effect." Data readout is immediately initiated by a module when conversion is complete regardless of the state of the Master Gate. All readout modes are available in singles mode; however, the random access CAMAC readout will not automatically generate the clear signal when the last datum is read. Normally, the master gate is disabled on units that are placed in singles mode by setting bit 5 of control register 2. Then, if singles data collection is desired in selected modules in a readout chain, the unselected modules can be inhibited by suppressing the gate input to the FERA driver. In a readout chain, either singles mode or coincidence mode should be used in all modules, *not* a combination of modules in singles mode and coincidence mode.

5. MAINTENANCE AND ADJUSTMENTS

There are two adjustments that may be made by the user of the AD413A ADC module: the upper-level discriminator setting, and the individual offset adjustment for each channel.

5.1. UPPER-LEVEL DISCRIMINATOR

The upper-level discriminator (ULD) setting is determined by potentiometer R27. See Main Component Assembly Drawing at the end of this manual. To set the ULD to an appropriate value, measure the voltage from U17 pin 3 to ground with a voltmeter. Adjust R27 until the voltage at U17 pin 3 corresponds to the desired ULD setting.

5.2. INDIVIDUAL OFFSET ADJUSTMENT

Each linear input on the AD413A has an offset adjustment, which may require adjustment on occasion. The offset adjustment is located on the stretcher boards. A1 is the stretcher board for input 1, A2 is the stretcher board for input 2, and so on. Once the appropriate board has been located , locate R1 on the stretcher board by referring to the Stretcher Component Assembly Drawing. With nothing connected to the input, measure the voltage between U5 pin 6 on the stretcher board and ground. Adjust R1 until the voltage is 0 V. On occasion it may be desirable to set the offset to something other than 0 V. For correct operation, the offset should not be set more than 20 mV from 0V.

APPENDIX A: RECOMMENDED CABLE COMPONENTS

Since each experimental system is unique, no attempt is made to supply standard cables to form an ECL bus readout chain. To build the necessary cables, the following will be required:

Control Bus Cable

Parts: 16-conductor ribbon cable with 0.050 inches between conductors.
3M part number = 3365/16

16-position header configured, two rows of 8 sockets.
3M part number = 3452-6006
AMP part number = 499497-3

Construction: Using a ribbon cable construction tool (3M 3698-08), place one header on the cable for each AD413A in the readout chain and one header for the FERA driver on the end. Headers should be positioned such that a minimum of cable separates the AD413As.

Data Output Cable

Parts: 34-conductor ribbon cable with 0.050 inches between conductors.
3M part number = 3365/34

34-position header configured, two rows of 17 sockets.
3M part number = 3414-6006
AMP part number = 499498-9

Construction: Using a ribbon cable construction tool (3M 3698-08) place one header on the cable for each AD413A in the readout chain and one header for the FERA driver on the end. Headers should be positioned such that a minimum of cable separates the A7778D413As.

Patch Cables (used for REN/PASS readout chain)

Parts: 2-position header for twisted pair cable.
AMP part number = 5-87456-3
Sockets for header.
AMP part number = 1-87756-8

Construction: Using a crimp tool (AMP 90202-2-N), crimp sockets on both ends of individual stranded wire. Take two such wires and tightly twist them to form a twisted pair cable. Plus the sockets into the header to form the cable.