Back

FURUNO

SERVICE MANUAL

ECHO SOUNDER

MODEL FE-700

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•Your Local Agent/Dealer

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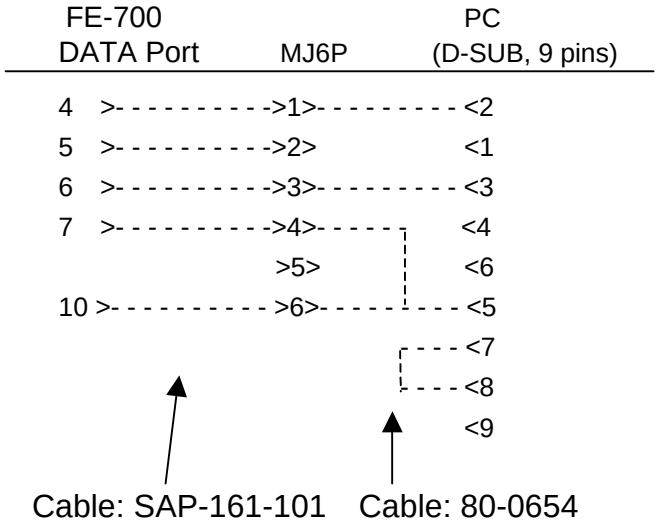
FE-700
(MAYA)

How to upgrade software

Necessary tools:
1) A DOS/V compatible PC (NEC PC98 cannot be used.)
2) OS: MS-DOS/Windows 95/98
3) Interconnection cables: 80-0654 and SAP-161-101
4) New Software

Fabricate the interconnection cable between the monitor unit and the PC as below.



1. New software supplied is a self-extracting file. Make a new file on the PC, copy a file supplied, fe700vx.exe to the new file, then, double-click the fe700vx.exe icon. Nine files are extracted.

   Up700.bat, load600.b, load600.b96, uppg.exe, dummy.b, boot600.bin, upboot60.bat, fe700t1.bin, update.txt

2. Copy these files to a floppy disk to execute the program from the floppy disk.
3. Connect the DATA port on the FE-700 display unit to the serial I/O port of the PC.
4. Turn on the PC. Do not as yet turn on the FE-700.
5. Select MS-DOS prompt in the program file to run MS-DOS program.
   C:¥windows> appears.
6. Insert the program disk and type **A:**, followed by Enter key.
   A:¥> is on the screen.
7. Type **up700** and press Enter key.

8. Select baud rate “2:19200.”
   “TARGET power on” comes on the PC screen.
9. Turn on the FE-700.
10. Wait for about 6 minutes.

    The PC screen shows the progresses of updating. When loading of new software is completed, “Finish version up.ted” appears on the PC screen while the FE-700 shows normal picture.

11. Turn off the FE-700 and the PC to disconnect the cable.

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Information

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WRITTEN BY

Addenda No.2 to Service Manual for FE-700. Pub No. SME-23660

FE-700
Capacitor with Wrong Polarity

②

E/S
FCV

Following capacitors are fitted with wrong polarity. Change MAIN board and C4 on CONE board. If not, communication error between FE-700 and a printer/PC will result typically.

Unit	Board	Parts No.
Display unit, FE-701	MAIN, 02P6280A	C29
Distribution box, FE-702	CONE, 02P6283	C4

This information is applicable to the units having following serial numbers.

2232-0001 to 1860 (except for 1852), 1917, 1997,1998, 2061, 2063, 2064, 2259, 2275, 2297, 2305, 2306, 2308, 2306, 2309, 2331, 2333, 2345, 2347, 2348, 2364 to 2366, 2367, 2369, 2370, 2371, 2376, 2385, 2394, 2403, 2408 to 2416, 2419, 2423, 2428, 2435, 2436

Necessary parts

Parts name	Type	Code number	Remarks
MAIN board	02P6280A	001-229-670	C29 with correct polarity
Capacitor	ECA-1HM010B	000-135-484	For CONE board

Identification
The PCB is wrongly marked with a - sign. When the capacitor is placed with - sign on the board, the polarity is wrong. See next page.

Capacitors C4 and C29 are also marked wrongly in schematic diagrams, Dwg. Nos. C2336-K12-A and C2336-K03-A respectively.

Note:
When MAIN board 02P6280 is replaced with 02P6280A, ANLG board must be modified. Refer to FQ2-2003-001.

Factory-modified sets
From the production in September 2003

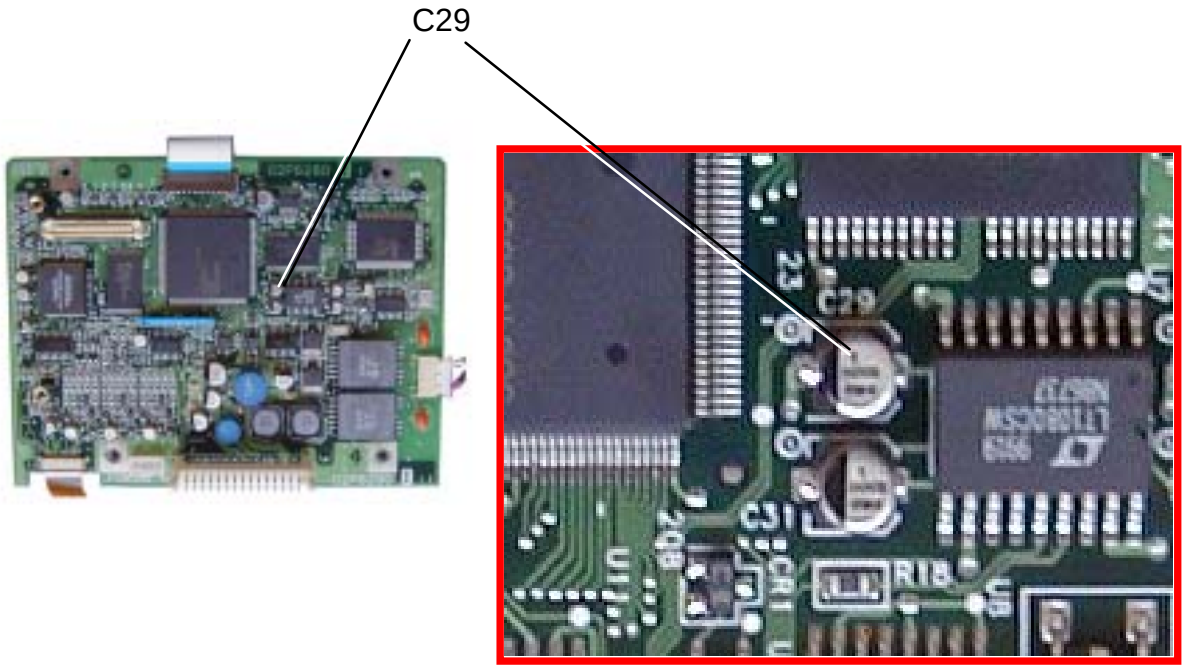


Figure 1 C29 on MAIN board (02P6280(A) with wrong polarity

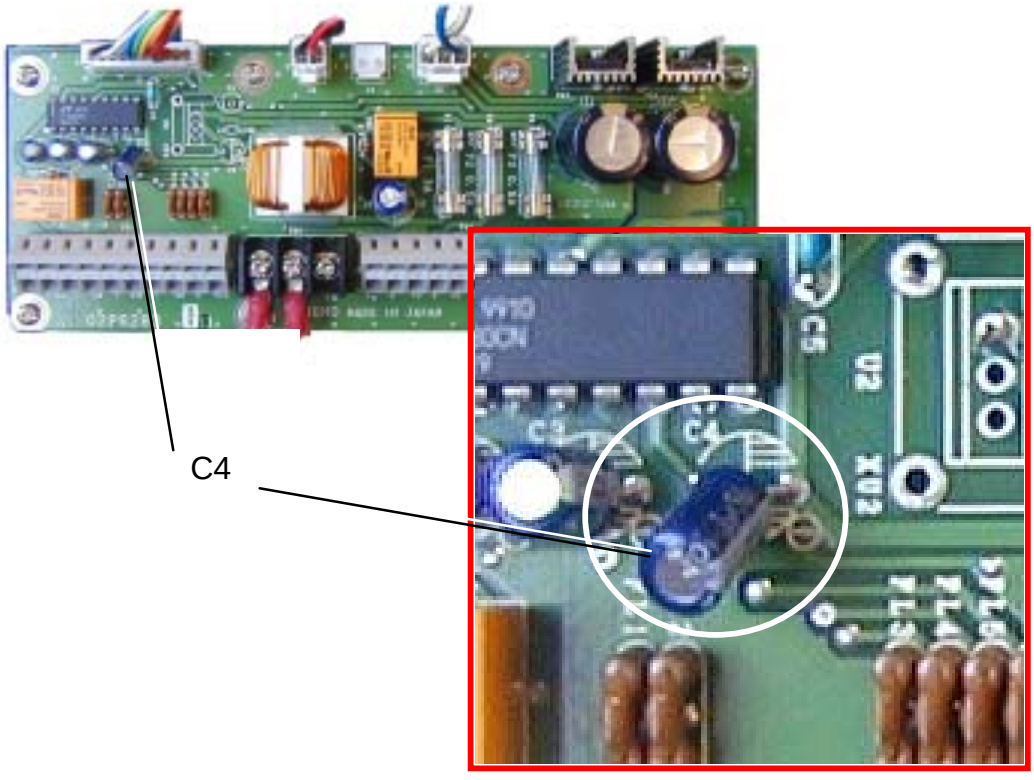
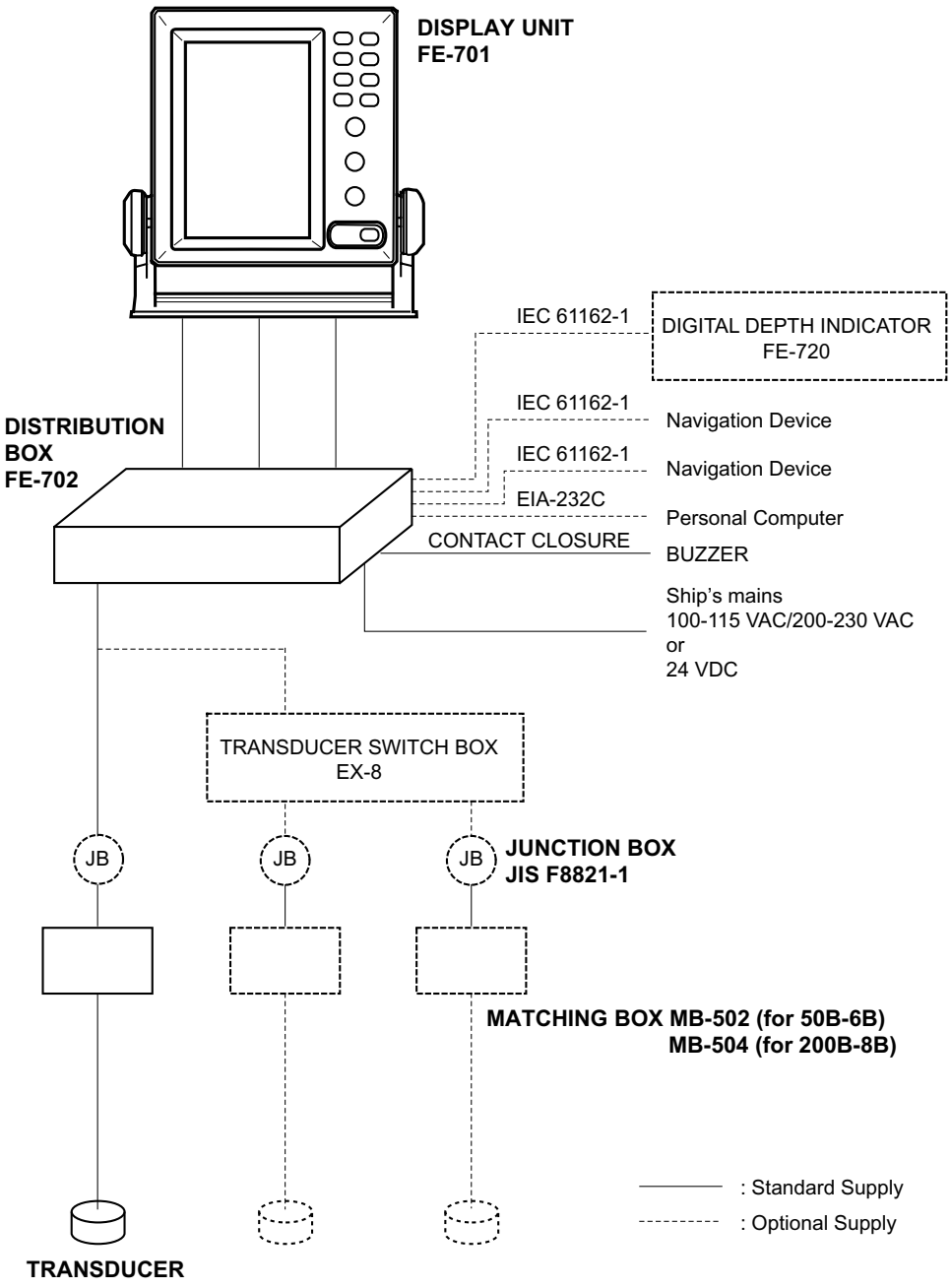


Figure 2 C4 on CONE board (02P6283) with wrong polarity

CONTENTS

SYSTEM CONFIGURATION

The FE-700 consists of Display Unit (FE701) , Distribution Box (FE702), Transducer Switching Box (EX-8) and Matching Box (MB-502/MB-504). The Switching Box and Matching Box connected to switching box are supplied optionally.



Chapter 1. Circuit Description

1.1 GENERAL BLOCK DIAGRAM

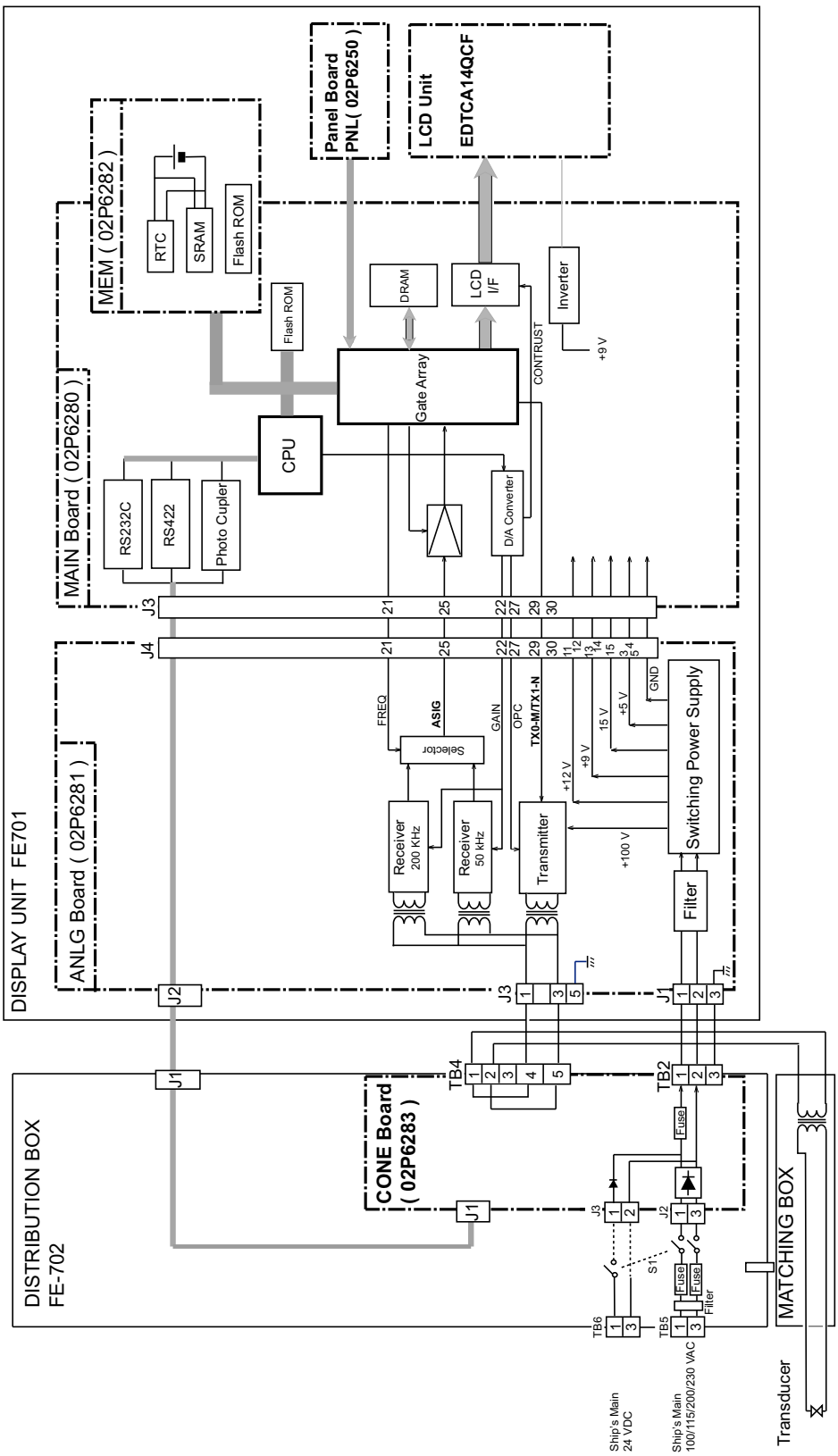


Figure 1.1 General Block Diagram

1.2 FUNCTION OF EACH UNIT

Display Unit (FE-701)

Board/Unit	Functions
MAIN Board (02P6280)	1) Processes depth signal by the CPU and the gate array, and converts them into the video signal. 2) Receives panel signal. 3) Detects the depth. 4) Generates the "SHALLOW DEPTH ALARM". 5) Includes a LCD I/F and an inverter for LCD backlighting. 6) Communicates with external equipment in IEC61162-1 and RS232C data format.
ANLG Board (02P6281)	Consists of a power circuit, a depth sounder circuit and an interface circuit.
PNL Board (02P6250)	Consists of keys, rotary switches, VRs, LEDs for panel illumination and a buzzer.
MEM Board (02P6282)	1) Memorizes the depth and time for 24 hours. 2) Contains a backup battery and a clock circuit.
Color Display (EDTCA14QCF)	Consists of an LCD and a cold cathode tube for LCD backlighting.

Distribution Box (FE-702)

Board/Unit	Functions
CONE Board	1) Interfaces the I/O signal between the Display Unit and External Unit. 2) Converts 100/115/200/230 VAC to 24 VDC for the Display Unit.

Matching Box (MB-502/MB-504)

Matches impedance between transmitter/receiver and transducer.

Transducer Switching Box (EX-8)

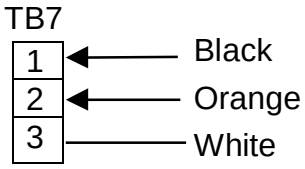
Selects the transducer to be used.

1.3 POWER SUPPLY

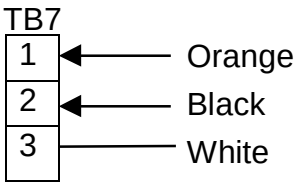
Either 24 VDC or 100-115/200-230 VAC ship's mains is connected to the Distribution Box.

The connection on TB7 must be changed depending on ship's mains, as follows.

1) When ship's main is 100 to 115 VAC;



2) When ship's main is 200 to 230 VAC;



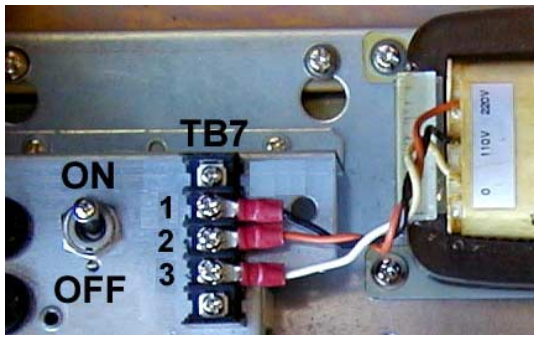


Figure 1.2 Connections on TB7

The AC supply voltage is converted to 24 VDC on the CONE board in the Distribution Box and supplied to the Display Unit and the Digital Depth Indicator.
The DP-ON signal (+5V) from the ANLG board activates the relay K2 on the CONE board in the Distribution Box, and then the 24 VDC is supplied to the Digital Depth Indicator through relay K2. See Figure 1.3.

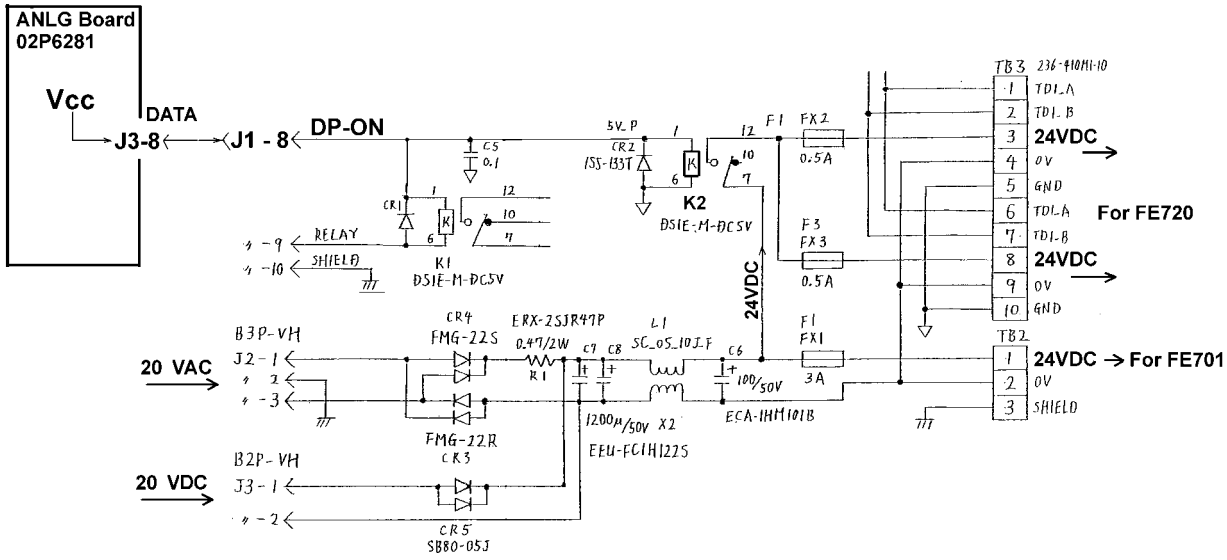
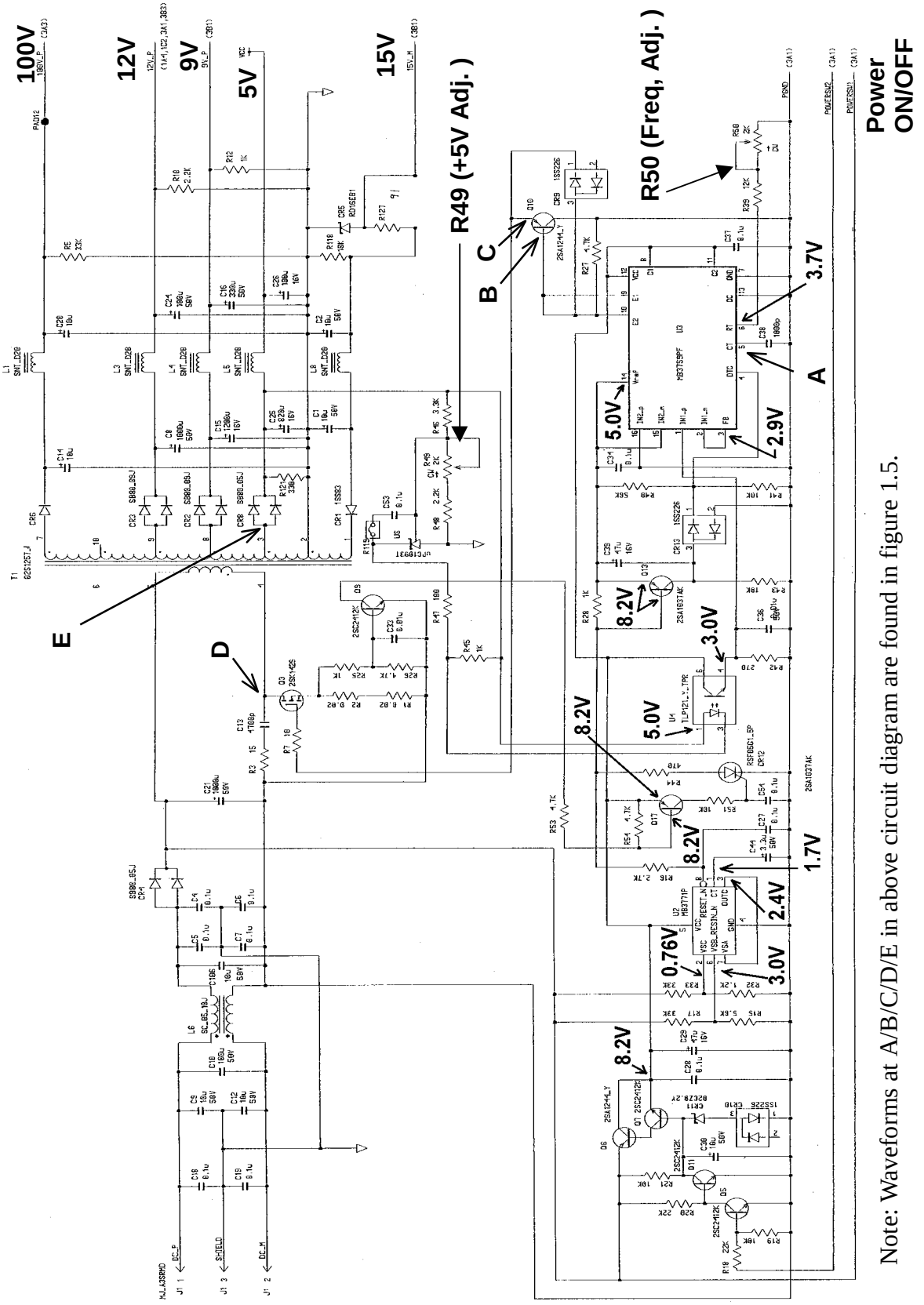


Fig. 1.3 Power circuit on the CONE board

Switching Regulator Circuit

The switching regulator on the ANLG board generates 100 V for TX amplifier, 9 V for LCD inverter and 15/12/5 V for other circuits.



Note: Waveforms at A/B/C/D/E in above circuit diagram are found in figure 1.5.

Figure 1.4 Switching regulator circuit on the ANLG board

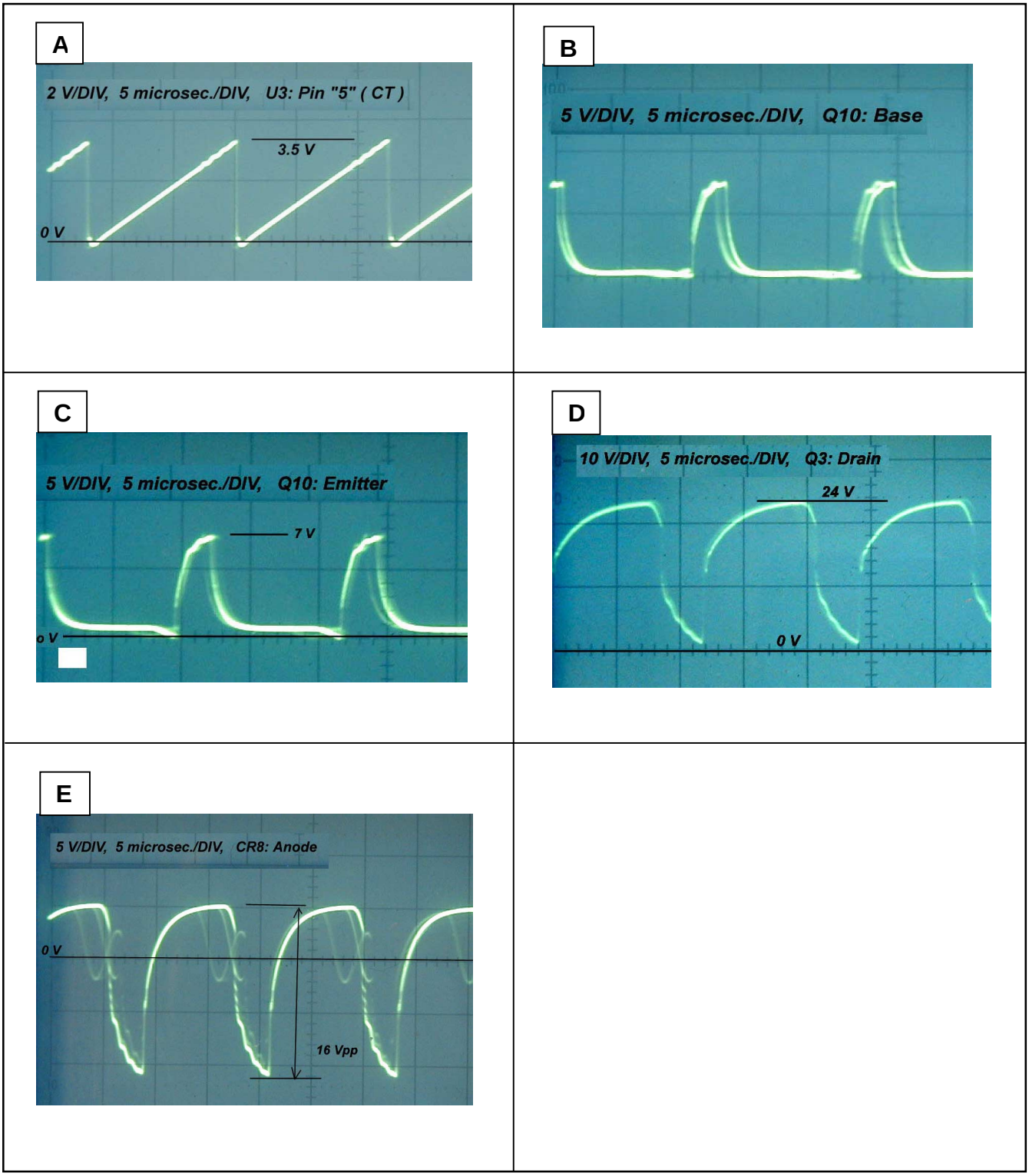


Figure 1.5 Waveforms at A/B/C/D/E on the switching regulator circuit.

1.4 TRANSMISSION CIRCUIT

The transmission amplifier circuit is commonly used for both frequencies, 50/200 kHz. The transmission frequency is set on the System Menu 3. Transmission carrier signal "TX0/TX1" are generated by Gate Array U10 on the MAIN board 02P6280 and supplied to the TX driver circuit. Figure 1.6 shows the transmission amplifier circuit.

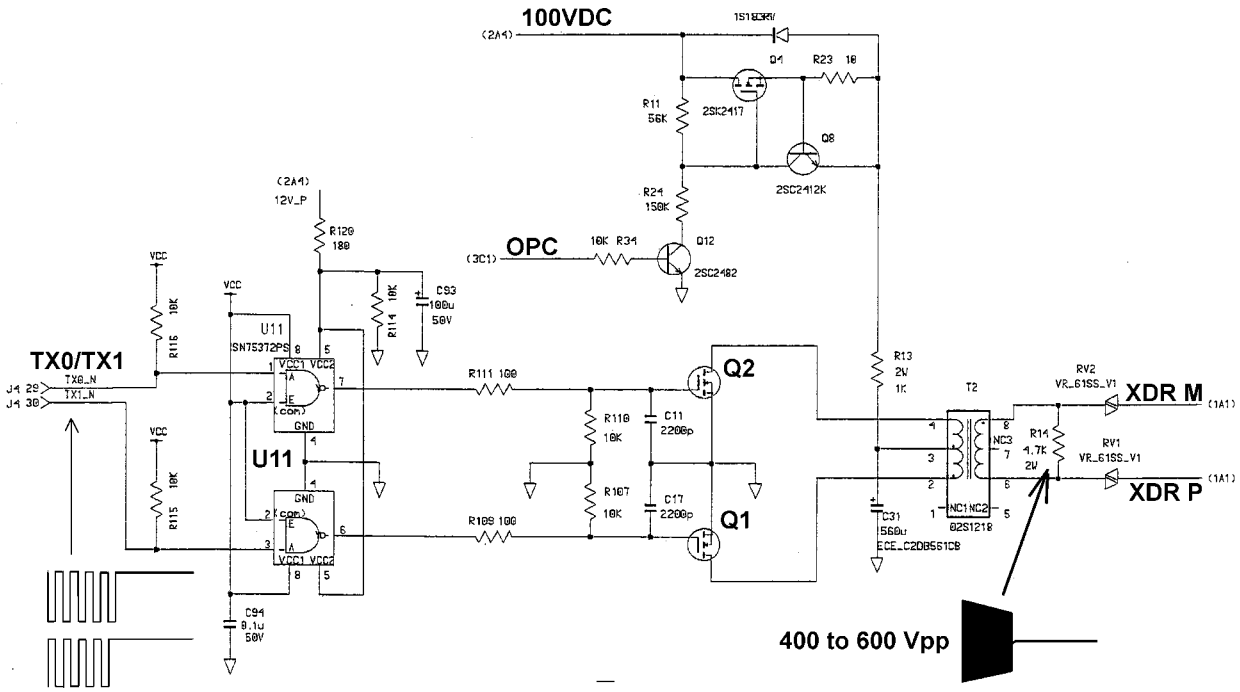


Figure 1.6 Transmission Circuit on the ANLG Board

1.5 RECEIVING CIRCUIT

The received signal is amplified by the Log Amplifier Circuit. Both 200 and 50 kHz RX circuits are located on the ANLG board and the one of RX circuits is selected by U9 in accordance with the System Menu 3 setting.

Figure 1.7 shows the receiving amplifier circuit.

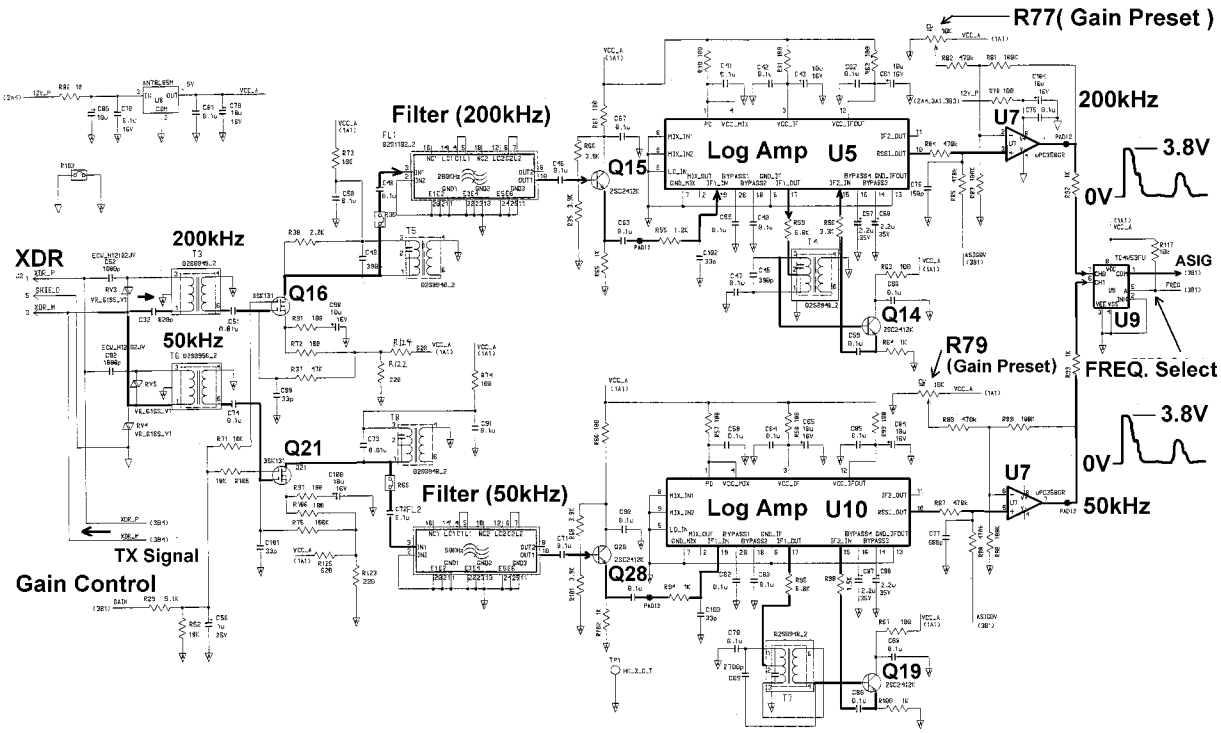


Figure 1.7 Receiving amplifier circuit on the ANLG board

Gain Control Circuit

Figure 1.8 shows the gain control circuit. The gain VR setting is detected by the CPU as binary code data "000 to 255" which is converted to DC gain control voltage by the A/D converter U5. The gain control voltage (1.9 to 3.8V) controls the amplitude of Q16/Q21 in the receiving circuit.

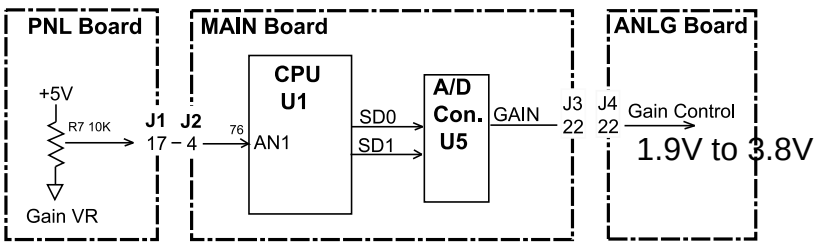
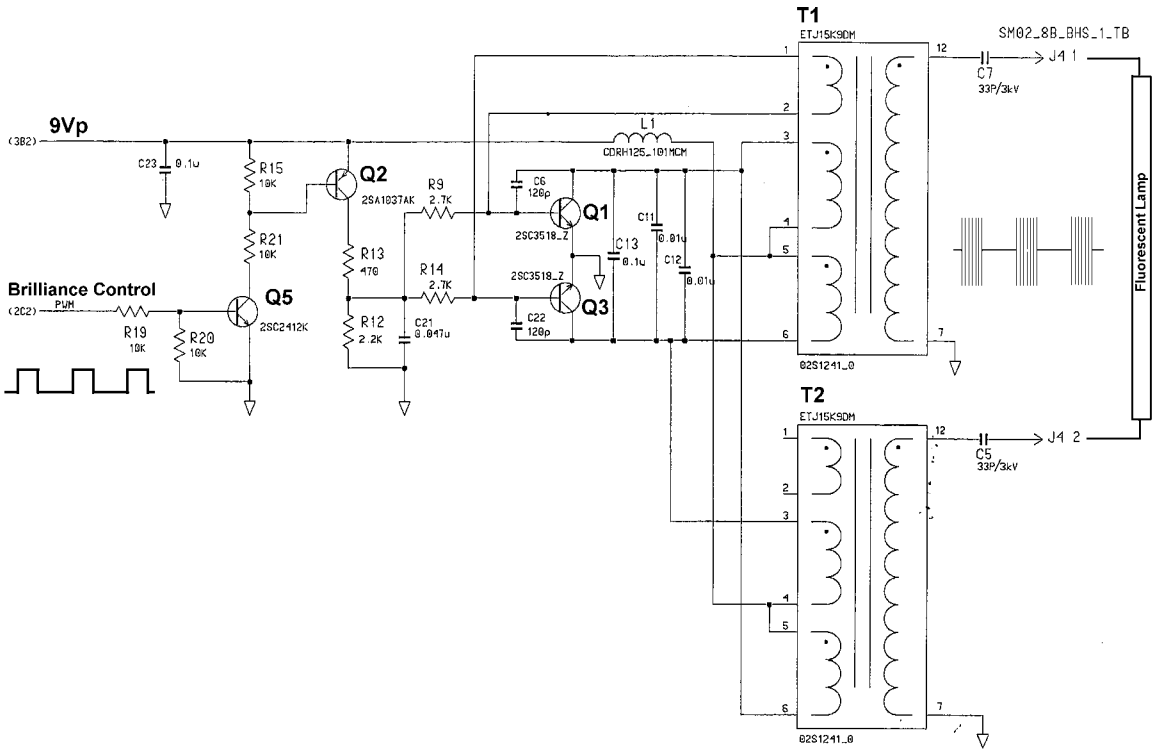


Figure 1.8 Gain control circuit

1.6 DISPLAY

The TFT LCD module is employed for the presentations. The control circuit and fluorescent lamp for backlighting are molded in the LCD unit "EDTCA14QCF". The life of the fluorescent lamp is approx. 20,000 hours if it is used with max. brightness.

High voltage for LCD backlighting is generated on the MAIN board and is outputed from J4-#1 and #2 to the LCD unit. Figure 1.9 shows the LCD inverter circuit. The output level between J4-#1 and #2 is approx. 1.6 to 2.0kVpp when LCD unit is connected.



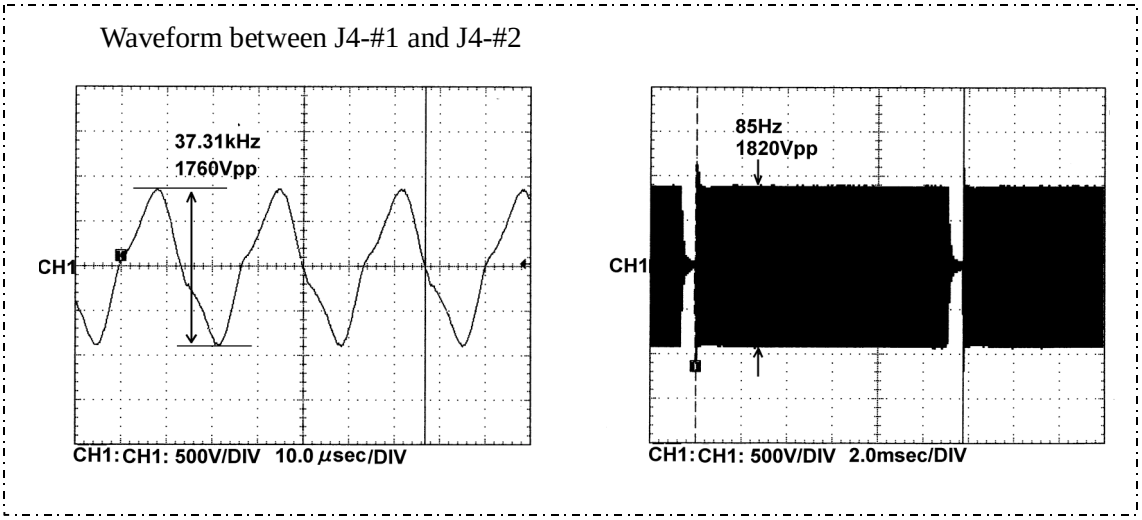


Figure 1.9 LCD inverter circuit on the MAIN board

I/O Signals of LCD Module

Pin	Signal	Specification/Function
1	STH1	Source Driver Start Pulse 1 (When RL is High)
2	OEH	Pulse for switching the output current of the Source Driver
3	Q2H	Control signal for switching the Video Data for the Source Driver
4	CPH1	Source Driver Sampling Pulse 1
5	CPH2	Source Driver Sampling Pulse 2
6	CPH3	Source Driver sampling Pulse 3
7	GND	0 V
8	BLUE	Video Signal (Blue)
9	GREEN	Video Signal (Green)
10	RED	Video Signal (Red)
11	VB	Controls buffer current of Source Driver Output
12	RL	+3V (change left/right shift direction)
13	STH2	Source Driver Start Pulse 2
14	VEE	Positive source voltage (+5V) for the Source Driver
15	Vcom	Applied voltage for facing electrode(amplitude changes with brightness control)
16	VGH	+12V for the Gate Driver
17	VDD	+3V for the Source Driver and Gate Driver
18	STV2	Gate Driver Start pulse 2
19	OEV	Selects the output of the Gate Driver (H: VGL output)
20	CPV	Clocked pulse for the Gate Driver
21	UD	-15V (change upper/lower shift direction)
22	STV1	Not Used
23	VSS	Negative source voltage(-15V) for Gate Driver
24	Vgoff	Gate Off voltage (The level is changed by Brightness Adjuster)

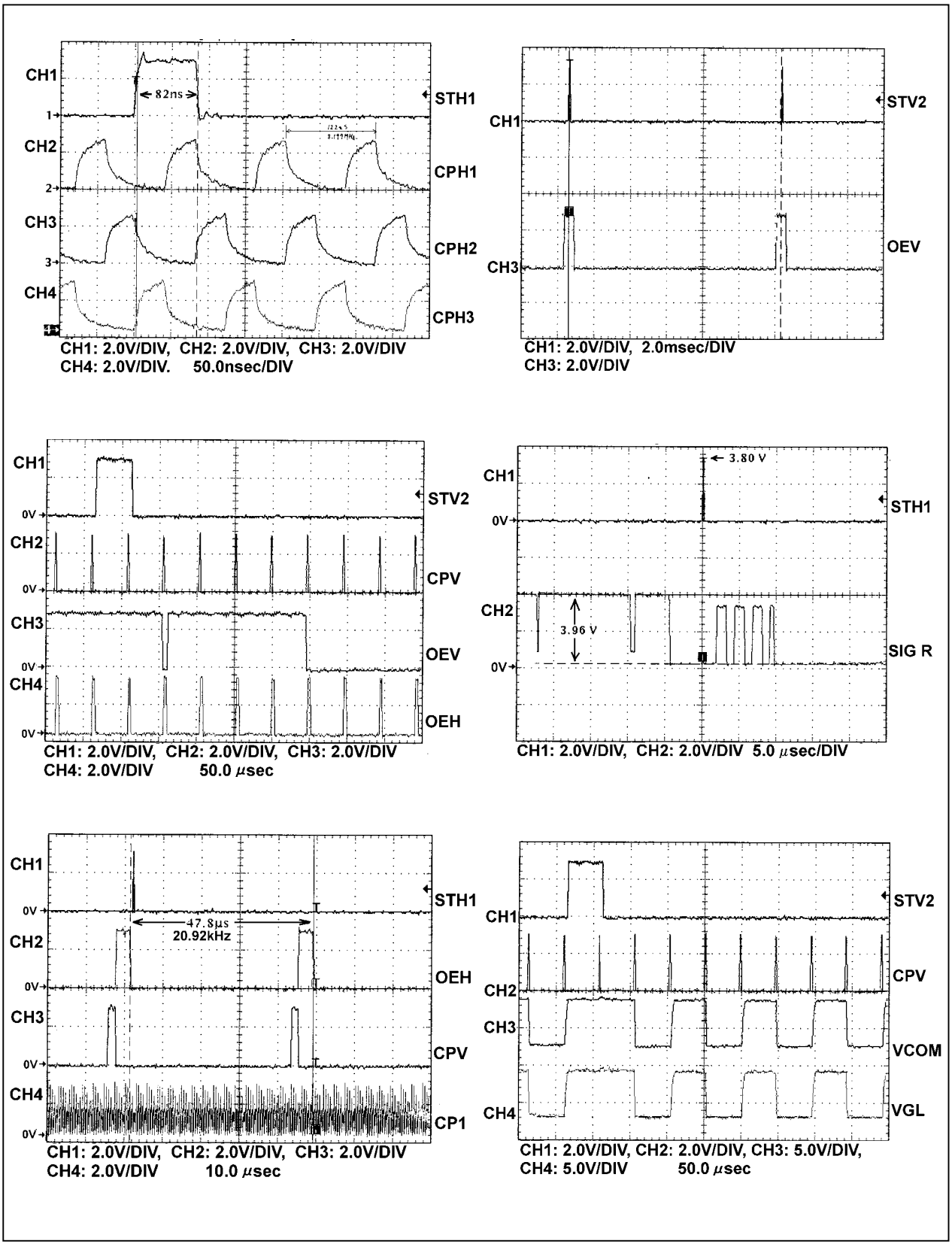


Figure 1.10 Output Waveforms from LCD interface circuit

Chapter 2. Maintenance

2.1 ADJUSTMENT

ANLG board

	Measuring Point	Ratings	Adjuster
Vcc (+5V)	J5, #3 and GND (TP1)	+5±0.02 V	R49, ANLG Board
Switching frequency	U3,#9 and U3, #7 (GND)	83.4~83.8 kHz	R50, ANLG Board

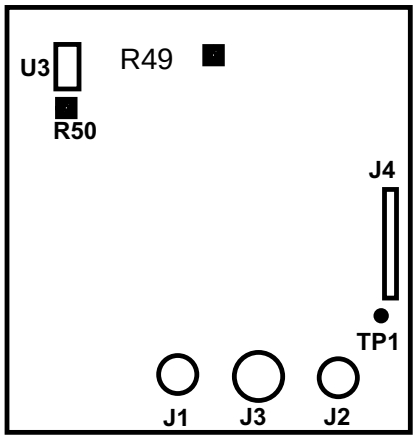


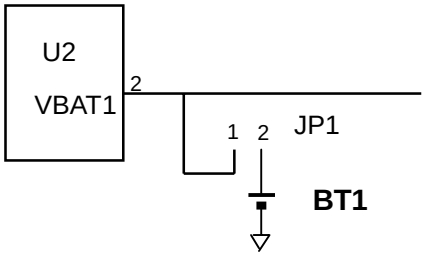
Figure 2.1 Adjuster on the ANLG board

2.2 REPLACEMENT OF LITHIUM BATTERY

The battery on the MEM board must be replaced when the low battery alarm appears on the display.

Note: Before removing the battery, disconnect JP1.

Type of Battery	Code No.
CR2450-F2ST2	000-133-495



WARNING!

Take care to avoid external short-circuiting of the battery. A sustained high-rate of discharge could create a ***burn or fire hazard!***

Figure 2.2 Memory Backup Circuit on the MEM board

Chapter 3. Troubleshooting

3.1 DIAGNOSTIC TEST

Function Test

Function test is performed by the following key operation.

1. Press the POWER key while pressing any key.
2. Release the key when the optional mode selection display appears.
3. Press the [-] key to select the TEST.

The following display appears.

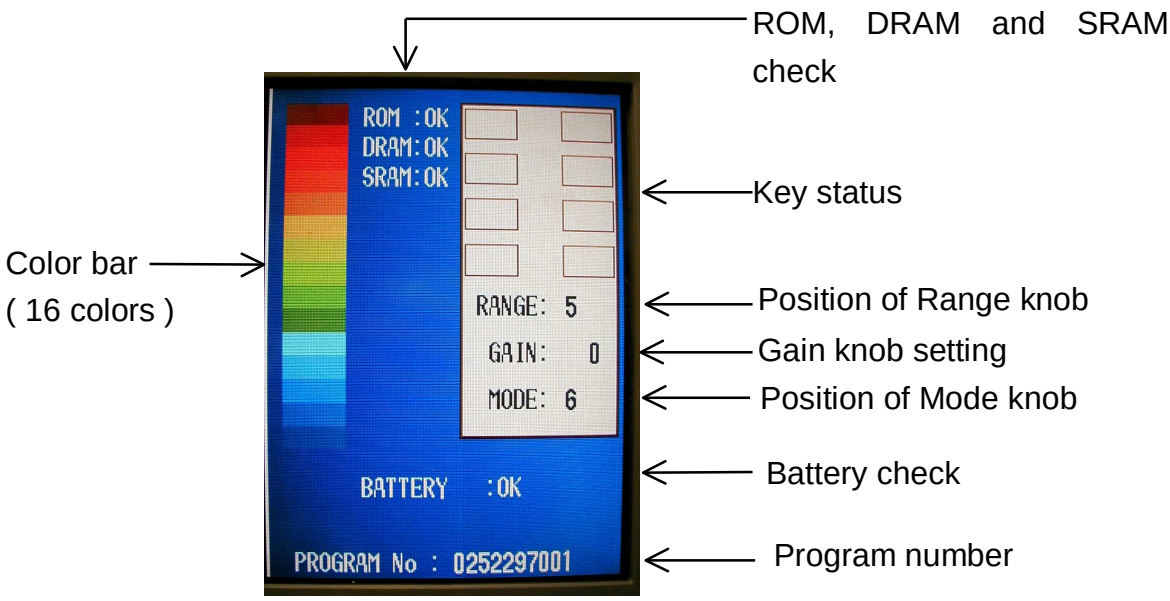


Figure 3.1 Test Screen

ROM, DRAM, SRAM and Battery check

The ROM, DRAM, SRAM and internal battery are checked and the results are displayed as OK or NG. If NG appears, following devices are suspected to be defective.

ROM NG : U14 of the MAIN board
DRAM NG : U16 of the MAIN board
SRAM NG : U7/U8 of the MEM board
Battery NG : Battery (BT 1) of the MEM board

Key status

Press and release each key (except the POWER switch) one by one. If the key is normal, its on-screen location lights in black while the key is pressed.

If some abnormal condition obtained, the PANEL and MAIN board are suspected to be defective.

Range, Gain and Mode knobs

Operate the controls. The RANG and MODE control setting indications should be the same as actual control settings. The GAIN control setting indication should be among 0 to 235-255.

If some abnormal condition is obtained by controlling the RANGE and MODE knobs, the PANEL or MAIN board (Gate array U10) is suspected to be defective.

If some abnormal condition is obtained by controlling the GAIN knob, the PANEL or U1 (CPU) of MAIN board is suspected to be defective.

Test Pattern

Self-test is performed by the following key operation.

1. Turn on the power while pressing any key.
2. Press the BRILL key three times. Press the BRILL key again to change the test pattern as below.

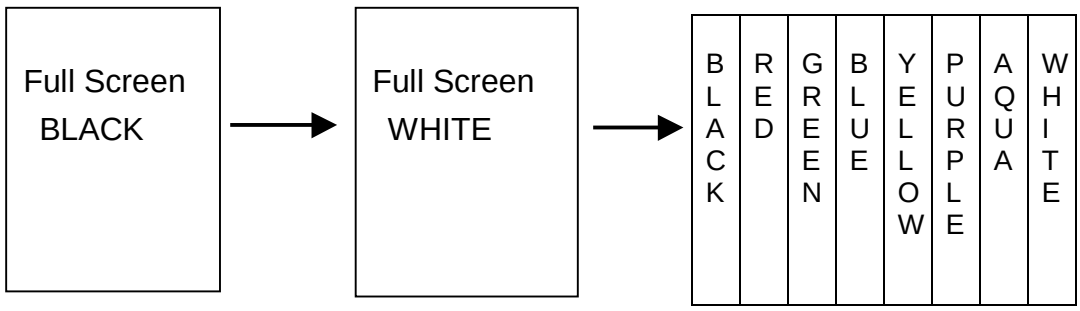


Figure 3.2 Test pattern

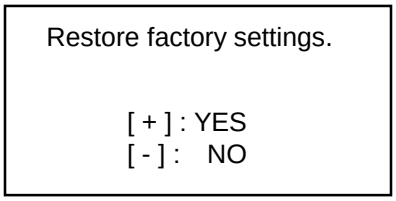
The " Full Screen BLACK/WHITE " checks the pixels of LCD.

The eight color gradation checks the R.G.B signals of LCD interface circuit on the MAIN board.

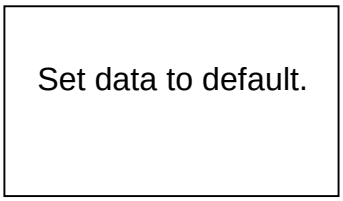
3.2 CLEARING THE MEMORY

To clear all data in the memory, follow the steps below.
Factory settings are restored after this operation.

1. Turn on the power while pressing any key. Release the keys when the optional mode window appears.
2. Press the [▲] key. The following window appears.



3. Press the + key to clear the memory. The following display appears while data is being cleared;



4. After cleared, the OPTIONAL MODE menu appears.

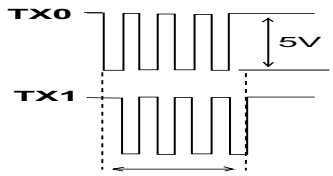
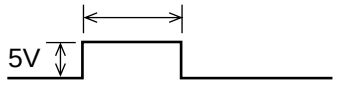
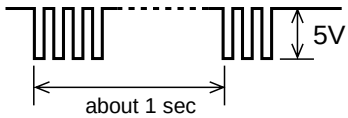
3.3 ALARM AND ERROR MESSAGE

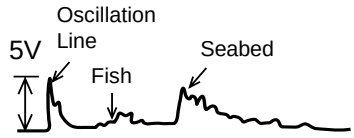
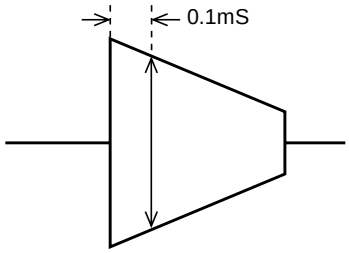
When the Lithium Battery voltage becomes less than 2.66V, **" LOW BATTERY ALARM"** message is displayed on the screen in red.

When the IEC61162 data is interrupted, **" EPFS ERROR"** message is displayed on the screen in red. The EPFS ERROR message is displayed only when DATA 1 screen of OS DATA display is selected.

When the depth becomes shallower than the set range, **" SHALLOW DEPTH ALARM"** message is displayed on the screen and the alarm sounds.

3.4 INSPECTION OF EACH BOARD

Board/Unit : MAIN board (02P6236)				
Signal	In/Out	Measuring Points	Measured by	Rating/Remarks
FREQ	Output	ANLG Board J4, #21 and GND	Oscilloscope	50 kHz :「H」 200 kHz :「L」 (L=0 V, H=5 V)
TX0/TX1	Output	ANLG Board J4, #29 and GND J4, #30 and GND	Oscilloscope	 Changes depending on range setting 1) TX0 and TX1 have opposite phase each other. 2) Frequency is equal to the TX frequency.
KP	Output	MAIN Board J6, #3 and J6, #4	Oscilloscope	Changes depending on range setting  Same timing as TX0 and TX1
GAIN	Output	ANLG Board J4, #22 and GND	Multimeter	Changes according to gain setting Setting「0」: about 1.9 V Setting「5」: about 3.1 V Setting「10」: about 3.8 V
IEC61162 TD-A , TD-B	Output	ANLG Board J4, #17 and #18	Oscilloscope	 Changes depending on data

Board/Unit : MAIN board (02P6236)				
Signal	In/Out	Measuring Points	Measured by	Rating/Remarks
Vcc	Power Line	J4, #3 and GND	Multimeter	+5±0.02V
+12 V	Power Line	J4, #11 and GND	Multimeter	+12.0±0.5V
+9 V	Power Line	J4, #13 and GND	Multimeter	+9.0±0.3V
-15 V	Power Line	J4, #15 and GND	Multimeter	-15.0± 0.5V
ASIG	Output	J4, #25 and GND	Oscilloscope	
Primary Power	Power Line	Q6 Collector and J4, #6 (P.GND)	Multimeter	About 9V
TX-H TX-C	Output	Across R14	Oscilloscope	Connect XDR and put into water. Shift : 0m Range : 200m 50kHz : 400~600Vpp 200kHz : 400~600Vpp 

Chapter 4. Parts Location

4.1 DISPLAY UNIT

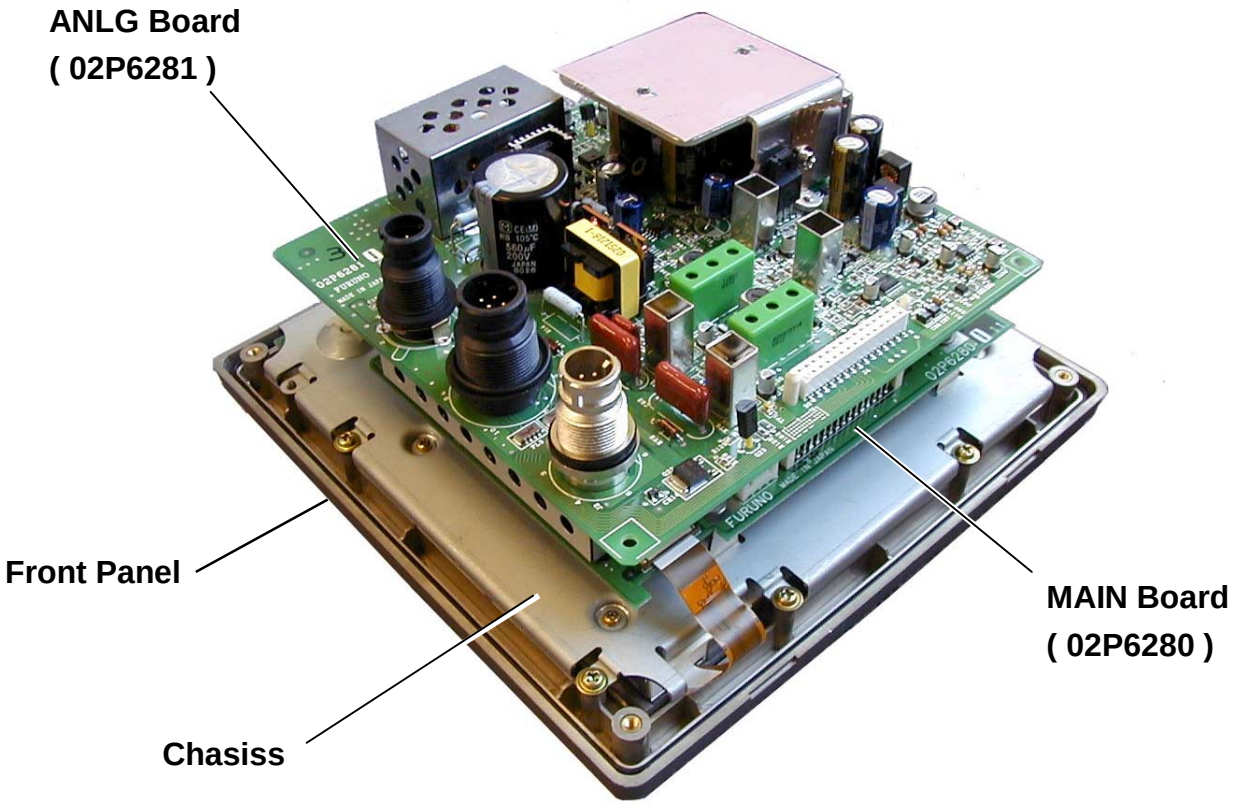


Figure 4.1 Parts Assembly

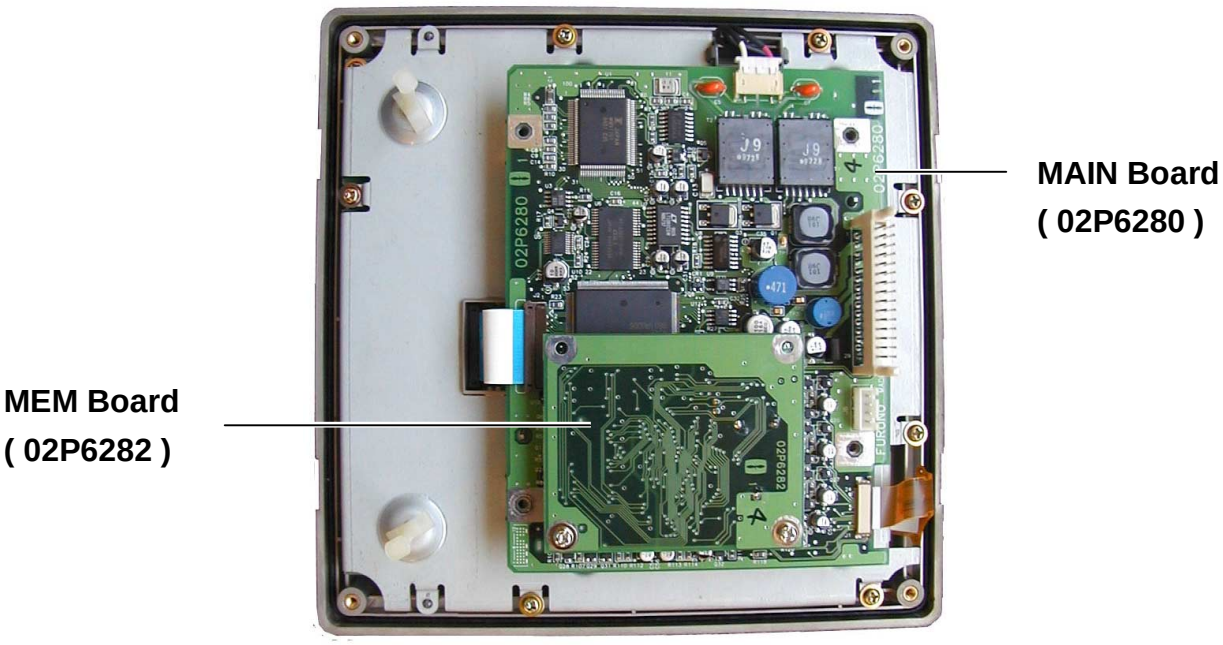


Figure 4. 2 Front Panel Assembly

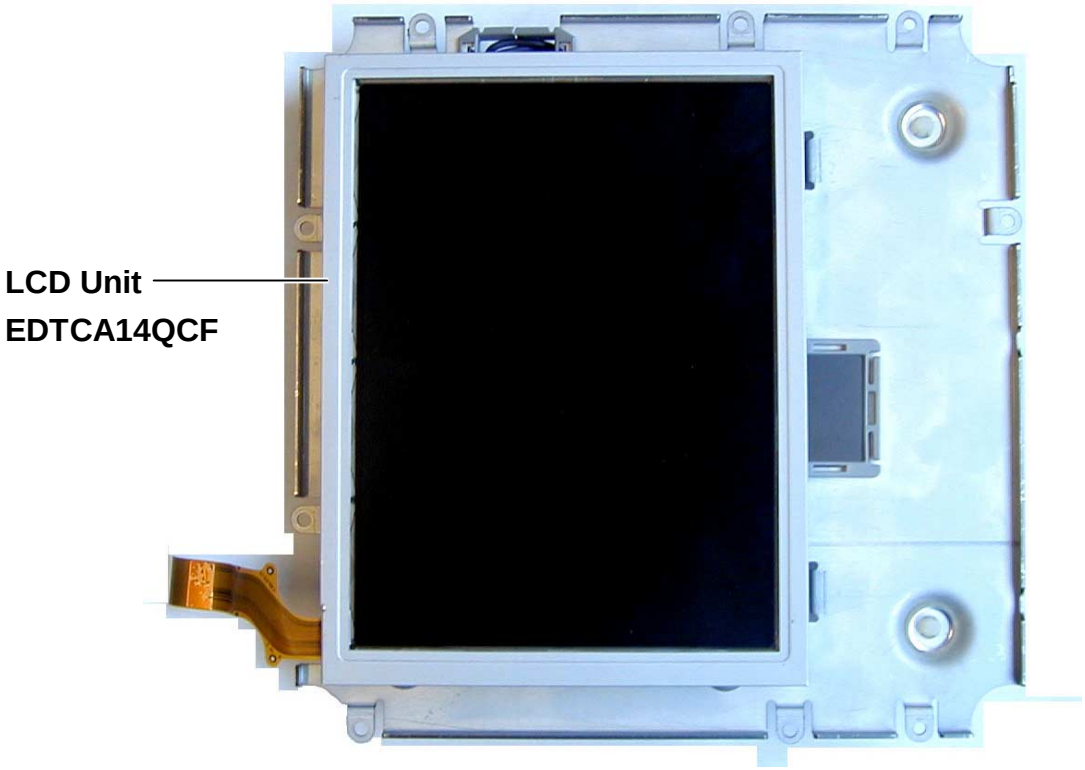


Figure 4.3 LCD Unit

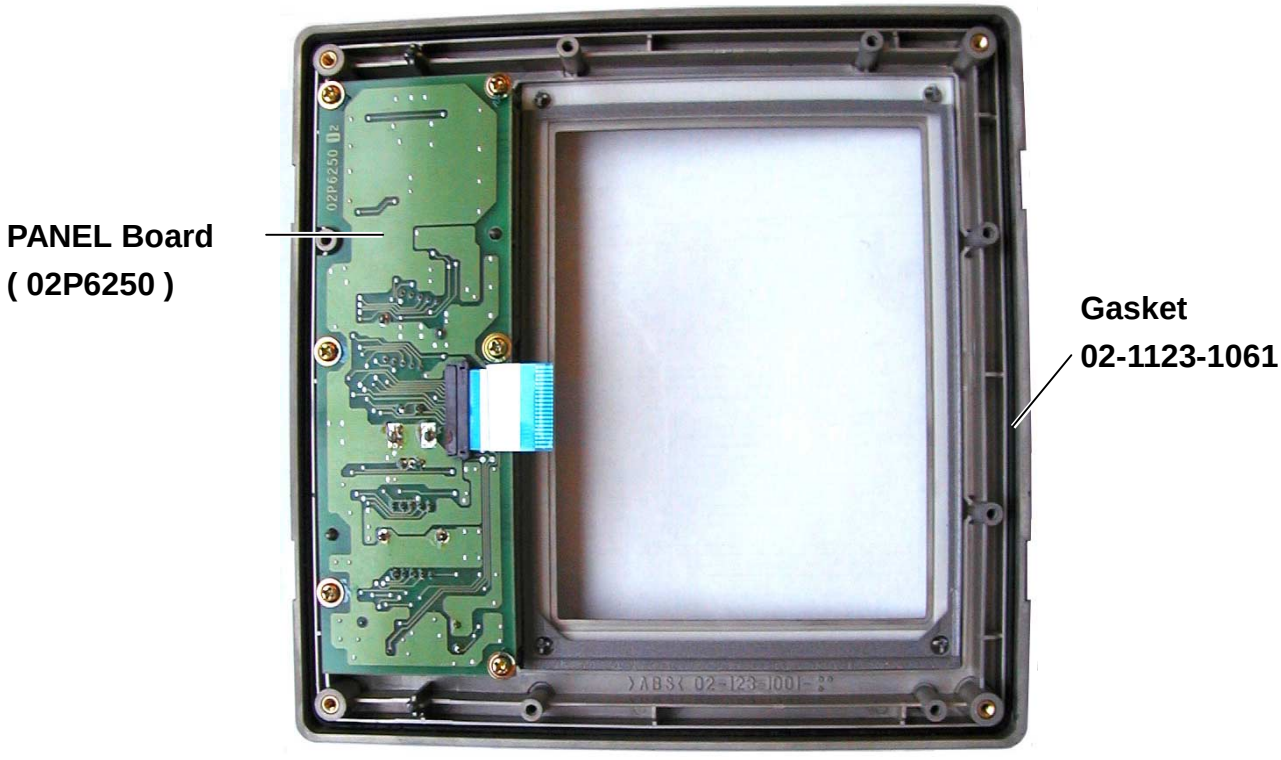


Figure 4.4 Front Panel

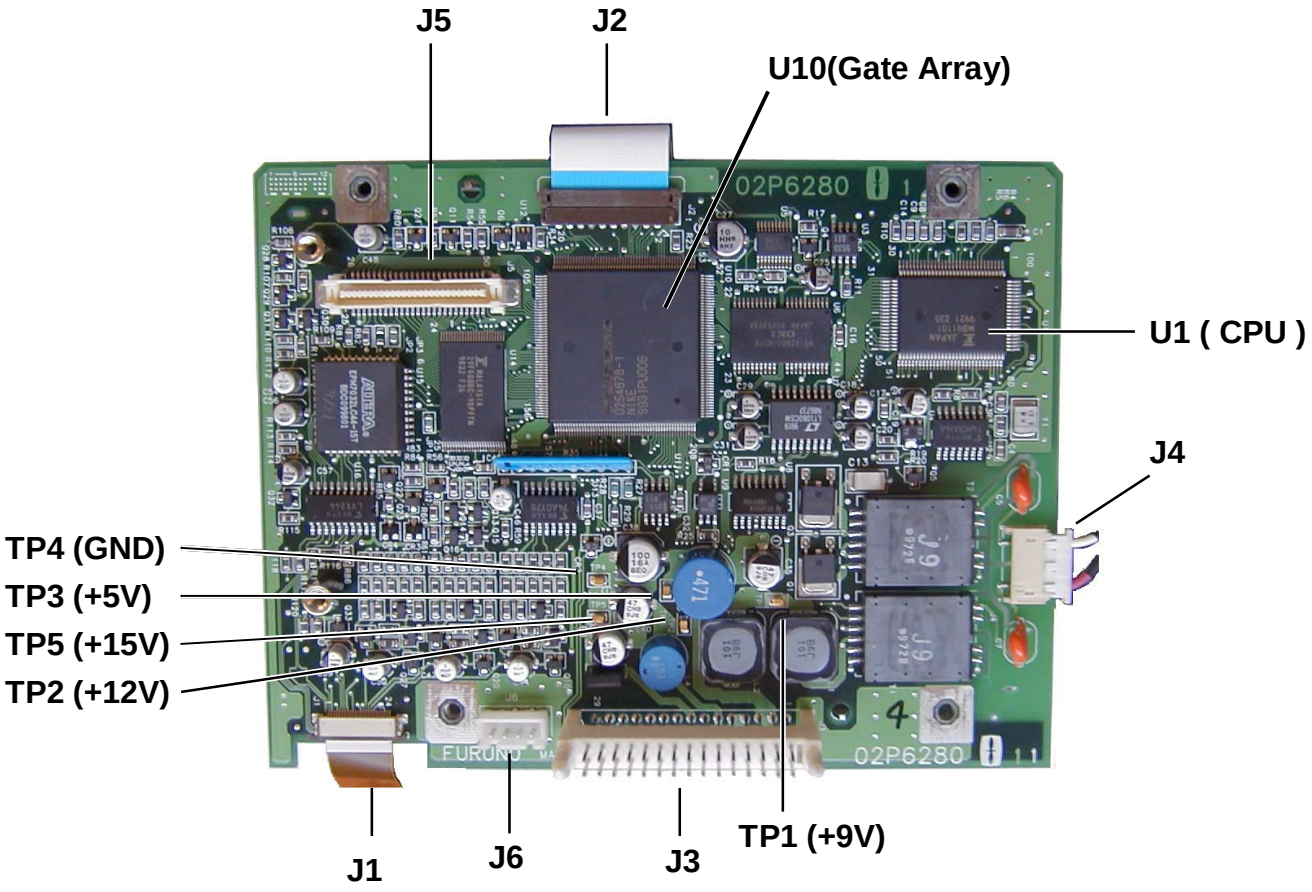


Figure 4.5 MAIN Board (02P6280)

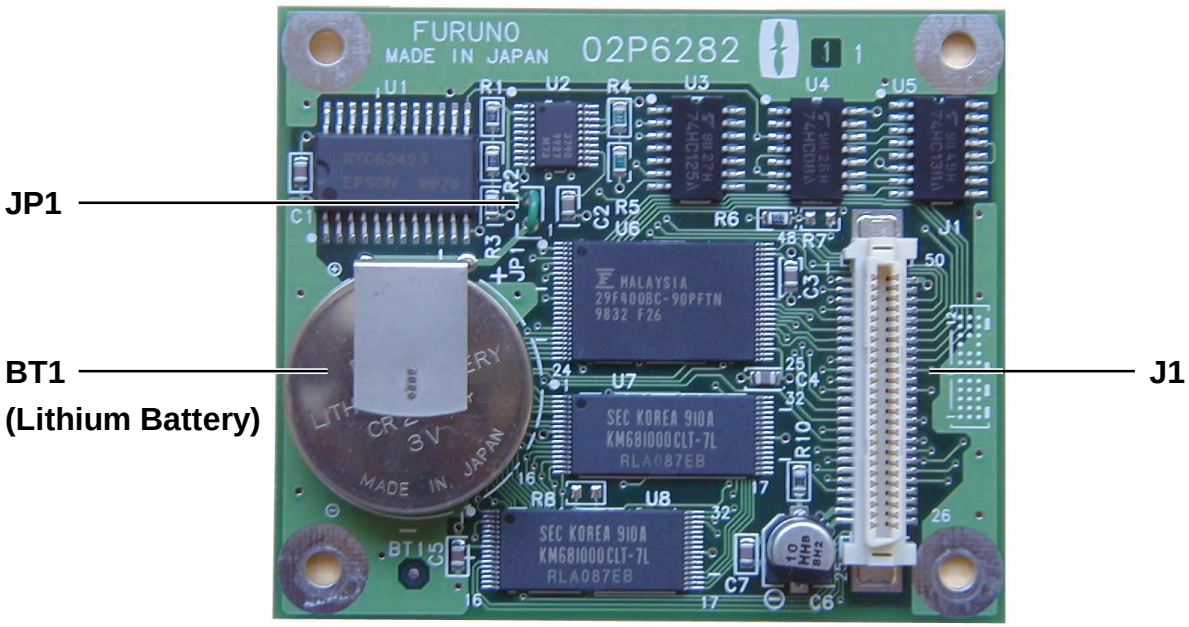


Figure 4.6 MEM Board (02P6282)

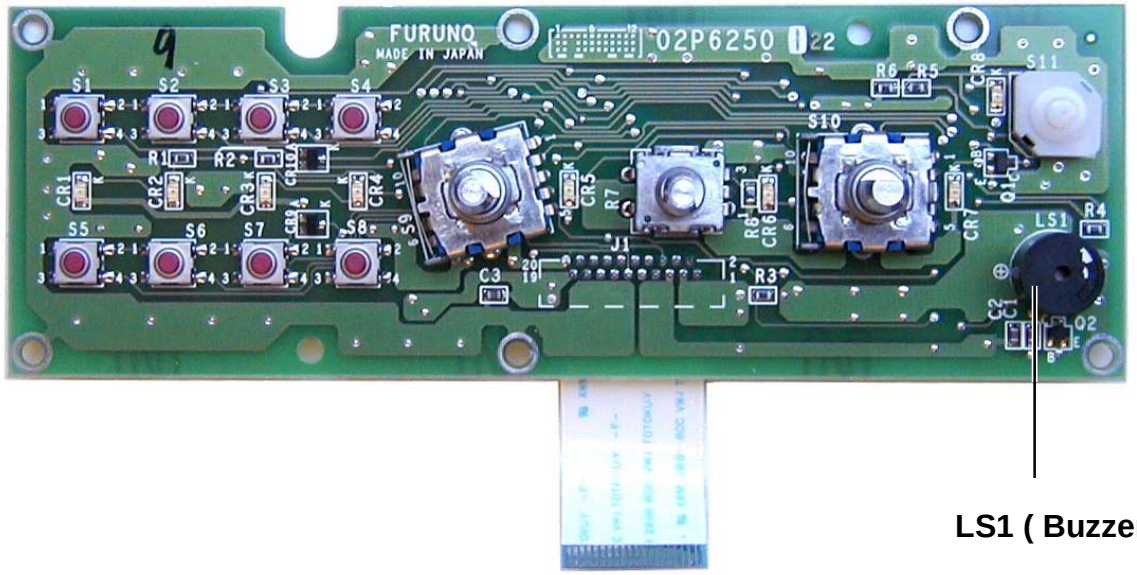


Figure 4.7 PANEL Board (02P6250)

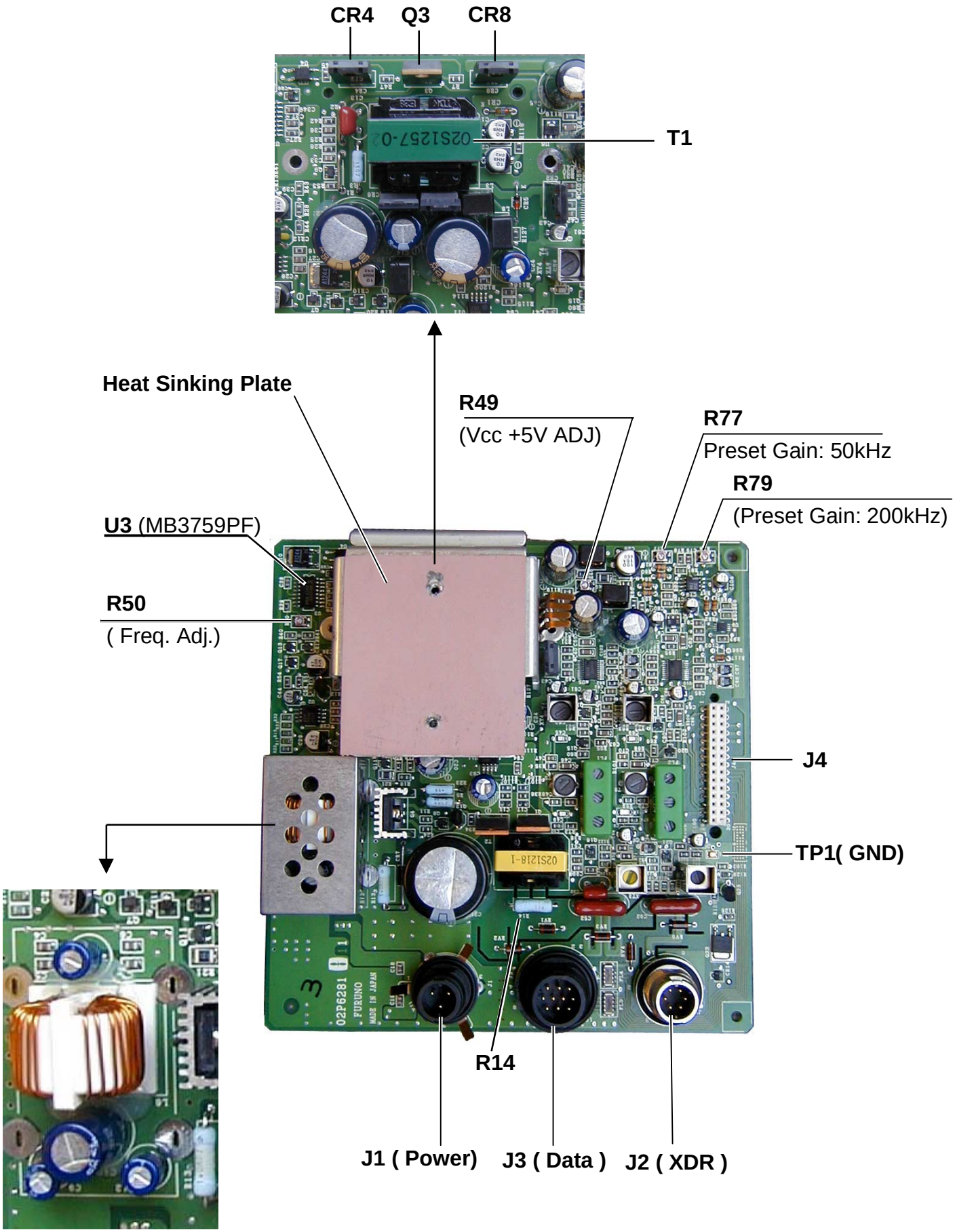


Figure 4.8 ANLG Board (02P6281)

4.2 DISTRIBUTION BOX

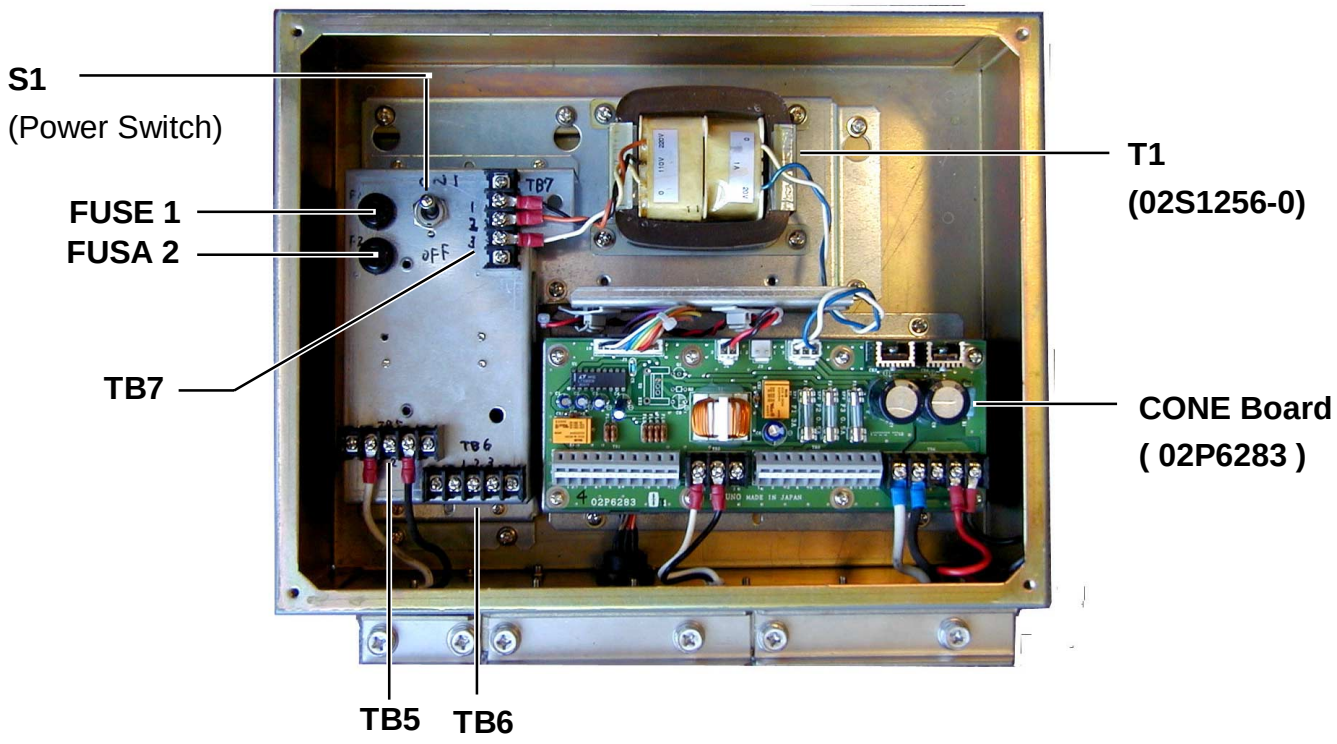


Figure 4.9 Distribution Box (FE702)

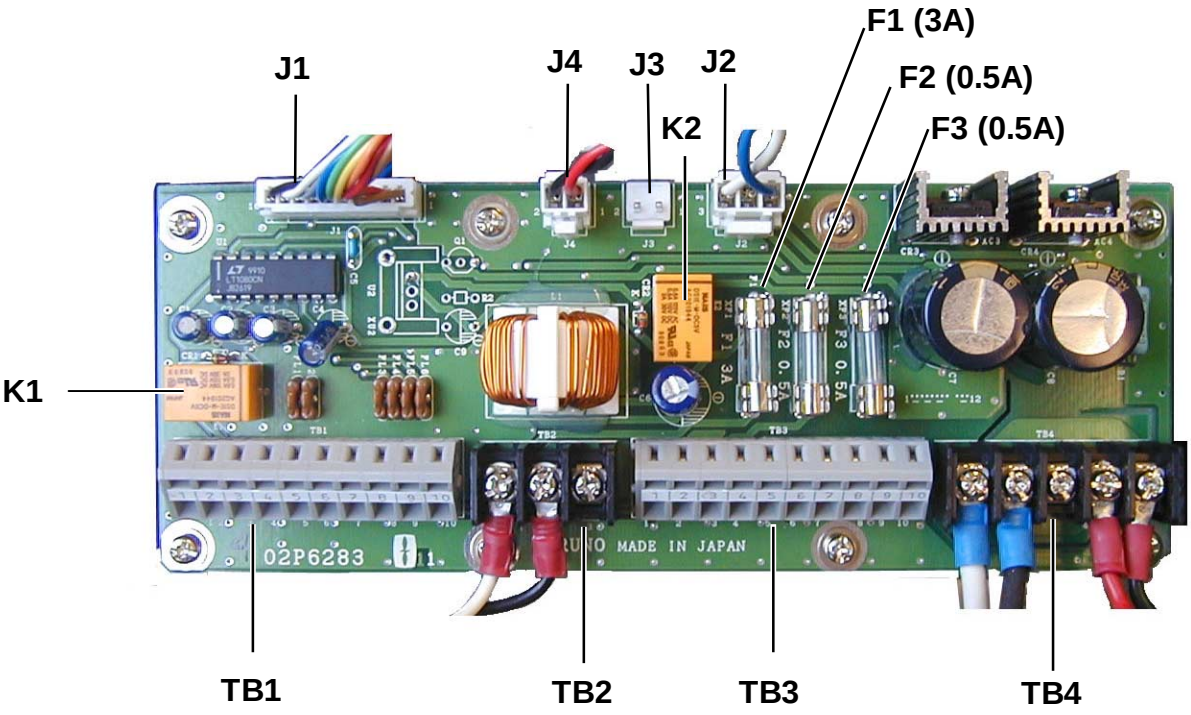
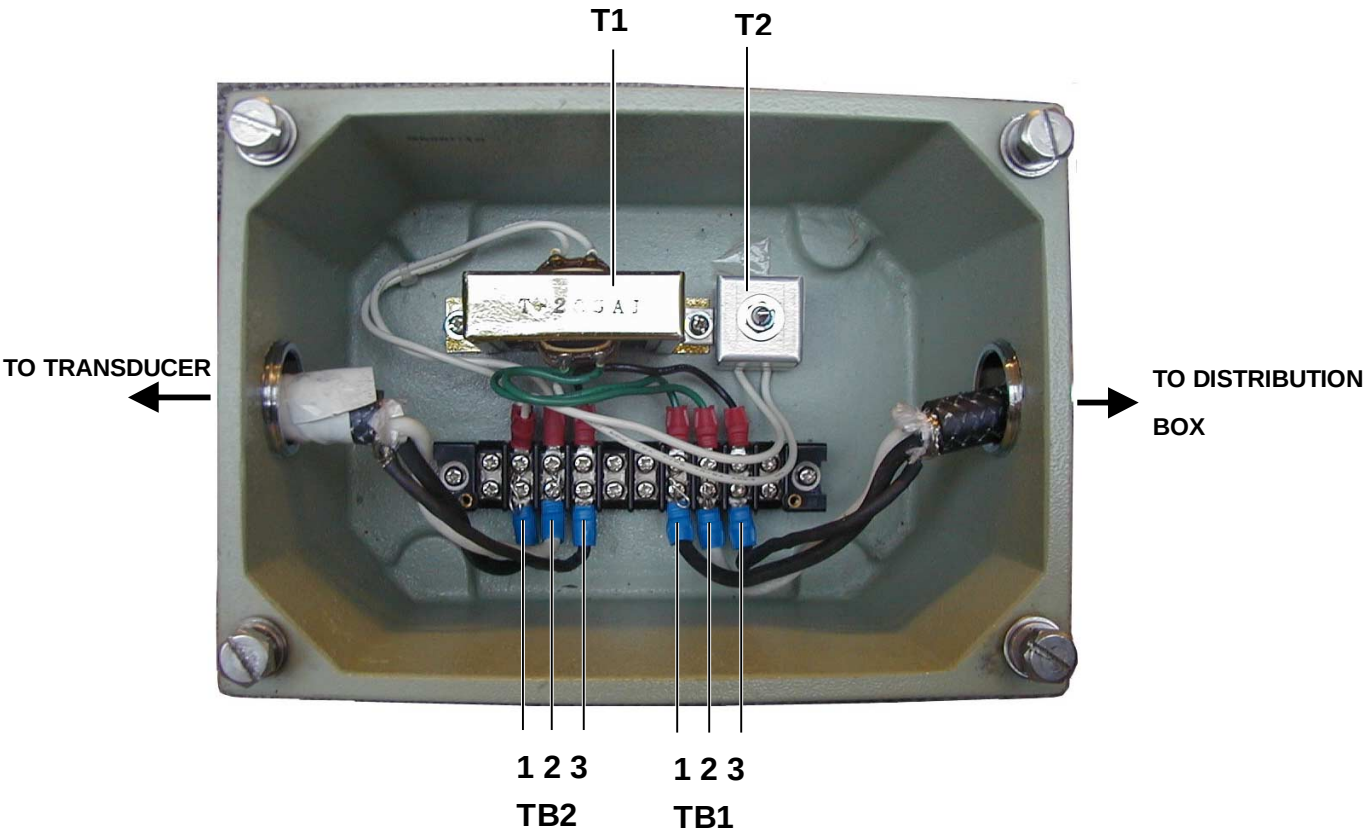


Figure 4.10 CONE Board (02P6283)

4.3 MATCHING BOX



FREQ	T1	T2	XDR
50 kHz	T-203BJ	T-204B	50B-6B
200 kHz	T-205AJ	T-206A	200B-8B

Figure 4.11 Matching Box (MB502)

4.4 SWITCH BOX

Figure 4.12 Switch Box, Front View

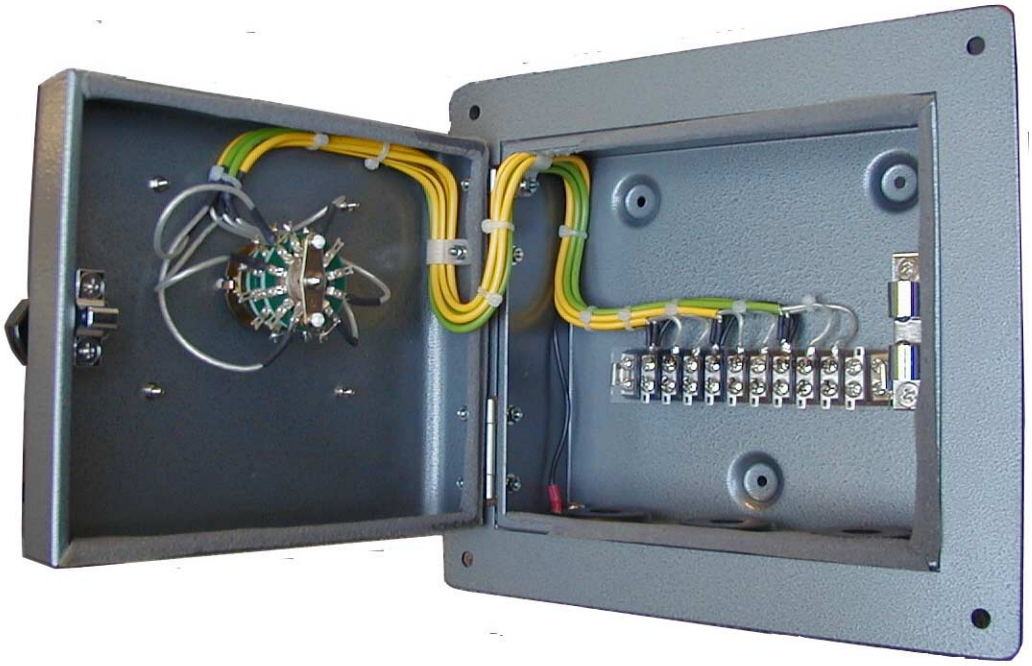


Figure 4.13 Switch Box, Inside View

Chapter 5. Digital interface (IEC 61162-1)

5.1 I/O SENTENCES

Input

RMA, RMC, GLL, GGA, VTG, ZDA

Output

DPT, DBS, DBT

5.2 SENTENCE DESCRIPTION

DPT - Depth

1MG Resolution A.224 (VII). Water depth relative to the transducer and offset of the measuring transducer.
Positive offset numbers provide the distance from the transducer to the waterline. Negative offset numbers provide the distance from the transducer to the part of the keel of interest.

$--DPT, x.x, x.x*hh<CR><LF>

- Checksum
- Offset from transducer, in meters = distance from transducer to water-line
- Water depth relative to the transducer, in meters

GLL - Geographic position - latitude/longitude

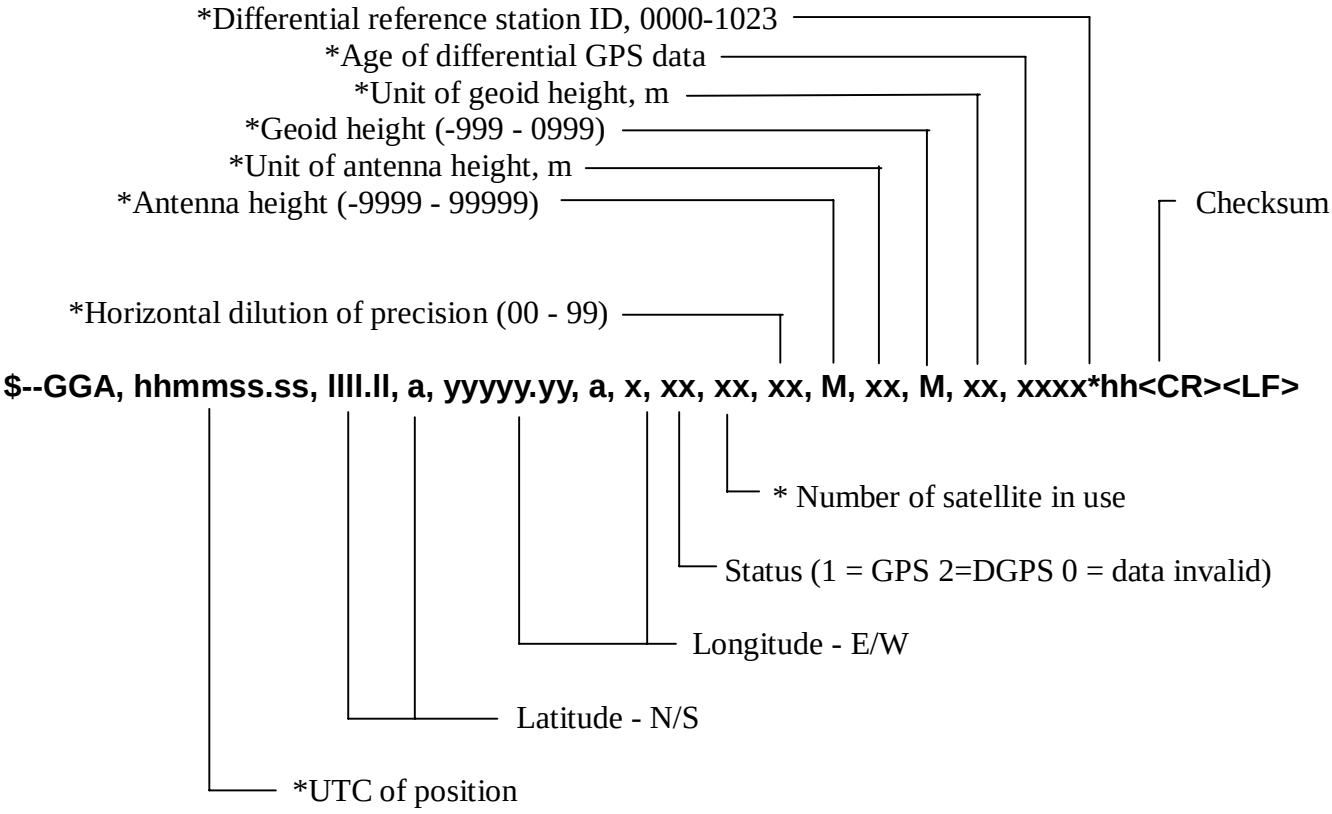
Latitude and longitude of present vessel position, time of position fix and status.

$--GLL, llll.ll, a, yyyyy.yy, a, hhmmss.ss, A*hh<CR><LF>

- Checksum
- Status (A = data valid V = data invalid)
- UTC of position
- Longitude, E/W
- Latitude, N/S

GGA - Global positioning system (GPS) fix data

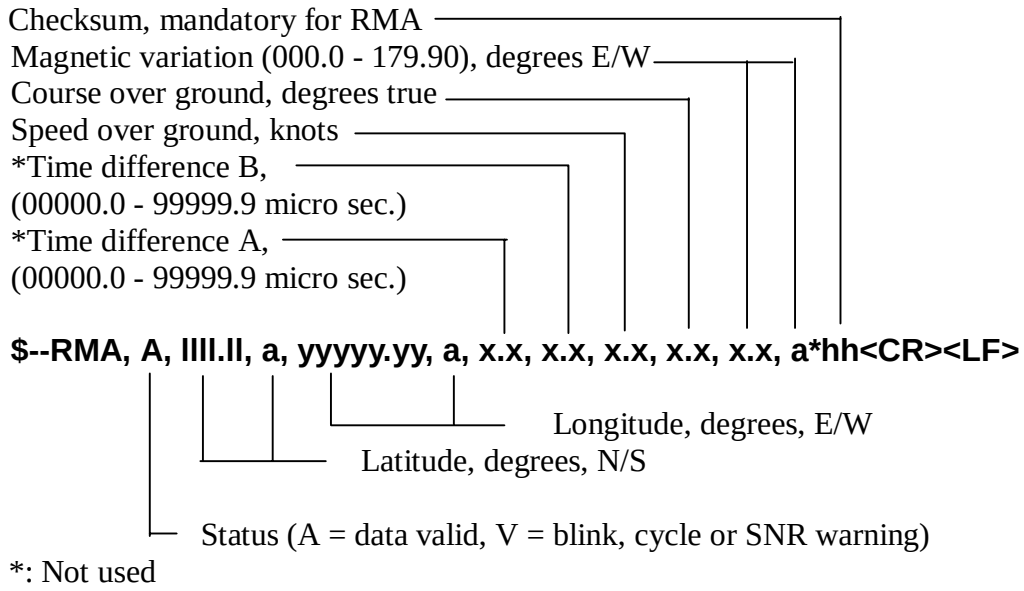
Time, position and fix related data for a GPS receiver.



* : Not used

RMA - Recommended minimum specific LORAN-C data

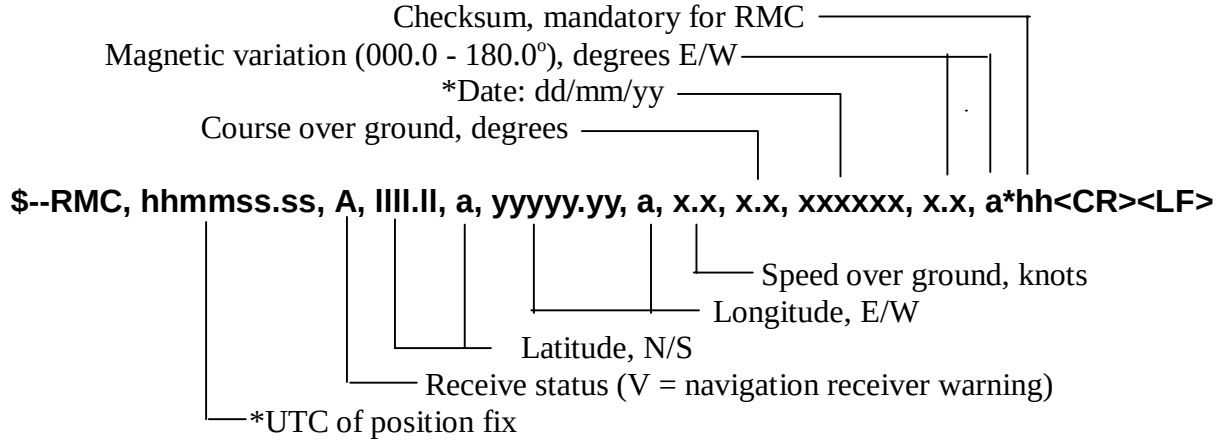
Position, course and speed data provided by a LORAN-C receiver. Time differences A and B are those used in computing latitude/longitude. Checksum is mandatory in this sentence. This sentence is transmitted at intervals not exceeding 2 s and is always accompanied by RMB when a destination waypoint is active. RMA and RMB are the recommended minimum data to be provided by a LORAN-C receiver. All data fields must be provided, null fields used only when data is temporarily unavailable.



*: Not used

RMC - Recommended specific GPS/TRANSIT data

Time, date, position, course and speed data provided by a GPS or TRANSIT navigation receiver. Checksum is mandatory in this sentence. This sentence is transmitted at intervals not exceeding 2 s and is always accompanied by RMB when a destination waypoint is active. RMC and RMB are the recommended minimum data to be provided by a GPS or TRANSIT receiver. All data fields must be provided, null fields used only when data is temporarily unavailable.



*: Not used

VTG- Course over ground and ground speed

The actual course and speed relative to the ground

$--VTG, x.x, T, x.x, M, x.x, N, x.x, K*hh<CR><LF>

- Checksum
- Speed, km/h
- Speed, knots
- Course degrees magnetic
- Course degrees true

ZDA - Time and date

UTC, day, month, year and local time zone.

$--ZDA. hhmmss.ss, xx, xx, xxxx, xx, xx*hh<CR><LF>

- Checksum
- Local zone description, minutes
- Local zone description, hours
- *Yea r
- *Month, 01 to 12
- *Day, 0 to 3l
- UTC

*: Not used

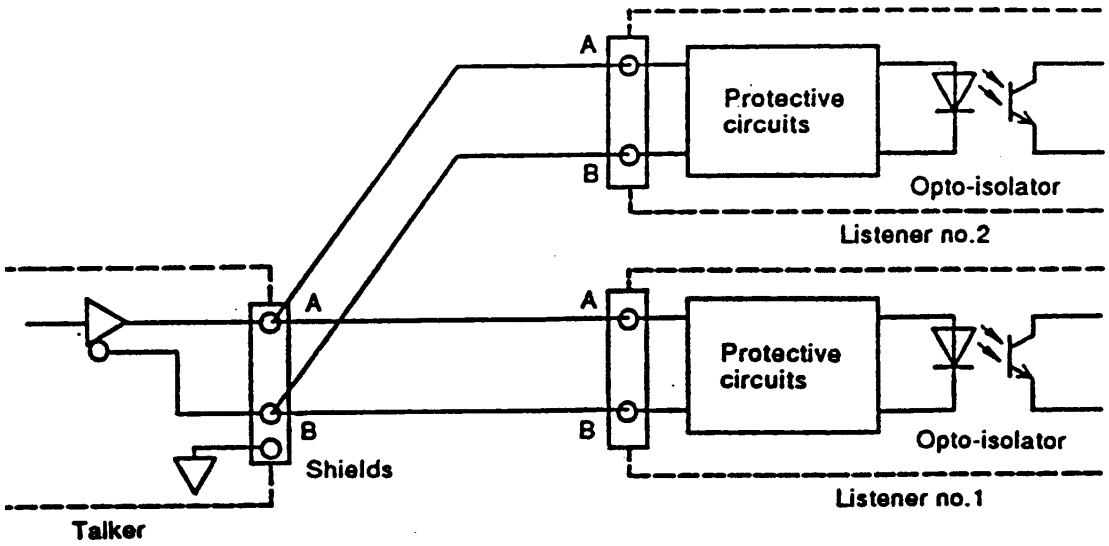
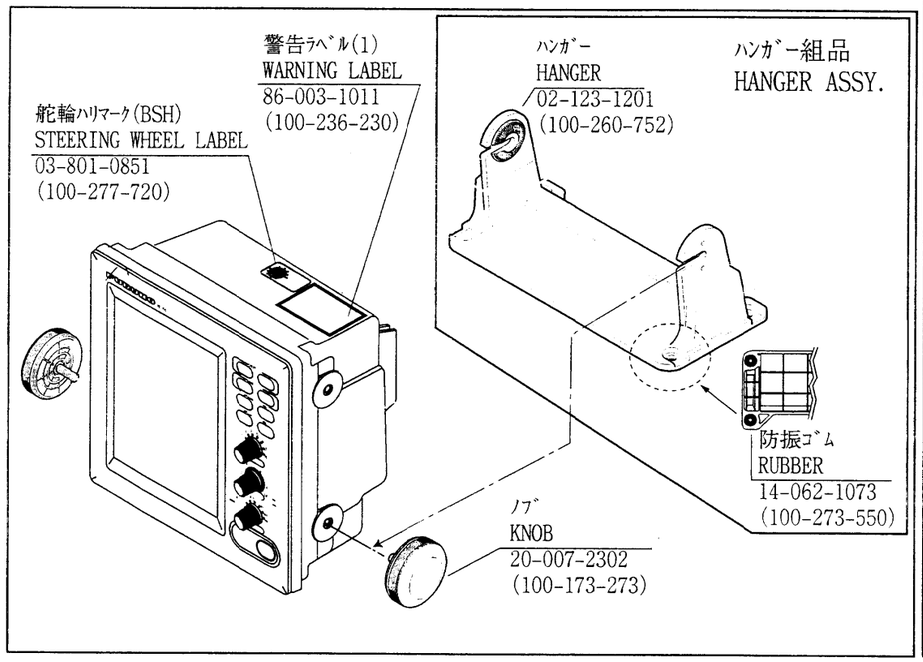
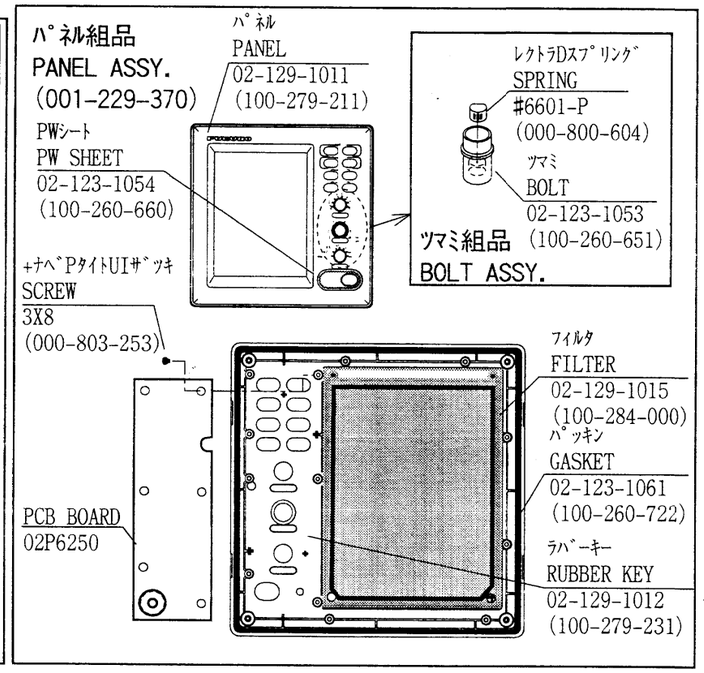


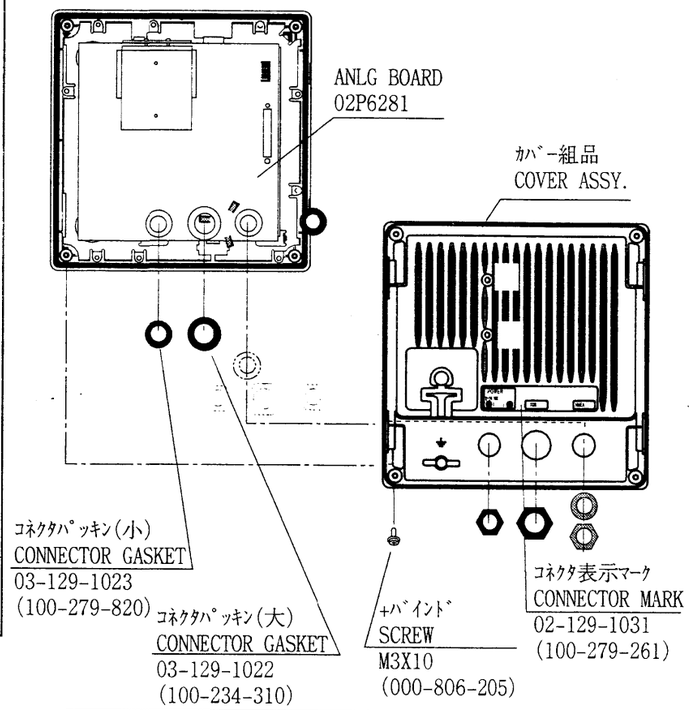
Figure 5.1 Input and output circuit

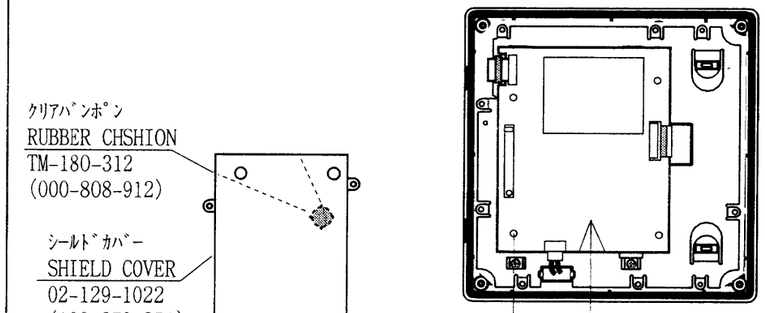
PARTS LIST

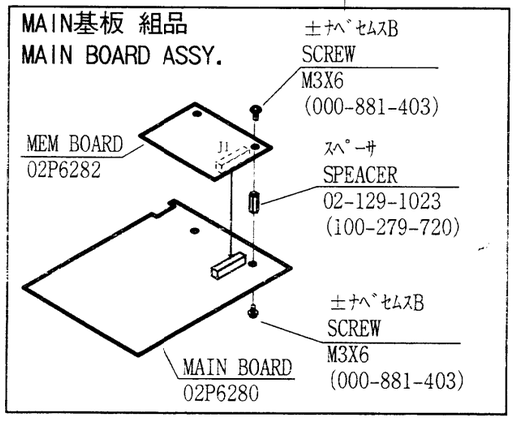
UNIT	NAME	TYPE	CODE NUMBER
FE-701	MAIN Board Assembly(MAIN/MEM)		001229190
	MAIN Board	02P6280	001229200
	MEM Board	02P6282	001229220
	ANLG Board	02P6281	001229240
	PNL Board	02P6250	001389720
	LCD	EDTCA14QCF	000142777
FE-702	CONE Board	02P6283	001229030

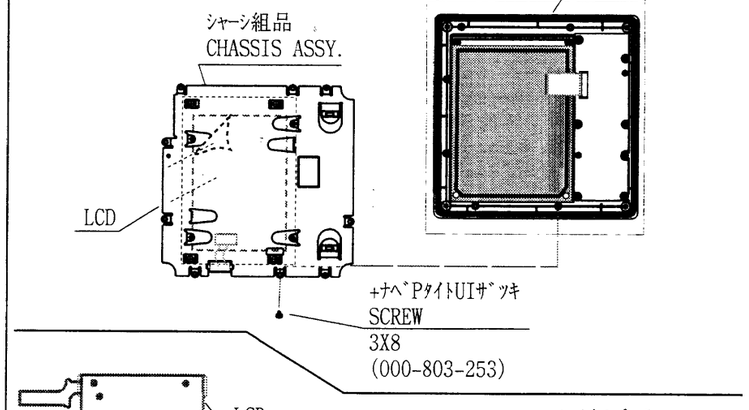


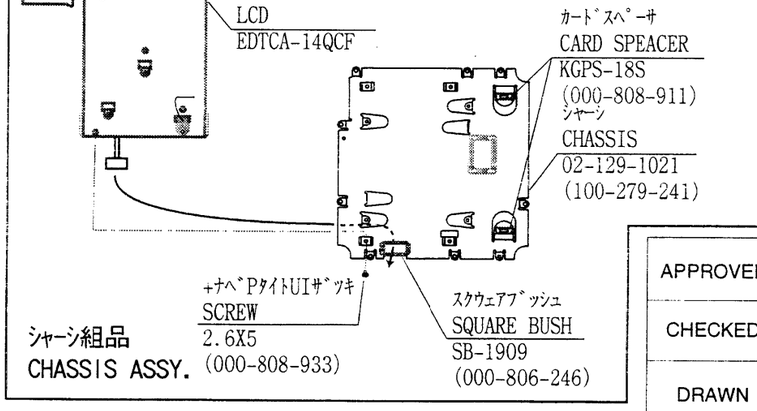


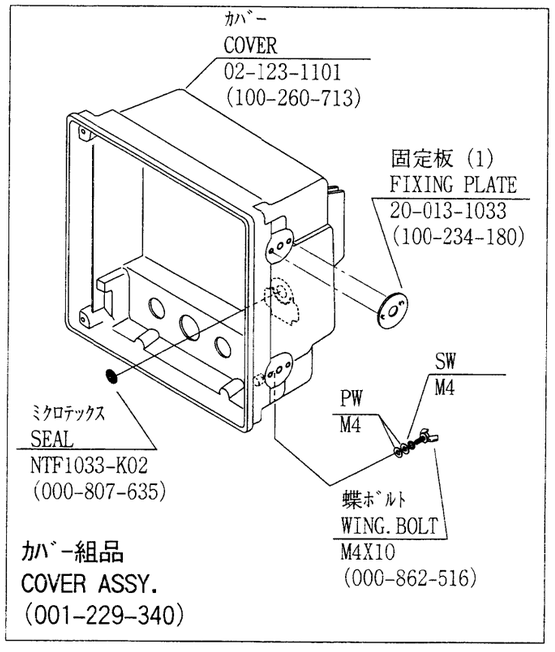












APPROVED	APR・17・2000 S.KOIZUMI	TITLE	指示器 DISPLAY UNIT
CHECKED	APR・17・2000 TAKAHASHI	FE-701	
DRAWN	APR・17・2000 F.MIYOSHI	DWG. NO.	C2366-E01-A

電源部組品
POWEWR UNIT ASSY.
(001-228-980)

端子台
TERMINAL BOARD
ML-250S1AXF-3P

ﾅﾍﾞｾﾑｽA
SCREW
M3X15
(000-881-107)

ｽｸｳｪｱﾌﾞｯｼｭ
SQUARE BUSH
SB-1909
(000-126-024)

ﾋｭｰｽﾞﾎﾙﾀﾞｰ
FUSE HOLDER
FH-043A

ﾅﾍﾞｾﾑｽA
SCREW
M3X15
(000-881-107)

ﾌｨﾙﾀｰ取付板
FILTER FIXING PLATE
02-129-2022
(100-279-101)

端子台
TERMINAL BOARD
ML-250S1AXF-3P

端子台
TERMINAL BOARD
ML-250S1AXF-3P

ﾄｸﾞﾙｽｲｯﾁ
SWITCH
M-2032L/B

ｸﾗﾝﾌﾟ
CLAMP
CKS-05-L
(000-570-251)

警告貼りﾏｰｸ
WARNING LABEL
66-022-2012
(100-237-730)

Ⓐ

Ⓐ

+ﾅﾍﾞｾﾑｽBK
SCREW
M3X8
(000-804-626)

ﾉｲｽﾞﾌｨﾙﾀ
NOISE FILTER
ZCB2203-11

ﾄﾗﾝｽ取付板
TRANSFORMER FIXING PLATE
02-129-2023
(100-279-111)

ﾅﾍﾞｾﾑｽB
SCREW
M3X8
(000-881-404)

ﾄﾗﾝｽ
TRANSFORNER
02S1256

ﾅﾍﾞｾﾑｽB
SCREW
M4x8
(000-881-445)

ｽｸｳｪｱﾌﾞｯｼｭ
SQUAR BUSH
SB-1909
(000-126-024)

端子台ｶﾊﾞｰ
TERMINAL BOARD COVER
ML-250-C-5P
(000-142-772)

ｸﾗﾝﾌﾟ
CLAMP
CKS-05-L
(000-570-251)

電源部組品
POWER UNIT ASSY.

ﾅﾍﾞｾﾑｽB
SCREW
M3X8
(000-881-404)

CON BOARD
02P6283

舵輪ﾊﾘﾏｰｸ(BSH)
STEERING WHELL LABEL
03-801-0851
(100-277-720)

警告ﾗﾍﾞﾙ(1)
WARING LABEL
86-003-1011
(100-236-230)

配線ﾊﾘﾏｰｸ
LABEL
02-129-2012
(100-279-070)

ﾅﾊﾞｲﾝﾄﾞｾﾑｽF
SCREW
M4X8
(000-806-407)

本体ｶﾊﾞｰ
BODY COVER
02-129-2011
(100-279-051)-2.5GY5/1.5
(100-279-060)-7.5BG7/2

本体ｹｰｽ
BODY CASE
02-129-2021
(100-279-081)-2.5GY5/1.5
(100-279-090)-7.5BG7/2

ｱｰｽｵｻｴ
GROUND PLATE
02-015-1106
(201-511-061)

蝶ﾎﾞﾙﾄ
WING.BOLT
M5X15
(000-862-517)

PW
SW M5
M5

ｱｰｽﾊﾘﾏｰｸ
GROUND LABEL
03-144-1438
(100-266-480)

DATAﾊﾘﾏｰｸ
DATA LABEL
02-129-2025
(100-281-780)

MJ-XHｺﾈｸﾀ組品
CONNECTOR ASSY.
02-1002(R10-10P)

ﾅﾍﾞｾﾑｽB
SCREW
M4X8
(000-881-445)

ｽｸｳｪｱﾌﾞｯｼｭ
SQUARE BUSH
SB-1909
(000-126-024)

基板取付板
PRINTED BOARD
FIXING PLATE
02-129-2024
(100-279-120)

ｹｰﾌﾞﾙ押さえ板(2)
CABLE FIXING PLATE
02-129-2033
(100-279-151)

+ｱﾌﾟｾｯﾄUIｾﾑｽB
SCREW
M6X16
(000-800-420)

ｹｰﾌﾞﾙ押さえ板(1)
CABLE FIXING PLATE
02-129-2032
(100-279-141)

ﾏｽｷﾝｸﾞｰｼｰﾄ
MASKING SHEET
02-129-2034
(100-279-132)

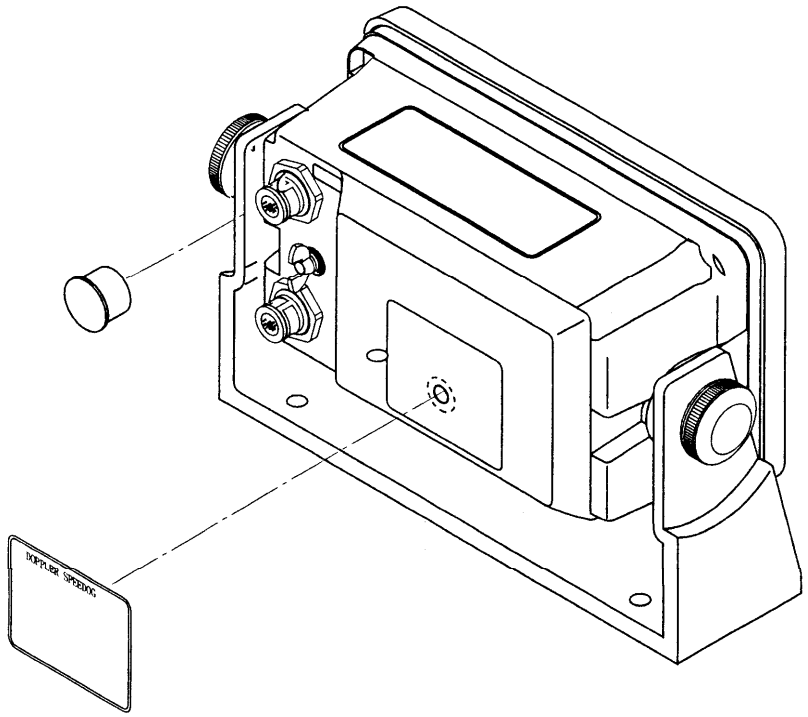
ｹｰﾌﾞﾙｸﾗﾝﾌﾟ
CABLE CLAMP
02-129-2031
(100-279-132)

ﾅﾍﾞｾﾑｽA
SCREW
M4X25
(000-881-154)

APPROVED	APR・17・2000 S.KOIZUMI	TITLE	分配箱
CHECKED	APR・17・2000 TAKAHASHI	FE-702	DISTRIBUTION BOX
DRAWN	APR・14・2000 F.MITSUSHI	DWG. NO.	C2366-E02-A

50x50x80x80

Code No. 000-029-024



APPROVED	MAY・8・2000 Takahashi	TITLE	深度表示器
CHECKED	APR・28・2000 T.TAKAHASHI	FE-720	DIGITAL DEPTH INDICATOR
DRAWN	APR・27・2000 E MIYOSHI	DWG. NO.	C2366-E03-B

FURUNO

電気部品表
ELECTRICAL PARTS LIST
2000年　4月

Model	FE-701/FE-720	
Unit	指示器/深度表示器 DISPLY UNIT/DIGITAL DEPTH INDICATOR	
Ref.Dwg.	C2366-K01-A	Page
Blk.No.		**E-1**

SYMBOL 回路記号	TYPE 型式	CODE No. ｺｰﾄﾞ番号	REMARKS 備考	SHIPPABLE ASSEMBLY 出荷単位組品
	PRINTED CIRCUIT BOARD	**プリント基板**		
	02P6281, ANLG	001-229-240		X
	02P6282, MEM	001-229-220		X
	02P6280, MAIN	001-229-190		X
	65P6000, ICP	002-889-330	FE-720	
	PANEL ASSEMBLY	**パネル組品**		
	FE-701	001-229-370	w/PNL 02P6250付	X
	COVER	**カバー組品**		
	FE-701	001-229-340		X
	LCD	**LCD**		
	EDTCA-14QCA	000-142-777		
	CABLE w/CONNECTOR	**コネクタ付ケーブル**		
	65S1227	000-142-659	MJ-PH, 6P	
	65S1228	000-142-660	MJ-PH, 7P	

FURUNO

電気部品表
ELECTRICAL PARTS LIST
2000年　4月

Model	FE-702		
Unit	分配箱 DISTRIBUTION BOX		
Ref.Dwg.	C2366-K02-B	Page	
Blk.No.		**E-2**	

SYMBOL 回路記号	TYPE 型式	CODE No. ｺｰﾄﾞ番号	REMARKS 備考	SHIPPABLE ASSEMBLY 出荷単位組品
	PRINTED CIRCUIT BOARD	プリント基板		
	02P6283,CONE	001-229-030		X
	POWER ASSEMBLY	電源組品		
	FE-702	001-228-980		X
	TRANSFORMER	トランス		
T1	02S1256-0	000-142-779		
	SWITCH	スイッチ		
S1	M-2032L/B	000-474-351		
	FILTER	フィルタ		
FL1	ZCB2203-11	000-128-847		
	FUSE	ヒューズ		
F1	FGMB 1A 250V	000-142-771		
F2	FGMB 1A 250V	000-142-771		
	FUSE HOLDER	ﾋｭｰｽﾞﾎﾙﾀﾞｰ		
FX1	FH043A	000-138-885		
FX2	FH043A	000-138-885		
	TERNINAL BOARD	端子台		
TB5	ML250S1AXF-3P	000-142-535		
TB6	ML250S1AXF-3P	000-142-535		
TB7	ML250S1AXF-3P	000-142-535		
	JACK	ジャック		
J1	MJ-A10SRMD	000-126-663		
	CABLE w/CONNECTOR	コネクタ付ケーブル		
	02-1001 (2P)	001-228-800	VH CONNECTOR	
	02-1002 (R10-10P)	001-228-860	MJ-XH CONNECTOR	

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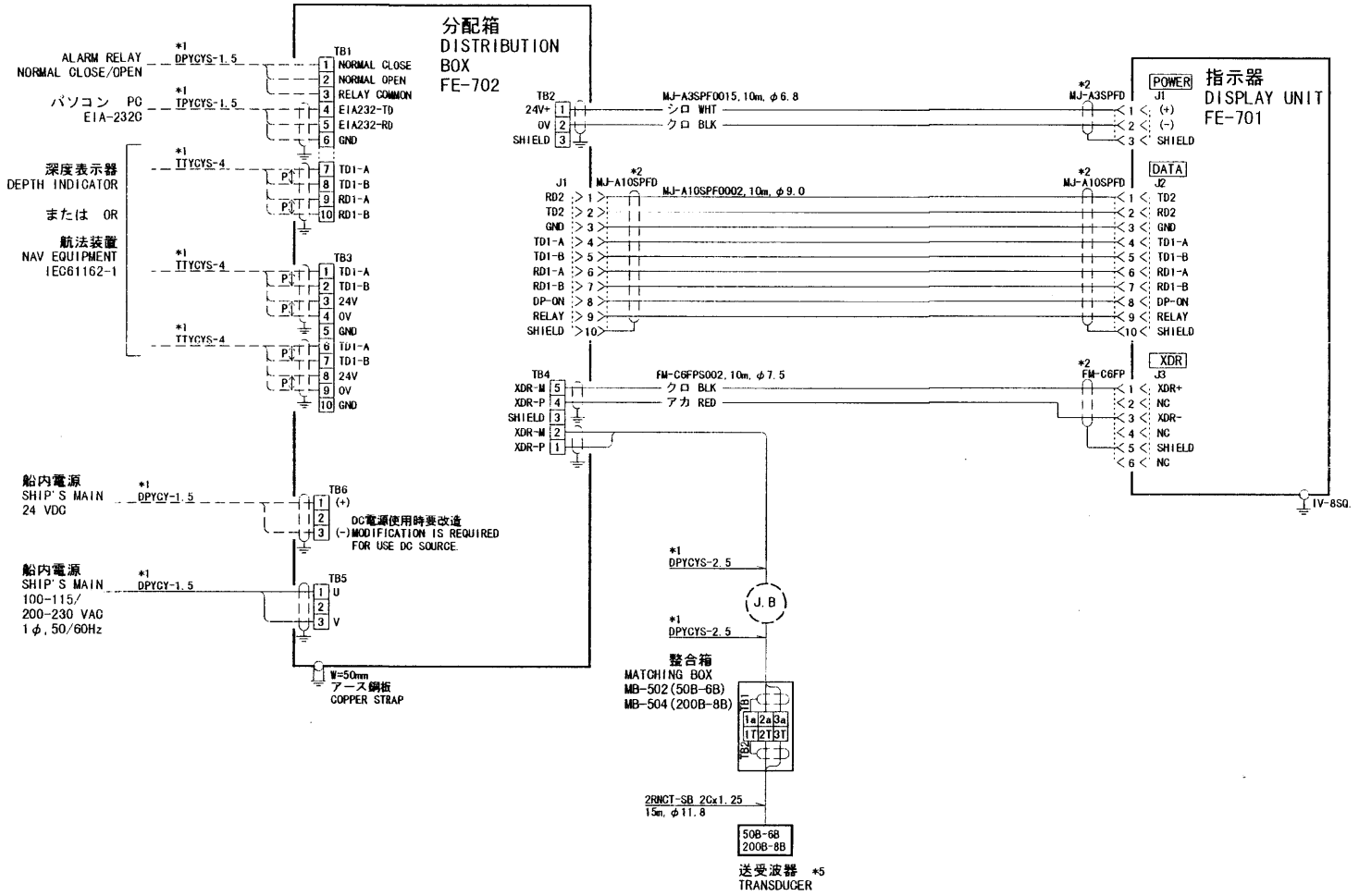


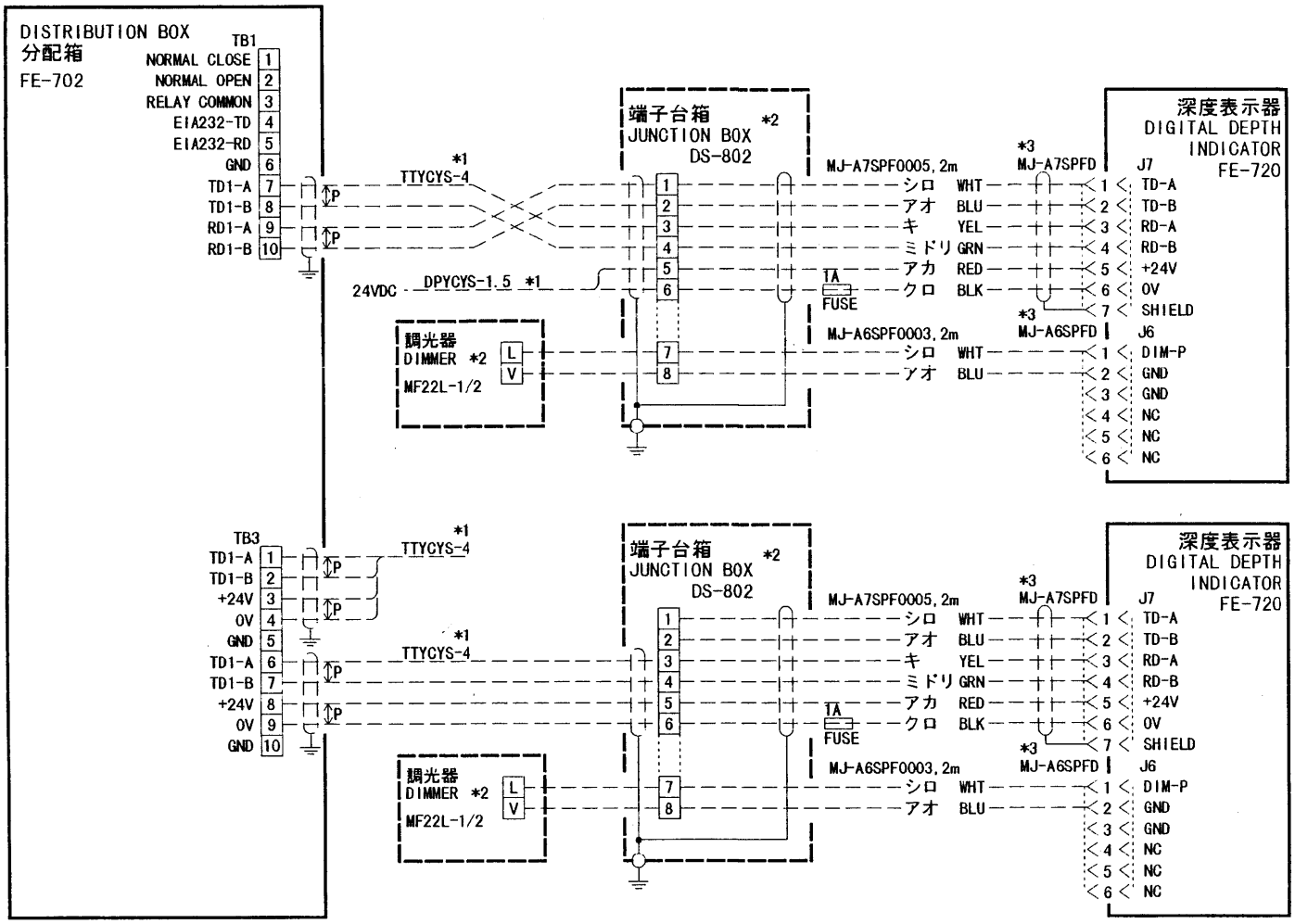
注記
＊1）現地手配
＊2）工場にて取付済み
＊3）オプション
＊4）分配器から整合箱までの最大長は400m。
＊5）本体の周波数は工場出荷時に200kHzに設定。
50kHzのときは必ずメニュー設定を変更のこと。

NOTE
*1. LOCAL SUPPLY.
*2. FITTED AT FACTORY.
*3. OPTION
*4. MAXIMUM CABLE LENGTH BETWEEN DISTRIBUTION BOX AND MATCHING BOX IS 400 m.
*5. TRANSMITTING FREQUENCY HAS BEEN SET TO 200 kHz AT FACTORY.
WHEN 50 kHz IS INSTALLED, CHANGE THE SETTING AT THE MENU.

DRAWN Mar 15'00 T.YAMASAKI		TITLE	FE-700
CHECKED Mar 15'00 Y.K		名称	音響測深機
APPROVED Mar 16'00 S.Fukuma			相互結線図
SCALE	MASS kg	NAME	NAVIGATIONAL ECHO SOUNDER
DWG. No. C2366-C01- D			INTERCONNECTION DIAGRAM

FURUNO ELECTRIC CO., LTD.

FURUNO

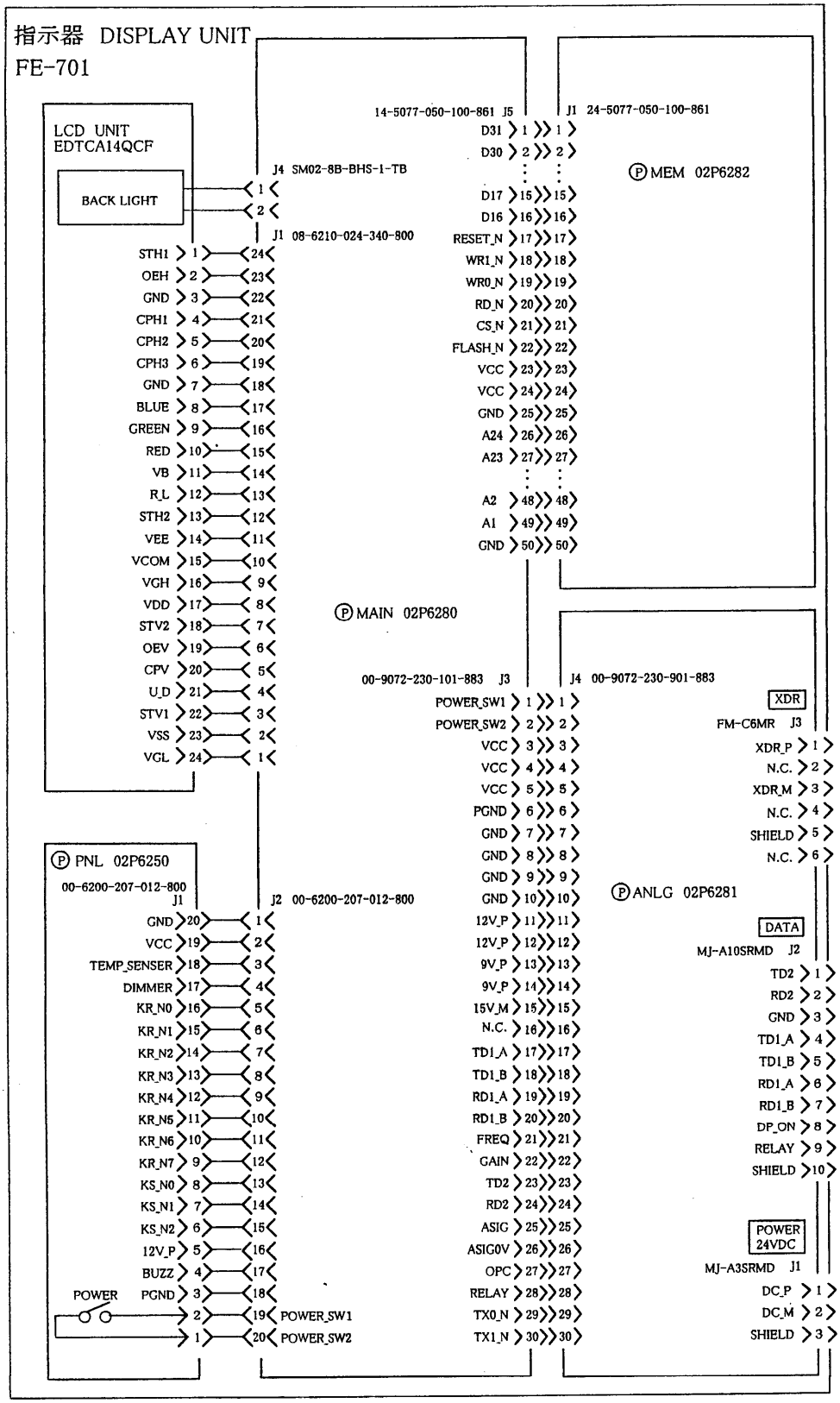


注記
＊1）現地手配
＊2）オプション
＊3）工場にて取付済み。

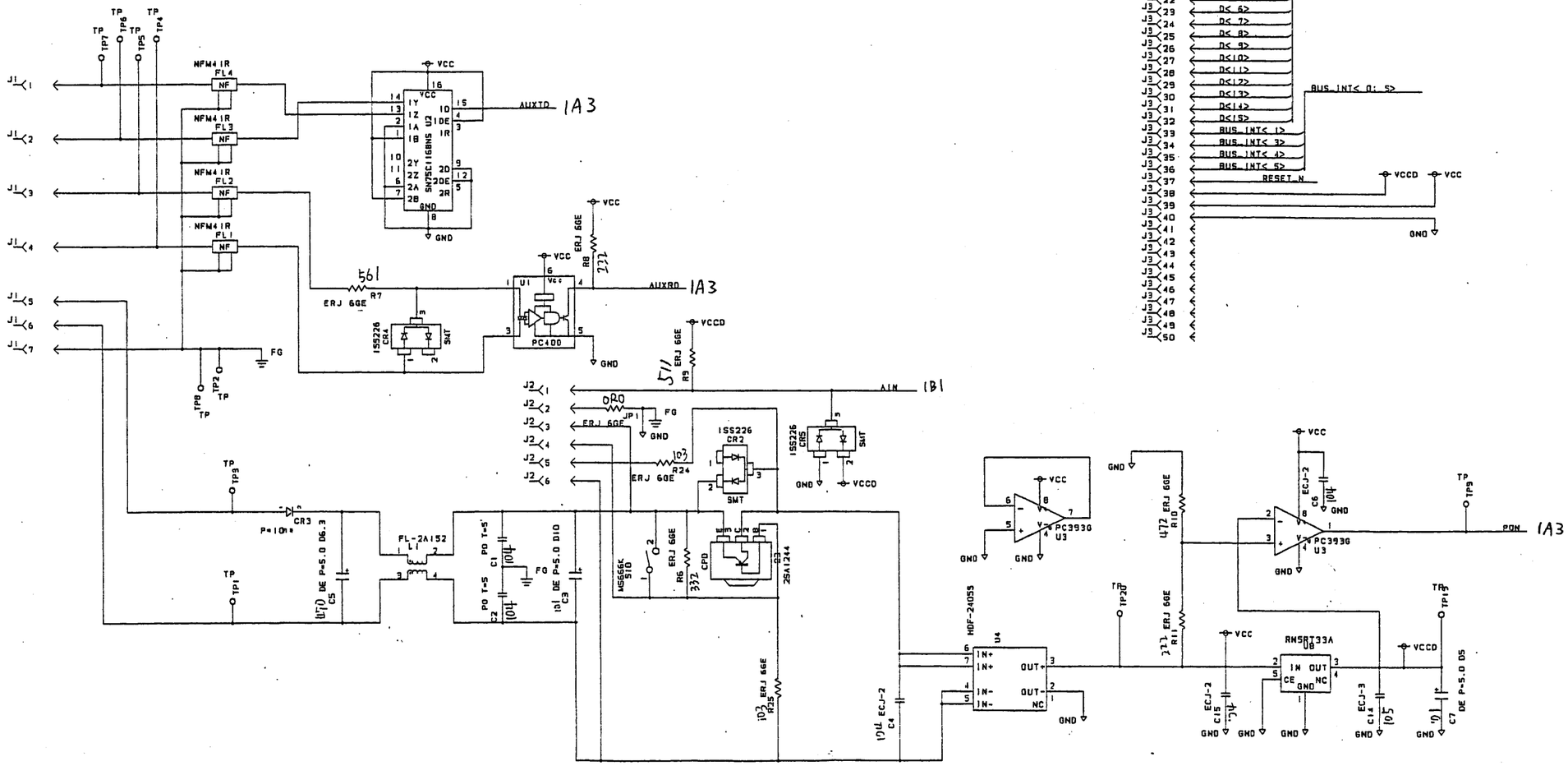
NOTE
*1. LOCAL SUPPLY.
*2. OPTION.
*3. FITTED AT FACTORY.

DRAWN Jan 25 '00 T.YAMASAKI			TITLE FE-720
CHECKED Jan 25 '00 K.KUSUNOKI			名称 深度表示器
APPROVED Jan 25 '00 K.KUSUNOKI		FE-700	相互結線図
SCALE	MASS kg		NAME DIGITAL DEPTH INDICATOR
DWG. No. C2366-C02- B		02-129-1004- 0	INTERCONNECTION DIAGRAM

FURUNO ELECTRIC CO., LTD.

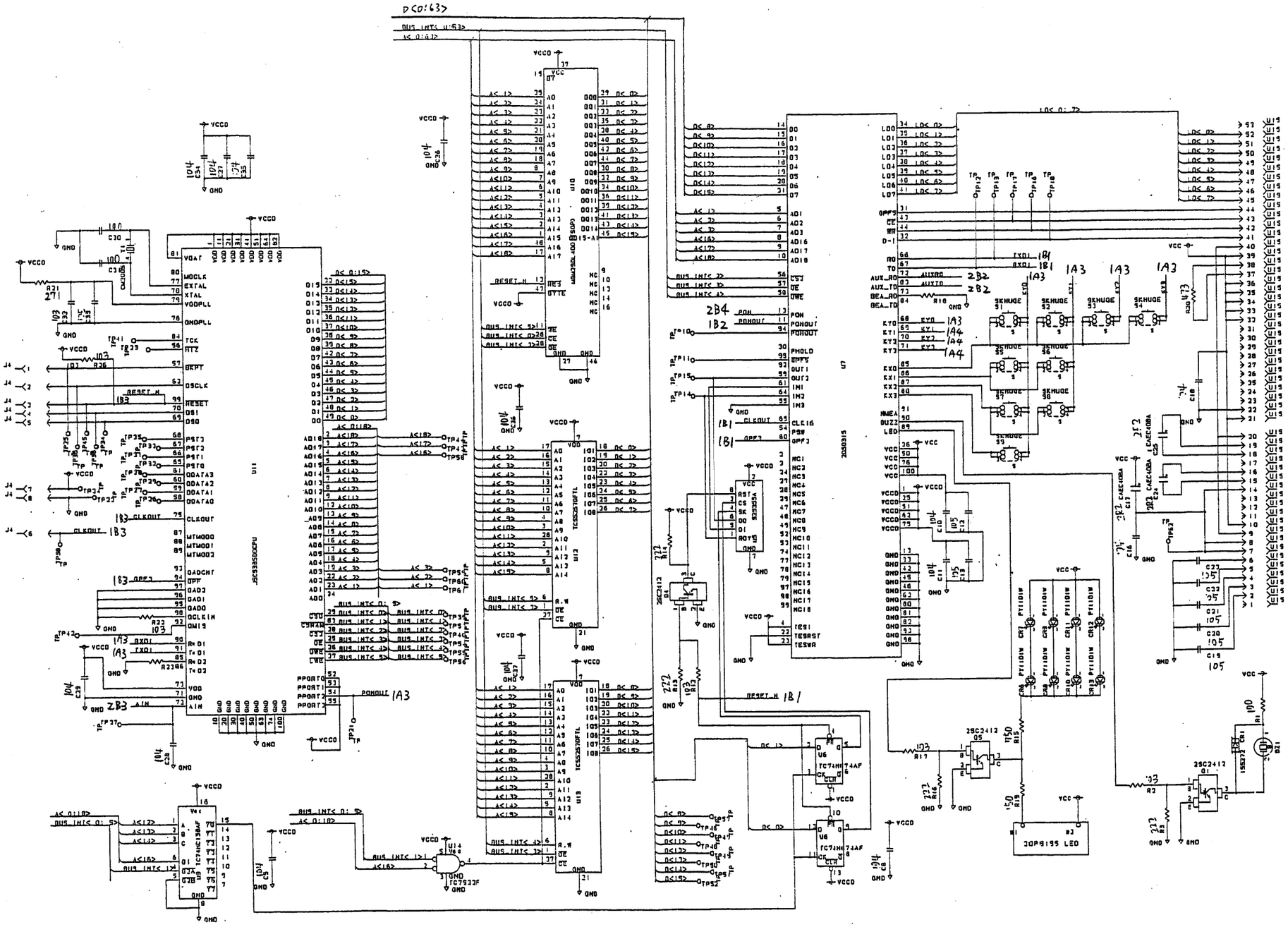


DRAWN Oct 8 '99 T.YAMASAKI			TYPE FE-701
CHECKED Oct 8 '99 K.Kusunoki			名称 指示器（総合）
APPROVED Oct 8 '99 K.Kusunoki		FE-700	回路図
SCALE /	MASS kg	APPLICABLE TO; (MODEL)	BLOCK NO.	NAME DISPLAY UNIT(GENERAL)
DWG NO. C2366-K01- A		02-129-1002- 0		SCHEMATIC DIAGRAM

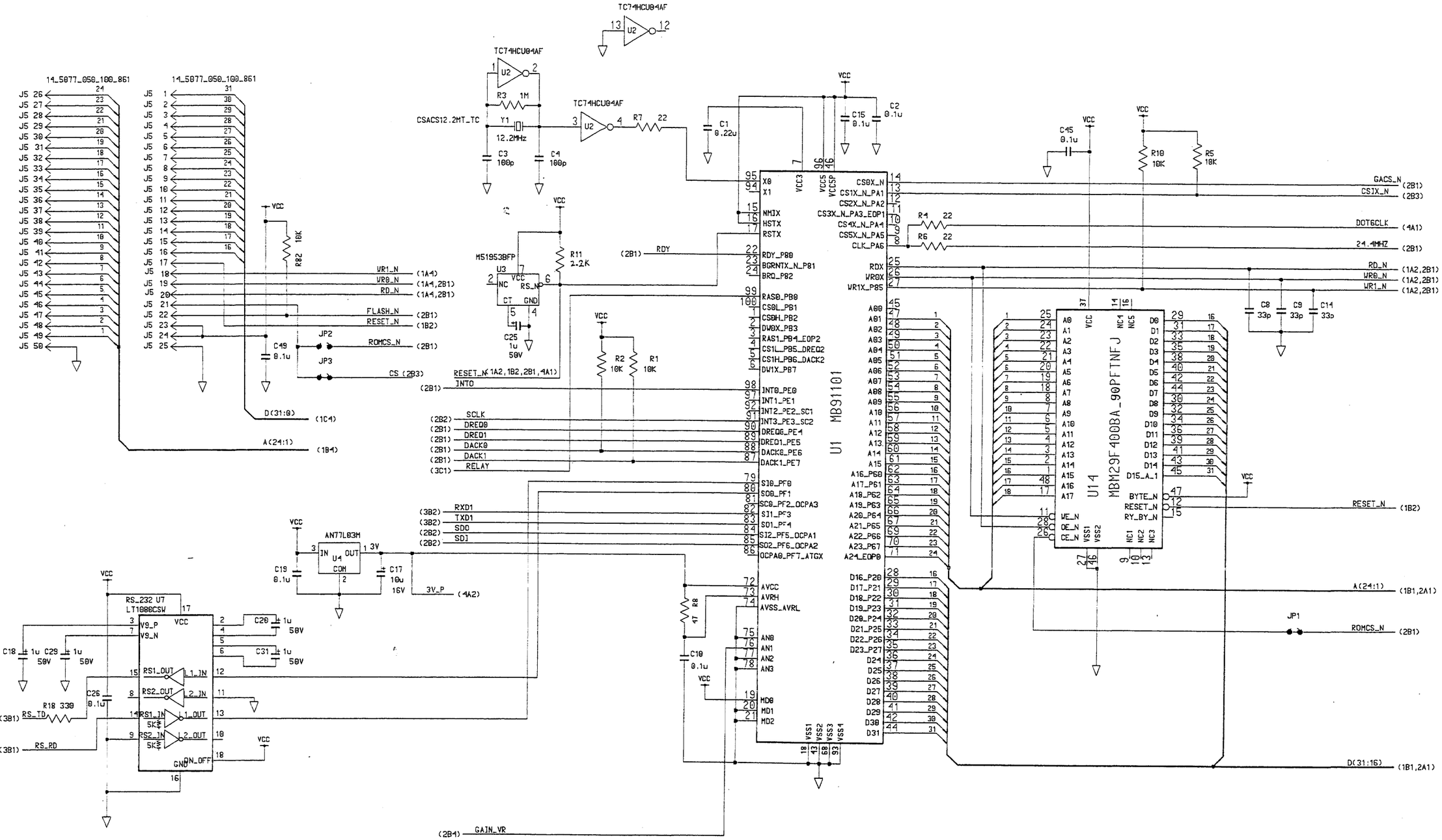


DRAWN Dec 13'99 T.YAMASAKI			TYPE 65P6000(2/2)
CHECKED Dec 14'99 K.Kusunoki	FE-720 DS-840 DS-830 DS-800		名称 指示器
APPROVED Dec 14'99 K.Kusunoki			回路図
SCALE / MASS kg	APPLICABLE TO; (MODEL)	BLOCK NO.	NAME DISPLAY
DWG NO. C7247-K05- A	65-005-2001- 1		SCHEMATIC DIAGRAM

FURUNO



DRAWN Dec 13 '99 T.YAMASAKI				TYPE 65P6000(1/2)
CHECKED Dec 14 '99 K.Kusuda	FE-720 DS-840			名称 指示器
APPROVED Dec 14 '99 K.Kusuda	DS-830 DS-800			回路図
SCALE /	MASS kg	APPLICABLE TO; (MODEL)	BLOCK NO.	NAME DISPLAY
DWG NO. C7247-K04- A		65-005-2001- 1		SCHEMATIC DIAGRAM



DRAWN Dec 13 '99 T.YAMASAKI			TYPE 02P6280(1/4)
CHECKED Dec14'99 K.KUSUHARA			名称 メイン基板
APPROVED Dec14'99 K.KUSUHARA	FE-701	1B 1	回路図
SCALE / MASS kg	APPLICABLE TO; (MODEL)	BLOCK NO.	NAME MAIN PCB
DWG NO. C2366-K03- A	02-129-1101- 0		SCHEMATIC DIAGRAM

U10
uPD65803GD
02S4678_1

U5 M62352GP_75EC

U6 M5M51426SC-60TS_K

U11 uPC311G2

U12 TC7S08F

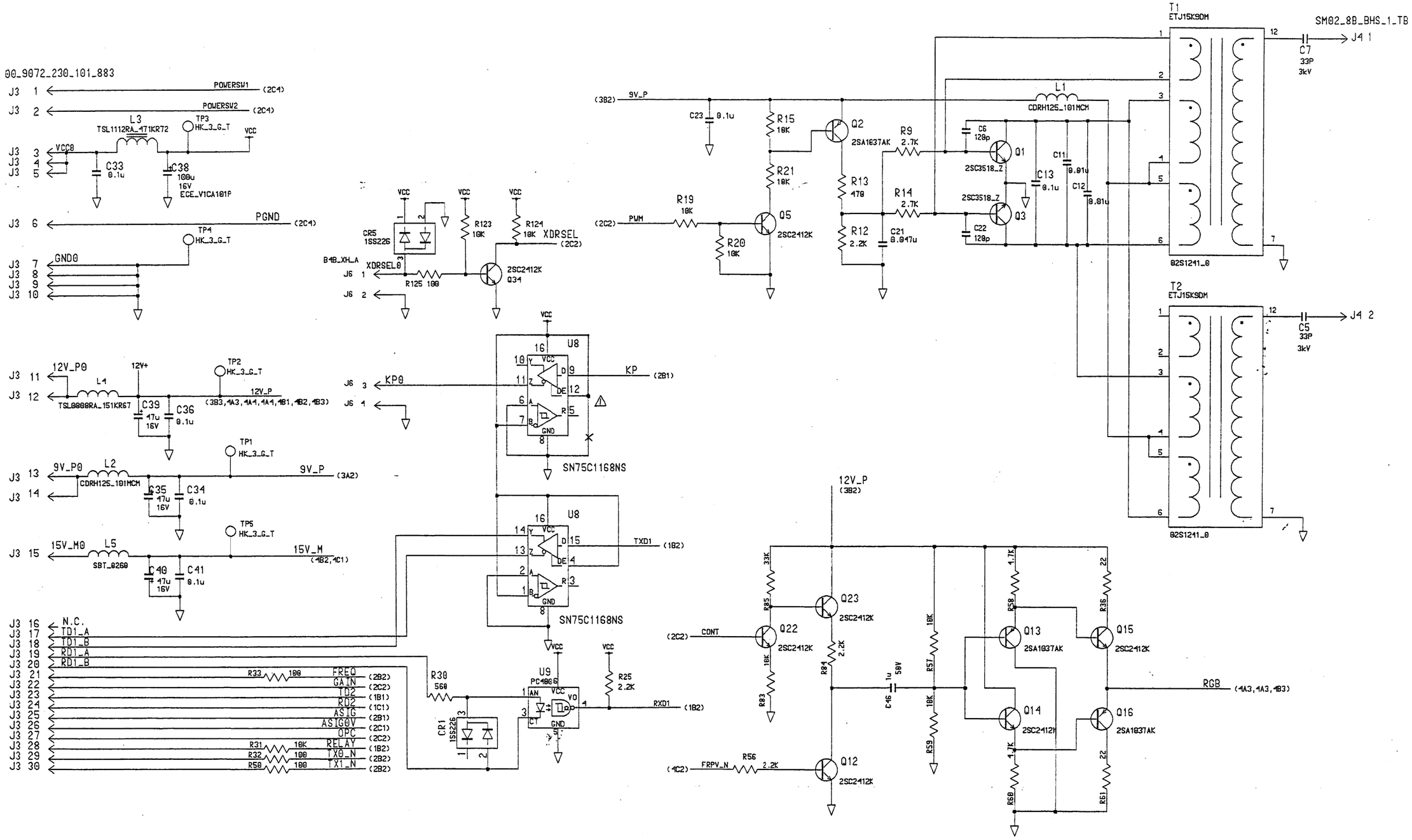
Q4 2SC2412K

CR2 1SS226

R35 MRG_C08B1KohmJ

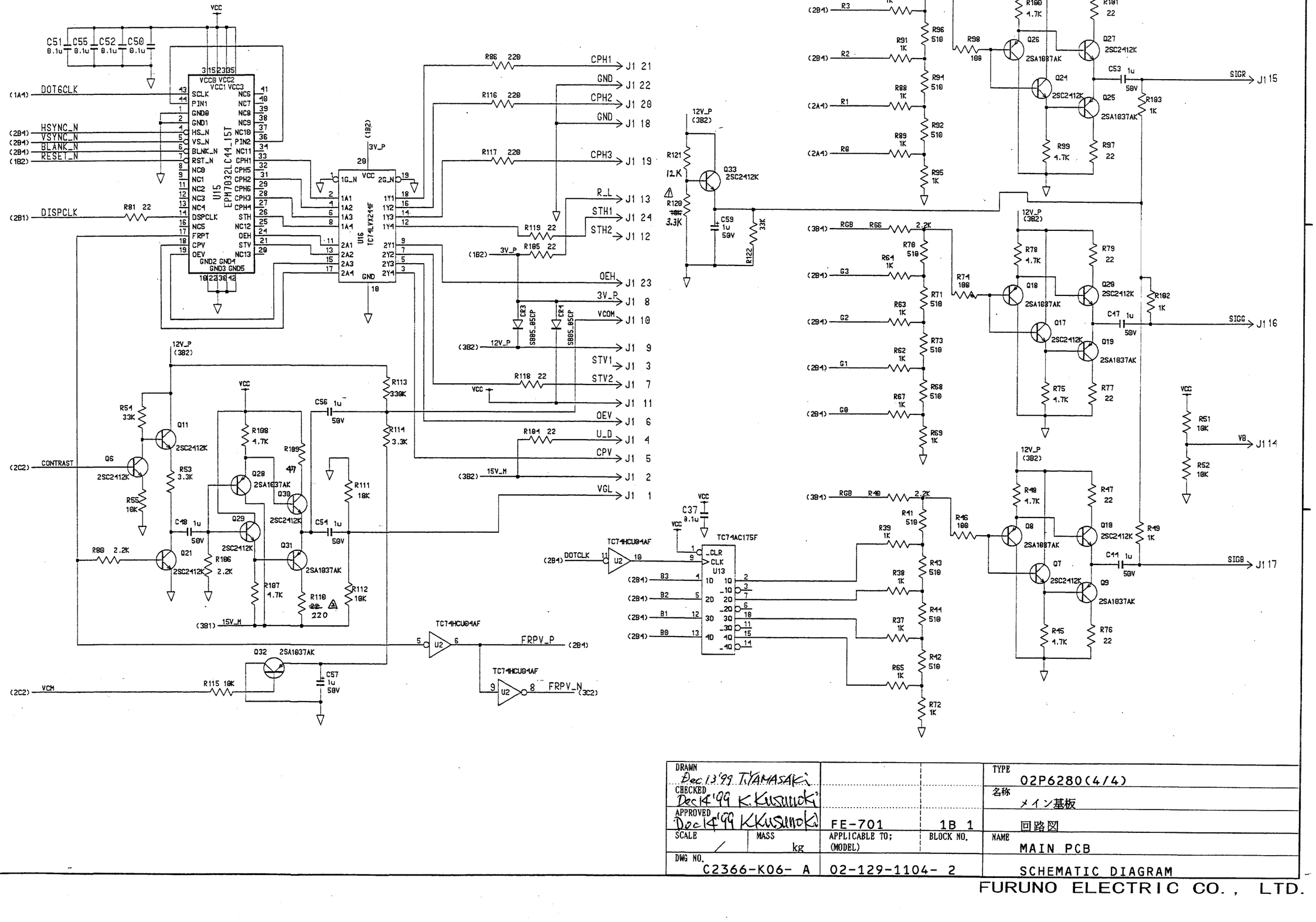
00_6200_207_012_800

DRAWN Dec13'99 T.YAMASAKI			TYPE 02P6280(2/4)
CHECKED Dec14'99 K.Kitsuki			名称 メイン基板
APPROVED Dec14'99 K.Kitsuki	FE-701	1B 1	回路図
SCALE /	MASS kg	APPLICABLE TO; (MODEL)	BLOCK NO.	NAME MAIN PCB
DWG NO. C2366-K04- A	02-129-1102- 1			SCHEMATIC DIAGRAM



DRAWN Dec 13'99 T.YAMASAKI			TYPE 02P6280(3/4)
CHECKED Dec 14'99 K.KUSUNOKI			名称 メイン基板
APPROVED Dec 14'99 K.KUSUNOKI	FE-701	1B 1	回路図
SCALE / MASS kg	APPLICABLE TO; (MODEL)	BLOCK NO.	NAME MAIN PCB
DWG NO. C2366-K05- A	02-129-1103- 1		SCHEMATIC DIAGRAM

FURUNO



DRAWN Dec 13'99 T.YAMASAKI			TYPE 02P6280(4/4)
CHECKED Dec14'99 K.KUSUNOKI			名称 メイン基板
APPROVED Dec14'99 K.KUSUNOKI	FE-701	1B 1	回路図
SCALE / MASS kg	APPLICABLE TO; (MODEL)	BLOCK NO.	NAME MAIN PCB
DWG NO. C2366-K06- A	02-129-1104- 2		SCHEMATIC DIAGRAM

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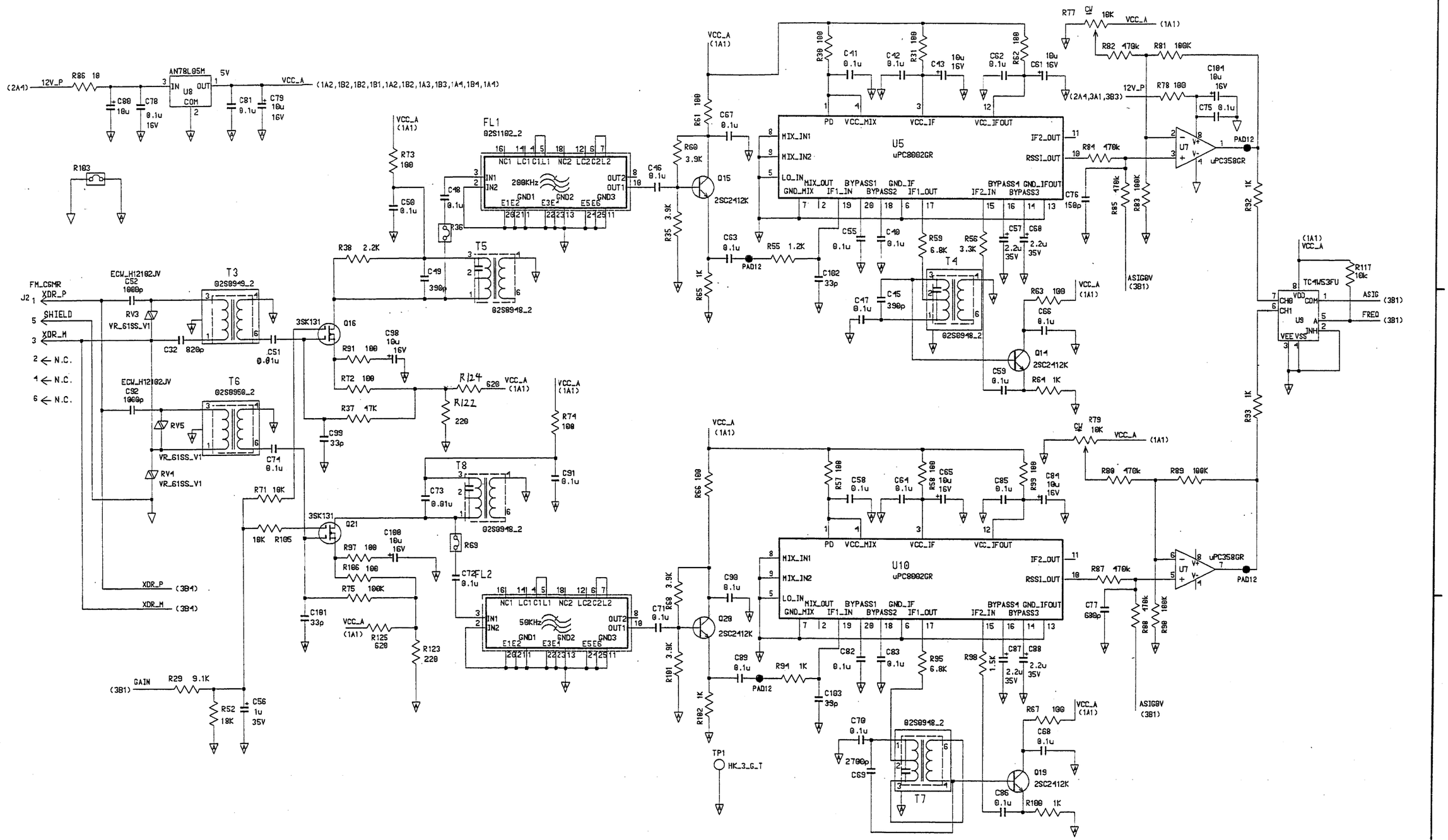
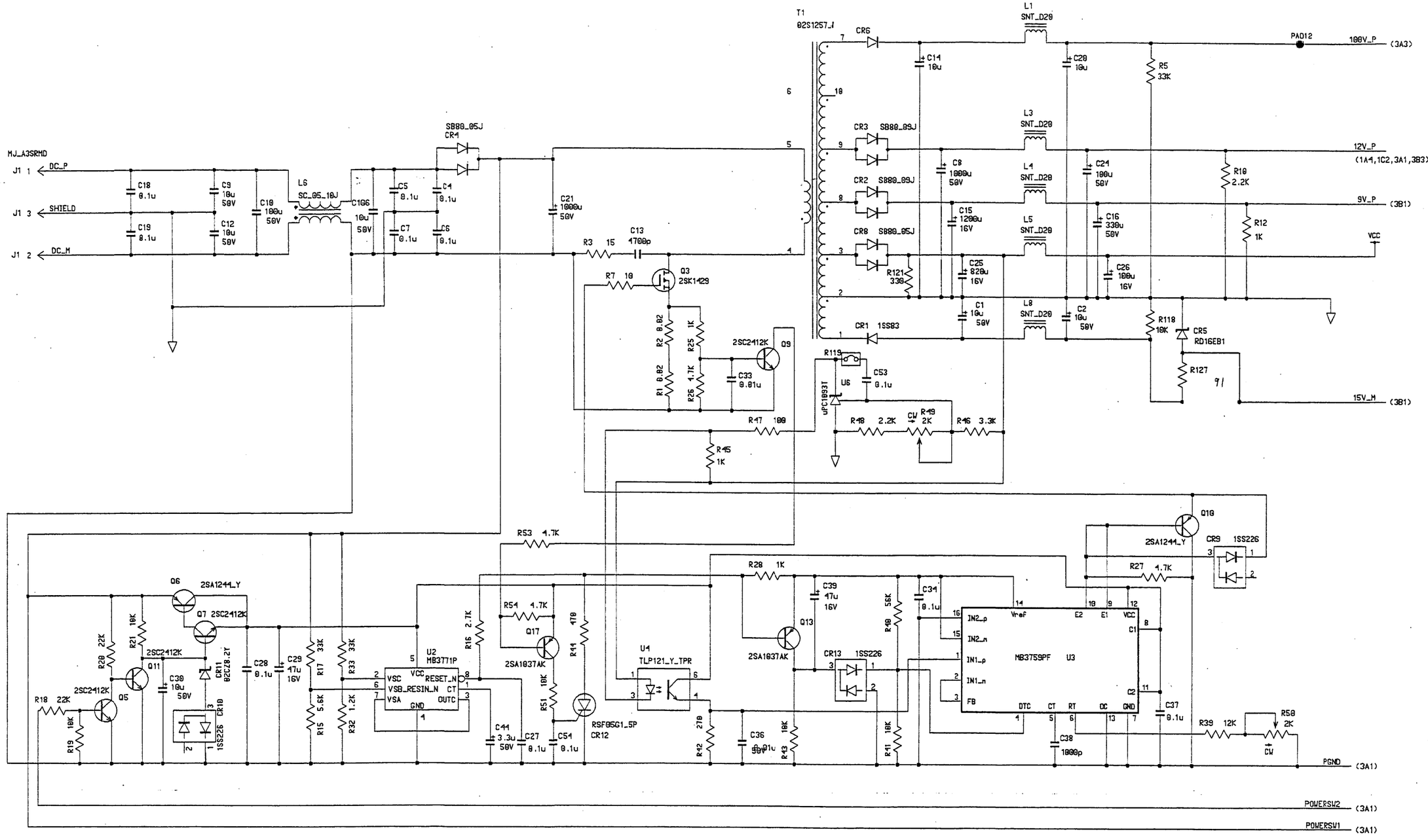
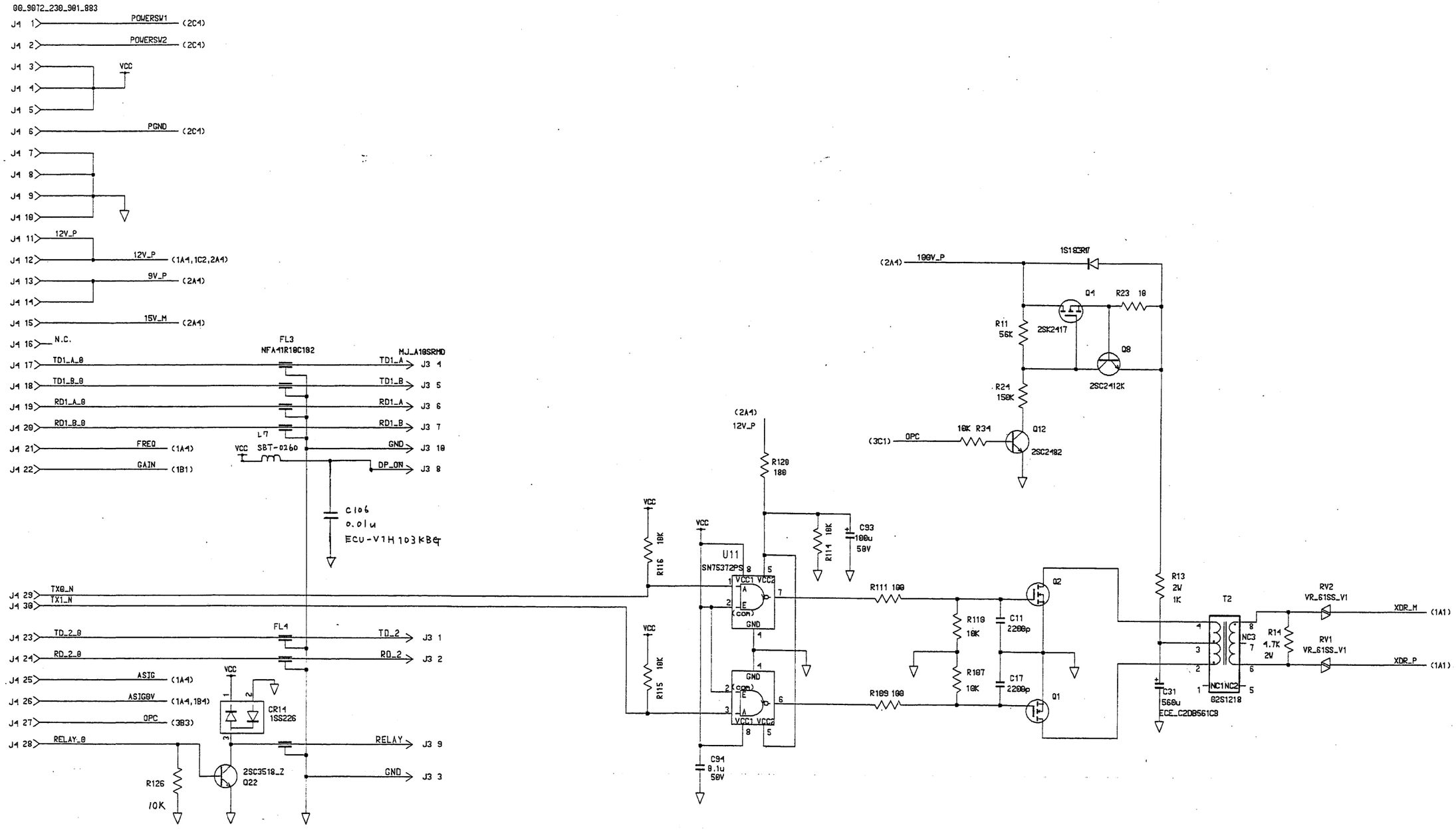


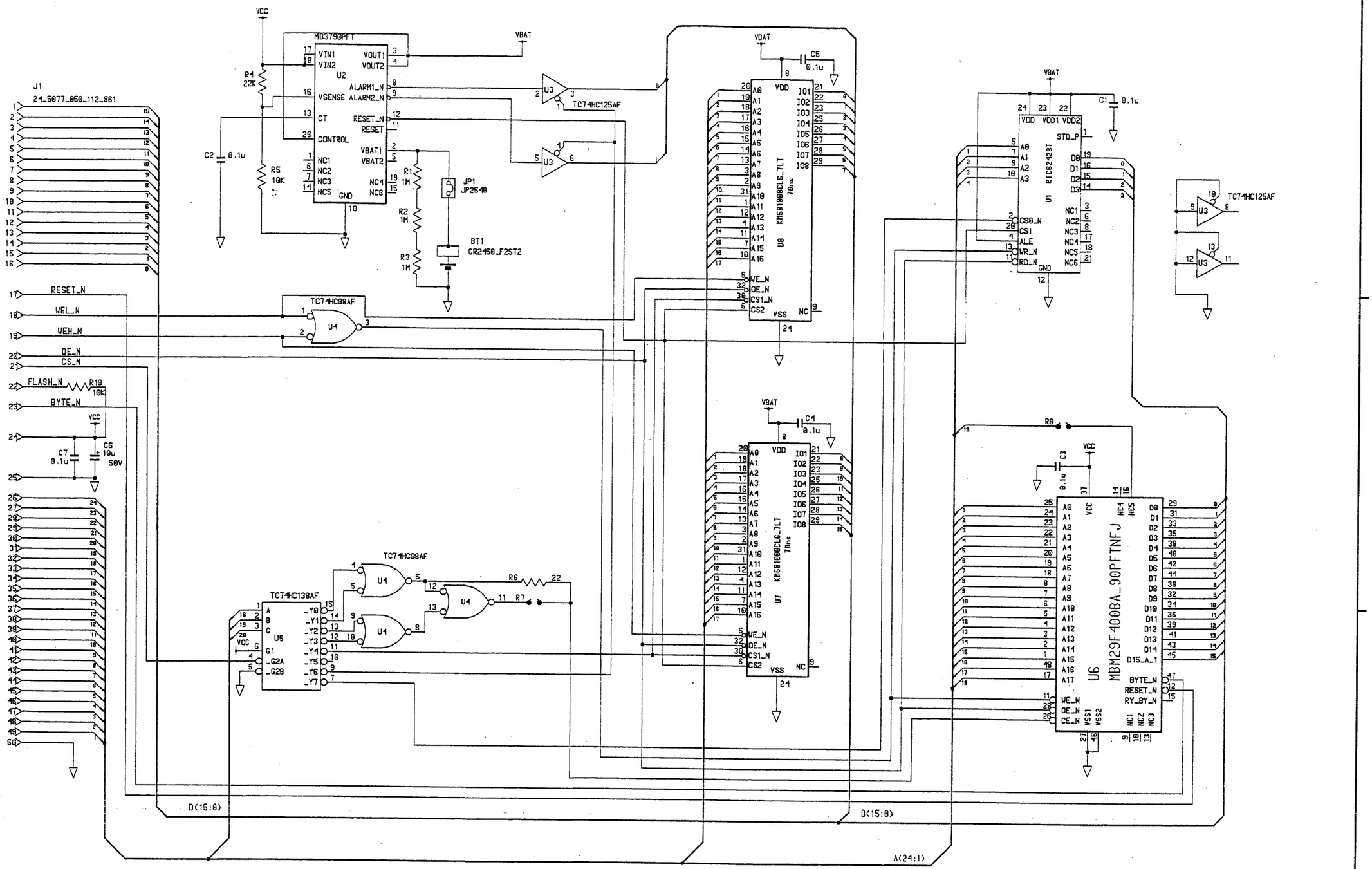
DRAWN Dec13'99 T.YAMASAKI			TYPE 02P6281(1/3)
CHECKED Dec14'99 K.KUSUMOTO			名称 アナログ基板
APPROVED Dec14'99 K.KUSUMOTO	FE-701	1B 2	回路図
SCALE / MASS kg	APPLICABLE TO; (MODEL)	BLOCK NO.	NAME ANLG PCB
DWG NO. C2366-K07- A	02-129-1201- 1		SCHEMATIC DIAGRAM



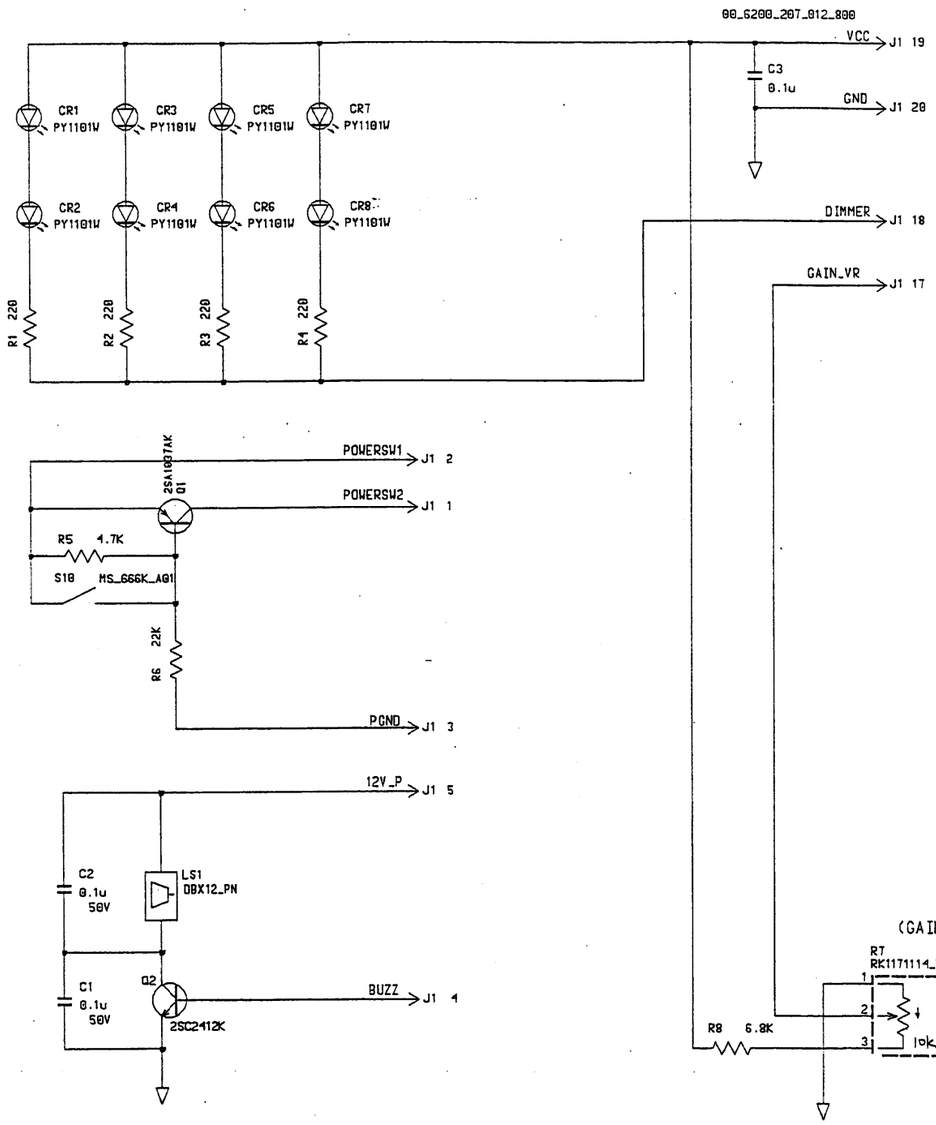
DRAWN Dec 13'99 T.YAMADA			TYPE 02P6281(2/3)
CHECKED Dec 14'99 K.Kusuda			名称 アナログ基板
APPROVED Dec 14'99 K.Kusuda	FE-701	1B 2	回路図
SCALE / MASS kg	APPLICABLE TO; (MODEL)	BLOCK NO.	NAME ANLG PCB
DWG NO. C2366-K08- A	02-129-1202- 2		SCHEMATIC DIAGRAM



DRAWN Dec13'99 T.YAMASAKI			TYPE 02P6281(3/3)
CHECKED Dec14'99 K.Kusunoki			名称 アナログ基板
APPROVED Dec14'99 K.Kusunoki	FE-701	1B 2	回路図
SCALE / MASS kg	APPLICABLE TO; (MODEL)	BLOCK NO.	NAME ANLG PCB
DWG NO. C2366-K09- A	02-129-1203- 1		SCHEMATIC DIAGRAM



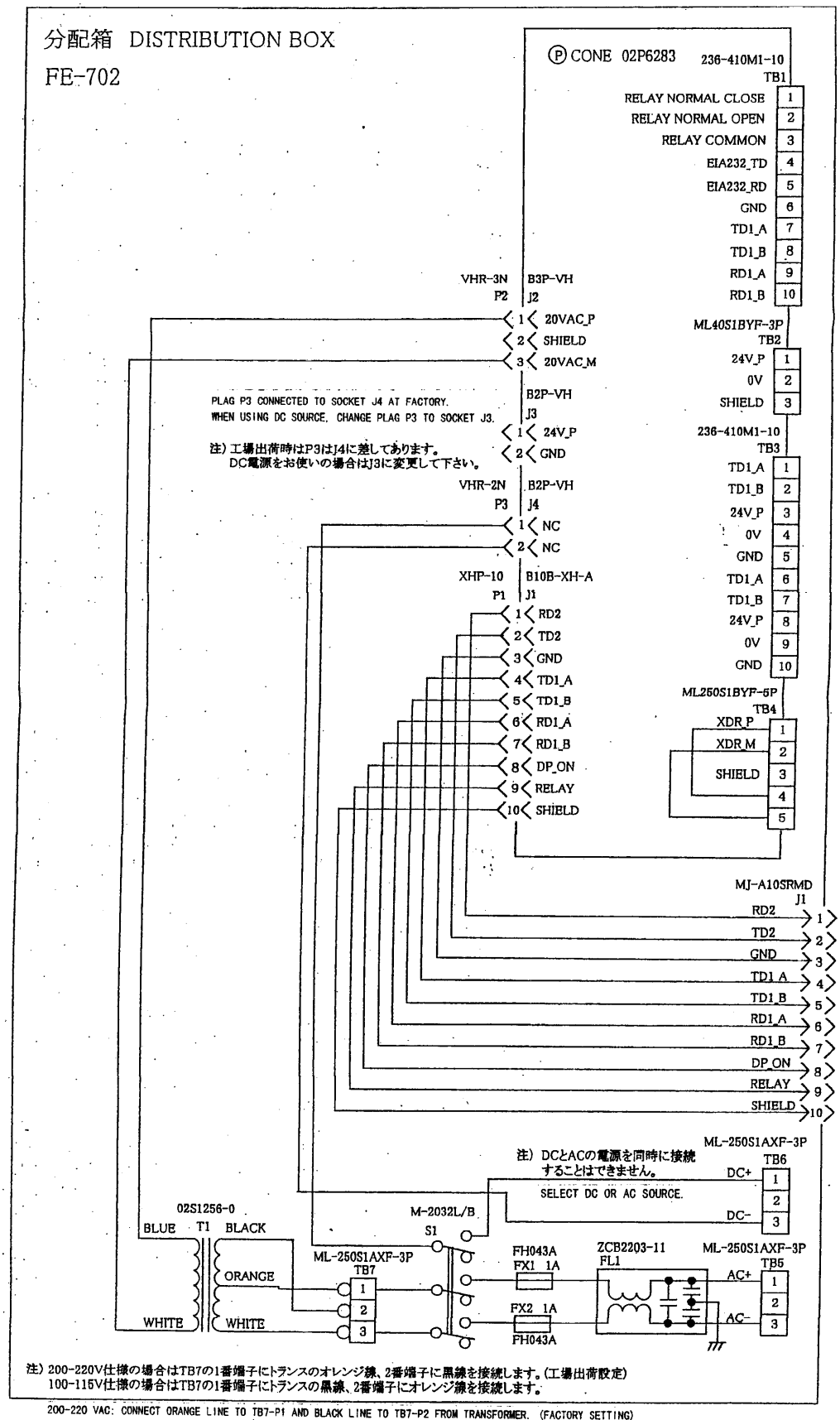
DRAWN Dec 13 '99 T.YAMASAKI			TYPE 02P6282
CHECKED Dec 14 '99 K.KASUNOKI			名称 メモリ基板
APPROVED Dec 14 '99 K.KASUNOKI	FE-701	1B 3	回路図
SCALE / MASS kg	APPLICABLE TO; (MODEL)	BLOCK NO.	NAME MEM PCB
DWG NO. C2366-K10- A	02-129-1301- 0		SCHEMATIC DIAGRAM



DRAWN Dec 13'99 T.YAMASAKI			TYPE 02P6250
CHECKED Dec14'99 K.KUSUNOKI			名称 パネル基板
APPROVED Dec14'99 K.KUSUNOKI	FE-701	1B 4	回路図
SCALE / MASS kg	APPLICABLE TO; (MODEL)	BLOCK NO.	NAME PNL PCB
DWG NO. C2366-K11- A	02-123-1301- 3		SCHEMATIC DIAGRAM

分配箱 DISTRIBUTION BOX

FE-702



注) 200-220V仕様の場合はTB7の1番端子にトランスのオレンジ線、2番端子に黒線を接続します。(工場出荷設定)
100-115V仕様の場合はTB7の1番端子にトランスの黒線、2番端子にオレンジ線を接続します。

200-220 VAC: CONNECT ORANGE LINE TO TB7-P1 AND BLACK LINE TO TB7-P2 FROM TRANSFORMER. (FACTORY SETTING)
110-115 VAC: CONNECT BLACK LINE TO TB7-P1 AND ORANGE LINE TO TB7-P2 FROM TRANSFORMER.

DRAWN Dec/0 99 T.YAMASAKI			TYPE FE-702
CHECKED Dec 10 '99 K.Kusunoki			名称 分配器（総合）
APPROVED Dec/0 '99 K.Kusunoki		FE-700	回路図
SCALE /	MASS kg	APPLICABLE TO; (MODEL)	BLOCK NO.	NAME DISTRIBUTION BOX(GENERAL)
DWG NO. C2366-K02- B		02-129-1003- 2		SCHEMATIC DIAGRAM

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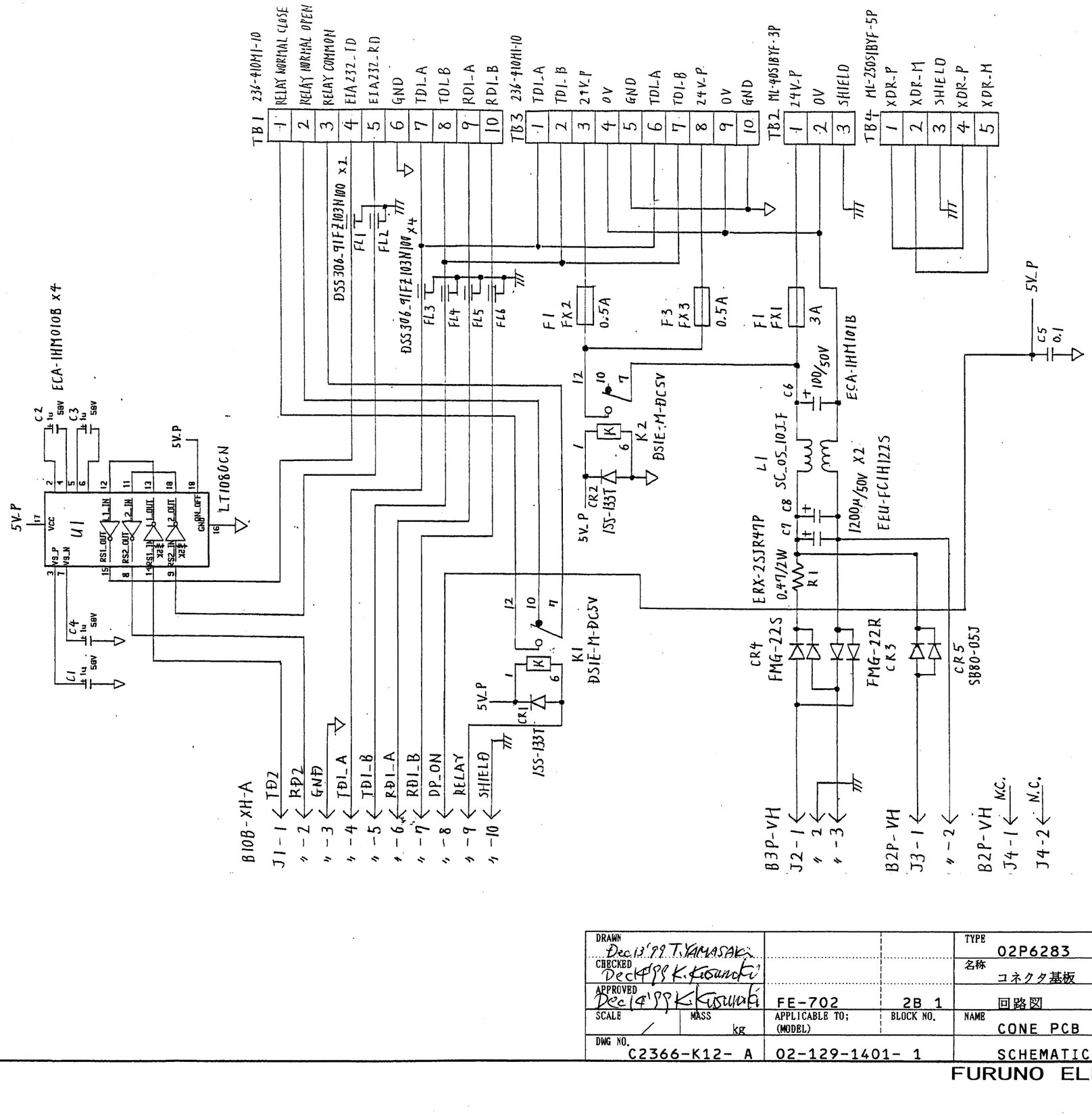
FURUNO



DRAWN Dec13'99 T.YAMASAKI			TYPE 02P6283
CHECKED Dec14'99 K.Kusunoki			名称 コネクタ基板
APPROVED Dec14'99 K.Kusunoki	FE-702	2B 1	回路図
SCALE / MASS kg	APPLICABLE TO; (MODEL)	BLOCK NO.	NAME CONE PCB
DWG NO. C2366-K12- A	02-129-1401- 1		SCHEMATIC DIAGRAM