17MB12
TFT TV
SERVICE MANUAL

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1 INTRODUCTION

17MB12 Main Board is a single board IDTV project, consists of Micronas and NEC concept. VCT_Pro and Emma2LL are used as controller for TV and IDTV side respectively. VCT_Pro is capable of handling Audio processing, video processing, motion adaptive upconversion (MAU), Scaling-Display processing and FPD control (DPS), unified memory for audio video and Text, 3D comb filter-PC connectivity, OSD and text processing. Emma2LL is capable of handling MPEG1 and MPEG2 decoding and provide nearly all the functionality required to realise a high performance and cost-effective digital set-top box or integrated digital TV.
TV supports DVB-T reception and following analog receptions PAL, SECAM, NTSC colour standards and multiple transmission standards as B/G, D/K, I/I', and L/L' including German and NICAM stereo.

Sound system output is supplying 2x8W (10%THD) for stereo 8Ω speakers.
Supported peripherals are:

1 RF input VHF1, VHF3, UHF @ 75Ohm
1 FAV input
2 SCART sockets
1 SVHS input
1 Stereo Headphone input
1 YPbPr
1 PC input
2 HDMI input
1 Stereo audio input for PC and YPbPr
1 Stereo audio output
1 Subwoofer
1 Spdif

2 TUNER

Vertical mounted digital tuner is used in the product, which is suitable for analog reception with DRX-A. The tuning is available through the digitally controlled I2C bus (PLL). Below you will find info on the Tuner in use.

2.1 General description of DTT71307:

The DTT 755XX is designed for digital terrestrial reception in VHFIII and UHF, compliance with the European digital terrestrial standard ETS 300 744. In addition the tuner covers all analog channels from 44,25 MHz to 863,25 MHz. It is a two band concept VHF and UHF,with VHF switch between VHF low (VHF I) and VHF high (VHF III).

2.2 Features of DTT71307:

- VHF I/III/ UHF frequency range
- . Antenna loop through (optional)
- . Low phase noise

- ¸ High level digital IF outputs
- ¸ RF-Modulator input for loop through to TV output (optional)
- ¸ Wide band AGC
- ¸ Indoor Antenna power feed through (optional)

2.3 Pinning:

Pin	Symbol	Description
1	MOI	RF modulator input or antenna power supply input
2	RAG	RF AGC output / input
3	CAS	Chip I2C address select
4	SCL	I2C serial clock
5	SDA	I2C serial data
6	VC1	+5V supply voltage for loop through
7	VC2	+5V supply voltage for tuner
8	XTO/GPIO	4MHz crystal oscillator output or GPIO
9	VTS	Open or +33V
10	IF2	IF output symmetrical
11	IF1	IF output symmetrical

3 AUDIO AMPLIFIER STAGE WITH TDA8932

3.1 General Description

The TDA8932 device is the high-power version that delivers an output power of 2 x 10 WRMS to 2 x 25 WRMS in a Single Ended (SE) configuration or 10 WRMS to 50 WRMS in a Bridge Tied Load (BTL) configuration. The TDA8933 device is the low-power version that delivers an output power of 2 x 5 WRMS to 2 x 15 WRMS in a Single Ended (SE) configuration or 10 WRMS to 20 WRMS in a Bridge Tied Load (BTL) configuration. This high efficiency SMA device is designed to operate without a heat sink and has the flexibility to operate from either an asymmetrical supply or a symmetrical supply with a wide range (10 V to 36 V or +/-5 V to +/-18 V). The TDA8932/33 device utilizes two advanced features, respectively the thermal fold back and the cycle-by-cycle current limiting to avoid audio holes (interruptions) during normal operation.

3.2 Features

• High efficiency Class-D audio amplifier due to a low RDS_ON
• Operates from a wide voltage range 10 V to 36 V (asymmetrical) or +/-5 V to +/-18 V (symmetrical)
• Maximum power capability:
• TDA8932 is 2 x 25 WRMS maximum in 4 Ω SE without heat sink
• TDA8933 is 2 x 15 WRMS maximum in 8 Ω SE without heat sink
• Cycle-by-cycle current limiting to avoid interruption during normal operation
• Unique Thermal Foldback (TF) to avoid interruption during normal operation
• Integrated Half Supply Voltage (HVP) buffers for reference and SE output capacitance (asymmetrical supply)
• Internal logic for pop-free power supply on/off cycling
• Low standby-current in SLEEP-mode for power saving regulations

3.3 Applications

- Flat-TV application
- Flat panel monitors
- Multimedia systems
- Wireless speakers
- Micro systems

3.4 Pinning

SYMBOL	PIN	DESCRIPTION
$V_{SSD(HW)}$	1	Negative digital supply voltage and handle-wafer connection (heat spreader). With an asymmetrical supply, the $V_{SSD(HW)}$ is connected to the system ground. With a symmetrical supply, the $V_{SSD(HW)}$ is connected to the negative supply line.
IN1P	2	Positive audio input for power stage 1.
IN1N	3	Negative audio input for power stage1.
DIAG	4	Input/output to indicate the FAULT mode. DIAG has an internal pull-up and should left floating when un used.
ENGAGE	5	Input with internal pull-up to switch between MUTE mode and OPERATING mode.
POWERUP	6	Input to switch between SLEEP mode and mute mode.
CGND	7	Control ground, reference for POWERUP, ENGAGE and DIAG. This CGND is connected to the system ground.
V_{DDA}	8	Positive analogue supply voltage.
V_{SSA}	9	Negative analogue supply voltage.
OSCREF	10	Input to set the frequency for the internal oscillator (master configuration). In slave configuration this pin should be connected to V_{SSA}.
HVPREF	11	Decoupling of the internal half-supply voltage reference (asymmetrical supply). With a symmetrical supply, this pin should be connected to the supply ground.
INREF	12	Decoupling for the input reference voltage.
TEST	13	Test signal input for testing purpose only (leave floating or connect to V_{SSA}).
IN2N	14	Positive audio input for power stage 2.
IN2P	15	Negative audio input for power stage 2.
$V_{SSD(HW)}$	16	Negative digital supply voltage and handle-wafer connection (heat spreader).
$V_{SSD(HW)}$	17	Negative digital supply voltage and handle-wafer connection (heat spreader).
DREF	18	Decoupling of the internal 5 V regulator.
HVP2	19	Half-supply voltage buffer for the SE capacitor of output 2 (asymmetrical supply). With a symmetrical supply, this pin should be left floating (n.c.).
V_{DDP2}	20	Positive supply voltage for the power stage 2.
BOOT2	21	Bootstrap for the high-side driver, power stage 2.
OUT2	22	PWM output, power stage 2.
V_{SSP2}	23	Negative supply voltage for the power stage 2.
STAB2	24	Decoupling of the internal 11 V regulator for power stage 2.
STAB1	25	Decoupling of the internal 11 V regulator for power stage 1.
V_{SSP1}	26	Negative supply voltage for the power stage 1.
OUT1	27	PWM output, power stage 1.
BOOT1	28	Bootstrap for the high-side driver, channel 1.
V_{DDP1}	29	Positive supply voltage for the power stage 2.
HVP1	30	Half-supply voltage buffer for the SE capacitor of output 1 (asymmetrical supply). With a symmetrical supply, this pin should be left floating (n.c.).
OSCIO	31	Oscillator input in the slave configuration or the oscillator output in the master configuration.
$V_{SSD(HW)}$	32	Negative digital supply voltage and handle-wafer connection (heat spreader).

4 POWER STAGE

The DC voltages required at various parts of the chassis and inverters are provided by a main power supply unit and power interface board. The main power supply unit is designed for 24V and 12V DC supply. Power stage which is on-chasis generates +24V

for audio amplifier, 1.8V and 3.3V stand by voltage and 8V, 12V, 5V and 3.3Vsupplies for other different parts of the chassis.

5 MICROCONTROLLER (VCTP)

5.1 General Features

The VCT 7wxyP is dedicated to high-quality FPD and double-scan TV sets. Modular design and deep-submicron technology allow the economic integration of features in LCD/plasma TV and in all classes of double-scan CRT TV sets. The VCT 7wxyP family is based on approved functional blocks of existing Micronas products for audio and video.
Each member of the family contains the entire audio, video, up-conversion processing for 4:3 and 16:9 50/60 Hz progressive or 100/120 Hz interlaced stereo TV sets and the control/data interface for flat-panel displays. The integrated microcontroller is supported by a powerful OSD and graphics generator with integrated teletext acquisition.

5.1.1 Controller:

- High-performance 8-bit microcontroller, 8051 compatible
- Up to 512 kByte in system program Flash
- WST, PDC, VPS, and WSS acquisition
- Closed caption and V-chip acquisition
- Up to 10 page on chip teletext memory
- Up to 1000 pages with internal memory
- Up to 30 GPIO

5.1.2 Audio:

- Multistandard TV-sound demodulation:
  - -All A2/NICAM standards
  - -BTSC/SAP with DBX
  - -EIA-J
- Baseband sound processing for loudspeaker channel:
  - -Volume, bass, treble, loudness, balance
  - -Spatial effect (e.g. pseudo stereo)
  - -Micronas AROUND
  - (Virtual Dolby Surround optional)
  - -Micronas BASS
  - -BBE
  - -SRS WOW
  - -SRS TruSurround XT
  - -Lipsync function

5.1.3 Video:

- CVBS, S-VHS, YCrCb and RGB inputs
- HDTV YPrPb and RGB inputs
- ITU656 input
- Linedoubling with vertical detail enhancement (without internal memory)

- State of the art motion adaptive up conversion (with internal memory)
- 4H adaptive comb filter for PAL/NTSC (without internal memory)
- 3D comb filter for PAL/NTSC (with internal memory) (Optional)
- Internal SDR RAM interface
- Powerful horizontal and vertical scaling inclusive
- Nonlinear horizontal scaling “panorama vision”
- picture adaptive image improvements (DCE, LSE, CTI, SCE, NCE)
- non-linear colorspace enhancement (NCE) with 32 programmable slopes and sections per RGB component (blue stretch, static black stretch, gamma correction).
- Dynamic contrast enhancement (DCE) (histogram based black stretch with peak black and activity detection and contrast adaption)
- Luma sharpness enhancement (LSE)
- Color transient improvement (CTI)
- Selective color enhancement (SCE) for skin tone correction, blue and green stretch

5.2 Multistandard Sound Processor (MSP) Features

The MSP receives the analog Sound IF signal from the tuner and converts it to digital with its internal SIF-AD converter. The MSP is able to demodulate all TV sound standards worldwide including the digital NICAM system. TV stereo sound standards that are unavailable for a specific **VCTP** version are processed in analog mono sound of the standard. In that case, stereo or bilingual processing will not be possible.

- Sound IF input
- Worldwide FM/AM-mono sound demodulation
- FM stereo sound demodulation (A2, EIA-J)
- BTSC/SAP demodulation with DBX
- NICAM demodulation
- FM radio & RDS/RBDS demodulation
- Automatic standard detection
- automatic volume correction (AVC)
- Automatic sound select
- Baseband processing for loudspeaker channel:
  volume, bass, treble, loudness, balance
  - -spatial effect (e.g. pseudo stereo)
  - -Micronas AROUND
  - -Micronas BASS
  - -SRS WOW (optional)
  - -SRS TruSurround XT (optional)
  - -delayline for lipsync function (shared memory)
  - -Virtual Dolby Surround (optional)
- 1 I2S input for external ATSC/DVD decoder
- 1 I2S interface for audio delayline
- 1 SPDIF output
- Audio i/o switches
  - -4 analog stereo line inputs and 2 analog stereo line outputs (configurable 5 analog stereo line inputs and 1 analog stereo line output)
  - -1 analog stereo loudspeaker output

-1 analog subwoofer output
-1 analog stereo headphone output

5.3 Video Features

The TVT is a Teletext decoder for decoding World System Teletext data, as well as Video Programming System (VPS), Program Delivery Control (PDC), and Wide-Screen Signalling (WSS) data used for PALplus transmissions (line 23). The device also supports Closed Caption acquisition and decoding.
The TVT provides an integrated general-purpose, fully 8051-compatible microcontroller with television-specific hardware features. The microcontroller has been enhanced to provide powerful features such as memory banking, data pointer, additional interrupts, shared memory access etc.
The TVT has an internal XRAM of 32 KB and a BOOT ROM of 4 KB. For operation the code is fetched from a 16bit FLASH, which can be addressed up to 1 MByte.
The controller with dedicated hardware does most of the internal TTX acquisition processing, transfers data to/from external memory interface, and receives/transmits data via I2C-bus interface. In combination with dedicated hardware, the slicer stores TTX data in a VBI buffer of 1 KB. The microcontroller firmware performs all the acquisition tasks (hamming and parity checks, page search, and evaluation of header control bits) once per field. Additionally, the firmware can provide high-end Teletext features like Packet-26 handling, FLOF/TOP and list-pages. The interface-to-user software is optimized for minimal overhead. TVT is realized in deep submicron technology with 1.8 V supply voltage and 3.3 V I/O (TTL compatible).

- 16 analog video inputs (4xCVBS/Y/C + 3xRGB/YCrCb/YPrPb)
- Video input switch matrix
- 3 analog video outputs (integrated Y+C adder)
- 24-bit RGB/H/V/clk input (e.g. ext. DVI decoder) or 656 8bit input
- 656 8bit input/output (e. g. for external high-end up conversion by FRCA)
- Multi-standard color decoder PAL/NTSC/SECAM including all substandards
- 2D adaptive comb filter for PAL/NTSC with vertical peaking
- 3D-comb filter for PAL/NTSC (Optional)
- Macrovision compliant multi-standard sync processing
- Trilevel sync slicer for HDTV
- Macrovision detection
- High-quality soft mixer controlled by Fast Blank (alpha blending)
- Fastblank monitor via I2C
- Noise measurement
- Letterbox detection (auto-wide)
- Split screen (OSD and video side by side) and AV PIP

5.4 Controller Features

The TVT is a Teletext decoder for decoding World System Teletext data, as well as Video Programming System (VPS), Program Delivery Control (PDC), and Wide-Screen Signalling (WSS) data used for PALplus transmissions (line 23). The device also supports Closed Caption acquisition and decoding.
The TVT provides an integrated general-purpose, fully 8051-compatible microcontroller with television-specific hardware features. The microcontroller has been enhanced to

provide powerful features such as memory banking, data pointer, additional interrupts, shared memory access etc.

- High performance 8-bit microcontroller, 8051 instruction set compatible
- 81 MHz system clock, two machine cycles per instruction
- On-chip debug support (OCDS)
- Up to 512 kByte in system program Flash
- 256 byte on-chip program RAM
- 128 byte on-chip extended stack RAM
- 4-level, 24-input interrupt controller
- Patch module for 16 ROM locations
- Two 16-bit reloadable timers
- Capture compare timer for infrared decoding
- Watchdog timer
- Uart
- Real time clock
- PWM units (2 channels 14-bit, 6 channels 8-bit)
- 8-bit ADC (4 channels)
- I2C bus master/slave interface
- Up to 32 programmable I/O ports

5.5 OSD & Teletext Features

The on-chip display unit for displaying Level 1.5 Teletext data can also be used for customer-defined onscreen displays.
The TVT has an internal XRAM of 32 KB and a BOOT ROM of 4 KB. For operation the code is fetched from a 16bit FLASH, which can be addressed up to 1 MByte.
In combination with dedicated hardware, the slicer stores TTX data in a VBI buffer of 1 KB. The microcontroller firmware performs all the acquisition tasks (hamming and parity checks, page search, and evaluation of header control bits) once per field. Additionally, the firmware can provide high-end Teletext features like Packet-26 handling, FLOF/TOP and list-pages. The interface-to-user software is optimized for minimal overhead.

5.6 Port Allocation

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
1		656O6 P4_6 TDOFW	IN/OUT	RtoGND	Digital 656 Bit 6 Output Port 4, Bit 6 Input/Output JTAG Interface Data Output (FW Controller)
2		656O5 P4_5 TDIFW	IN/OUT	RtoGND	Digital 656 Bit 5 Output Port 4, Bit 5 Input/Output JTAG Interface Data Input (FW Controller)
3		656O4 P4_4 TMSFW	IN/OUT	RtoGND	Digital 656 Bit 4 Output Port 4, Bit 4 Input/Output JTAG Interface Mode Select Input (FW Contr.)
4		656O3 P4_3 TCLK	IN/OUT	RtoSUP	Digital 656 Bit 3 Output Port 4, Bit 3 Input/Output JTAG Interface Clock Input (TV Controller)
5		656O2 P4_2 TDO	IN/OUT	RtoGND	Digital 656 Bit 2 Output Port 4, Bit 2 Input/Output JTAG Interface Data Output (TV Controller)

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
6		656O1 P4_1 TDI	IN/OUT	RtoGND	Digital 656 Bit 1 Output Port 4, Bit 1 Input/Output JTAG Interface Data Input (TV Controller)
7		656O0 P4_0 TMS	IN/OUT	RtoGND	Digital 656 Bit 0 Output (LSB) Port 4, Bit 0 Input/Output JTAG Interface Mode Select Input (TV Contr.)
8		RESETQ	IN/OUT	OBL	$\overline{\text{Reset}}$ Input/Output
9		AIN1R	IN	LV	Analog Audio 1 Input, Right
10		AIN1L	IN	LV	Analog Audio 1 Input, Left
11		AIN2R	IN	LV	Analog Audio 2 Input, Right
12		AIN2L	IN	LV	Analog Audio 2 Input, Left
13		AIN3R	IN	LV	Analog Audio 3 Input, Right
14		AIN3L	IN	LV	Analog Audio 3 Input, Left
15		AIN4R	IN	LV	Analog Audio 4 Input, Right
16		AIN4L	IN	LV	Analog Audio 4 Input, Left
17		VREFAU	ANA	OBL	Reference Voltage, Audio
18		VSUP8.0AU	SUPPLY	OBL	Supply Voltage Analog Audio, 8.0 V
19		GNDA	SUPPLY	OBL	Ground Analog Audio, Platform Ground
20		SGND	ANA	OBL	Analog Signal GND
21		AOUT2R AIN5R	IN/OUT	LV	Analog Audio 2 Output, Right Analog Audio 5 Input, Right
22		AOUT2L AIN5L	IN/OUT	LV	Analog Audio 2 Output, Left Analog Audio 5 Input, Left
23		AOUT1R	OUT	LV	Analog Audio 1 Output, Right
24		AOUT1L	OUT	LV	Analog Audio 1 Output, Left
25		HEADPHONER	OUT	LV	Analog Headphone Output, Right
26		HEADPHONEL	OUT	LV	Analog Headphone Output, Left
27		SPEAKERR	OUT	LV	Analog Loudspeaker Output, Right
28		SPEAKERL	OUT	LV	Analog Loudspeaker Output, Left
29		SUBWOOFER TEST	IN/OUT	LV	Analog SUBWOOFER Output Test Input
30		VREFSIF	ANA	OBL	Reference Voltage, Audio SIF
31		SIFIN+	IN	GND	Differential Sound IF Input
32		SIFIN-	IN	GND	Differential Sound IF Input
33		VSUP5.0	SUPPLY	OBL	Supply Voltage Analog, 5.0 V

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
34		GNDA	SUPPLY	OBL	Ground Analog, Platform Ground
35		GND3.3DIG	SUPPLY	OBL	Ground Digital Interfaces
36		VSUP3.3DIG	SUPPLY	OBL	Supply Voltage Digital Interfaces, 3.3 V
37		SPDIF_OUT	OUT	LV	SPDIF Output
38		I2S_DA_IN	IN	GND	Audio Bus Data Input
39		I2S_CL	IN	GND	Audio Bus Clock Input
40		I2S_WS	IN	GND	Audio Bus Word Strobe Input
41		I2S_DEL_OUT	OUT/IN	LV	Audio Delay Line Bus Data Output/Input
42		I2S_DEL_IN	IN/OUT	GND	Audio Delay Line Bus Data Input/Output
43		I2S_DEL_CL	OUT/IN	LV	Audio Delay Line Bus Clock Output/Input
44		I2S_DEL_WS	OUT/IN	LV	Audio Delay Line Word Strobe Output/Input
45		VSUP3.3RAM	SUPPLY	OBL	Supply Voltage Ram, 3.3 V
46		GND3.3RAM	SUPPLY	OBL	Ground Ram
47		DVS	IN	GND	Digital or Analog Video VSYNC HD Input
48		DEN	IN	GND	Digital Video Enable Input
49		DCLK	IN	GND	Digital Video Clock Input
50		DRI7	IN	GND	Digital Video Red 7 Input
51		DRI6	IN	GND	Digital Video Red 6 Input
52		DRI5	IN	GND	Digital Video Red 5 Input
53		DRI4	IN	GND	Digital Video Red 4 Input
54		DRI3	IN	GND	Digital Video Red 3 Input
55		DRI2	IN	GND	Digital Video Red 2 Input
56		DRI1	IN	GND	Digital Video Red 1 Input
57		DRI0	IN	GND	Digital Video Red 0 Input (LSB)
58		DGI7	IN	GND	Digital Video Green 7 Input
59		DGI6	IN	GND	Digital Video Green 6 Input
60		DGI5	IN	GND	Digital Video Green 5 Input
61		DGI4	IN	GND	Digital Video Green 4 Input
62		DGI3	IN	GND	Digital Video Green 3 Input
63		DGI2	IN	GND	Digital Video Green 2 Input
64		DGI1	IN	GND	Digital Video Green 1 Input

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
65		DGI0	IN	GND	Digital Video Green 0 Input (LSB)
66		DBI7	IN	GND	Digital Video Blue 7 Input
67		DBI6	IN	GND	Digital Video Blue 6 Input
68		DBI5	IN	GND	Digital Video Blue 5 Input
69		DBI4	IN	GND	Digital Video Blue 4 Input
70		DBI3	IN	GND	Digital Video Blue 3 Input
71		DBI2	IN	GND	Digital Video Blue 2 Input
72		DBI1	IN	GND	Digital Video Blue 1 Input
73		DBI0	IN	GND	Digital Video Blue 0 Input (LSB)
74		GND3.3DRI	SUPPLY	OBL	Ground Digital Ram Interface
75		VSUP3.3DRI	SUPPLY	OBL	Supply Voltage Digital Ram Interface, 3.3 V
76		GND3.3COM	SUPPLY	OBL	Ground Common
77		VSUP3.3COM	SUPPLY	OBL	Supply Voltage Common, 3.3V
78		XTALIN	IN	OBL	Analog Crystal Input
79		XTALOUT	OUT	OBL	Analog Crystal Output
80		CLKOUT	OUT	RtoGND	Digital 20MHz Clock Output
81		VSO	OUT	RtoGND	Vertical Sync Output, Frontend
82		HSO	OUT	RtoGND	Horizontal Sync Output, Frontend
83		SCL	IN/OUT	OBL	I^2C Bus Clock Input/Output
84		SDA	IN/OUT	OBL	I^2C Bus Data Input/Output
85		GND3.3FL	SUPPLY	OBL	Ground Flash
86		VSUP3.3FL	SUPPLY	OBL	Supply Voltage Flash, 3.3 V
87		P2_0	IN/OUT	RtoGND	Port 2, Bit 0 Input/Output
88		P2_1	IN/OUT	RtoGND	Port 2, Bit 1 Input/Output
89		P2_2	IN/OUT	RtoGND	Port 2, Bit 2 Input/Output
90		P2_3	IN/OUT	RtoGND	Port 2, Bit 3 Input/Output
91		P2_4 TDI	IN/OUT	RtoGND	Port 2, Bit 4 Input/Output JTAG Interface Data Input
92		P2_5 TMS	IN/OUT	RtoGND	Port 2, Bit 5 Input/Output JTAG Interface Mode Select Input
93		OSDV DBO2_0	IN/OUT	RtoGND	Graphic Vertical Sync Input/Output Channel 2 Digital 0 Blue Output (LSB)

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
94		OSDH DBO2_1	IN/OUT	RtoGND	Graphic Horizontal Sync Input/Output Channel 2 Digital 1 Blue Output
95		GND3.3IO1	SUPPLY	OBL	Ground Digital Input/Output Port 1
96		VSUP3.3IO1	SUPPLY	OBL	Supply Voltage Input/Output Port 1, 3.3 V
97		OSDCLK DBO2_2	IN/OUT	RtoGND	Graphic Clock Input/Output Channel 2 Digital 2 Blue Output
98		OSDFSW DBO2_3	IN/OUT	RtoGND	Graphic Fast Switch Input/Output Channel 2 Digital 3 Blue Output
99		OSDHCS1 P3_6 DBO2_4	IN/OUT	RtoGND	Graphic Half Contrast 1 Input/Output Port 3, Bit 6 Input/Output Channel 2 Digital 4 Blue Output
100		OSDHCS0 P3_7 DBO2_5	IN/OUT	RtoGND	Graphic Half Contrast 0 Input/Output (LSB) Port 3, Bit 7 Input/Output Channel 2 Digital 5 Blue Output
101		OSDB3 P3_5 DBO2_6	IN/OUT	RtoGND	Graphic Blue 3 Input/Output (MSB) Port 3, Bit 5 Input/Output Channel 2 Digital 6 Blue Output
102		OSDB2 P3_4 DBO2_7	IN/OUT	RtoGND	Graphic Blue 2 Input/Output Port 3, Bit 4 Input/Output Channel 2 Digital 7 Blue Output (MSB)
103		OSDB1 DGO2_0	IN/OUT	RtoGND	Graphic Blue 1 Input/Output Channel 2 Digital 0 Green Output (LSB)
104		OSDB0 DGO2_1	IN/OUT	RtoGND	Graphic Blue 0 Input/Output Channel 2 Digital 1 Green Output
105		OSDG3 P3_3 DGO2_2	IN/OUT	RtoGND	Graphic Green 3 Input/Output (MSB) Port 3, Bit 3 Input/Output Channel 2 Digital 2 Green Output
106		OSDG2 P3_2 DGO2_3	IN/OUT	RtoGND	Graphic Green 2 Input/Output Port 3, Bit 2 Input/Output Channel 2 Digital 3 Green Output
107		OSDG1 DGO2_4	IN/OUT	RtoGND	Graphic Green 1 Input/Output Channel 2 Digital 4 Green Output
108		OSDG0 DGO2_5	IN/OUT	RtoGND	Graphic Green 0 Input/Output Channel 2 Digital 5 Green Output
109		OSDR3 P3_1 DGO2_6	IN/OUT	RtoGND	Graphic Red 3 Input/Output (MSB) Port 3, Bit 1 Input/Output Channel 2 Digital 6 Green Output
110		OSDR2 P3_0 DGO2_7	IN/OUT	RtoGND	Graphic Red 2 Input/Output Port 3, Bit 0 Input/Output Channel 2 Digital 7 Green Output (MSB)
111		OSDR1 DRO2_0	IN/OUT	RtoGND	Graphic Red 1 Input/Output Channel 2 Digital 0 Red Output (LSB)

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
112		OSDR0 DRO2_1	IN/OUT	RtoGND	Graphic Red 0 Input/Output (LSB) Channel 2 Digital 1 Red Output
113		GND3.3IO1	SUPPLY	OBL	Ground Digital Input/Output Port 1
114		VSUP3.3IO1	SUPPLY	OBL	Supply Voltage Input/Output Port 1, 3.3 V
115		PCS5 P2_7	IN/OUT	RtoGND	Flat Panel Control Select 5 Output Port 2, Bit 7 Input/Output
116		PCS4 P2_6	IN/OUT	RtoGND	Flat Panel Control Select 4 Output Port 2, Bit 6 Input/Output
117		PCS3 P4_1	IN/OUT	RtoGND	Flat Panel Control Select 3 DE2 Output Port 4, Bit 1 Input/Output
118		PCS2 P4_0	IN/OUT	RtoGND	Flat Panel Control Select 2 DE1 Output Port 4, Bit 0 Input/Output
119		PCS1 P4_3	IN/OUT	RtoGND	Flat Panel Control Select 1 H Output Port 4, Bit 3 Input/Output
120		PCS0 P4_2	IN/OUT	RtoGND	Flat Panel Control Select 0 V Output Port 4, Bit 2 Input/Output
121		PCLK2	OUT	LV	Flat Panel Control Clock 2 Output
122		PCLK1	OUT	LV	Flat Panel Control Clock 1 Output
123		GND1.8DIG	SUPPLY	OBL	Ground Digital Core
124		VSUP1.8DIG	SUPPLY	OBL	Supply Voltage Digital Core, 1.8 V
125		DBO1_0 DRO2_2 LVDSA_4P	OUT	LV	Channel 1 Digital 0 Blue Output[1] (LSB) Channel 2 Digital 2 Red Output[1] LVDS Channel 1 bit 4 Positive Output[2]
126		DBO1_1 DRO2_3 LVDSA_4N	OUT	LV	Channel 1 Digital 1 Blue Output[1] Channel 2 Digital 3 Red Output[1] LVDS Channel 1 bit 4 Negative Output[2]
127		DBO1_2 DRO2_4 VSUP3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 2 Blue Output[1] Channel 2 Digital 4 Red Output[1] Supply Digital Voltage LVDS[2] Port, 3.3 V
128		DBO1_3 DRO2_5 LVDSA_3P	OUT	LV	Channel 1 Digital 3 Blue Output[1] Channel 2 Digital 5 Red Output[1] LVDS Channel 1 bit 3 Positive Output[2]
129		DBO1_4 DRO2_6 LVDSA_3N	OUT	LV	Channel 1 Digital 4 Blue Output[1] Channel 2 Digital 6 Red Output[1] LVDS Channel 1 bit 3 Negative Output[2]
130		DBO1_5 DRO2_7 GND3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 5 Blue Output[1] Channel 2 Digital 7 Red Output[1] (MSB) Ground Digital LVDS[2], 3.3 V
131		DBO1_6 DBO1_0 LVDSA_CLKP	OUT	LV	Channel 1 Digital 6 Blue Output[1] Channel 1 Digital 0 Blue Output[1] (LSB) LVDS Channel 1 Clock Positive Output[2]

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
132		DBO1_7 DBO1_1 LVDSA_CLKN	OUT	LV	Channel 1 Digital 7 Blue Output[1)] Channel 1 Digital 1 Blue Output[1)] LVDS Channel 1 Clock Negative Output[2)]
133		VSUP3.3IO2 VSUP3.3LVDS	SUPPLY	OBL	Supply Digital Output[1)] Port 2 Supply Digital Voltage LVDS[2)], 3.3 V
134		GND3.3IO2 LVDSA_2P	SUPPLY OUT	OBL LV	Ground Voltage Output[1)] Port 2, 3.3 V LVDS Channel 1 bit 2 Positive Output[2)]
135		DBO1_8 DBO1_2 LVDSA_2N	OUT	LV	Channel 1 Digital 8 Blue Output[1)] Channel 1 Digital 2 Blue Output[1)] LVDS Channel 1 bit 2 Negative Output[2)]
136		DBO1_9 DBO1_3 GND3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 9 Blue Output[1)] (MSB) Channel 1 Digital 3 Blue Output[1)] Ground Digital LVDS[2)], 3.3 V
137		DGO1_0 DBO1_4 LVDSA_1P	OUT	LV	Channel 1 Digital 0 Green Output[1)] (LSB) Channel 1 Digital 4 Blue Output[1)] LVDS Channel 1 bit 1 Positive Output[2)]
138		DGO1_1 DBO1_5 LVDSA_1N	OUT	LV	Channel 1 Digital 1 Green Output[1)] Channel 1 Digital 5 Blue Output[1)] LVDS Channel 1 bit 1 Negative Output[2)]
139		DGO1_2 DBO1_6 VSUP3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 2 Green Output[1)] Channel 1 Digital 6 Blue Output[1)] Supply Digital Voltage LVDS[2)], 3.3 V
140		DGO1_3 DBO1_7 LVDSA_0P	OUT	LV	Channel 1 Digital 3 Green Output[1)] Channel 1 Digital 7 Blue Output[1)] (MSB) LVDS Channel 1 bit 0 Positive Output[2)]
141		DGO1_4 DGO1_0 LVDSA_0N	OUT	LV	Channel 1 Digital 4 Green Output[1)] Channel 1 Digital 0 Green Output[1)] (LSB) LVDS Channel 1 bit 0 Negative Output[2)]
142		DGO1_5 DGO1_1 VSUP1.8LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 5 Green Output[1)] Channel 1 Digital 1 Green Output[1)] Supply Analog Voltage LVDS[2)], 1.8 V
143		DGO1_6 DGO1_2 REXT	OUT ANA	LV OBL	Channel 1 Digital 6 Green Output[1)] Channel 1 Digital 2 Green Output[1)] LVDS External Resistor[2)]
144		DGO1_7 DGO1_3 GND1.8LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 7 Green Output[1)] Channel 1 Digital 3 Green Output[1)] Ground Analog LVDS[2)], 1.8 V
145		DGO1_8 DGO1_4 LVDSB_3P	OUT	LV	Channel 1 Digital 8 Green Output[1)] Channel 1 Digital 4 Green Output[1)] Dual-LVDS Channel 2 bit 3 Positive Output[2)]
146		DGO1_9 DGO1_5 LVDSB_3N	OUT	LV	Channel 1 Digital 9 Green Output[1)] (MSB) Channel 1 Digital 5 Green Output[1)] Dual-LVDS Channel 2 bit 3 Negative Output[2)]

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
147		DRO1_0 DGO1_6 GND3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 0 Red Output[1] (LSB) Channel 1 Digital 6 Green Output[1] Ground Digital LVDS[2], 3.3 V
148		DRO1_1 DGO1_7 LVDSBCLKP	OUT	LV	Channel 1 Digital 1 Red Output[1] Channel 1 Digital 7 Green Output[1] (MSB) Dual-LVDS Channel 2 Clock Positive Output[2]
149		GND3.3IO2 LVDSBCLKN	SUPPLY OUT	OBL LV	Ground Digital Output[1] Port 2 Dual-LVDS Channel 2 Clock Negative Output[2]
150		VSUP3.3IO2 VSUP3.3LVDS	SUPPLY	OBL	Supply Voltage Output[1] Port 2, 3.3 V Supply Digital Voltage LVDS[2], 3.3 V
151		DRO1_2 DRO1_0 LVDSB_2P	OUT	LV	Channel 1 Digital 2 Red Output[1] Channel 1 Digital 0 Red Output[1] (LSB) Dual-LVDS Channel 2 bit 2 Positive Output[2]
152		DRO1_3 DRO1_1 LVDSB_2N	OUT	LV	Channel 1 Digital 3 Red Output[1] Channel 1 Digital 1 Red Output[1] Dual-LVDS Channel 2 bit 2 Negative Output[2]
153		DRO1_4 DRO1_2 GND3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 4 Red Output[1] Channel 1 Digital 2 Red Output[1] Ground Digital LVDS[2], 3.3 V
154		DRO1_5 DRO1_3 LVDSB_1P	OUT	LV	Channel 1 Digital 5 Red Output[1] Channel 1 Digital 3 Red Output[1] Dual-LVDS Channel 2 bit 1 Positive Output[2]
155		DRO1_6 DRO1_4 LVDSB_1N	OUT	LV	Channel 1 Digital 6 Red Output[1] Channel 1 Digital 4 Red Output[1] Dual-LVDS Channel 2 bit 1 Negative Output[2]
156		DRO1_7 DRO1_5 VSUP3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 7 Red Output[1] Channel 1 Digital 5 Red Output[1] Supply Digital Voltage LVDS[2], 3.3 V
157		DRO1_8 DRO1_6 LVDSB_0P	OUT	LV	Channel 1 Digital 8 Red Output[1] Channel 1 Digital 6 Red Output[1] Dual-LVDS Channel 2 bit 0 Positive Output[2]
158		DRO1_9 DRO1_7 LVDSB_0N	OUT	LV	Channel 1 Digital 9 Red Output[1] (MSB) Channel 1 Digital 7 Red Output[1] (MSB) Dual-LVDS Channel 2 bit 0 Negative Output[2]
159		P1_7 TDO	IN/OUT	RtoGND	Port 1, Bit 7 Input/Output JTAG Interface Data Output
160		P1_6 TCLK	IN/OUT	RtoSUP	Port 1, Bit 6 Input/Output JTAG Interface Clock Input
161		P1_5	IN/OUT	RtoGND	Port 1, Bit 5 Input/Output
162		P1_4	IN/OUT	RtoGND	Port 1, Bit 4 Input/Output
163		GND3.3DAC	SUPPLY	OBL	Ground DAC
164		VSUP3.3DAC	SUPPLY	OBL	Supply Voltage DAC, 3.3V

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
165		P1_3 ROUT PWM3	IN/OUT	RtoGND	Port 1, Bit 3 Input/Output Analog Red Output PWM Bit 3 Output
166		P1_2 GOUT PWM2	IN/OUT	RtoGND	Port 1, Bit 2 Input/Output Analog Green Output PWM Bit 2 Output
167		P1_1 BOUT PWM1	IN/OUT	RtoGND	Port 1, Bit 1 Input/Output Analog Blue Output PWM Bit 1 Output
168		P1_0 SVMOUT REV	IN/OUT	RtoGND	Port 1, Bit 0 Input/Output Scan Velocity Modulation Output REV Output
169		VSUP1.8FE	SUPPLY	OBL	Supply Voltage Analog Video Frontend, 1.8 V
170		VSUP3.3FE	SUPPLY	OBL	Supply Voltage Analog Video Frontend, 3.3 V
171		VIN22 DHS	IN	LV	Analog Video 22 H-Sync Input Digital Video H-Sync Input
172		VIN21	IN	LV	Analog Video 21 B HD Input
173		VIN20	IN	LV	Analog Video 20 G HD Input
174		VIN19	IN	LV	Analog Video 19 R HD Input
175		VIN18	IN	LV	Analog Video 18 Fast Blank 2 Input
176		VIN17	IN	LV	Analog Video 17 B HD Input
177		VIN16	IN	LV	Analog Video 16 G HD Input
178		VIN15	IN	LV	Analog Video 15 R HD Input
179		VIN13	IN	LV	Analog Video 13 B HD Input
180		VIN12	IN	LV	Analog Video 12 G HD Input
181		VIN11	IN	LV	Analog Video 11 R HD Input
182		VIN9	IN	LV	Analog Video 9 Y or B SD Input
183		VIN8	IN	LV	Analog Video 8 C or Fast Blank 1 Input
184		VIN7	IN	LV	Analog Video 7 Y or G SD Input
185		VSUP1.8FE	SUPPLY	OBL	Supply Voltage Analog Video Frontend, 1.8 V
186		GNDA	SUPPLY	OBL	Analog Video Frontend, Platform Ground
187		VIN6	IN	LV	Analog Video 6 C or R SD Input
188		VIN5	IN	LV	Analog Video 5 Y/CVBS Input
189		VIN3	IN	LV	Analog Video 3 CVBS Input
190		VIN2	IN	LV	Analog Video 2 CVBS Input

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
191		VIN1	IN	LV	Analog Video 1 CVBS Input
192		VSUP3.3VO	SUPPLY	OBL	Supply Voltage Analog Video Output, 3.3 V
193		VOUT3	OUT	LV	Analog CVBS Video 3 Output
194		VOUT2	OUT	LV	Analog CVBS Video 2 Output
195		VOUT1	OUT	LV	Analog CVBS Video 1 Output
196		GND3.3IO3	SUPPLY	OBL	Ground Digital Input/Output Port 1
197		VSUP3.3IO3	SUPPLY	OBL	Supply Voltage Input/Output Port 1, 3.3 V
198		656I0 P3_0	IN/OUT	RtoGND	Digital 656 Bit 0 Input (LSB) Port 3, Bit 0 Input/Output
199		656I1 P3_1	IN/OUT	RtoGND	Digital 656 Bit 1 Input Port 3, Bit 1 Input/Output
200		656I2 P3_2	IN/OUT	RtoGND	Digital 656 Bit 2 Input Port 3, Bit 2 Input/Output
201		656I3 P3_3	IN/OUT	RtoGND	Digital 656 Bit 3 Input Port 3, Bit 3 Input/Output
202		656I4 P3_4	IN/OUT	RtoGND	Digital 656 Bit 4 Input Port 3, Bit 4 Input/Output
203		656I5 P3_5	IN/OUT	RtoGND	Digital 656 Bit 5 Input Port 3, Bit 5 Input/Output
204		656I6 P3_6	IN/OUT	RtoGND	Digital 656 Bit 6 Input Port 3, Bit 6 Input/Output
205		656I7 P3_7	IN/OUT	RtoGND	Digital 656 Bit 7 Input Port 3, Bit 7 Input/Output
206		656CLKI	IN	GND	Digital 656 Clock Input
207		656CLKO	OUT	LV	Digital 656 Clock Output
208		656O7 P4_7 TCLKFW	IN/OUT	RtoSUP	Digital 656 Bit 7 Output Port 4, Bit 7 Input/Output JTAG Interface Clock Input (FW Controller)

1) TTL output version only

2) LVDS output version only

6 DRX 3961A

6.1 General Desription

The DSP-based Analog TV IF Demodulator DRX 396xA performs the entire multistandard Quasi Split Sound (QSS) TV IF processing, AGC, video demodulation, and generation of the sound IF (SIF), requiring only one SAW filter. The IC is designed for applications in TV sets, VCRs, PC cards, and TV tuners.
The alignment-free DRX 396xA does not need special external components. All control functions and status registers are accessible via I2C bus interface.

6.2 Features

- Multistandard QSS IF processing with a single SAW
- Highly reduced amount of external components (no tank circuit, no potentiometers, no SAW switching)

- Programmable IF frequency (38.9 MHz, 45.75 MHz, 32.9 MHz, 58.75 MHz, 36.125 MHz etc.)
- Digital IF processing for the following standards: B/G, D/K, I, L/L', and M/N
- Standard specific digital post filtering
- Standard specific digital video/audio splitting
- Standard specific digital picture carrier recovery:
  -Alignment-free
  -Quartz-stable and accurate
  -Stable frequency lock at 100% modulation and overmodulation up to 150%
  -Quartz-accurate AFC information
- Programmable standard specific digital group delay equalization
- Automatically frequency-adjusted Nyquist slope, therefore optimum picture and sound performance over complete lock in frequency range
- Standard-specific digital AGC and delayed tuner AGC with programmable tuner take-over point
- Fast AGC due to linear structure
- Adaptive back porch control, therefore fast positive modulation AGC
- No sound traps needed at video output
- SIF output with standard-dependent pre-filtering and amplitude-controlled output level
- Optimal sound SNR due to carrier recovery without quadrature distortions
- FM radio capability without external components and with standard TV tuner
- Prepared for digital TV (DVB-C, DVB-T, ATSC)
- I2C bus interface

7 SERIAL 64K I2C EEPROM M24C64WBN6

7.1 General Description

M24C64WBN6 is a 64 Kbit Electrically Erasable PROM. These I2C-compatible electrically erasable programmable memory (EEPROM) devices are organized as 8192x8 bits. It supports 400kHz Protocol I2C uses a two-wire serial interface, comprising a bi-directional data line and a clock line.
The M24C64WBN6 is available in the standard 8-pin (Vcc, WC, SDA (i2c data), SCL (i2c clock), Vss,E0,E1,E2). WC pin is critcal pin. If WP is high, writing is not possible to EEPROM. If WP is low, writing is possible to EEPROM.

7.2 Features

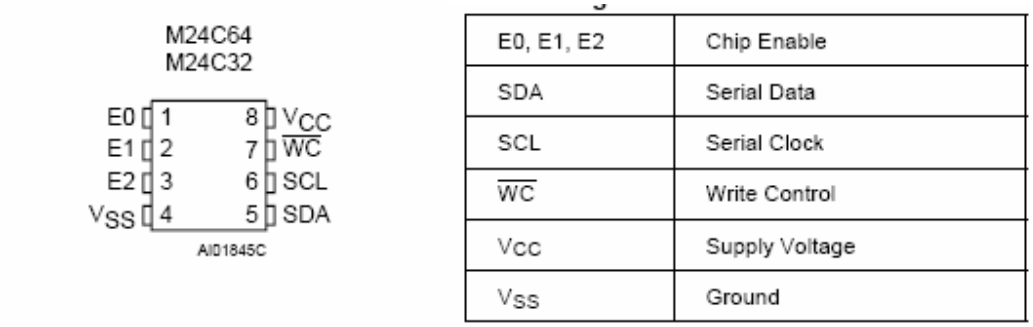
- Two-Wire I2C Serial Interface Supports 400kHz Protocol
- Single Supply Voltage:
  – 4.5 to 5.5V for M24Cxx
  – 2.5 to 5.5V for M24Cxx-W
  – 1.8 to 5.5V for M24Cxx-R
- Write Control Input
- BYTE and PAGE WRITE (up to 32 Bytes)

- RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Protection
- More than 1 Million Erase/Write Cycles
- More than 40-Year Data Retention

7.3 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage Temperature	–65	150	°C
T_{LEAD}	Lead Temperature during Soldering	See note [1]		°C
V_{IO}	Input or Output range	–0.50	6.5	V
V_{CC}	Supply Voltage	–0.50	6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]	–4000	4000	V

7.4 Pinning



E0, E1, E2	Chip Enable
SDA	Serial Data
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

8 CLASS AB STEREO HEADPHONE DRIVER TDA7050

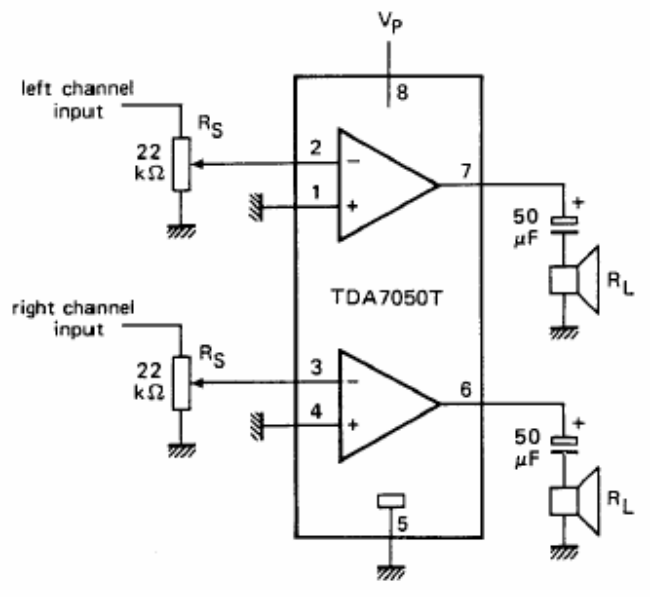
8.1 General Description

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

8.2 Features

· Limited to battery supply application only (typ. 3 and 4 V)
· Operates with supply voltage down to 1,6 V
· No external components required
· Very low quiescent current
· Fixed integrated gain of 26 dB, floating differential input
· Flexibility in use - mono BTL as well as stereo
· Small dimension of encapsulation (see package design example).

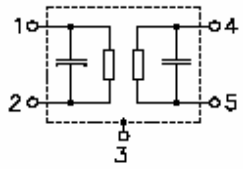
8.3 Pinning



9 SAW FILTER X6966M

9.1 Features:

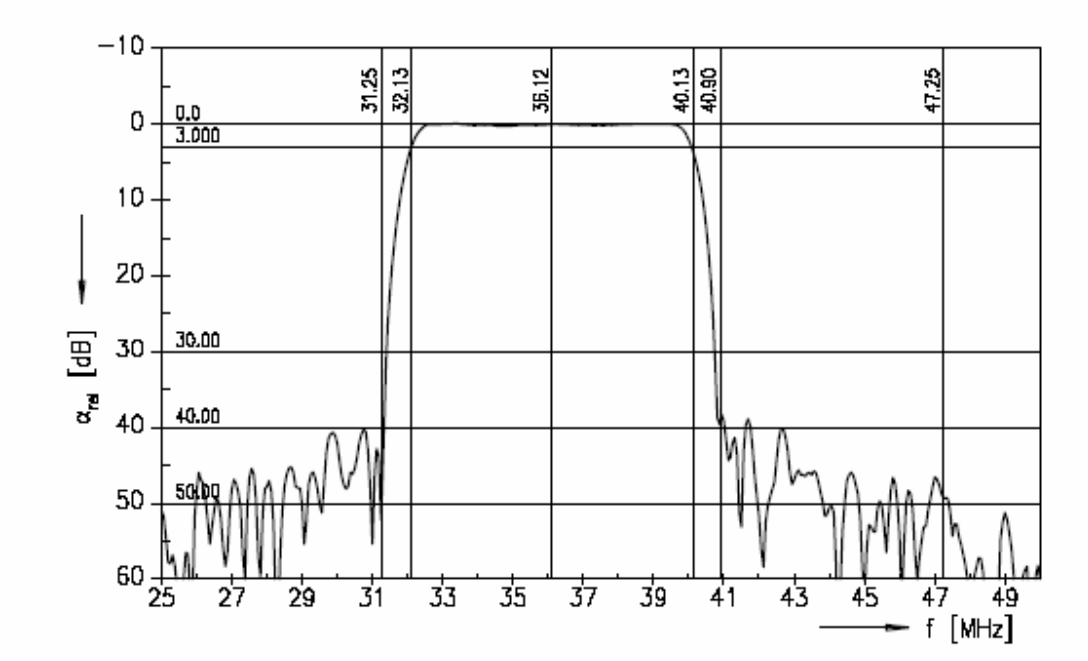
- IF filter for digital cable TV
- Plastic package SIP5K

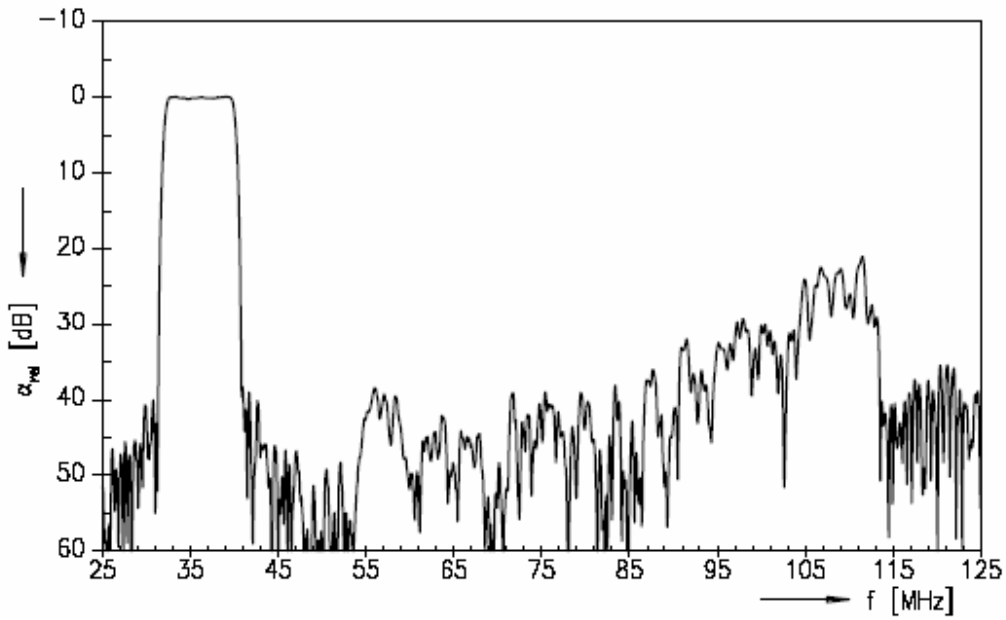


9.2 Pin configuration:

1 Input
2 Input - ground
3 Chip carrier - ground
4 Output
5 Output

9.3 Frequency response:





10 MPEG DECODER µPD61115

10.1 DESCRIPTION

The *µ*PD61115 device is a member of the second generation of multimedia processors based on NEC's Enhanced MultiMedia Architecture (EMMArchitecture). These devices provide nearly all the functionality required to realise a high performance and cost-effective digital set-top box or integrated digital TV.

10.2 FEATURES

- MPEG1 and MPEG2-TS/PS compliant
- High performance MIPS32™ 4Kc™ main CPU core
- High performance MIPS32™ 4Km™ sub-CPU core
- Integrated DVB descrambling with family options for Irdeto and Multi2
- 36 PID filters, 32 section filters
- Video Outputs: 4 DACs for RGB, Component video, S-video and composite output with support for PAL, NTSC and SECAM
- 4 graphics planes
- Audio Output: 2-channel PCM and SPDIF
- Peripherals support
    - two fast UARTs with 16byte FIFOs
    - I2C interface
    - infrared receiver
    - three wire clocked serial interface
- System timers, RTC and Watchdog timer
- Motorola/Intel Bus.

11 DRX 3973D

Fourth-Generation COFDM Demodulators

11.1 Introduction

The DRX 3973D and the DRX 3977D are fourth-generation COFDM demodulators that offer today's highest level of front-end integration resulting in ultimate DVB-T digital reception, compliant to ETS 300 744, DTG D-Book, EICTA E-Book, and Nordig Unified v1.0.2 .

The DRX 3973/77D applies cutting-edge digital filtering techniques in combination with a high-performance A/D-converter and PLL configuration, resulting in superior performance figures in the presence of digitaland analog adjacent channels.

Progressive channel estimator algorithms provide exceptional performance in multipath- and dynamicecho
conditions – an especially important feature for single-frequency networks and indoor reception.

The state-of-the-art impulsive noise cruncher suppresses interferences originating from sources such as
cars, electrical motors, and household appliances.

11.2 Features

- Highest level of front-end integration and flexibility:
    - Integrated PGA (programmable gain amplifier) 30 dB
    - Single 8 MHz SAW filter operation

- 2 AGC control signals available for RF and IF amplifier control
- Flexible clock reference options
- Re-use of 4 MHz tuner clock reference
- Pre-SAW sense input for optimal RF AGC setting and RF-level measurement

❖ Excellent digital reception performance:
- Superior digital and analog adjacent channel performance (> −40dB for QEF)
- Impulsive noise cruncher
- Multipath and dynamic echoes

❖ The input IF frequency ranging up to 44 MHz ensures upward compatibility for new tuner topologies
❖ Integrated microprocessor to perform autonomous detection and operation of all possible DVB-T
modes, without interaction with the host processor
❖ Fully automatic and fast signal acquisition: UHF and VHF band-scan in <20 seconds
❖ Meets all international DVB-T receiver specifications: Nordig Unified, DTG, EICTA
❖ Comfortable software drivers for integration of tuner and COFDM demodulator
❖ Secondary serial interface for tuner control
❖ 5 V tolerant AGC and secondary serial protocol outputs
❖ 2 general purpose I/O pins (GPIO)
❖ Configurable parallel or serial MPEG-TS output
❖ PMQFP64-2 package: footprint 10□10 mm (DRX 3973D)
❖ PQFN48-1 package: small footprint 7□7 mm (DRX 3977D)
❖ IEEE 1149.1 boundary scan

11.3 Applications

❖ IDTV / hybrid TV
❖ Set-top boxes
❖ PVR / DVDR
❖ Network interface modules (NIM)
❖ PC-TV applications

12 PI6CX100-27MHz 3.3V VCXO for Set-Top Box Applications

12.1 Features

❖ • 3.3V operating voltage
❖ • Uses an inexpensive external crystal
❖ • On-chip VCXO with pull range of 240ppm
❖ • VCXO tuning voltage from 0 to 3.3V
❖ • 10mA output drive at CMOS levels
❖ • Available in SOIC package

12.2 Description

The PI6CX100-27 is a low-cost, high-performance 3.3V VCXO, designed to replace expensive VCXO modules. The on-chip Voltage Controlled Crystal Oscillator accepts a

0 to 3.3V input voltage to cause clocks to vary by ±120ppm. This device uses an inexpensive external pullable crystal at 27 MHz to produce the same output frequency.The PI6CX100-27 is designed for Set-Top Box applications.

13 74V1G08

SINGLE 2-INPUT AND GATE

- HIGHSPEED: tPD = 4.3 ns (TYP.) atVCC= 5V
- LOWPOWERDISSIPATION:
- ICC =1 □A (MAX.) at TA =25 oC
- HIGHNOISEIMMUNITY:
- VNIH=VNIL =28%VCC (MIN.)
- POWERDOWN PROTECTIONON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
- |IOH| = IOL = 8 mA(MIN)
- BALANCEDPROPAGATIONDELAYS:
- tPLH □tPHL
- OPERATINGVOLTAGERANGE:
- VCC (OPR)= 2V to 5.5V
- IMPROVEDLATCH-UP IMMUNITY

- DESCRIPTION

- The 74V1G08 is an advanced high-speed CMOS SINGLE 2-INPUT AND GATE fabricated with sub-micron silicon gate and double-layer metal wiring C2MOS technology.

14 FMS6145

Low Cost Five Channel 4th Order Standard Definition Video Filter Driver

Description

The FMS6145 Low Cost Video Filter (LCVF) is intended to replace passive LC filters and drivers with a low-cost integrated device. Five 4th order filters provide improved image Quality compared to typical 2nd or 3rd order passive solutions.

The FMS6145 may be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal diode clamps and bias circuitry
may be used if AC-coupled inputs are required.

The outputs can drive AC or DC-coupled single (150Ω) or dual(75Ω) loads. DC-coupling the outputs removes the need for output coupling capacitors. The input DC levels will be offset approximately +280mV at the output.

Features

- Five fourth-order 8MHz (SD) filters
- Transparent input clamping
- Dual video load drive (2Vpp, 75Ω)
- AC or DC-coupled inputs
- AC or DC-coupled outputs
- DC-coupled outputs eliminate AC-coupling capacitors
- 5V only
- Lead (Pb) Free TSSOP-14 package

Applications

- Cable set top boxes
- Satellite set top boxes
- DVD players
- HDTV
- Personal video recorders (PVR)
- Video on demand (VOD)

15 IC DESCRIPTIONS AND INTERNAL BLOCK DIAGRAM

LM1117
LM1086
MP1593
FDC642P
SIL9011
24LC02
µPA672T
M74HC4052
Max809
24LC21

15.1 LM1117

15.1.1 General Description

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry standard LM317. The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V. The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to as-sure output voltage accuracy to within ±1%. The LM1117 series is available in SOT- 223, TO-220, and TO-252 D-PAK packages. A minimum of 10µF

tantalum capacitor is required at the output to improve the transient response and stability.

15.1.2 Features

- Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
- Space Saving SOT-223 Package
- Current Limiting and Thermal Protection
- Output Current 800mA
- Line Regulation 0.2% (Max)
- Load Regulation 0.4% (Max)
- Temperature Range
- LM1117 0°C to 125°C
- LM1117I -40°C to 125°C

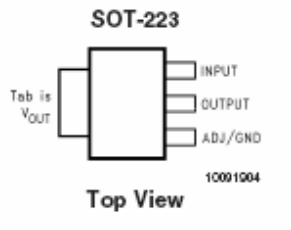
15.1.3 Applications

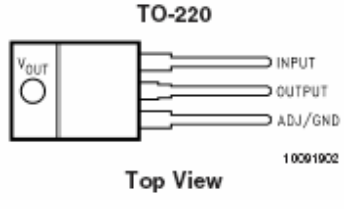
- 2.85V Model for SCSI-2 Active Termination
- Post Regulator for Switching DC/DC Converter
- High Efficiency Linear Regulators 15
- 32” TFT TV Service Manual 10/01/2005
- Battery Charger
- Battery Powered Instrumentation

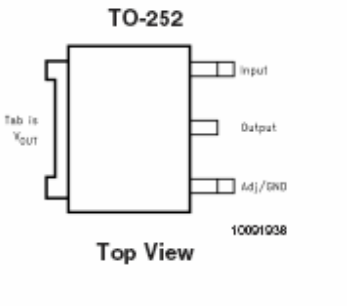
15.1.4 Absolute Maximum Ratings

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
DC Input Voltage	V_{IN}		7	V
Lead Temperature (Soldering, 5 Seconds)	T_{SOL}		260	℃
Storage Temperature Range	T_{STG}	−65	150	℃
Operating Junction Temperature Range	T_{OPR}	0	125	℃

15.1.5 Pinning







15.2 LM1086

15.2.1 General Description

The LM1086 is a low dropout three terminal regulator with 1.5A output current capability.

The output voltage is adjustable with the use of a resistor divider. Dropout is guaranteed at a maximum of 500 mV at maximum output current. It's low dropout voltage and fast transient response make it ideal for low voltage microprocessor applications. Internal current and thermal limiting provides protection against any overload condition that would create excessive junction temperature.

15.2.2 Features

- Low Dropout Voltage 500mV at 1.5A Output Current
- Fast Transient Response
- 0.015% Line Regulation
- 0.1% Load Regulation
- Current Limiting and Thermal Protecion.
- Adjustable or Fixed Output Voltage(1.8, 2.5, 2.85, 3.0, 3.3, 3.45, 5.0V)
- Surface Mount Package SOT-223 & TO-263 (D2 Package)
- 100% Thermal Limit Burn-in

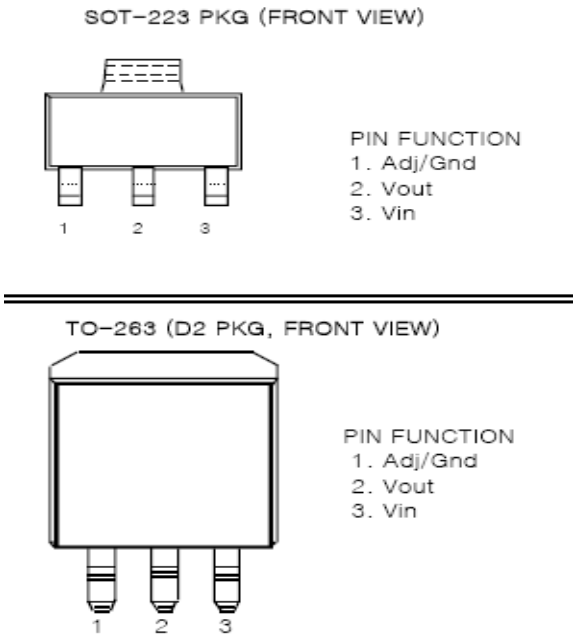
15.2.3 Applications

- Battery Charger
- Adjustable Power Supplies
- Constant Current Regulators
- Portable Instrumentation
- High Efficiency Linear Power Supplies
- High Efficiency "Green" Computer Systems
- SMPS Post-Regulator
- Power PC Supplies
- Powering VGA & Sound Card

15.2.4 Absolute Maximum Ratings

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Supply Voltage	Vin	7	V
Operating Junction Temperature Range	Topr	0~125	℃
Storage Temperature Range	Tstg	-65~150	℃
Thermal Resistance Junction to Case TO-263	Tjc	3	C/W
Thermal Resistance Junction to Ambient TO-263	Tja	60	C/W
Lead Temperature (Soldering) 10 sec.	Tsol	300	℃
Maximum Output Current	Imax	1.5	A

15.2.5 Pinning



15.3 MP1593

15.3.1 General Description

The MP1593 is a step-down regulator with an internal Power MOSFET. It achieves 3A continuous output current over a wide input supply range with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilization. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown. Adjustable soft-start reduces the stress on the input source at turn-on. In shutdown mode the regulator draws 20μA of supply current. The MP1593 requires a minimum number of readily available external components to complete a 3A step down DC to DC converter solution.

15.3.2 Features

- 3A Output Current
- Programmable Soft-Start
- 100mΩ Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic Capacitors
- Up to 95% Efficiency
- 20μA Shutdown Mode
- Fixed 385KHz Frequency
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Wide 4.75 to 28V Operating Input Range
- Output Adjustable from 1.22V
- Under Voltage Lockout
- Available in 8-Pin SOIC Package

15.3.3 Applications

- Distributed Power Systems
- Battery Chargers

- Pre-Regulator for Linear Regulators
- Flat Panel TVs
- Set-Top Boxes
- Cigarette Lighter Powered Devices
- DVD/PVR Devices

15.3.4 Absolute Maximum Ratings

Supply Voltage V_{IN} ..... –0.3V to 30V
Switch Voltage V_{SW} ..... –0.5V to V_{IN}+0.3V
Boost Voltage V_{BS} ..... V_{SW}–0.3V to V_{SW}+6V
All Other Pins ..... –0.3V to 6V
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to 150°C

15.3.5 Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown Supply Current		V_{EN} = 0V		20	30	µA
Supply Current		V_{EN} = 2.6V; V_{FB} = 1.4V		1.0	1.2	mA
Feedback Voltage	V_{FB}	4.75V ≤ V_{IN} ≤ 28V; V_{COMP} < 2V	1.194	1.222	1.250	V
Error Amplifier Voltage Gain	A_{EA}			400		V/V
Error Amplifier Transconductance	G_{EA}	ΔI_{COMP} = ±10 µA	500	800	1120	µA/V
High Side Switch On Resistance	$R_{DS(ON)1}$			100	140	mΩ
Low Side Switch On Resistance	$R_{DS(ON)2}$			10		Ω
High Side Switch Leakage Current		V_{EN} = 0V; V_{SW} = 0V		0	10	µA
Current Limit			3.3	4.7	6.5	A
Current Sense to COMP Transconductance	G_{CS}			6.2		A/V
Oscillation Frequency	f_{OSC1}		335	385	435	KHz
Short Circuit Oscillation Frequency	f_{OSC2}	V_{FB} = 0V	25	45	60	KHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 1.0V		90		%
Minimum Duty Cycle	D_{MIN}	V_{FB} = 1.5V			0	%
EN Threshold Voltage			0.9	1.2	1.5	V

15.3.6 Pinning

Pin1:BS
High-Side Gate Drive Boost Input. BS supplies the drive for the high-side N-Channel MOSFET switch. Connect a 10nF or greater capacitor from SW to BS to power the high side switch.

Pin2:IN
Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 4.75V to 28V power source. Bypass IN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
Pin3:SW
Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.

Pin4:GND
Ground.
Pin5:FB
Feedback Input. FB senses the output voltage to regulate that voltage. Drive FB with a resistive voltage divider from the output voltage. The feedback threshold is 1.222V.
Pin6:COMP
Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required.
Pin7:EN
Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive EN low to turn it off. An Under Voltage Lockout (UVLO) function can be implemented by the addition of a resistor divider from VIN to GND. For complete low current shutdown its needs to be less than 0.7V. For automatic startup, leave EN unconnected.
Pin8:SS
Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1μF capacitor sets the soft-start period to 10ms. To disable the soft-start feature, leave SS unconnected.

15.4 FDC642P

15.4.1 General Description

This p-channel 2.5V specified MOSFET is produced using Fairchild's advanced PowerTrench process that has been especially tailored to minimize on state resistance and yet maintain low gate charge for superior switching performance.

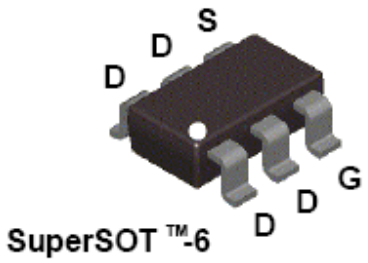
15.4.2 Features

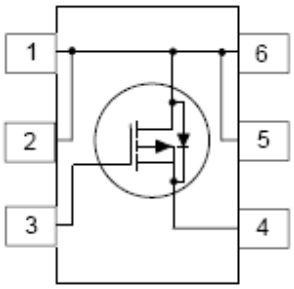
- -4 A, -20 V. $R_{DS(ON)}$ = 0.065 Ω @ V_{GS} = -4.5 V
  $R_{DS(ON)}$ = 0.100 Ω @ V_{GS} = -2.5 V
- Fast switching speed.
- Low gate charge (7.2nC typical).
- High performance trench technology for extremely low $R_{DS(ON)}$.
- SuperSOT™-6 package: small footprint (72% smaller than standard SO-8); low profile (1mm thick).

15.4.3 Absolute Maximum Ratings

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage		±8	V
I_D	Drain Current - Continuous	(Note 1)	-4	A
	Drain Current - Pulsed	(Note 1a)	-20	
P_D	Power Dissipation for Single Operation	(Note 1a)	1.6	W
		(Note 1b)	0.8	
T_J, T_{stg}	Operating and Storage Junction Temperature Range		-55 to +150	°C

15.4.4 Pinning





15.5 ANX9021

The ANX9021 is an advanced multimedia receiver compliant with High Definition Multimedia Interface (HDMI) Specification 1.1. HDMI is the first transport standard to unify digital video, audio, and control data over low cost cables. It connects digital television, flat panel displays and project systems digitally to multimedia sources: DVD players, high definition set top boxes, digital video tape recorders, and personal computers. Digital transmission, in turn, delivers an uncompromising multimedia experience. HDMI also includes encryption for premium contents pursuant to the High bandwidth Digital Content Protection (HDCP) standard. The ANX9021 embeds the HDCP keys and key selection vectors to reduce manufacturing complexity and system cost.

15.5.1 Features

Dual channel HDMI receiver supporting link data rate up to 1.65 Gbps
HDMI 1.1, HDCP 1.1 and DVI 1.0 compliant
WideEye™ architecture for signal conditioning and equalization
support cable length up to 20m
better than 10E 12 bit error rate
Digital interface to video processor supporting
24 bit RGB / YCbCr 4:4:4
16/20/24 bit YCbCr 4:2:2
8/10/12 bit YCbCr 4:2:2 (ITU BT 656)
12 bit double data rate interface
Color space conversion: RGB to/from YCbCr both directions (601 and 709 standards)
Auto video mode configuration
Analog RGB/YPbPr output with 8 bit linearity
Digital audio interface
32 to 192 kHz audio sampling rate
Up to 4 I2S interface for 8 channel audio
S/PDIF interface supporting PCM, Dolby

Digital™, DTS™ digital audio transmission using IEC 60958 and IEC61937
Configurable soft mute
Integrated HDCP decryption engine and pre programmed keys
Programmable power management with automatic shutdown for power conservation
Supports automated link integrity checking
144 lead TQFP package supporting lead free and green requirements
Pinout compatible with Silicon Image

15.6 24LC02

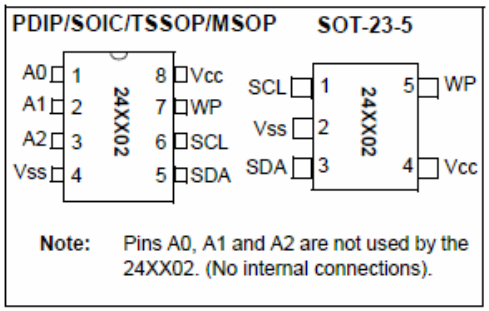
15.6.1 General Description

24AA02/24LC02B (24XX02*) is a 2 Kbit Electrically Erasable PROM. The device is organized as one block of 256 x 8-bit memory with a 2-wire serial interface. Low-voltage design permits operation down to 1.8V, with standby and active currents of only 1µA and 1mA, respectively. The 24XX02 also has a page write capability for up to 8 bytes of data.

15.6.2 Features

- Single supply with operation down to 1.8V
- Low-power CMOS technology
  -1mA active current typical
  -1µA standby current typical (I-temp)
- Organized as 1 block of 256 bytes (1 x 256 x 8)
- 2-wire serial interface bus, I^2C™ compatible
- Schmitt Trigger inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (24AA02) and 400 kHz (24LC02B) compatibility
- Self-timed write cycle (including auto-erase)
- Page write buffer for up to 8 bytes
- 2ms typical write cycle time for page write
- Hardware write-protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- 1,000,000 erase/write cycles
- Data retention > 200 years
- 8-lead PDIP, SOIC, TSSOP and MSOP packages
- 5-lead SOT-23 package
- Pb-free finish available
- Available for extended temperature ranges:
  -Industrial (I): -40°C to +85°C
  -Automotive (E): -40°C to +125°C

15.6.3 10.6.3 Pinning



Note: Pins A0, A1 and A2 are not used by the 24XX02. (No internal connections).

Name	PDIP	SOIC	TSSOP	MSOP	SOT23	Description
A0	1	1	1	1	—	Not Connected
A1	2	2	2	2	—	Not Connected
A2	3	3	3	3	—	Not Connected
Vss	4	4	4	4	2	Ground
SDA	5	5	5	5	3	Serial Address/Data I/O
SCL	6	6	6	6	1	Serial Clock
WP	7	7	7	7	5	Write-Protect Input
Vcc	8	8	8	8	4	+1.8V to 5.5V Power Supply

15.7 µPA672T

15.7.1 General Description

N-channel Mos-Fet array for switching.The µPA672T is a super-mini-mold device provided with two MOS FET elements. It achieves high-density mounting and saves mounting costs.

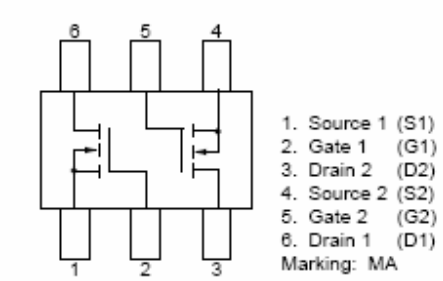
15.7.2 Features

- Two MOS FET circuits in package the same size as SC-70
- Automatic mounting supported

15.7.3 Absolute Maximum Ratings

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Drain to Source Voltage	V_{DSS}		50	V
Gate to Source Voltage	V_{GSS}		±7.0	V
Drain Current (DC)	$I_{D(DC)}$		100	mA
Drain Current (pulse)	$I_{D(pulse)}$	PW ≤ 10 ms, Duty Cycle ≤ 50 %	200	mA
Total Power Dissipation	P_T		200 (Total)	mW
Channel Temperature	T_{ch}		150	°C
Storage Temperature	T_{stg}		–55 to +150	°C

15.7.4 Pinning



15.8 M74HC4052

15.8.1 General Description

The M74HC4052 is a dual four-channel analog MULTIPLEXER/DEMULTIPLEXER fabricated with silicon gate C2MOS technology and it is pin to pin compatible with the equivalent metal gate CMOS4000B series. It contains 8 bidirectional and digitally controlled analog switches.

15.8.2 Features

- LOW POWER DISSIPATION: ICC = 4mA(MAX.) at TA=25°C
- LOGIC LEVEL TRANSLATION TO ENABLE 5V LOGIC SIGNAL TO COMMUNICATE
- WITH ±5V ANALOG SIGNAL
- LOW "ON" RESISTANCE:
  70W TYP. (VCC - VEE = 4.5V)
  50W TYP. (VCC - VEE = 9V)
- WIDE ANALOG INPUT VOLTAGE RANGE: ±6V
- FAST SWITCHING:
  tpd = 15ns (TYP.) at TA = 25 °C
- LOW CROSSTALK BETWEEN SWITCHES
- HIGH ON/OFF OUTPUT VOLTAGE RATIO
- WIDE OPERATING SUPPLY VOLTAGE RANGE (VCC - VEE) = 2V TO 12V
- LOW SINE WAVE DISTORTION: 0.02% at VCC - VEE = 9V
- HIGH NOISE IMMUNITY: VNIH = VNIL = 28 % VCC (MIN.)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 4052

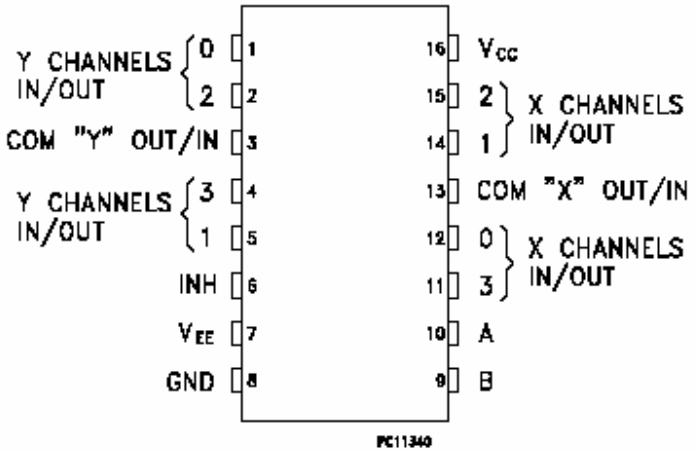
15.8.3 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_{CC} - V_{EE}	Supply Voltage	-0.5 to +13	V
V_I	Control Input Voltage	-0.5 to V_{CC} + 0.5	V
$V_{I/O}$	Switch I/O Voltage	V_{EE} -0.5 to V_{CC} + 0.5	V
I_{CK}	Control Input Diode Current	± 20	mA
I_{IOK}	I/O Diode Current	± 20	mA
I_T	Switch Through Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

15.8.4 Pinning

VEE supply pin is provided for analog input signals. It has an inhibit (INH) input terminal to disable all the switches when high. For operation as a digital multiplexer/demultiplexer, VEE is connected to GND.
A and B control inputs select one channel out of four in each section. All inputs are equipped with protection circuits against static discharge and transient excess voltage.



15.9 Max809

15.9.1 General Description

The MAX809 and MAX810 are cost−effective system supervisor circuits designed to monitor VCC in digital systems and provide a reset signal to the host processor when necessary. No external components are required.
The reset output is driven active within 10 _sec of VCC falling through the reset voltage threshold. Reset is aintained active for a timeout period which is trimmed by the factory after VCC rises above the reset threshold. The MAX810 has an active−high RESET

output while the MAX809 has an active−low RESET output. Both devices are available in SOT−23 and SC−70 packages.

15.9.2 Features

- Precision VCC Monitor for 1.5 V, 1.8 V, 2.5 V, 3.0 V, 3.3 V, and 5.0 V Supplies
- Precision Monitoring Voltages from 1.2 V to 4.9 V Available in 100 mV Steps
- Four Guaranteed Minimum Power−On Reset Pulse Width Available (1 ms, 20 ms, 100 ms, and 140 ms)
- RESET Output Guaranteed to VCC = 1.0 V.
- Low Supply Current
- Compatible with Hot Plug Applications
- VCC Transient Immunity
- No External Components
- Wide Operating Temperature: −40°C to 105°C
- Pb−Free Packages are Available

15.9.3 Absolute Maximum Ratings

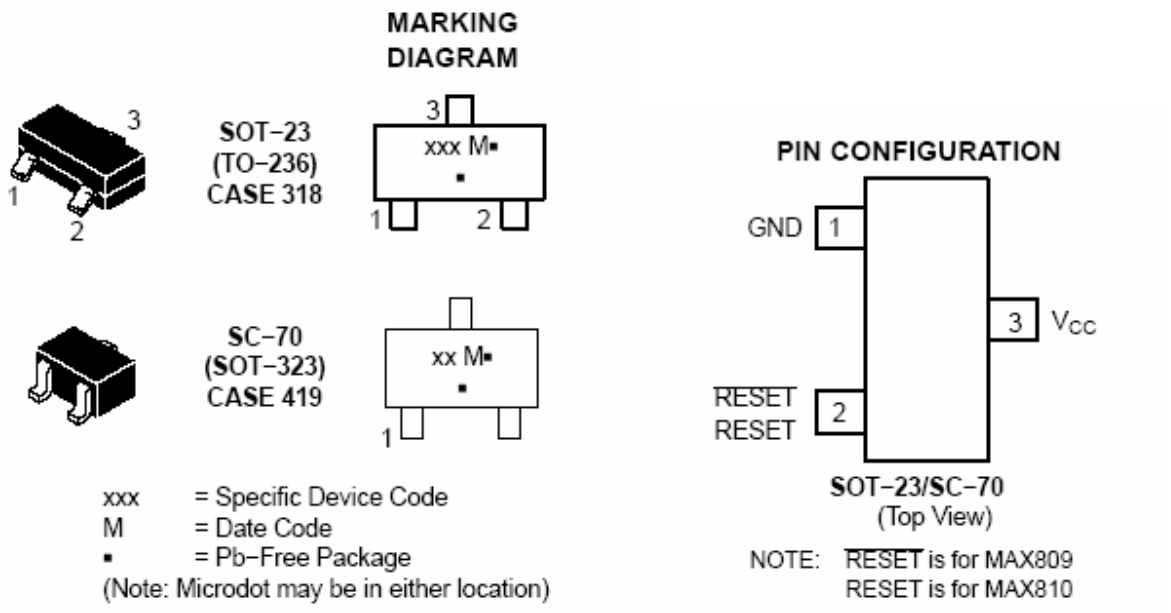
Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} to GND)	V_{CC}	−0.3 to 6.0	V
RESET Output Voltage (CMOS)		−0.3 to (V_{CC} + 0.3)	V
Input Current, V_{CC}		20	mA
Output Current, $\overline{RESET}$		20	mA
dV/dt (V_{CC})		100	V/μsec
Thermal Resistance, Junction−to−Air (Note 1) SOT−23 SC−70	$R_{\theta JA}$	301 314	°C/W
Operating Junction Temperature Range	T_J	−40 to +105	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Lead Temperature (Soldering, 10 Seconds)	T_{sol}	+260	°C
ESD Protection Human Body Model (HBM): Following Specification JESD22−A114 Machine Model (MM): Following Specification JESD22−A115		 2000 200	V
Latchup Current Maximum Rating: Following Specification JESD78 Class II Positive Negative	$I_{Latchup}$	 200 200	mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. This based on a 35x35x1.6mm FR4 PCB with 10mm^2 of 1 oz copper traces under natural convention conditions and a single component characterization.
2. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}} \quad \text{with } T_{J(max)} = 150°C$$

15.9.4 Pinning



15.1024LC21

15.10.1 General Description

The 24LC21 is a 1K bit electrically erasable programmable memory (EEPROM), organized by 8 bits.This device can operate in two modes: Transmit Only mode and I2C bidirectional mode. When powered, the device is in Transmit Only mode with EEPROM data clocked out from the rising edge of the signal applied on VCLK.

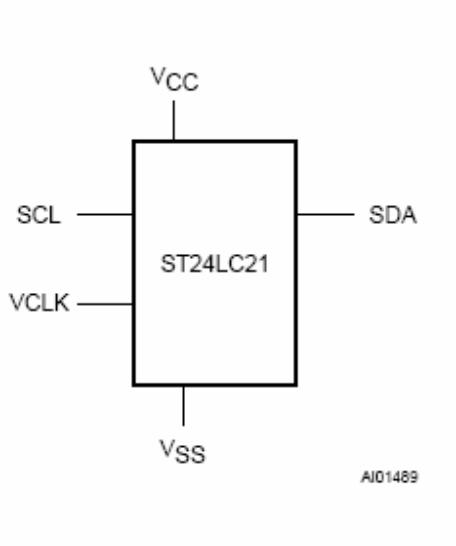
15.10.2 Features

- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- 2.5V to 5.5V SINGLE SUPPLY VOLTAGE
- 400k Hz COMPATIBILITY OVER the FULL RANGE of SUPPLY VOLTAGE
- TWO WIRE SERIAL INTERFACE I2C BUS COMPATIBLE
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES

15.10.3 Absolute Maximum Ratings

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1	0 to 70	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

15.10.4 Pinning



SDA	Serial Data Address Input/Output
SCL	Serial Clock (I^2C mode)
V_{CC}	Supply Voltage
V_{SS}	Ground
VCLK	Clock Transmit only mode

16 SERVICE MENU SETTINGS

In order to reach service menu,

- First Press **"MENU"**
- Then press the remote control code, which is **"4725"**

16.1 Video Setup

- ***Panel Select <.....>***
  - ***CHI MEI 16/9 32 inch***
  - ***LG 16/9 26 inch***
  - ***SAMSUNG 16/9 32 inch***

- **Picture Mute <.....>**
  *If "Yes" selected, **"Picture mute"** feature is active.*
- ***Blue Screen <.....>***
  *If "Yes" selected, **"Blue Background"** item is seen in **"Feature"** menu.*
- **YC Delay <.....>**

- ***Tuner PAL <.....>*** *Value between -8 to+7*
- ***Ext PAL <.....>*** *Value between -8 to+7*
- ***SECAM <.....>*** *Value between -8 to+7*
- ***NTSC <.....>*** *Value between -8 to+7*

- **AGC (dB) <*****.....>*** *Value between 0 to+8*

16.2 AudioSetup

- ***Equalizer <.....>***

  If "Yes" selected, ***"Equalizer"*** *item is seen in* ***"Sound"*** *menu.*

- ***BBE***
- ***SRS WOW***
- ***Virtual Dolby Surround <.....>***

  If "Yes" selected, Virtual Dolby Surround feature is seen in ***"Sound"*** *menu with selected Virtual Dolby Text.*
- ***Virtual Dolby Text*** *The selected item is seen as Virtual Dolby Srround Text.*
  - ***3DS***
  - ***Virtual Dolby***
  - ***3D Panorama***
- ***AVL <.....>***

  If "Yes" selected, ***"AVL"*** *item is seen in* ***"Sound"*** *menu.*
- ***Carrier Mute <.....>***

  If "Yes" selected, ***"Carrier mute"*** *feature is active.*
- ***Audio Delay Offset***
- ***Prescale***
  - ***FM Presc. AVL On <.....>*** *Value between 0 to +127*
  - ***AM Presc. AVL On <.....>*** *Value between 0 to +127*
  - ***NICAM Presc. AVL On <.....>*** *Value between 0 to +127*
  - ***I2S Presc. AVL On <.....>*** *Value between 0 to +127*
  - ***SCART Presc. AVL On <.....>*** *Value between 0 to +127*
  - ***FM Presc. AVL Off <.....>*** *Value between 0 to +127*
  - ***AM Presc. AVL Off <.....>*** *Value between 0 to +127*
  - ***NICAM Presc. AVL Off <.....>*** *Value between 0 to +127*
  - ***I2S Presc. AVL Off <.....>*** *Value between 0 to +127*
  - ***SCART Presc. AVL Off <.....>*** *Value between 0 to +127*
- ***Dynamic Bass <.....>***

  If "Yes" selected, ***"Dynamic Bass"*** *item is seen in* ***"Sound"*** *menu.*
- ***Subwoofer <.....>***

  If "Yes" selected, ***"Subwoofer"*** *item is seen in* ***"Sound"*** *menu.*

16.3 Options 1

- ***VCTP Version <.....>***
  - ***Basic+***
  - ***Basic***
- ***Double Digit <.....>***

  If "Yes" selected, ***"Double Digit"*** *button is active for channel selection.*
- ***TEA6415C Available <.....>***

  If "Yes" selected, video switch IC is active on hardware.
- ***TEA642X Available<.....>***

If "Yes" selected, audio switch IC is active on hardware.

- ***Power-Up Mode <.....>***
  - ***StandBy*** *If selected, TV opens in stand by mode.*
  - ***L.State*** *If selected, TV opens in Last State mode.*
- ***TV Open Mode <.....>***
  - ***Source***
  - ***1st TV***
  - ***Last TV***
- ***Select Languages <.....>*** *"Yes" selected languages are seen as option under the* ***"Language"*** *item in* ***"Feature"*** *menu*
  - ***Language Set 1***
    - ***German <.....>***
    - ***French <.....>***
    - ***Spanish <.....>***
    - ***Italian <.....>***
    - ***Danish <.....>***
    - ***Finnish <.....>***
    - ***Swedish <.....>***
  - ***Language Set 2***
    - ***Greek <.....>***
    - ***Norwegian <.....>***
    - ***Dutch <.....>***
    - ***Portuguse <.....>***
    - ***Polish <.....>***
    - ***Turkish <.....>***
    - ***Russian <.....>***
    - ***Czech <.....>***
  - ***Language Set 3***
    - ***Hungarian <.....>***
    - ***Slovak <.....>***
    - ***Slovenian <.....>***
    - ***Romanian <.....>***
    - ***Bulgarian <.....>***
    - ***Croatian <.....>***
    - ***Serbian <.....>***
    - ***Hebrew <.....>***

- ***First APS <.....>***

  If "Yes" selected, first time TV opens by asking APS.
- ***APS Volume <.....>*** *value between 0 to+63*
- ***Burn In Mode <.....>***

  If "Yes" selected, TV opens with Burn-In mode. This mode is used in manufacturing.
- ***APS Test***
- ***HDMI WP <.....>***

  If "Yes" selected, HDMI EDID ROM is write protected.

16.4 Options 2

- ***Autostore <.....>***
  If "Yes" selected, Channel is automatically stored.
- ***Led Type <.....>***
  - ***1 Led 1 Colour***
  - ***1 Led 2 Colours***
  - ***2 Led 2 Colours***
- ***PC PIP <.....>***
- ***PC Stand By <.....>***

16.5 Service Scan/Tuning Setup

- ***Search for L/L' <.....>***
- ***Pref. Search Standard <.....>***
  - ***BG, DK, I***
  - ***L/L'***
  - ***M***
- ***Station Ident <.....>***
- ***ATS Delay Time (ms) <.....>*** *Value between 20 to 250*
- ***Color Killer Threshold <.....>*** *Value between 0 to +255*
- ***Tuner Options <.....>***
  - ***Control Byte <.....>*** *Value between 0 to +255*
  - ***Low-Mid – Low Byte <.....>*** *Value between 0 to +255*
  - ***Low-Mid – High Byte <.....>*** *Value between 0 to +255*
  - ***Mid-High – Low Byte <.....>*** *Value between 0 to +255*
  - ***Mid-High – High Byte <.....>*** *Value between 0 to +255*
  - ***BSW1 <.....>*** *Value between 0 to +255*
  - ***BSW2 <.....>*** *Value between 0 to +255*
  - ***BSW3 <.....>*** *Value between 0 to +255*

16.6 External Source Settings

- ***DTV <.....>***
- ***DVD <.....>***
- ***Ext 2 S-Video <.....>***
- ***Ext 3 <.....>***
- ***Ext 3 S-Video <.....>***
- ***FAV <.....>***
- ***BAV <.....>***
- ***S-Video <.....>***
- ***HDMI 1 <.....>***
- ***HDMI 2 <.....>***
- ***YPbPr <.....>***
- ***PC <.....>***

16.7 Picture Mode

- ***Sources <.....>***
  - ***Tuner***
  - ***CVBS***
  - ***RGB***

        - ***SVHS***
        - ***HDMI***
        - ***YPbPr***
        - ***PC***
        - ***PIP***
- ***Picture Mode <.....>***
        - ***Dynamic***
        - ***Natural***
        - ***Cinema***

- ***Colour Temp <.....>***
        - ***Cool***
        - ***Normal***
        - ***Warm***
- ***Contrast <.....>*** *Value between 0 to +63*
- ***Brightness <.....>*** *Value between 0 to +63*
- ***Sharpness <.....>*** *Value between 0 to +15*
- ***Colour <.....>*** *Value between 0 to +63*
- ***Backlight <.....>*** *Value between 0 to +255*
- ***R <.....>*** *Value between -63 to +63*
- ***G <.....>*** *Value between -63 to +63*
- ***B <.....>*** *Value between -63 to +63*

16.8 Reset TV-Set

- ***Initialize NVM from ROM***
        Press green button to reset the NVM from ROM

17 SOFTWARE UPDATE DESCRIPTION

17.1 Analog Software Update Via I^2C

Step.1
Short the second and third pins of PL_402. Power ON and keep shorting the pins 3-5 seconds.
Step.2
Then connect the I^2C update tool to parallel port of PC.
Step.3
Connect the other end of the tool to PL_402.
Step.4
Run Cosima_VCTP Visual I^2C software update program.
Step.5
When you click to box near **“0”** at **“Bootloader Version”** item, you will see **“42”.**
If you couldn’t see **“42”** or a **“No Acknowledge from Slave!”** is appeared,
There may be a connection problem sourced from PC port, or update tool.
Or you may forget to power ON.

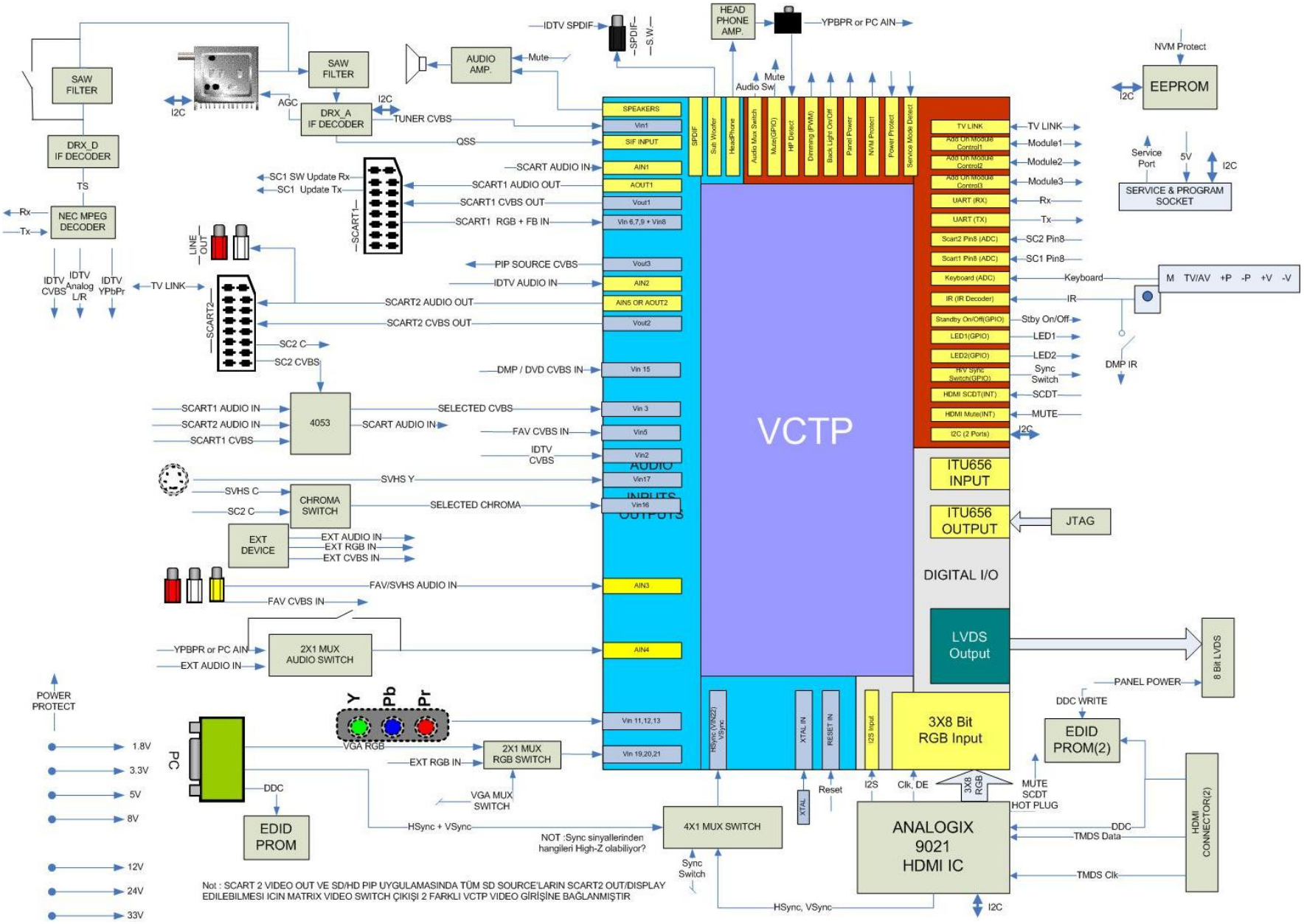
Step.6
After **“42”** is seen, Click **“Erase Flash”**
Step.7
Select the bin. file from near the **“Load Bin”**
Step.8
Click **“Load Bin”** and load the required bin. file.
Step.9
Unpick the I^2C cable from Chasis
Step.10
Power off and on again TV set to produce hard reset.
Step.11
Initialize the NVM from “**Reset TV-set”** item from service menu

17.2 Analog Software Update Via UART

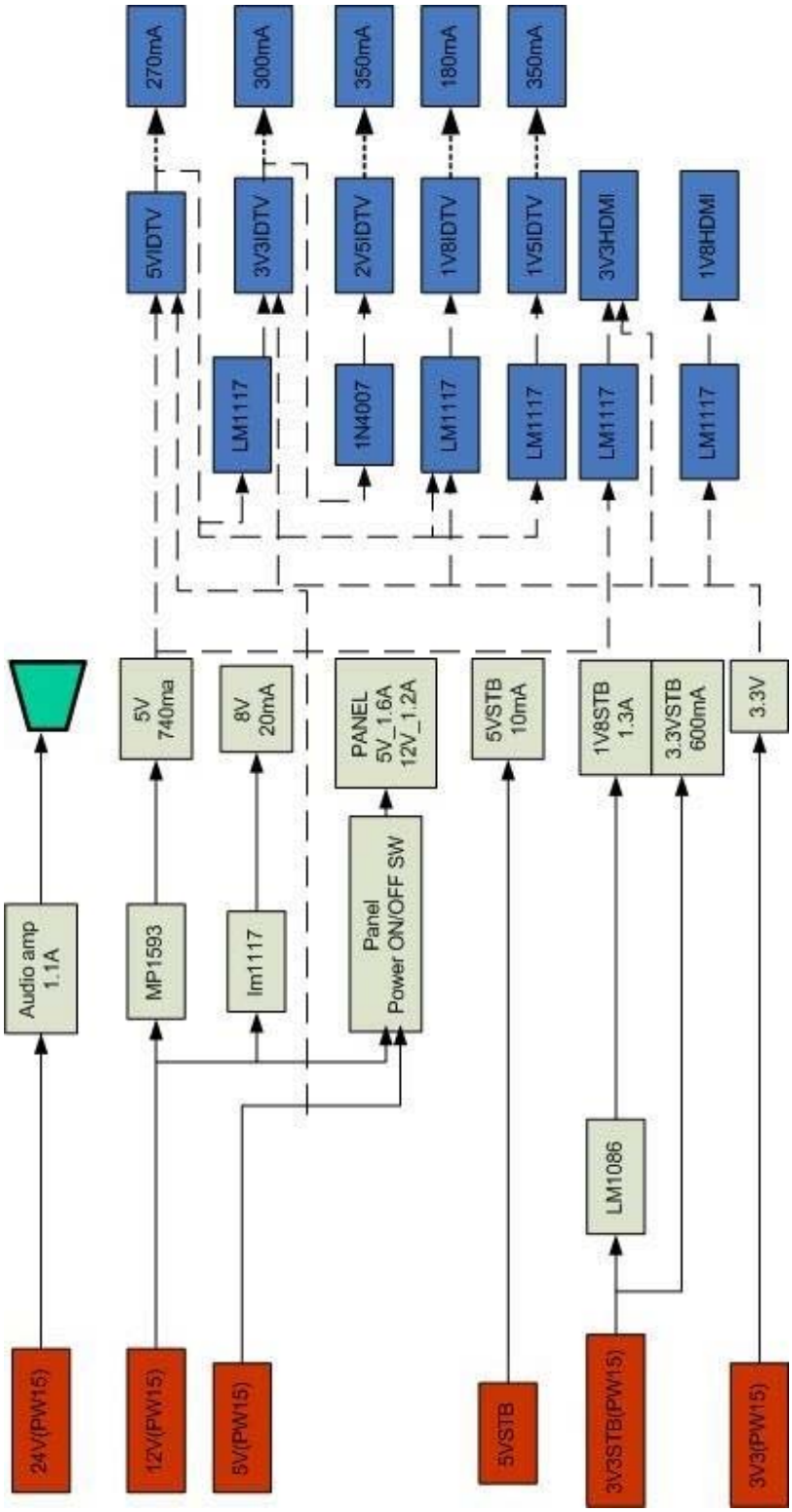
Step.1
Connect the serial cable from PC Com port to PL104 connector on 17PRG01-1 module card.
Step.2
Connect the programming cable from SCART(PL103) on 17PRG01-1 module card to SCART1 connector on TV chassis side.
Step.3
Run a RS232 terminal tool like Hyper Terminal.
Step.4
Following settings of the terminal tool are necessary:
Protocol: Xmodem
Port: COMx
Baud Rate: 115200
Data Bits: 8
Parity: none
Stop Bits: 1
Com. Control: none
Step.5
Load the bin file from **“Browse”** and Click **“Send”**
Step.6
Power off and on again TV set to produce hard reset.

18 BLOCK DIAGRAMS

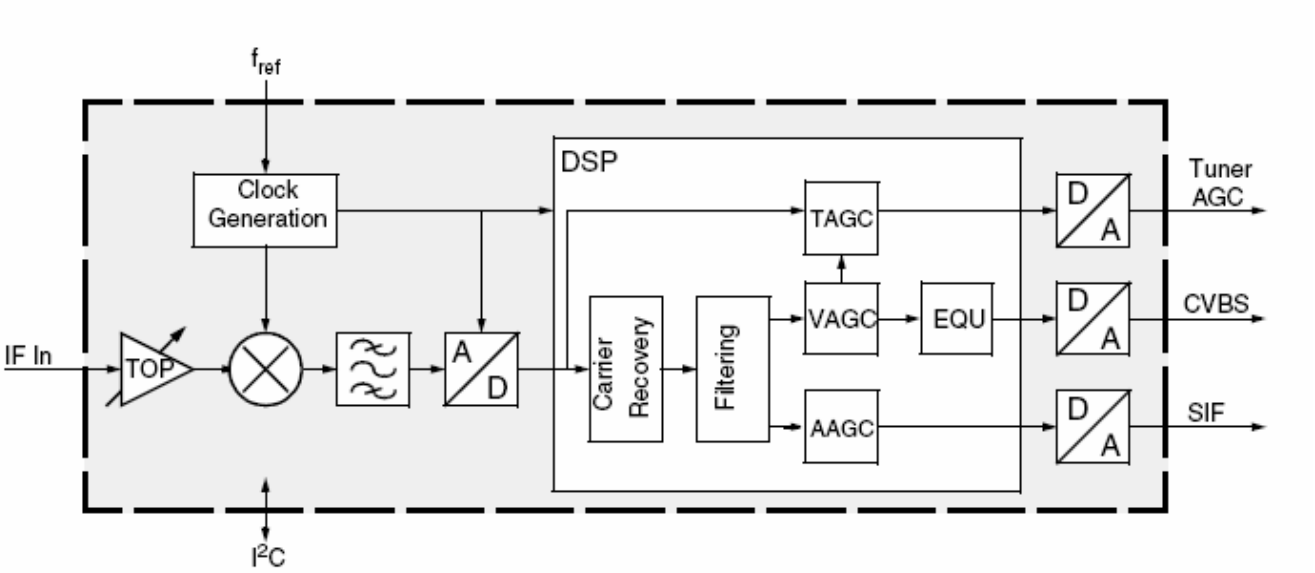
18.1 General Block Diagram


VCTP
SAW FILTER
DRX_D IF DECODER
TS
NEC MPEG DECODER
Rx
Tx
IDTV CVBS
IDTV Analog L/R
IDTV YPbPr
TV LINK
SAW FILTER
I2C
AGC
DRX_A IF DECODER
I2C
TUNER CVBS
QSS
AUDIO AMP.
Mute
IDTV SPDIF
SPDIF
S/W
HEAD PHONE AMP.
YPBPR or PC AIN
Mute
Audio Sw
NVM Protect
I2C
EEPROM
Service Port
5V
I2C
SERVICE & PROGRAM SOCKET
SC1 SW Update Rx
SC1 Update Tx
SCART1
SCART1 AUDIO IN
SCART1 AUDIO OUT
SCART1 CVBS OUT
SCART1 RGB + FB IN
LINE OUT
SCART2
PIP SOURCE CVBS
IDTV AUDIO IN
SCART2 AUDIO OUT
SCART2 CVBS OUT
SC2 C
SC2 CVBS
DMP / DVD CVBS IN
SCART1 AUDIO IN
SCART2 AUDIO IN
SCART1 CVBS
4053
SELECTED CVBS
SCART AUDIO IN
FAV CVBS IN
IDTV CVBS
SVHS Y
SVHS C
SC2 C
CHROMA SWITCH
SELECTED CHROMA
EXT DEVICE
EXT AUDIO IN
EXT RGB IN
EXT CVBS IN
FAV/SVHS AUDIO IN
FAV CVBS IN
YPBPR or PC AIN
EXT AUDIO IN
2X1 MUX AUDIO SWITCH
SPEAKERS
Vin1
SIF INPUT
AIN1
AOUT1
Vout1
Vin 6,7,9 + Vin8
Vout3
AIN2
AIN5 OR AOUT2
Vout2
Vin 15
Vin 3
Vin5
Vin2
Vin17
Vin16
AIN3
AIN4
Vin 11,12,13
Vin 19,20,21
SPDIF
Sub Woofer
HeadPhone
Audio Mux Switch
Mute(GPIO)
HP Detect
Dimming (PWM)
Back Light On/Off
Panel Power
NVM Protect
Power Protect
Service Mode Detect
TV LINK
Add On Module Control1
Add On Module Control2
Add On Module Control3
UART (RX)
UART (TX)
Scart2 Pin8 (ADC)
Scart1 Pin8 (ADC)
Keyboard (ADC)
IR (IR Decoder)
Standby On/Off(GPIO)
LED1(GPIO)
LED2(GPIO)
R/V Sync Switch(GPIO)
HDMI SCDT(INT)
HDMI Mute(INT)
I2C (2 Ports)
TV LINK
Module1
Module2
Module3
Rx
Tx
SC2 Pin8
SC1 Pin8
Keyboard
IR
Stby On/Off
LED1
LED2
Sync Switch
SCDT
MUTE
I2C
M TV/AV +P -P +V -V
DMP IR
ITU656 INPUT
ITU656 OUTPUT
JTAG
DIGITAL I/O
LVDS Output
8 Bit LVDS
PANEL POWER
DDC WRITE
EDID PROM(2)
3X8 Bit RGB Input
HSync(V/N2) VSync
XTAL IN
RESET IN
I2S Input
I2S
Clk, DE
3X8 RGB
MUTE SCDT HOT PLUG
XTAL
Reset
ANALOGIX 9021 HDMI IC
DDC
TMDS Data
TMDS Clk
HDMI CONNECTOR(2)
I2C
HSync, VSync
4X1 MUX SWITCH
Sync Switch
NOT :Sync sinyallerinden hangileri High-Z olabiliyor?
HSync + VSync
VGA MUX SWITCH
2X1 MUX RGB SWITCH
EXT RGB IN
VGA RGB
Y
Pb
Pr
PC
DDC
EDID PROM
POWER PROTECT
1.8V
3.3V
5V
8V
12V
24V
33V
Not : SCART 2 VIDEO OUT VE SD/HD PIP UYGULAMASINDA TÜM SD SOURCE'LARIN SCART2 OUT/DISPLAY EDILEBILMESI ICIN MATRIX VIDEO SWITCH ÇIKIŞI 2 FARKLI VCTP VIDEO GİRİŞİNE BAĞLANMIŞTIR

18.2 Power Management

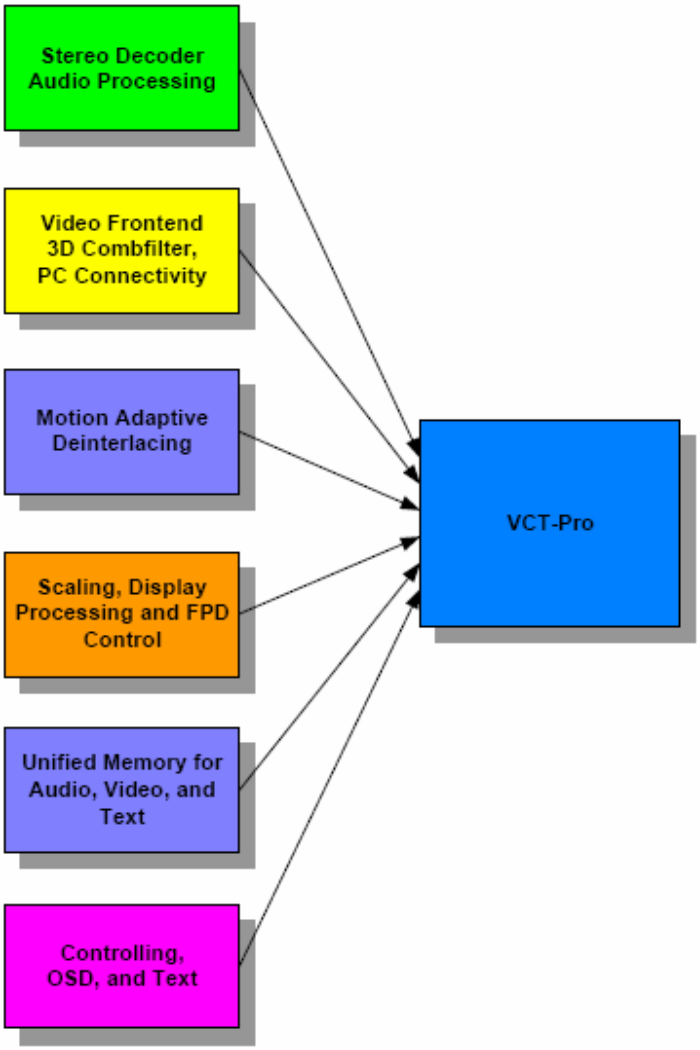


18.3 DRX (IF Demodulator) Block Diagram

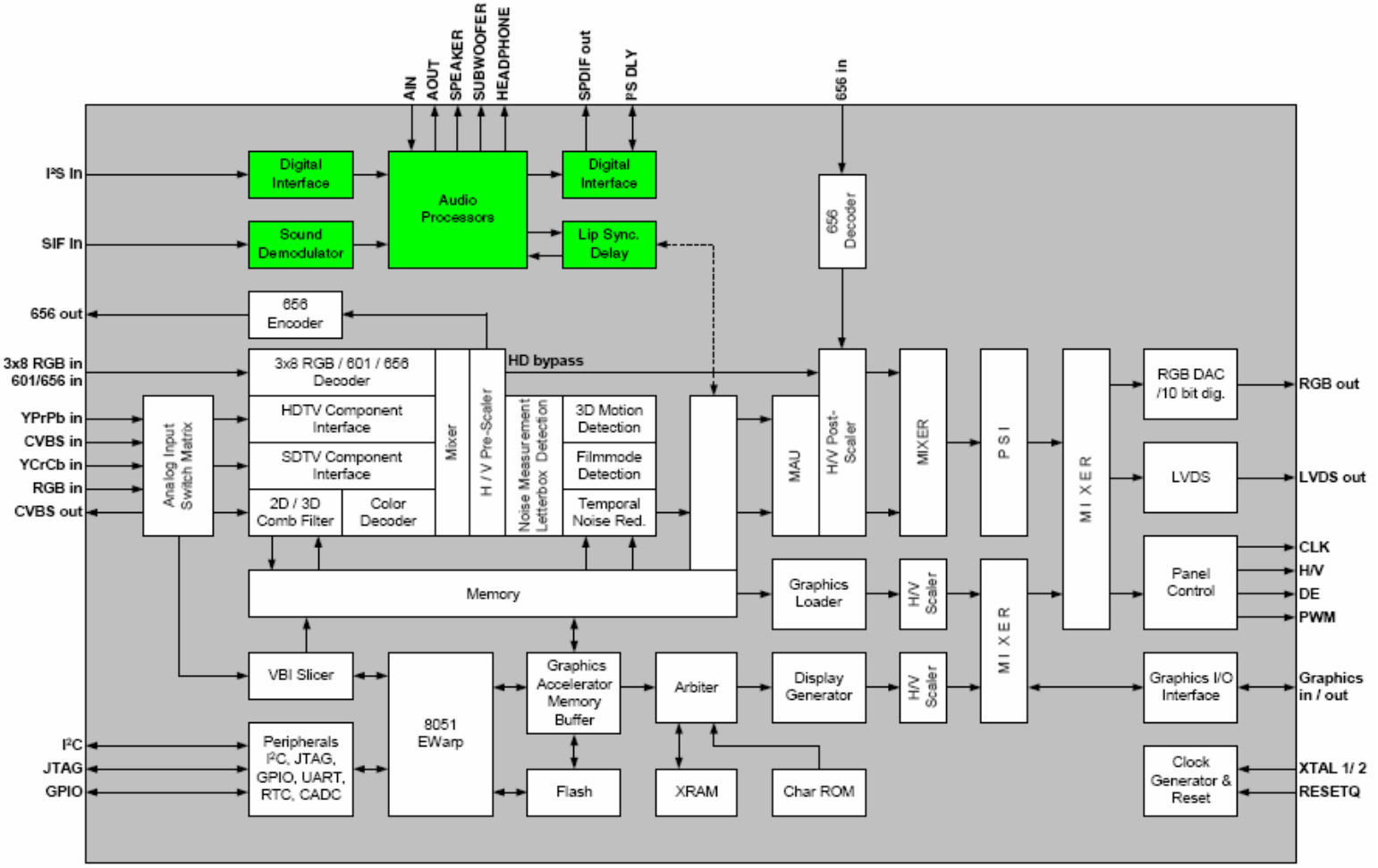


18.4 VCT Pro

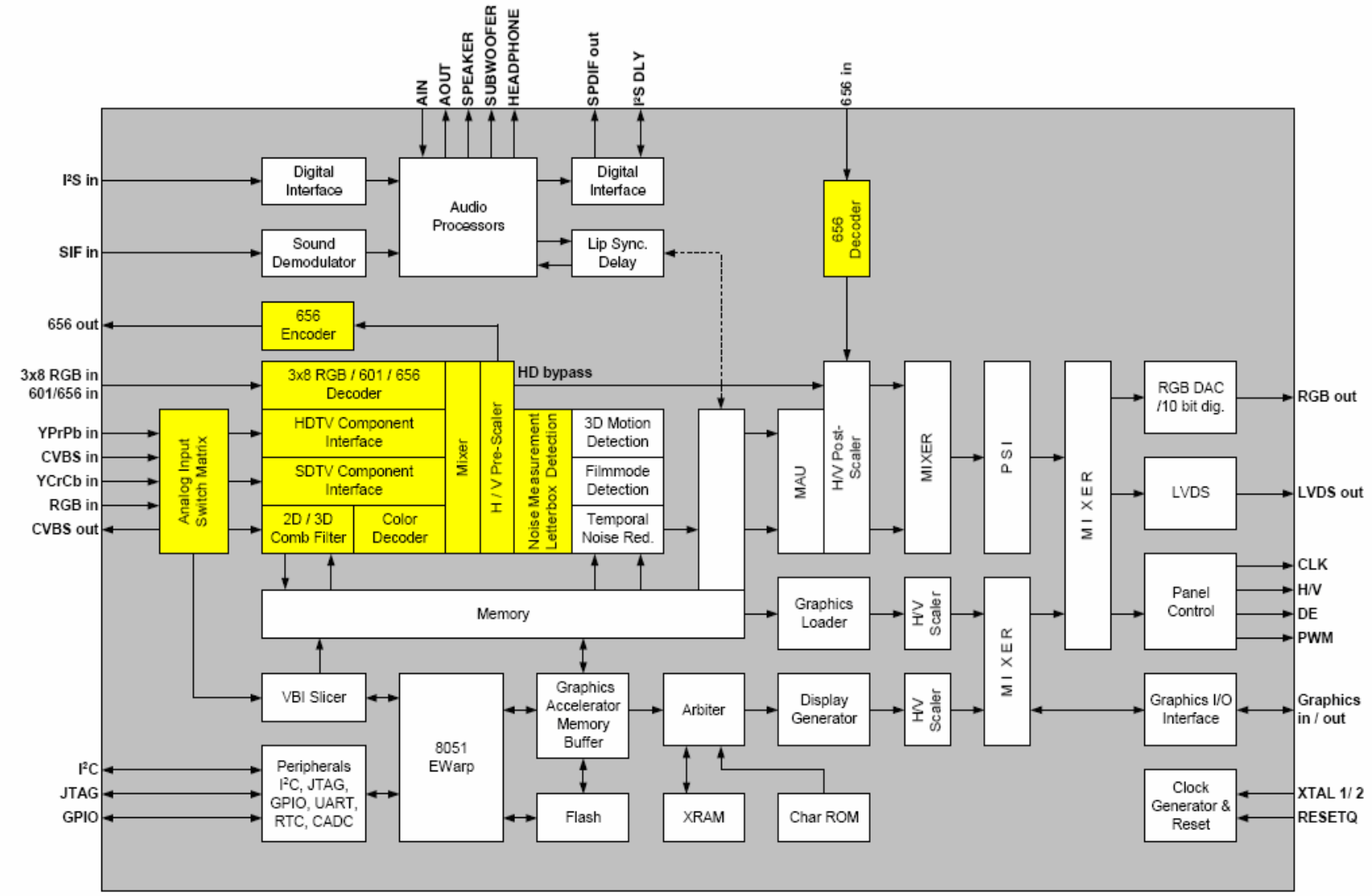
18.4.1 General Block Diagram


Stereo Decoder
Audio Processing
Video Frontend
3D Combfilter,
PC Connectivity
Motion Adaptive
Deinterlacing
Scaling, Display
Processing and FPD
Control
Unified Memory for
Audio, Video, and
Text
Controlling,
OSD, and Text
VCT-Pro

18.4.2 MSP Block Diagram



18.4.3 Video Processor of VCT 7wxyP Block Diagram


AIN
AOUT
SPEAKER
SUBWOOFER
HEADPHONE
SPDIF out
I²S DLY
656 in
I²S in
SIF in
Digital Interface
Sound Demodulator
Audio Processors
Digital Interface
Lip Sync. Delay
656 Decoder
656 out
656 Encoder
3x8 RGB in
601/656 in
3x8 RGB / 601 / 656 Decoder
HD bypass
YPrPb in
CVBS in
YCrCb in
RGB in
CVBS out
Analog Input Switch Matrix
HDTV Component Interface
SDTV Component Interface
2D / 3D Comb Filter
Color Decoder
Mixer
H / V Pre-Scaler
Noise Measurement Letterbox Detection
3D Motion Detection
Filmmode Detection
Temporal Noise Red.
MAU
H/V Post-Scaler
MIXER
PSI
MIXER
RGB DAC /10 bit dig.
RGB out
LVDS
LVDS out
Panel Control
CLK
H/V
DE
PWM
Memory
Graphics Loader
H/V Scaler
MIXER
VBI Slicer
8051 EWarp
Graphics Accelerator Memory Buffer
Arbiter
Display Generator
H/V Scaler
Graphics I/O Interface
Graphics in / out
I²C
JTAG
GPIO
Peripherals I²C, JTAG, GPIO, UART, RTC, CADC
Flash
XRAM
Char ROM
Clock Generator & Reset
XTAL 1/ 2
RESETQ

IC100
DRX3960A

AVSS_ADC 1
AVDD_ADC 2
ANATSTX 3
ANATSTY 4
AVDD_FE8 5
AVSS_FE8 6
AVSS_FE401 7
IFINX 8
AVDD_FE40 9
IFINY 10
AVSS_FE402 11
AVDD_SYN 12
AVSS_SYN 13
SHIELD 14
TEST0 15
TEST1 16
TEST2 17
CVBS 18
REF_SW 19
SIF 20
AVDD_DAC 21
AVSS_DAC 22
TEST_EN 23
RESETQ 24
SDA 25
SCL 26
DVDD_CAP 27
DVDD 28
DVSS 29
DVSS_CAP 30
PORT0 31
PORT1 32
TUNER_AGC 33
PORT2 34
PORT3 35
PORT4 36
ADR_SEL 37
PORT5 38
DVDD_ADC 39
DVSS_ADC 40
XTALIN 41
XTALOUT 42
VREF 43
SGND 44

IC101
74HCT4053

1 2Y1
2 2Y0
3 3Y1
4 3Z
5 3Y0
6 E
7 VEE
8 GND
16 VCC
15 2Z
14 1Z
13 1Y1
12 1Y0
11 S1
10 S2
9 S3

38.9MHz_TVTUN100

AGC 1
VT 2
AS 3
SCL 4
SDA 5
NC 6
VS 7
NC/ADC 8
VST 9
IF2/GND 10
IF1 11

Q101 BF799
Q102 BF799
Q103 BC848B
Q104 BC848B
Q105 FDC642P
Q106 BC858B
Q107 BC848B
Q108 BC848B
Q100 BC848B

Z100 X6966M
IN1 OUT1
IN2 OUT2
GND

FOR THE USE OF EXTERNAL CLOCK
C124,C134 IS 1NF [30012581]
X100 AND C123 IS REMOVED

DRX POWER SUPPLY

SHEET3 VCTP PIN80

SHEET 8
SW_ENABLE1
CHROMA_SW
AUDIO_MUX_SW
AMP/DVD_SWITCH

SHEET 3
SYNC_SW2
IDTV_YPbPr_SW
SCL_3V3_IC
SDA_3V3_IC
TUNER_CVBS_IN
RESET_IC

SHEET3
SCL_5V_IC
SDA_5V_IC

SHEET 3,5,6

SHOUL BE CONNECTED TO DRX GND

5V_TUNER
5V_DRX
3V3_DRX
5VL
VCC_5V
VCC_8V_VIDEO
VCC_3V3
12V_IF
DIG_IF-
DIG_IF+
ACTIVE_ANT.
AGC_DVB
SCLK_TUNER
SDATA_TUNER
TV/DVB_SWITCH
antenna_control
shortcir.
QSS

PTC RES
SHORT
N.C.

FROM 100 to 150

VESTEL ELECTRONICS	
17MB12-1 TUNER-DRX.1of13	
Date	Author
17.04.2007	ISMAIL YILMAZLAR SADIK SEHIT

TO SHT7
SC2_AUDIO_L_OUT
SC2_AUDIO_R_OUT
SC2_AUDIO_R_IN
SC2_AUDIO_L_IN
SC2_PIN8
TO SHT3
TV_LINK_3V
3V3_STBY
5V_STBY
SC2_SVHS_C
SC2_CVBS_IN
VCC_5V_VIDEO
VCC_3V3
VCC_5V
VCC_5V_EXT
VCC_8V
SVHS_C
SC2_SVHS_C
CHROMA_SW
CHROMA_SW_INV
SELECTED_C
PL203
Rx-Data
Tx-Clock
C5V6
C5V6_SOD123
SC1_AUDIO_R_IN
SC1_AUDIO_L_IN
SC1_AUDIO_R_OUT
SC1_AUDIO_L_OUT
SC1_CVBS_OUT
SC1_CVBS_IN
SC1_B
SC1_PIN8
SC1_G
vctpprog.
SC1_R
SC1_FB
TO SHT3 SHT7[TO VIDEO SW]
VOUT1
VOUT2
SHT3
VCTP_AOUT1R
VCTP_AOUT1L
SC1_AUDIO_R_OUT
SC1_AUDIO_L_OUT
SC1_AUDIO_L_IN
SC1_AUDIO_R_IN
TO SHT3 VCTP
HP_DETECT
HP_OUT_L
HP_OUT_R
TO SHT4
FAV_HP
FAV_AUDIO_L_IN
FAV_AUDIO_R_IN
FAV_CVBS_IN
TO SHT7
SC1_CVBS_OUT
SVHS_Y
SVHS_C
FAV_AUDIO_R_IN
FAV_AUDIO_L_IN
FAV VIDEO
PL200
DSUB_VGA_CONN
PL201
PL202
PL204
IC200
ST24LC21
SCL
SDA
VCLK
VCC
VSS
NC1
NC2
NC3
NC4
PC_R
PC_G
PC_B
TO SHT7
RGB SW
PC_HSYNC
PC_VSYNC
TO SHT3
SYNC SW
DDC_5V
DDC_SDA
DDC_SCL
PC_VSYNC
DDC_5V
TO SHT3 VCTP
PC_AUDIO_L_IN
PC_AUDIO_R_IN
HP_OUT_L
HP_OUT_R
JACK-AK16
JK201
PL206
DMP_DVD_VS_IN
DMP_DVD_CVBS_IN
DMP_DVD_AUDIO_L_IN
DMP_DVD_AUDIO_R
RESET_IC
I/O_1
IR_DMP/DV
DVB_TX
DVB_RX
SDA_3V3_IC
SCL_3V3_IC
IRQ
SW_ENAB
DMP_DVD_VSYNC
DMP_DVD_HSYNC
DMP_DVD_SWIT
SPDIF
VCTP_SPDIF
JK202
JACK_RCA_9P_YPBPR_SPDIF_LINIO
LINE_L_OUT
LINE_R_OUT
PC_AUDIO_R_IN
PC_AUDIO_L_IN
SC2_AUDIO_R_OUT
SC2_AUDIO_L_OUT
LINE_R_OUT
LINE_L_OUT
YPBPR_Y
YPBPR_PB
YPBPR_PR
SUBW
FERRITE
JUMPER_SMD_0402
S206
FROM 200 to 400

VESTEL ELECTRONICS

17MB12-1 PERIPHERAL.2of13

Date	Author
13.01.2006	ISMAIL YILMAZLAR SADIK SEHIT

VCT6953P
IC301

PC STANDBY MODE SYNC DETECTION

5V_STBY, R410 10k, R419 10k, R423 10k KEYBOARD, R424 10k sync_detect
PC_HSYNC R401 10k, PC_VSYNC R402 10k
Q401 BC848B, Q403 BC848B, Q405 BC848B, Q404 BC848B
C406 100n 10V, C417 1u 16V, R412 10k
VCC_3V3 R418 10k, R420 47k

JTAG CONN.

TCK, TDO, TDI, TMS
PL401: 10 9 8 7 6 5 4 3 2 1
3V3_STBY R417 47R
R428 4x47R: R1 8 R2 7 R3 6 R4 5
R411 4k7, Q402 BC848B, R408 47k
Q400 BC848B, R400 4k7, R401 47k
D411 C5V6, R413 10R, R571 1k, C416 470u 16V
IC400 LM809, C498 10p 50V, S445

EXTERNAL AMP.

PL400: 1 2 3 4 5
AMP_MUTE

SHEET 4
HEADPHONE_R, HEADPHONE_L, AMPLIFIER_R, AMPLIFIER_L
R407 47k, R416 47k SHORT, R405 10k N.C., R414 10k N.C.
R406 47k SHORT, R415 47k SHORT, R404 10k N.C., R409 10k N.C.
C430 50V 3n3, C435 25V 68n, C445 100n 10V, C425 50V 3n3
C418 10n 16V, R421 4k7, C419 10n 16V, R422 4k7
AMPLIFIER_R_NEG, AMPLIFIER_L_NEG, vctp audio ground

SHEET 1
QS9

VCTP POWER SUPPLIES

VCC_5V, VCC_8V, 3V3_STBY
L407, L400, L408, L401, L406 600_100MHZ_3A, L402, L409, L403, L412, L404, L411, L405, L410, L413, L414
VSUP_5V_SIF, VSUP_3V3_DAC, VSUP_8V_AU, VSUP_3V3_FE, VSUP_1V8_DIG, VSUP_3V3_DIG, VSUP_1V8_FE, VSUP_3V3_LVDS, VSUP_3V3_DRI_RAM, VSUP_1V8_LVDS, VSUP_3V3_IO1, VSUP_3V3_FL, VSUP_3V3_IO3, VSUP_3V3_VO
D412 C3V6, TANTAL CASE A, D410 C3V6

SHEET 2
SC_AUDIO_R_IN, SC_AUDIO_L_IN, IDTV_R, IDTV_L, FAV_AUDIO_R_IN, FAV_AUDIO_L_IN, DMPORPC_R_AUDIO, DMPORPC_L_AUDIO
C442–C452 1u 16V, C439 3n3 50V, C437 100n 10V

SHEET 3
VCTP_AOUT2R, VCTP_AOUT2L, VCTP_AOUT1R, VCTP_AOUT1L

SHEET 5
HDMI_CEC_SEL, EQ_1, R427 10k, VSUP_3V3_COM
SYNC_SW1, R430 10k, VSUP_3V3_COM
R426 4x10k, R425 10k 3V3_STBY, sync_detect

SHEET 5
SDA, SCK, WS
R434 47R, R435 47R, R436 47R
R431 4k7, VCTP_SPDIF
R437 47R, R451 10k, R438 10k, R450 10k, R433 47R
HDMI_DE, HDMI_CLK, HDMI_R7, HDMI_R6, HDMI_R5
R432 4x47R, R452 10k

SHEET 5
R449 4x10k, R444 4x10k, R445 4x10k, R446 4x10k, R447 4x10k, R448 4x10k
R441 4x10k, R443 4x10k, R454 4x10k, R456 4x10k, R439 4x10k, R453 4x10k
HDMI_R0 … HDMI_R7, HDMI_G0 … HDMI_G7, HDMI_B0 … HDMI_B7
VSUP_3V3_DRI_RAM

SHEET 1
R426 4x47R, R427 4x47R, R428 4x47R, R429 4x47R
R424 4x47R, R423 4x47R, R422 4x47R, R421 4x47R
R420 4x47R, R419 4x47R, R418 4x47R, R417 4x47R
R416 4x47R, R415 4x47R, R414 4x47R, R413 4x47R
R412 4x47R, R411 4x47R, R410 4x47R, R409 4x47R
R408 4x47R, R407 4x47R, R406 4x47R, R405 4x47R
R404 4x47R, R403 4x47R, R402 4x47R, R401 4x47R
R400 4x47R, R399 4x47R, R398 4x47R, R397 4x47R
R396 4x47R, R395 4x47R, R394 4x47R, R393 4x47R
R392 4x47R, R391 4x47R, R390 4x47R, R389 4x47R
R388 4x47R, R387 4x47R, R386 4x47R, R385 4x47R
R384 4x47R, R383 4x47R, R382 4x47R, R381 4x47R
R380 4x47R, R379 4x47R, R378 4x47R, R377 4x47R
R376 4x47R, R375 4x47R, R374 4x47R, R373 4x47R
R372 4x47R, R371 4x47R, R370 4x47R, R369 4x47R
R368 4x47R, R367 4x47R, R366 4x47R, R365 4x47R
R364 4x47R, R363 4x47R, R362 4x47R, R361 4x47R
R360 4x47R, R359 4x47R, R358 4x47R, R357 4x47R

656O7 208, 656CLKO 207, 656CLKI 206, 656I7 205, 656I6 204, 656I5 203, 656I4 202, 656I3 201, 656I2 200, 656I1 199, 656I0 198, VSUP3.3IO3 197, GND3.3IO3 196
VOUT1 195, VOUT2 194, VOUT3 193, VSUP3.3V3 192, VIN1_19 191, VIN1_20 190, VIN1_21 189, VIN1_22 188, VIN1_23 187, GND3.3VIN1 186, VSUP1.8FE_2 185, VIN2_7 184, VIN2_8 183, VIN2_9 182, VIN1_0 181, VIN1_1 180, VIN1_2 179, VIN1_3 178, VIN1_4 177, VIN1_5 176, VIN1_6 175, VIN1_7 174, VIN2_0 173, VIN2_1 172, VIN2_2 171, VSUP3.3FE 170, VSUP1.8FE_1 169, P1_0 168, P1_1 167, P1_2 166, P1_3 165, VSUP3.3DAC 164, GND3.3DA 163, P1_4 162, P1_5 161, P1_6 160, P1_7 159, LVDSB_0 158, LVDSB_1 157

SHEET 5
SHEET1,2,8
VOUT1, VOUT2, TUNER_CVBS_IN, IDTV_CVBS_IN, SC_CVBS_IN, FAV_CVBS_IN, SC1_R, SC1_G, SC1_FB, SC1_B, PR_IDTV_R_IN, Y_IDTV_G_IN, PB_IDTV_B_IN, DMP_DVD_CVBS_IN, SELECTED_C, SVHS_Y, VGA_DVDIMP_R, VGA_DVDIMP_G, VGA_DVDIMP_B
R365 75R, R366 75R, R367 75R, R368 75R, R369 75R, R370 75R, R371 75R, R372 75R, R373 75R, R374 75R, R375 75R, R376 75R
C459 220u 16V, C460 220n, C461 220u 16V, C462 220u 16V, C463 220u 16V, C464 220u 16V, C465 220u 16V, C466 220u 16V, C467 220u 16V, C468 220u 16V, C469 220u 16V, C470 220u 16V, C471 220u 16V, C472 220u 16V, C473 220u 16V, C474 220u 16V, C475 220u 16V, C476 220u 16V, C477 220u 16V, C478 220u 16V, C479 220u 16V, C480 220u 16V, C481 220u 16V, C482 220u 16V, C483 220u 16V, C484 220u 16V, C485 220u 16V
R461 10k, R462 10k, R463 10k, R464 10k, R465 10k, R466 10k, R467 10k, R468 10k, R469 10k, R470 10k, R471 10k, R472 10k, R473 10k, R474 10k, R475 10k, R476 10k, R477 10k, R478 10k, R479 10k, R480 10k, R481 10k, R482 10k, R483 10k, R484 10k
VSUP_3V3_VO, VSUP_3V3_FE, VSUP_3V3_FL, VSUP_3V3_IO3, VSUP_3V3_COM, VSUP_3V3_DIG, VSUP_3V3_DAC, VSUP_3V3_DRI_RAM, VSUP_3V3_IO1, VSUP_3V3_LVDS, VSUP_1V8_DIG, VSUP_1V8_FE, VSUP_1V8_LVDS, VSUP_3V3_VO
HSYNC, VSYNC, DAYLIGHT_DIM, EDID_CONTROL, SCL_3V3, SDA_3V3, EEPROM, SHEET 7: SCL_7, SCL_PIN

S449, S401, S402, S403, S404, S405, S406, S407, S408, S409, S410, S411, S412, S413, S414, S415, S416, S417, S418, S419, S420, S421, S422, S423, S424, S425, S426, S427, S428, S429, S430, S431, S432, S433, S434, S435, S436, S437, S438, S439, S440, S441, S442, S443, S444, S445, S446, S447, S448

IC303 M74HC4052

DMP_DVD_CVBS_IN, 1k R523
HDMI_HSYNC, HSYNC, S420, S405, R522 1k
PC_HSYNC, PC_VSYNC, S434, S435, R549 1k, R552 1k, R558 4k7, R564 4k7, R553 4k7, S436, R557 47k, S448

Y0 1		VCC 16	5V_STBY
Y2 2		X2 15	HDMI_VSYNC
COM_Y_OUT_IN 3		X1 14	PC_VSYNC
Y3 4		COM_X_OUT_IN 13	VSYNC
Y1 5		X0 12	MP_DVD_VS_IN
INH 6		X3 11	
VEE 7		A 10	
GND 8		B 9	

SYNC SWITCH

KEYBOARD CONN.

KEYBOARD, R494 47k, R504 47k, PL403: 2 1
R486 1k5, VSUP_3V3_COM, KEYBOARD
C487 100n 10V, D407 C5V6, C488 10V 100n, C489 16V 1u, C490 10V 100n
5V_COM, VCC_5V, S417
PL402 VSUP_3V3_COM: 1 2 3 4 5, HWSDA, KEYBOARD
S407 NEGLEO, R490 4k7, HDMI_DETECT, C486 100n 10V, R485 4k7
R491 1k, R492 4k7, Q407 BC848B, S408, Q406 BC848B, S409, R505 4k7, R513 4k7, R502 4k7, R506 4k7
HDMI_MUTE, HDMI_SCDT, SHEET 5

LVDS OUTPUT

VSUP3.3LVDS5	156		VSUP_3V3_LVDS
LVDSB_1N	155		*NC
LVDSB_1P	154		*NC
GND3.3LVDS4	153		
LVDSB_2N	152		*NC
LVDSB_2P	151		*NC
VSUP3.3LVDS4	150		VSUP_3V3_LVDS
LVDSB_CLKN	149		*NC
LVDSB_CLKP	148		*NC
GND3.3LVDS3	147		
LVDSB_3N	146		*NC
LVDSB_3P	145		*NC
GND1.8LVDS	144		
REXT	143	R496 6k2	
VSUP1.8LVDS	142		VSUP_1V8_LVDS
LVDSA_0N	141		TXOUT0-
LVDSA_0P	140		TXOUT0+
VSUP3.3LVDS3	139		VSUP_3V3_LVDS
LVDSA_1N	138		TXOUT1-
LVDSA_1P	137		TXOUT1+
GND3.3LVDS2	136		
LVDSA_2N	135		TXOUT2-
LVDSA_2P	134		TXOUT2+
VSUP3.3LVDS2	133		VSUP_3V3_LVDS
LVDSA_CLKN	132		TXCLKOUT-
LVDSA_CLKP	131		TXCLKOUT+
GND3.3LVDS1	130	R499 10k	VSUP_3V3_LVDS
LVDSA_3N	129		TXOUT3-
LVDSA_3P	128		TXOUT3+
VSUP3.3LVDS1	127		VSUP_3V3_LVDS
LVDSA_4N	126		*NC
LVDSA_4P	125		*NC
VSUP1.8DIG	124		VSUP_1V8_DIG
GND1.8DIG	123		
PCLK1	122		
PCLK2	121		
PCS0	120	R495 100R	CABLE_DET1
PCS1	119		
PCS2	118		
PCS3	117	47R	LED2
PCS4	116	R497 47R	LED1
PCS5	115	R498	
VSUP3.3IO1_2	114	R514 10k	VSUP_3V3_COM
GND3.3IO1_2	113		
OSDR0	112		
OSDR1	111		
OSDR2	110		
OSDR3	109		
OSDG0	108		
OSDG1	107		
OSDG2	106	R500 47R	
OSDG3	105	R501 47R	

R508 10k VSUP_3V3_COM, HDMI1_CEC, R512 10k VSUP_3V3_COM, HDMI1_HOTPLUG
R568 1k2 VSUP_3V3_COM, S450, Q432 BC848B, STBY_ON_OFF
R509 10k VSUP_3V3_COM, R510 10k VSUP_3V3_COM, R511 10k VSUP_3V3_COM
R503 10k VSUP_3V3_COM, R516 4k7, Q408 BC848B, R517 47R, SCL_3V3, R518 47R, SDA_3V3
R489 10k VSUP_3V3_COM, R567 4k7 VSUP_3V3_COM, MP_MUTE, IRQ, R493 10k VSUP_3V3_COM, XTSYN_SW, W_PROTECT

IC302 IC308 24LC32A M24C128 24C64 USED 30021752

A0	1		VCC 8
E0	1		VCC 8
A1	2		WP 7
E1	2		WC 7
A2	3		SCL 6
E2	3		SCL 6
VSS	4		SDA 5
VSS	4		SDA 5

C499 10p 50V, C498 22p 50V, C497 10p 50V, C495 10p 50V, C496 10p 50V, C492 10V 10u, C493 22p 50V, C494 22p 50V

TUNER

X400 29.25MHz, C407 22p 50V, C408 22p 50V
R467 10k, R468 10k, R469 10k, R470 10k, R471 10k, R472 10k, R473 10k, R474 10k, R475 10k, R476 10k, R477 10k, R478 10k, R479 10k, R480 10k, R481 10k, R482 10k, R483 10k, R484 10k
IR_VCTP, UART_RX, UART_TX, CABLE_DET1, RESET_IC, VSUP_3V3_COM, VSUP_3V3_FL, VSUP_3V3_IO1, VSUP_3V3_IO3, VSUP_3V3_VO, VSUP_3V3_DRI_RAM, VSUP_3V3_CXM, VSUP_3V3_DIG, VSUP_3V3_DAC, VSUP_3V3_FE, VSUP_1V8_DIG, VSUP_1V8_FE, VSUP_1V8_LVDS, VSUP_3V3_LVDS, VSUP_3V3_COM
DRX_CLK, L415 600_100MHZ_3A, L416, C464 50V 3n3, C466 50V 3n3, C465 100n 10V
L417,L416 SHOULD BE 30016659
S465 SOULD BE B2R
HWSCL, HWSDA, COMMON I2C

IR DETECT & LED DRIVE

5V_STBY, 3V3_STBY, S429, S432
IR_DMP/DVD_SWITCH, R524 100R, R525 10k
PL405: 5 4 3 2 1
3V3_STBY, IR_DMP/DVD, Q418 BC848B, R539 4k7, S428
IR_VCTP, R533 4k7, R561 220R
LED2, R531 3k3, Q426 BC848B, R562 220R, VSUP_3V3_COM, R524 10k
LED1, R526 10k, VSUP_3V3_COM, R538 3k3, Q428 BC848B
S430, S433, S436, S442, S443, S444, S445, S446, S447

HDMI_HOTPLUG

INT, HDMI0_HOTPLUG, SHEET 5
vctpprog., C497 10p 50V, R547 47k, R565 10k
Tx-Clock, Rx-Data, C495 10p 50V, C496 10p 50V, Q423 BC848B, Q421 BC848B, Q424 BC848B
R550 47k, R559 47k, R551 47k, R566 10k, UART_TX, UART_RX
Q430 BSN20, Q431 BSN20, R540 47k, R541 47k, R545 10k, R536 47k, R542 47k, R543 47k, R548 47k
HWSDA, HWSCL, SCL_5V_IC, SDA_5V_IC, SCL_3V3_IC, SDA_3V3_IC, S440, S448

TV_LINK_3V3

S411, Q409 BC848B, R521 4k7, R522 4k7, S417
PANEL_VCC_ON/OFF, R502 4k7, PANEL_VCC

IR_DMP/DVD_SWITCH

S412, S413, PANEL_VCC
S410: 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
TXOUT0-, TXOUT0+, TXOUT1-, TXOUT1+, TXOUT2-, TXOUT2+, TXCLKOUT-, TXCLKOUT+, TXOUT3-, TXOUT3+
S422, S423, S424, S425, PANEL_VCC, VCC_3V3, VCC_5V, VCC_12V
CBU_GO, R537 10k, VSUP_3V3_COM, R546 10k, VSUP_3V3_COM, R507 10k, R530 10k, S419, R520 10k, VSUP_3V3_COM
S439, Q427 BC848B, R560 4k7, STBY_ON_OFF
PL404, LVDS OUTPUT

SHORT CIRCUIT AND HEADPHONE DETECT

*POWER ON/OFF PORT SAVING
R482 10k, R483 10k, VSUP_3V3_COM
S427, PROTECT_DETECT, S429, S431, R529 1k, R553 10k
D409 C5V6, C493 10u 16V, R548 4k7, Q419 BC848B, HP_DETECT

FROM 400	
VESTEL ELECTRONICS	
17MB12-1 TUNER-DRX.3of13	
Date	Author
17.04.2007	ISMAIL YILMAZLAR SADIK SEHIT

FROM 600 to 650

VESTEL ELECTRONICS	
17MB12 AUDIO AMP. 4of13	
Date	Author
03.01.2006	ISMAIL YILMAZLA RASIT GOKALAN

IC555

IC550 UPA672T

IC551 UPA672T

IC552 24LC02

IC553 24LC02

IC554 UPA672T

IC556 SN74CB3Q3305

VESTEL ELECTRONICS	
17MB12-1 HDMI. 5of13	
Date	Author
17.04.2007	ISMAIL YILMAZLAR SADIK SEHIT

FROM 650 to 750

HDMI CONNECTOR 0

HDMI CONNECTOR 1

HEADPHONE AMPLIFIER

IC600 TDA1308T

IC475 TDA8932

IC862 PI5V330_SOIC

IC652 M74HC4052

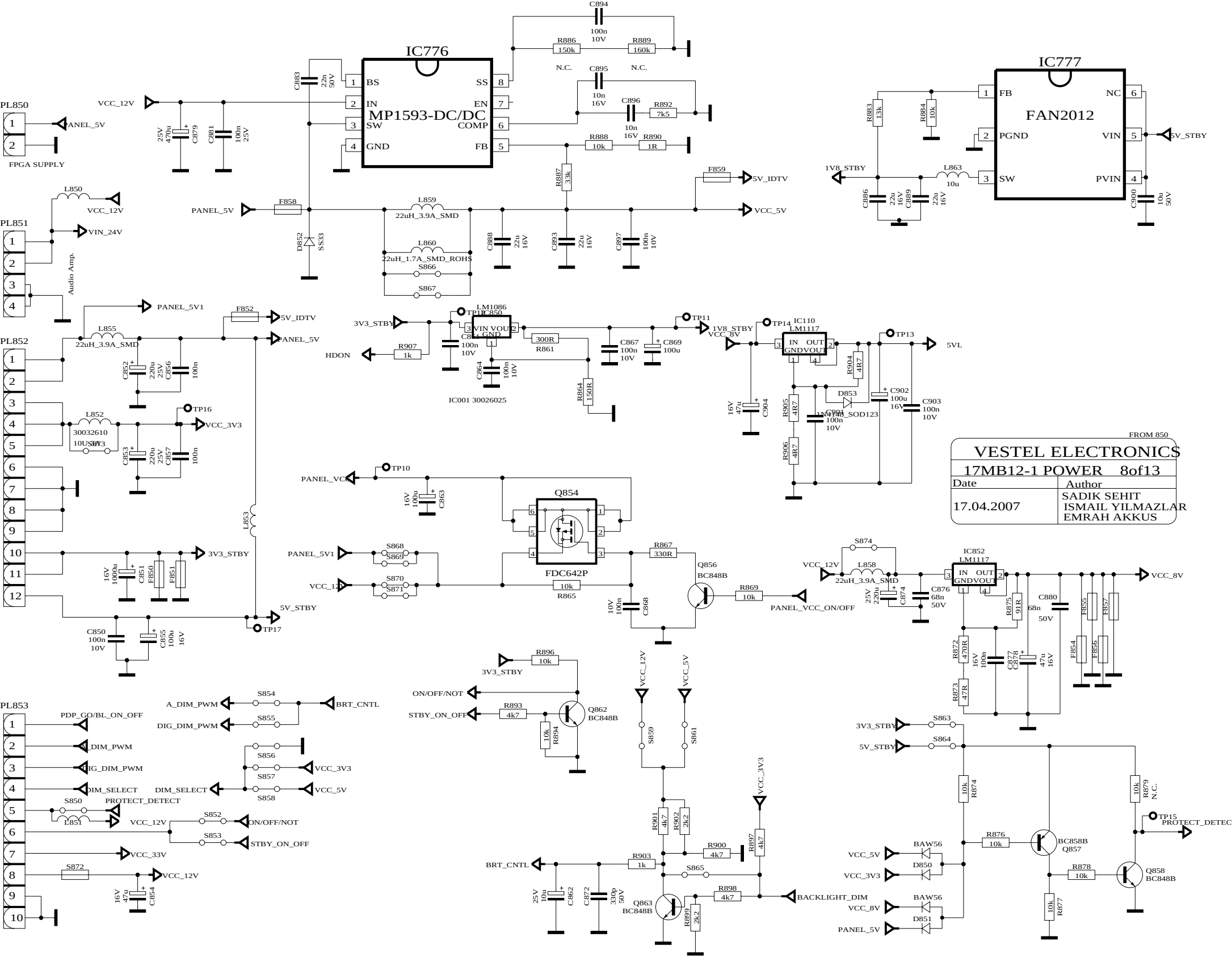
IC653 74HCT4053

IC656 FMS6145

IC657 PI5V330_SOIC

VESTEL ELECTRONICS	
17MB12-1 AUDIO&SW 6of13	
Date	Author
17.04.2007	SADIK SEHIT ISMAIL YILMAZLAR

FROM 750 to 850


IC776
MP1593-DC/DC
BS
SS
IN
EN
SW
COMP
GND
FB
IC777
FAN2012
FB
NC
PGND
VIN
SW
PVIN
PL850
FPGA SUPPLY
PANEL_5V
PL851
Audio Amp.
VIN_24V
PL852
PL853
VCC_12V
VCC_3V3
VCC_5V
VCC_8V
VCC_33V
5V_STBY
3V3_STBY
5V_IDTV
PANEL_5V1
PANEL_VCC
HDON
5VL
1V8_STBY
BACKLIGHT_DIM
PROTECT_DETEC
PDP_GO/BL_ON_OFF
A_DIM_PWM
B_DIM_PWM
DIG_DIM_PWM
DIM_SELECT
BRT_CNTL
ON/OFF/NOT
STBY_ON_OFF
PANEL_VCC_ON/OFF
IC110
LM1117
IC852
LM1117
LM1086
IC001 30026025
FDC642P
BC848B
BC858B
BAW56
FROM 850
VESTEL ELECTRONICS
17MB12-1 POWER 8of13
Date
17.04.2007
Author
SADIK SEHIT
ISMAIL YILMAZLAR
EMRAH AKKUS

UPD6111
IC860

MPEG DECODER

TO SHT3

PL952

PL950

JTAG

JTAG & ETAG CONNECTOR

IC204

M24C128

VCXO CIRCUIT

PI6CX100-27WE

IC861

27MHz-SMD2-SMD

STRAP PIN JUMPERS

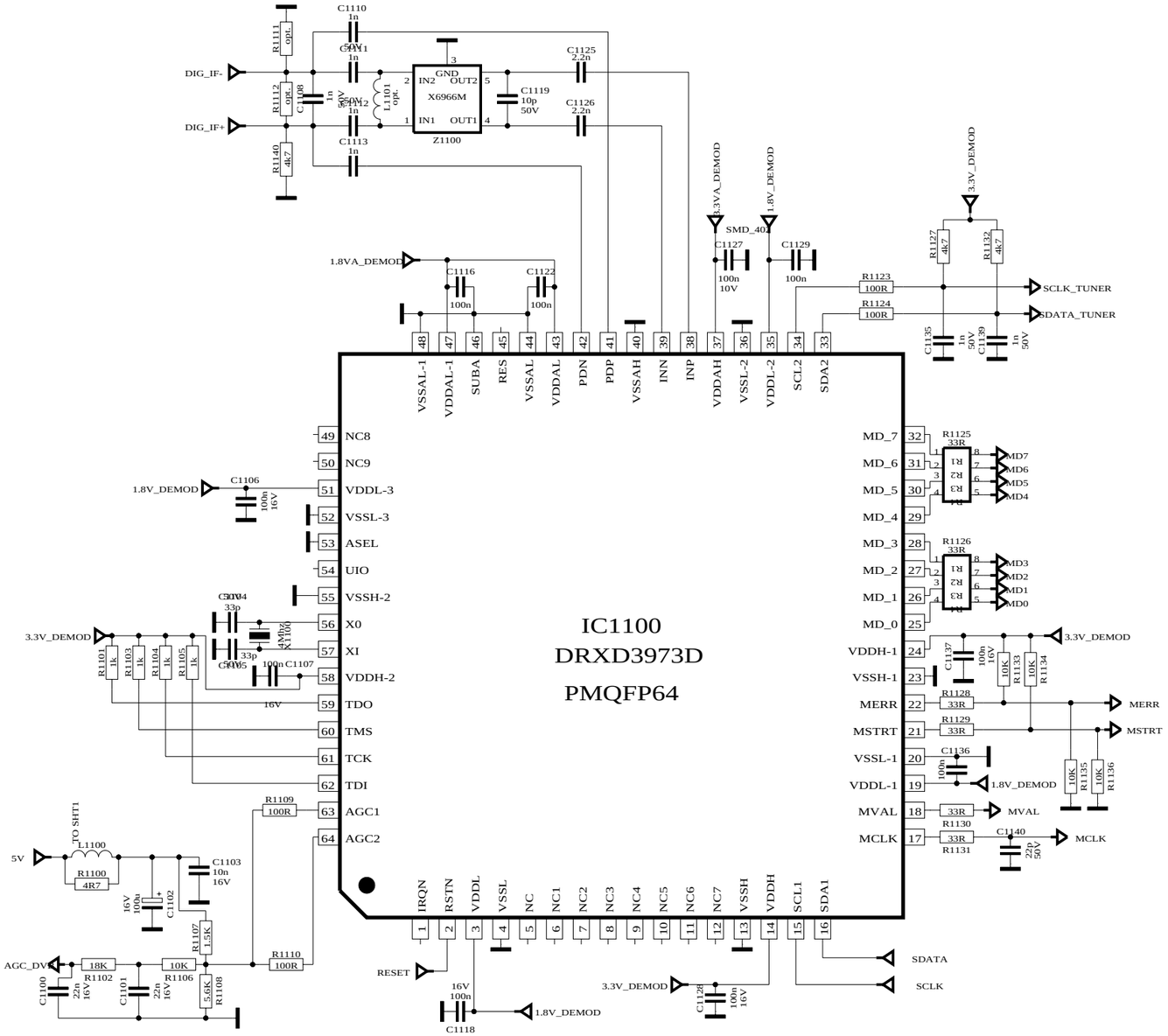
RESET CIRCUITS

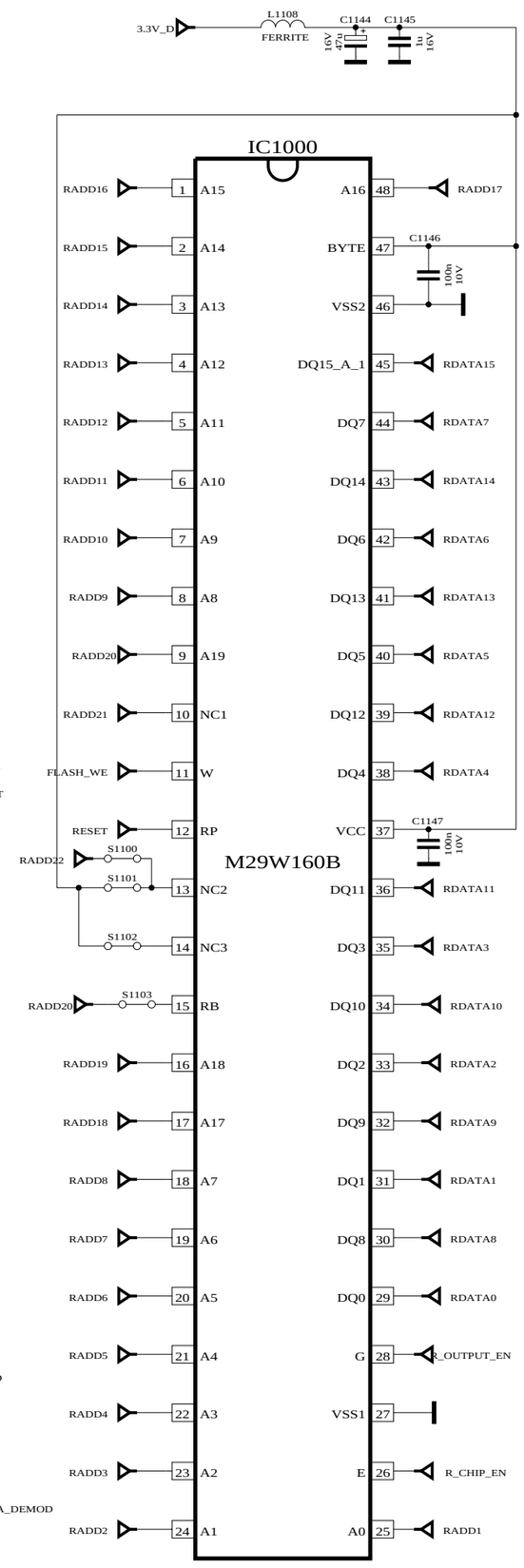
PL951

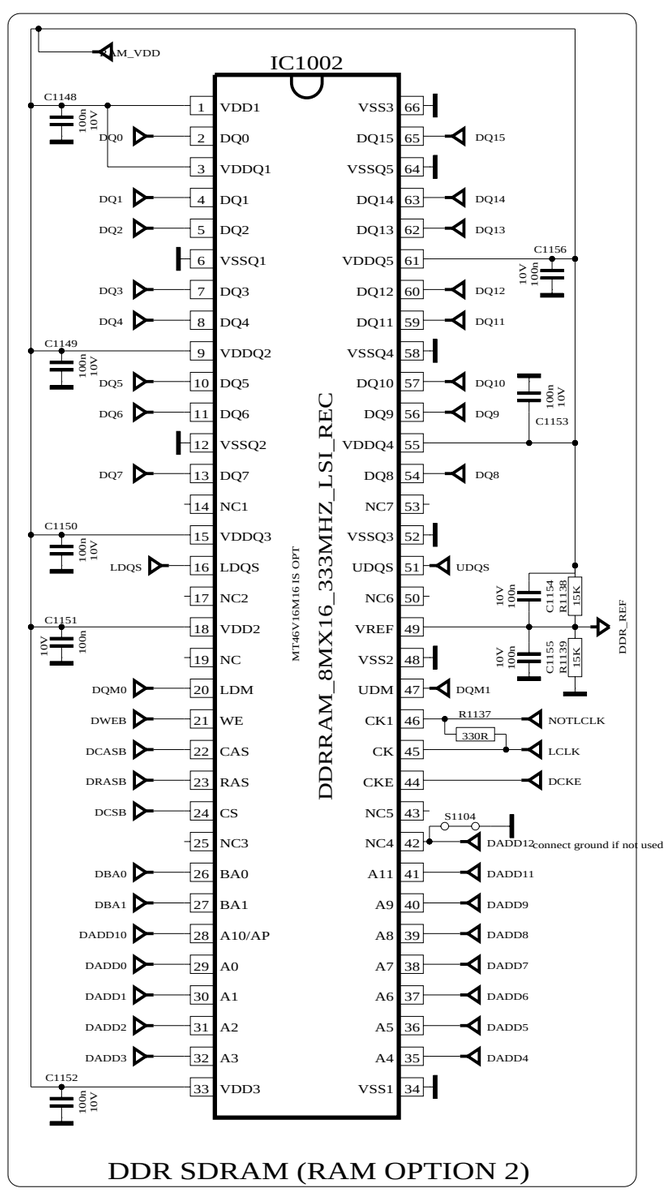
POWER

VESTEL ELECTRONICS	
17MB12-1 MPEG 9of13	
Date	Author
17.04.2007	SADIK SEHIT ISMAIL YILMAZLAR ONUR KORHAN SAY

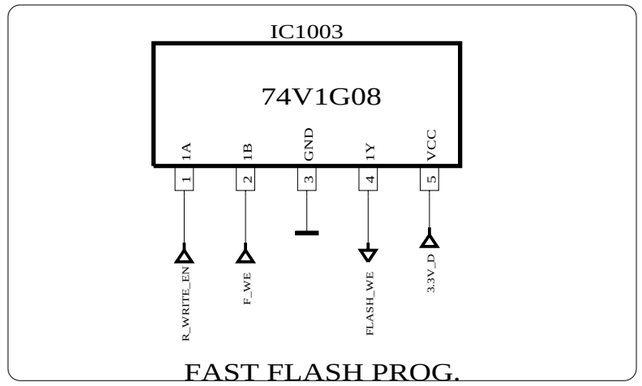
FROM 950



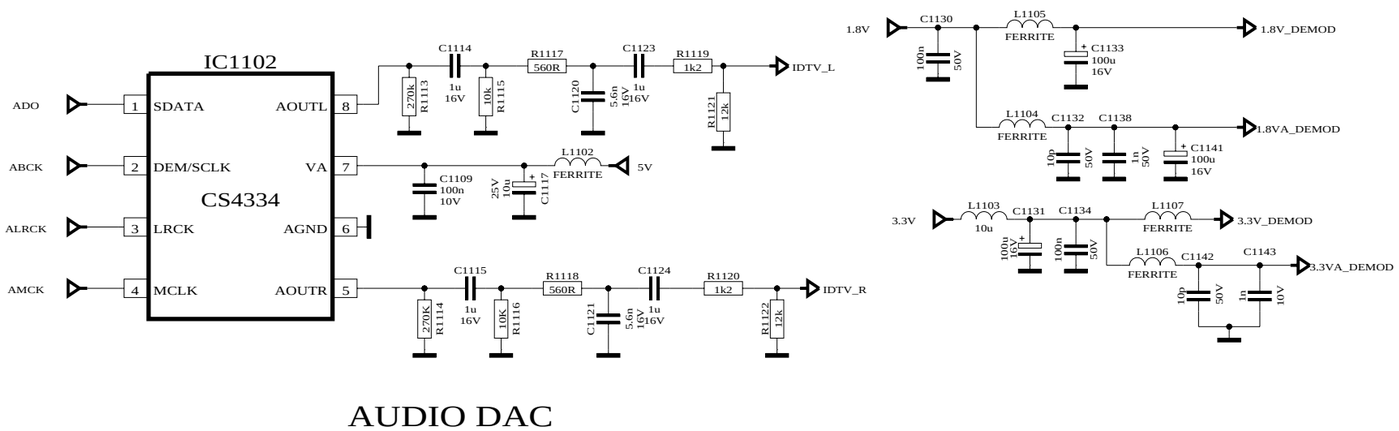




DDR SDRAM (RAM OPTION 2)



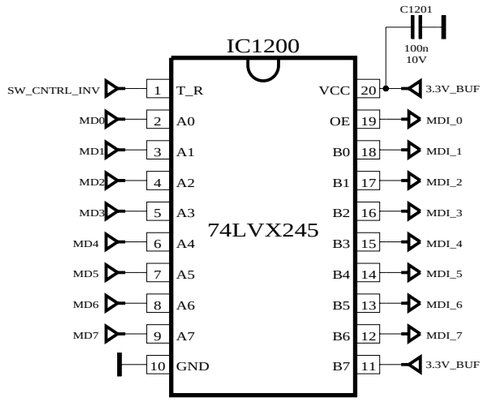
FAST FLASH PROG.

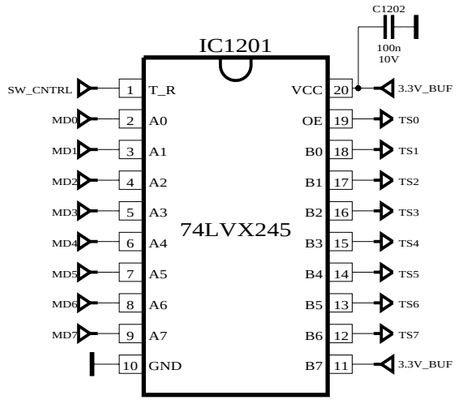


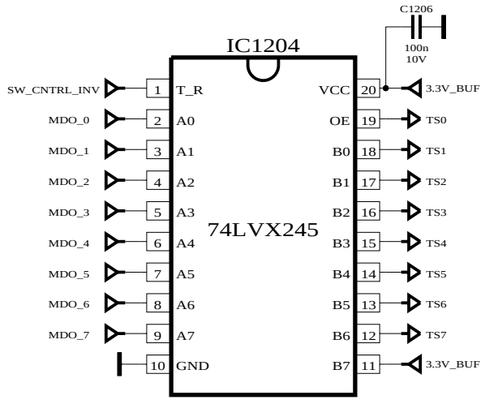
AUDIO DAC

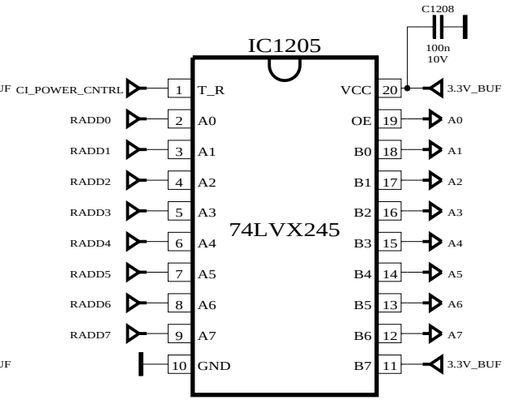
FROM 1000 to 1050

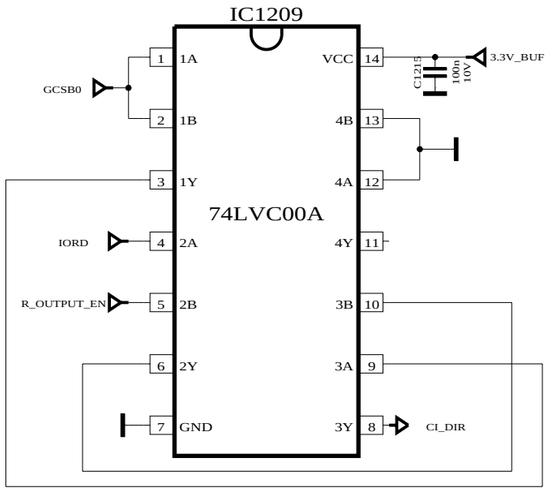
VESTEL ELECTRONICS	
17MB12-1 MPEG RAM 9of13	
Date	Author
17.04.2007	SADIK SEHIT ISMAIL YILMAZLAR ONUR KORHAN SAYIN

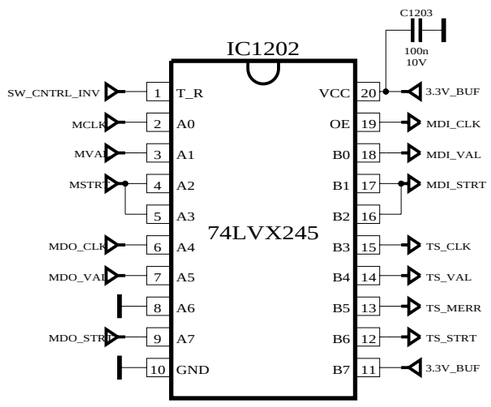


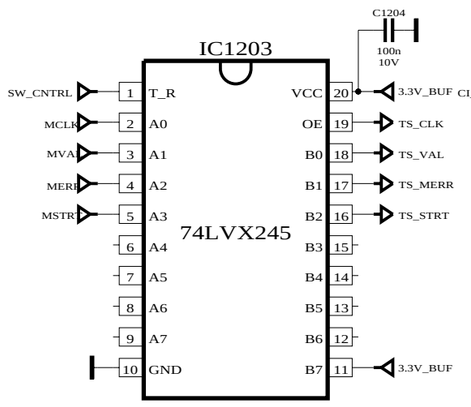


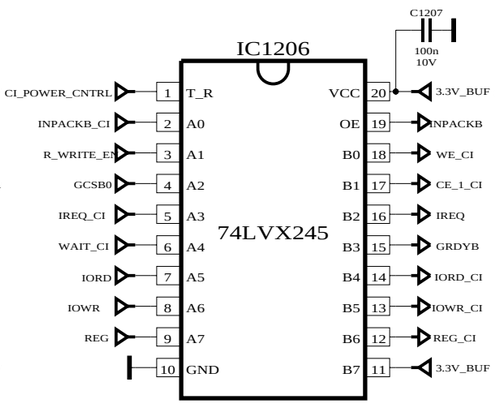


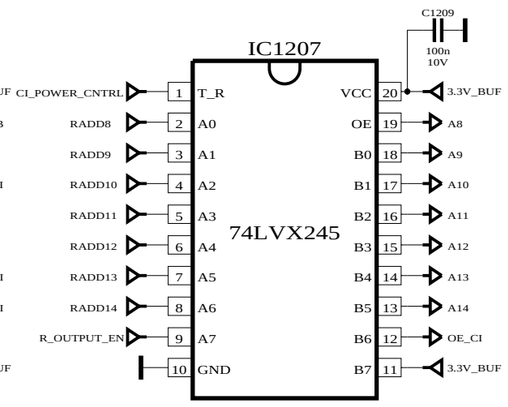


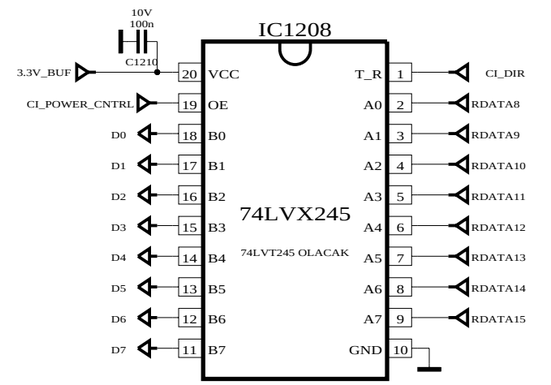


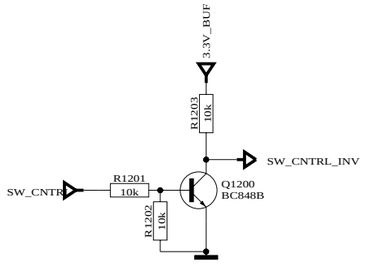


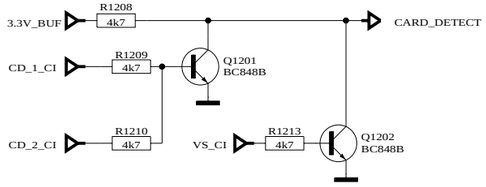


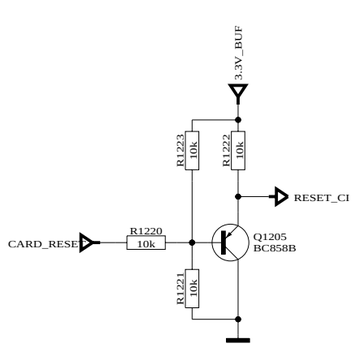


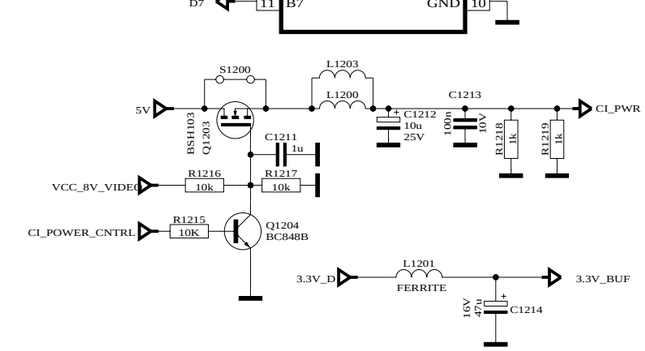


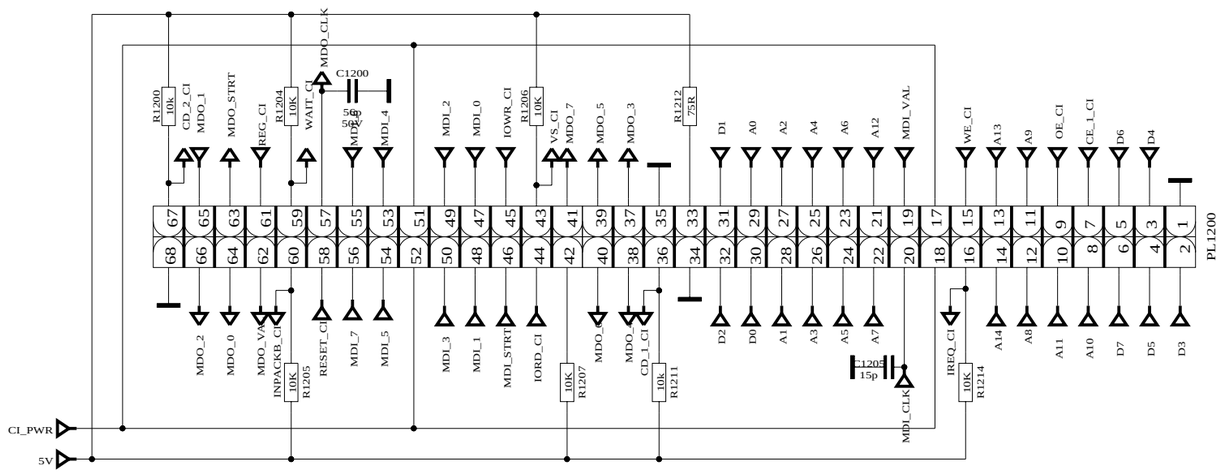












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Date	Author
17.04.2007	SADIK SEHIT ISMAIL YILMAZLAR ONUR KORHAN SAYI

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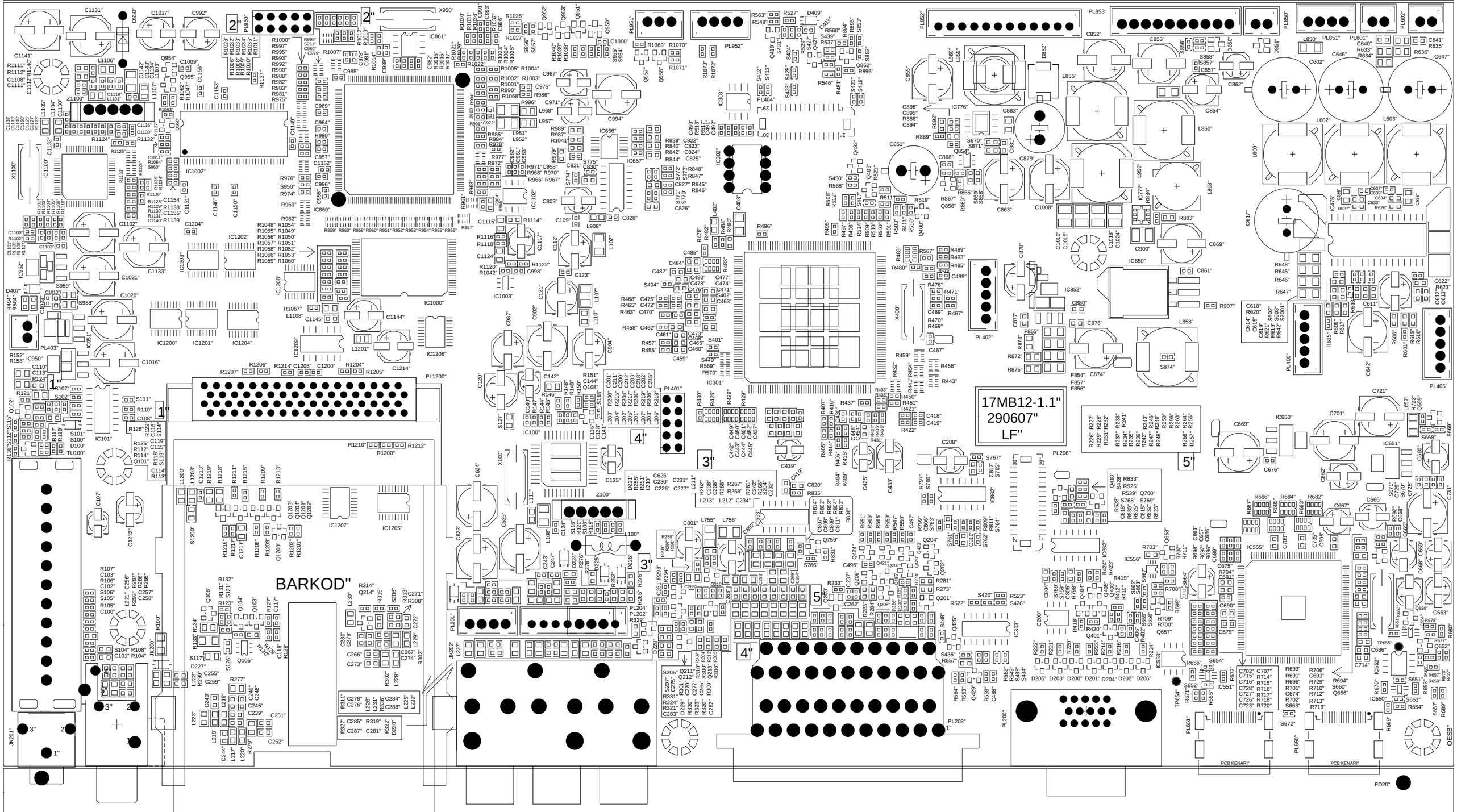

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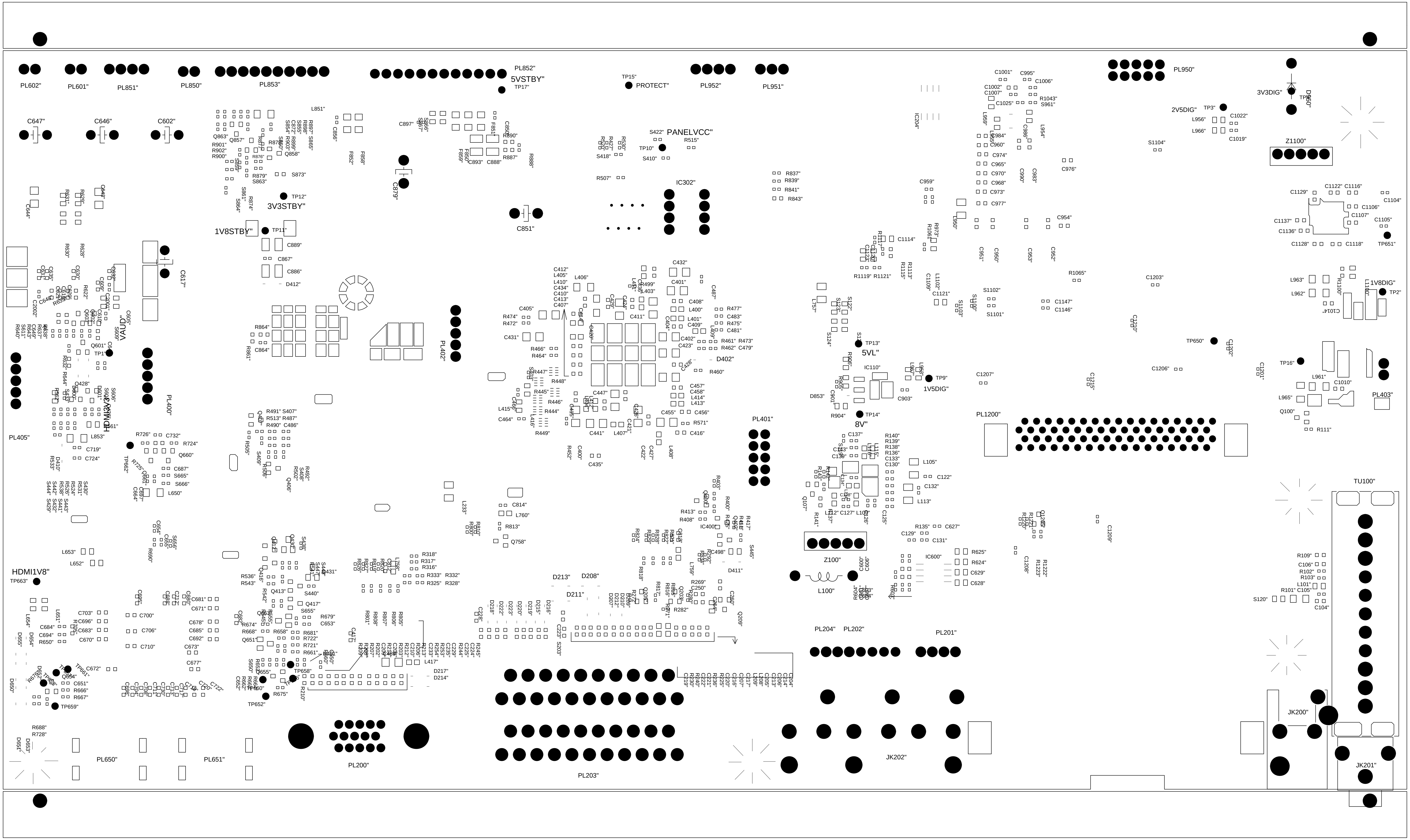

PL602"
PL601"
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PL950"
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Z1100"
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C602"
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PL405"
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PL1200"
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TP2"
TP650"
TP651"
TP16"
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TU100"
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TP663"
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