		Short Message	Message Menu	Short Message
		Remaining Rental Time Inquiry	Remaining Time	Inquires about the remaining rental time
		AUX A	AUX A	AUX A
		AUX B	AUX B	AUX B
2	HOOK/ MONI	Hook Check		This option should be selected when palm microphone is used.
		Monitor		This option should be selected when desktop microphone is used.
3	Selector Knob	Selector Knob		For controlling the volume as well as selecting the channel and zone

Circuit Description

Frequency Configuration

The receiver utilizes double conversion superheterodyne. The first IF is 49.95MHz and the second IF is 450KHz. The first local oscillator signal is supplied by the PLL circuit, while the second local oscillator signal (49.5MHz) is generated from the frequenc MHz The PLL circuit generates the frequencies required for transmission. See Fig.1.

Frequency Range VHF: 136MHz-174MHz

UHF: 400MHz-470MHz;

Receiver Circuit

The receiver section configuration is shown as Fig. 1.

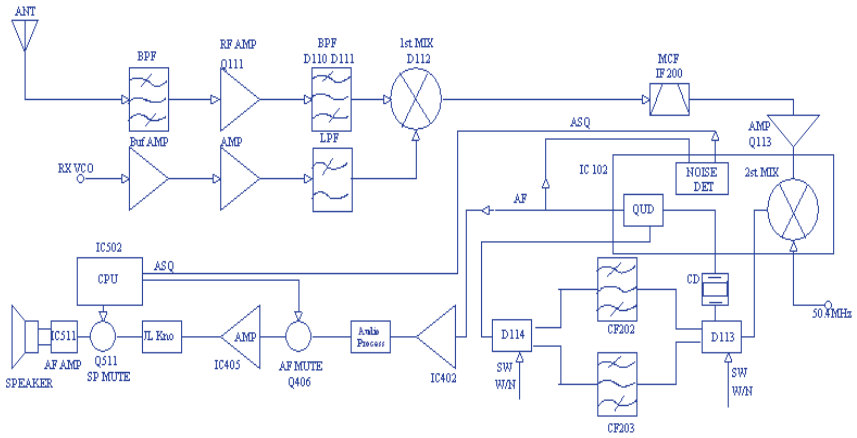


Fig. 1 Receiver Circuit

2.1 RF AMP BPF

The circuit consists of front-stage BPF, RF amplifier (Q111) and final-stage BPF (D110 and D111). The

bandpass frequency range varies with the radio models. The BPF is used to eliminate unwanted signals and let only wanted signals go to the mixer.

2.2 First Mixer Circuit

The signal output from RF AMP&BPF is mixed with the first LO signal from the PLL circuit at the mixer (D112) to generate a 49.95MHz first IF signal. Then the first IF signal will feed through a crystal filter (IF200) to further remove spurious signals.

2.3 IF Amplifier Circuit

After amplified at Q113, the first IF signal enters IC102 (TA31136FN), where it is mixed with the second LO signal (50.4MHz) to generate a 450KHz second IF signal. Then the second IF signal feeds through a pair of ceramic filters (N: CF202; W: CF203) where unwanted signals are removed. Finally the signal goes to the frequency discriminating circuit of IC102 to output audio signal from Pin 9.

2.4 Audio Amplifier Circuit

The audio signal from IC102 is amplified and filtered at IC402, and then amplified again at IC401 (the received signaling is separated and sent to CPU for decoding). Then the signal passes through Q406 (AF MUTE), and enters IC405 for further amplification. After the volume is controlled at K301 on the control panel, and SP MUTE is controlled at Q511, the signal feeds into IC511 to output audio signal to drive the speaker.

2.5 Squelch Control Circuit

One flow of the audio signals from IC102 feeds into IC102 (from Pin8) for amplification, filtering and rectification, and then a SQL level is derived. Then the SQL level is sent to CPU (IC502) for comparison with the reference level to generate a level which controls AFMUTE and SP MUTE. The level controls Q406 and Q511 to open or close the audio channel.

Transmitter Circuit

The transmitter circuit is composed of MIC circuit, modulation circuit, RF driver, final-stage power amplifier circuit and APC circuit.

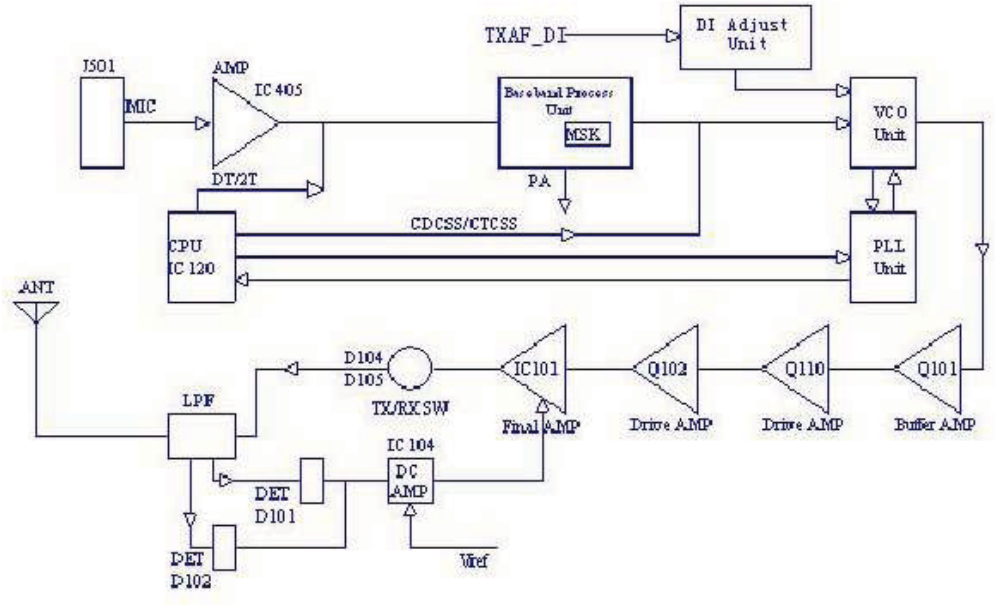


Fig. 2 Transmitter Circuit

3.1 MIC and Modulation Circuit

The audio signal from MIC is amplified at IC405, and further amplified, pre-emphasized and encoded at IC 401. It is added with signaling before going to VCO for modulation.

The DI modulation circuit is composed of IC407 and peripheral circuits (see the figure above). The signal goes to the DI modulation circuit via the TXAF_DI port, and then goes to the VCO unit. The signal amplitude can be adjusted manually via VR802, allowing accurate modulation of DI without any distortion. This circuit can serve as input or output port for GPS and encryption, promoting the radio functions to be further expanded.

3.2 RF Driver and Final-stage PA Circuit

TX-RF signal output from Q703 in the VCO circuit is amplified at Q101, driver PA Q110 and Q109, and final-stage PA IC101. The signal passes through LPF and goes to the antenna for transmission.

3.3 APC Circuit

The circuit is used to keep output power at a constant preset value. In this circuit, D101 and D102 convert the signal from detector into DC voltage, which is then compared with the reference voltage from CPU in IC104 to output a DC voltage. The DC voltage controls gate electrode of IC101, so as to control the output power.

■ 4. PLL Circuit

PLL circuit supplies frequency to receive the first LO signal and TX signal. The circuit consists of TX

frequency oscillator (Q701), RX frequency oscillator (Q702), buffer amplifier (Q703), RF amplifier (Q102), PLL IC (IC801), LPF and TX/RX VCO switch (Q704/Q706).

In TX mode, IC502 provides the frequency data to and activates PLL IC. Meanwhile, Q704 is turned on to activate TX VCO. The output signal is amplified by Q703 and Q102. Then PLL IC divides the signal into 2.5KHz, 5KHz or 6.25KHz. And phase of it is compared with that of reference frequencies 2.5KHz , 5KHz or 6.25KHz from the 16.8MHz crystal oscillator. The crystal oscillator has operating frequency of 16.8MHz and frequency stability of 2.5ppm. The frequency control voltage output from the phase comparator passes through LPF (Q802 and Q803), and then is sent to TX VCO. In the meantime, TX modulation signal is passed to TX VCO for frequency modulation.

The working principle of RX mode is similar to that of TX mode.

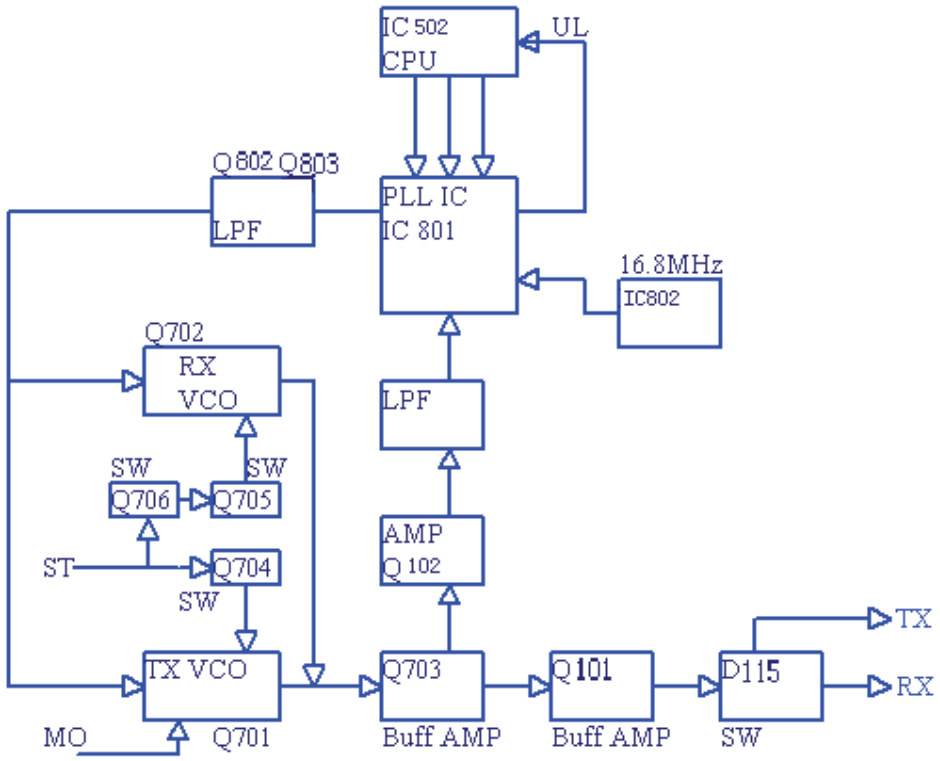


Fig. 3 PLL Circuit

■ 5. Control Circuit

The circuit comprises CPU circuit, reset circuit and power control circuit.

5.1 CPU

IC120 (CPU) operates at 9.8304MHz, and controls EEPROM (IC501), RX circuit, TX circuit, control circuit and display circuit, as well as data transmission with peripheral equipment.

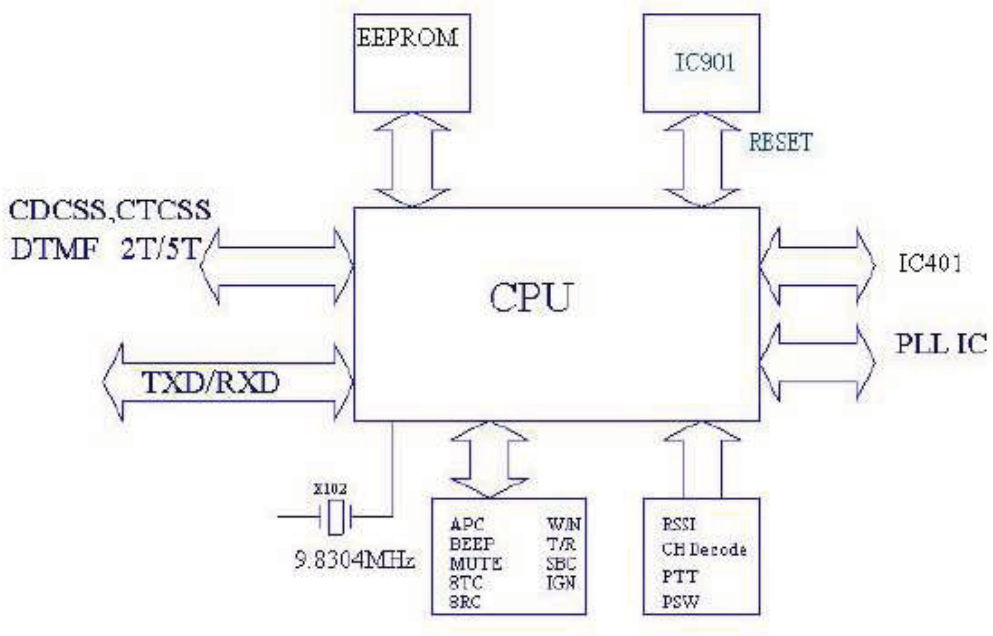


Fig. 4 Control Circuit

5.2 Reset Circuit

The reset circuit consists of a reset IC (CN813LESA) and peripheral circuits. When a breakdown occurs due to change of external voltage, the CPU would automatically reboot your radio through the reset IC (IC901).

5.3 Power Control Circuit

Power supply of the radio is derived from +B. D515 and D516 are diodes for over-voltage protection. The power can be switched on or off via software (see the figure below):

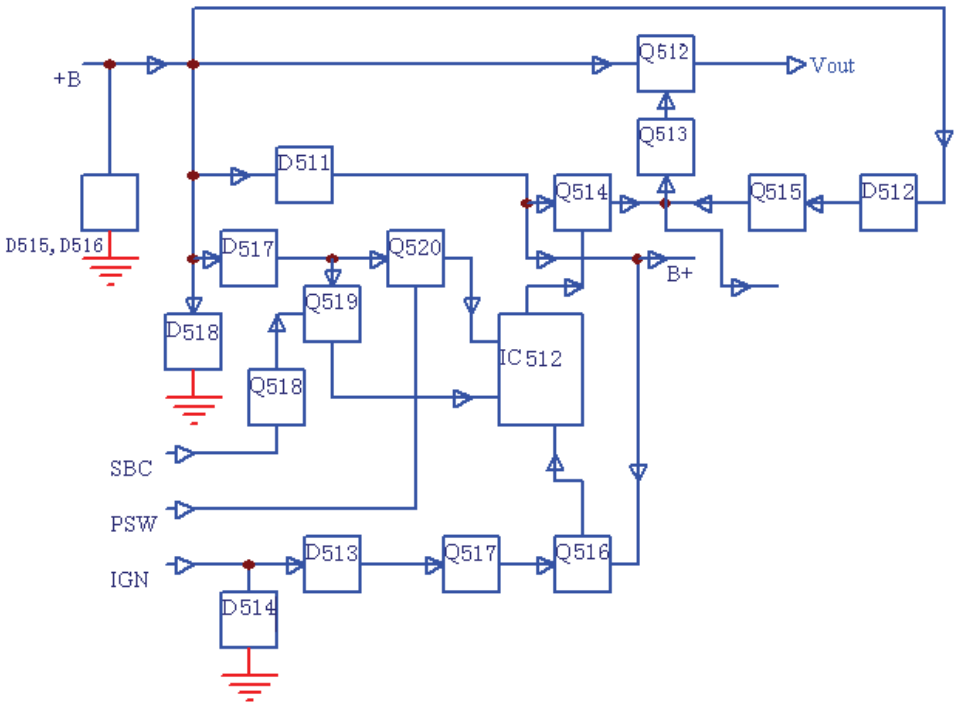
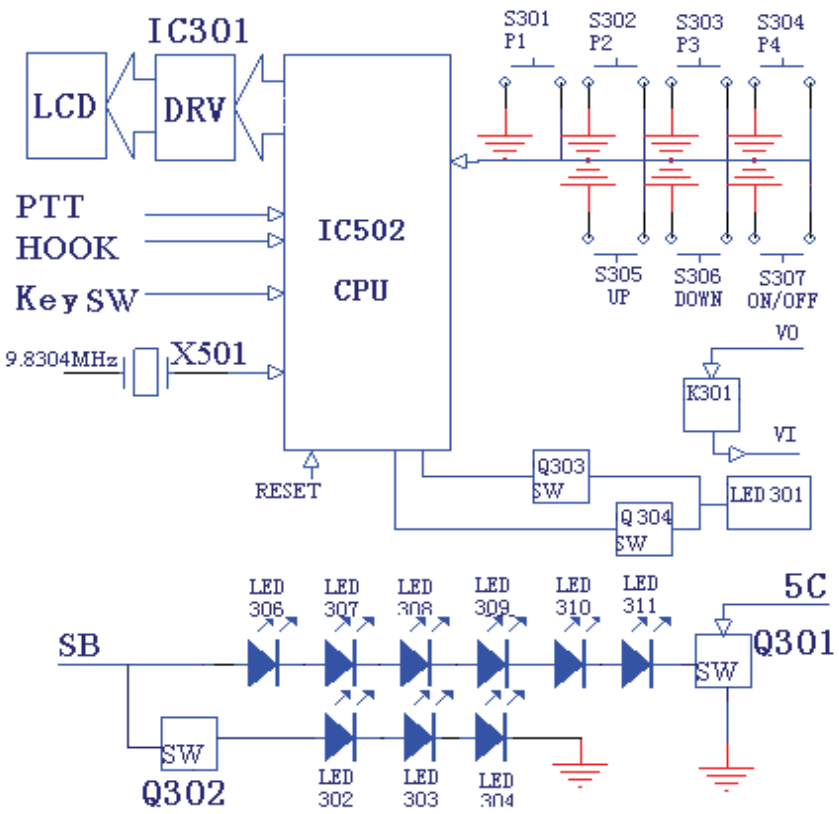


Fig. 5 Power Supply Circuit

Vout supplies power for IC601, IC602 and IC803, which generate 8V, 5V and 3.3V voltage respectively to supply the whole circuit.

6. Display Circuit

Display circuit comprises CPU (IC502), LCD, LED and other components. Application can be operated manually through programmable keys **P1**-**P4** as well as ▲ and ▼. Channel information is displayed on the 14-segment display.



Semiconductor Data

1. Positive voltage regulator: TA7805F (Power Unit IC602), TA7808S (Power Unit IC601)
2. EEPROM: CAT24C256WI 256K CATALYST (CPU Unit IC501)

2-1. Pin Function

Pin Function

Pin No.	Name	I/O	Function
1～3	A0～A2	I	Address input
4	GND		Ground
5	SDA	I/O	Serial data input/output
6	SCL	I	Serial clock input
7	Write Protect		Write protect
8	VCC		+5V