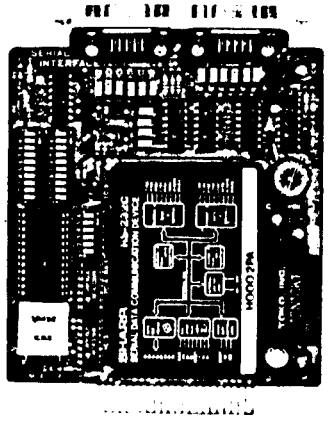
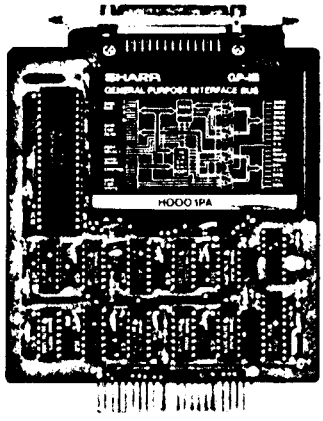
SHARP SERVICE MANUAL

PDSMX81013-MZ



RS-232C
Serial Interface Card
MZ-8BI03



GP-IB Interface Card
MZ-8BI04

FEATURES

MZ-8BI03

- A serial interface card for MZ-80B, capable of converting parallel 8-bits data to serial data to transmit and receive.
- Integrating two channels of interface conforming to RS-232C (JIS-C-6361) into one board.
- Employment of Z-80SIO/0, one of Z-80 family, enabling to deal with various interrupts.

MZ-8BI04

- GP-IB interface card for MZ-80B, capable of freely controlling measuring instrument groups conforming to IEC standards IEEE-488 and enabling low cost, automatic measuring system.
- Capable of programming by improved BASIC.

SHARP CORPORATION

Contents

MZ-8BI03 SPECIFICATIONS

Item	Specifications
Communication method	Asynchronous
Standard	In compliance with EIA RS-232C
Control LSI	Z-80SIO/0
Number of channels	2 (Channel A and Channel B)
20mA current loop	Changeover is allowed for one channel (Channel B)
Baud rate	Can be set independently for the two channels (Manual setting using switch)
Number of baud rates	10 (75, 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600 baud)
Character length	5, 6, 7 or 8 bits (Selection by software)
Parity bit	Odd, none or even
Stop bit	1, 1½ or 2
Mode	Either terminal mode or modem mode can be selected for each channel (through the use of jumper chip).
Interrupt	Z-80 vector interrupt can be used.
Port address	Manual setting with switch
Operating temperature	0°C ~ 50°C
Storage temperature	−25°C ~ 80°C

(Note) The above-mentioned specifications may be changed in the future for improvement of the product.

MZ-8BI03 GENERAL INFORMATION

■ Introduction

There are two methods of data communication between computer and external equipment: 8-bit parallel and bit serial.

The serial interface card MZ-8BI03 (hereinafter referred to as "interface card") permits data communication by the bit serial method. This interface card is manufactured in accordance with EIA RS-232C (the Electronic Industries Association RS-232C), and used for data communication with other equipment having interface based on RS-232C.

■ Functions of this interface card

The interface card has the following functions.

1. One card has two channels, each of which is capable of transmitting/receiving data independently.
2. One of the ten baud rates can be selected by operating the switch on the card. Baud rates can be set independently for the two channels.
3. Output connector signals to external equipment can be in either terminal mode or modem mode through the operation of the jumper chip.
4. This interface card can be used as 20mA current loop for one channel.

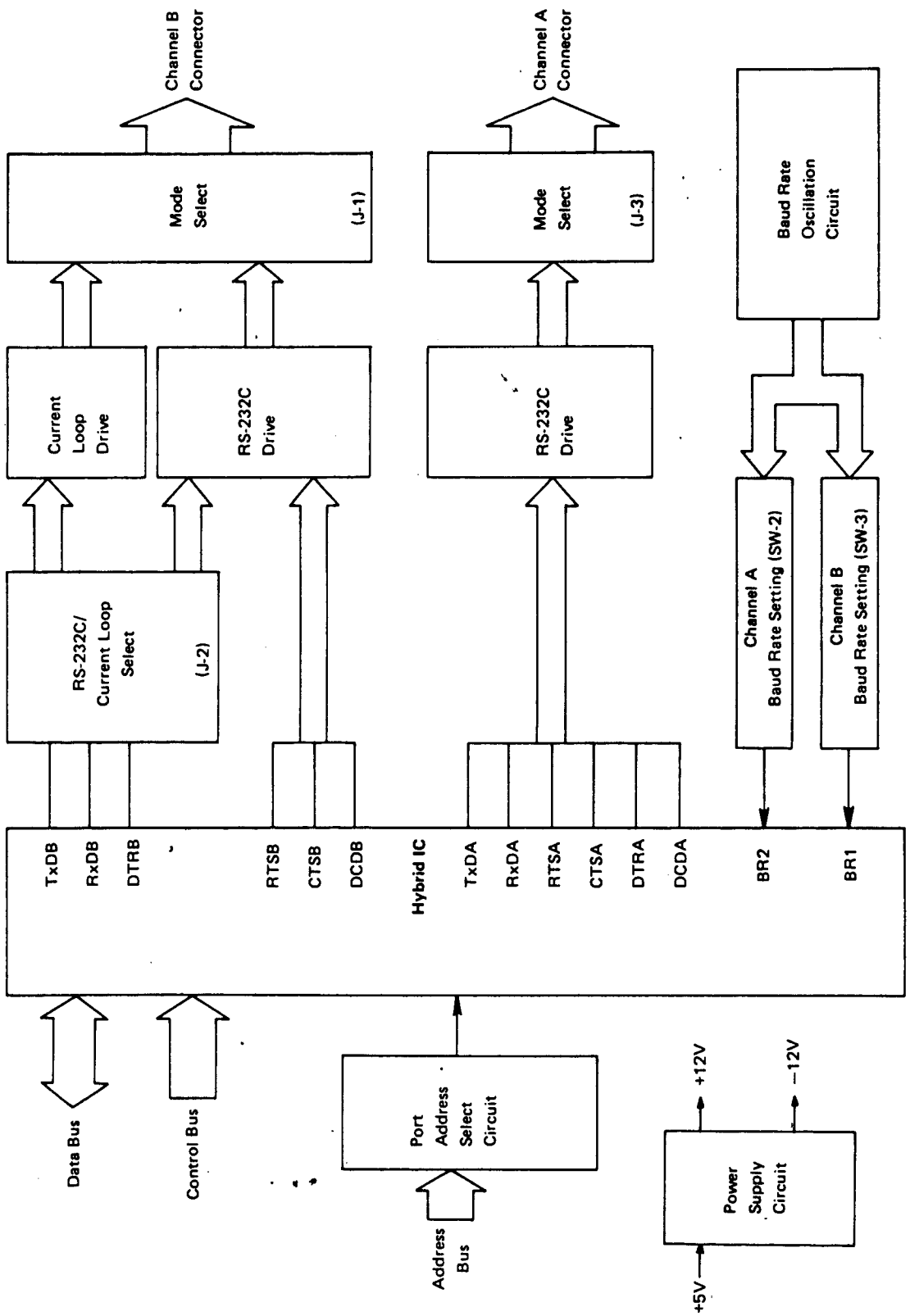
■ Applications

Equipped with the above-mentioned functions, the interface card has a variety of applications. Some applications of this very versatile serial interface card are shown below.

1. Data communication between computers on telephone line via acoustic couplers
2. Printer
3. Plotter
4. Digitizer
5. Color display
6. Card reader
7. Magnetic tape equipment

MZ-8BI03 DESCRIPTION OF CIRCUIT

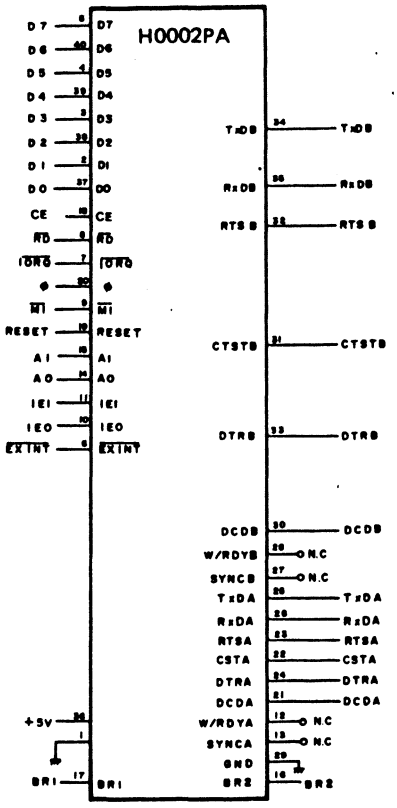
■ Circuit Diagram



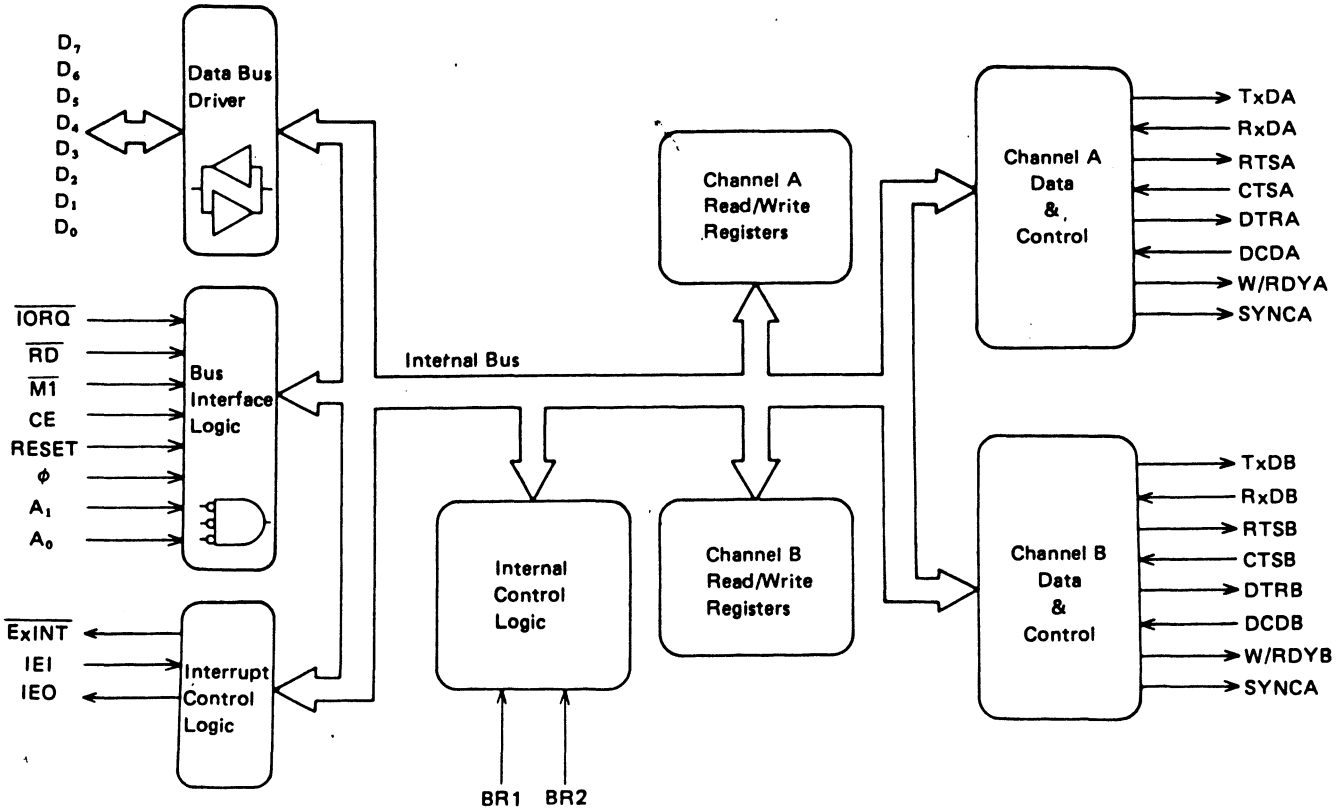
■ Construction of Circuit

The serial interface card consists of the following six blocks.

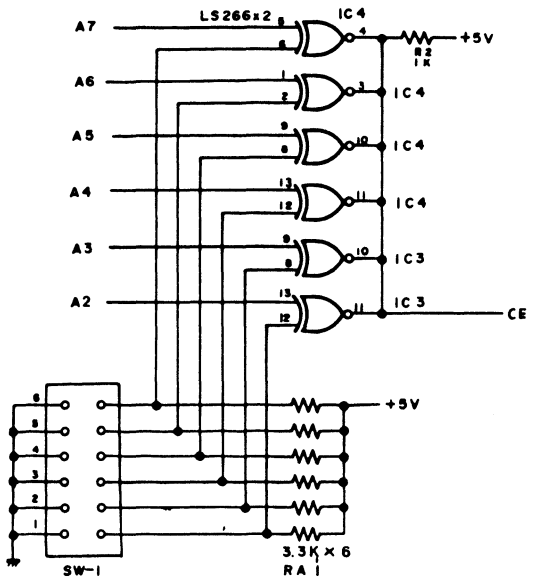
- Block 1 Hybrid IC circuit



- Block Diagram of Hybrid IC

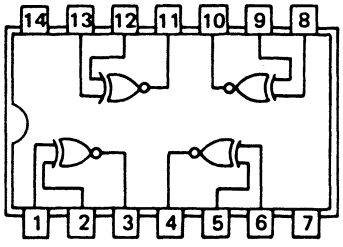


- Block 2 Port Address Select Circuit

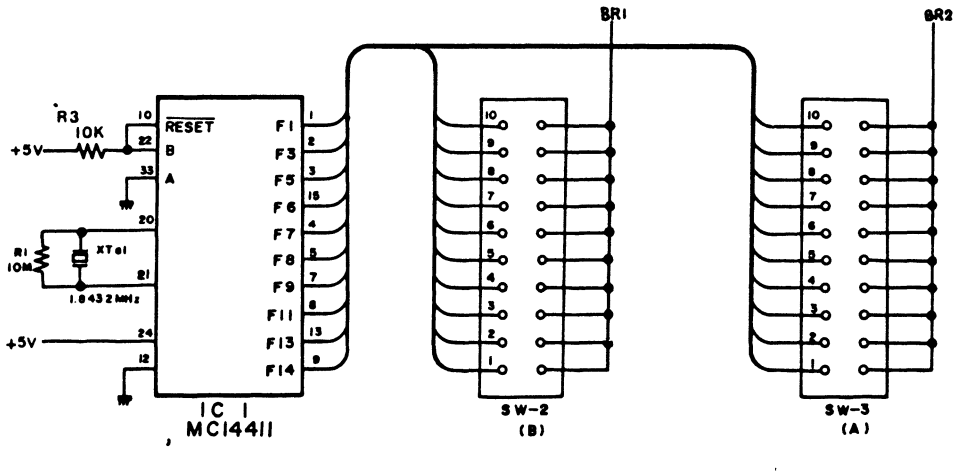


- IC3, 4 RH-iX0190PAZZ
(SN74LS266N)

PIN ASSIGNMENT
(Top View)

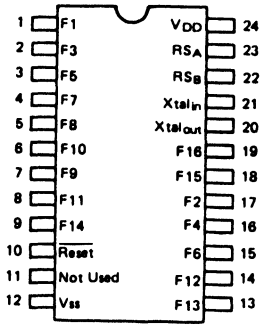


- Block 3 Baud Rate Oscillation and Setting Circuit

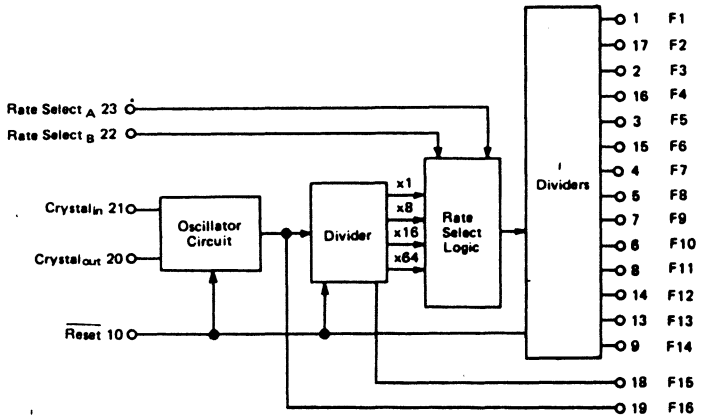


- IC1 RH-iX0297PAZZ (MC14411)

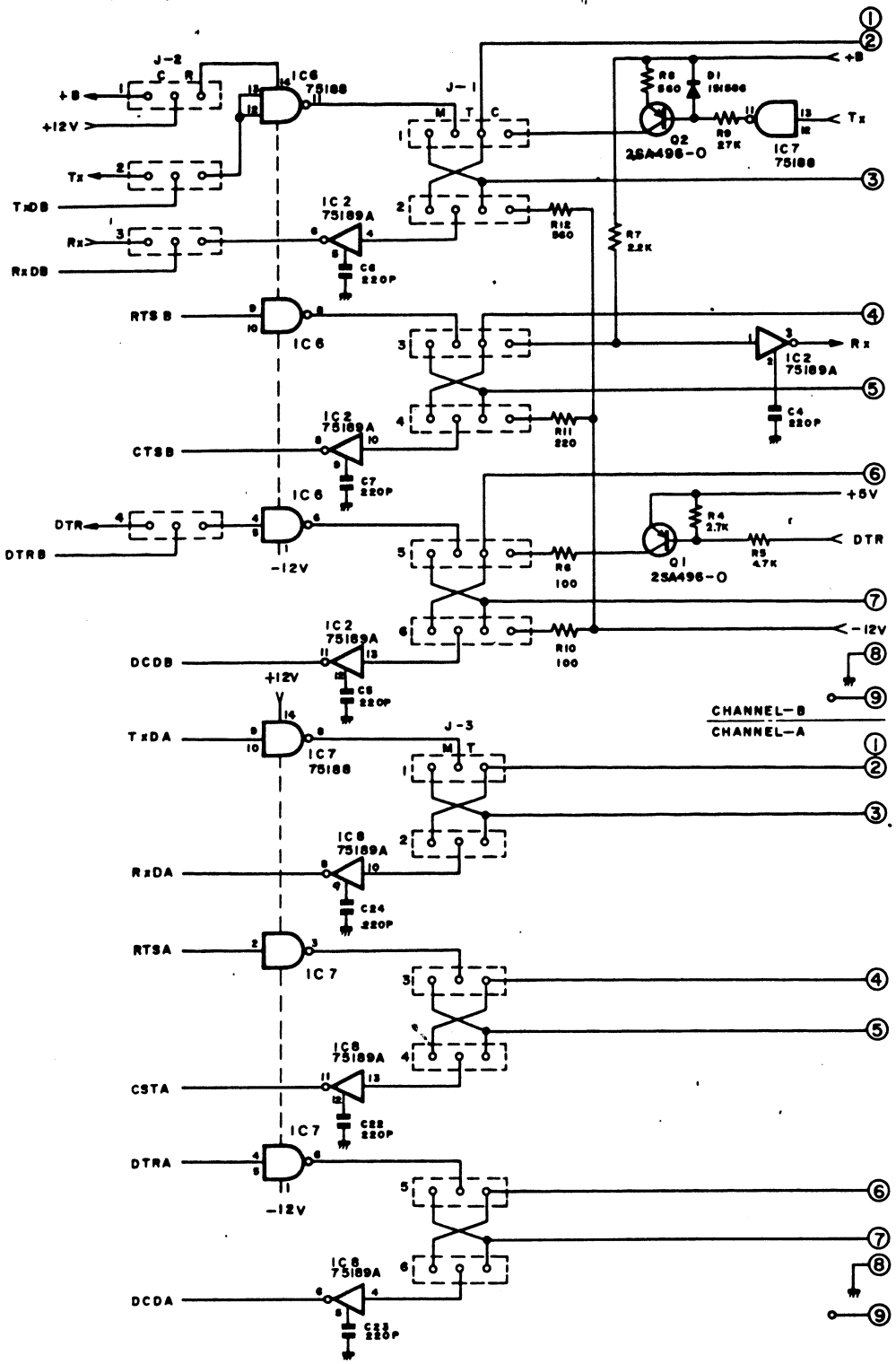
PIN ASSIGNMENT
(Top View)



BLOCK DIAGRAM

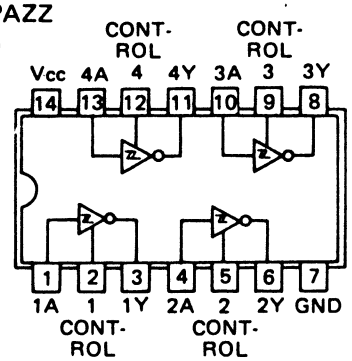


- Block 4 Driver, Jumper, Switch and Connector Circuit



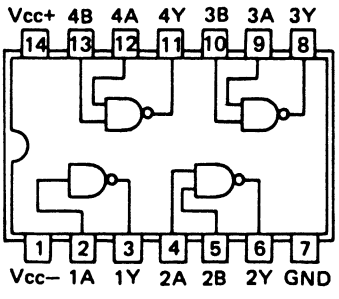
- IC2, 8 RH-iX0305PAZZ (SN75189A)

PIN ASSIGNMENT (Top View)

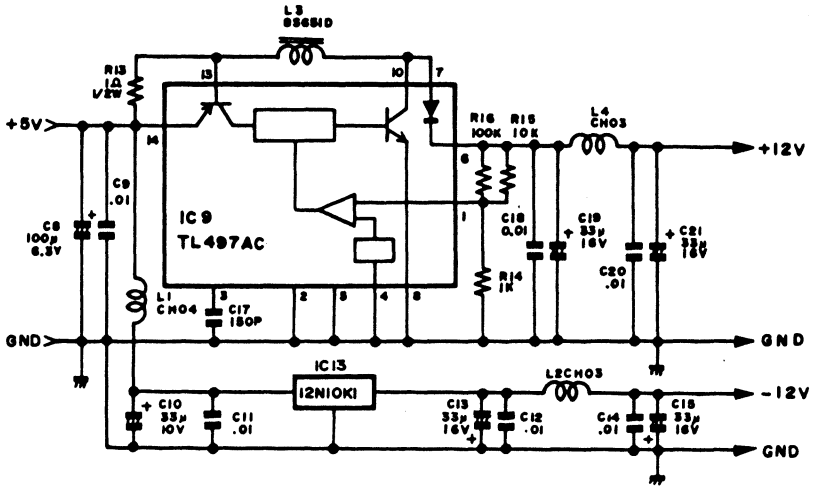


- IC7, 8 RH-iX0085PAZZ (SN75188N)

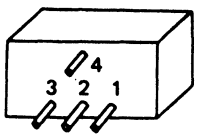
PIN ASSIGNMENT (Top View)



- Block 5 Power Supply Circuit



- IC13 DUNTK0064PAZZ
  (12N10K1)



1. GND
2. V in
3. V out
4. N.C

- Block 6 Bus Interface Circuit

MZ-8BI03 TROUBLESHOOTING

The serial interface card consists of six blocks and, if each block functions normally, a faulty operation is caused by an external factor (Ex: program, the counterpart machine, etc.).

■ Circuit Blocks and Check of Behavior

Block	Circuit	Behavior
1	Hybrid	Z-80SIO is built in and test the function by the test program.
2	Port address selector	Check if an address code set by SW-1 (DIP switch) is output. If the output does not agree, wired-or output is a low level.
3	Borate oscillation and setting	Check if MC14411 is outputting. Frequencies are as follows: F1 = 153.6 KHz　F8 = 9,600 Hz F3 = 76.8 KHz　F9 = 4,800 Hz F5 = 38.4 KHz　F11 = 2,400 Hz F6 = 28.8 KHz　F13 = 1,758.8 Hz F7 = 19.2 KHz　F14 = 1,200 Hz Be sure that two or more switches of SW-2 and SW-3 (DIP switch) are not turned on. Tolerable deviations are ±0.1% for each frequency. In measurement, consider that the waveform of MC14411 varies according to the load capacity because MC14411 is CMOS.
4	Drivers, jumpers, switches and connectors	Check the status of input signal. ● Output of 75188 / Input of 75189 } High level: −10V to −12V, Low level: 10V to 12V ● Input of 75188 / Output of 75189 } TTL level (High: 0V to 0.8V, Low: 2.5V to 5V) ● If reset, the output terminal of the hybrid IC is in the high level (high level of TTL level).
5	Power supply ● 5V line ● +12V line ● −12V line	Be sure that the voltage is +5V ±5%. Be sure that the output of DC-DC converter is: +12V ±10%, −12V ±10%
6	Bus interface	Since there is no circuit part, examine if the signal is input to the board normally. The hybrid IC is not actuated unless the clock signal is applied to the ϕ terminal of the hybrid IC.

■ Faulty symptoms and connected circuit blocks

Circuit blocks						Faulty symptoms and probable causes
1	2	3	4	5	6	
O	O			O	O	• Transmission buffer is not empty. • Control does not return from the transmission routine in test program run. (Causes) • Hybrid IC doesn't function normally. • ϕ clock is inoperative. • Wrong port address selection. • Abnormal 5V power supply. • Other.
		O	O	O		• Error message is generated from Z-80SIO (parity error, overrun error, framing error, etc.) (Causes) • Wrong borate setting. • Abnormal borate oscillator. • Wrong jumper setting (J-1, J-2 and J-3) • Abnormal +12V or −12V line. • Faulty connector. • Faulty counterpart machine. • Other.
O		O	O	O		• Signal is not input. • Control does not return from input routine in test program run. (Causes) • Wrong borate setting. • Abnormal borate oscillator. • Abnormal +12V or −12V line. • Wrong jumper setting (J-1, J-2 and J-3) • Faulty connector. • Faulty operation of hybrid IC. • Faulty counterpart machine. • Faulty driver IC. • Other.

"O" shows a related circuit.

Circuit blocks						Faulty symptoms and probable causes
1	2	3	4	5	6	
			O	O		• +12V or −12V line deviates over ±10%. (Causes) • Faulty TL497AC. • Faulty 12N10K1. • Short circuited load. • Short circuited electrolytic capacitor. • Other.
O		O				Borate oscillator does not output. (Causes) • Faulty MC14411. • Faulty crystal. • Two or more dip switches (SW-2, SW-3) turned on. • Faulty borate clock input circuit of hybrid IC. • Other.

"O" shows a related circuit.

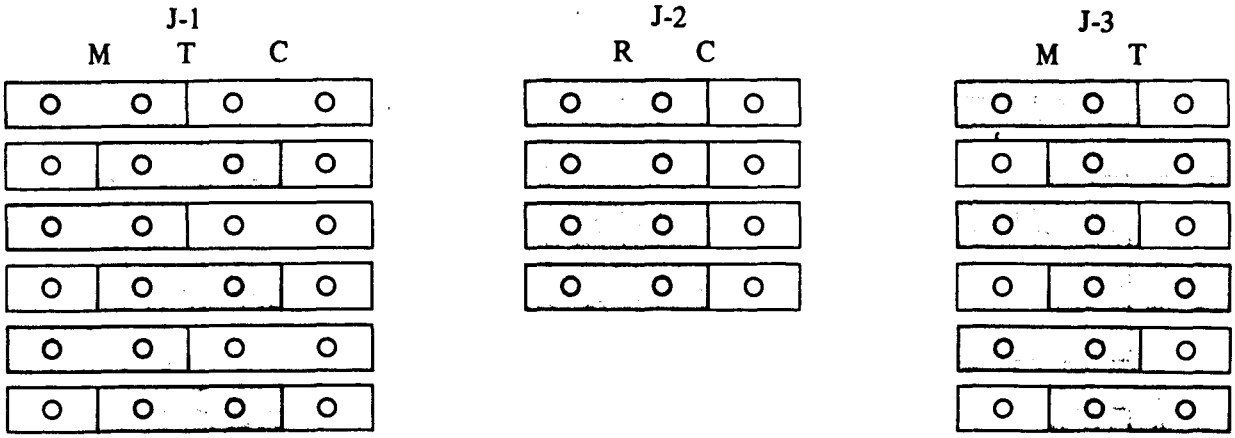
MZ-8BI03 TEST PROGRAM

■ Self-diagnosis program

Let μs consider a program for self-diagnosis of this interface card and assume that data are transmitted from Channel A are received by Channel A. For channel B, similar communication system shall be adopted. Self-diagnosis of the interface card can be made by examining whether the receive data and transmit data are the same at the time of transmission/receiving.

■ Setting jumper blocks on the card

For the self-diagnosis as mentioned above, set the jumper blocks on the card as follows.



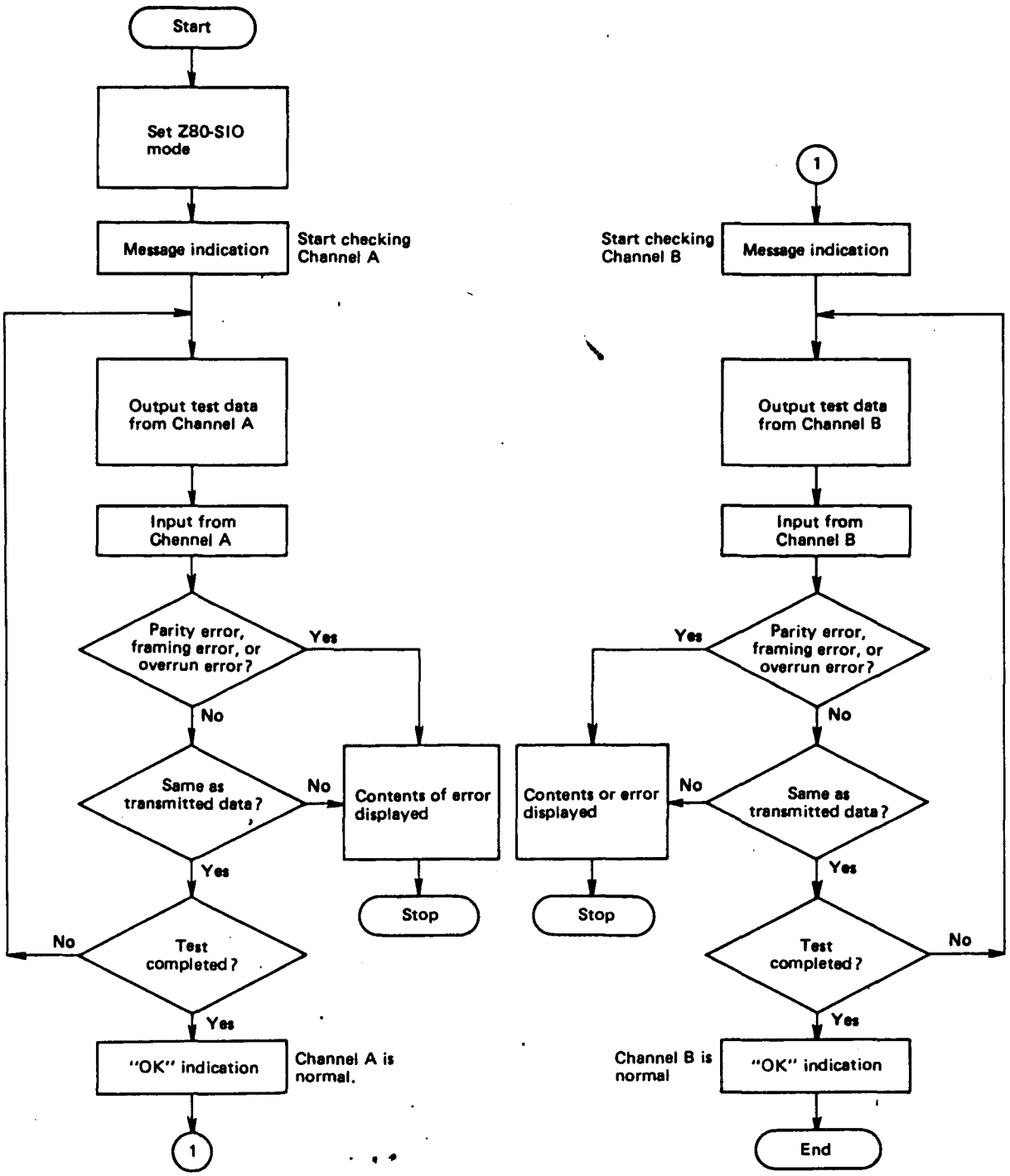
Since port addresses B0H, B1H, B2H and B3H are used in the program, set the switch SW-1 in the following (factory setting).

Switch segment	6	5	4	3	2	1
Switch position	OFF	ON	OFF	OFF	ON	ON

Set the switch for baud rate setting as desired. After setting each mode, install the card in MZ-80B. On this occasion, signal cable needs not to be connected.

■ Flow Chart of Self-diagnosis Program

Start testing Channel A. Stop the program when an error occurs. If Channel A is found normal, test Channel B then.



■ Program by BASIC language

Now, let us draw up the program described in the above-mentioned flow chart, using †BASIC languages. The program list is shown later.

In the BASIC program, the routine to control the interface card is composed of machine language. The machine language data are written into the memory by POKE statement and the routine is called by USR statement. The routine is made by programming statement Nos. 1000 through 1990.

Statement Nos. 1080 ~ 1160. . . . . .Parameters

Clock rate	: x 16
Stop bit	: 2 bits
Parity	: Present
Odd/even of parity	: Even
Transmit/receive character	: 8 bits
Auto enable	: Set

Statement Nos. 1180 ~ 1370. . . . . .Mode setting routine.
Statement Nos. 1550 ~ 1610. . . . . .Channel A input routine.
Input data are stored in Address CHAR.
Error flags are stored in Address INER@.
Statement Nos. 1630 ~ 1740. . . . . .Channel B input routine.
Input data are stored in Address CAHR.
Error flags are stored in Address INER@.
Statement Nos. 1780 ~ 1840. . . . . .Channel A output routine.
Transmit data are stored in Address CHAR.
Statement Nos. 1860 ~ 1930. . . . . .Channel B output routine.
Transmit data are stored in Address CHAR.
Statement Nos. 1950 ~ 1990. . . . . .Writes machine language data in the memory.

†BASIC Version: SB-6510, SB-5510

by BASIC language

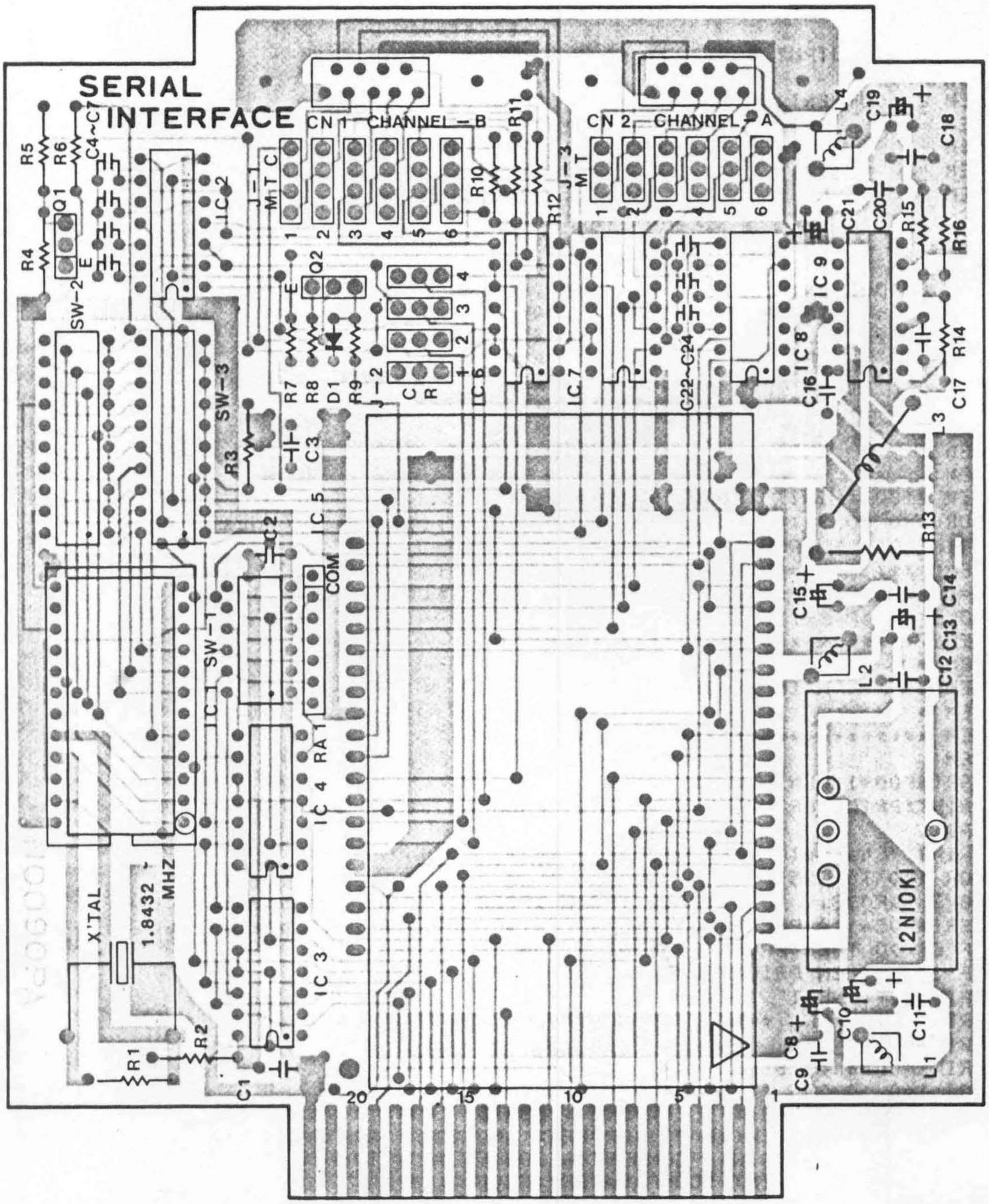
```
1000 REM ************************************************
1010 REM *                                              *
1020 REM *  Serial I/F Subroutine for MZ-8BI03 on MZ-80B  *
1025 REM *            ( by BASIC interpreter )           *
1030 REM *                                              *
1040 REM ************************************************
1050 REM *
1060 REM ***  Parameter  ***
1070 REM *
1080 REM WR      DEFB    18H         :DATA 18
1090 REM         DEFB    10H         :DATA 10
1100 REM         DEFB    10H         :DATA 10
1110 REM WR4     DEFB    4           :DATA 04
1120 REM         DEFB    4FH         :DATA 4F
1130 REM WR5     DEFB    5           :DATA 05
1140 REM         DEFB    EAH         :DATA EA
1150 REM WR3     DEFB    3           :DATA 03
1160 REM         DEFB    E0H         :DATA E0
1170 REM
1180 REM MODE    ENT                 ; [ adr.=$F009 ]
1190 REM         LD      C,CHACT     :DATA 0E,B1
1200 REM         LD      B,9         :DATA 06,09
1210 REM         LD      HL,WR       :DATA 21,00,F0
1220 REM         OTIR                :DATA ED,B3
1230 REM         LD      C,CHBCT     :DATA 0E,B3
1240 REM         LD      B,9         :DATA 06,09
1250 REM         LD      HL,WR       :DATA 21,00,F0
1260 REM         OTIR                :DATA ED,B3
1270 REM         LD      A,3         :DATA 3E,03
1280 REM         OUT     (CHACT),A   :DATA D3,B1
1290 REM         LD      A,(WR3+1)   :DATA 3A,08,F0
1300 REM         OR      1           :DATA F6,01
1310 REM         OUT     (CHACT),A   :DATA D3,B1
1320 REM         LD      A,3         :DATA 3E,03
1330 REM         OUT     (CHBCT),A   :DATA D3,B3
1340 REM         LD      A,(WR3+1)   :DATA 3A,08,F0
1350 REM         OR      1           :DATA F6,01
1360 REM         OUT     (CHBCT),A   :DATA D3,B3
1370 REM         RET                 :DATA C9
1380 REM
1390 REM ***  INPUT ROUTINE  ***
1400 REM     (INER@)=0   NO ERROR
1410 REM        bit4=1   PARITY ERROR
1420 REM        bit5=1   OVERRUN ERROR
1430 REM        bit6=1   FRAMING ERROR
1440 REM
1450 REM INER@   ENT                 ; [ adr.=$F032 ]
1460 REM         DEFS    1           :DATA 00
1470 REM CHAR    ENT                 ; [ adr.=$F033 ]
1480 REM         DEFS    1           :DATA 00
1490 REM
1500 REM CHAIN   ENT                 ; [ adr.=$F034 ]
1510 REM         IN A,(CHACT)        :DATA DB,B1
1520 REM         RRCA                :DATA 0F
1530 REM         JR      NC,CHAIN    :DATA 30,FB
1540 REM         LD      A,1         :DATA 3E,01
1550 REM         OUT     (CHACT),A   :DATA D3,B1
1560 REM         IN      A,(CHACT)   :DATA DB,B1
1570 REM         AND     70H         :DATA E6,70
1580 REM         LD      (INER@),A   :DATA 32,32,F0
1590 REM         IN      A,(CHADT)   :DATA DB,B0
1600 REM         LD      (CHAR),A    :DATA 32,33,F0
1610 REM         RET                 :DATA C9
```

```
1630 REM CHBIN  ENT                 ; [ adr.=$F04A ]
1640 REM        IN A,(CHBCT)        :DATA DB,B3
1650 REM        RRCA                :DATA 0F
1660 REM        JR      NC,CHBIN    :DATA 30,FB
1670 REM        LD      A,1         :DATA 3E,01
1680 REM        OUT     (CHBCT),A   :DATA D3,B3
1690 REM        IN      A,(CHBCT)   :DATA DB,B3
1700 REM        AND     70H         :DATA E6,70
1710 REM        LD      (INER@),A   :DATA 32,32,F0
1720 REM        IN      A,(CHBDT)   :DATA DB,B2
1730 REM        LD      (CHAR),A    :DATA 32,33,F0
1740 REM        RET                 :DATA C9
1750 REM
1760 REM ***  OUTPUT ROUTINE  ***
1770 REM
1780 REM CHAOUT ENT                 ; [ adr.=$F060 ]
1790 REM        IN      A,(CHACT)   :DATA DB,B1
1800 REM        BIT     2,A         :DATA CB,57
1810 REM        JR      Z,CHAOUT    :DATA 28,FA
1820 REM        LD      A,(CHAR)    :DATA 3A,33,F0
1830 REM        OUT     (CHADT),A   :DATA D3,B0
1840 REM        RET                 :DATA C9
1850 REM
1860 REM CHBOUT ENT                 ; [ adr.=$F06C ]
1870 REM        IN      A,(CHBCT)   :DATA DB,B3
1880 REM        BIT     2,A         :DATA CB,57
1890 REM        JR      Z,CHBOUT    :DATA 28,FA
1900 REM        LD      A,(CHAR)    :DATA 3A,33,F0
1910 REM        OUT     (CHBDT),A   :DATA D3,B2
1920 REM        RET                 :DATA C9
1930 REM        END                 :DATA END
1940 REM
1950 DIM X(30):LIMIT $F000 :P=15*4096
1960 FOR J=0 TO 9:X(J)=J:NEXT:FOR J=0 TO 5:X(17+J)=J+10:NEXT
1965 PRINT"SIF SUBROUTIN LOADING"
1970 READ X$:IF X$="END" THEN 3000
1980 J=16*X(ASC(MID$(X$,1,1))-48)+X(ASC(MID$(X$,2,1))-48)
1990 POKE P,J:P=P+1:GOTO 1970
3000 REM  ***************************
3010 REM *                         *
3020 REM *      MAIN PROGRAM       *
3030 REM *                         *
3040 REM ***************************
3050 REM
3060 USR($F009):REM   mode set
3070 PRINT:PRINT:PRINT "*****  TEST PROGRAM  (Serial I/F MZ-8BI03)  ***** "
3080 PRINT
3090 PRINT "Channel A TEST "
3100 FOR I=0 TO 255
3110 POKE  $F033,I :USR($F060):POKE $F033,0  : REM channel-A output
3120 USR($F034):A=PEEK($F033):ER=PEEK($F032) : REM channel-A input
3130 IF ER<>0 THEN PRINT"COMMUNICATION ER = ";ER:STOP
3140 IF I<>A THEN PRINT"COMPARA ER":STOP
3150 PRINT".";:NEXT
3160 PRINT"***  OK  ***"
3170 PRINT
3180 PRINT"Channel B TEST "
3190 FOR I=0 TO 255
3200 POKE $F033,I:USR($F06C):POKE $F033,0    : REM channel-B output
3210 USR($F04A):A=PEEK($F033):ER=PEEK($F032) : REM channel-B input
3220 IF ER<>0 THEN PRINT "COMMUNICATION ER = ";ER:STOP
3230 IF I<>A THEN PRINT "COMPARA ER":STOP
3240 PRINT"#";:NEXT
3250 PRINT"***  OK  ***"
3260 END
```

MZ-8BI03 PWB AND CIRCUIT DIAGRAM

Notes: The printed wiring board circuit diagram are subject to change without prior notice.

■ **Printed Wiring Board**



■ Circuit Diagram

A: PARTS SIDE

B		A
+5V	1	+5V
D3	2	D2
D4	3	D1
D5	4	D0
D6	5	GND
D7	6	A15
φ	7	A14
$\overline{M1}$	8	A13
$\overline{WR}$	9	A12
$\overline{RD}$	10	A11
$\overline{IORQ}$	11	A10
$\overline{MREQ}$	12	A9
GND	13	A8
$\overline{HALT}$	14	A7
IEI	15	A6
IEO	16	A5
RESET	17	A4
$\overline{ExRESET}$	18	A3
$\overline{ExINT}$	12	A2
$\overline{ExWAIT}$	20	A1
$\overline{NMI}$	21	A0
GND	22	GND

SW. NO	BAUD RATE
10	9600
9	4800
8	2400
7	1800
6	1200
5	600
4	300
3	150
2	110
1	75

MZ-8B103

MZ-8BI04 SPECIFICATIONS

Item	Specifications
Interface standard	In accordance with IEC Standard/TC66.
Interface funcion	Functions executable in MZ-80B version-up BASIC language.

Function	Subset	Description
SH	SH1	All functions
AH	AH1	All functions
T	T_6	Basic talker Serial poll Cancellation of talker by MLA
L	L_4	Basic listener Cancellation of listener by MTA
C	C_1	System controller
	C_2	IFC transmit, controller in charge
	C_3	REN transmit
	C_4	Response to SRQ
	C_6	Interface message transmit Controller receive Controller pass Controll pass to itself Parallel poll
SR	SR0	No function
RL	RL0	No function
PP	PP0	No function
DT	DT0	No function
DC	DC0	No function

Output connector	(Male type) connector in compliance with IEC Standard
Operating temperature	5°C ~ 35°C
Storage temperature	0°C ~ 50°C
Power source	DC 5V (supplied from MZ-80B)

Reference

The following specifications are "reference" specifications, since difference is caused by cable quality, connector connection, noise and other environmental conditions.

1. Number of instruments per system — 15 max. including MZ-80B
2. Full length of cable per system — 20m or less
   However, length per instrument shall be about 2m. If the number of instruments exceed 11 in one system, cables of 2m or less shall be used between instruments so that the full length will be 20m or less.

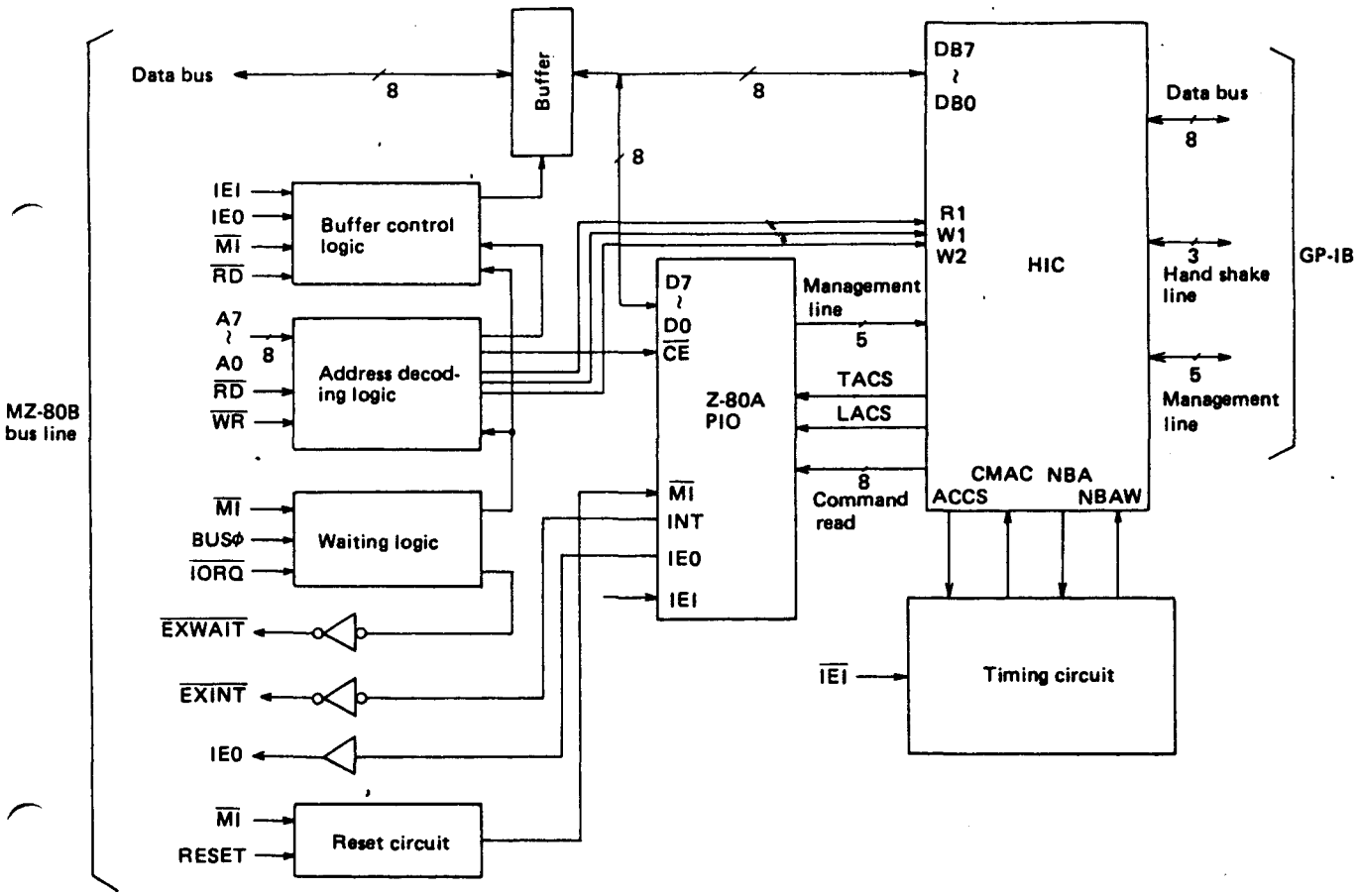
(Note) The above-mentioned specifications may be changed in the future for improvement of the product.

MZ-8BI04 DESCRIPTION OF CIRCUIT

▪ Block Diagram

This interface circuit consists of a hybrid IC (H0001PA) for GP-IB, Z-80APIO and various logics to connect them to the extension I/O of MZ-80B.

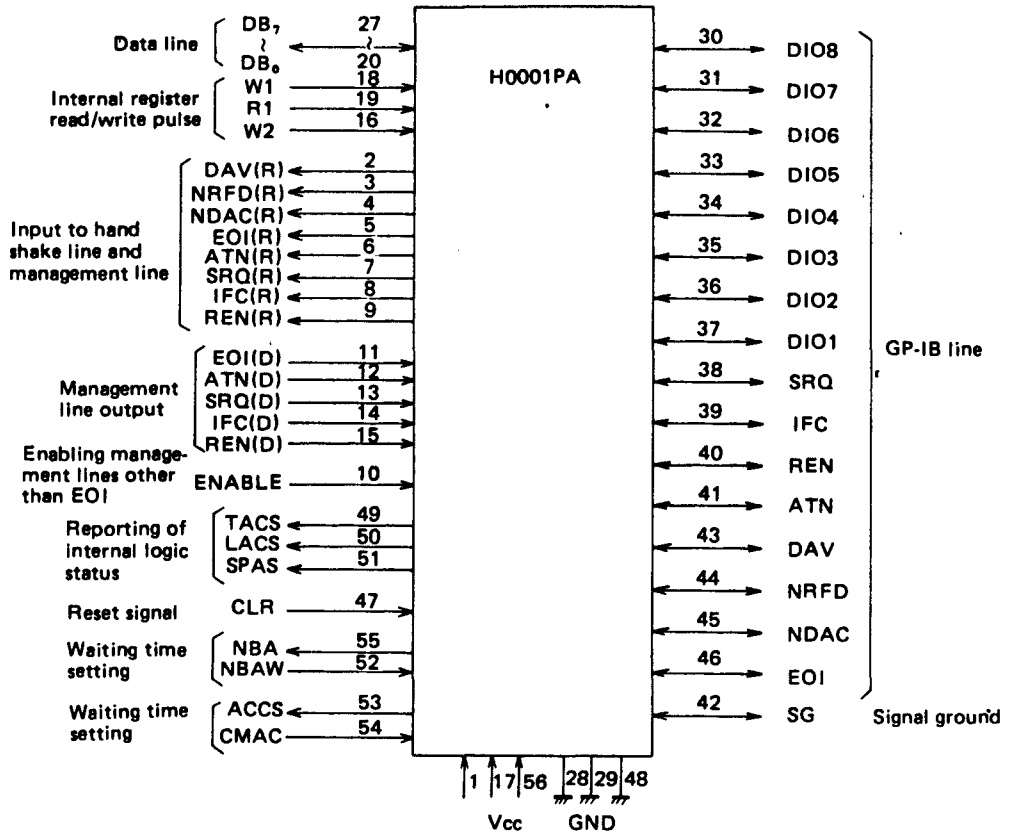
Some of included logics are a waiting logic and a data buffer control logic so that the mode 2 interrupt of Z-80A can be utilized by Z-80APIO.



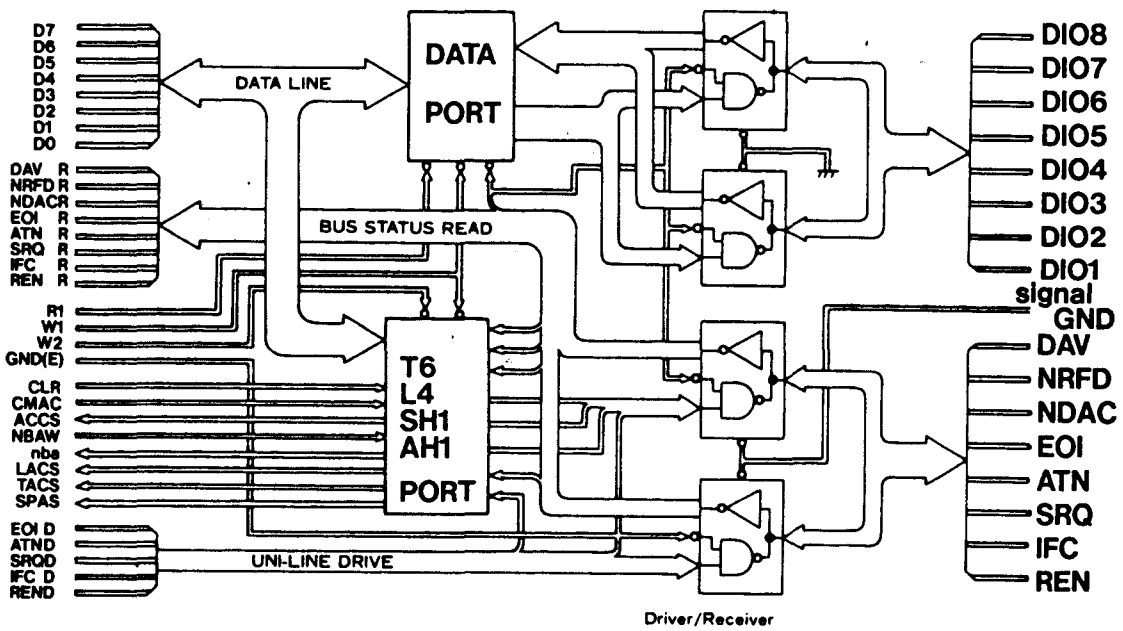
MZ-8BI04 Block Diagram

■ Description of Hybrid IC RMPTH0001PAZZ for GP-IB

The hybrid IC mounted on the GP-IB interface MZ-8BI04 of MZ-80B integrates the hand shake logic, bus driver/receiver, etc. which are the proper circuits of GP-IB circuit, into one package. By connecting this HIC (hybrid IC) to the I/O ports of an ordinary microcomputer, the functions of T_6, L_4, SH_1 and AH_1 and the inputting and outputting of the management line and data line are enabled.



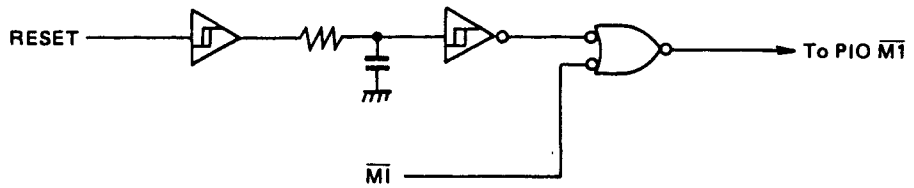
- **Block Diagram of Hybrid IC**



■ Description of Each Circuit

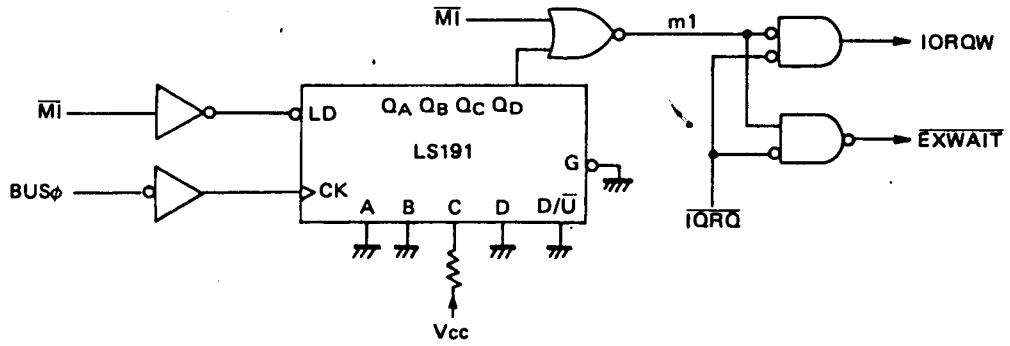
Each circuit will be described. The logic diagrams used for description are simplified schemata of logic.

1. Reset Circuit



The circuit is intended to reset PIO by the RESET signal from MZ-80B CPU board. Z-80APIO is reset when $\overline{MI}$ terminal is active for 2 clock cycles or over providing that both $\overline{RD}$ and $\overline{IORQ}$ signals are not active. The RC circiut in the diagram is a low pass filter provided for preventing faulty operation due to noise.

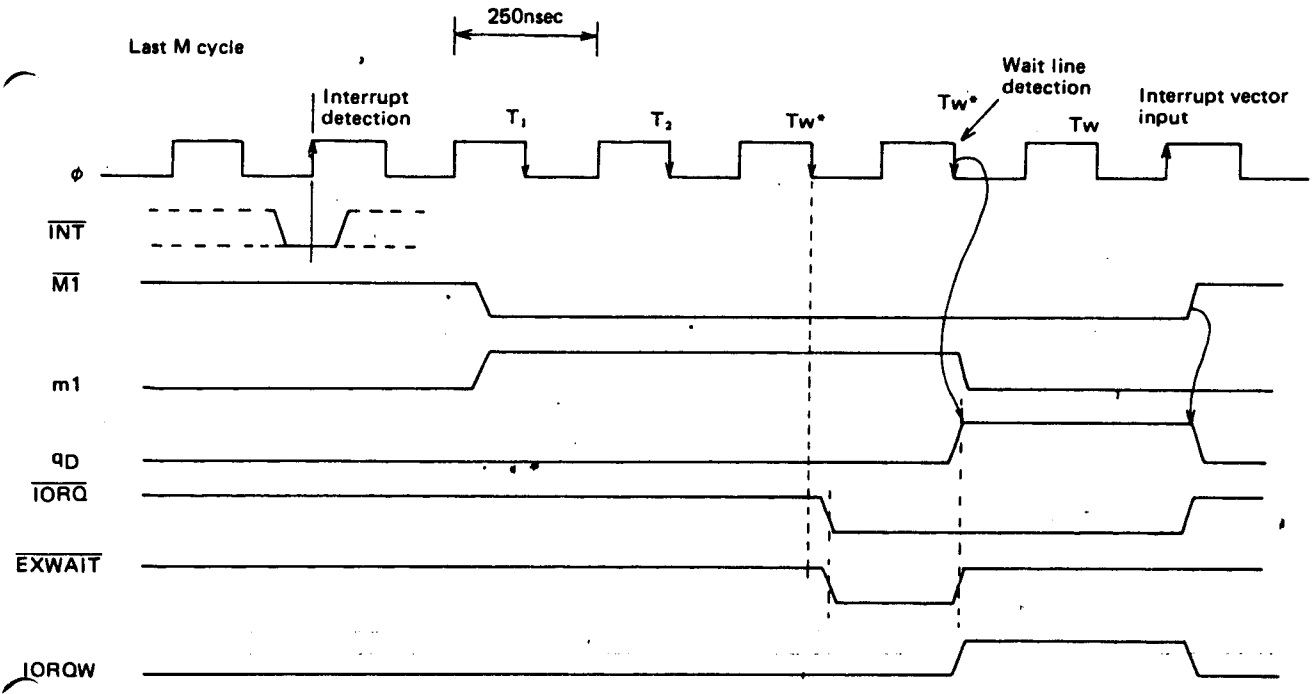
2. Waiting Circuit



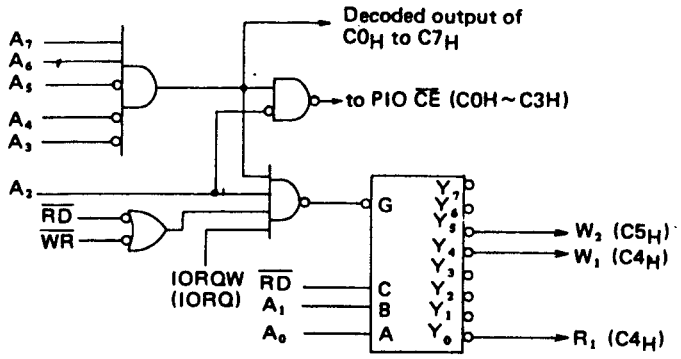
The waiting circuit corrects the timing of the interrupt vector transmitting from PIO to CPU in the interrupt acknowledge cycle. Thus, $\overline{IORQW}$ develops a signal of reversed $\overline{IORQ}$ and $\overline{EXWAIT}$ doesn't develop pulse in other cycle than the interrupt acknowledge cycle.

This waiting circuit does not correct the timing of the daisy chain. With the delay of the daisy chain, IEO look ahead is carried out on the extension I/O interface of MZ-80B.

The timing chart in the interrupt acknowledge cycle is illustrated below.

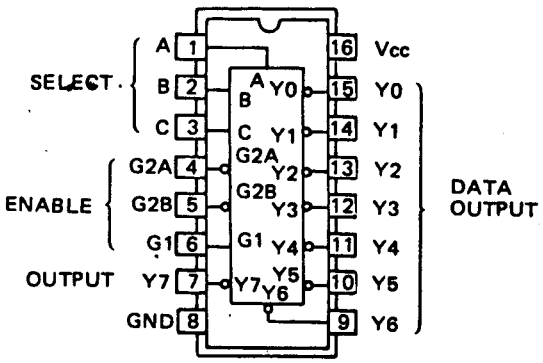


3. Address Decoding Logic



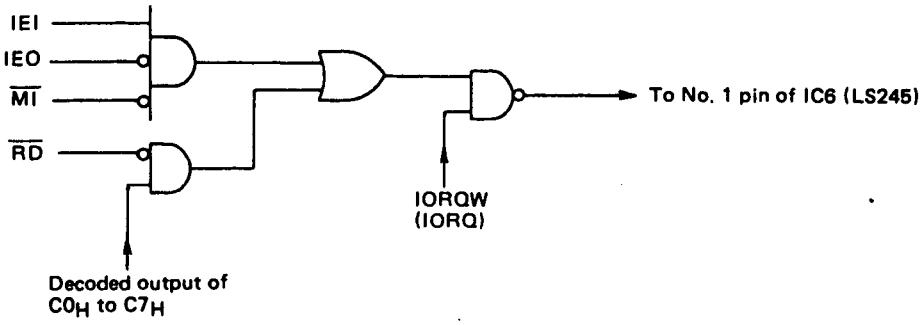
• IC9 RH-iX0303PAZZ
SN74LS138N

Pin Assignment (Top View)



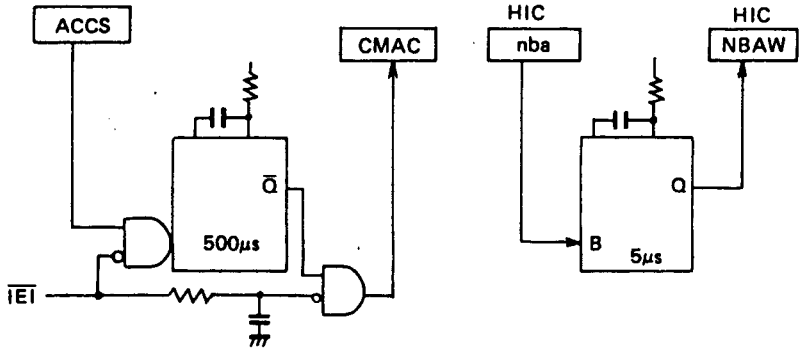
The address decoding logic forms $\overline{CE}$ signal of PIO and R_1, W_1 and W_2 signals of HIC from the signals A_0 to A_7, $\overline{RD}$, $\overline{WR}$ and IOPQW. The decoded output of $C0_H$ to $C7_H$ is used by the data buffer control logic.

4. Data Buffer Control Logic



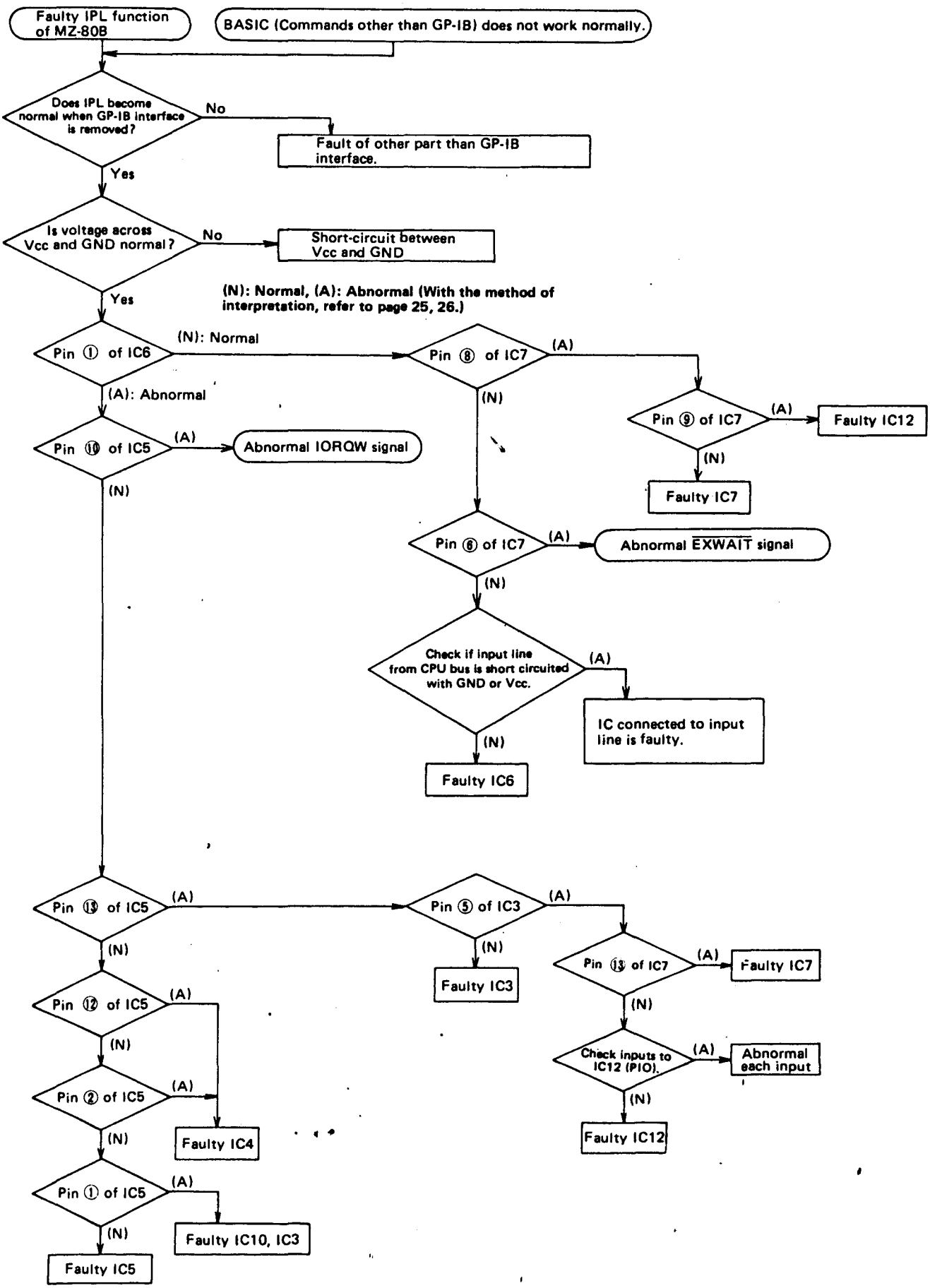
The data buffer control logic regulates the buffer connecting the CPU data bus line and the bus lines of PIO and HIC. CPU reads data when the No. 1 pin of IC6 is in low level. CPU reads data when the IO addresses of $C0_H$ to $C7_H$ are input to CPU and CPU reads the interrupt vector from PIO in the mode 2 interrupt acknowledge cycle.

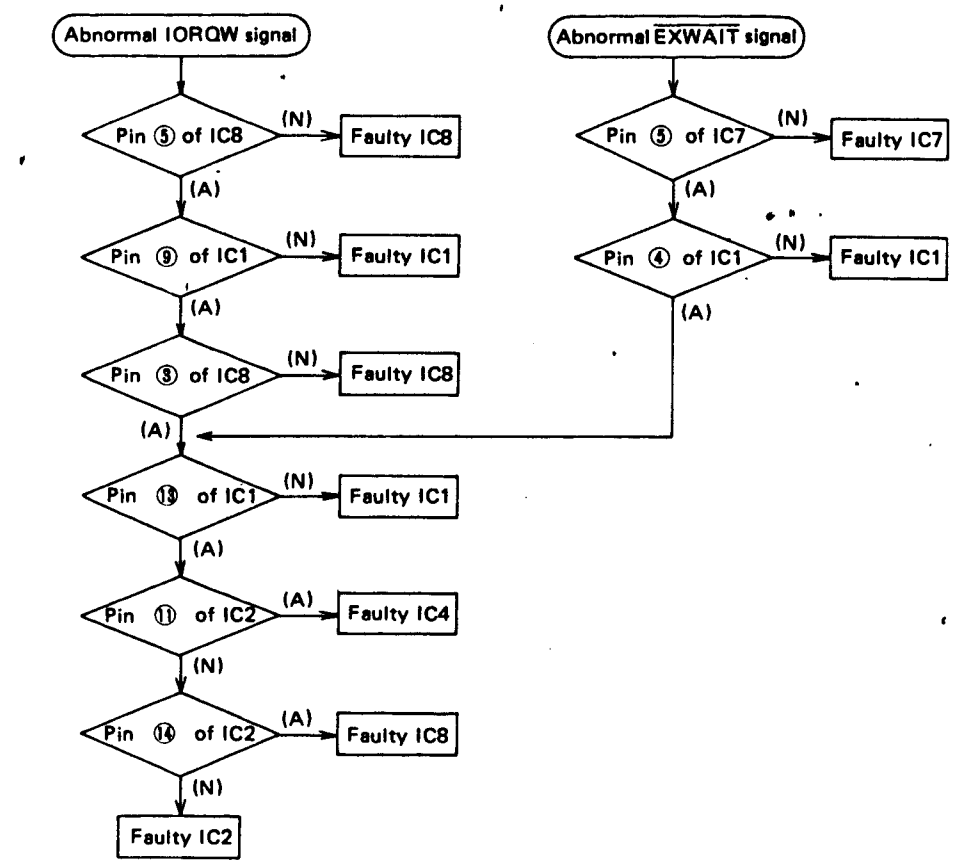
5. Timing Circuit

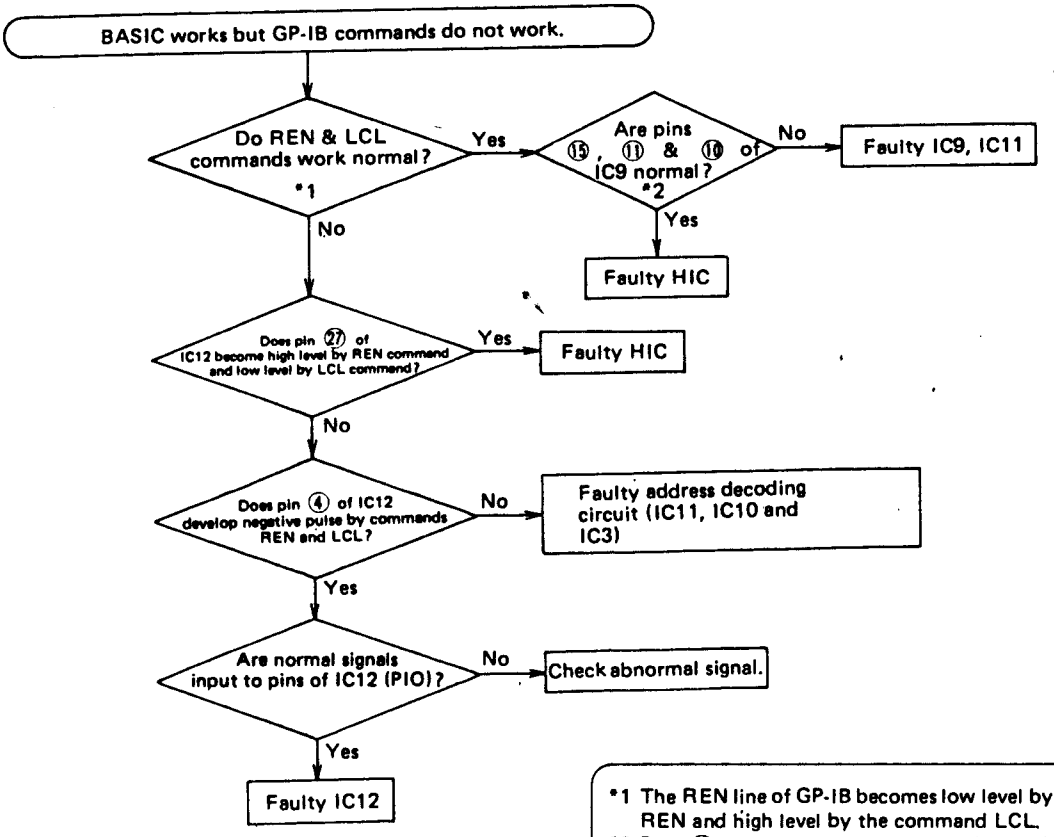


The timing circuit forms pulses of about 500μsec. and about 5μsec. 500μsec. determines the time for receiving one command when the ATN signal is received in the slave mode and 5μsec. determines the time from transmitting data on to the GP-IB data bus to outputting DAV. It is so designed that 500μsec. pulse is not generated until IEI becomes high level, by considering the disposition of ATN by interrupt.

MZ-8BI04 TROUBLESHOOTING







*1 The REN line of GP-IB becomes low level by the command REN and high level by the command LCL.

*2 Pin ⑮ : outputs negative pulse by reading I/O address C4H (196).
Pin ⑪ : outputs negative pulse by writing on to I/O address C4H (196).
Pin ⑩ : outputs negative pulse by writing on to I/O address C5H (197).

■ Methods of Interpreting Whether Normal or Abnormal

Each terminal is normal if it is in the following status in the "READY" condition after run by BASIC.

Pin No. of IC	Normal condition	
IC1 ④	Negative pulse	Same as $\overline{MI}$ (CPU bus)
IC1 ⑨	Positive pulse	Reversed $\overline{MI}$ (CPU bus)
IC1 ⑬	Constant L level	
IC2 ⑪	Positive pulse	Reversed $\overline{MI}$ (CPU bus)
IC2 ⑭	Reversed busϕ	
IC3 ⑤	Constant H level	
IC5 ①	Positive pulse	(Turns H level when XXC0H to XXC7H are transmitted address bus.)
IC5 ②	Positive pulse	Reversed $\overline{RD}$ (CPU bus)
IC5 ⑩	Positive pulse	Reversed $\overline{IORQ}$ (CPU bus)
IC5 ⑫	Positive pulse	Reversed $\overline{MI}$ (CPU bus)
IC5 ⑬	Constant L level	
IC6 ①	Constant H level	
IC7 ⑤	Constant H level	
IC7 ⑥	Constant H level	
IC7 ⑧	Constant H level	
IC7 ⑨	Constant H level	
IC7 ⑬	Constant H level	
IC8 ③	Negative pulse	Same as $\overline{MI}$ (CPU bus)
IC8 ⑤	Negative pulse	Same as $\overline{IORQ}$ (CPU bus)

Output terminals of address decoding circuit

IC11 ⑥	Develops negative pulse when I/O address C0H to C3H (192 to 195) are accessed.
IC9 ⑮	Develops negative pulse when I/O address C4H (196) is read out.
IC9 ⑪	Develops negative pulse when data are written on to I/O address C4H (196).
IC9 ⑩	Develops negative pulse when data are written on to I/O address C5H (197).

Input terminals of PIO

IC12 ⑤	Same signal as A1 (CPU bus)
⑥	Same signal as A0 (CPU bus)
㉟	Same signal as $\overline{RD}$ (CPU bus)
㊱	Same signal as $\overline{IORQ}$ (CPU bus)
㊲	Same signal as $\overline{M1}$ (CPU bus)
㉔	Same signal as IEI (CPU bus)
㉕	Same signal as BUSϕ (CPU bus)

	In BASIC ready status	At transmission of data to GP-IB	At receiving data in slave mode
IC13 ⑬	Constant L level	Outputs positive pulse of about 5μsec.	Constant L level
IC13 ⑫	Constant H level	Constant H level	Outputs negative pulse of about 500μsec.

MZ-8BI04 PWB AND CIRCUIT DIAGRAM

Notes: The printed wiring board and circuit diagram are subject to change without prior notice.

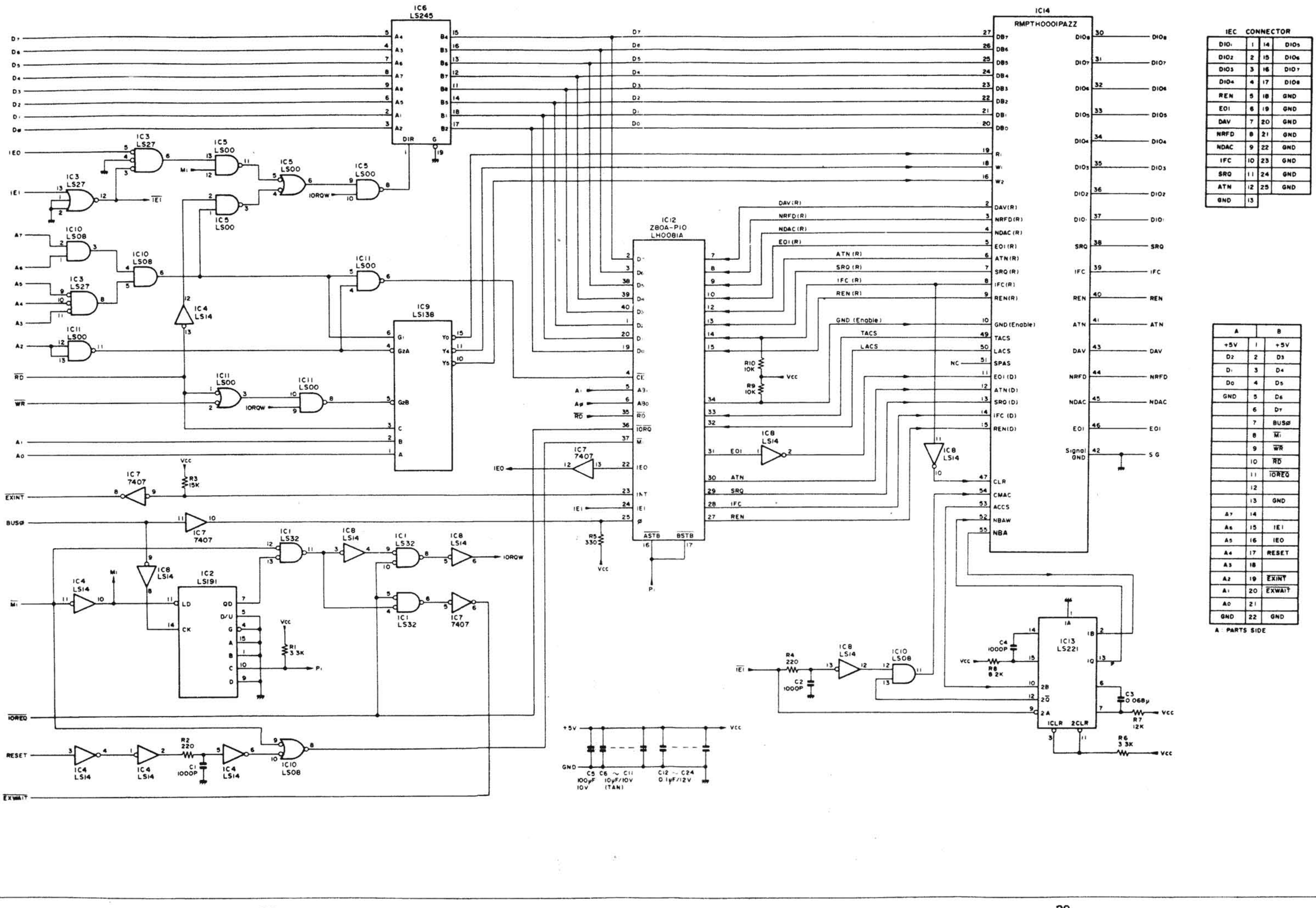
■ Printed Wiring Board

Perspective View

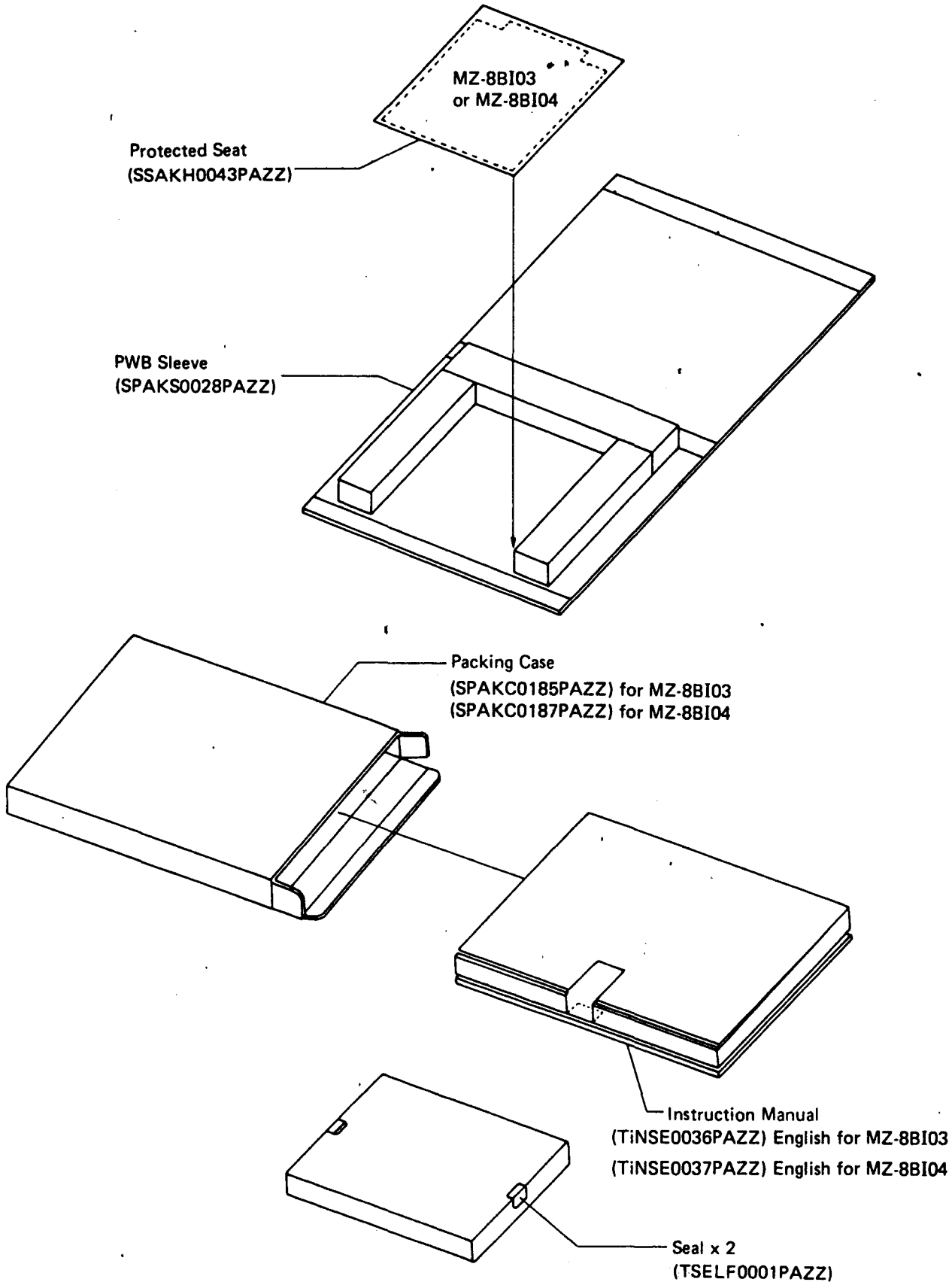
Parts-fitted face

Opposite Side

■ Circuit Diagram



PACKING METHOD



REPLACEMENT PARTS LIST

"HOW TO ORDER REPLACEMENT PARTS"

To have your order filled promptly and correctly, please furnish the following information.
1. MODEL NAME 2. REF. NO.
3. PART NO. 4. DESCRIPTION

NOTES: Be sure to use regular parts for securing the safety and reliability of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

MODEL MZ-8BI03

REF. NO.	PART NO.	DESCRIPTION	CODE
INTEGRATED CIRCUITS			
IC1	RH-iX0297PAZZ	MC14411	BA
IC2, IC8	RH-iX0305PAZZ	SN75189AN	AM
IC3, IC4	RH-iX0190PAZZ	SN74LS266N	AF
IC5	RMPTH0002PAZZ	Hybrid IC	BU
IC6, IC7	RH-iX0085PAZZ	SN75188N	AM
IC9	RH-iX0152PAZZ	TL497CN	AU
IC13	DUNTK0064PAZZ	12N10K1	BF
TRANSISTORS AND DIODE			
Q1, Q2	VS2SA496-Ō/-1	2SA496-Ō	AF
D1	VHD1S1586//1A	1S1586	AB
RESISTORS			
R1	VRC-MT2EG106K	10M ohm, 1/4W	AA
R2, R14	VRD-SC2EF102J	1K ohm, 1/4W	AA
R3, R15	VRD-SC2EF103J	10K ohm, 1/4W	AA
R4	VRD-SC2EF272J	2.7K ohm, 1/4W	AA
R5	VRD-SC2EF472J	4.7K ohm, 1/4W	AA
R6, R10	VRD-SC2EF101J	100 ohm, 1/4W	AA
R7	VRD-RU2EE222J	2.2K ohm, 1/4W	AA
R8	VRD-RU2EE561J	560 ohm, 1/4W	AA
R9	VRD-RU2EE273J	27K ohm, 1/4W	AA
R11	VRD-SC2EF221J	220 ohm, 1/4W	AA
R12	VRD-SC2EF561J	560 ohm, 1/4W	AA
R13	VRN-RT2HC1R0F	1 ohm, 1/2W	AB
R16	VRD-SC2EF104J	100K ohm, 1/4W	AA
RA1	RMPTC1019PAZZ	Resistor Array 3.3K ohm x 6	AC
CAPACITORS			
C1, C2	VCTYPU1BD104Z	0.1MFD, 12V, Ceramic	AB
C3, C16	VCTYPU1BD104Z	0.1MFD, 12V, Ceramic	AB
C4, C7, C22, C24	VCKZPR1HB221K	220PFD, 50V, Ceramic	AA
C8	VCEAAU0JW107Y	100MFD, 6.3V, Aluminum	AB
C9, C11, C12, C14, C18, C20	VCKZPR1HF103P	0.01MFD, 50V, Ceramic	AA
C10	VCSACU1AE336K	33MFD, 10V, Tantalum	AD
C13, C15, C19, C21	VCEAAU1CW336Y	33MFD, 16V, Aluminum	AB
C17	VCCSPR1H6151J	150PFD, 50V, Ceramic	AA
MISCELLANEOUS			
L1	RCiLF7863VAZZ	Coil CH04	AG
L2, L4	RCiLF7862VAZZ	Coil CH03	AG
L3	RCiLF7864VAZZ	Coil 8S651	AK
X'TAL	RCRSA0017PAZZ	Crystal 1.8432MHz	AP
SW1	QSW-D0004PAZZ	Dip Switch (6 contacts)	AR
SW2, SW3	QSW-D0006PAZZ	Dip Switch (10 contacts)	AR
J-1	QPLGZ0103PAZZ	4-Pin Plug	AD
J-2, J-3	QPLGZ0102PAZZ	3-Pin Plug	AC
	QJUM-0004PAZZ	Jumper (for J-1, J-2, J-3)	AF
CN1, CN2	QPLGZ0104PAZZ	9-Pin Terminal	AY
	LANGK0296PAZZ	Fixing Metal (for two 9-Pin terminal)	AF
	QSŌCZ0010PAZZ	24-Pin IC Socket	AF
	TiNSE0036PAZZ	Instruction Manual (English)	BP

MODEL MZ-8BI04 PARTS LIST

MODEL MZ-8BI04

REF. NO.	PART NO.	DESCRIPTION	CODE
INTEGRATED CIRCUITS			
IC1	RH-iX0078PAZZ	SN74LS32N	AF
IC2	RH-iX0276PAZZ	SN74LS191N	AL
IC3	RH-iX0149PAZZ	SN74LS27N	AF
IC4, IC8	RH-iX0102PAZZ	SN74LS14N	AM
IC5, IC11	RH-iX0070PAZZ	SN74LS00N	AE
IC6	RH-iX0124PAZZ	SN74LS245N	AR
IC7	RH-iX0200PAZZ	SN7407N	AG
IC9	RH-iX0303PAZZ	SN74LS138N	AG
IC10	RH-iX0075PAZZ	SN74LS08N	AE
IC12	RH-iX0229PAZZ	LH0081A Z-80APIO	BD
IC13	RH-iX0227PAZZ	SN74LS221N	AN
IC14	RMPTH0001PAZZ	Hybrid IC	BY
RESISTORS			
R1, R6	VRD-SC2EF332J	3.3K ohm, 1/4W	AA
R2, R4	VRD-SC2EF221J	220 ohm, 1/4W	AA
R3	VRD-SC2EF153J	15K ohm, 1/4W	AA
R5	VRD-SC2EF331J	330 ohm, 1/4W	AA
R7	VRD-SC2EF123J	12K ohm, 1/4W	AA
R8	VRD-SC2EF822J	8.2K ohm, 1/4W	AA
R9, R10	VRD-SC2EF103J	10K ohm, 1/4W	AA
CAPACITORS			
C1, C2	VCKYPU2HB102K	1,000PFD, 500V, Ceramic	AA
C3	VCQYKU1HM683K	0.068MFD, 50V, Film	AB
C4	VCQSMU1HM102J	1,000PFD, 50V, Film	AC
C5	VCEAAU1AW107M	100MFD, 10V, Aluminum	AB
C6 ~ C11	VCSACU1AE106M	10MFD, 10V, Tantalum	AD
C12 ~ C24	VCTYPU1BD104Z	0.1MFD, 12V, Ceramic	AB
MISCELLANEOUS			
	QPLGZ0105PAZZ	25-Pin Terminal	BC
	LANGK0297PAZZ	Fixing Metal of 25-Pin Terminal	AG
	TiNSE0037PAZZ	Instruction Manual (English)	BR