

# SHARP SERVICE MANUAL

CODE:00ZPCE500SM/E



## MODEL PC-E500

### 1. Product outline

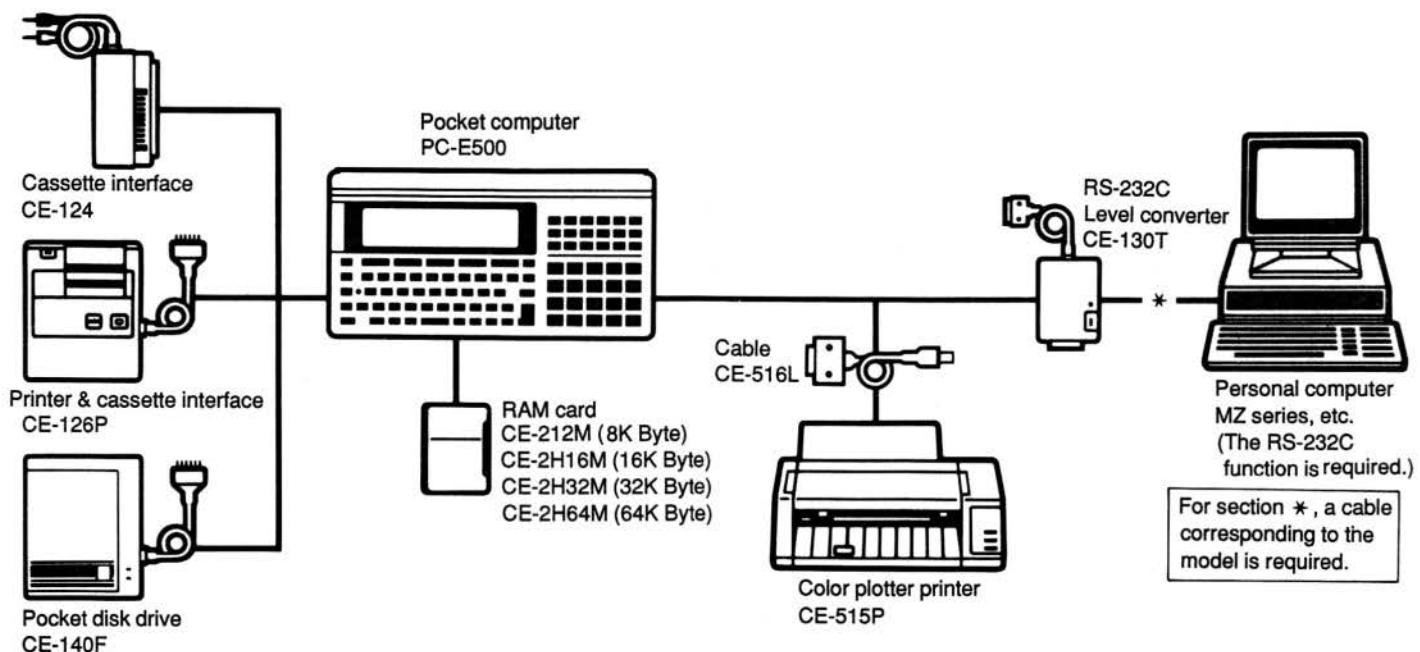
The PC-E500 employs the large display (40 digits x 4 lines) and 32KB memory (standard).

### 2. Specifications

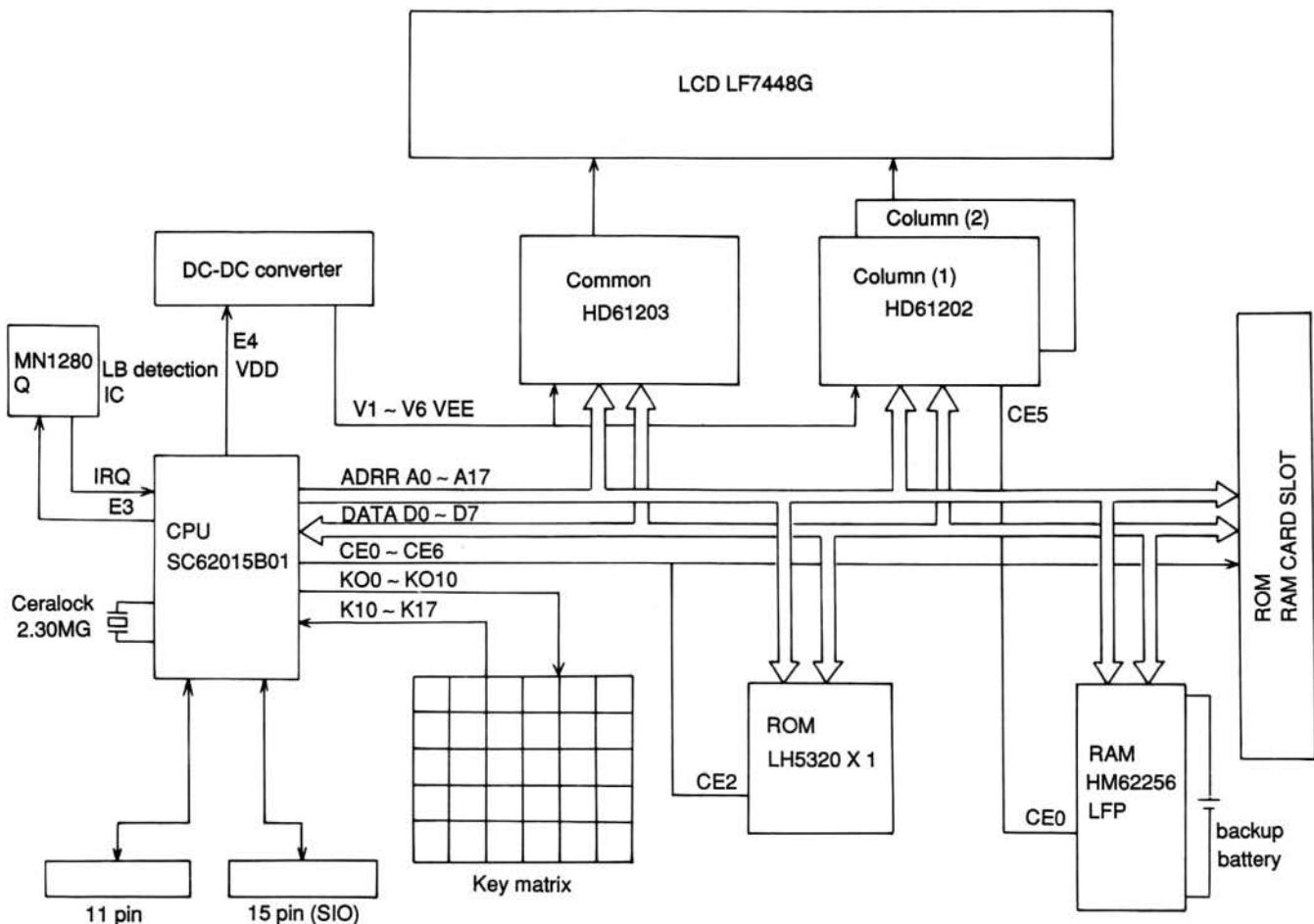
Model name	: PC-E500
Display	: 40 digits x 4 lines (5 x 7 dot matrix liquid crystal display)
Calculation digit	: Single accuracy calculation; 10 digits (Mantissa) + 2 digits (Exponent) Double accuracy calculation; 20 digits (Mantissa) + 2 digits (Exponent) In CAL, MATRIX, or STAT mode, calculation is performed in single accuracy.
Calculation system	: In the sequence of formula. (Priority judgement function)
Program language	: BASIC
CPU	: CMOS 8 bit CPU
System ROM	: 128 K Byte
Memory capacity	: System area about 3.8 K Byte Fixed variable (A - Z) area 312 Byte Program data area 28600 Byte
Stack	: Total 145 Byte Subroutine; 4 Byte for one stage FOR-NEXT; 21 Byte for one stage
Basic calculation functions	: Basic calculations; Addition, subtraction, multiplication, division Functional calculation; Trigonometric function, reverse trigonometric function, hyperbolic function, reverse hyperbolic function, logarithm, exponent, angle conversion, power, power root, coordinate conversion, extraction of the square root, integration, absolute value, code function, pi, etc.

Edit function	: Cursor shift, right/left ( $\blacktriangleleft$ , $\triangleright$ ) Insertion (INS) Delete (DEL, BS) Line up, down ( $\uparrow$ , $\downarrow$ )
Serial I/O machine	
Communication system	: Start-stop synchronous (asynchronous) system, half duplex/total duplex mode
Communication speed	: 300, 600, 1200, 2400, 4800, 9600bps (bit per second)
Parity bit	: Even number, odd number, none
Word length	: 7, 8 bit
Stop bit	: 1, 2 bit
Connector	: 15-pin connector (for connection with external devices)
Output signal level	: C-MOS level (4 – 6V)
Interface signal	: Input ..... RD, CS, CD Output ..... SD, RS, RR, ER Others ..... SG, FG, VC
Memory protection	: Battery backup (Backups the program and data when the power is turned off.)
Operating temperature	: 0 ~ 40°C
Power source	: DC 6V (R03 x 4)
Battery operating time	: About 70 hours of continuous operation (Under the operating temperature of 20°C, 10 minutes of calculation or program execution and 50 minutes of display for every hour) • There may be some variation depending on the operating environment and using conditions.
Power consumption	: 0.07W
External dimension	: 200mm (W) x 100mm (D) x 14mm (H)
Weight	: 250g (Including the battery)
Accessories	: Hard cover, R03 battery x 4, Instruction Manual

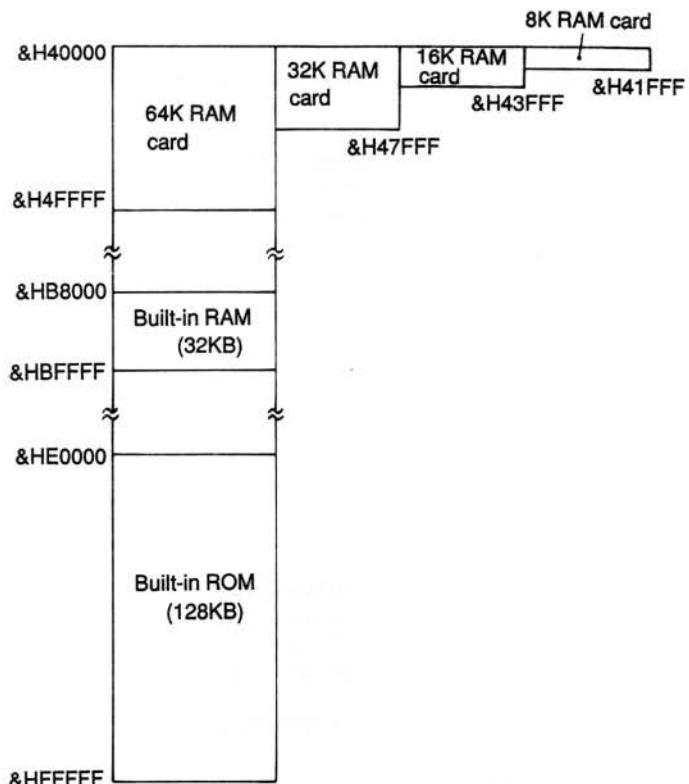
### 3. System configuration



### 4. PC-E500 system block diagram



## 5. Memory map



## 6. LSI description

CPU (SC62015) terminal signal description

Terminal No.	Signal name	Input/Output	Signal description
1	X1	Output	Ceramic oscillation output
2	X2	Input	Ceramic oscillation input
3	X3	Output	CR oscillation output
4	X4	Input	CR oscillation input
5	VDD	Output	Display power (converter) control output
6	VCC	Power	⊕ power input terminal
7	RESET	Input	Reset input. Reset at high level.
8	GND	Power	⊖ power input terminal
9	TEST	Input	Test input
10	CI	Input	Cassette signal input terminal
11	CO	Output	Cassette signal output terminal
12	ON	Input	ON key input terminal. Normally pulled down to low level.
13	WR	Output	Write clock. Normally high level.
14	MRQ	-	(Not used.)
15	K10	Input	Key input terminal
~	~	~	
22	K17	Input	
23	DIO0	I/O	Data bus
~	~	~	
30	DIO7	I/O	
31	A0	Output	Address bus
~	~	~	
49	A18	Output	
50	VDISP	-	(Not used.)
51	VA	-	
52	φD	Output	Clock output terminal for display chip
53	KO15	Output	SIO PRQ (Not used.)
54	KO14	Output	SIO ER, High level with OPEN command.
55	KO13	Output	SIO RR (Reception in the main body side allowed)
56	KO12	Output	SIO RS (Send request in the main body side)
57	KO11	Output	Key strobe signal
58	KO10	Output	
59	IRQ	Input	Low battery detection input terminal

Terminal No.	Signal name	Input/Output	Signal description	
60	φOUT	-		(Not used.)
61	CE7	-		ROM card chip select signal (active high)
62	CE6	Output	Chip select signal for display chip (Active high)	10000 ~ 1FFFF
63	CE5	Output		00000 ~ 03FFF, 08000 ~ 0BFFF
64	CE4	-		(Not used.)
65	CE3	-		Internal ROM chip enable signal
66	CE2	Output	RAM card chip enable signal	C0000 ~ FFFFF
67	CE1	Output	Internal RAM chip enable signal	40000 ~ 7FFFF
68	CE0	Output		80000 ~ BFFFF
69	φA	-		
70	DIS	-		(Not used.)
71	HA	-		
72	RD	-		
73	KO9	Output	Key strobe signal	
?	?	?		
82	KO0	Output		
83	RXD	Input	SIO RD (Receive data)	
84	TXD	Output	SIO SD (Send data)	
85	E15	Input		
86	E14	Input		CE-140F data input terminal
87	E13	Input		
88	E12	Input		
89	E11	Output	11 pin DIN	P-ch open output
90	E10	Output	11 pin DOUT	P-ch open output
91	E9	Output	11 pin IO2	P-ch open output
92	E8	Output	11 pin IO1	P-ch open output
93	E7	Input	11 pin ACK	
94	E6	Output	11 pin BUSY	P-ch open output
95	E5	-	(Not used.)	
96	E4	Output	Display power (converter) control signal	
97	E3	Output	Low battery voltage control signal	
98	E2	Input	SIO CS (Opponent side send enable)	
99	E1	Input	SIO CD (Opponent side send request)	
100	E0	Input	SIO PAK (Not used.)	

## 7. Low battery detection circuit

The PC-E500 is equipped with the low battery detection circuit. The operations of the circuit are described below. (Part location numbers may differ from those in the actual circuit diagram.)

When input voltage VIN exceeds the detection voltage VD, the output of the voltage detection IC [LBIC(MN1280)] is driven from Low to High. When VIN falls under VD, the output is driven from High to Low.

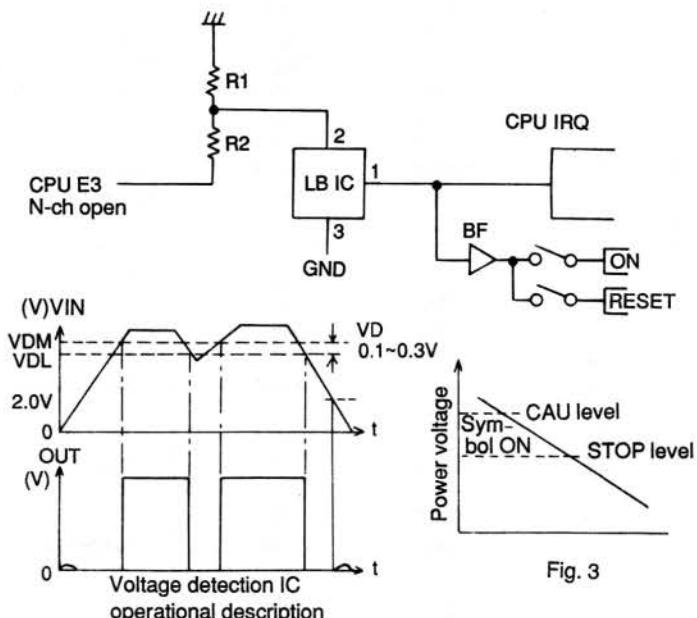
The LBIC (MN1280) detects both the CAU level and the STOP level by dividing the voltage applied to the input terminal (2 pin) with R1 and R2 and by turning on/off R2 with CAU signal of G-A.

When the power voltage falls under the CAU level, as shown in Fig. 3, the BATT symbol lights up. When the power voltage falls further under the STOP level, the symbol goes off.

For CAU level detection, the CPU E3 it turned on (low level) and the CPU IRQ terminal state is observed. (If the IRQ is at Low level, the symbol lights up.)

When the CAU level is detected, the CPU E3 terminal is turned off (high impedance). (When the CPU E3 terminal is turned off, resistor division is not performed and the voltage at LBIC 2 pin increases, driving the output from Low to High.) The CPU IRQ terminal state is checked again to detect the STOP level.

After the STOP level is detected, the ON key and the RESET key become ineffective.



Low battery detection circuit check

CAU level VCC – GND: 4.2V to 4.6V  
STOP level VCC – GND: 3.8V to 4.2V

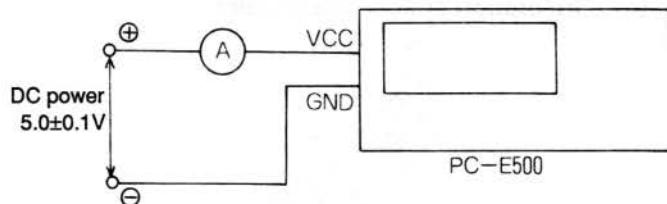
Fig. 3

## 8. Current consumption check

Power source: DC +5.0V is supplied to 11-pin connector No.2 pin (VCC) and 0V to No.3 pin (GND).

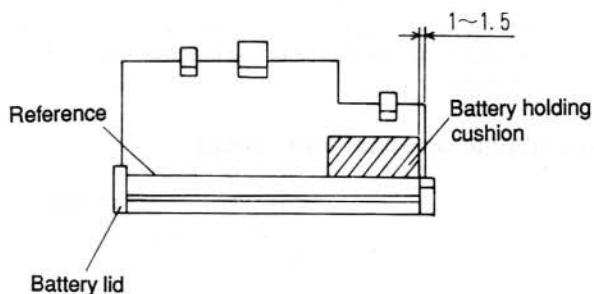
Current: ON (BASIC mode ">" is displayed); 3.24mA or less  
OFF (Power off); 64μA or less

LSI circuit		SPEC (Max.)	Actual use (Max.)
SC62015B01 (CPU)	RUN During display OFF	f=2304kHz 220μA 3μA	← ← ←
LH5320x1 (2Mb ROM)	RUN HLT	t <sub>RC</sub> =120ns 70mA 15μA	f=306kHz 4.59mA ←
HM62256LFP-12SLT (32KB RAM)	RUN HLT	t <sub>RC</sub> =120ns 70mA 100μA	f=153kHz, 1.29mA ←
HD61203		f=600kHz 1.0mA	←
HD61202 (x2)	During access during display HLT	500μA 100μA 15μA	← ← ←
MN1280Q (Low battery detection IC)		30μA	←
DC-DC converter (input)		1.2mA	←
VDD		1.0mA	←

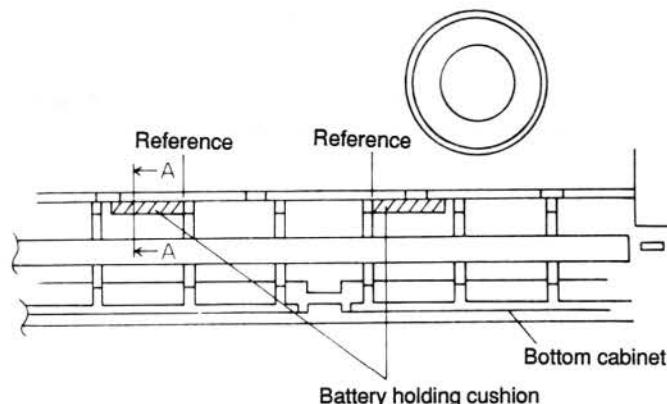


## 9. Note for servicing

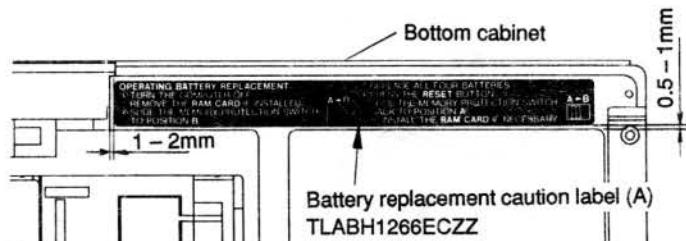
### 9-1. Battery holding cushion attachment



### 9-2. Battery holding cushion attachment

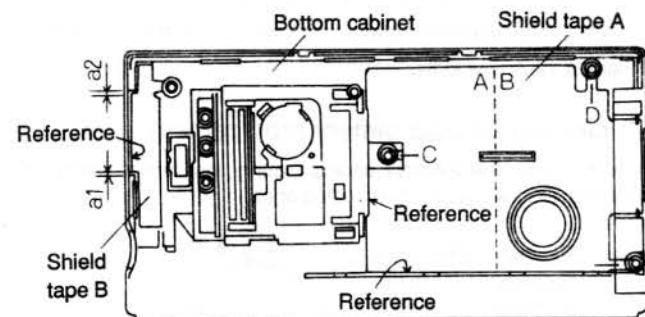


### 9-3. Battery replacement label attachment

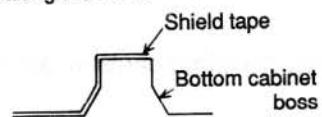


- Must be free from tilt.

### 9-4. Shield tape attachment



Note: When attaching to the boss section, attach neatly along the boss.



#### Attachment procedure

##### Shield tape A

- 1) Remove the separation paper in side B, and bend section C and D as shown below.
- 2) Fit the A side with the reference, and paste the B side.
- 3) Remove the separation paper, and attach the tape.



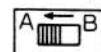
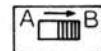
- 4) Attach the three boss sections. (Fit the boss holes with the shield tape holes.)
- 5) Attach the tape so that there is no slack.

##### Shield tape B

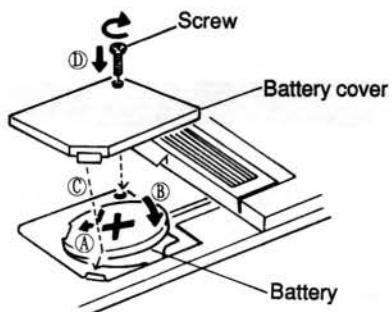
- 1) Bend E section. (Similar to C section.)
- 2) Fit with the reference and attach so that a1 and a2 are even.
- 3) Attach the boss section. (Fit the boss hole and the shield tape hole.)
- 4) Attach the tape so that there is no slack.

### 9-5. Main PWB replacement procedure

- ① Press the OFF key. (If a RAM card is installed, remove it.)
- ② Switch the select switch from A to B.
- ③ Replace all the four batteries with new ones.
- ④ Press the RESET switch.
- ⑤ Switch the select switch from B to A. (Install the RAM card.)



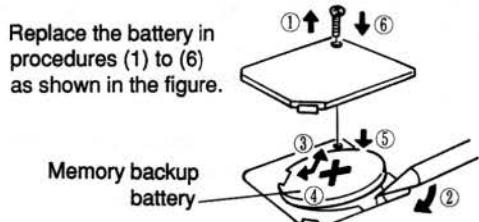
## 9-6. Memory backup battery cover attachment



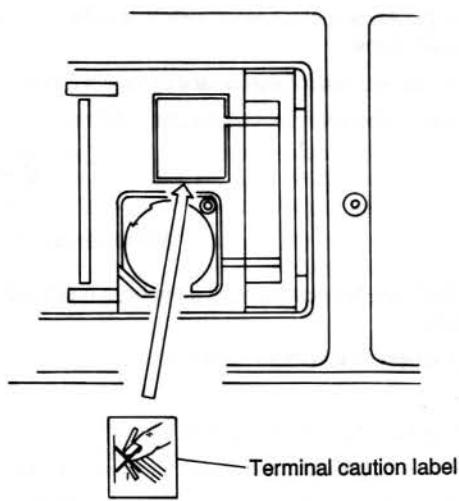
- Ⓐ Hang the battery on the larger pawl.
- Ⓑ Push the battery to hang on the smaller pawl.
- Ⓒ Hang the battery cover pawl on the cabinet, and push it to attach.
- Ⓓ tighten the screw to fix.

## 9-7. Memory backup battery replacement

When replacing the memory backup battery, be sure to install four batteries (R03 x 4). (Use unexhausted ones.)

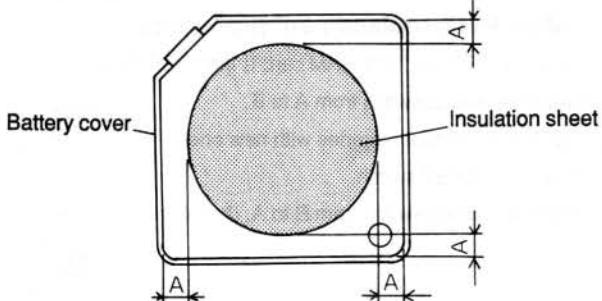


## 9-8. Terminal caution label attachment



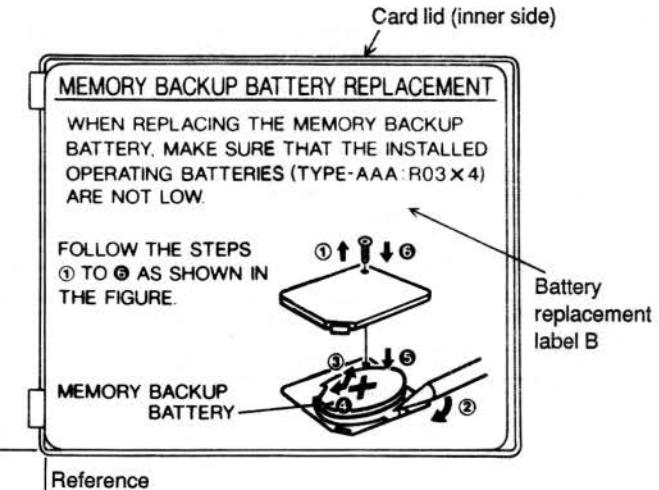
- \* Paste the label correctly in position.

## 9-9. Battery insulation sheet attachment



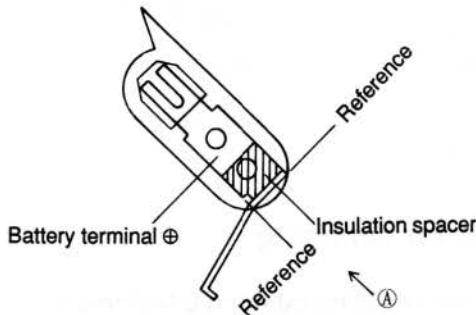
Attach the insulation sheet to the center so that dimensions A (4 positions) are all the same.

## 9-10. Battery replacement label B attachment



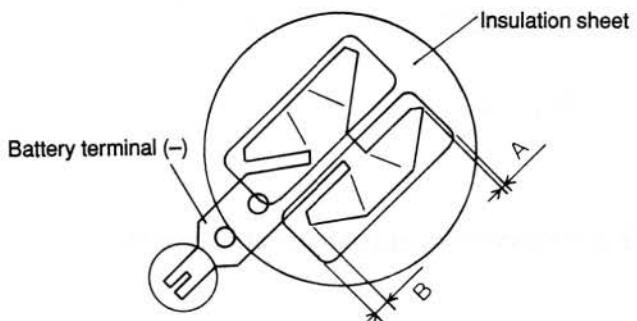
- Must be free from tilt.

## 9-11. Insulation spacer attachment



- 1) Solder the battery terminal +.
- 2) Take the insulation spacer with tweezers and insert under the battery terminal from side A. (Note that the paste side is the battery terminal side.)

## 9-12. Insulation sheet attachment



- Attach the insulation sheet so that it does not cover the spring by minimizing dimension A and maximizing dimension B.

## 10. Check software for servicing

- Check item

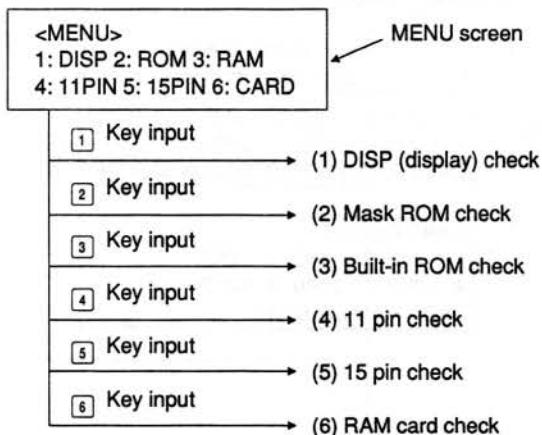
- (1) Liquid crystal visual check (alternate display)
- (2) Mask ROM verify check
- (3) Built-in RAM read/write check
- (4) 11 pin I/O check
- (5) 15 pin I/O check
- (6) RAM card read/write check

- Required tools

Jig UKOGC3020CSZZ: Used for (4) and (5).

- Outline of using method

Before inputting a check software, clear the RAM completely.  
When check (6) is executed, the RAM card content is deleted.  
Save programs and data before check, if necessary.



Note: To end a check, press the BRK[ON] key.

- Details of each check

(1) DISP (display) check

MENU screen



Alternate display  
All symbols light up.

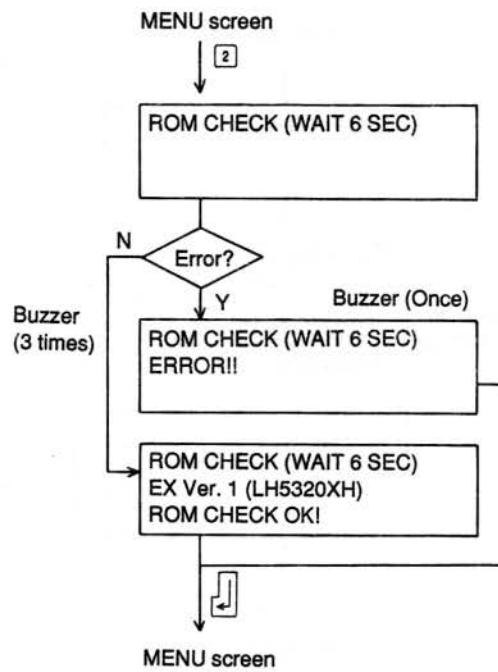


Alternate reversion  
all symbols go off.

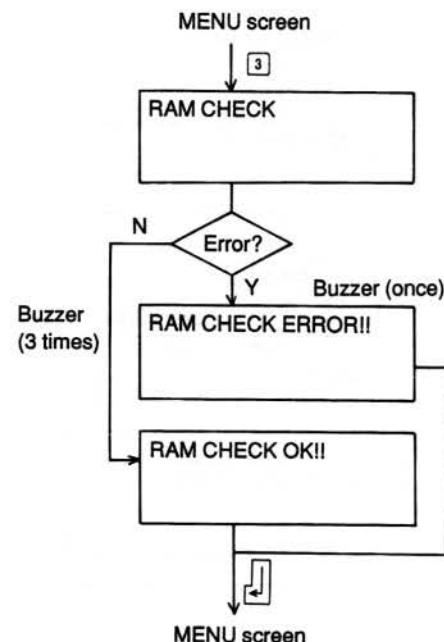


MENU screen

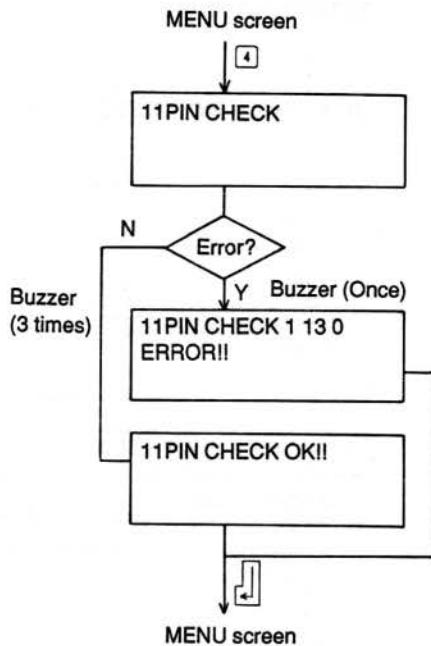
(2) Mask ROM check



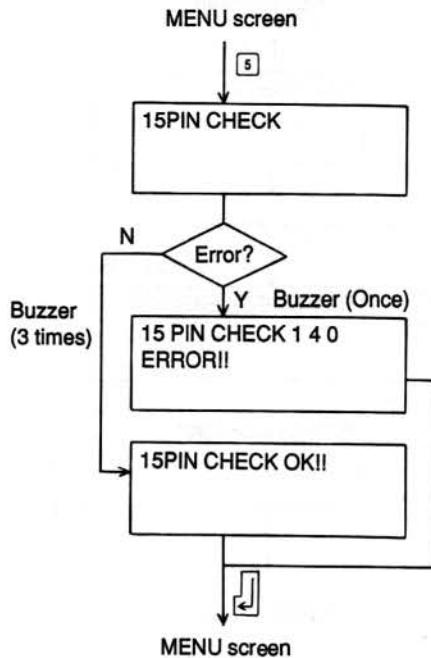
(3) Built-in RAM check



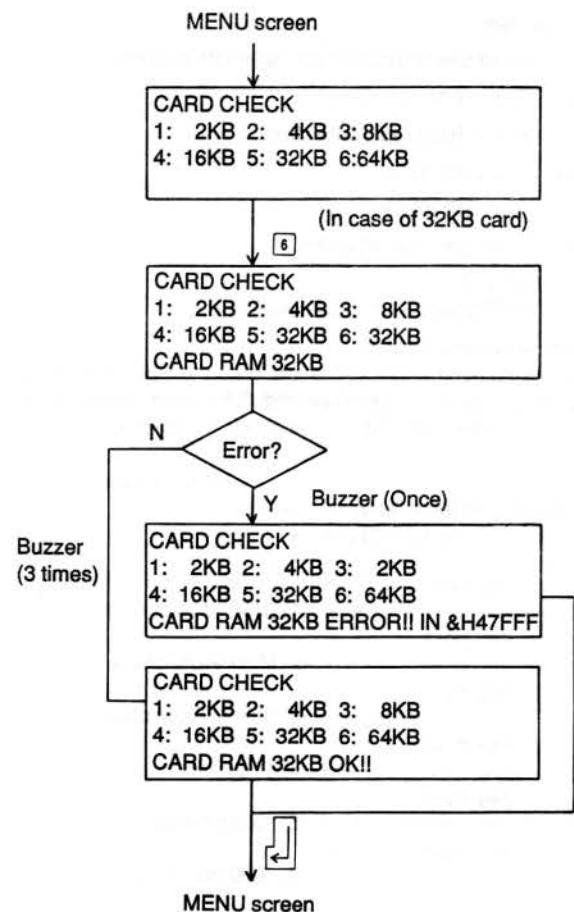
(4) 11 pin check



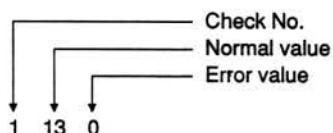
(5) 15 pin check



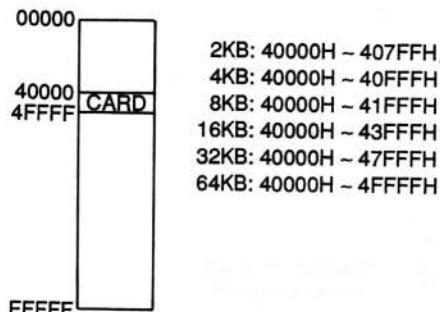
(6) RAM card check



- The error code in 11 pin check or 15 pin check means as follows:



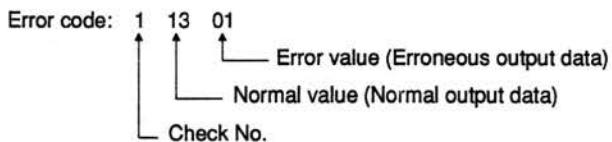
- For details of error, see "Error code description".



- Addresses are checked from higher one to lower one, and the error address found first is displayed.

- Error code description

(Example) In 11 pin check error:



See the 11pin check code table.

NO	(Output port)					(Input port)					Normal data
	BUSY	Din	Dout	IO2	IO1	ACK	Din	Dout	IO2	IO1	
0	0	0	0	0	1	1	0	0	1	1	13

The above table shows that input port signal "10011" is normal when output port signal is "000001." ("10011" is a binary number which is converted into "13" in hexadecimal number system.)

When 11 pin check error code is "1 13 01," it shows that input port signal is erroneously "01 (00001)" though it should be "13 (10011)." ("01" is a binary number which is converted into "1" in hexadecimal number system.)

That is, data at ACK and IO2 are erroneous.

- 11 pin check code table

NO.	(Output port)					(Input port)					Normal data
	BUSY	Din	Dout	IO2	IO1	ACK	Din	Dout	IO2	IO1	
0	0	0	0	0	0	0	0	0	0	0	00
1	0	0	0	0	1	1	0	0	1	1	13
2	0	0	0	1	0	1	0	0	1	1	13
3	0	0	0	1	1	1	0	0	1	1	13
4	0	0	1	0	0	1	1	1	0	0	1C
5	0	0	1	0	1	1	1	1	1	1	1F
6	0	0	1	1	0	1	1	1	1	1	1F
7	0	0	1	1	1	1	1	1	1	1	1F
8	0	1	0	0	0	1	1	1	0	0	1C
9	0	1	0	0	1	1	1	1	1	1	1F
A	0	1	0	1	0	1	1	1	1	1	1F
B	0	1	0	1	1	1	1	1	1	1	1F
C	0	1	1	0	0	1	1	1	0	0	1C
D	0	1	1	0	1	1	1	1	1	1	1F
E	0	1	1	1	0	1	1	1	1	1	1F
F	0	1	1	1	1	1	1	1	1	1	1F
10	1	0	0	0	0	1	0	0	0	0	10
11	1	0	0	0	1	1	0	0	1	1	13
12	1	0	0	1	0	1	0	0	1	1	13
13	1	0	0	1	1	1	0	0	1	1	13
14	1	0	1	0	0	1	1	1	0	0	1C
15	1	0	1	0	1	1	1	1	1	1	1F
16	1	0	1	1	0	1	1	1	1	1	1F
17	1	0	1	1	1	1	1	1	1	1	1F
18	1	1	0	0	0	1	1	1	0	0	1C
19	1	1	0	0	1	1	1	1	1	1	1F
1A	1	1	0	1	0	1	1	1	1	1	1F
1B	1	1	0	1	1	1	1	1	1	1	1F
1C	1	1	1	0	0	1	1	1	0	0	1C
1D	1	1	1	0	1	1	1	1	1	1	1F
1E	1	1	1	1	0	1	1	1	1	1	1F
1F	1	1	1	1	1	1	1	1	1	1	1F

- 15 pin check code table

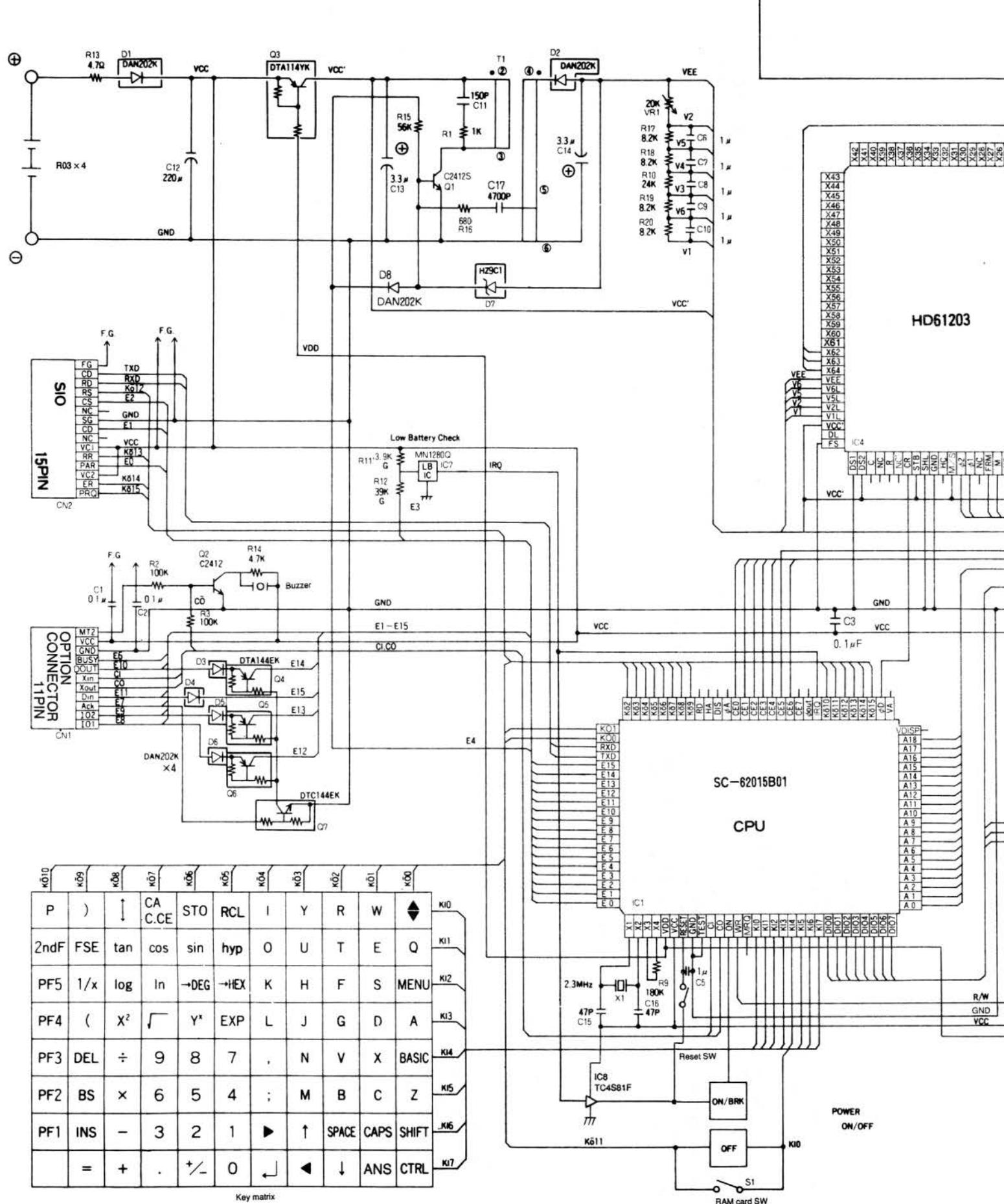
NO.	(Output port)					(Input port)					Normal data
	PRQ	ER	RR	RS	CS	CD	PAK				
0	0	0	0	0	0	0	0	0	0	0	00
1	0	0	0	1	1	1	0	0	0	0	04
2	0	0	1	0	0	1	0	0	0	0	02
3	0	0	1	1	1	1	1	0	0	0	06
4	0	1	0	0	0	0	0	0	0	1	01
5	0	1	0	1	1	1	0	1	1	0	05
6	0	1	1	0	0	0	1	1	1	1	03
7	0	1	1	1	1	1	1	1	1	1	07
8	1	0	0	0	0	0	0	0	0	1	01
9	1	0	0	1	1	0	1	0	0	1	05
A	1	0	1	0	0	0	1	1	1	1	03
B	1	0	1	1	1	1	1	1	1	1	07
C	1	1	0	0	0	0	0	0	0	1	01
D	1	1	0	1	1	1	0	0	0	1	05
E	1	1	1	0	0	1	1	1	1	1	03
F	1	1	1	1	1	1	1	1	1	1	07

```

10:ARUM
20:IF PEEK &BFD1A+PEEK &
    BFD1B*&100+PEEK &BFD1
    C*&10000<>&BFC00 THEN
    *I
30:POKE &BFE03,&1A,&FD,&
    0B,&00,&05,&00:CALL &
    FFFD8
40:/*A:CLS :PRINT "<MENU>
50:PRINT "1:DISP 2:ROM
    3:RAM
60:PRINT "4:11PIN 5:15PI
    N 6:CARD
70:A=VAL INKEY$
80:IF A<10R A>6THEN 70
90:ON A GOSUB *B,*C,*D,*E,*F,*G
100:GOTO *A
110:*B:B=&BFC97:S=PEEK B
    :T=PEEK (B+1):U=PEEK
    (B+2):V=PEEK (B+3)
120:A$="55AA":C=255:GOSU
    B *&H:GOSUB *I
130:A$="AA55":C=0:GOSUB
    *H:GOSUB *I
140:POKE B,S,T,U,V
150:RETURN
160:/*H:POKE B,C,C,C,C
170:CLS :FOR I=1TO 4:GCU
    RSOR (0,I*8-1):FOR J
    =0TO 119:GPRINT A$:
    NEXT :NEXT
180:RETURN
190:/*C:CLS :PRINT "ROM C
    HECK (WAIT 6 SEC)"
200:M=&BEEA0:GOSUB *J:CA
    LL M
210:B$="" :A$=HEX$ PEEK (
    M-1)+HEX$ PEEK (M-2)
220:IF A$="5C7E"LET B$=
    135"
230:IF A$="DC70"LET B$=
    122"
240:IF A$="350E"LET B$=
    111"
250:IF A$="A05A"LET B$=
    10-
260:IF A$="9944"LET B$=
    21H"
270:IF A$="B0DC"LET B$=
    20D"
280:IF B$=""BEEP 1:PRINT
    "ROM ERROR!":GOTO *
    I
290:IF B$<"2"PRINT "JAPA
    N ";:GOTO 310
300:PRINT "EX ";
310:PRINT "Ver.":MID$ (B
    $,2,1);"(LH5320X";RI
    GHT$ (B$,1);")":BEEP
    3:PRINT "ROM CHECK
    OK!"
320:GOTO *
330:/*J:POKE M,&0C,&00,&0
    ,&0C,&09,&00,&0A,&0
    ,&00,&09,&04,&44,&3
    ,&6C,&04,&1B,&08,&A
    B,&DE,&EE,&0B,&07,&0
    ,&00,&00,&00,&00,&0
    ,&00,&00,&20,&AB
340:RETURN
350:/*D:CLS :PRINT "RAM C
    HECK ";
360:POKE &5D,0,&90,&B,0,
    &DC,&B
370:M=&BEEA0:GOSUB *K:CA
    LL M
380:IF PEEK &66=0BEEP 3:
    PRINT "OK!!":GOTO *I
390:BEEP 1:PRINT "ERROR!
    ! IN &H":HEX$ PEEK &
    65+RIGHT$ ("0"+HEX$ PEE
    K &64,2)+HEX$ PEE
    K &63
400:GOTO *
410:/*E:CLS :PRINT "11PIN
    CHECK ";
420:RESTORE *L
430:D=PEEK &F3:E=PEEK &F
    4
440:POKE &F3,D AND &BF
450:/*Y:FOR I=0TO 15
460:POKE &F4,I
470:F=PEEK &F5:G=PEEK &F
    6
480:J=(F AND &80)/8+(G A
    ND &F0)/16
490:READ K
500:IF J<>K THEN PRINT H
    EX (I);HEX (K);HEX (J):
    GOTO *M
510:NEXT
520:IF Z=1THEN *Z
530:Z=1:POKE &F3,D OR 64
540:GOTO *Y
550:/*Z:POKE &BFCBF,64
560:L=PEEK &FD:POKE &FD,
    ((L AND &8F)+80):M=P
    EEK &FF
570:IF (M AND 2)THEN *S
    ELSE *M
580:/*S:POKE &FD,((L AND
    &8F)+64):M=PEEK &FF
590:IF (M AND 2)THEN *M
600:BEEP 3:PRINT "OK!!"
610:GOTO *
620:/*L:DATA 0,19,19,19,2
    8,31,31,31,28,31,31,
    31,28,31,31,31,16,19
    ,19,19,28,31,31,31,2
    8,31,31,31,28,31,31,
    31
630:/*M:BEEP 1:PRINT "ERR
    OR !"
640:POKE &F3,D,E:POKE &F
    D,L
650:/*N:GOTO *
660:/*F:CLS :RESTORE *Q:P
    RINT "15PIN CHECK ";
670:F1=(PEEK &F1)AND 15
680:FOR I=0TO 15
690:POKE &F1,F1+16*I
700:READ SI01
710:SI02=((PEEK &F5) AND
    7)
720:IF SI01=SI02 THEN 73
    0 ELSE PRINT HEX (I)
    ;HEX (SI01);HEX (SI0
    2):GOTO *O
730:NEXT
740:POKE &F1,F1
750:F7=PEEK &F7:F8=PEEK
    &F8:F9=PEEK &F9:FB=P
    EEK &FB
760:POKE &FB,&8F:POKE &F
    7,&3C
770:FOR I=1TO 100:NEXT
780:F8=PEEK &F8
790:IF (F8 AND 32)THEN P
    RINT "RD HIGH ";:GOT
    O *P
800:POKE &F7,&BC
810:FOR I=1TO 100:NEXT
820:F8=PEEK &F8
830:IF (F8 AND 4)=4THEN
    840ELSE PRINT " RD L
    OW ";:GOTO *P
840:POKE &FB,FB:POKE &F7
    ,F7
850:BEEP 3:PRINT "OK!!"
860:GOTO *
870:/*Q:DATA 0,4,2,6,1,5,
    3,7,1,5,3,7,1,5,3,7
880:/*P:POKE &FB,FB:POKE
    &F7,F7
890:/*O:BEEP 1:PRINT "ERR
    OR !"
900:GOTO *
910:/*G:CLS :PRINT "CARD
    CHECK"
920:IF INKEY$ <>""THEN *
    G
930:PRINT "1: 2KB 2: 4K
    B 3: 8KB
940:PRINT "4:16KB 5:32K
    B 6:64KB
950:/*R:A$=INKEY$ :IF A$<
    "1"OR A$>"6"THEN *R
960:POKE &5D,0,0,4,255,2
    ^VAL A$*4-1,4
970:M=&BEEA0:GOSUB *
980:PRINT "CARD RAM";STR
    $ (2^VAL A$); "KB ";
990:CALL M
1000:IF PEEK &66=0BEEP 3
    :PRINT "OK!!":GOTO
    *I
1010:BEEP 1:PRINT "ERROR
    !! IN &H":HEX$ PEEK
    &65+RIGHT$ ("0"+HE
    X$ PEEK &64,2)+HEX$ PEEK
    &63
1020:GOTO *I
1030:/*K:POKE M,&08,&FF,&
    32,&84,&60,&B0,&04,
    &32,&A4,&63,&7C,&04
    ,&48,&01,&60,&01,&1
    A,&02,&48,&01,&32,&
    C7,&63,&5D,&1B,&15,
    &08,&FF,&32,&84,&60
    ,&32
1040:POKE M+&20,&A4,&63,
    &32,&E0,&04,&67,&32
    ,&63,&67,&1A,&14,&7
    C,&04,&48,&01,&60,&
    01,&1A,&02,&48,&01,
    &32,&C7,&63,&5D,&1B
    ,&1C,&08,&00,&12,&0
    2,&08
1050:POKE M+&40,&01,&32,
    &A0,&66,&9F,&07
1060:RETURN
1070:/*I
1080:IF INKEY$ =""THEN *
    I
1090:RETURN

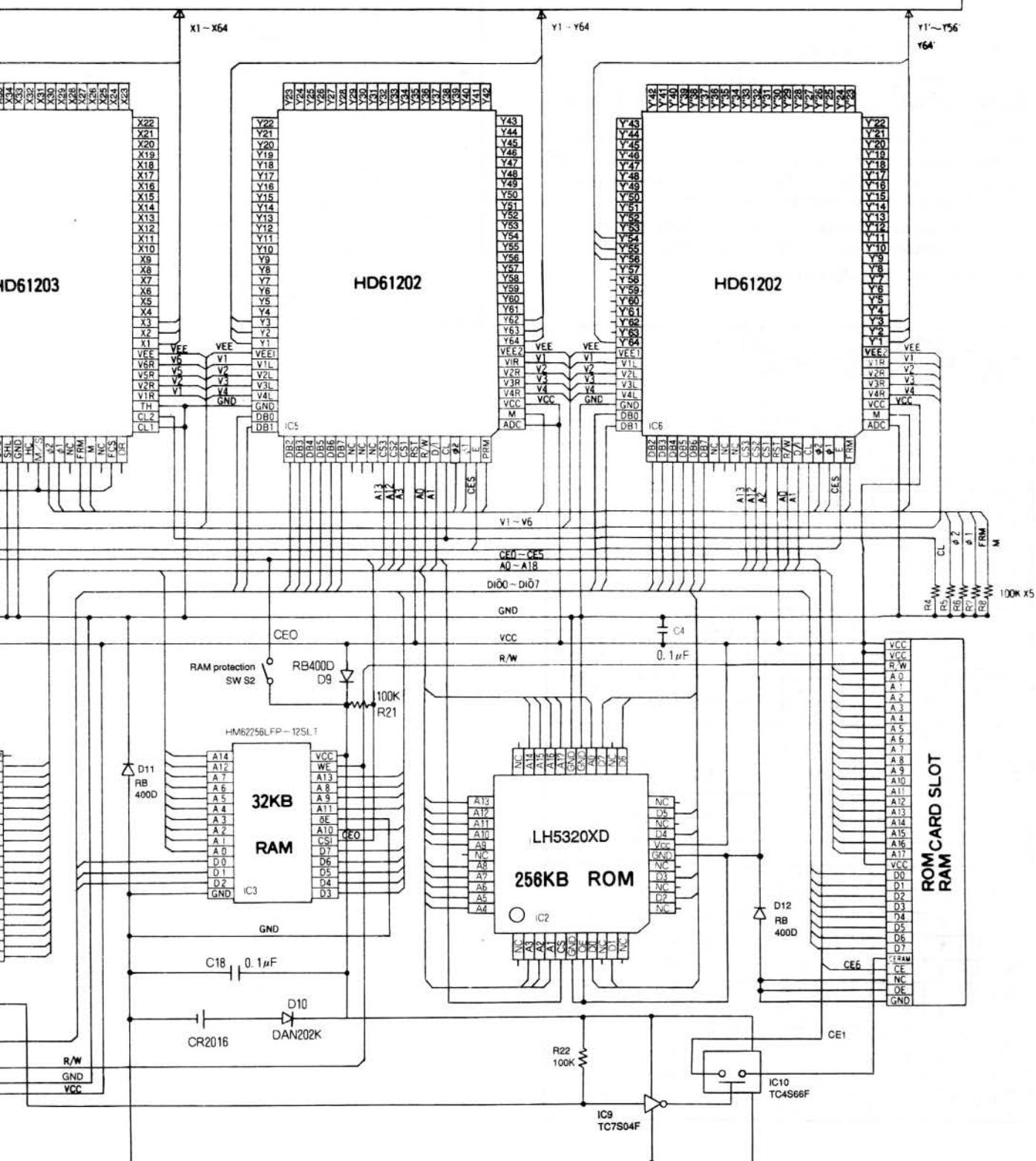
```

## 11. Circuit diagram

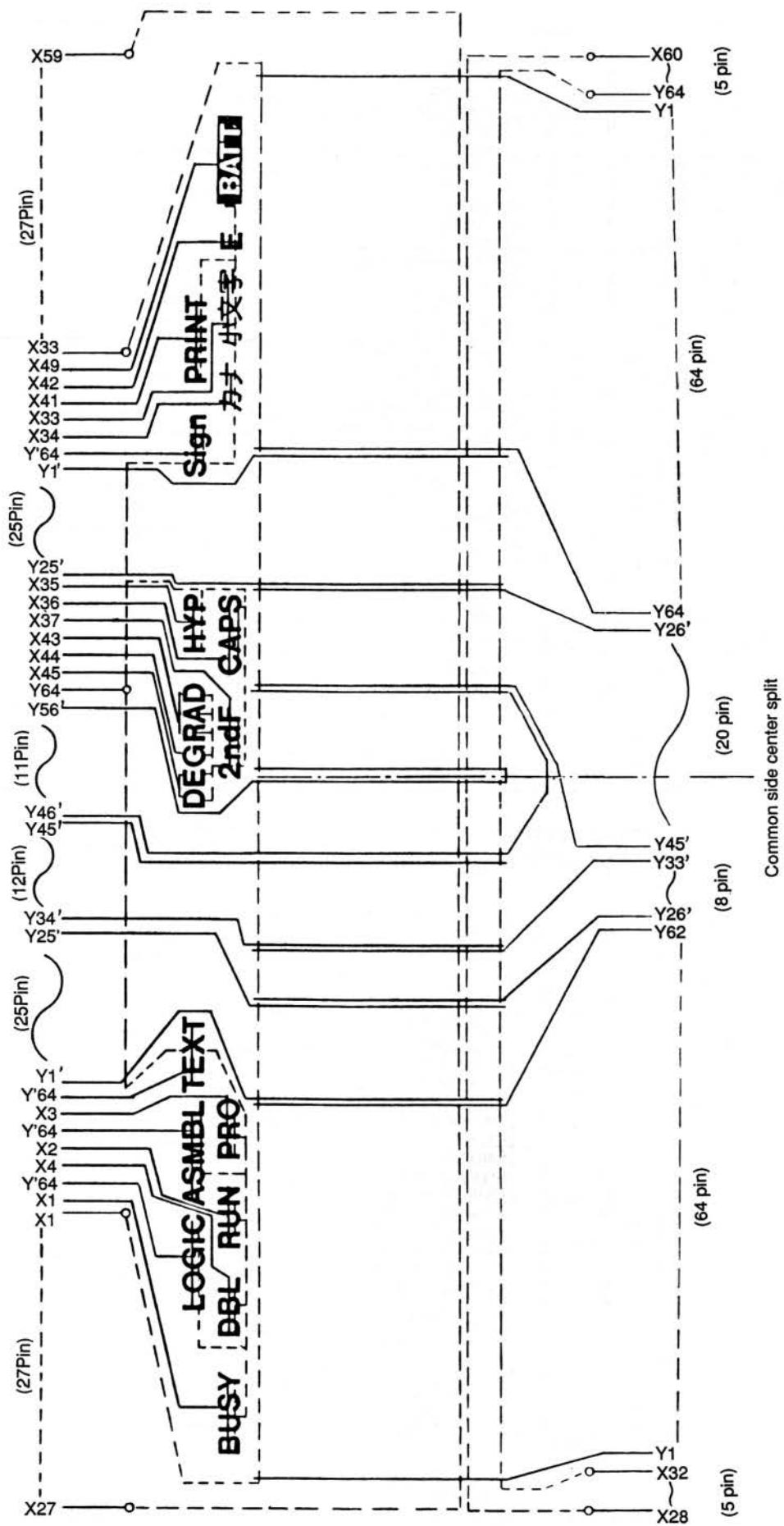


**LCD**

240 x 32 dots

**LF7448G**

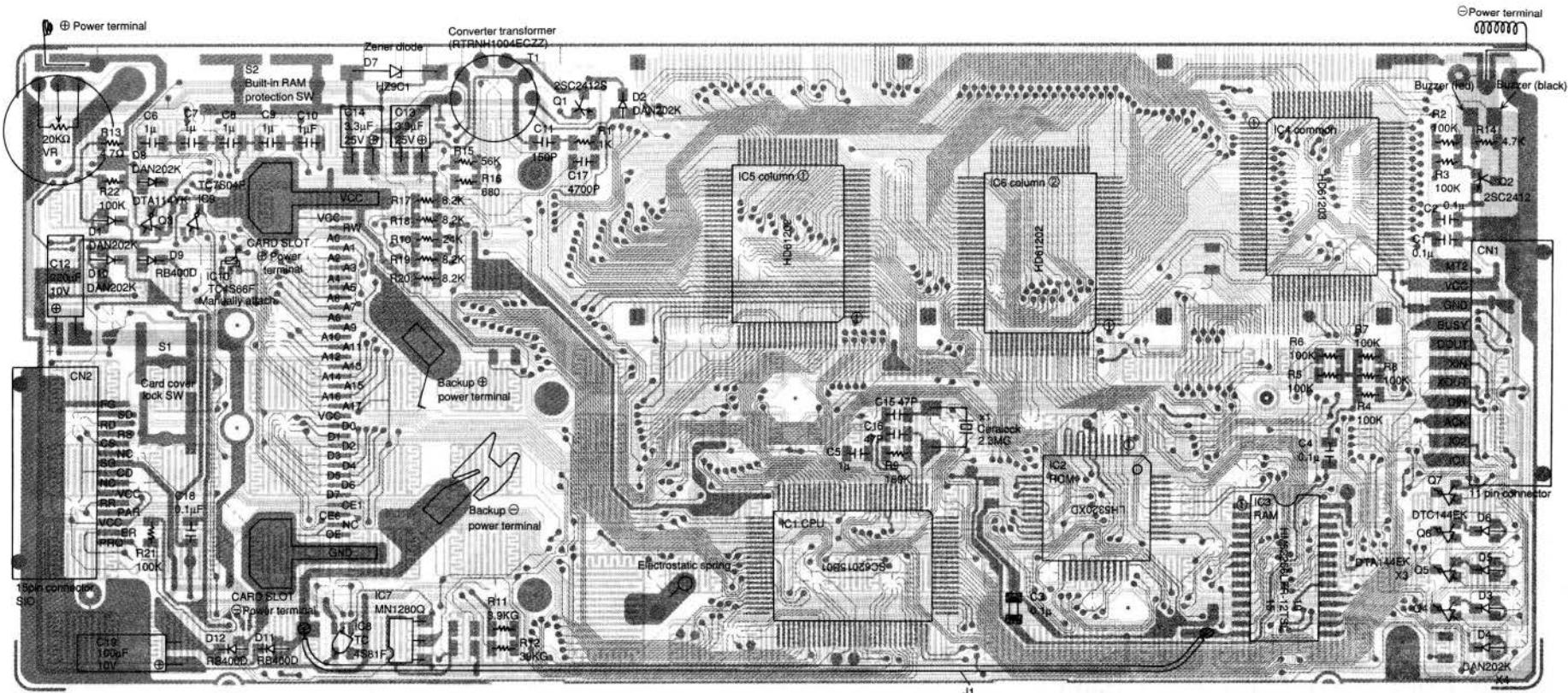
## 12. LCD wiring diagram



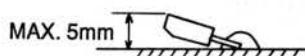
X1 ~ X64 HD61203  
 Y1 ~ Y64 HD61202 ①  
 Y1 ~ Y56 HD61202 ②  
 Symbol LOGIC, ASMBL, TEXT, and Sign are not used in the PC-E500.

## 13. Parts signals arrangement

### 13-1. Parts side

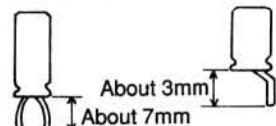


- Solder the IC7 (MN1280Q) without folding its pin as shown in the figure.



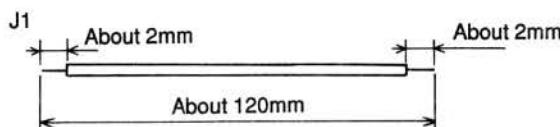
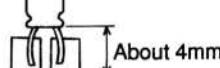
- Electrolytic capacitor

• C12, C19 (220 $\mu$ F)

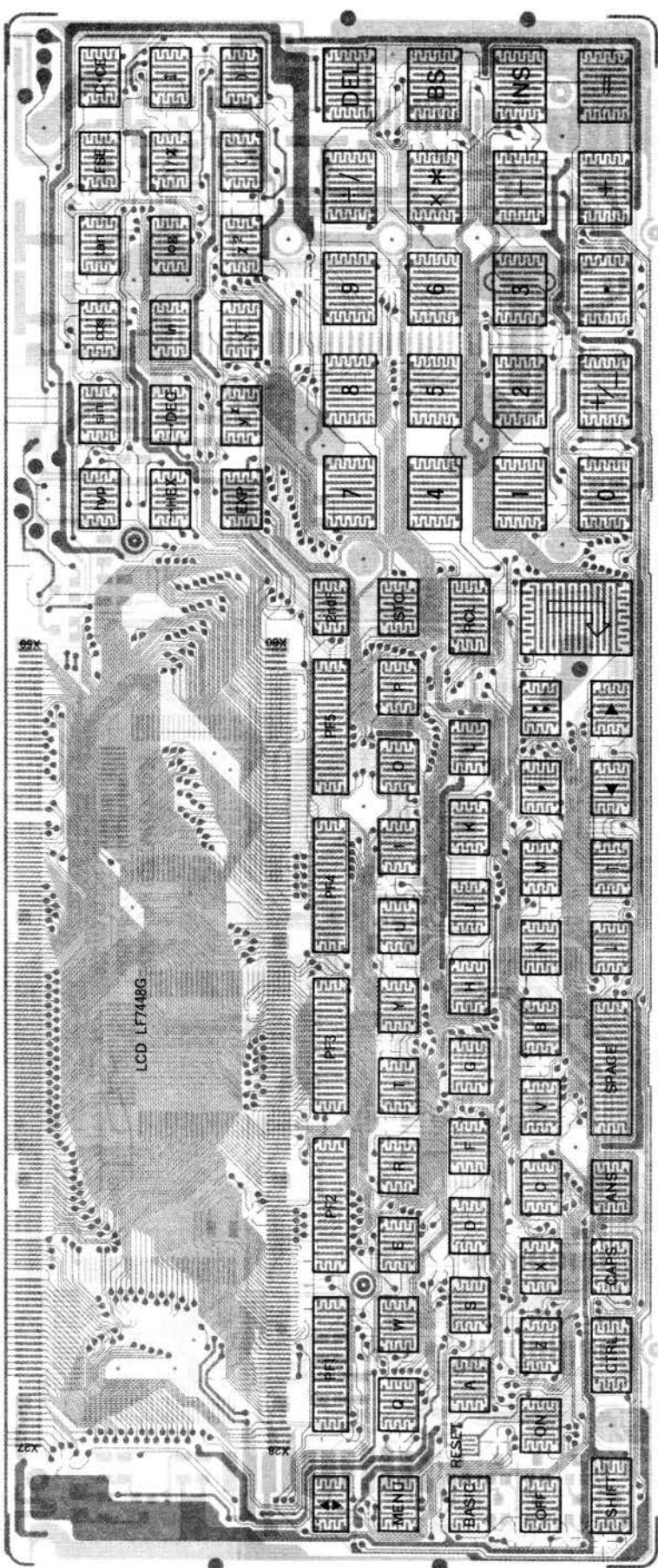


- C13, 14 (3.3 $\mu$ F)

Keep it away from zener diode.



## 13-2. Key side



## 14. Parts

## 1 Ext

NO.	
1	G C
2	G C
3	G F
4	P F
5	P S
6	P G
7	P G
8	C P
9	D U
10	L X
11	P G
12	G F
13	P T
14	Q T
15	Q T
16	Q C
17	M S
18	P T
19	R A
20	P T
21	G C
22	L X
23	L F
24	T C
25	G F
26	L X
28	P C
29	P Z
30	G F
31	L X
32	J K
33	T L
34	P C
35	T L
101	L X

## 2 PW

NO.	
1	D U
2	M S
3	M S
4	P G
5	P S
6	P S
7	P Z
8	Q C
9	Q C
10	Q T
11	Q T
12	Q T
13	Q T
14	Q T
15	R C
16	R C
17	R C
18	R H
19	R T
20	R V
21	V C
22	V C
23	V C
24	V C
25	V H
26	V H
27	V H
28	V H
29	V H
30	V H
31	V H
32	V H
33	V H
34	V H
35	V H
36	V R
37	V R

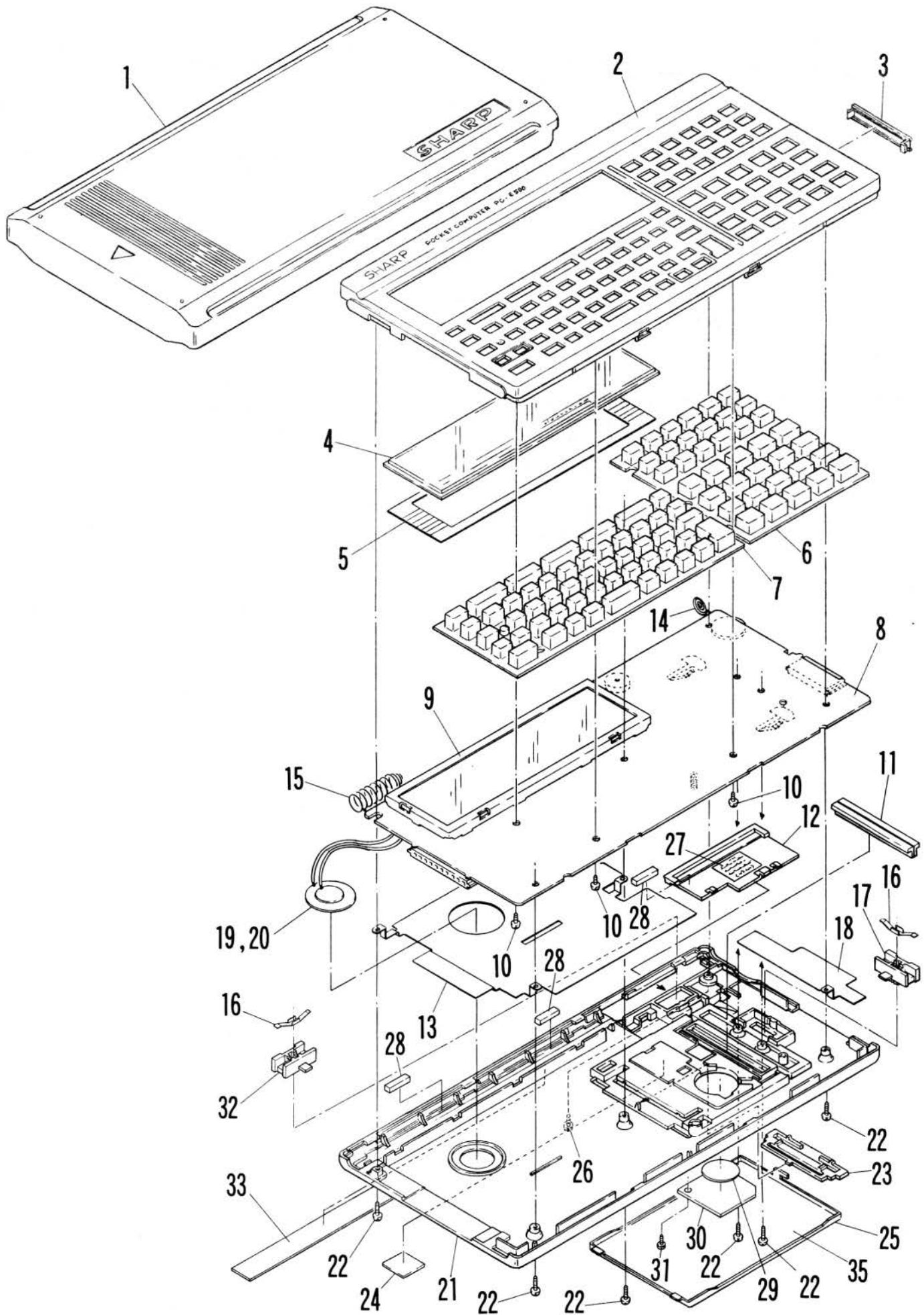
## 14. Parts list & Guide

### 1 Exteriors

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	GCASP1006ECZZ	A G	N	D	Hard case
2	GCABB1047EC03	A L	N	D	Top cabinet
3	GFTAA1287CCSA	A B		D	Connector lid (for 15pin connector)
4	PFILW1010ECZZ	A D	N	D	Acryl filter
5	PSLDP1026ECSA	A C	N	C	Display mask
6	PGUMM1031ECSA	A K	N	B	Key rubber B
7	PGUMM1030ECSB	A M	N	B	Key rubber A
8	CPWBN1079EC02	B X	N	E	PWB unit
9	DUNT-1343ECZZ	A Y	N	E	LCD unit
10	LX-BZ1109CCZZ	A A		C	Screw (2×4.5)
11	PGUMS1549CCZZ	A E		C	PWB card connector
12	GFTAB1015ECZZ	A B	N	D	Battery lid
13	PTPEH1038EC01	A D	N	C	Shield tape A
14	QTANZ1019ECZZ	A B	N	C	Battery terminal $\oplus$
15	QTANZ1021ECZZ	A C	N	C	Battery terminal $\ominus$
16	QCNTM1042CCZZ	A A		C	Slide switch terminal
17	MSLIP1031CC04	A C	N	C	Slider for connector lid
18	PTPEH1039EC01	A B	N	C	Shield tape B
19	RALMB1030CCZZ	A D		B	Buzzer (EFB-S49C02P)
20	PTPEH1213CCZZ	A B		C	Adhesive tape for buzzer
21	GCABA1048EC01	A G	N	D	Bottom cabinet
22	LX-BZ1263CCZZ	A A	N	C	Screw
23	LFIX-1190CCSF	A B	N	C	Fixing plate for card
24	TCAUK1242CCZZ	A A		C	Caution label
25	GFTAU1006ECS	A F	N	D	Card lid
26	LX-BZ1038CCZZ	A A		C	Screw
28	PCUSS1010ECZZ	A A	N	C	Cushion
29	PZETL1046ECZZ	A A	N	C	Insulation sheet for battery
30	GFTAB1306CCZZ	A D		D	Battery cover
31	LX-BZ1024ECZZ	A A	N	C	Screw
32	JKNBZ1225CCZZ	A B		C	Slide switch knob
33	TLABH1266ECZZ	A C	N	D	Battery replacement label A
34	PCUSS1010ECZZ	A A	N	C	Cushion
35	TLABH1267ECZZ	A C	N	D	Battery replacement label B
101	LX-NZ1020CCZZ	A A		C	Nut
					(Attach to the top cabinet)

### 2 PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	DUNT-1343ECZZ	A Y	N	E	LCD unit
2	MSPRC1007ECZZ	A B		C	Card cover spring
3	MSPRC1277CCZZ	A A		C	Connector spring (for 15pin connector)
4	PGUMS1027ECZZ	A B	N	B	Rubber connector
5	PSPAP1011ECZZ	A A	N	C	Insulation spacer
6	PSPAP1289CCZZ	A A		C	Spacer for 11pin connector
7	PZETL1050ECZZ	A A	N	C	Insulation sheet
8	QCNCW1001EC1A	A G		C	Connector (11pin)
9	QCNCW1368CC1E	A M		C	Connector (15pin)
10	QTANZ1019ECZZ	A B	N	C	Battery terminal $\oplus$
11	QTANZ1021ECZZ	A C	N	C	Battery terminal $\ominus$
12	QTANZ1478CCSA	A C		C	Power terminal
13	QTANZ1545CCZZ	A A	N	C	Terminal for memory back up battery $\oplus$
14	QTANZ1557CCZZ	A B	N	C	Terminal for memory back up battery $\ominus$
15	RC-CZD105ECZZ	A C		C	Capacitor ( $1\mu F$ )
16	RC-EZ107AEC1A	A B	N	C	Capacitor (10WV $100\mu F$ )
17	RCRM-1003ECZZ	A D	N	B	Crystal (2.3MHz)
18	RHDZ1001ECZZ	A D	N	B	Diode (RB400D)
19	RTRNH1004ECZZ	A K	N	B	Converter transformer
20	RVR-Z2400QCZZ	A F		B	Variable resistor ( $20K\Omega$ )
21	VCCCTP1HH151J	A A		C	Capacitor (50WV 150PF)
22	VCCCTP1HH470J	A A		C	Capacitor (50WV 47PF)
23	VCEAJU1EW335M	A B	N	C	Capacitor (25WV 3.3 $\mu F$ )
24	VCKYTP1HB472K	A A	N	C	Capacitor (50WV 4700PF)
25	VHDDAN202K/-1	A B		B	Diode (DAN202K)
26	VHEHZ9C1///-1	A B		B	Zener diode (HZ9C1)
27	VHHD61202/-1	A S	N	B	IC (HD61202)
28	VHHD61203/-1	A X		B	IC (HD61203)
29	VHLH5320XH-1	A Y	N	B	IC (LHS320XH)
30	VHIMN1280Q/-1	A E		B	IC (MN1280Q)
31	VHISCB62015B01	B A	N	B	IC (SC62015B01)
32	VHITC4S66F/-1	A C	N	B	IC (TC4S66F)
33	VHITC4S81FTP	A C	N	B	IC (TC4S81FTP)
34	VHITC7S04FTP	A C		B	IC (TC7S04FTP)
35	VH6256LF1XSL	B B	N	B	IC (6256LF1XSL)
36	VRS-TP2BD102J	A A		C	Resistor (1/8W $1.0K\Omega \pm 5\%$ )
37	VRS-TP2BD104J	A A		C	Resistor (1/8W $100K\Omega \pm 5\%$ )



## **2** PWB unit

### **3 Packing material & Accessories**

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**SHARP CORPORATION  
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1989 August Printed in Japan ©