



GE Medical Systems

Technical Publications

2244781

Revision 7

CT/e, CT ProSpeed AI/FI Series Advanced Theory of Operation

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LIST OF EFFECTIVE PAGES

Tab - Section	Page	REV
-	Title page Title page rear	7 blank
(Warning and other important information)	a to d	0
(Revision Information)	A to B	7
1 (System)	i	6
General Description	1-1 to 1-6	3
Subsystem Overview	2-1 to 2-14	6
Power Distribution	3-1 to 3-18	6
Scan Operation	4-1 to 4-5	0
2 (Operator Console)	i	0
General Description	1-1 to 1-5	0
Host Processor	2-1 to 2-4	0
NPR (NP Recon Engine)	3-1 to 3-6	0
DBPCI (DAS Buffer for PCI Bus)	4-1 to 4-6	0
DASIFN95M	5-1 to 5-10	0
Connector Boards	6-1 to 6-6	0

Other OC Components	7-1 to 7-4	0
3 (Table/Gantry)	i	7
General Description	1-1 to 1-3	7
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Functional Description	3-1 to 3-21	7
4 (DAS/Detector)	i	0
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Detector	2-1 to 2-7	0
Data Acquisition System (DAS)	3-1 to 3-19	0
5 (X-ray Generator)	i	2
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General Description - II	2-1 to 2-5	3
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Typical Signals	4-1	1
Functional Description	5-1 to 5-9	0
Software	6-1 to 6-3	3
Exception Handling	7-1 to 7-4	0
-	Blank/Rear cover	-

REVISION HISTORY

REV	Date	Primary Reason for Change	
7	12/21/01	System	-
		Operator Console	-
		Table/Gantry	Minor modification (Sec. 1). Updated the step motor driver descriptions (Sec. 3).
		DAS/Detector	-
		X-ray Generator	-
6	11/01/01	System	Minor modification (Sec. 2, 3).
		Table/Gantry	Minor modification (Sec. 1). Added: Waveforms and test point locations for 4K Table (2297024) (Sec. 3).
5	7/25/01	System	Included the 2297024 Table data (Sec. 2). Included the PDU2 information (Sec. 3)
		Table/Gantry	Included the 2297024 Table information (Sec. 1, 3).
4	12/08/00	Table/Gantry	Added foot switch denomination.
3	8/31/00	System	Adopted the new revision control for Sec 1, 2, 3.
		Table/Gantry	Adopted the new revision control for Sec. 1, 2, 3.
		X-ray Generator	Adopted the new revision control for Sec. 2, 6.
2	5/31/00	-	A correction to Table Gantry Section; delete Foot Switch and Touch Sensor information.
1	2/25/00	-	A correction to XG section; 200VPDU note; 1 mm Slice; System block diagram.
0	11/18/99	-	Initial release.

SYSTEM

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SECTION 1 - GENERAL DESCRIPTION

1-1 INTRODUCTION

The features of this CT (Computed Tomography) system, one of the ProSpeed AI/FI series CT scanners, include the following:

- Workstation type information processing system,
- Solid-state x-ray intensity detector,
- Continuous rotation type gantry with slip rings and high frequency coupling.

This CT system is comprised of the following main components (called subsystems):

- Operator Console (called OC)
- Scanning Gantry (called gantry)
This subsystem further includes the following subsystems:
 - DAS/Detector
 - X-ray Generator (called XG)
- Patient Table (called table)
- Power Distribution Unit (called PDU)

The system may include some of the following customer option equipments:

- Advantage Windows Image Workstation
- Image Camera

1-2 SYSTEM OVERVIEW

Illustration 1-1 shows the system block diagram.

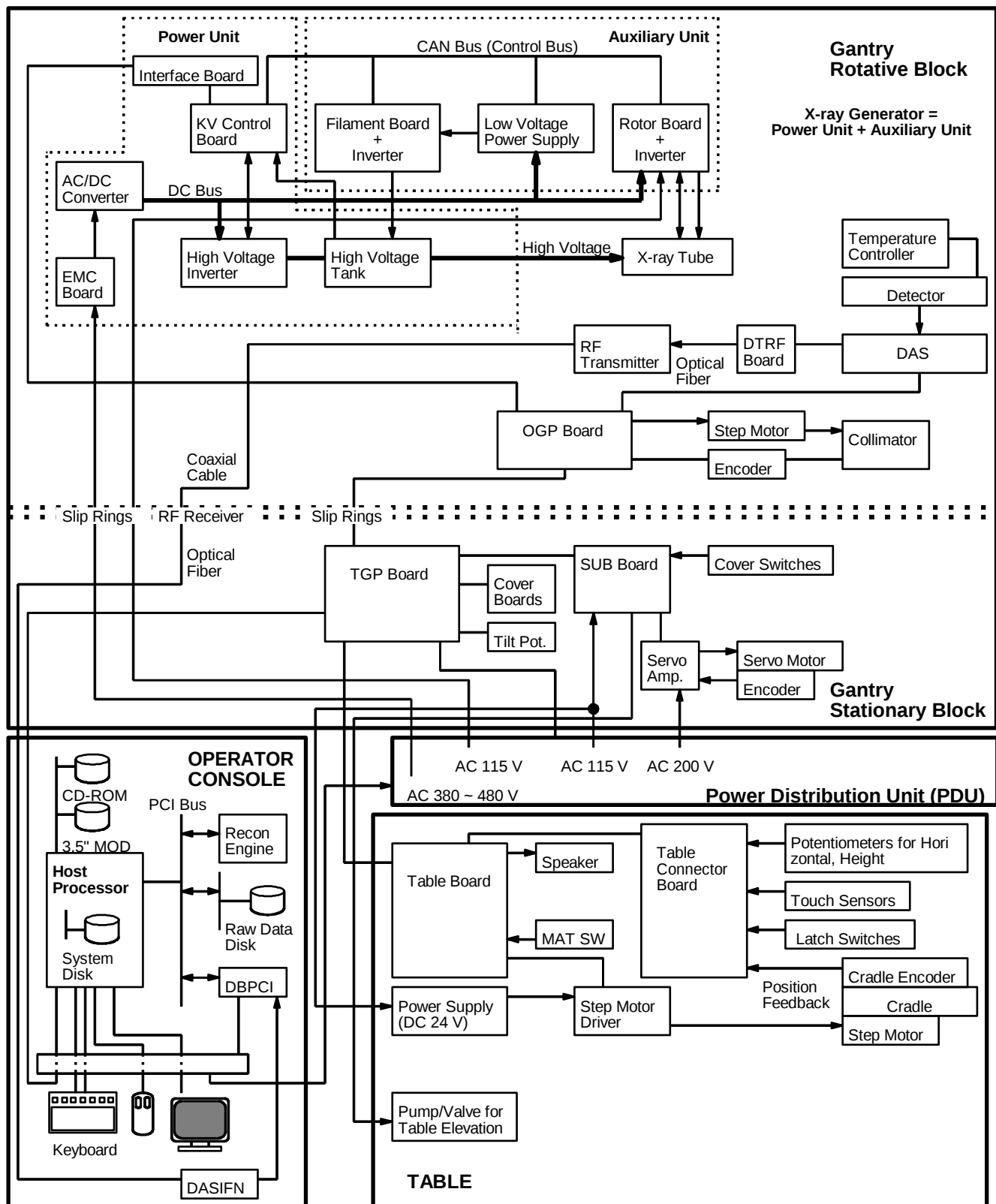
The operator console (OC) controls the entire system, according to the operator's operations. The OC sends instructions to the processor of the TGP board, which then controls the gantry and table subsystems according to the instructions.

The TGP board processor also passes the OC instructions to the processor of the OGP board which is equipped on the gantry rotative frame. The OGP board controls the DAS subsystem, the collimator aperture, or positioning lights according to the passed instructions.

The OGP board processor also passes the instructions from the TGP board to the processor of the x-ray generator subsystem. The XG processor controls the x-ray generator according to the instructions (originally from the OC).

Reversely, the OC receives status information from the TGP board or other processors (via the TGP board).

Illustration 1-1 System Block Diagram



1-3 SYSTEM SPECIFICATIONS AND DATA

The following tables describe system specifications and data.

Table 1-1 Scan Time

Scan Time [sec]	
Standard	with 1.0 sec Scan Option
-	-
-	0.7 (Half scan)
1.0 (Half scan)	1.0
1.5	1.5
2.0	2.0
3.0	3.0
5.0	5.0

Table 1-2 Scan/Recon/Cal FOV

Scan/Recon FOV	Cal FOV
P-Head (18)	Small (25)
Head (25)	Small (25)
Body (43)	Large (43)

Table 1-3 Image Spatial Resolution Related

No. of Actual Scan Views		No. of Detector Active Channels	Recon Matrix
Full Scan	Half Scan		
972	635	685	512 X 512 320 X 320 256 X 256

1-3 SYSTEM SPECIFICATIONS AND DATA (CONTINUED)

Table 1-4 KV-MA Stations

KV	MA
120	20, 30, 40, ..., 180, 190, 200 (in 10 mA increments)
140	20, 30, 40, ..., 140, 150, 160 (in 10 mA increments)

Table 1-5 Slice Thickness

Slice Thickness [mm]
(1), 2, 3, 5, 7, 10

Table 1-6 Other Specifications

Exposure Start Angle (Axial Scan)
Head & Posteriafossa Studies: 90/270 deg. Other Studies: 0/180 deg.

1-4 SYSTEM OPTIONS

Table 1-7 Main System Options

Category		Name	Description
Scan/Recon	High speed scan	• Fast Scan 1.0 sec	-
	Helical scan	• 30 Slice Helical	-
	High speed recon	• Fast Recon	Speeds up recon time from 6 sec to 4 sec.
Storage Device	Main memory for Host processor	• 256 MB	-
	Magnetic optical disk drive (MOD)	• MOD	5" MOD
Filming	Laser camera	• Analog interface • Digital interface	-
Network	Ethernet	• Advantage Windows	-
Software		• 3D Imaging • Denta Scan	-
Collimator		• 1 mm Slice	-

SECTION 2 - SUBSYSTEM OVERVIEW

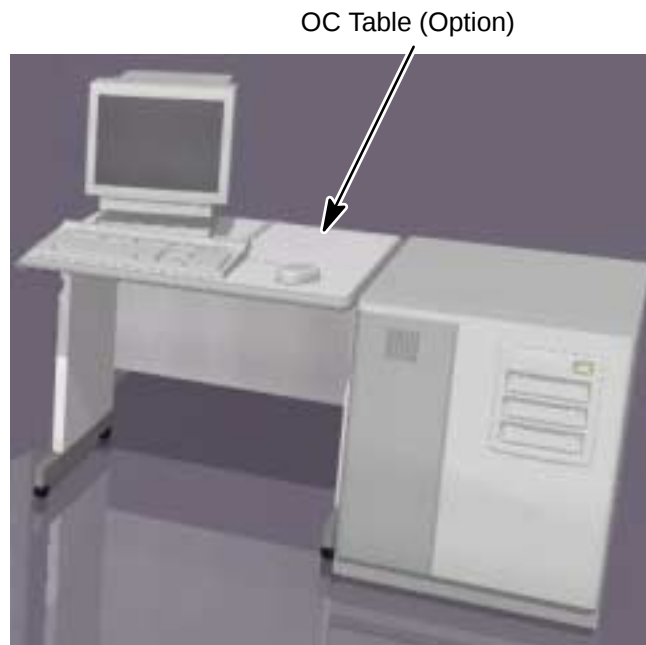
2-1 OPERATOR CONSOLE (OC)

The OC controls the entire CT system.

The OC performs information processings, and interfaces between the operator and the system.

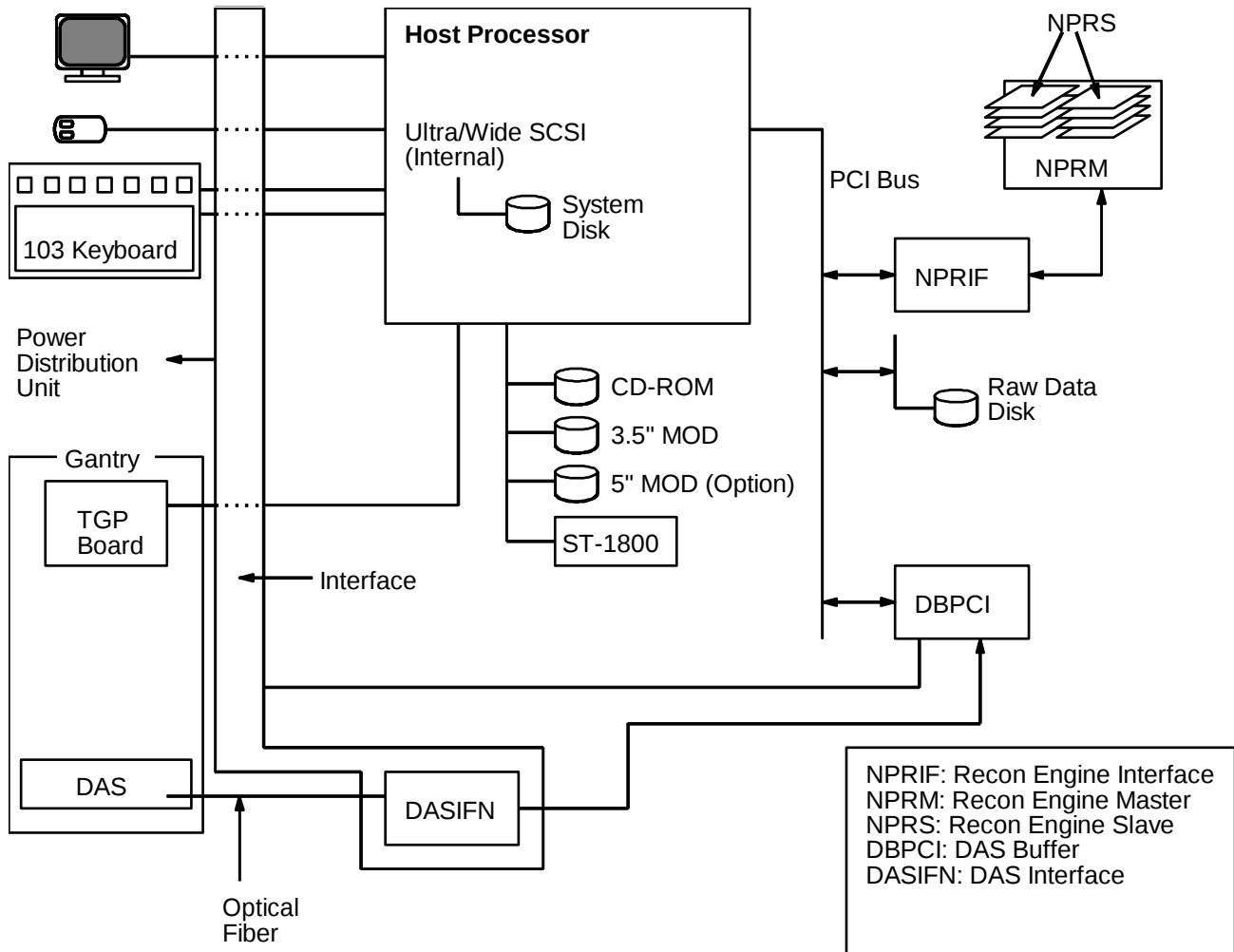
Illustration 2-2 shows a block diagram of the OC.

Illustration 2-1 Operator Console



2-1 OPERATOR CONSOLE (CONTINUED)

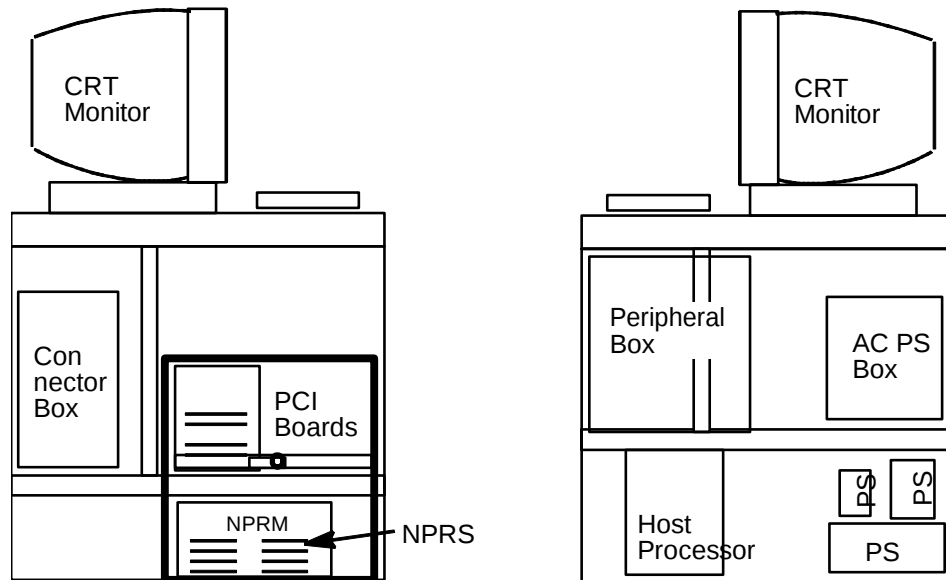
Illustration 2-2 OC Block Diagram



2-1 OPERATOR CONSOLE (CONTINUED)

The hardware for data processings is based on the PCI bus architecture and can be divided into several hardware blocks shown and described in Illustration 2-3 and Table 2-1.

Illustration 2-3 OC Hardware Blocks



2-1 OPERATOR CONSOLE (CONTINUED)

Table 2-1 Data Processing Blocks

Hardware Block	Main Component	Description
Host Processor	Central Processor, Main Memory, I/O Controller, Graphics Processor, Audio Processor	Includes also one PCI slot.
	System Hard Disk Drive	Stores system and application software, and images. Also stores calibration files and system parameters.
Peripheral Box	Raw Data Hard Disk Drive	Raw data is stored to this high-speed disk while scans are performed.
	5" MOD Drive	Archives images.
	3.5" MOD Drive	Archives raw data files. Used also during system software loading.
	CD-ROM Drive	Loads system software.
PCI Boards	NPRIF Board	Performs interfaces between the PCI bus and the NPRM board.
	DBPCI Board	Functions as a DAS data buffer.
NPR (Recon Engine) (Functionally, this block also includes NPRIF of the PCI Board Nest)	NPRM Board	Operates as a master; connected to the NPRIF board by cables.
	NPRS Boards	Operate as slaves; equipped on the NPRM board.
Connector Box	DASIFN Board	Receives DAS data from the gantry.
Operator-machine Interface	CRT	17 inch color monitor; 512 x 512 matrix image display
	Keyboard, Mouse, (Trackball)	The keyboard includes 'Scan Set' button, 'Scan' button, etc.

2-2 GANTRY

Illustration 2-4 Gantry and Table



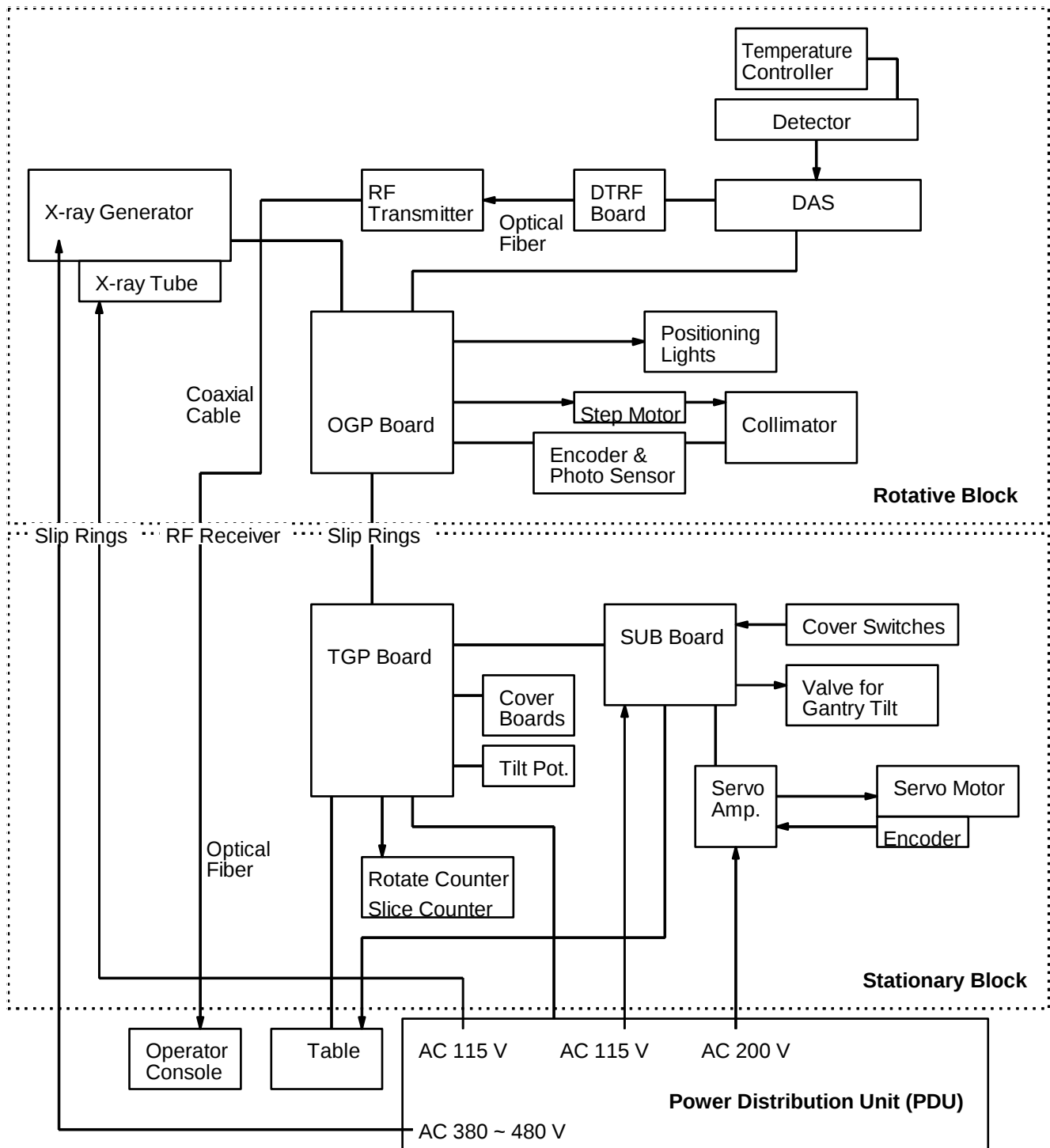
Illustration 2-5 shows a block diagram of gantry electrics.

The gantry subsystem includes the following main components/subsystems:

- X-ray generator
- DAS/Detector
- Collimator
- Axial motor:
This motor rotates the gantry rotational block, on which, x-ray tube, x-ray generator, DAS/Detector, OGP board, or collimator are installed, during axial scans.
- TGP (Table and Gantry Processor) board
This board controls the whole gantry/table subsystems; this board receives instructions from the operator console (OC), performs gantry/table mechanical controls, communicates with the OGP board, and send status information to the OC.
- OGP (On Gantry Processor):
This board controls the operations of components equipped on the gantry rotational block, such as x-ray generator, DAS/Detector, collimator, or positioning lights.

2-2 GANTRY (CONTINUED)

Illustration 2-5 Block Diagram of Gantry Electrics



2-2 GANTRY (CONTINUED)

Gantry Tilt

- As described in Table 2-2, the gantry hydraulic pump and cylinders can tilt the gantry ± 20 deg. from vertical.

Slip & RF Rings

These are used for power and signal transmission between the rotational and stationary assemblies of the gantry.

- Power rings (total: 6): AC 115 V (2 P), AC 380 ~ 480 V (3 P), GND
Signal rings (total:6): DAS TRIG, Tx, Rx
RF ring (1 Ch.): DAS data; DAS data are transmitted by high frequency (Radio Frequency) coupling.

Collimator

The collimator assembly consists of a removable bow-tie filter, and an aperture assembly.

The filter adjusts the intensity distribution of the x-ray beam to a proper shape.

The aperture regulates x-ray beam width to a slice thickness of 2 mm, 3 mm, 5 mm, 7 mm, or 10 mm at the ISO center.

Detector Temperature Control

The detector includes a heater to warm itself. The heater is powered by a DC 24 V supply, and this supply is on/off controlled by the temperature controller to keep the detector at a specified temperature. The controller includes a microprocessor which controls the power to the heater, with a feedback from a thermistor equipped on the detector.

2-2 GANTRY (CONTINUED)

Table 2-2 shows several gantry specifications and data.

Table 2-2 Specifications and Data

Item	Specifications or Data
Gantry Aperture	650 mm
Height of ISO Center	900 mm
Focus to Aperture (Collimator surface) Distance	179.6 mm
Focus to ISO Distance	541.0 mm
Focus to Detector (Scinti surface) Distance	949.075 mm
Tilt Range [deg.]	Fwd 20.0 ~ Bwd 20.0 (0.5 deg. increments)
Gantry Pulses	15552 pulses/rotation
X-ray Tube Park Position	at one o'clock position

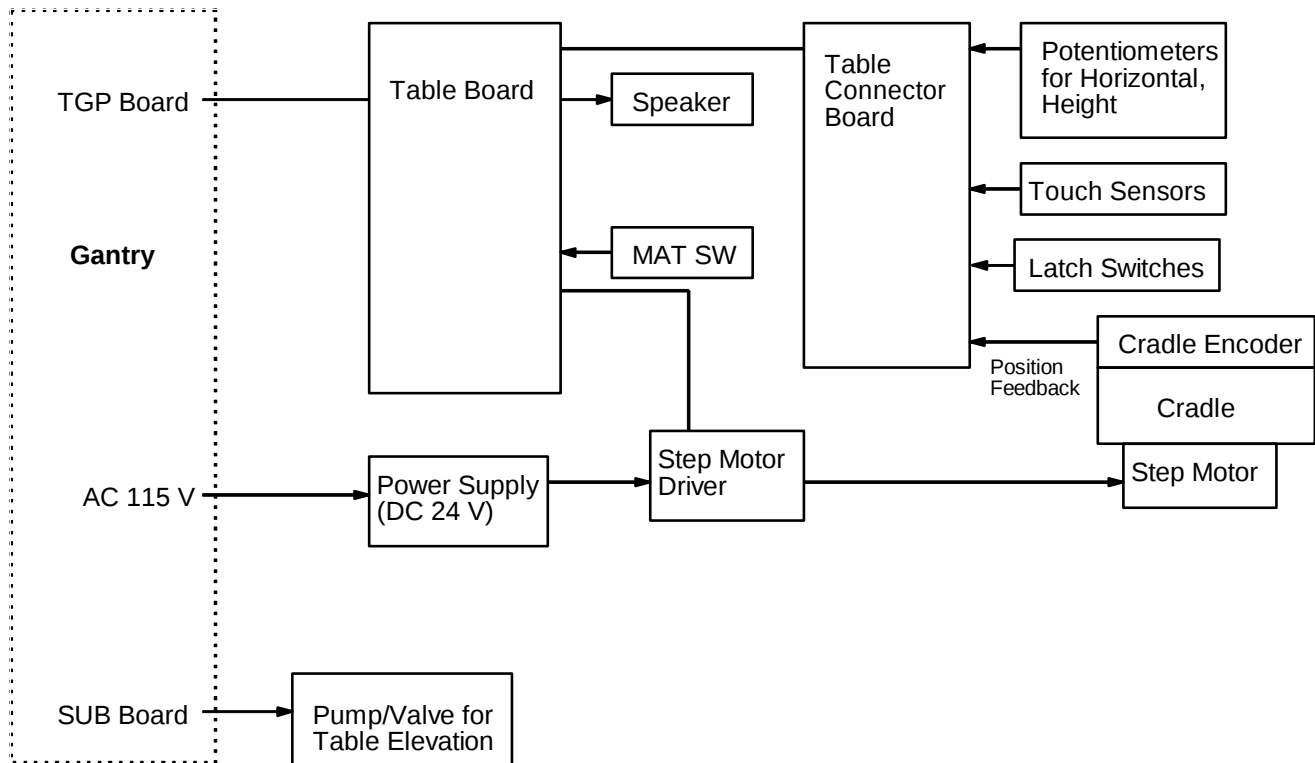
2-3 TABLE

A step motor moves the cradle in the longitudinal direction (In/Out) and the hydraulic pump and cylinder raises/lowers (Up/Down) the table.

Buttons on the gantry control the table/cradle operations. The cradle also moves under the OC control during scout scan, Table Set, or axial scan intervals.

Illustration 2-6 shows a block diagram of table electronics.

Illustration 2-6 Block Diagram of Table Electronics



2-3 TABLE (CONTINUED)

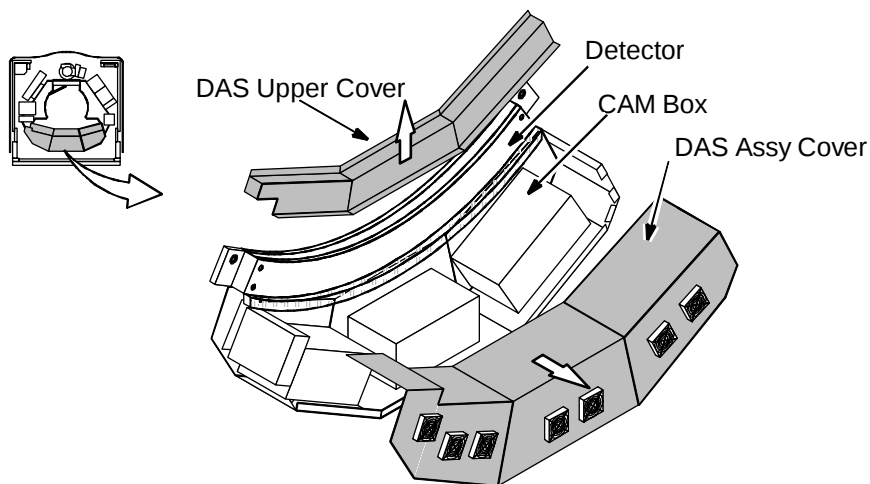
Table 2-3 shows several table specifications and data.

Table 2-3 Specifications and Data

Item	Specifications or Data
Weight	(For Table 2244226-x (called YMS Table)) Approximately 245 kg (For Table 2297024 (called 4K Table)) Approximately 305 kg
Elevation Range	400 ~ 900 (Height of ISO) mm
Cradle Material	metalfree
Maximum Cradle Travel	1520 mm
Cradle Travel Speed	75.0 mm/sec
Scannable Range (using Cradle Extender); See below.	1190 mm (at -140 mm down from ISO)
Scannable Range: When the cradle (equipped with an extender) is fully extended, the distance between the farthest end of the cradle extender and the scan plane is called Scannable Range.	

2-4 DAS/DETECTOR

Illustration 2-7 DAS/Detector



Detector

The detector converts the x-ray beam intensities it receives to electric signals.

The detector is mainly composed of a number of Detector Modules. A detector module includes a scintillator which emits lights when there are incident x-rays on it, and a photo diode which generates electric currents when it receives lights. The generated electric currents are fed to CAM boards contained in the DAS.

- Channel pitch: 1.15 mm, 0.06946 deg.
- Scintillator material: Lumex Crystal
- Photo diode type: Planer type Si diode

Table 2-4 Number of Detector Channels

Channel	Number
Detector Modules	45
Active Channels	685
Reference Channels	10 + 10
Q-cal Channels	3
Ground Channels	3 + 3 + 6

2-4 DAS/DETECTOR (CONTINUED)

DAS

The Data Acquisition System (DAS) charges the electric currents from the detector, then converts them to voltage signals, digitizes them, and transfers the data to the operator console via RF coupling and serial communication lines.

The CIF board, which is one of the components of the DAS subsystem, includes a microprocessor. This microprocessor communicates with the OGP board installed on the gantry rotational block, and controls the overall DAS operations.

- Output Data: 0 ~ 523744

2-5 X-RAY GENERATOR

The x-ray generator is directly installed on the gantry rotative structure.

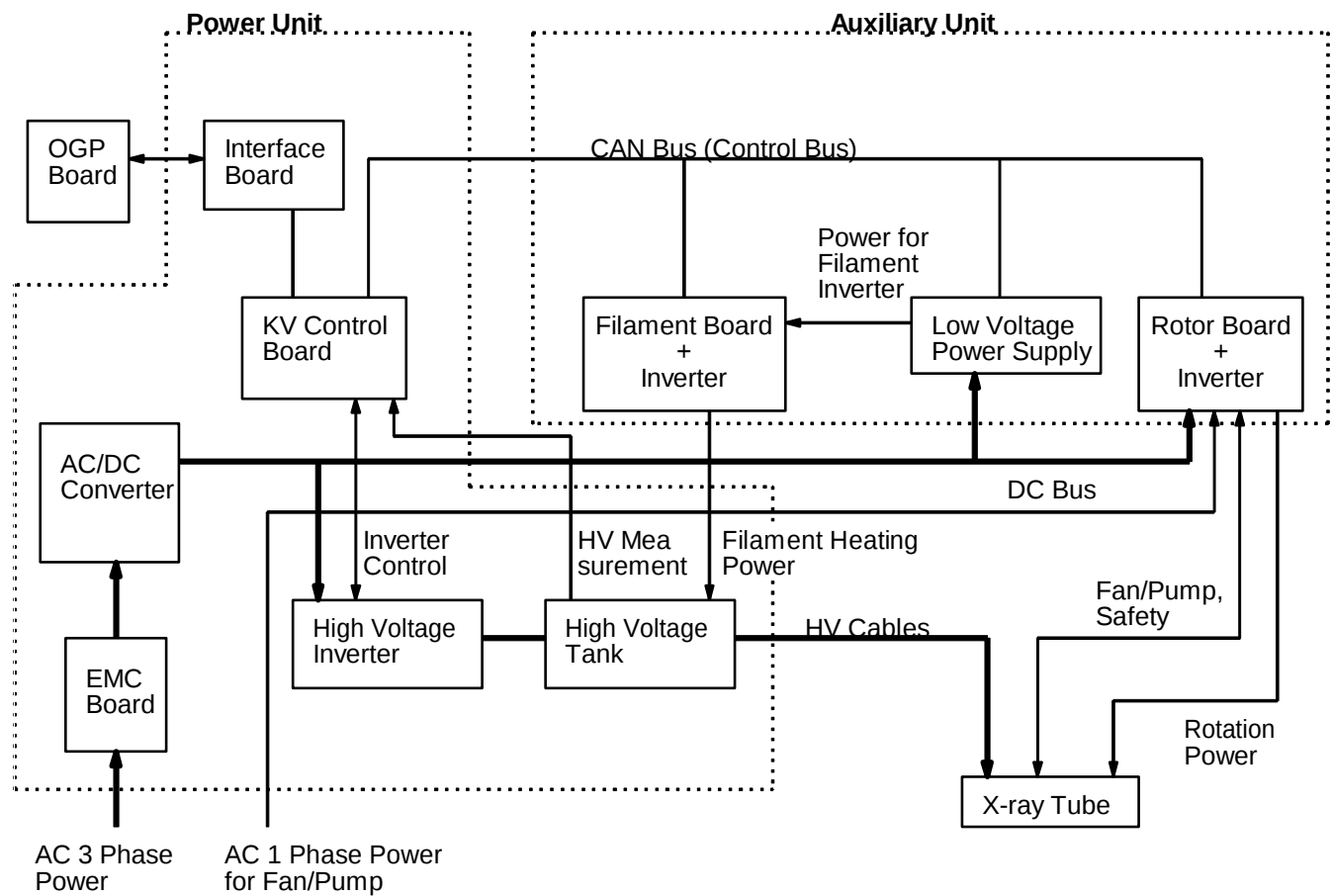
The x-ray generator supplies DC high voltage power to the x-ray tube to generate x-rays.

The generator includes circuit boards for filament current control, X-ray tube rotor control, and KV control/overall control of the generator operations. It also includes a high voltage tank and inverters for high frequency power, rotor power, and filament power.

Illustration 2-8 shows a block diagram of the x-ray generator subsystem. As shown, the generator is physically comprised of two units: Power Unit and Auxiliary Unit.

The KV Control Board includes a processor which controls the generator operations and communicates with the OGP Board.

Illustration 2-8 X-ray Generator



2-5 X-RAY GENERATOR (CONTINUED)

X-ray Tube

Table 2-5 shows main characteristics of the x-ray tube.

Table 2-5 X-ray Tube (CTMX 135) Main Characteristics

Characteristic	Specification
Focus Size	IEC 336 W: 0.7 mm L: 0.6 mm
Fan (X-ray) Beam Angle	> 62 deg.
Al Equivalent Filtration	1.0 mm
Anode Heat Capacity	2.0 MHU
Anode Cooling Rate	500 kHU/min.
Housing Cooling Rate	275 kHU/min.
Rotor Speed	8000 rpm

SECTION 3 - POWER DISTRIBUTION

Note

PDU stands for Power Distribution Unit. There exist two types of PDUs: either one of the two is used for CT/e, CT ProSpeed AI, or FI system. In this section, abbreviations **PDU1** and **PDU2** are used to distinguish one from the other, as follows:

PDU2: Its part No. is 2298849 (400 V) or 2298852 (200 V).

PDU1: Its part No. is 2247557-x (400 V) or 2247554-x (200 V).

3-1 POWER DISTRIBUTION UNIT (FOR PDU1)

Note

For PDU2, see Section 3-2, Power Distribution Unit (for PDU2).

The power distribution unit (PDU) provides powers to all the subsystems.

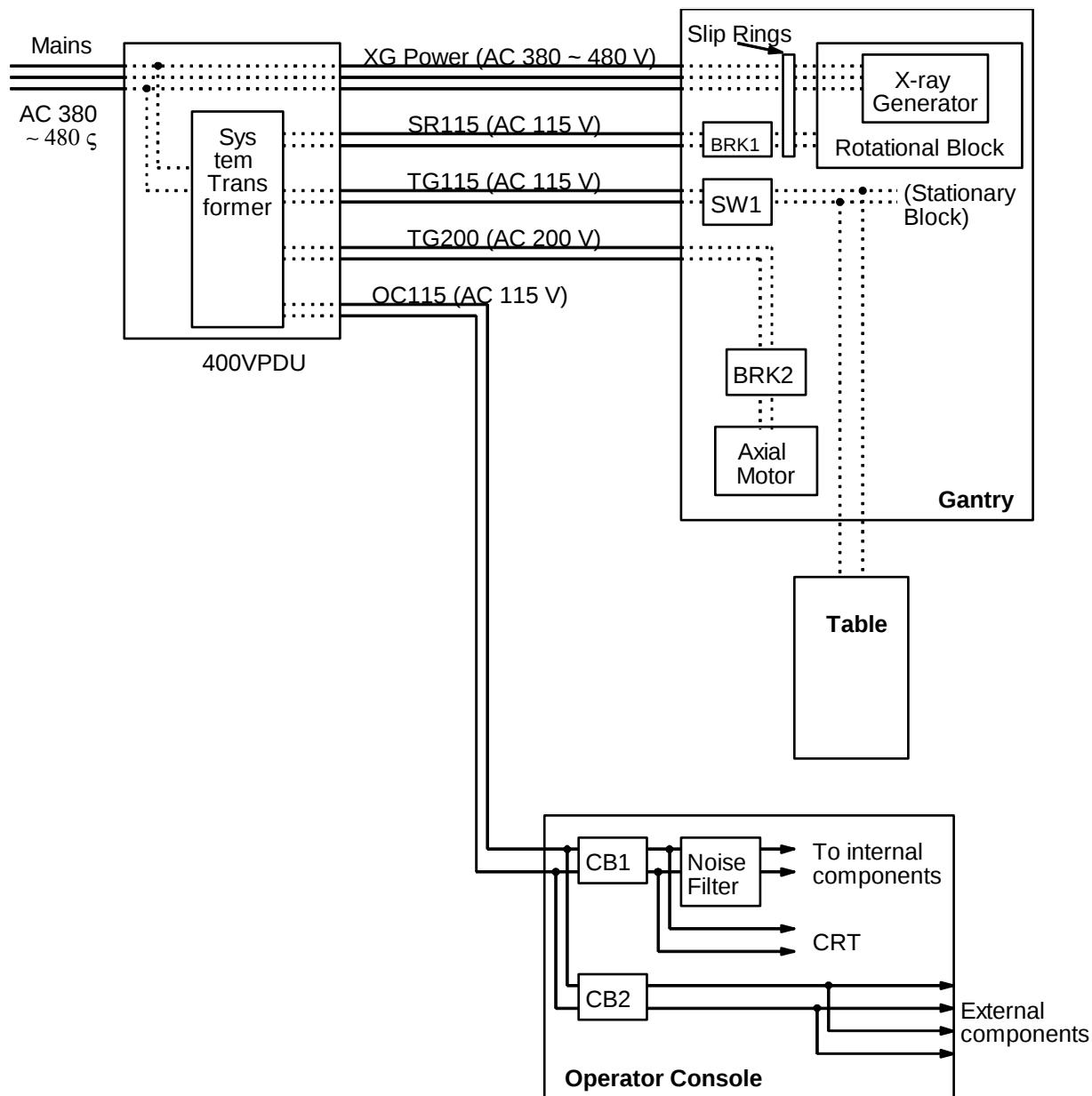
Two types of PDUs are available: 400VPDU and 200VPDU. Either one of two types is used according to the mains voltage (main power from the power distribution box of sites). (200VPDUs are used in Japan only.)

See Illustration 3-1 (400VPDU) or 3-2 (200VPDU). These illustrations describe the following:

- All the powers except 'XG Power' are output from the system transformer on the PDU. (200VPDUs generate 'XG Power' by a step-up transformer.)
- 'XG Power' powers the x-ray generator (XG) equipped on the gantry rotational block. Powers for x-ray tube high voltage, x-ray tube anode rotation, XG control circuit boards, etc. are derived from this power. However, the fan and pump for the x-ray tube are powered by 'SR115.'
- 'SR115' powers all the components equipped on the gantry rotational block except the x-ray generator.
- 'TG115' powers all the components equipped on the gantry stationary block except the axial motor. The gantry tilt pump also is operated by this power. 'TG115' also powers the table subsystem.
- 'TG200' powers the axial motor which rotates the gantry rotational block.
- 'OC115' supplies power to the operator console.

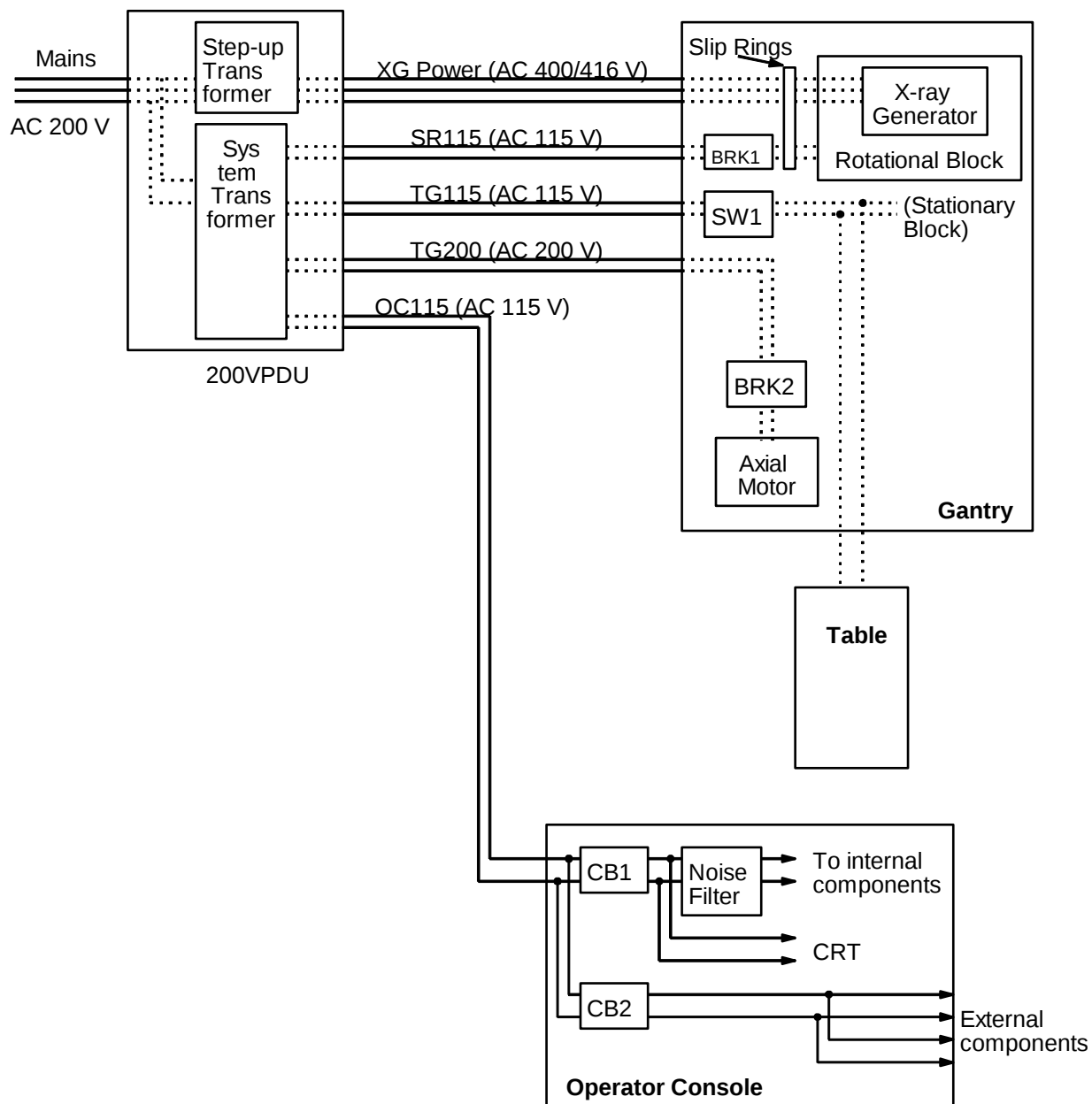
3-1 POWER DISTRIBUTION UNIT (FOR PDU1) (CONTINUED)

Illustration 3-1 Power Distribution to Subsystems (400VPDU)



3-1 POWER DISTRIBUTION UNIT (FOR PDU1) (CONTINUED)

Illustration 3-2 Power Distribution to Subsystems (200VPDU)



3-1 POWER DISTRIBUTION UNIT (FOR PDU1) (CONTINUED)

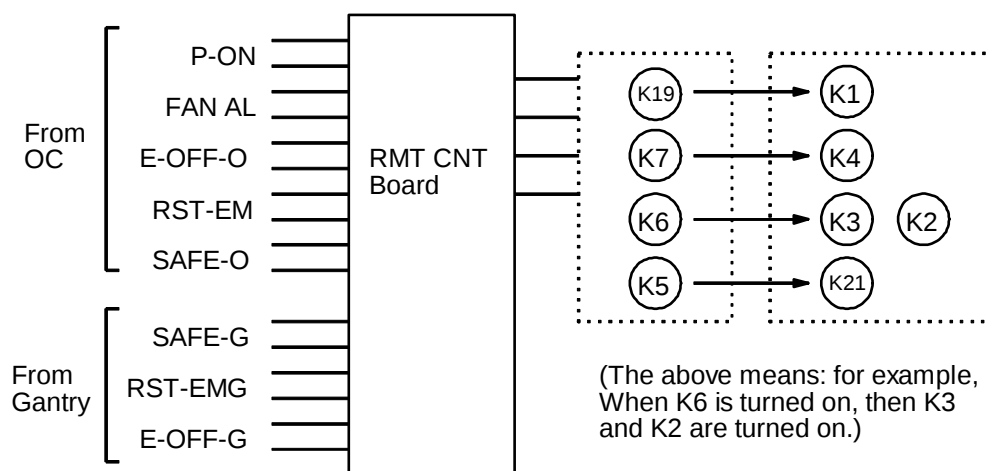
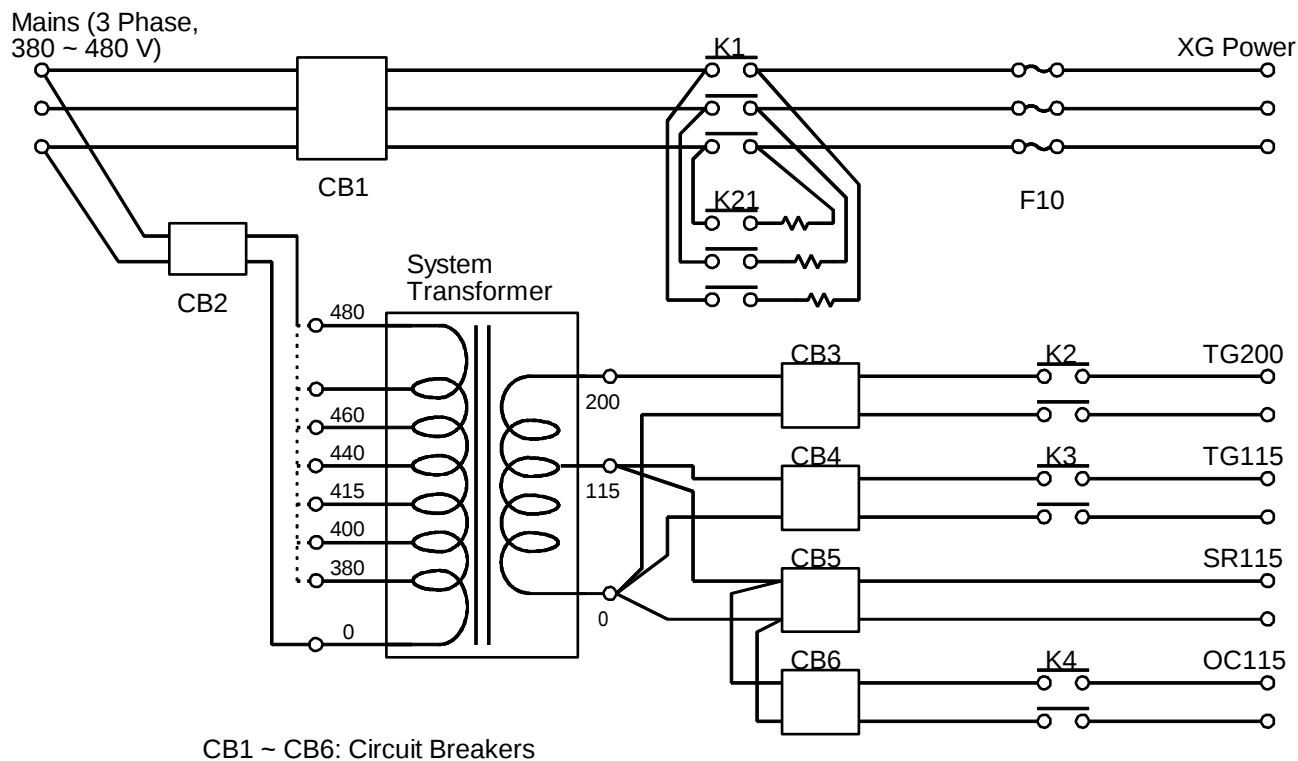
Illustration 3-3 (400VPDU) or 3-4 (200VPDU) shows the simplified circuit diagram of the PDU.

As shown;

- **(400VPDU):**
The voltage of mains power should be within a range of 380 V ~ 480 V. The system transformer provides terminals for 380 V, 400 V, ... , 480 V to connect power to the nearest voltage terminal.
- **(200VPDU):**
The system transformer provides a terminal for 200 V to connect the mains power.
- The 'SR115' output is not controlled by any relay contacts; the power is always present in the CT system unless circuit breakers CB2 or CB5 are turned off.
- The RMT CNT board contains relays which turn on/off K5, K6, K7, or K19 according to signals from the operator console and gantry.
- The relay K1 is turned on some delay time later after K21 is turned on.
The resistors connected to the relay K21 suppress rush currents.
- Circuit breakers CB1, CB2, ... , CB6 can turn OFF powers, as written below:
 - CB1: XG Power
 - CB2: TG200, TG115, SR115, OC115
 - CB3: TG200
 - CB4: TG115
 - CB5: SR115
 - CB6: OC115

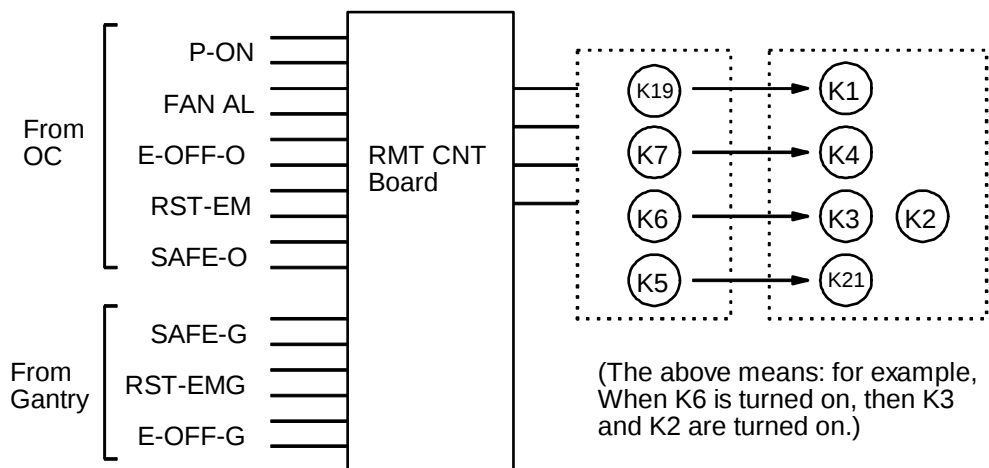
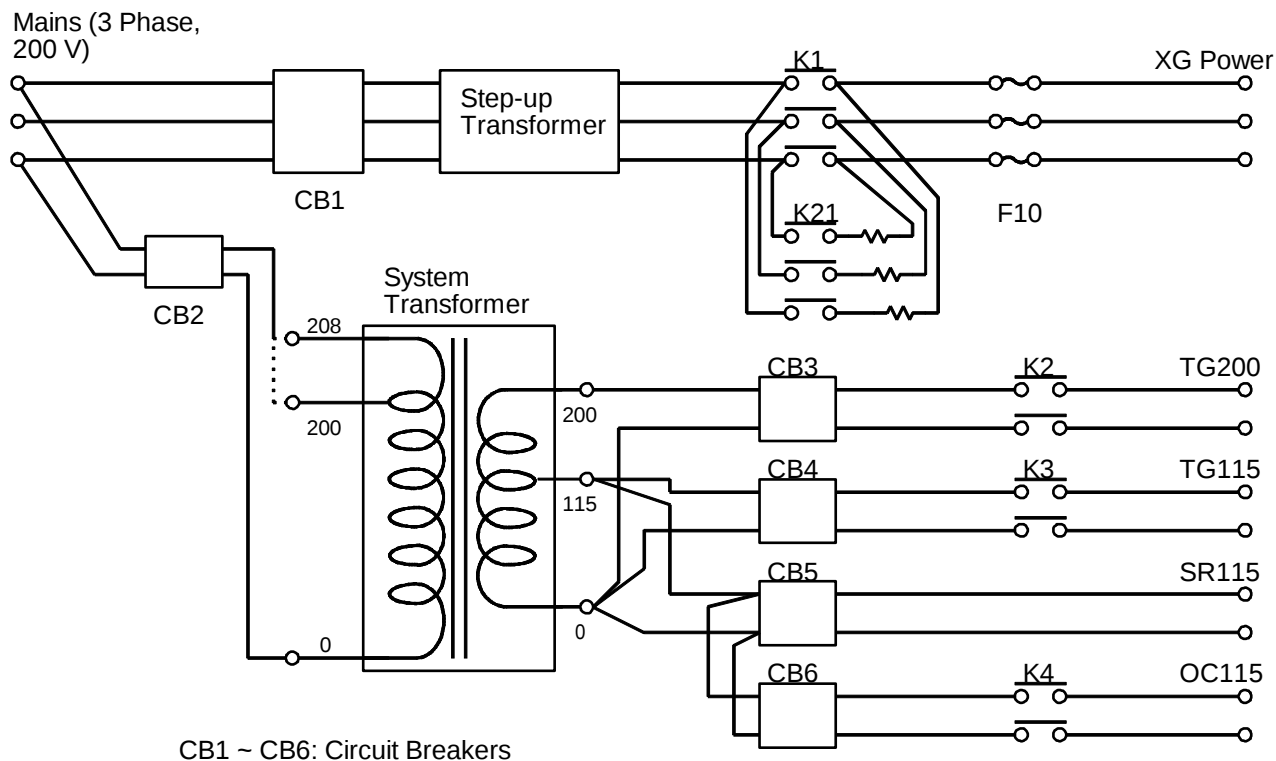
3-1 POWER DISTRIBUTION UNIT (FOR PDU1) (CONTINUED)

Illustration 3-3 Inside of PDU (400VPDU)



3-1 POWER DISTRIBUTION UNIT (FOR PDU1) (CONTINUED)

Illustration 3-4 Inside of PDU (200VPDU)



3-1 POWER DISTRIBUTION UNIT (FOR PDU1) (CONTINUED)

3-1-1 Power On/Off Timing Chart

The power on/off controls of 'XG Power', 'TG200', 'TG115', etc. shown in Illustration 3-1 or 3-3 (or, 3-2 or 3-4, for 200VPDU) are shown in Illustration 3-5.

In the illustration;

'E-OFF' turns 'close' or 'open' when either 'E-OFF-O' or 'E-OFF-G' turns 'close' or 'open.'

That 'Safety Loop' turns 'close' or 'open' means the system safety loop is closed or opened, including both 'SAFE-O' and 'SAFE-G' turns 'close' or 'open.' (See the 'Safety Loop' (3-3) description)

'Reset Emergency' turns 'close' or 'open' when either 'RST-EM' or 'RST-EMG' turns 'close' or 'open.'

Illustration 3-5 describes the following:

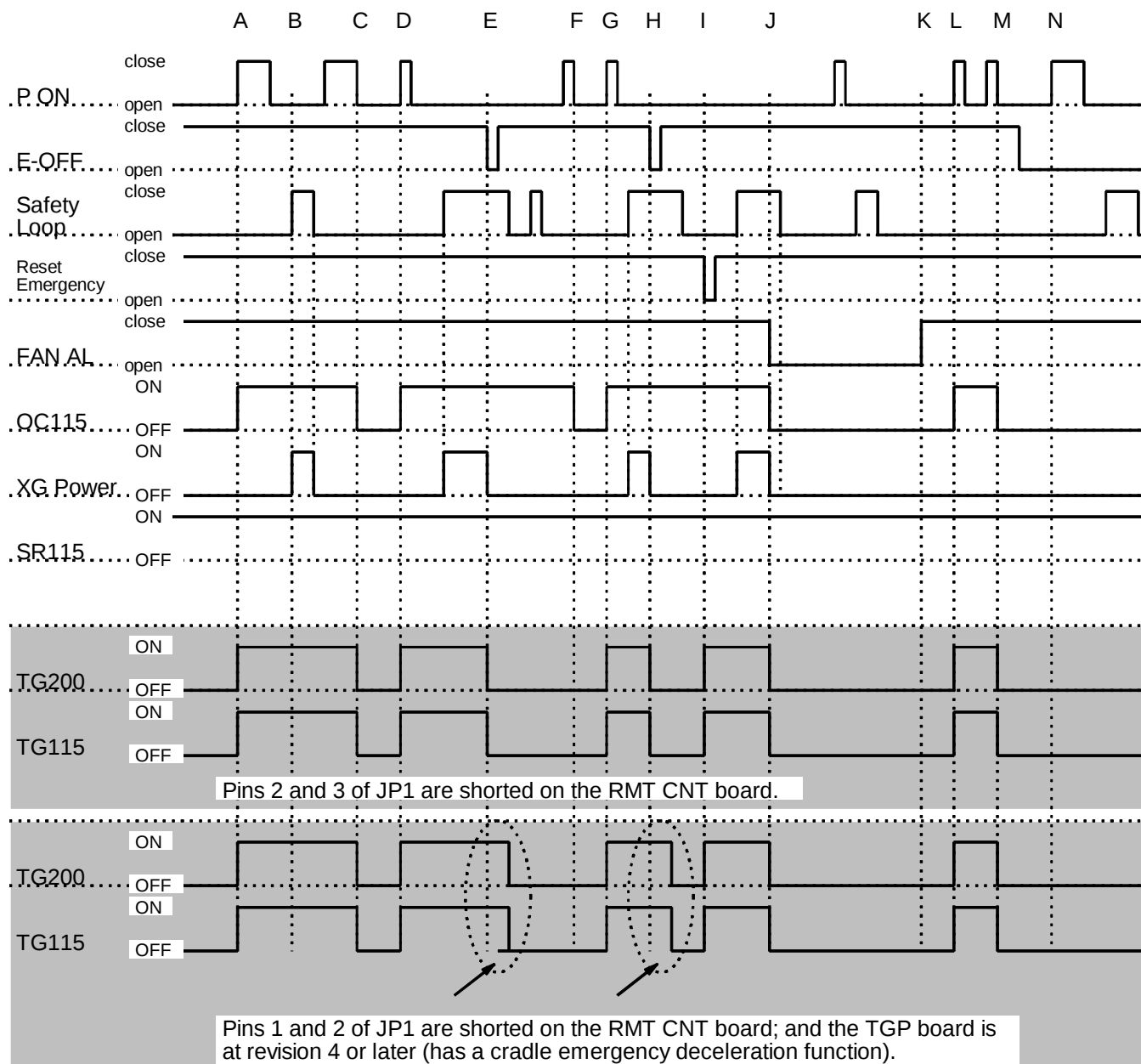
- Timing B:
Only when 'Safety Loop' turns 'close', 'XG Power' turns ON.
- Timing E:
When 'E-OFF' turns 'open', 'XG Power', 'TG200', and 'TG115' turn OFF; however, 'OC115' remains ON.

If pins 1 and 2 of JP1 are shorted on the RMT CNT board and the TGP board is at revision 4 or later (has a cradle emergency deceleration function), 'TG200' and 'TG115' turn OFF 0.4 sec ~ 0.5 sec later after 'E-OFF' turns 'open'; during this period, the cradle is decelerated to a halt.

- Timing I:
When 'Reset Emergency' turns 'open', 'TG200' and 'TG115' are brought to ON.
- Timing J:
When 'FAN AL' turns 'open', 'XG Power', 'TG200', 'TG115' and also 'OC115' all turn OFF.

3-1 POWER DISTRIBUTION UNIT (FOR PDU1) (CONTINUED)

Illustration 3-5 Power On/Off Timing Chart



Note

'Safety Loop' is always closed in normal conditions after the system is switched ON or reset; this means that 'XG Power' is always supplied to the gantry in normal conditions.

3-2 POWER DISTRIBUTION UNIT (FOR PDU2)

Note

For PDU1, see Section 3-1, Power Distribution Unit (for PDU1).

The power distribution unit (PDU) provides powers to all the subsystems.

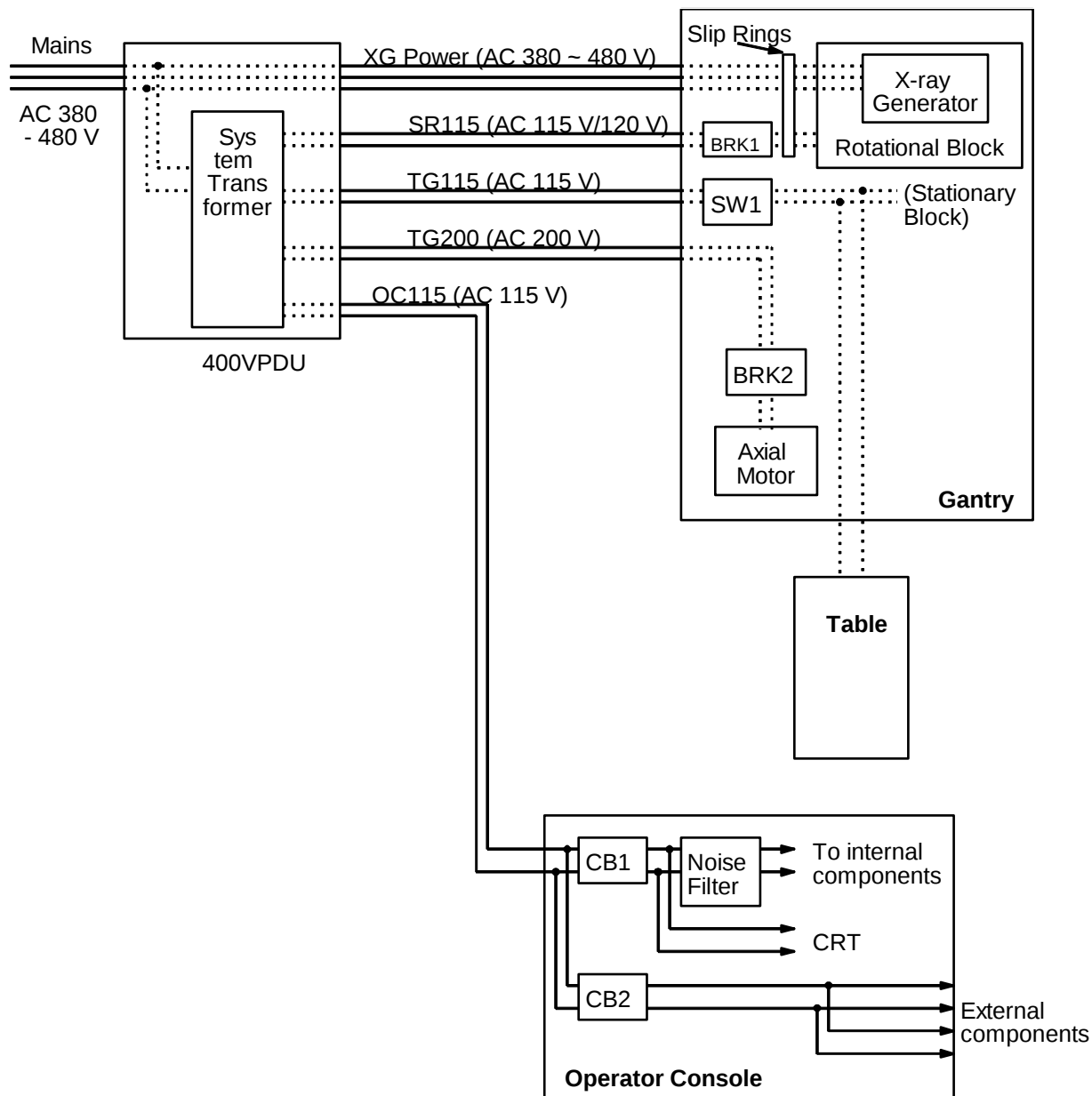
Two types of PDUs are available: 400VPDU and 200VPDU. Either one of two types is used according to the mains voltage (main power from the power distribution box of sites). (200VPDUs are used in Japan only.)

See Illustration 3-6 (400VPDU) or 3-7 (200VPDU). These illustrations describe the following:

- All the powers except 'XG Power' are output from the system transformer on the PDU. (200VPDUs generate 'XG Power' by a step-up transformer.)
- 'XG Power' powers the x-ray generator (XG) equipped on the gantry rotational block. Powers for x-ray tube high voltage, x-ray tube anode rotation, XG control circuit boards, etc. are derived from this power. However, the fan and pump for the x-ray tube are powered by 'SR115.'
- 'SR115' powers all the components equipped on the gantry rotational block except the x-ray generator.
- 'TG115' powers all the components equipped on the gantry stationary block except the axial motor. The gantry tilt pump also is operated by this power. 'TG115' also powers the table subsystem.
- 'TG200' powers the axial motor which rotates the gantry rotational block.
- 'OC115' supplies power to the operator console.

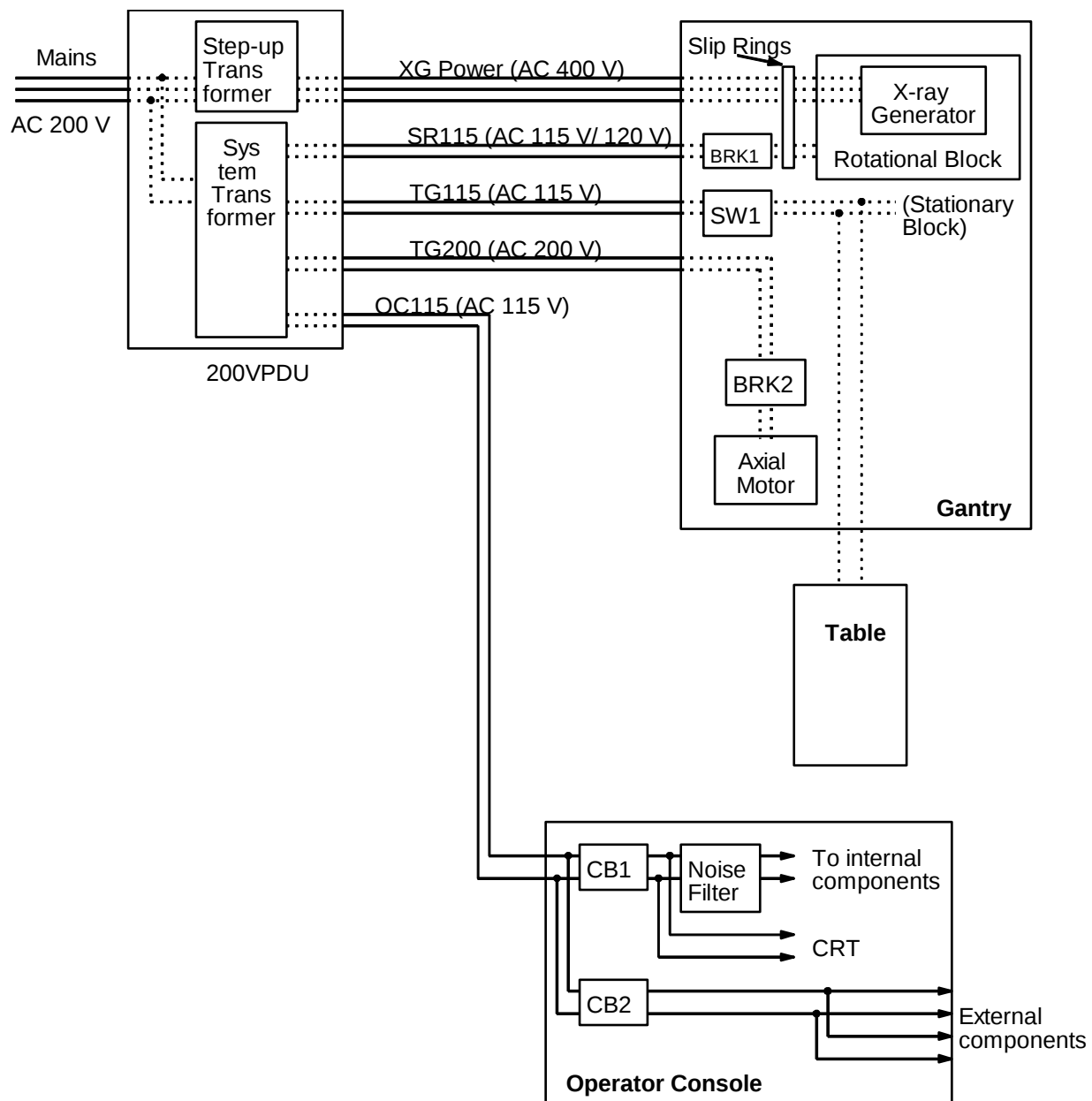
3-2 POWER DISTRIBUTION UNIT (FOR PDU2) (CONTINUED)

Illustration 3-6 Power Distribution to Subsystems (400VPDU)



3-2 POWER DISTRIBUTION UNIT (FOR PDU2) (CONTINUED)

Illustration 3-7 Power Distribution to Subsystems (200VPDU)



3-2 POWER DISTRIBUTION UNIT (FOR PDU2) (CONTINUED)

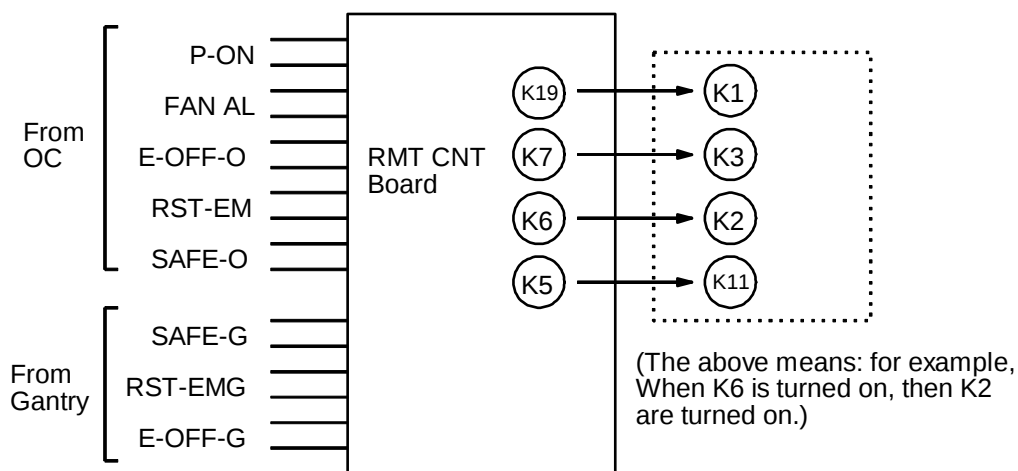
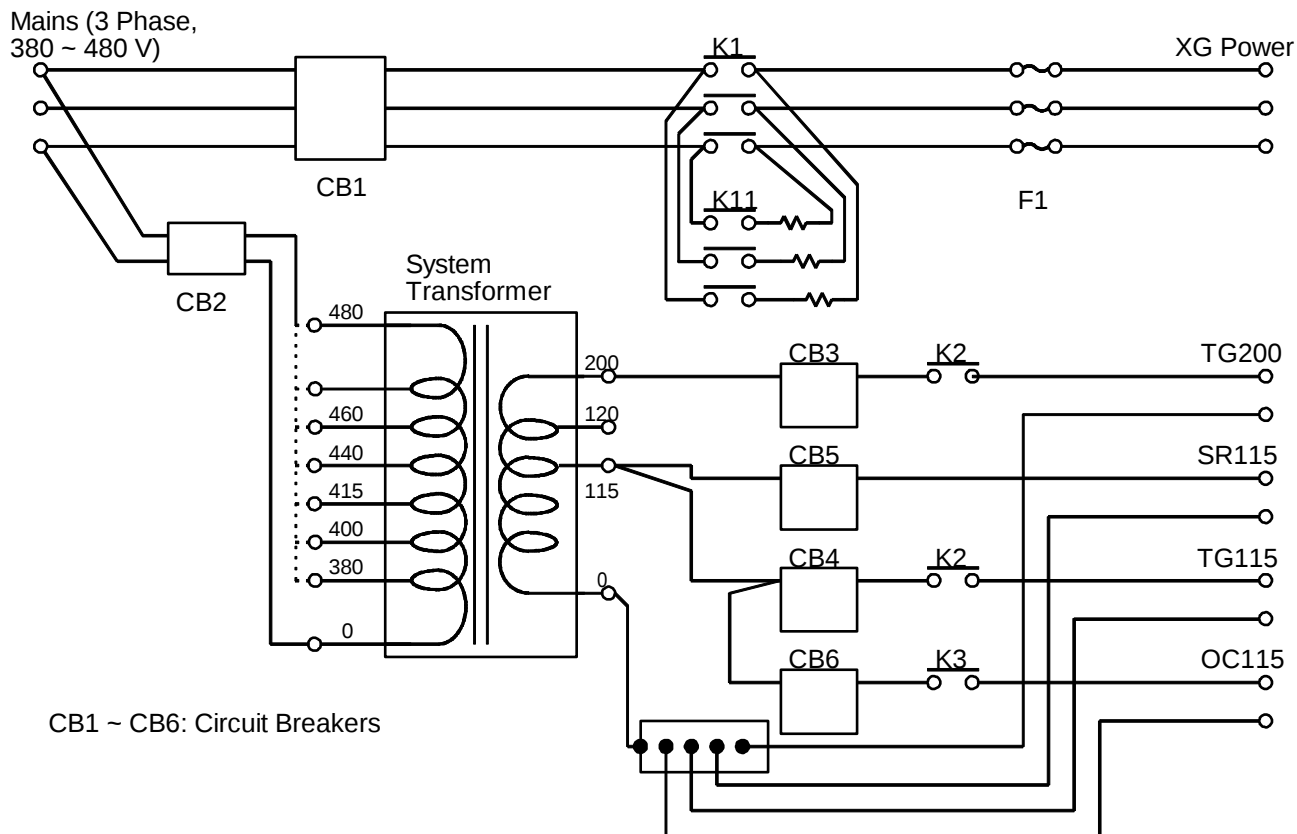
Illustration 3-8 (400VPDU) or 3-9 (200VPDU) shows the simplified circuit diagram of the PDU.

As shown;

- **(400VPDU):**
The voltage of mains power should be within a range of 380 V ~ 480 V. The system transformer provides terminals for 380 V, 400 V, ... , 480 V to connect power to the nearest voltage terminal.
- **(200VPDU):**
The system transformer provides a terminal for 200 V to connect the mains power.
- The 'SR115' output is not controlled by any relay contacts; the power is always present in the CT system unless circuit breakers CB2 or CB5 are turned off.
- The relay K1 is turned on some delay time later after K11 is turned on.
The resistors connected to the relay K11 suppress rush currents.
- Circuit breakers CB1, CB2, ... , CB6 can turn OFF powers, as written below:
 - CB1: XG Power
 - CB2: TG200, TG115, SR115, OC115
 - CB3: TG200
 - CB4: TG115
 - CB5: SR115
 - CB6: OC115

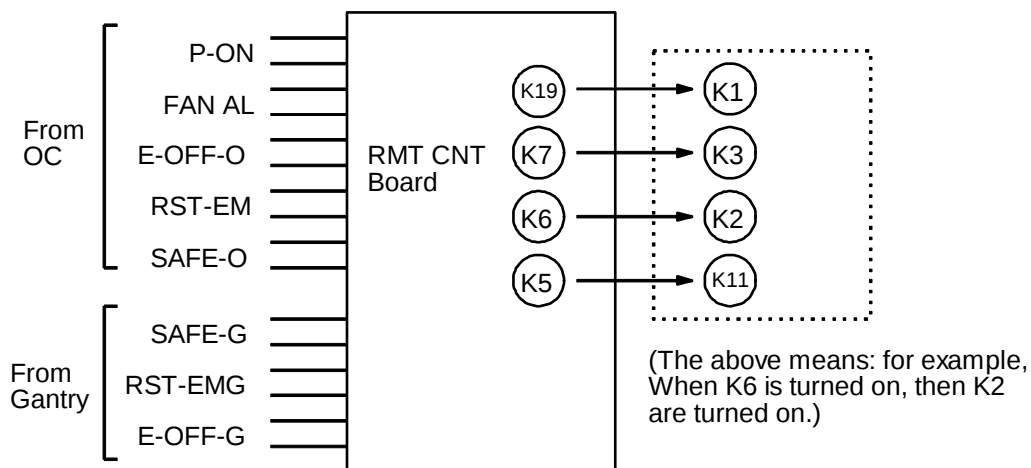
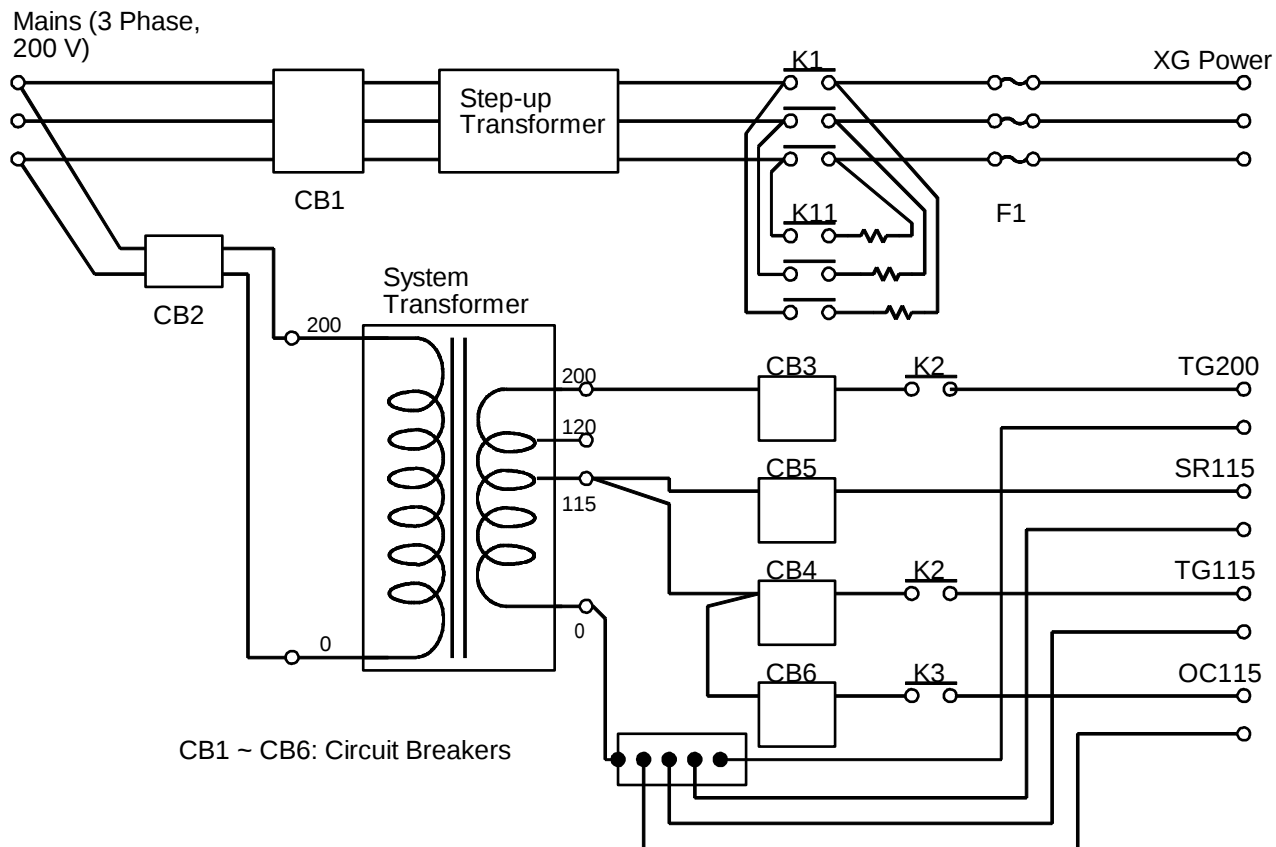
3-2 POWER DISTRIBUTION UNIT (FOR PDU2) (CONTINUED)

Illustration 3-8 Inside of PDU (400VPDU)



3-2 POWER DISTRIBUTION UNIT (FOR PDU2) (CONTINUED)

Illustration 3-9 Inside of PDU (200VPDU)



3-2 POWER DISTRIBUTION UNIT (FOR PDU2) (CONTINUED)

3-2-1 Power On/Off Timing Chart

The power on/off controls of 'XG Power', 'TG200', 'TG115', etc. shown in Illustration 3-6 or 3-8 (or, 3-7 or 3-9, for 200VPDU) are shown in Illustration 3-10.

In the illustration;

'E-OFF' turns 'close' or 'open' when either 'E-OFF-O' or 'E-OFF-G' turns 'close' or 'open.'

That 'Safety Loop' turns 'close' or 'open' means the system safety loop is closed or opened, including both 'SAFE-O' and 'SAFE-G' turns 'close' or 'open.' (See the 'Safety Loop' (3-3) description)

'Reset Emergency' turns 'close' or 'open' when either 'RST-EM' or 'RST-EMG' turns 'close' or 'open.'

3-2 POWER DISTRIBUTION UNIT (FOR PDU2) (CONTINUED)

Illustration 3-10 Power On/Off Timing Chart

INPUT Control

PON SW

E-OFF

Safety-Loop

RESET Emer

FAN ALA

OUTPUT Control

OC115(K3)

XG400(K1)

Resistor(k11)

Timer1(Smart Gantry)

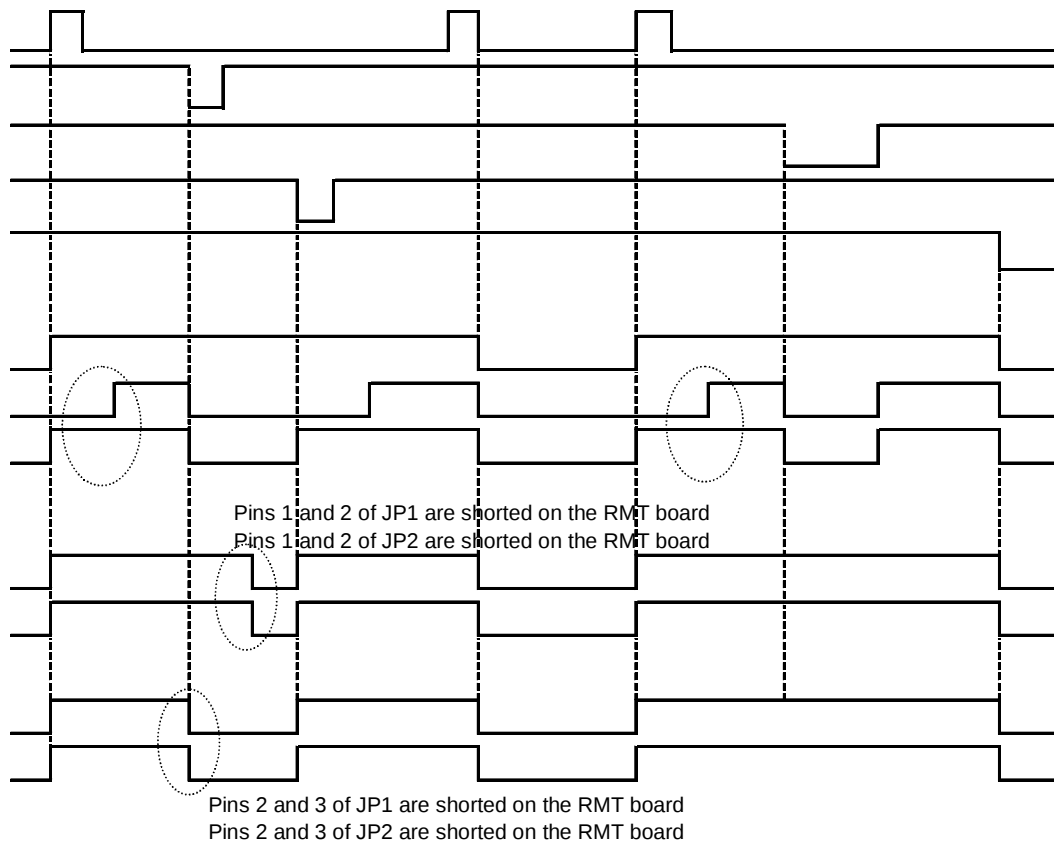
TG115(K2)

TG200(K2)

Timing2(general)

TG115(K2)

TG200(K2)



Note

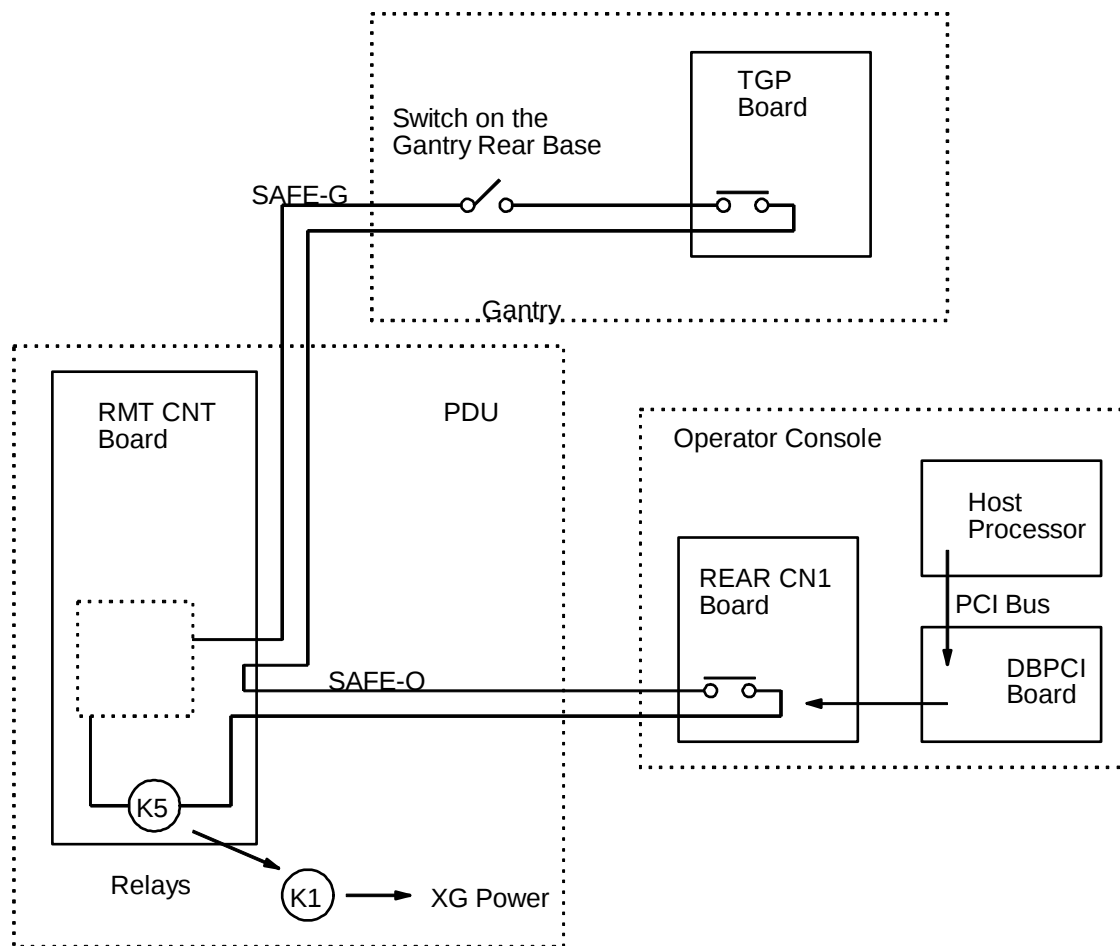
'Safety Loop' is always closed in normal conditions after the system is switched ON or reset; this means that 'XG Power' is always supplied to the gantry in normal conditions.

3-3 SAFETY LOOP

Illustration 3-11 shows a diagram of the system safety loop.

As shown, components on the gantry rotational block are not involved in the safety loop.

Illustration 3-11 Safety Loop



3-3 SAFETY LOOP (CONTINUED)

Open of Safety Loop

The safety loop can be opened by any of the following:

- Switch equipped on the gantry rear base.
- Control by the TGP board:
The TGP board opens the safety loop in any of the following cases:
 - When the TGP board receives from the OGP board a safety loop open demand due to an overtime of x-ray exposure.
 - When the TGP board detects abnormal communication with the OGP board or the operator console (host processor) during x-ray exposure.
- Control by the host processor (i.e., system software):
The host processor opens the safety loop in any of the following cases:
 - When the host processor receives a safety loop open demand from the TGP board.
 - When the host processor detects an overtime of x-ray exposure.
 - When the host processor detects an extra scan (other than scans which the host processor instructed the TGP board to perform) performed.
- Control by the DBPCI board:
While an x-ray exposure is performed, the board opens the safety loop to terminate the exposure if the board detects that the host processor does not normally respond to interrupts issued by the board.
- Signals such as 'E-OFF', 'FAN AL', etc.

SECTION 4 - SCAN OPERATION

4-1 WARM-UP SCANS

The system requires the 'Warm-up' scans to warm-up the x-ray tube just after power-on and prior to starting the first scan, or when more than three hours have elapsed since the last scan.

The warm-up scans also have to be performed before performing phantom calibration which updates the calibration files (CAL files), if more than three hours have elapsed since the last scan.

The following scans are performed during the warm-up scan sequence.

Table 4-1 Warm-up Scans

Scan	Scan Parameter	No. of Scans
for x-ray tube warming	Axial, 2.0 sec, 120 kV, 80 mA, 2 mm	(Until the anode heat level reaches 5.0%.)
	Axial, 2.0 sec, 120 kV, 100 mA, 2 mm	(Until the anode heat level reaches 13.0%.)
	Axial, 2.0 sec, 120 kV, 200 mA, 2 mm	(Until the anode heat level reaches 48.0%.)
for data collection	Axial, 43 FOV, 1.0 sec, 120 kV, 200 mA, 10 mm	1
	Axial, 25 FOV, 3.0 sec, 120 kV, 60 mA, 10 mm	1
	Axial, 25 FOV, 1.0 sec, 120 kV, 60 mA, 10 mm	1

The first three series of scans warm-up the x-ray tube.

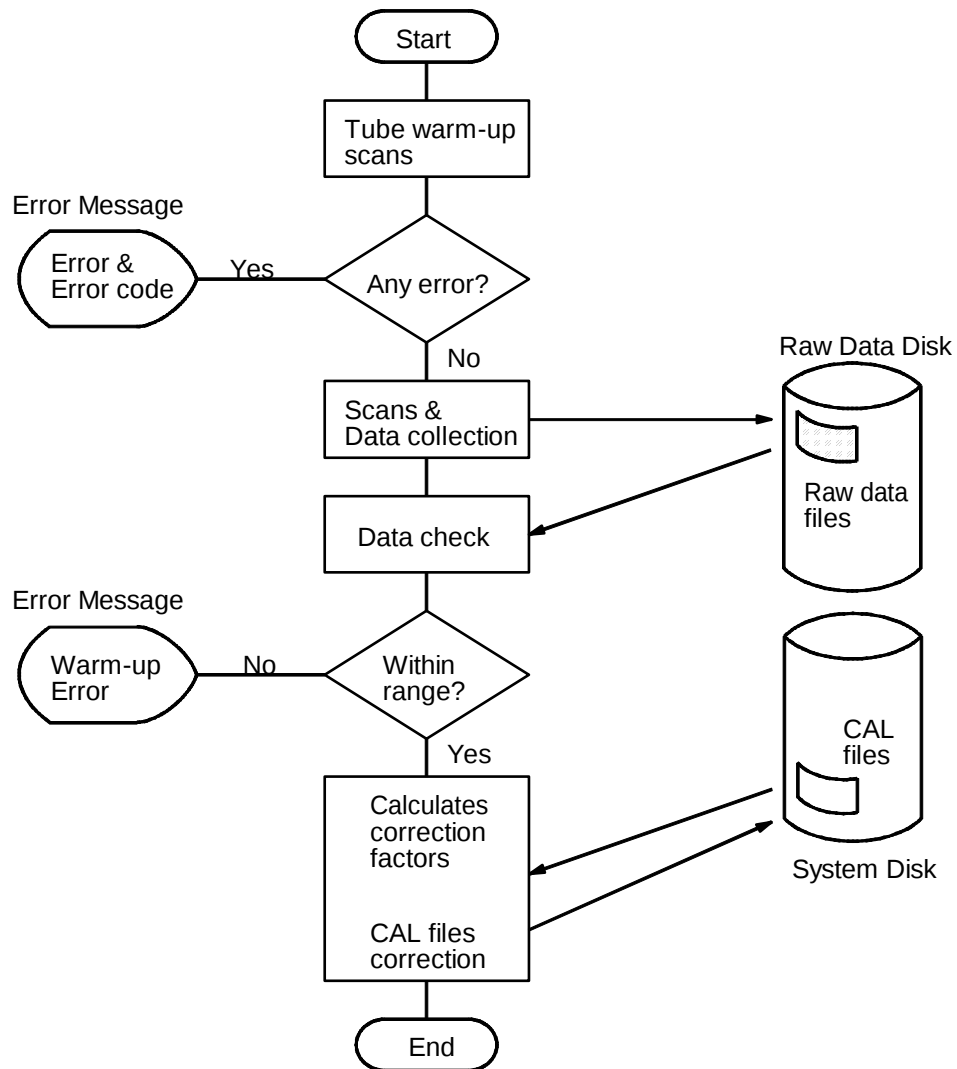
During the last three scans, data is collected to analyze it and update the CAL files:

The data is stored and whether the data falls within the specified range is checked. If data is out of range, the system reports a 'WARM-UP ERROR.' If data is within range, the system compares the data and the previous warm-up data and calculates correction factors for the CAL files, and updates the CAL files.

Illustration 4-1 shows the warm-up scan sequence.

4-1 WARM-UP SCANS (CONTINUED)

Illustration 4-1 Warm-up Sequence



4-2 AXIAL SCANS

Prior to the actual x-ray exposure, the system collects 256 views of offset data generated from the DAS. The offset data is used to correct actual x-ray data.

The system performs a full 360 deg. scan (clockwise direction only) during 1.0, 1.5, 2.0, 3.0 or 5.0 sec. These are called scan speeds or scan times, and not all of the them are available to all the systems; the available scan speeds or times vary according to system models or options installed on the systems.

During a scan, the system collects 972 views of data. A view period differs according to the scan speed. The following table shows this relation:

Scan Speed (sec)	View Period (∞ sec/view)
1.0	1029
1.5	1543
2.0	2058
3.0	3086
5.0	5144

The view period is synchronized with the azimuth encoder pulse.

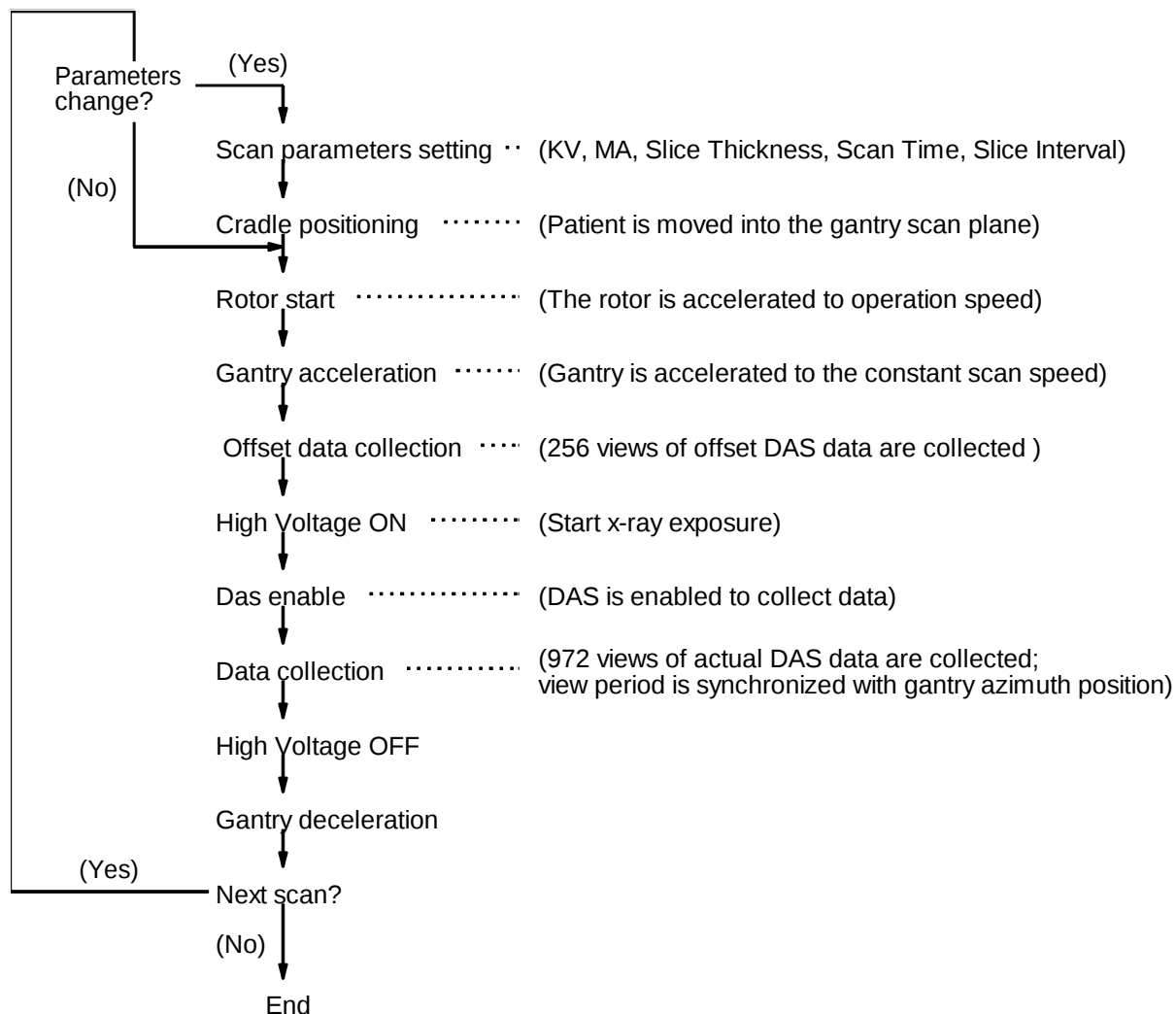
Axial scans are initiated from either 0 deg. or 180 deg. azimuth angle except for helical scans; during helical scans, scans can be initiated from any azimuth angle.

The system knows gantry azimuth position by azimuth encoder pulse counts and the Gantry Pulse which indicates that the gantry azimuth is at this moment at 0 deg., i.e., home position).

Illustration 4-2 shows the axial scan sequence.

4-2 AXIAL SCANS (CONTINUED)

Illustration 4-2 Axial Scan Sequence



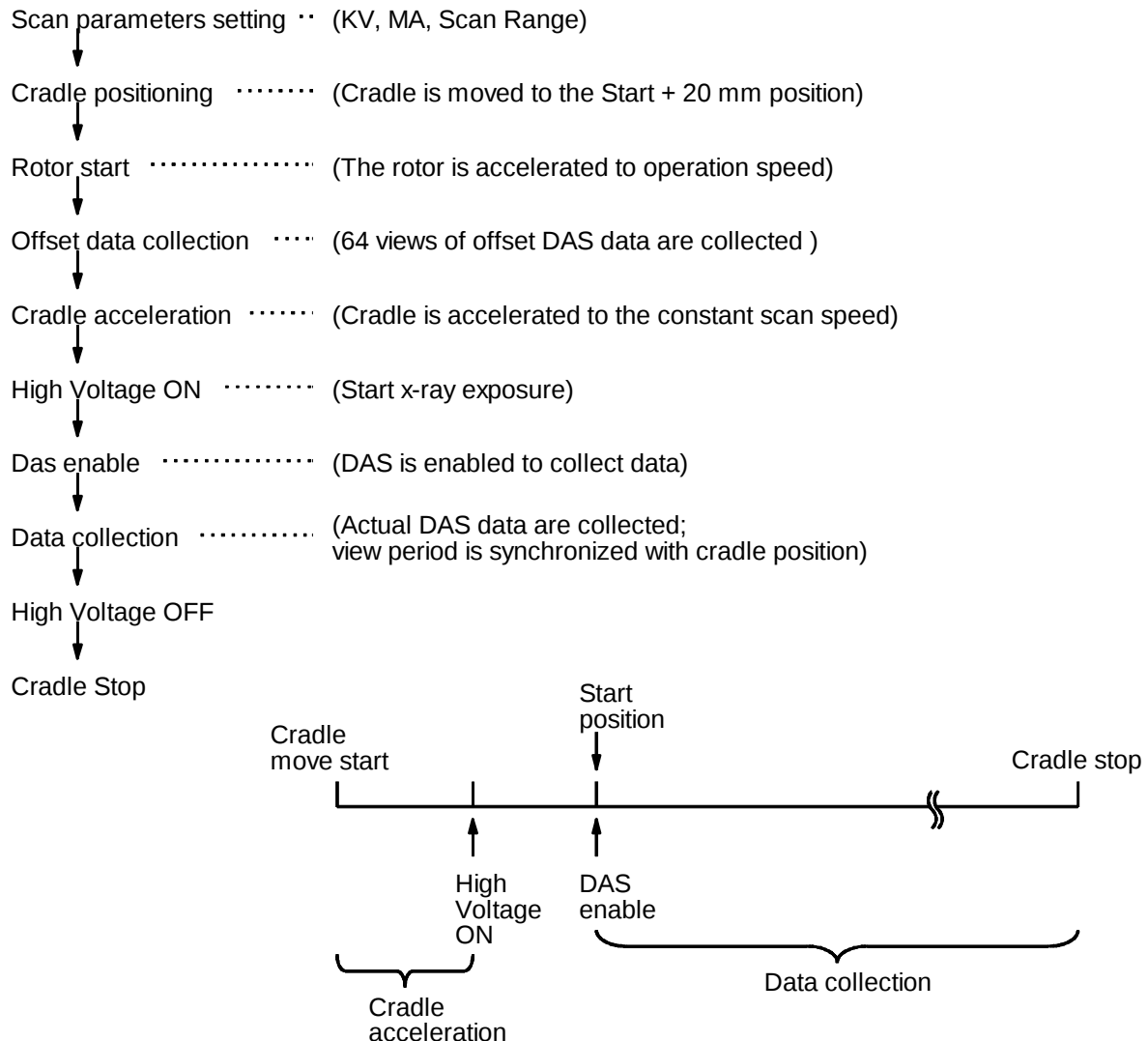
4-3 SCOUT SCANS

Prior to the actual x-ray exposure, the system collects 64 views of offset data generated from the DAS. The offset data is used to correct actual x-ray data.

The system advances the cradle and collects data from 685 active channels. The cradle speed is 75 mm/sec, and data collection timing is synchronized with the cradle encoder pulse.

Illustration 4-3 shows the scout scan sequence.

Illustration 4-3 Scout Scan Sequence



OPERATOR CONSOLE

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SECTION 1 - GENERAL DESCRIPTION

1-1 OVERVIEW

The information processing system (operator console) is based on the PCI (Peripheral Component Interconnect) bus architecture.

The host processor of the operator console is a Unix workstation, which is on the market.

(Workstation: The physical hardware that contains the CPU and graphics boards, a system disk, and a power supply. You connect it to a monitor, keyboard, and mouse to configure a working system.)

The model type of this workstation is called 'O2.'

Illustration 1-1 shows a block diagram of the operator console of this CT system.

O2 System Software

'O2 System Software' is the standard IRIX operating system software for the O2 and Silicon Graphics tools that come on the system disk and on the CD-ROM that you use in the event of a system crash.

(IRIX: Silicon Graphics's version of the UNIX operating system)

PCI Bus

'PCI' stands for Peripheral Component Interconnect - a bus specification. The PCI bus is a high-performance local bus used to connect peripherals to memory and a microprocessor. A wide range of vendors make devices that plug into the PCI bus.

The PCI bus can be operated at its intended high-performance by using DMA transfers.

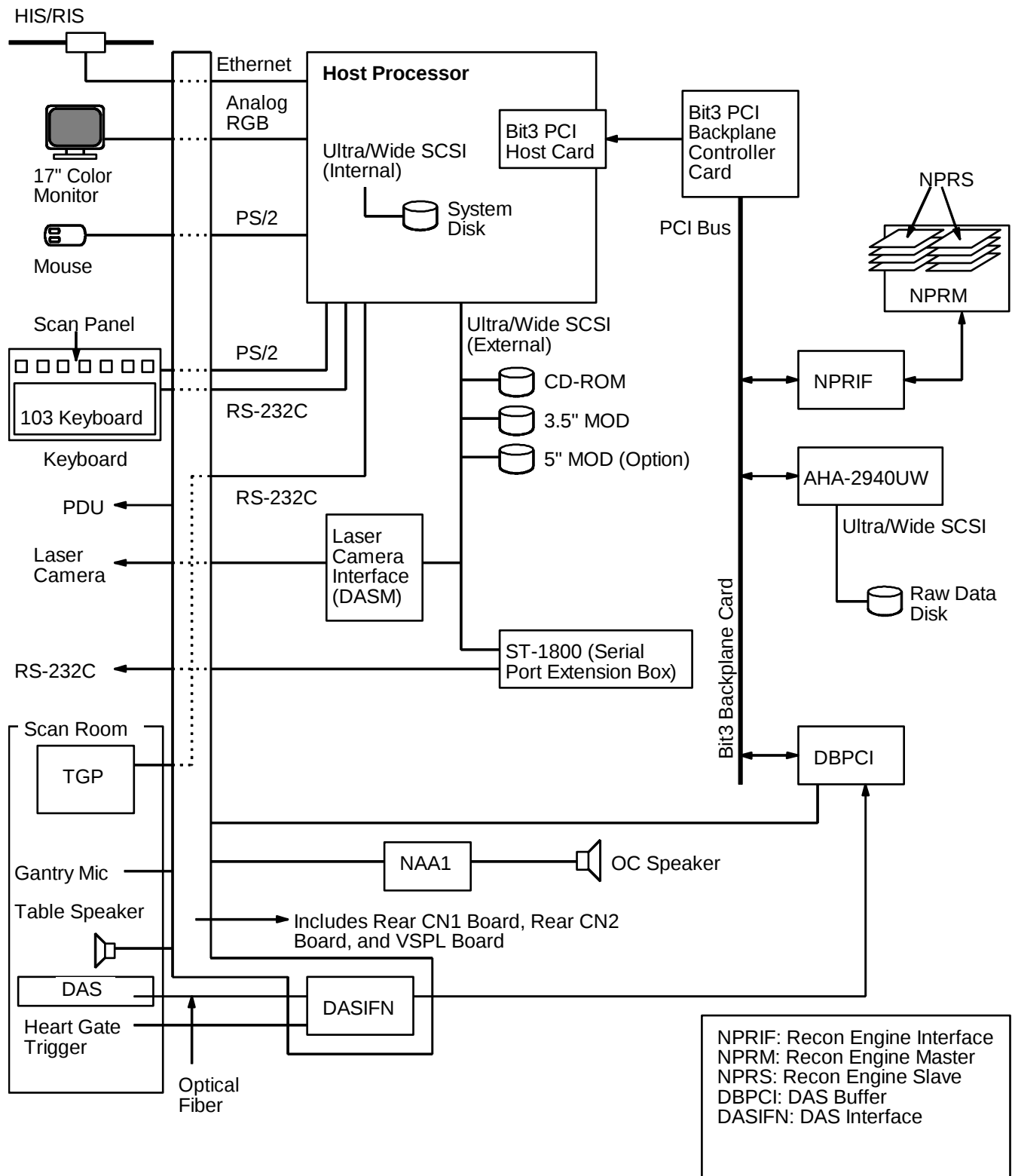
To perform DMA transfers with the PCI bus, a DMA controller should be equipped on the connected peripheral.

Address Map

For a PCI bus based computer system, memory address mapping and I/O address mapping of PCI devices are determined during Configuration Cycle which the host processor generates when the system is powered on. Each of the PCI devices requests its required address space size from the host processor during the cycle.

The PCI devices also (such are DBPCI, NPRIF, others) within this operator console are relocatable in the PCI address space. This means that address mappings of the PCI devices are not fixed. The physical addresses assigned by the host processor can be known by reading a set value on a base address register within configuration registers of each PCI device. (With a VME bus, base addresses are determined by dip switches.)

Illustration 1-1 Operator Console Block Diagram



1-2 MAIN COMPONENT DESCRIPTION

Host Processor

The host computer performs all of the following operations:

User interface
Image processings/display (all processings except recon)
Communication
Database control
Raw data/image data flow control
Image storage
Scan/recon control

System Disk (Ultra/Wide SCSI; within the Host Processor)

The host processor includes a hard disk drive which is used as the system disk. This system disk mainly stores the followings:

System and application software
Images
Calibration files
System parameters

- Capacity: 4 GB

Image Storage: 3200 images (take up 3 GB (1 image/0.5 MB))

(The remained 1 GB storage is used for System software/swapping space + Application software)

NPR (NP Recon Engine)

This is a unit for performing high-speed recon operations.

This unit consists of the following three kinds of circuit boards:

- **NPRIF (NPR Interface):**
Performs interfaces between the PCI bus and the NPRM.
- **NPRM (NPR Master):**
Includes one master DSP (Digital Signal Processor), main memory called Global Memory 0, others.
- **NPRS (NPR Slave):**
Includes two slave DSP's which perform arithmetic operations under the NPRM control.

The NPRS is a piggyback board equipped on the NPRM, and up to eight NPRS boards can be equipped on the NPRM (i.e., up to 16 slave DSP's can be equipped).

The NPRIF only is connected to a PCI slot. The NPRIF and NPRM are connected by cables.

1-2 MAIN COMPONENT DESCRIPTION (CONTINUED)

DBPCI (DAS Buffer for PCI Bus)

This is a circuit board, serving as a ring buffer whose capacity is 4 MB. This buffer temporarily stores DAS data. This board also includes control registers for the OC keyboard, safety loop, others.

DASIFN (DAS Interface for NP)

This is a circuit board which converts raw data sent from the gantry in optical serial signals into electric parallel signals. During conversion, this board performs transfer error corrections. This board also includes one channel for receiving Heart Gate Trigger inputs.

PCI Expansion Unit

Consists of PCI Host Card, PCI Backplane Controller Card, PCI Backplane Card. Increases the number of slots which are connected to the PCI bus of the host processor. Circuit boards for scan/recon are connected to these slots (NPRIF, DBPCI, AHA-2940UW).

REAR CN1

This is a circuit board which mainly has two functions: Signal filtering and Audio control. This board is connected to OC external components such as keyboard, TGP board on the gantry, or Power Distribution Unit (PDU), and is also connected to OC internal components such as DBPCI board, NAA1 board, or others.

Raw Data Disk (Ultra/Wide SCSI)

This is a high-speed hard disk drive for storing raw data.

- Capacity: 2 GB

Raw Data Storage: 500 raw data files

(70% of the disk space is used for raw data storage; 30 % of it is not used, because of low read/write rate)

Archive Equipment (MOD)

5" MOD is used for archiving images.

3.5" MOD is used for archiving raw data files and also used during system software installation to temporarily store data.

- Capacity: 2.3/1.2 GB, Density: 4x/2x (Sony MOD)

Images: DICOM format

Raw data: YMS format as Unix files (Includes Cal files, others)

CD-ROM Drive

Used for system software loading.

1-3 OPERATIONAL DESCRIPTION

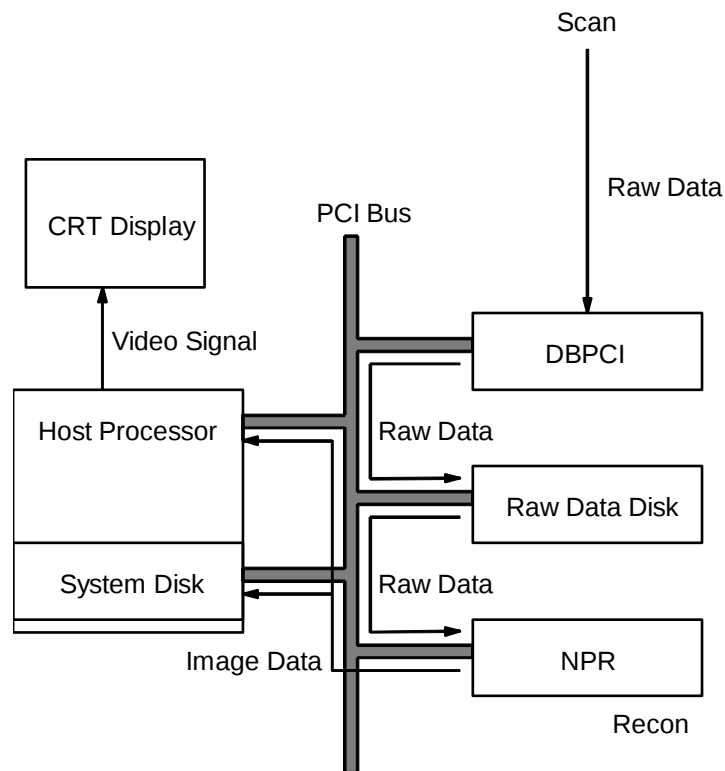
Scan Data Main Flow

Illustration 1-2 shows:

Raw data acquired during scans is first buffered by DBPCI;
The raw data is then stored to a hard disk drive which is a high-speed type and exclusively used for raw data storage;
The raw data is then transferred to the NPR where recon processing is performed;
The reconstructed images are then read by the host processor which converts the image data to video signal, as well as stores the image data to the system disk, which also stores system software.

As shown, raw data and image data are mainly transferred over the PCI bus.

Illustration 1-2 Scan Data Main Flow



SECTION 2 - HOST PROCESSOR

2-1 OVERVIEW

The host processor is a Unix workstation; its product name is 'O2.'

The host processor is the central unit within the operator console, performing various operations such are described below:

- Controls data transfer between data storage units and memory devices located on NPR, etc.
- Controls the entire scan sequence; it sends necessary instructions to relevant processors and devices, and receives status information from those processors and devices.
- Controls the NPR (NP Recon Engine).
- Performs graphics operations.

The host processor includes a DC power supply (175 watts); it requires AC 115 V power.

2-1 OVERVIEW (CONTINUED)

Table 2-1 shows main specifications of the host processor.

Table 2-1 Host Processor Specifications

Component		Specification
Central Processor	Model	MIPS R5000SC
	Operating Frequency	200 MHz
	Cache Memory	32 kB data/32 kB instruction primary cache 1 MB secondary cache
Main Memory	Capacity (standard)	256 MB (32 MB DIMM X 8)
	Type	Synchronous DRAM, 100 MHz, 4 banks, 288-bit wide
	Upgrade	up to 256 MB with 16 Mbit SDRAM up to 1 GB with 64 Mbit SDRAM
Hard Disk Drive (System Disk)	Capacity	4 GB (5400 rpm)
CD-ROM	Type	12 X
Graphics	Resolution	1280 x 1024 pixels 75.03 Hz Frame Rate 1024 x 768, 800 x 600, 640 x 480 also supported
	Frame Buffer Formats	32 + 32 bit FB (32 + 32 double buffered) 32 bit FB (16 + 16 double buffered) 16 bit FB (8 + 8 double buffered) 8 bit overlay
	Video Signal	Horizontal Statistics Horizontal Front Porch: 118.52 nsec ; 16 pixels Horizontal Back Porch: 1.84 μ sec ; 248 pixels Horizontal Sync : 1.07 μ sec ; 144 pixels Horizontal Active : 9.48 μ sec ; 1280 pixels Horizontal Line Rate : 79.98 KLines/sec First Field Statistics Vertical Front Porch : 12.50 μ sec ; 1.00 lines Vertical Back Porch : 475.14 μ sec ; 38.00 lines Vertical Sync : 37.51 μ sec ; 3.00 lines Vertical Active : 12.80 msec ; 1024.00 lines Vertical Sync Pulse : 38.58 μ sec ; 3.09 lines Pixel Clock : 135.00 MHz

2-1 OVERVIEW (CONTINUED)

Table 2-1 Host Processor Specifications (continued)

Component		
Built-in I/O (Input/Output)	-	PC (PS/2) compatible keyboard and mouse 2 x Ultra Fast/Wide SCSI single-ended, 1 internal, 1 external (40 MB/sec each) 2 x Serial 460 kbps (DB-9) 1284 Parallel (C miniature) 10BaseT/100BaseTX Ethernet standard (RJ-45)
Audio	-	Analog stereo input/output
Expansion Slot	-	One half-length, 64-bit PCI slot (10 W)
Operating System	-	IRIX 6.3 with XFS or later

2-2 BUILT-IN I/O (INPUT/OUTPUT) DESCRIPTION

The host processor has input/output ports for the following:

Display

Analog RGB signals are output from this port.

Keyboard/Mouse

A PS/2 keyboard and a mouse are connected these ports, respectively.

10BaseT/100BaseTX Ethernet

A diagnostic console, an independent console, or an HIS/RIS is connected to this port. DICOM compatible; the operator console can send (push) images to those devices using DICOM protocols at a 10 Mbits/sec maximum (the transfer speed varies according to receiver models, the size of transfer data, protocols, etc.).

Ultra/Wide SCSI (Internal - This port is provided within the host processor)

The O2 host processor includes a hard disk drive. This drive is used as the system disk, and is connected to this port. The disk is also used for storing images.

Ultra/Wide SCSI (External)

Since this port is a wide SCSI, the data bus of this port is 16-bit wide. However, within this OC, devices which handle eight-bit data such as CD-ROM drive, MOD drive, or Camera Interface are connected to this port in daisy chain.

Serial Port (RS-232C)

Provides two serial ports; one is used for communication with the TGP board, and the other is used for communication with scan keys (on the keyboard).

Audio

Provides audio input/output ports. The host processor can record audio signals from a microphone or other sources, and can play recorded audio data. This function is used for Autovoice.

PCI Bus Slot

The host processor is equipped with one PCI slot.

In order to expand the PCI bus, a 'PCI Host Card' is connected to this slot. The 'PCI Host Card' is a component of the PCI Expansion Unit.

SECTION 3 - NPR (NP RECON ENGINE)

3-1 OVERVIEW

NPR (NP Recon Engine) is one of the functional blocks within the operator console.

The NPR block constitutes a multi-processing structure to perform high-speed recon processings.

Illustration 3-1 is a block diagram showing the NPR structure.

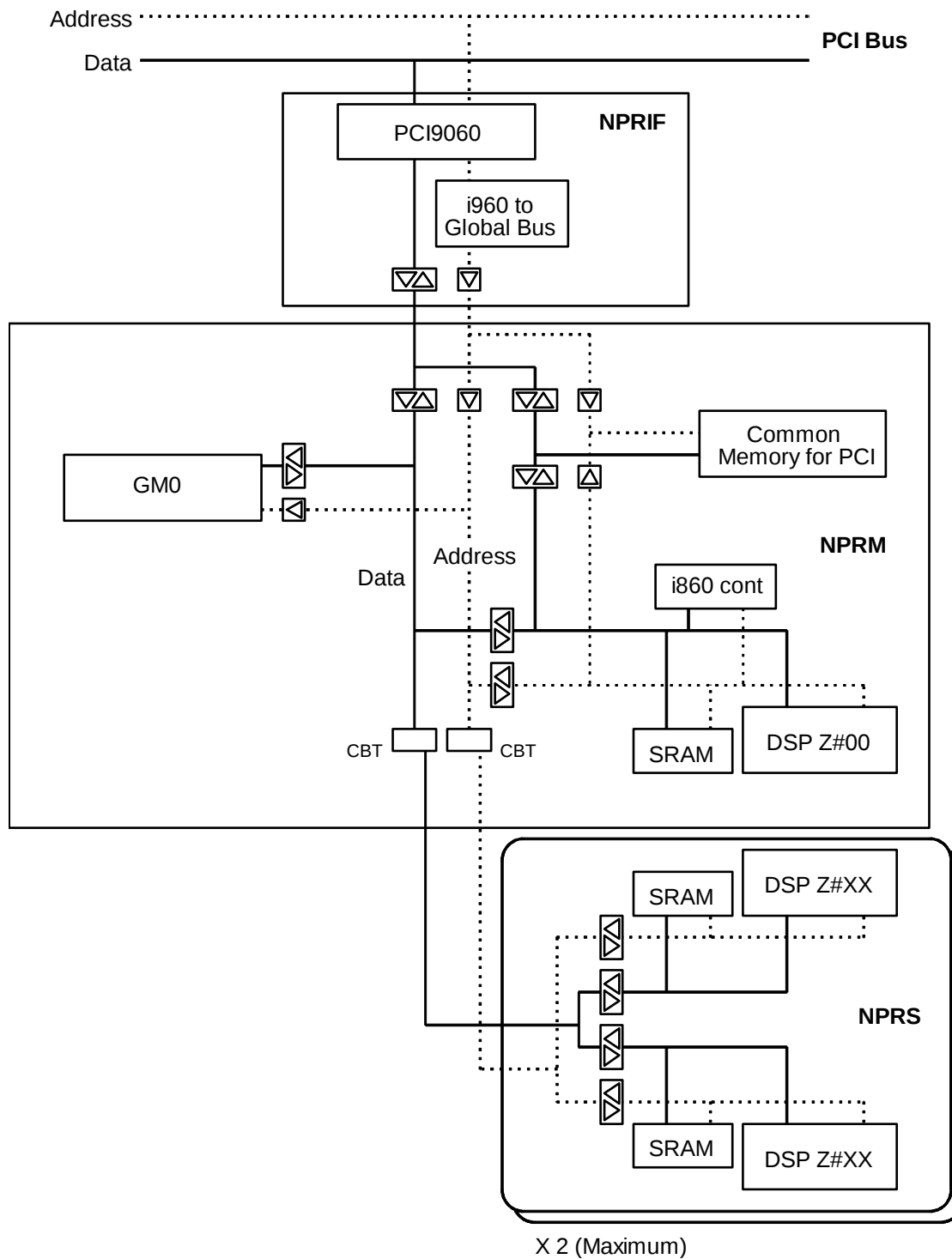
NPR consists of the following main circuit boards and devices:

- **NPRIF (NP Recon Interface)**
This board performs interfaces between the PCI bus and NPRM; that is, performs protocol conversion between the PCI bus and the local bus used within the NPRM.
- **NPRM (NP Recon Engine Master)**
This includes a DSP (Digital Signal Processor) which operates as the master DSP with other slave DSP's on NPRS. This DSP controls the operation of the slave DSP's and itself performs recon processings whenever considered efficient.
- **NPRS (NP Recon Engine Slave)**
NPRS is a piggyback board equipped on the NPRM. Up to four NPRS boards can be equipped. Each board includes two DSP's which are called slave DSP's; these operate under the control of the master DSP to perform recon processings.
The more the NPRS boards are installed, the faster the NPR performs recon processing, as follows:
(No) NPRS board: 6 sec recon
2 NPRS boards: 2 sec recon
- **Global Memory 0**
This is equipped on the NPRM.

The master and each of slave DSP's can communicate with each other (and also slave DSP's can communicate with one another), by Link Port Connection.

The communication is executed at a transfer rate of 36 MB/sec.

Illustration 3-1 NPR Functional Block Diagram

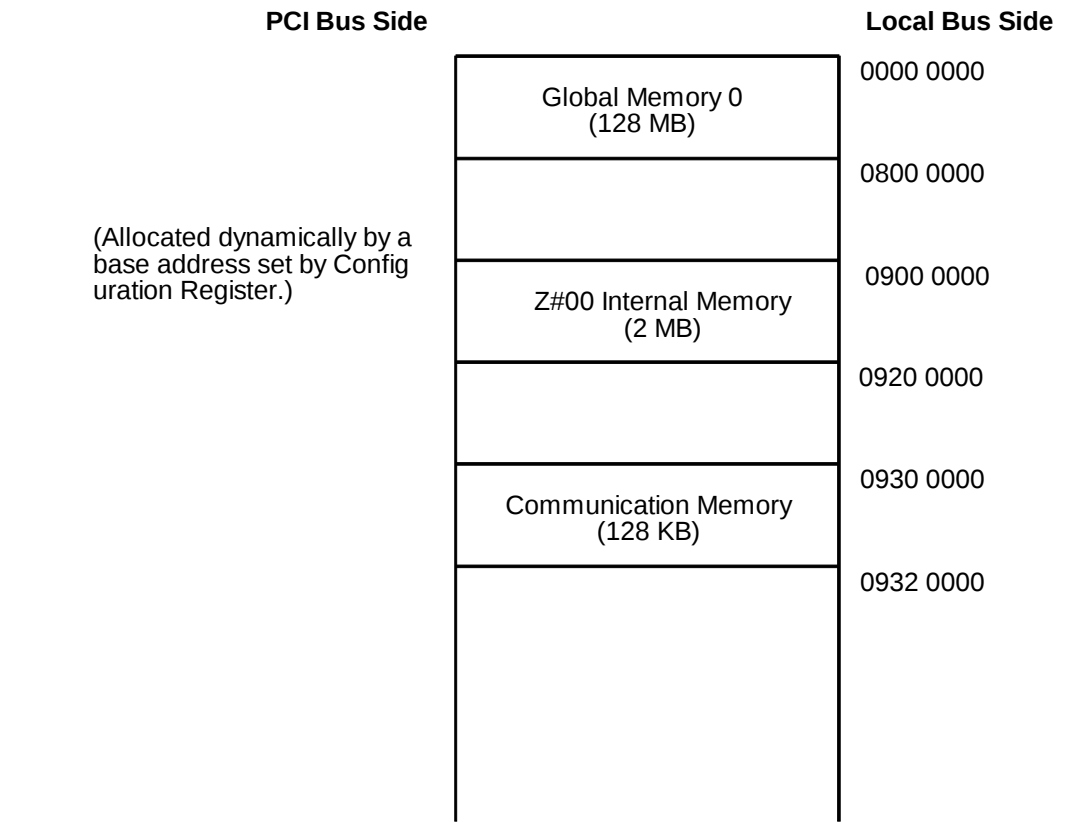


3-1 OVERVIEW (CONTINUED)

PCI Bus and NPR Bus

The NPR block is connected to the PCI bus.
 Illustration 3-2 shows the main part of the address map of the NPR block.
 The PCI side addresses (for Host Processor) are re-mapped into the local bus addresses as shown.
 The data access is in 32 bit (word)/Little Endian only.

Illustration 3-2 NPR Address Map



3-1 OVERVIEW (CONTINUED)

The following table describes which memory or register can be accessed by which processor.

Table 3-1 Accessible Memory and Registers

Processor	Host Processor (PCI Bus)	Z#00 (Master DSP) (on NPRM Board)	Z#XX (Slave DSP's; XX: up to 2) (on NPRS Boards)
Memory or Registers which can be accessed by the processor	Global Memory 0	Global Memory 0	Global Memory 0
	Communication Memory	Communication Memory	-
	Internal Memory of Z#00 (Master DSP)	Internal Memory of its own	Internal Memory of its own
	-	Internal Memory of Z#XX (Slave DSP's; XX: up to 2)	-
	-	Local Memory on its board and on NPRS boards	Local Memory of its board
	-	Communication Registers to/ from Slave DSP's	Communication Register to/from Master DSP

Global Bus Arbitration

The local bus for NPR is called Global Bus.

The access priority for the global bus is set as below:

- Host Processor (on PCI bus) > Z#00 (master DSP) > Z#01 > > Z#2

The global bus is freed for use on the 'Release on Request' basis.

3-2 HARDWARE DESCRIPTION

The following sections give some characteristics or descriptions about the main hardware constituting the NPR block.

3-2-1 DSP (Digital Signal Processor)

DSP's are the main devices on NPRM or NPRS boards.

'DSP Z#00' shown in Illustration 3-1 is the master DSP.

'DSP Z#XX' shown in Illustration 3-1 are slave DSP's. (XX: 01, 02, ... , up to 8; an actual number of slave DSP's equipped is a multiple of two)

- Model: ADSP-2106X
- 4 GWord address space (32 bit address), 32 bit data
- 40 MIPS (million instructions per second) at 40 MHz, 120 MFLOPS (million floating point operations per second) Peak, 80 MFLOPS Sustained
In practice, DSP's operate with the system clock of 36 MHz.
- Includes: 4 Mbits/2 Mbits On-chip SRAM (21060/21062), which is called 'Internal Memory.'

3-2-2 PCI Bus Interface

This function is provided by the NPRIF board.

- Model of the PCI bus interface chip: PCI9060 of PLX Technology
- Direct Slave Burst Mode and DMA can be executed.
However, when accessing the internal memory of Z#00 (master DSP), single access only is used.
- Always 32 bit data access
- Access Time: 2 clocks Peak when accessing the Global Memory 0.

3-2-3 Global Memory 0

Global Memory 0 is shown as 'GM0' in Illustration 3-1.

- Consists of SIMM's (EDO DRAM; Access Time: 50 nsec)
(SIMM: Single In-line Memory Module)
- Capacity: 32 or 64 MB
(32 MB: standard; 64 MB: future use (not determined))

3-2-4 Communication Memory for PCI Bus

- Capacity: 32 kWord (1 word: 4 bytes)
- Mapped on the PCI bus; Can be used for communication with the PCI bus master

3-2-5 Local Memory

Local Memory is shown as 'SRAM' in Illustration 3-1.

- The master DSP can access the local memory for slave DSPs'.
- Local Memory for the master DSP: 1 MB SRAM (Access Time: 12 nsec/0 wait access)
- Local Memory for the slave DSP's: 1 MB SRAM (Access Time: 12 nsec/0 wait access; or 12 nsec/1 wait access by the master DSP)

3-2-6 DSP Internal Memory

DSP internal memory is the on-chip SRAM of DSP's.

- The internal memory of the master DSP is mapped on the PCI bus; the host processor can access the memory and registers of the master DSP. The host processor loads programs to this memory.
- The internal memory of slave DSP's is mapped on the master DSP address space; the master DSP can access the memory and registers of slave DSP's. The master DSP loads programs to the memory.

3-2-7 Other

According to the number of NPRS boards and capacity of the Global Memory 0, switches should be set on the NPRM board.

SECTION 4 - DBPCI (DAS BUFFER FOR PCI BUS)

4-1 OVERVIEW

DBPCI is a PCI add-on board.

Raw data acquired by the DAS while scans are performed is immediately stored to the high-speed raw data disk. DBPCI is a buffer which temporarily stores DAS data (raw data), which has been converted into parallel format by the DASIFN board, until transferring it to the disk.

The DBPCI issues an interrupt to the PCI bus (to the host processor) to request a DMA transfer when the quantity of DAS data written into the DBM (DAS Buffer Memory) has reached to a set number.

(Or, before the ring buffer address for next data is set to the Start address from the End address; refer to Section 4-2-2)

Then, the host processor lets the DBPCI start the DMA transfer from the DBM to the raw data disk.

The DBPCI also has the following functions:

- **Raw Collection Timeout:**
While an x-ray exposure is performed, the board terminates the scan if the board does not receive data from the DASIFN board for a predetermined time, by issuing a DAS Error interrupt to the PCI bus.
- **Host Processor Hang-up:**
While an x-ray exposure is performed, the board opens the safety loop to terminate the exposure if the board detects that the host processor does not normally respond to interrupts issued by the board.

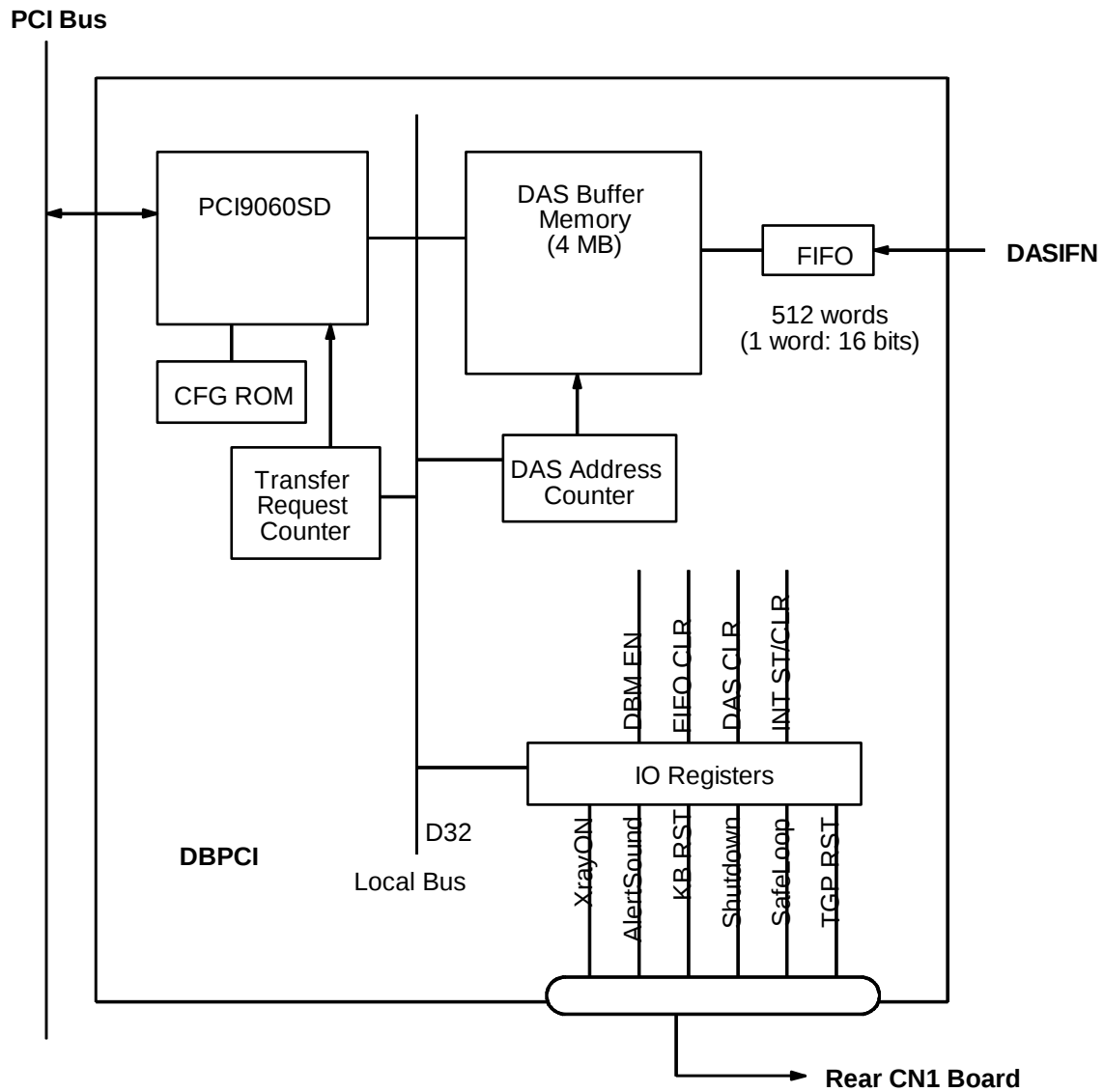
Illustration 4-1 shows the DBPCI structure.

DBPCI consists of the following major blocks:

- **PCI Bus Interface**
DBPCI has a local-PCI DMA (Direct Memory Access) function: DBPCI becomes the PCI bus master and performs a DMA data transfer from a local memory (DAS Buffer Memory) to a memory located on the PCI bus.
The transfer speed: more than 30 MB/sec; this will be limited by the access speed of a target.
- **DAS Buffer Memory (DBM)**
- **DASIFN Interface**
This block takes in DAS data from the DASIFN board to the memory (DBM).
The process speed (DAS data → Memory) is: 10 MB/sec Peak, 4 MB/sec Average.
- **Interface Registers**
DBPCI has several control/status registers such as for keyboard reset, safety loop control, etc.

4-1 OVERVIEW (CONTINUED)

Illustration 4-1 DBPCI Functional Block Diagram



4-2 EACH BLOCK DESCRIPTION

The following sections give some characteristics or descriptions about the main hardware constituting the DBPCI board.

4-2-1 PCI Bus Interface

The PCI bus interface is performed by the PCI bus interface chip.

- Model of the PCI bus interface chip: PCI9060SD of PLX Technology
- Address: 32 bits, Data: 32 bits, Clock: 33 MHz

PCI Bus and DBPCI Bus

The DBPCI board is connected to the PCI bus.

Illustration 4-2 shows the main part of the address map for the DBPCI board.

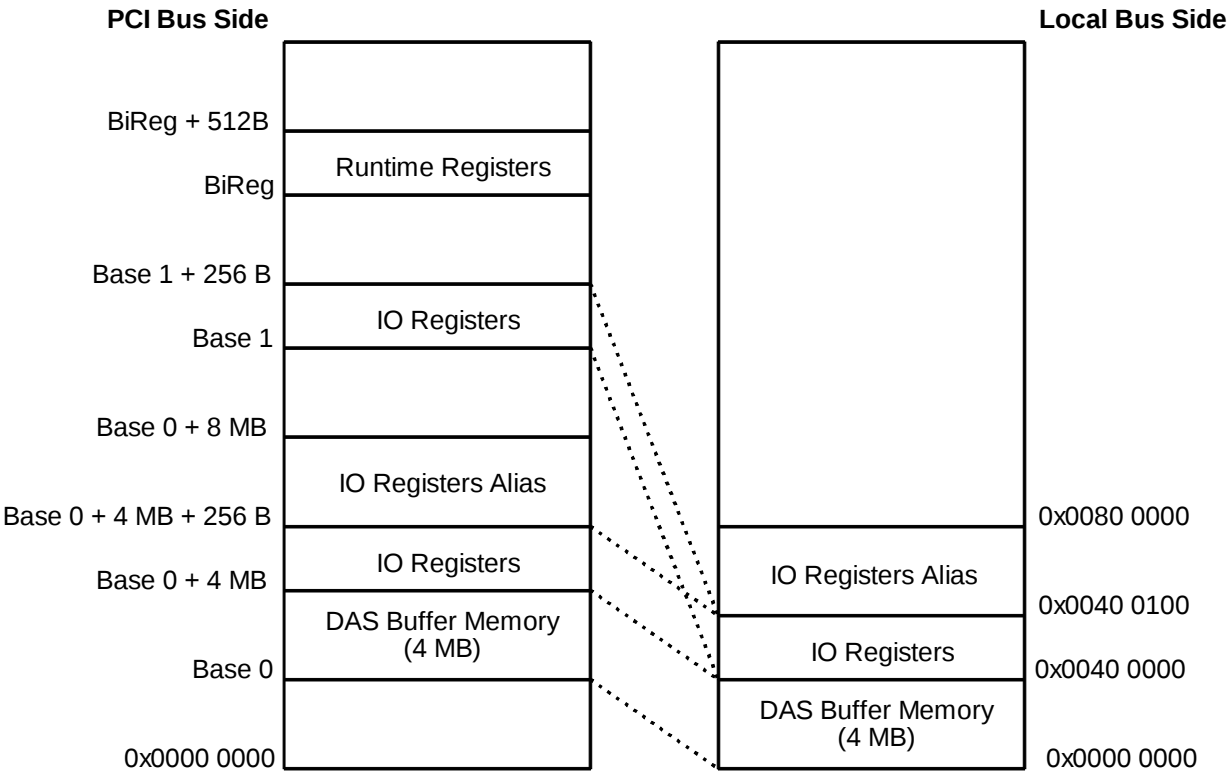
The PCI side addresses (for Host Processor) are re-mapped into the local bus addresses as shown.

The base addresses are determined by software.

The data access is in 32 bit (long word)/Little Endian only.

The runtime registers include internal registers of PCI9060SD, Configuration, DMA registers.

Illustration 4-2 DBPCI Address Map



4-2 EACH BLOCK DESCRIPTION (CONTINUED)

4-2-2 DAS Buffer Memory (DBM)

- DRAM is used like as a dual port memory; data is written to it from the FIFO and data is read to the PCI bus.
- Capacity: 4 MB, Address: 32 bits
- For devices on the PCI bus, this memory serves as an ordinary memory.

For the DASIFN board, this memory serves as a ring buffer.

DAS data is first written into the Start address, then written into the next address; this continues until DAS data is written into the End address. After this, further DAS data will be overwritten to the Start address.

However before the overwritten operation starts, an interrupt is issued to the PCI bus to request a DMA transfer.

Refer to Table 4-1.

- Memory Access Priority:
Priority 1: Memory Refresh
Priority 2: DAS Data Read
Priority 3: PCI Access

4-2-3 DASIFN Interface

- Includes a 512 words X 16 bits (1 word: 2 bytes) FIFO (First-In First-Out), not to fail to take in DAS data while some device is accessing the DBM via the PCI bus.
Normally the DBM is accessed by the single mode; or by the burst mode when the quantity of accumulated data in FIFO exceeds a set value.
- Since always two words of DAS data (16-bit data) are written into the DBM at the same time, the number of DAS data should be an even number.
- 'DBM Enable Register' can disable the DAS data take-in function when scans are not performed, to prevent wrong data reading due to electric noises.

4-2 EACH BLOCK DESCRIPTION (CONTINUED)

4-2-4 Control Registers

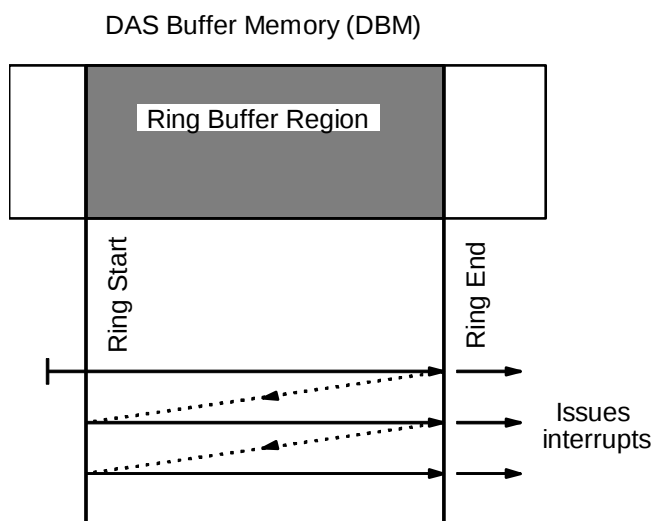
Table 4-1 describes main control registers equipped on the DBPCI board.

Table 4-1 Control Registers on DBPCI

Control Register	Function
For DAS Data Buffer	-
DAS Address Counter	Holds a DBM address which DAS data is written into. At first, an initial value (set on the DAS Address Ring Start register) is set to this counter, and then, the value of the counter increases every time DAS data is stored, until the value reaches a value set on the DAS Address Ring End register. This operation cycles. See Illustration 4-3.
DAS Address Ring Start	Sets the start address within the ring buffer memory.
DAS Address Ring End	Sets the end address within the ring buffer memory.
Transfer Request Counter	Counts how many times DAS data has been written into the memory; the counts equal (total transferred words of DAS data)/2. (A piece of DAS data consists of 16 bits (= 1 word), and write operation is performed in 32 bit data (= two words of DAS data))
For Interface	-
Shutdown	Sets the Shutdown Timer on the Front PNL to ON.
Safety Loop	Closes/opens the Safety Loop relay on the Rear CN1 board.
Keyboard Reset	Sets the keyboard to Reset.
TGP Reset	Makes the 'TGPRST' line active/inactive.
X-ray On Sound	Enables to make an alert sound during x-ray exposure.
Alert Sound	Requests an alert sound from the Rear CN1 board.
Timeout	Receives the 'Timeout' signal from the Audio Interface board. (Status Register)

4-2 EACH BLOCK DESCRIPTION (CONTINUED)

Illustration 4-3 Ring Buffer



SECTION 5 - DASIFN110M

Note

This section describes the DASIFN110M board and the DTRF110M board. '110M' means 110 Mbps (million bits per second). In this section, however, these boards are called DASIFN and DTRF, respectively, to make this section read more easily.

5-1 DAS DATA TRANSFER (DTRF → DASIFN)

As shown in Illustration 5-1, the DTRF board transmits DAS data to the DASIFN board through the RF rings. The communication functions of either board are the counterparts of the other. Therefore, it is important to understand the data transfer operation, in order to understand the DASIFN functions.

In this section, the RF transmitter → RF rings → FR receiver passage is simply regarded as a serial data transfer line.

Data stream from the DAS includes one word special code at the end of each view. This code is called View End Mark, consisting of 'FFF0h.'

The DTRF composes a communication packet for one view from data between View End Marks, and transfers the packets to the DASIFN.

The View End Marks are not sent to the DASIFN.

Packet Format

Illustration 5-2 shows a communication packet transferred from the DTRF during one view.

The DTRF first sends 'START' commands followed by Sync's, then, sends DAS data including FEC check data (in this duration no commands are sent), and then, sends 'END OK' or 'END NG' commands followed by Sync's; this is the sequence for one view.

'END OK' notifies the receiver (DASIFN) that a packet is normally composed.

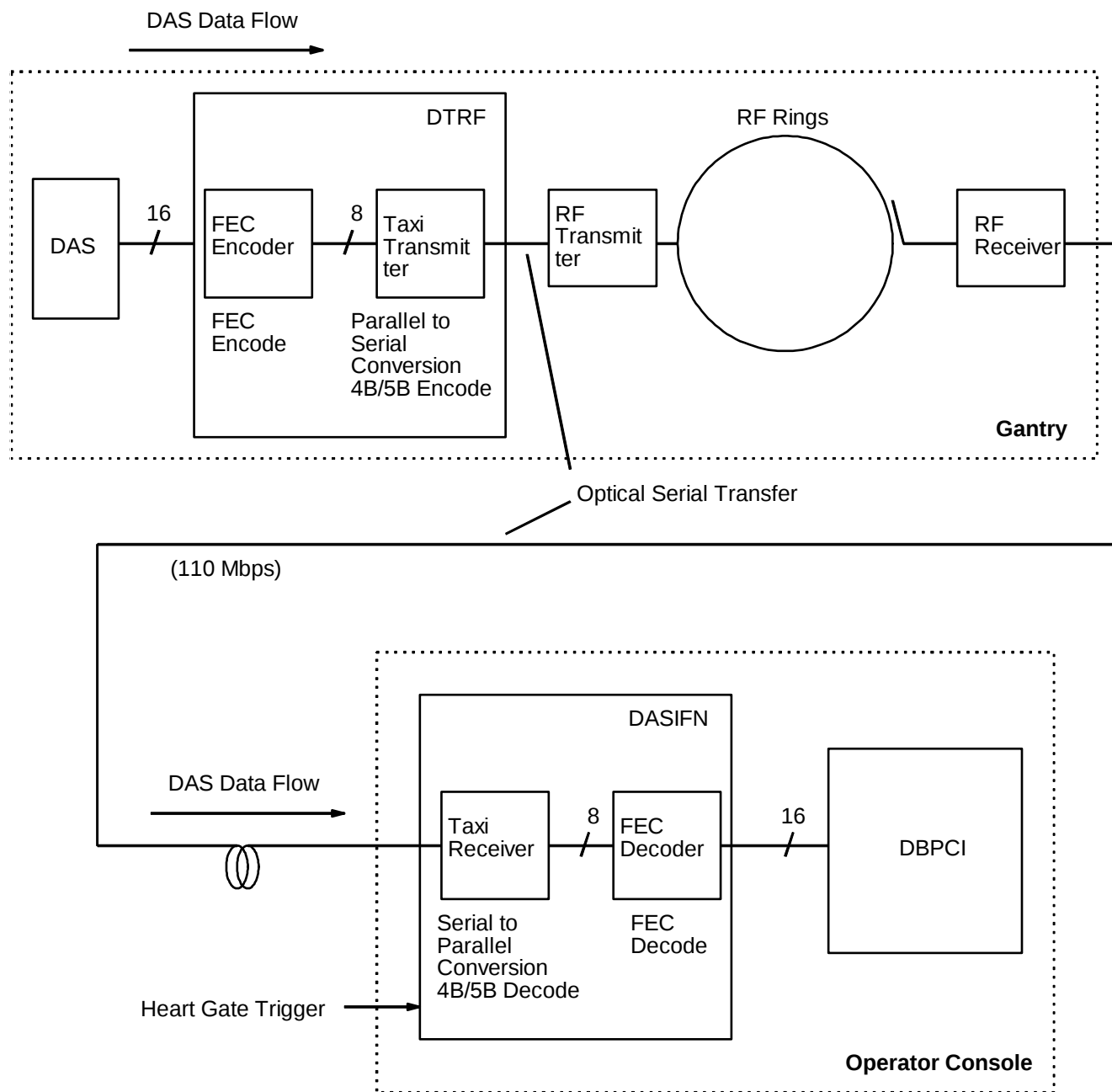
'END NG' notifies the receiver that a normal packet could not be composed for some reason.

The DASIFN starts the data receive sequence for one view upon receiving of the 'START' commands, and ends the sequence by receiving the 'END OK' or 'END NG' commands.

Sync signals are not included in Taxi Data.

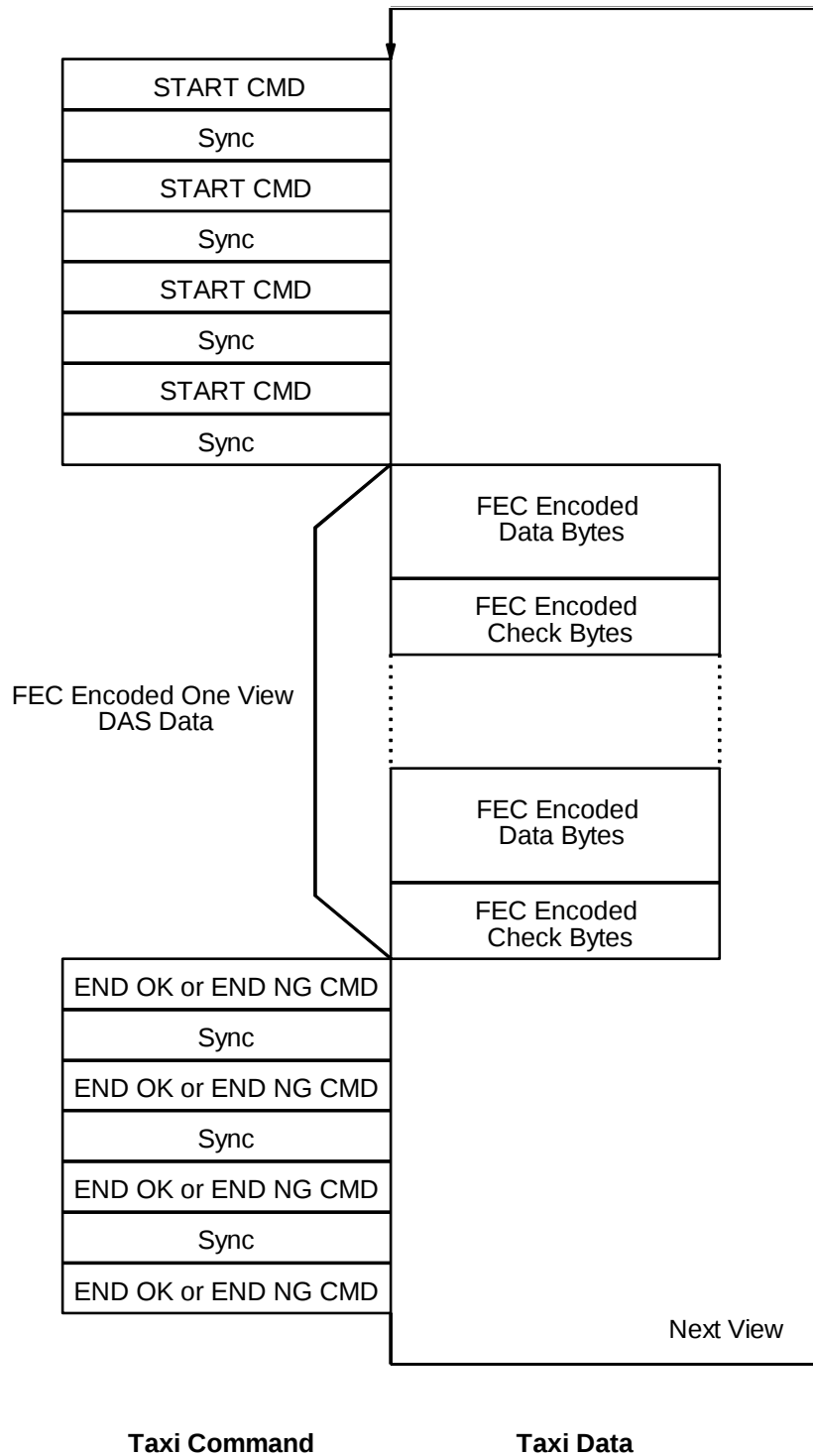
5-1 DAS DATA TRANSFER (DTRF → DASIFN) (CONTINUED)

Illustration 5-1 DAS Data Transfer



5-1 DAS DATA TRANSFER (DTRF → DASIFN) (CONTINUED)

Illustration 5-2 Packet Format for One View DAS Data



5-1 DAS DATA TRANSFER (DTRF → DASIFN) (CONTINUED)

FEC (Forward Error Correction) Encoder & Decoder (on DASIFN)

Since the serial data stream might be interrupted by noises (mainly burst noises), FEC is used to correct data error.

- The correction method is: Reed-Solomon, conforming to Intelsat IESS-308, Rev. 6B.
- The polynomial ' $P(x) = x^8 + x^7 + x^2 + x + 1$ ' is used to calculate Reed-Solomon codes.

Illustration 5-3 shows one FEC block. Refer also to Table 5-1.

With this block format, up to six error bytes (equals half the number of the check bytes within one block) can be restored to original values per block.

The FEC encoder (FEC decoder on the DASIFN board also) is operated in the continuous transmission mode, capable of processing at 5.5 MB/sec.

Illustration 5-3 One FEC Block

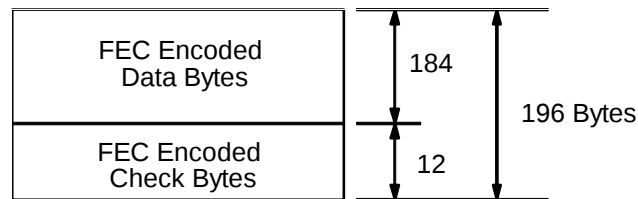


Table 5-1 Data Blocks per View

Data Bytes/Block	Number of Blocks/View	Data Bytes/View
184	8	1472 (= 184 X 8) (= 736 words)

5-1 DAS DATA TRANSFER (DTRF → DASIFN) (CONTINUED)

Taxi Transmitter

- Eight-bit parallel data is converted into 10-bit serial data by the 4B/5B encoding (ANSI X3T9.5).
- Transfer Coding Format: NRZI (Non Return to Zero Change on 1)

Data Transfer Line

The converted serial data is transferred over one optical cable in serial format.

- The wave length is 1300 nm.
- The serial data transmission rate is fixed at 110 Mbps.

5-2 DASIFN

Function

The DASIFN (DAS Interface for NP) has the following functions:

- Receives optical signals in serial data format, converts them into electric signals, and converts them into parallel data format.
- Corrects serial data communication errors (FEC Correction).
- Performs View Size Correction.
- Adds View End Mark (VEM) data to the end of DAS data train per view.
- Transfers 16-bit parallel DAS data to the DBPCI board
- Includes Heart Gate Trigger or other signals into VEM (View End Mark) data.

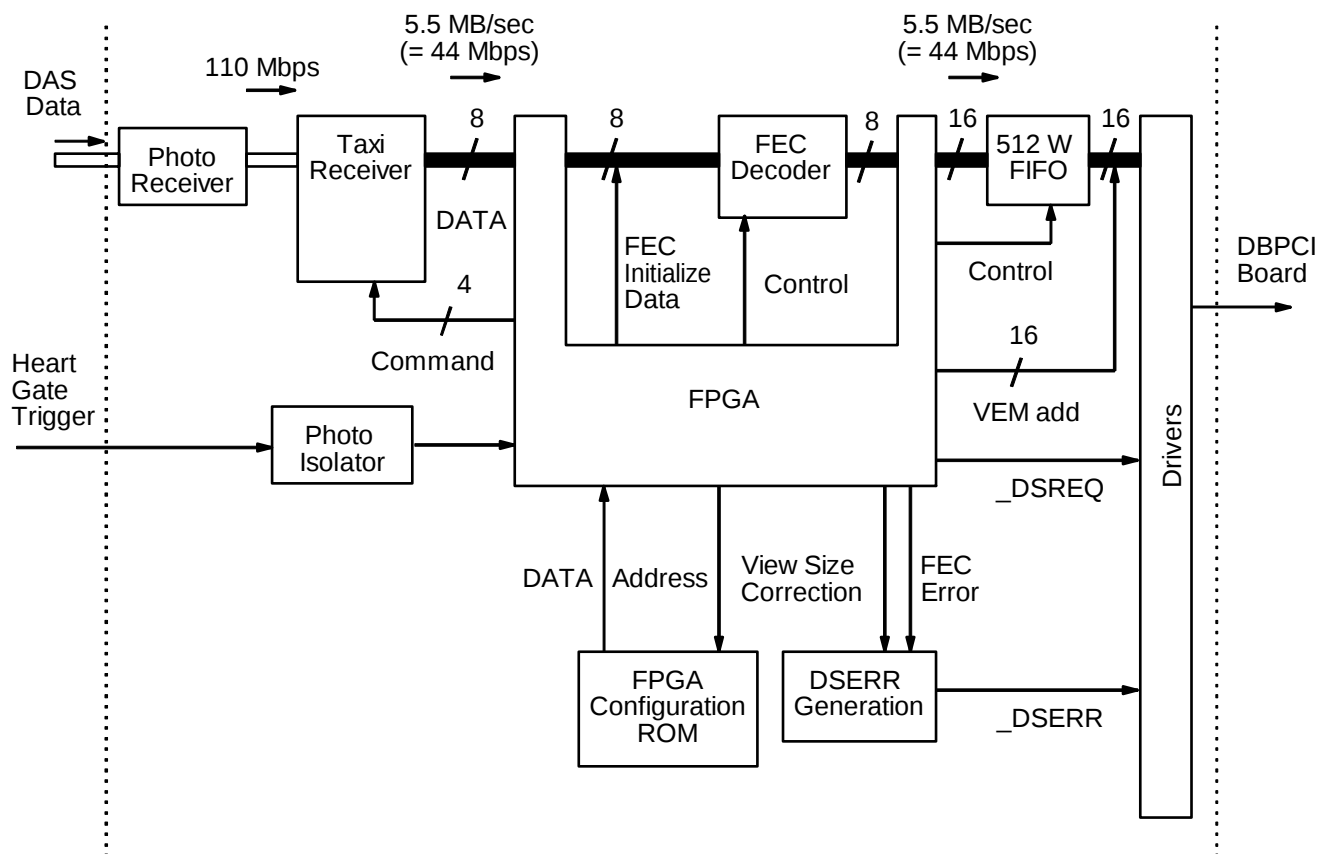
DASIFN Block Diagram

See Illustration 5-4;

- The photo receiver (of Hewlett Packard) converts the optical signals to electric signals.
- **Serial to Parallel Conversion:**
The Taxi Receiver chip (of Advanced Micro Devices) performs the 4B/5B decoding, conforming to ANSI X3T9.5 (FDDI).
- The FEC Decoder is initialized by the FPGA at a reset time. The initialize data includes FEC Block Length, Check Byte Length, etc.
The FEC decoder is operated in the continuous transmission mode, capable of processing at 5.5 MB/sec.
- The FPGA (Field Programmable Gate Array) converts eight-bit data from the FEC Decoder into 16-bit data, and this data is input to the FIFO.
- The converted DAS data (to 16-bit parallel data) is transferred to the DBPCI board via the 512 word FIFO (First-In, First-Out), at a rate of 5.5 MB/sec.
- Heart Gate Trigger or other signals are photo-isolated and recorded into VEM data when the leading edge of the signals is detected. Therefore, the heart gate triggers can be recorded with view interval accuracy.

5-2 DASIFN (CONTINUED)

Illustration 5-4 DASIFN Block Diagram



5-2 DASIFN (CONTINUED)

View Size Correction

736 pieces of DAS data are transferred per view from the DTRF. Refer to Table 5-1. The number 736 includes reference data, dummy data, and other data, in addition to active channel data (685 channels). Four VEM (View End Mark) data are added to the last of the transferred data per view in the DASIFN board. Consequently, 740 pieces of data are sent to the DBPCI board as data for one view. See Table 5-2.

Table 5-2 Data to DBPCI per View

From DTRF (words/view)	VEM Data (words)	To DBPCI (words/view)
736	4	740

Four View End Marks are to be put at the end of one view data train.

A part of DAS data transferred from the gantry to the DASIFN board might be lost or some non-data might be induced over the transfer lines by noises or other factors.

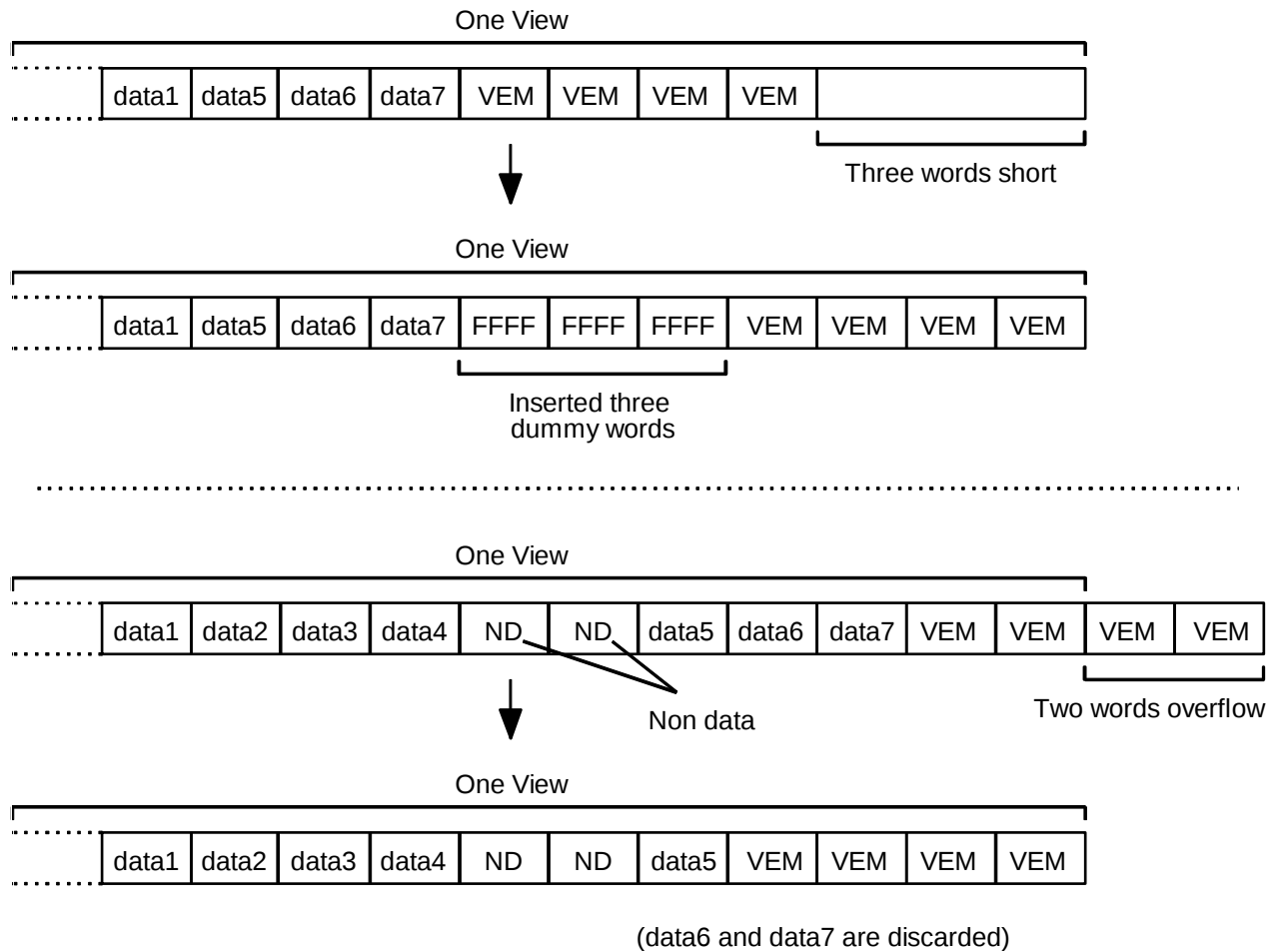
The DASIFN board has a View Size Correction function, which adjusts the number of data per view to be sent to the DBPCI board to the specified one (Table 5-2); in the following way (See Illustration 5-5).

- **When Data Short:**
When the number of transferred DAS data is short of the specified one, dummy data ('FFFF') is added; the number of dummy data equals the number short.
- **When Data Overflow:**
When the number of transferred DAS data exceeds the specified one, the last data is discarded; the number of discarded data equals the number of overflowed data.

Thus, the data train per view which the DBPCI board receives always includes four VEM's at the end of the data train.

5-2 DASIFN (CONTINUED)

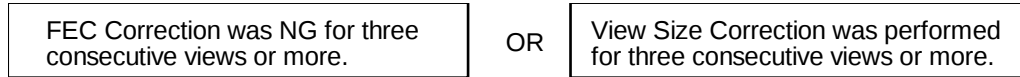
Illustration 5-5 View Size Correction



5-2 DASIFN (CONTINUED)

Fatal Error Detection

If a fatal error, as defined below, occurs, this is reported to the DBPCI board by the _DSERR signal.

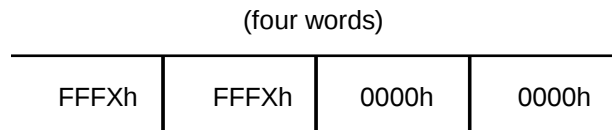


FEC correction error can be detected at the transmitter side (by 'END NG' command) and/or at the receiver side.

View End Mark

Four words as described in Illustration 5-6 are added to the last of one view DAS data train.

Illustration 5-6 View End Mark



X (= b3 b2 b1 b0) is a four-bit status flag, defined as below:

b3: 1 if View Size Correction was performed.

b2: 1 if FEC Correction was NG.

b1: 1 if Violation was detected during the Taxi serial communication.

b0: 1 when Heart Gate Trigger (edge =)

SECTION 6 - CONNECTOR BOARDS

6-1 CONNECTOR BOARDS

All the signal cables connected between the operator console (OC) and subsystems/components outside the OC run through these connector boards.

The connector boards mainly include filters for each signal line to improve the EMC (Electro-Magnetic Compatibility) performance of the OC. The REAR CN1 board also includes an audio mixer, relay for the safety loop, a video amplifier for slave monitors, and others.

6-2 REAR CN1 BOARD

Illustration 6-1 shows a block diagram of the REAR CN1 board.

The REAR CN1 board is connected to a slot of the connector box of the OC, and as shown in Illustration 6-1, the board is connected to OC external components such as the keyboard, TGP board on the gantry, or the Power Distribution Unit (PDU), and is connected to OC internal components such as DBPCI board, NAA1 board, or others.

The board functionally consists of the following two blocks:

- Filter Block
- Audio Mixer Block

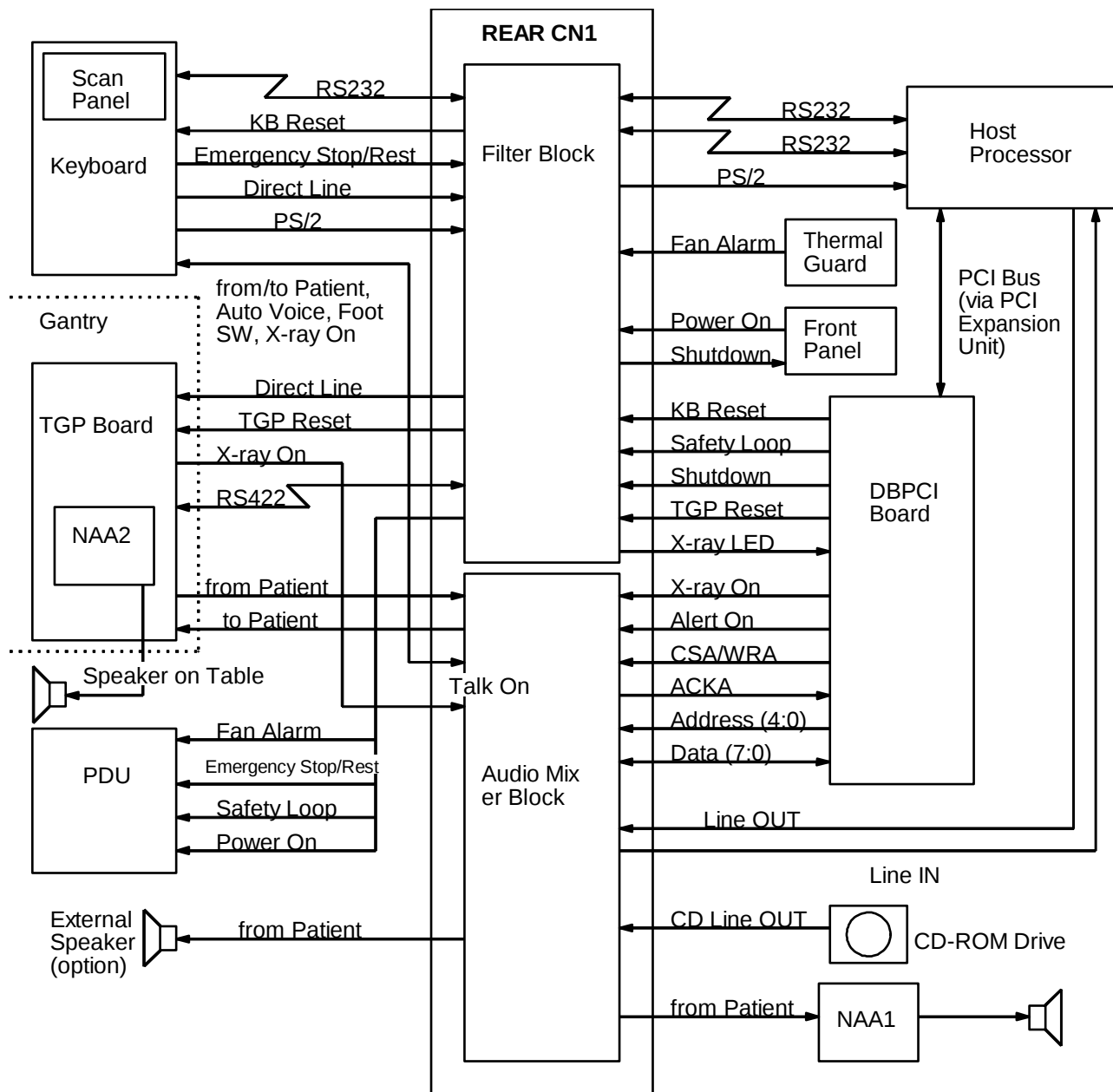
6-2-1 Filter Block

As shown in Illustration 1-1, this block includes the following interface circuits:

- **Keyboard Interface:**
Mainly interfaces between the keyboard (including the scan buttons) and the host processor.
- **TGP Interface:**
Mainly interfaces RS232/RS422 communications and Direct Lines between the TGP board located on the gantry and the host processor or keyboard.
- **PDU Interface:**
Mainly interfaces Power On/Off, Emergency, Safety Loop, or other signals between the Power Distribution Unit (PDU) and the keyboard or the FRONT PNL board of the OC.

6-2 REAR CN1 BOARD (CONTINUED)

Illustration 6-1 REAR CN1 Block Diagram



6-2 REAR CN1 BOARD (CONTINUED)

6-2-2 Audio Mixer Block

The audio mixer block of the REAR CN1 board Includes registers for audio function, and also includes an audio amplifier for headphones or external speakers (which are not the OC speaker which is driven by the NAA1 board).

See Illustration 6-2.

As shown, audio signals from several sources are mixed in this block.

- Audio Input Sources:
 - Microphone on the gantry (Intercom: From Patient)
 - Microphone on the OC keyboard (Intercom: To Patient)
 - Audio output on the host processor (Auto Voice play)
 - Audio output on the CD-ROM drive (BGM, or other)
 - Synthesized sounds on the REAR CN1 board (X-ray On, Alert)
These are generated using a programmable timer which is controlled by software.
- Audio Output Destinations:
 - Speaker on the gantry
 - Speaker on the OC
 - Audio input on the host processor (for recording Auto Voice messages)

6-2 REAR CN1 BOARD (CONTINUED)

Audio Input Switch

As shown in Illustration 6-2, analog switches are used to switch audio input sources, and are controlled by the 'Talk On' button on the keyboard or a foot switch connected to the keyboard.

- An intercom function is provided between the OC room and the gantry room. The 'Talk On' button on the keyboard switches communication direction, as described below:
 - While 'Talk On' is pressed, communication of "OC room → gantry room" is enabled; and both of Auto Voice (both in the OC room and the gantry room) and sound from the CD-ROM drive (both in the OC room and the gantry room) are disabled.
 - While 'Talk On' is released, communication of "gantry room → OC room" is enabled.

If a foot switch is provided, this also serves as the 'Talk On' button.

- The X-ray On sound and alert sounds in the OC room are always enabled, even when 'Talk On' is pressed.
- Auto Voice messages can be recorded by using the microphone equipped on the keyboard while pressing the 'Talk On' button.

While Auto Voice is being played, communication of "gantry room → OC room" can be disabled. This prevents Auto Voice sound degradation on the OC side, because: Auto Voice is played both in the OC room and the gantry room. If communication of "gantry room → OC room" is enabled, the Auto Voice messages are doubled on the OC side, which degrades the sounds.

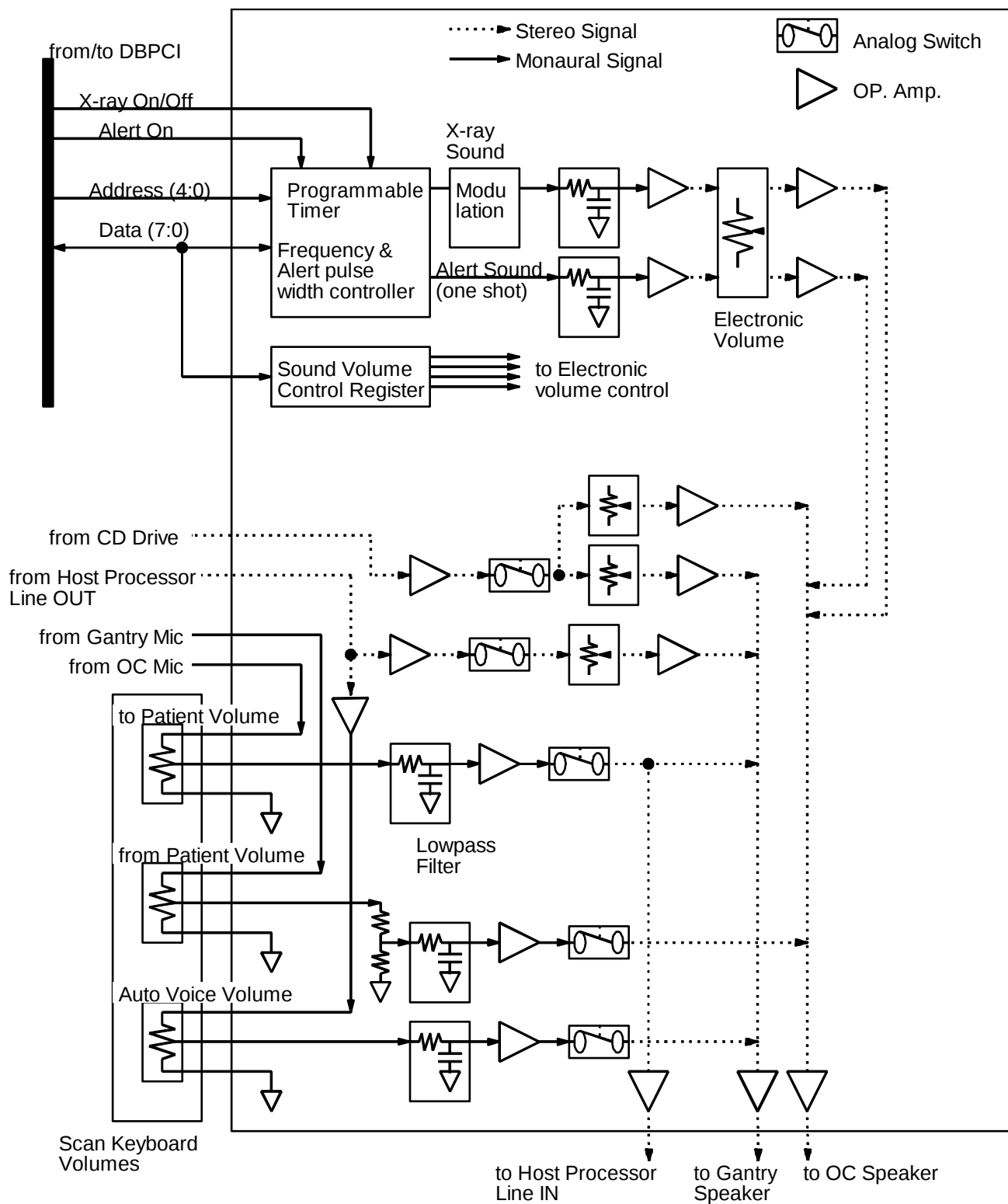
Volume Control

The following two kinds of volume control are provided.

- The following can be adjusted with the manual **volumes on the keyboard**:
 - Volume of communication of "OC room → gantry room" (through the keyboard microphone)
 - Recording level of Auto Voice messages (through the keyboard microphone)
 - Auto Voice volume in the gantry room
 - Volume of communication of "gantry room → OC room" (through the gantry microphone)
- The **electronic volumes** are controlled by software, controlling the following:
 - Auto Voice volume in the OC room
 - Sound volume from the CD-ROM drive both in the gantry room and the OC room
 - Alert sounds in the OC room
 - X-ray On sound in the OC room

6-2 REAR CN1 BOARD (CONTINUED)

Illustration 6-2 Audio Mixer Block



6-2 REAR CN1 BOARD (CONTINUED)

Audio Register Address Map

Illustration 6-3 shows an address map of audio control registers.

The addresses shown are mapped at an area within the DBPCI Input/Output address space of the host processor.

Registers mapped within the I/O register bases \$50 ~ \$7F are located on the DBPCI board. These are controlled by the host processor, and control signals only are sent from DBPCI to the REAR CN1 board.

Registers mapped within the I/O register bases \$80 ~ \$FF are located on the REAR CN1 board. These registers and the DBPCI board are connected via a dedicated bus.

Illustration 6-3 Audio Register Address Map

	D7	D0
\$b4		
\$b0		CD GA Volume Register
\$ac		CD OC Volume Register
\$a8		AV OC Volume Register
\$a4		Alert Volume Register
\$a0		X-ray Volume Register
		PIT1 Register
\$90		
		PIT0 Register
\$80		
\$60		AUX0 Auto Voice Playback Register
\$54		Alert Sound Register
\$50		X-ray On Sound Register

IO Register Base

Note:
 CD: CD-ROM Drive
 GA: Gantry
 OC: Operator Console
 AV: Auto Voice
 PIT: Sound Pulse Width Control

SECTION 7 - OTHER OC COMPONENTS

7-1 KEYBOARD, MOUSE

The keyboard used for this operator console integrates the following components:

- **103 Keyboard, Mouse:**
This 103 keyboard and the mouse have a PS/2 interface for connecting themselves to the host processor.
- **Scan Keys, Microphone:**
Keys used for scanning, and a microphone used for an intercom are incorporated into the keyboard. These keys are connected to the host processor via RS-232C.

The keyboard and the TGP board are connected by 'Direct Lines' for the remote cradle and gantry tilt control.

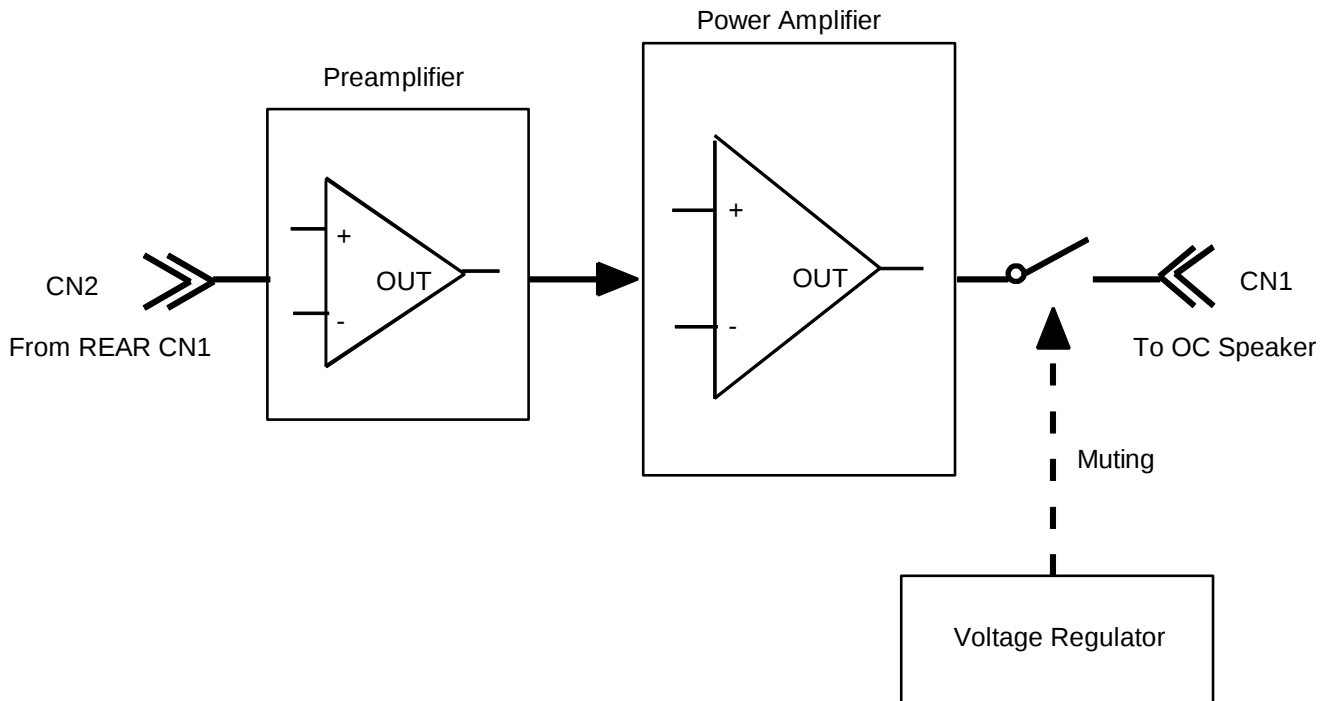
7-2 CRT DISPLAY

- 17" color monitor
- The resolution used for the CRT Display is 1280 x 1024 matrix.
The refresh rate used is 75 Hz.

7-3 NAA1 (NP AUDIO AMPLIFIER 1)

This is an amplifier board for the OC speaker. See the following block diagram.

Illustration 7-1 NAA1 Block Diagram



7-4 PCI EXPANSION UNIT

The host processor only provides one PCI slot. This unit expands this one slot to seven slots available. This unit consists of the following three boards (designed by Bit3):

PCI Host Card
PCI Backplane Controller Card
PCI Backplane Card

The main devices on these boards are PCI-PCI Bridge chips, which expand the number of slots in stages.

Illustration 7-2 shows a block diagram of the PCI Expansion Unit.

Table 7-1 describes installed circuit boards at those slots which are made available by the PCI Expansion Unit.

Table 7-1 PCI Slot Board

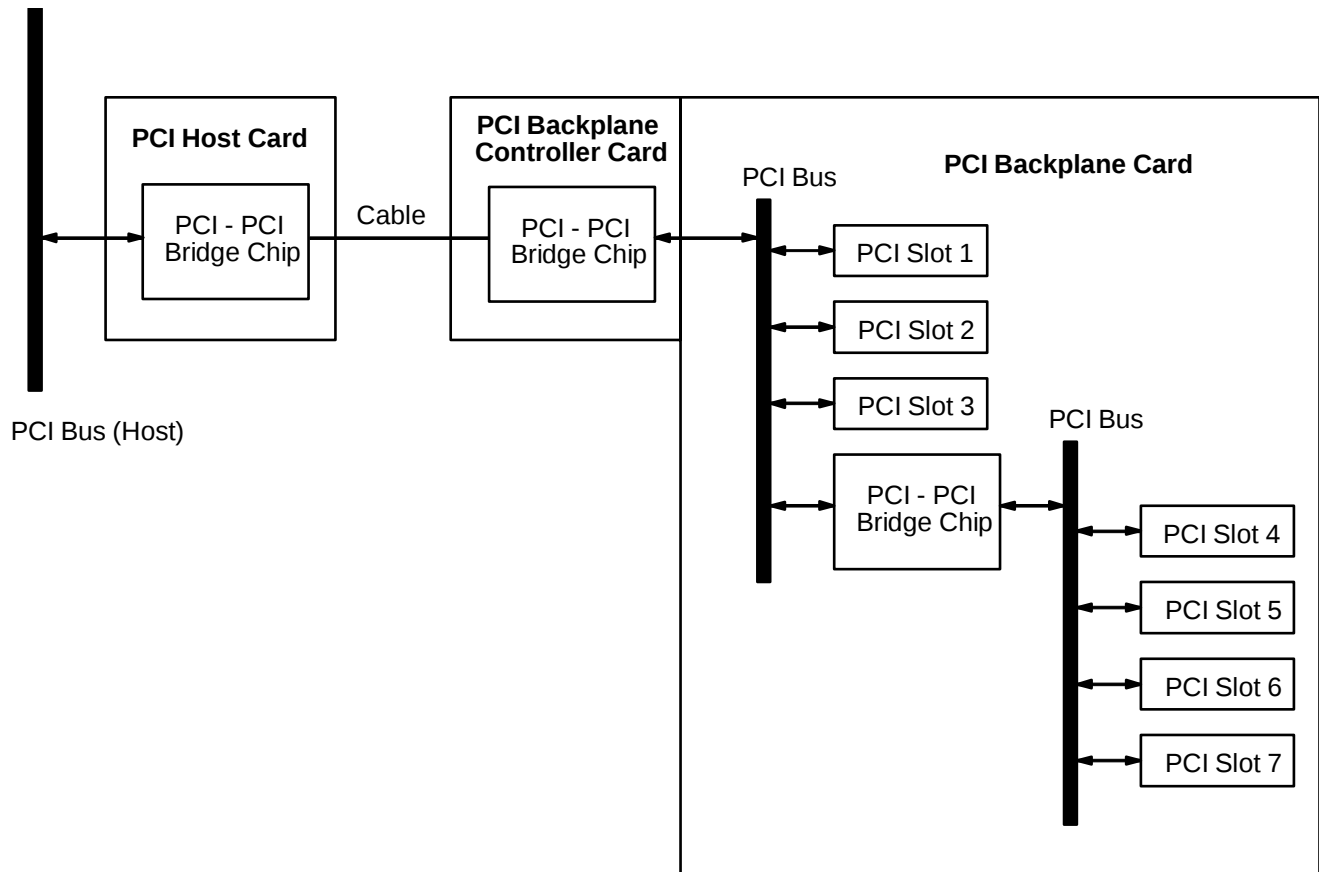
Slot	Board
Slot 1	NPRIF
Slot 2	DBPCI
Slot 3	(space)
Slot 4	AHA-2940UW
Slot 5	(space)
Slot 6	(space)
Slot 7	(space)

AHA-2940UW Card

This is a SCSI card of Adaptec. To this card, up to two hard disk drives can be connected for on-the-fly (high speed) raw data storage.

7-4 PCI EXPANSION UNIT (CONTINUED)

Illustration 7-2 PCI Expansion Unit



7-5 ST-1800 (SERIAL PORT EXTENSION BOX)

The host processor only provides two serial ports. To increase the number of available serial ports, the ST-1800 unit is used.

See Illustration 1-1 for the connection of the ST1800 unit within the operator console.

The unit is connected to the ultra/wide SCSI port of the host processor, and provides four serial ports available.

The serial ports may be used for connection with an InSite modem, a trackball, etc.

TABLE/GANTRY

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SECTION 1 - GENERAL DESCRIPTION

1-1 INTRODUCTION

The TGP (Table Gantry Processor) board is the main controller of the Table/Gantry subsystem. The TGP board receives command from the Operator Console and sends control commands to Table, Stationary Gantry and Rotating Gantry including OGP (On Gantry Processor), DAS and X-ray Generator. Although the DAS/Detector and X-ray Generator are in the Gantry, they are not explained in this subsystem.

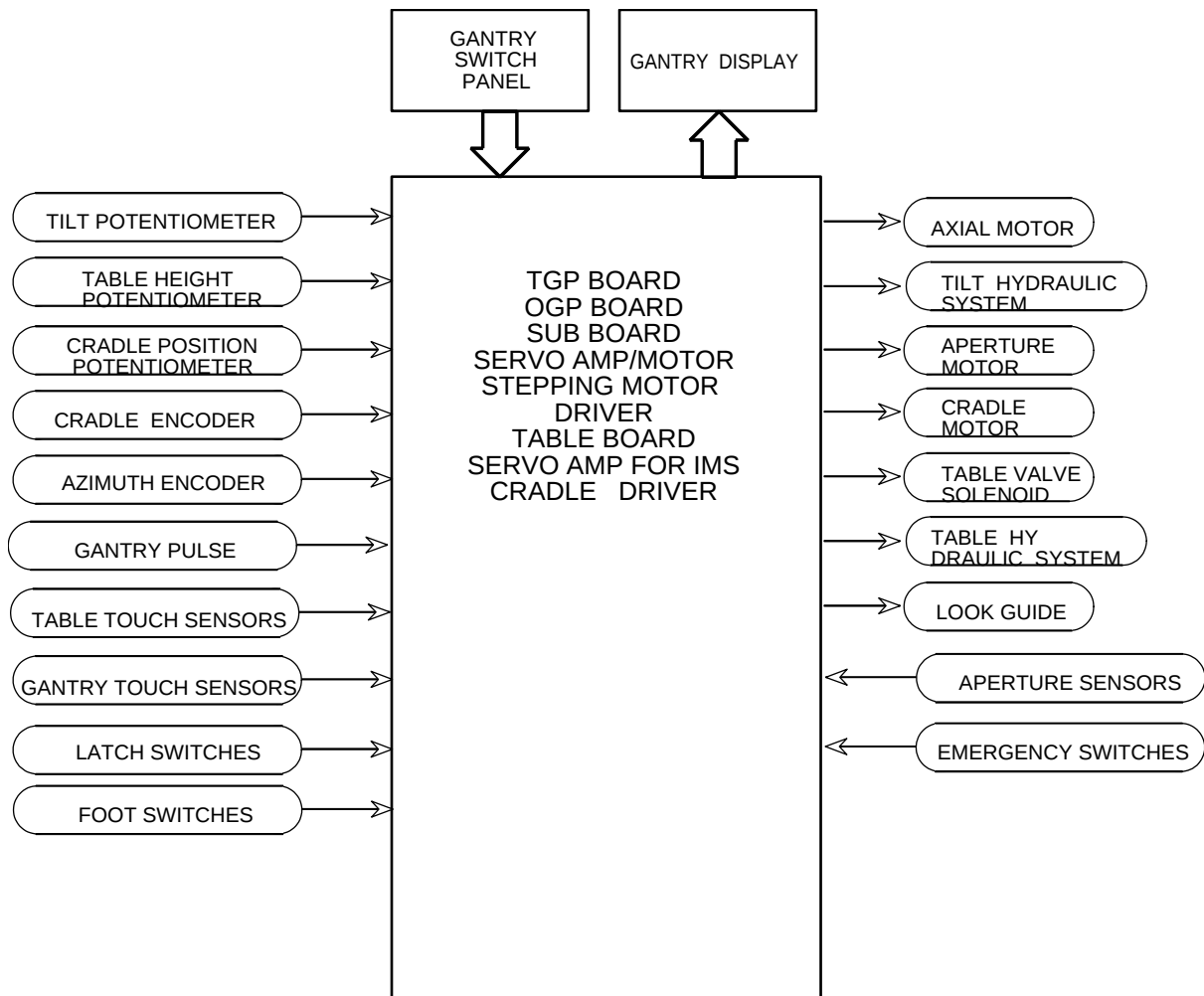
The Table/Gantry consists of the following components:

- TGP board
- OGP board
- SUB board
- Table board
- Servo Amp/Servo Motor
- Gantry Display
- Gantry Switch
- Collimator
- Positioning Light
- Hydraulic System (Gantry Tilt and Table elevation)
- Touch Sensors
- Cradle drive system

1-2 COMPONENTS INTERCONNECTION

The illustration 1-1 shows the components of the Table/Gantry.

Illustration 1-1 Table/Gantry



1-3 SPECIFICATIONS

The specifications of the Table/Gantry is as follows:

Gantry Rotation Speed

- 1, 1.5, 2, 3, 5 sec/rot.

Tilt Angle

- $20_{-} \pm 0.5_{-}$

Tilt Speed

- Approx. 1 sec / $_{-}$

Table Height

- 400 ~ 900 mm

UP/Down Speed

- **(For Table 2244226-x (called YMS Table))**
From 400 mm to 950 mm height: 30 sec -5 sec +10 sec.
- **(For Table 2297024 (called LCT Table))**
From 400 mm to 900 mm height: 24 sec -6 sec +10 sec.

Cradle Speed

- Slow 20 mm/sec
- Fast 100 mm/sec
- Scout 75 mm/sec
- Home 100 mm/sec

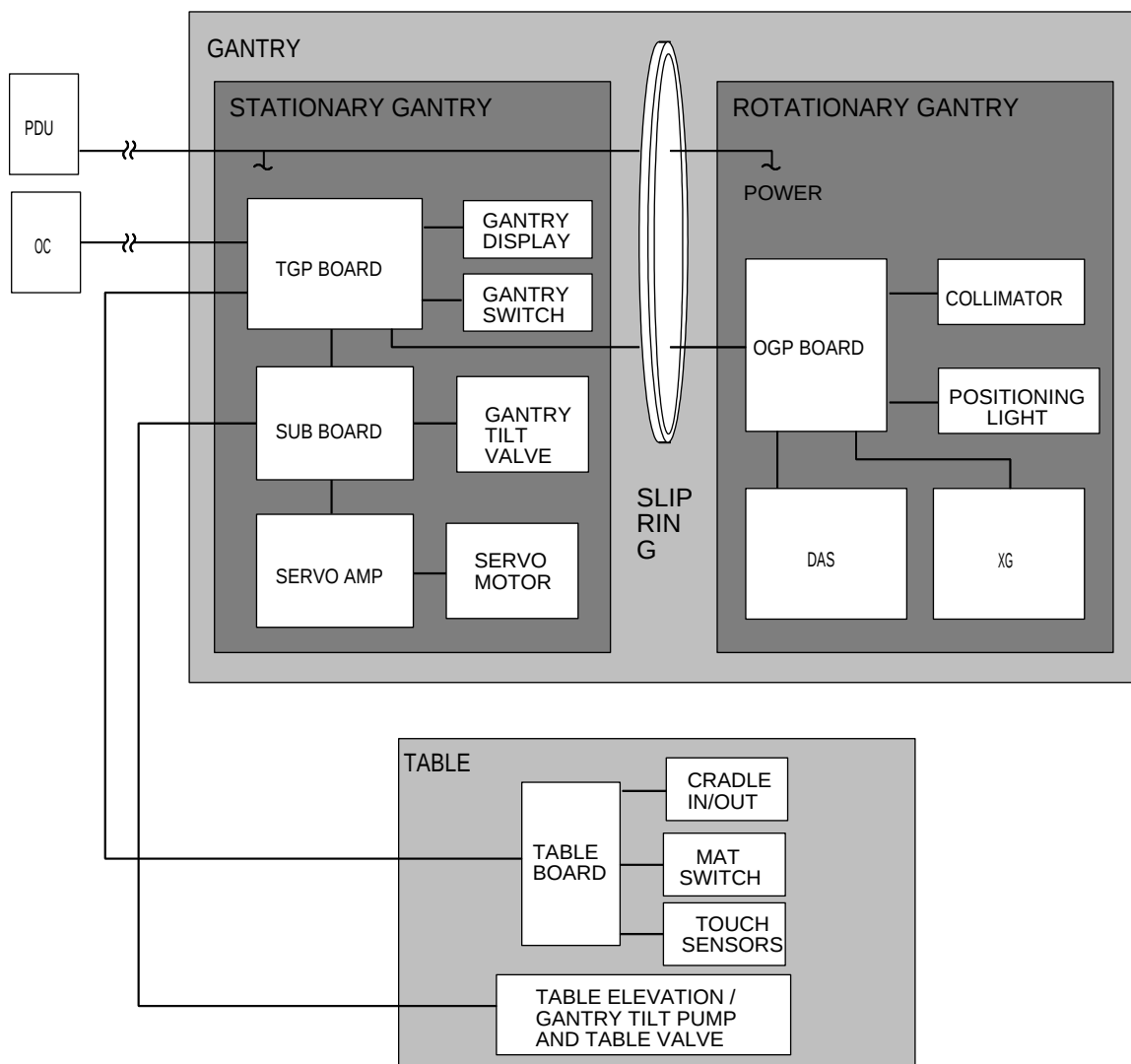
SECTION 2 - SUB-ASSEMBLY DESCRIPTION

2-1 OVERVIEW

The Table/Gantry consists of table and Gantry. The Gantry is divided into Stationary Gantry and Rotationaly Gantry. The communication between stationary and rotationaly Gantry is made by slip-ring, a rotation mechanism that permits electrical power and signals exchange.

The illustration 2-1 shows the Table/Gantry block diagram.

Illustration 2-1 Table/Gantry Block Diagram

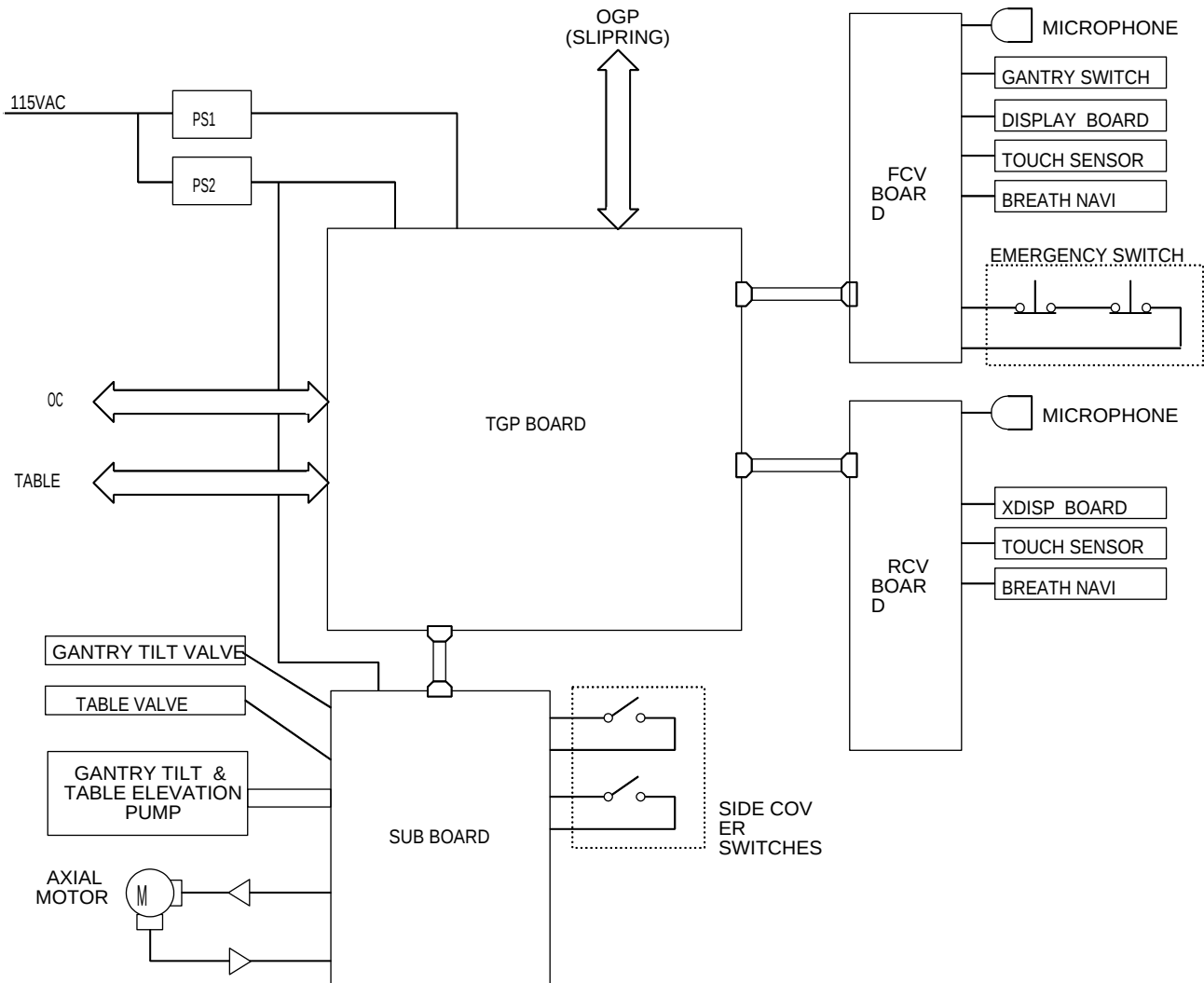


2-2 STATIONARY GANTRY

The stationary Gantry is mainly controlled by the TGP (Table Gantry Processor) board. The Illustration 2-2 shows the main components of the stationary Gantry.

The TGP board communicates with Operator Console and Table via cables and with the OGP board located in rotationary Gantry via cable and slipring.

Illustration 2-2 Stationary Gantry main components



The functions of the parts of the stationary Gantry are as follows:

PS1 and PS2

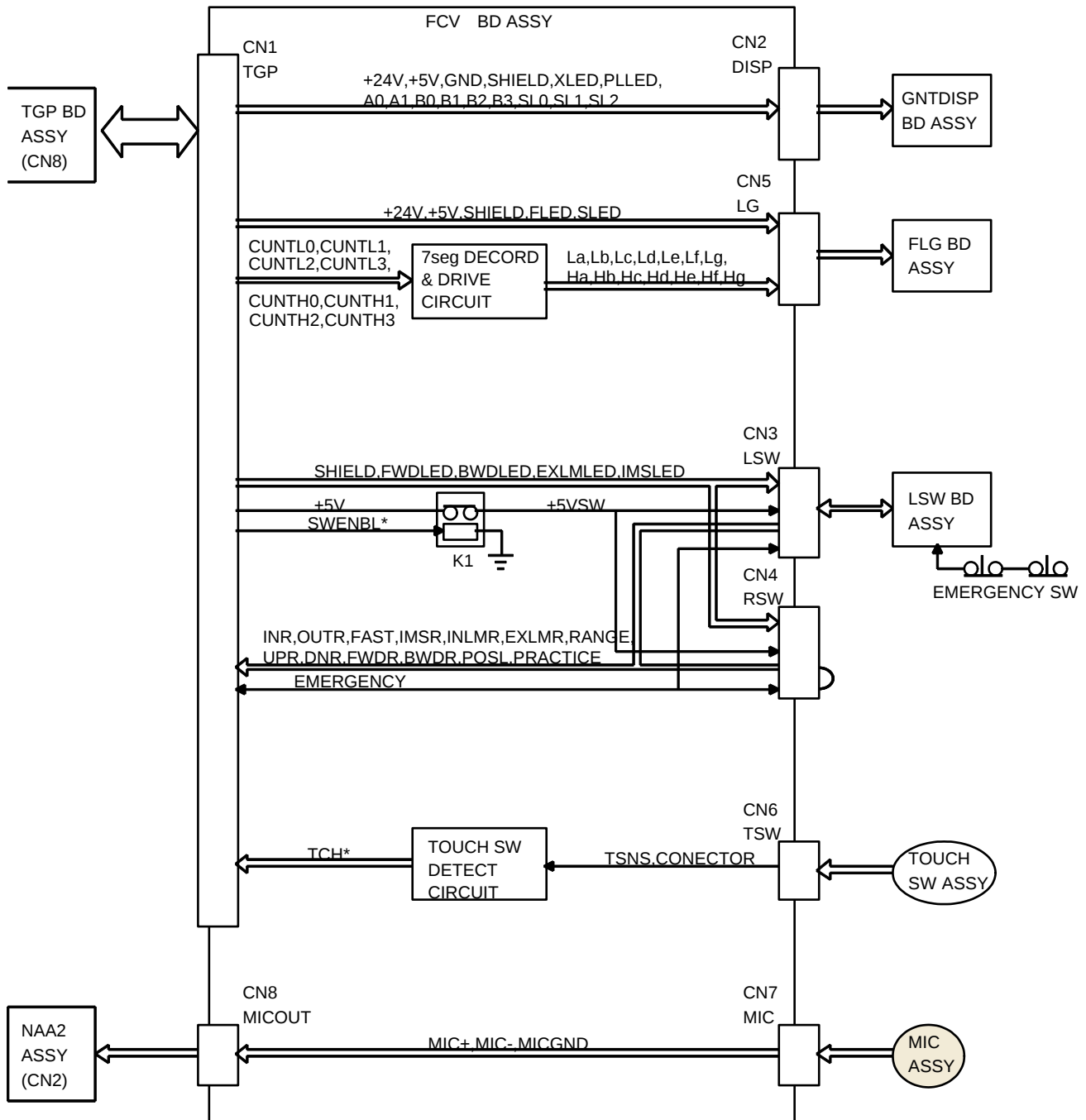
Supply power to TGP board and SUB board. PS1 supplies +5V, +12V and -12V. PS2 supplies +24V.

2-2 STATIONARY GANTRY (CONTINUED)

FCV (Front Cover) Board RCV (Rear Cover) Board

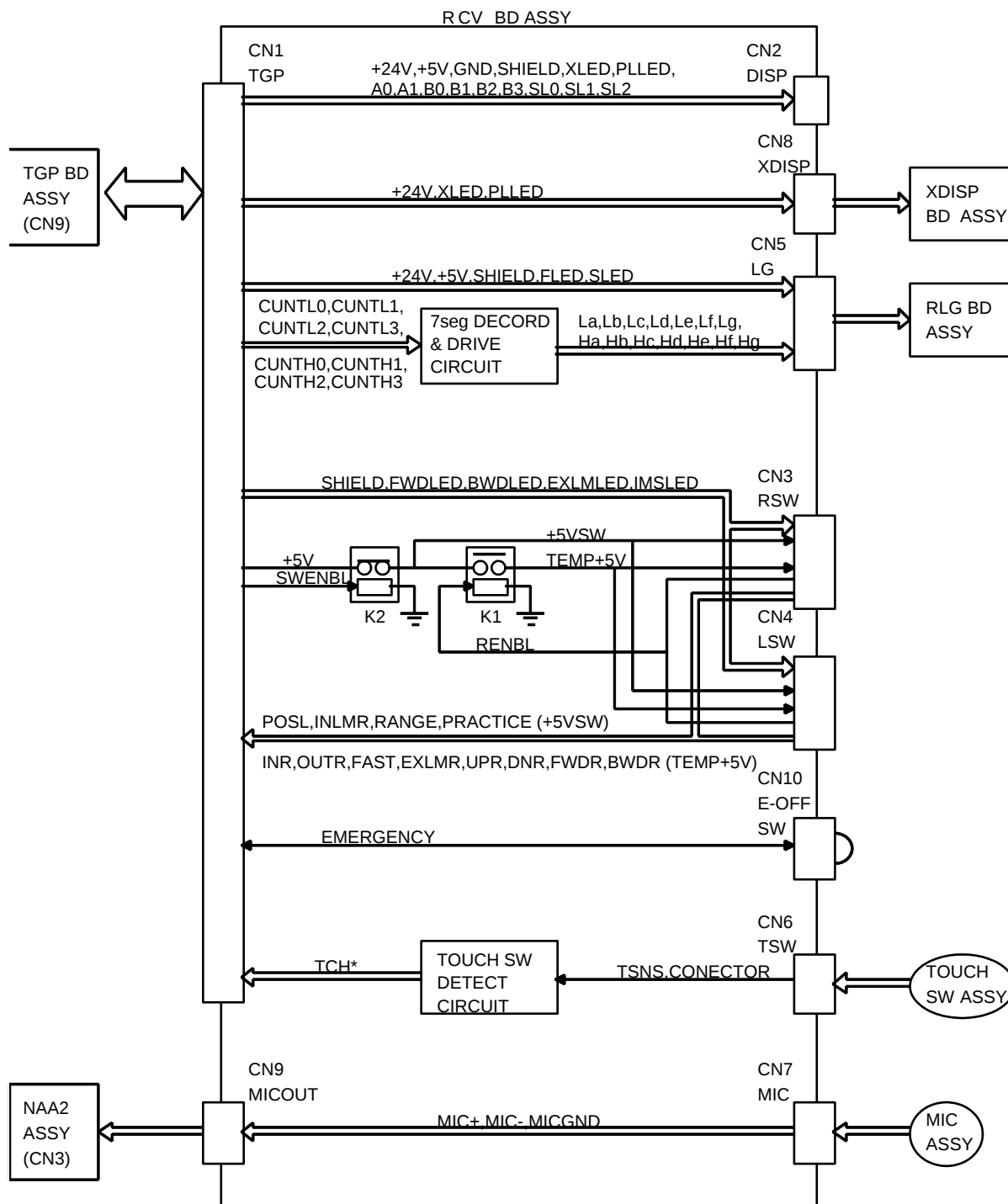
Contains connection circuitry to display board, touch sensors, breath navis and emergency switches.
See Illustration 2-3 and 2-4.

Illustration 2-3 FCV Block Diagram



2-2 STATIONARY GANTRY (CONTINUED)

Illustration 2-4 RCV Block Diagram



2-2 STATIONARY GANTRY (CONTINUED)

Display Board and XDISP board

Display board is the display located at middle upper side of the Gantry front cover.

XDISP board is the smaller display located at middle upper side of the Gantry rear cover.

Gantry Switches

Located at center of the front Gantry cover. These switches are used to tilt manage Gantry tilt, table and cradle movement and positioning light.

Gantry Microphone

Located at upper portion of the entrance of the Gantry opening, at the front and the rear side.

Touch Sensor

Located at front and at rear upper side of the Gantry cover to protect patient during tilt. When touch sensor at the front cover hit something during forward tilt, the tilt stops. When touch sensor at the rear cover hit something during backward tilt, the tilt stops.

Breath Navi

Located at upper portion of the entrance of the Gantry opening, at the front and the rear side to notify patient to breath, hold breath and show remaining scan time.

Emergency Switch

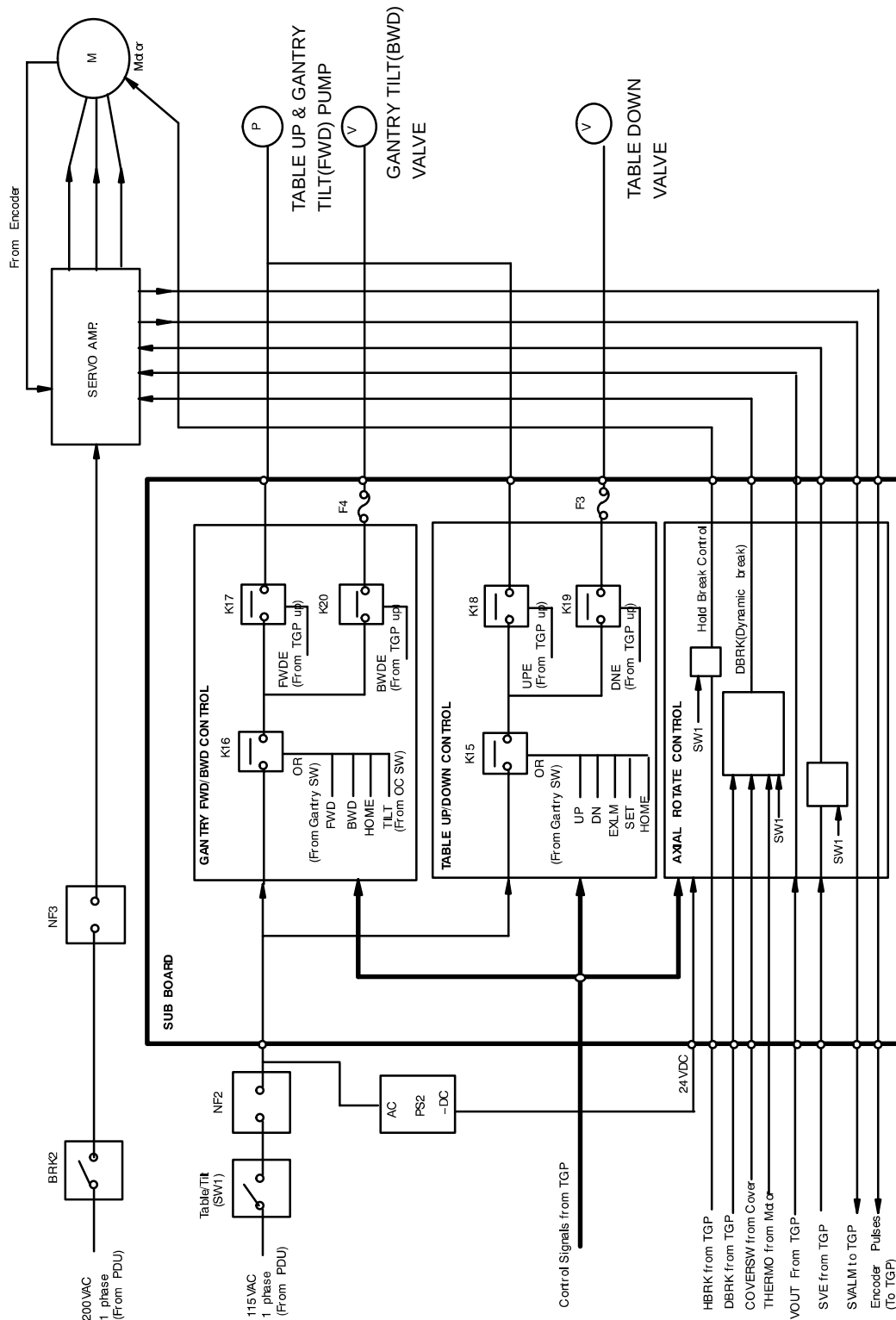
Located at left and right of both front Gantry cover.

SUB Board

The SUB board contains control circuitry for Gantry tilt, table elevation and servo amp for axial motor. Control these functions according to the command received from TGP board. Contains also connection to Gantry cover switches. See Illustration 2-5.

2-2 STATIONARY GANTRY (CONTINUED)

Illustration 2-5 SUB Board Block Diagram



2-2 STATIONARY GANTRY (CONTINUED)

TGP BOARD

There are three micro processors on the TGP Board. One controls the GANTRY Rotation, one controls the Table and the other controls the arbitration of commands from the gantry processor, table processor, scan processor (located on the OGP board) and the OC. See Illustration 2-6.

- Processor A for GANTRY CONTROL (GP)
- Processor B for TABLE CONTROL (TP)
- Processor C for MANAGEMENT (MP)

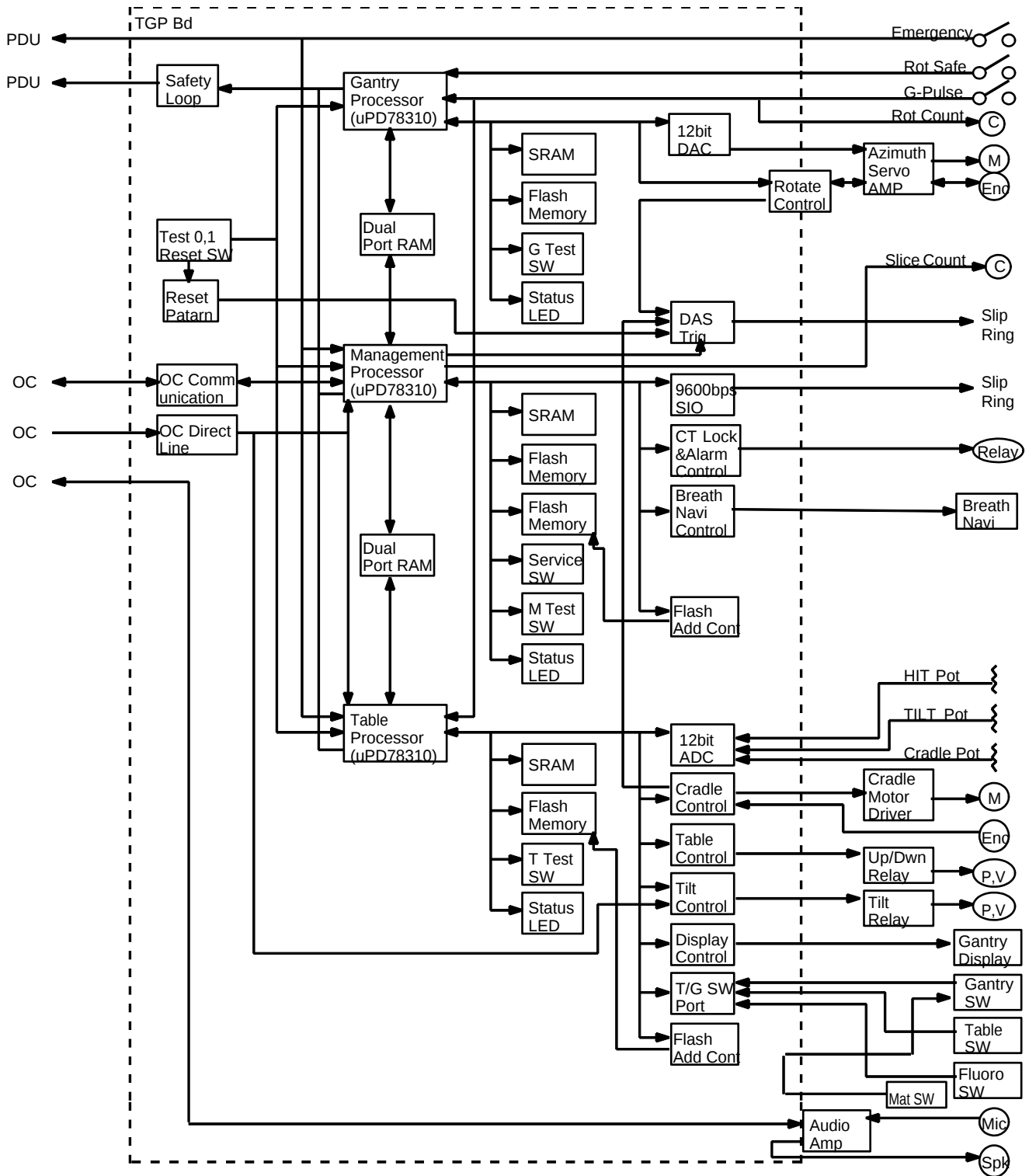
The Management processor communicates with the OC through serial links. The other processors (Gantry Processor and Table Processor) communicate with the Management Processor, and can receive commands from the OC via the Management Processor. The Gantry Processor and Table Processor also contain a serial communication port which is not used for communication between OC or other Processors, but rather is used for Data correction from the sensor switches.

The TGP Board issues commands *to* and receives status *from* the components it controls. The TGP oversees the following functions:

- AXIAL Drive control
- TILT Drive control
- CRADLE IN/OUT Drive control
- TABLE Elevation Drive control
- GANTRY Display control
- Breath Navi Display control
- GANTRY panel switch
- Error Detection

2-2 STATIONARY GANTRY (CONTINUED)

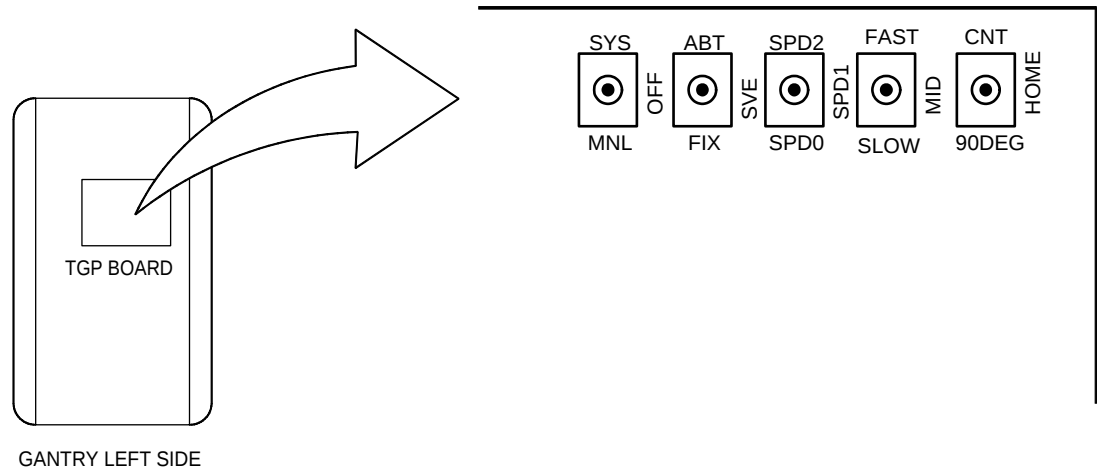
Illustration 2-6 TGP Block Diagram



2-2-1 TGP board Service Switches

There are five service switches at right upper side of the TGP board which are used to control the Gantry Rotation manually.

Illustration 2-7 TGP Board Service Switches



SYS : System Position. When the switch is in this position, the Gantry is controlled by the Operator Console.

OFF Disable the Gantry rotation. Servo Amplifier is disabled and Static brake activated.

MNL Manual Position. When the switch is in this position, the Gantry rotation is controlled manually, by the other switches described below.

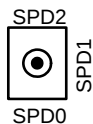


ABT : Arbitrary Mode. This switch is a spring loaded switch that enables Gantry rotation toward the direction selected by the rotation Direction switch (CNT/HOME/90DEG), by the fixed speed of XXX seconds per revolution.

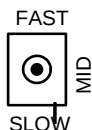
SVE : Servo Enable. Servo Amplifier is enabled and voltage command is 0 volts, that means there is no rotation at this position.

FIX : Rotates Gantry according to the selection of the Speed Selection switches (SPD2/SPD1/SPD0 and FAST/MID/SLOW) and Direction switch (CNT/HOME/90DEG).

2-2-1 TGP board Service Switches (continued)



and



These two switches sets the rotation speed
See table below

SPD2/SPD1/SPD0	SPD2	SPD2	SPD2	SPD1	SPD1	SPD1	SPD0	SPD0	SPD0
FAST/MID/SLOW	FAST	MID	SLOW	FAST	MID	SLOW	FAST	MID	SLOW
SPEED (sec/rot)	1.0	1.0	1.0	1.5	2	3	5	10	15



CNT : Clockwise rotation

HOME: Home position (X-ray tube at zero degree position)

90DEG: 90 degree position (X-ray tube at 90 degree position)

2-2-2 TGP Processors

The TGP board contains three processors:

Management Processor (MP)

The Management Processor oversees the functions of the Table/Gantry. It communicates with OC and according to the message received from OC, sends corresponding commands to Gantry processor, Table processor and OGP board.

The main functions of the Management processor are:

- Communication with OC - serial link
- Communication with OGP - serial link through slipping
- X-ray ON LED (on Gantry panel) control
- Positioning Light ON LED (on Gantry panel) control
- Look guide control
- Practice Switch (for look guide) control
- Tilt position, table height and cradle position adjustment. There is a ROM connected to management processor that contains adjustment data. The management processor reads this data, compares with the current positions and make adjustment as needed.

2-2-2 TGP Processors (continued)

Gantry Processor (GP)

The Gantry processor control the following functions:

- Positioning light switch
- Gantry rotation

Table Processor (TP)

The table processor control the following functions:

- Cradle In/Out
- Gantry Tilt
- Table Up/Down
- Gantry Display
- Gantry Switch
- Interlock

2-3 ROTATIONARY GANTRY

The Illustration 2-8 shows the main components of the rotary Gantry.

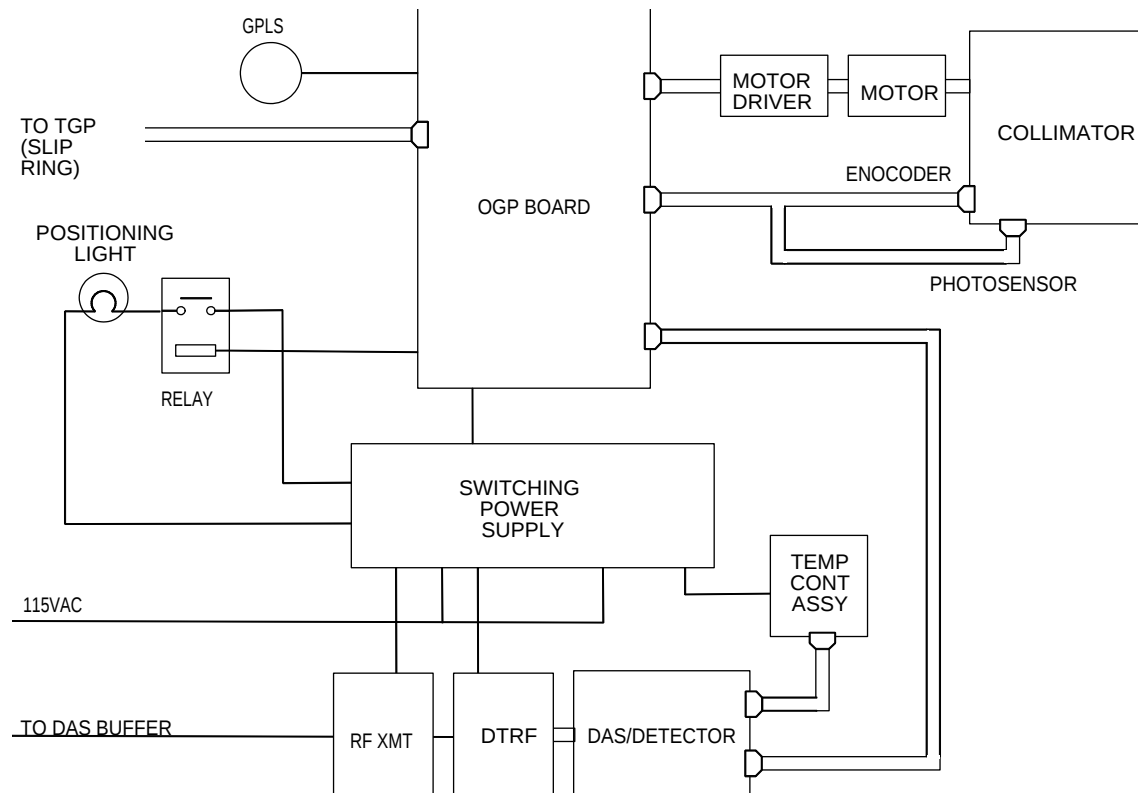
The functions of the parts of the stationary Gantry are as follows:

OGP Board

The OGP (On Gantry Processor) performs the following functions:
(For detail, refer to section 3, Functional Description.)

- X-ray exposure on/off control
- DAS data transfer timing
- Collimator control
- Positioning light control
- Scan control
- The automatic shut-off of the Tube Fan/Pump Power Supply after 30 minutes when the OC has been powered down.

Illustration 2-8 Rotatory Gantry main components



2-3 ROTATIONARY GANTRY (CONTINUED)

Switching Power Supply

Supply power to the OGP board, DTRF board, RF transmitter, Temp cont, DAS, and positioning light.

Supply power to the DAS and Temperature Control Box.

Collimator

Located at the exposure window of the X-ray tube, controls the aperture of the X-ray beam by moving the blades. The aperture can be 2,3,5,7 or 10 mm.

Motor Driver

Generates five phase pulses to control the stepping motor of the collimator. Receives pulse command from OGP board and convert it to other type of pulses.

Encoder

Sends the feedback pulse to the OGP to show the moved amount of the blades.

Photo Sensor

Detects when the collimator blades are in 1mm aperture

DAS

Data Acquisition System. Processes the data received from detector and send it to operator console. The detailed explanations are in the DAS/Detector sections.

Temp Cont Assy

Device that controls the Detector temperature

DTRF

Receives parallel data from DAS and convert them to serial data. The detailed explanations are in the DAS/Detector sections.

RF XMT

Converts Serial signal from DTRF to RF signal.

GPLS

Notify TGP and OGP board when the Gantry is at zero degree tube position.

2-4 SLIP RING

The SLIP RING transfers the following signals;

- DAS Data
- DAS Trigger
- TGP and OGP Communication message
- Safety Loop

2-4-1 MECHANISM

This Gantry slip ring system utilizes:

- Nine 480VAC power brushes (3 power lines x3 brushes)
- Four 115VAC power brushed (2 power lines x2 brushes)
- Three ground brushes (1 ground line x3 brushes)
- Twenty-four signal brushes (6 signal lines x 4 brushes)
- RF transmitter / receiver modules

Every slip ring has a corresponding terminator located on the opposite side of the transmitter terminal. See illustration 2-9.

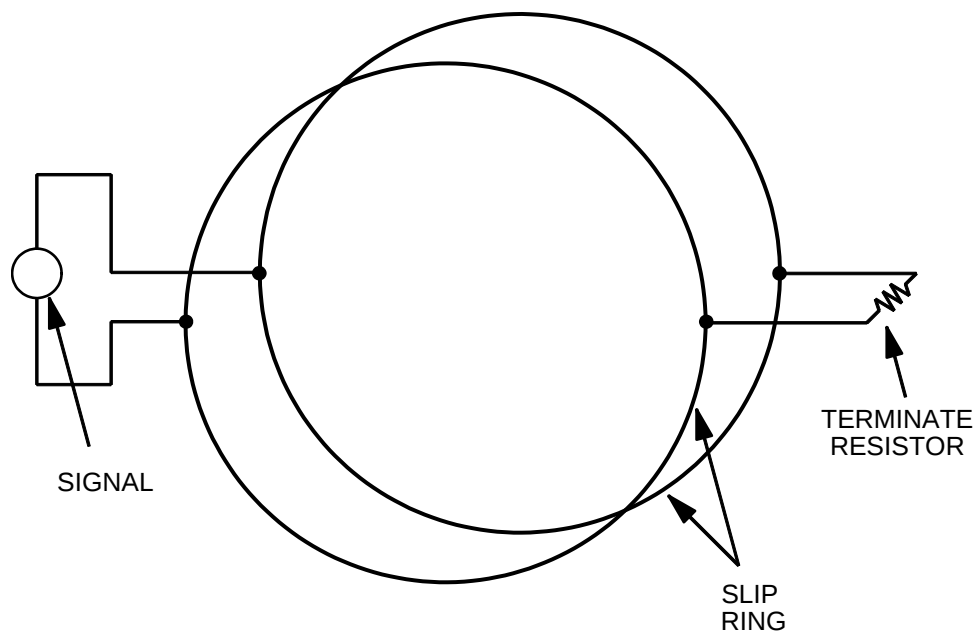


Illustration 2-9 Slip Ring Terminator

The characteristic Impedance should be less than or equal to approx. 50W.

2-5 TABLE

The Illustration 2-10 shows the main components of the table.

The description of the parts of the Table follows:

Table board

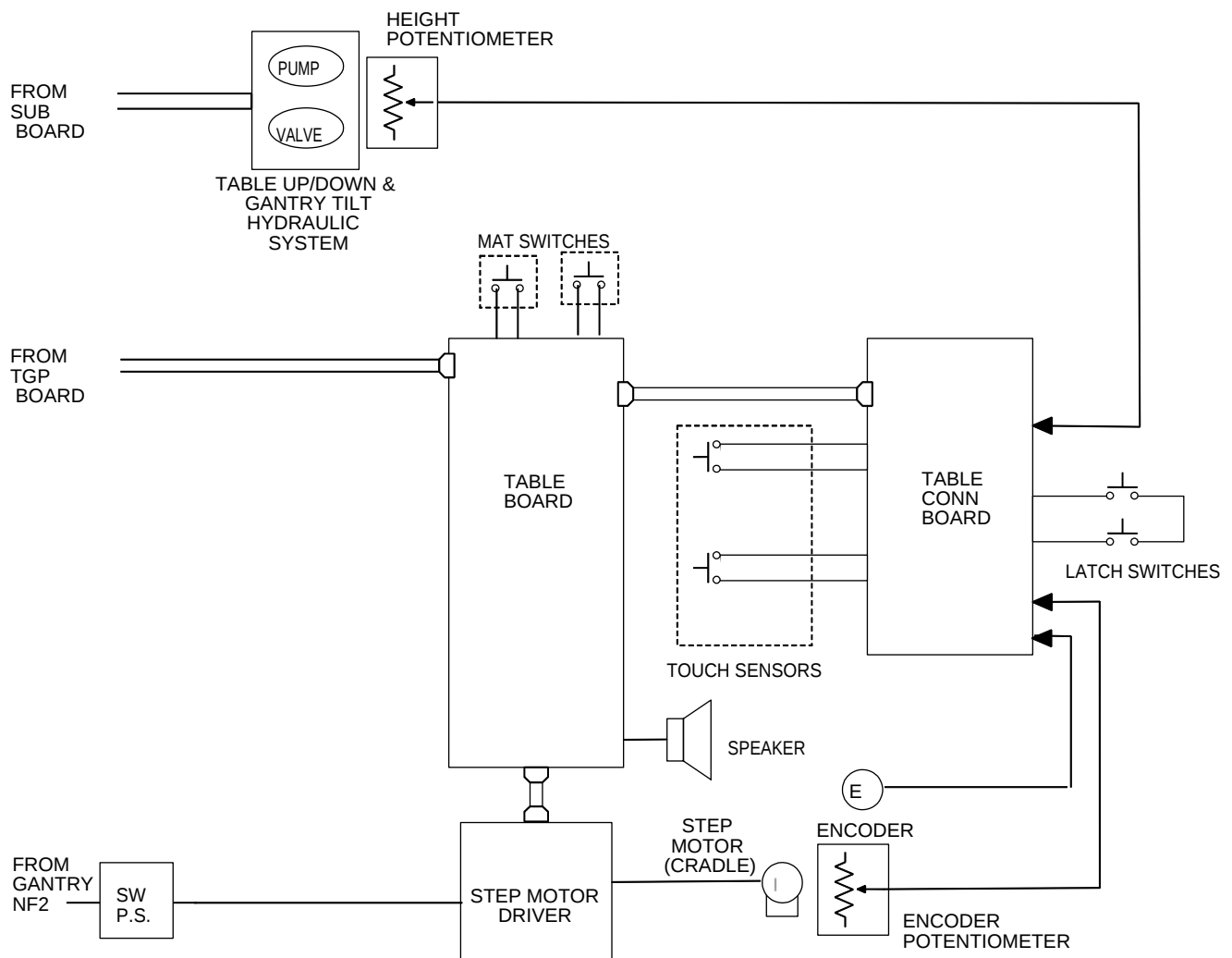
This is an interface board between TGP board and servo amp, stepping motor driver, and table CONN board.

TBL CONN board

This is an interface between Table board and potentiometers, touch sensors and latch switches.

This board has only connectors. For detail information, see schematic diagrams.

Illustration 2-10 Table



2-5 TABLE (CONTINUED)

Hydraulic System

Consists of pump, hose and cylinder. it is used for Table Up/Down and Gantry Tilt.

Cradle

Portion of the Table that executes longitudinal movement. It is controlled by step motor and motor driver.

Latch Switches

Positioned at both right and left sides of the Table, these switches release or latch the cradle. When both switches are pressed, the cradle is latched. When one of the switches is depressed, the cradle is released. They are for safety purpose.

Potentiometers

There are three potentiometers: Height potentiometer and Encoder (tilt) potentiometer. They are used for feedback purpose.

Touch Sensors

Located at under surface of the Table. They are for safety purpose.

Mat Switches

Located at both right and left sides of the table base. The Gantry panel switch can be available with the mat switch ON.

SECTION 3 - FUNCTIONAL DESCRIPTION

3-1 GANTRY TILT SYSTEM

The illustration 3-1 shows Gantry tilt control circuit. Following are the logics for tilt operation for which this circuit is designed for:

- Forward tilt is activated by tilt hydraulic pump.
- Backward tilt is performed by opening the tilt valve to drain the hydraulic oil, i. e., the gravity is the only external force for backward tilt.
- When the forward tilt switch is pressed, the backward tilt switch has no effect, and vice-versa.
- FWD signal is directly connected to forward tilt switch, but FWDE (forward enable) is not. FWDE turns active only if the TGP board permits. In other words, only if interlock condition is not occurring.

Illustration 3-1 Gantry Tilt System

