SECTION 15
MODULAR INPUT/OUTPUT SUBSYSTEM (MIOS1)

The modular I/O system (MIOS) consists of a library of flexible I/O and timer functions including I/O port, counters, input capture, output compare, pulse and period measurement, PWM and angle degree clock. Because the MIOS is composed of submodules, it is easily configurable for different kinds of applications. MIOS1 is the implementation of the MIOS architecture used in the MPC555.

The MIOS1 is composed of the following submodules:

- 1 MIOS bus interface submodule (MBISM)
- 1 MIOS counter prescaler submodule (MCPSM)
- 2 MIOS modulus counter submodules (MMCSM)
- 10 MIOS double action submodules (MDASM)
- 8 MIOS pulse width modulation submodules (MPWMSM)
- 1 MIOS 16-bit parallel port I/O submodule (MPIOSM)
- 2 MIOS interrupt request submodules (MIRSM)

15.1 MIOS1 Features

The basic features of the MIOS1 are as follows:

- Modular architecture at the silicon implementation level
- Disable capability in each submodule to allow power saving when its function is not needed
- Two 16-bit buses to allow action submodules to use counter data
- When not used for timing functions, every channel pin can be used as a port pin: I/O, output only or input only, depending on the channel function
- Submodules pin status bits:
- MIOS counter prescaler submodule (MCPSM):
  - — Centralized counter clock generator
  - — Programmable 4-bit modulus down-counter
  - — Wide range of possible division ratios: 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 and 16
  - — Count inhibit under software control
- Two MIOS modulus counter submodules (MMCSM), each with these features:
  - — Programmable 16-bit modulus up-counter with built-in programmable 8-bit prescaler clocked by MCPSM output
  - — Maximum increment frequency of the counter:
    - clocked by the internal Counter Clock: fSYS /2
    - clocked by the external pin: fSYS /4
  - — Flag setting and possible interrupt generation on overflow of the up-counter
  - — Time counter on internal clock with interrupt capability after a pre-determined time

— Optional pin usable as an external event counter (pulse accumulator) with overflow and interrupt capability after a pre-determined number of external events
— Usable as a regular free-running up-counter
— Capable of driving a dedicated 16-bit counter bus to provide timing information to action submodules — the value driven is the contents of the 16-bit up-counter register
— Optional pin to externally force a load of the counter with modulus value

- Ten MIOS double action submodules (MDASM), each with these features:
  - — Versatile 16-bit dual action unit allowing two events to occur before software intervention is required
  - — Six software selectable modes allowing the MDASM to perform pulse width and period measurements, PWM generation, single input capture and output compare operations as well as port functions
  - — Software selection of one of the two possible 16-bit counter buses used for timing operations
  - — Flag setting and possible interrupt generation after MDASM action completion
  - — Software selection of output pulse polarity
  - — Software selection of totem-pole or open-drain output
  - — Software readable output pin status
- Eight MIOS pulse width modulation submodules (MPWMSM), each with these features:
  - — Output pulse width modulated (PWM) signal generation with no software involvement
  - — Built-in 8-bit programmable prescaler clocked by the MCPSM
  - — PWM period and pulse width values provided by software:
    - Double-buffered for glitch-free period and pulse width changes
    - 2-cycle minimum output period/pulse-width increment (50 ns at fSYS = 40 MHz)
    - 50% duty-cycle output maximum frequency: 10 MHz
    - Up to 16 bits output pulse width resolution
    - Wide range of periods:
      - — 16 bits of resolution: period range from 3.27 ms (with 50 ns steps) to 6.71 s (with 102.4 μs steps)
      - — 8 bits of resolution: period range from 12.8 μs (with 50 ns steps) to 26.2 ms (with 102.4 μs steps)
    - Wide range of frequencies:
      - — Maximum output frequency at fSYS = 40 MHz with 16 bits of resolution and divide-by-2 prescaler selection: 305 Hz (3.27 ms.)
      - — Minimum output frequency at fSYS = 40 MHz with 16 bits of resolution and divide-by-4096 prescaler selection: 0.15 Hz (6.7 s.)
      - — Maximum output frequency at fSYS = 40 MHz with 8 bits of resolution and divide-by-2 prescaler selection: 78125 Hz (12.8 μs.)
      - — Minimum output frequency at fSYS = 40 MHz with 8 bits of resolution and divide-by-4096 prescaler selection: 38.14 Hz (26.2 ms.)
  - — Programmable duty cycle from 0% to 100%
  - — Possible interrupt generation after every period

— Software selectable output pulse polarity
— Software readable output pin status
— Possible use of pin as I/O port when PWM function is not needed

• MIOS 16-bit parallel port I/O submodule (MPIOSM):
— 16 parallel input/output pins
— Simple data direction register (DDR) concept for selection of pin direction

15.2 Submodule Numbering, Naming and Addressing

A block is a group of four 16-bit registers. Each of the blocks within the MIOS1 addressing range is assigned a block number. The first block is located at the base address of the MIOS1. The blocks are numbered sequentially starting from 0.

Every submodule instantiation is also assigned a number. The number of a given submodule is the block number of the first block of this submodule.

A submodule is assigned a name made of its acronym followed by its submodule number. For example, if submodule number 18 were an MPWMSM, it would be named MPWMSM18.

This numbering convention does not apply to the MBISM, the MCPSM and the MIRSMs. The MBISM and the MCPSM are unique in the MIOS1 and do not need a number. The MIRSMs are numbered incrementally starting from zero.

The MIOS1 base address is defined at the chip level and is referred to as the “MIOS1 base address.” The MIOS1 addressable range is 4 Kbytes.

The base address of a given implemented submodule within the MIOS1 is the sum of the base address of the MIOS1 and the submodule number multiplied by eight. (Refer to **Table 15-36**.)

This does not apply to the MBISM, the MCPSM and the MIRSMs. For these submodules, refer to the MIOS1 memory map (**Figure 15-2**).

15.3 MIOS1 Signals

The MIOS1 requires 34 pins: 10 MDASM pins, 8 MPWMSM pins and 16 MPIOSM pins. The usage of these pins is shown in the block diagram of **Figure 15-1** and in the configuration description of **Table 15-36**. In the figure, MDASM pins have a prefix MDA, MPWMSM pins have a prefix of MPWM and the port pins have a prefix of MPIO. The modulus counter clock and load pins are multiplexed with MDASM pins.

The MIOS1 input and output pin names are composed of five fields according to the following convention:

• “M”
• <submodule short_prefix>
• <submodule number>
• <pin attribute suffix> (optional)
• <bit number> (optional)

The pin prefix and suffix for the different MIOS submodules are as follows:

- MMCSM:
  - — submodule short_prefix: “MC”
  - — pin attribute suffix: C for the Clock pin
  - — pin attribute suffix: L for the Load pin
  - — For example, an MMCSM placed as submodule number n would have its corresponding input clock pin named MMCnC and its input load pin named MMCnL. On the MPC555 MMC6C is input on MDA11 and MMC22C is input on MDA13. The MMC6L is input on MDA12 and MMC22C is input on MDA14.
- MDASM:
  - — submodule short_prefix: “DA”
  - — pin attribute suffix: none
  - — For example a MDASM placed as submodule number n would have its corresponding channel I/O pin named MDAn
- MPWMSM:
  - — submodule short_prefix: “PWM”
  - — pin attribute suffix: none
  - — For example a MPWMSM placed as submodule number n would have its corresponding channel I/O pin named MPWMn
- MPIOSM:
  - — submodule short_prefix: “PIO”
  - — pin attribute suffix: B
  - — For example a MPIOSM placed as submodule number n would have its corresponding I/O pins named MPIOnB0 to MPIOnB15 for bit-0 to bit-15, respectively.

In the MIOS1, some pins are multiplexed between submodules using the same pin names for the inputs and outputs which are connected as shown in **Table 15-36**.

15.4 Block Diagram

Figure 15-1 is a block diagram of the MIOS1.

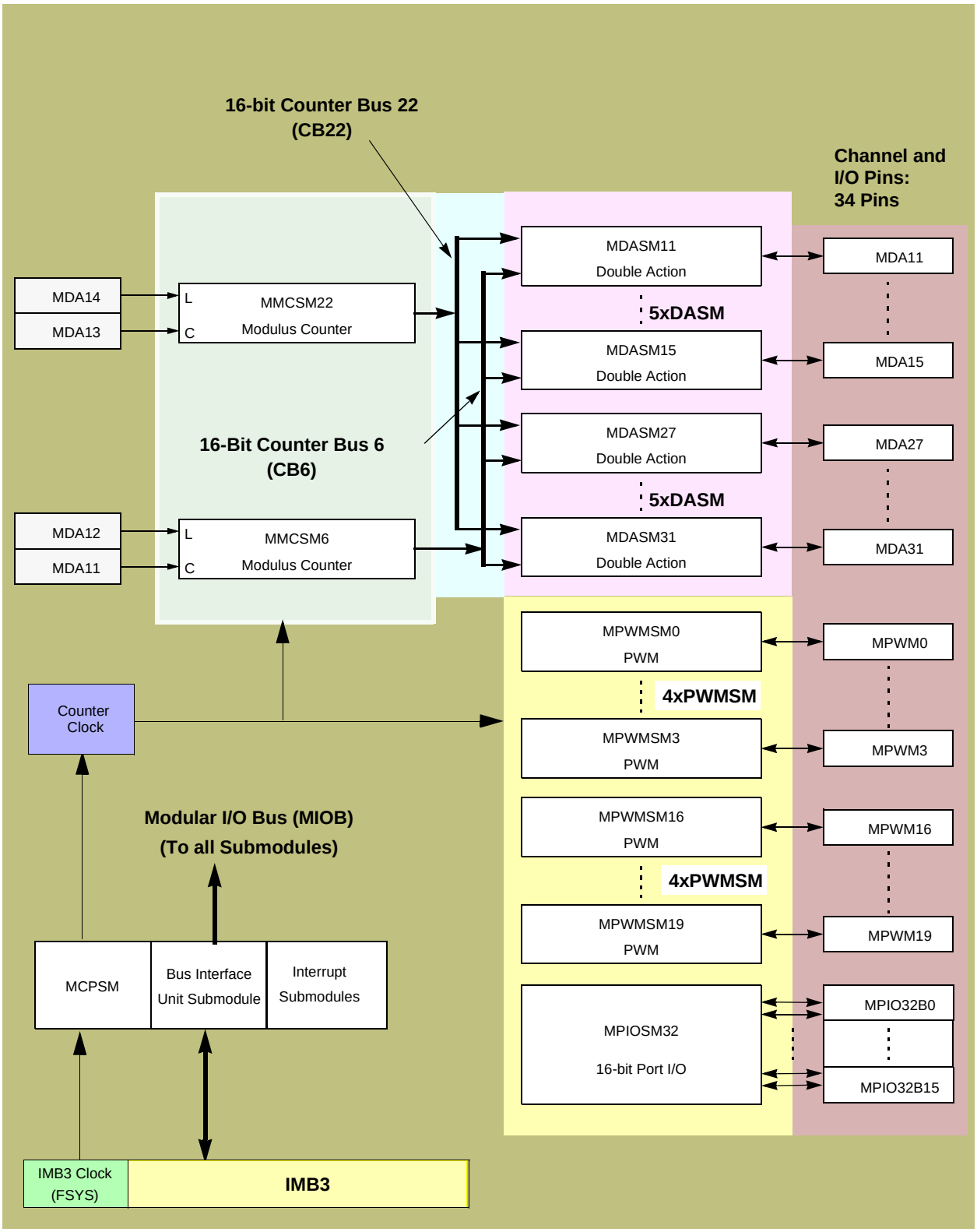

Figure 15-1 MIOS1 Block Diagram

15.5 MIOS1 Bus System

The internal bus system within the MIOS1 is called the modular I/O bus (MIOB). The MIOB makes communications possible between any submodule and the IMB3 bus master through the MBISM.

The MIOB is divided into three dedicated buses:

- The read/write and control bus
- The request bus
- The counter bus set

15.5.1 Read/Write and Control Bus

The read/write and control bus (RWCB) allows read and write data transfers to and from any I/O submodule through the MBISM. It includes signals for data and addresses as well as control signals. The control signals allow 16-bit simple synchronous single master accesses and supports fast or slow master accesses.

15.5.2 Request Bus

The request bus (RQB) provides interrupt request signals along with I/O submodule identification and priority information to the MBISM.

Note that some submodules do not generate interrupts and are therefore independent of the RQB.

15.5.3 Counter Bus Set

The 16-bit counter bus set (CBS) is a set of two 16-bit counter buses. The CBS makes it possible to transfer information between submodules. Typically, counter submodules drive the CBS, while action submodules process the data on these buses. Note, however, that some submodules are self-contained and therefore independent of the counter bus set.

15.6 MIOS1 Programmer's Model

The address space of the MIOS1 consist of 4 Kbytes starting at the base address of the module. The MIOS1 base address is a multiple of the addressable range. The overall address map organization is shown in **Figure 15-2**.

To find the base address of a given implementation, refer to **1.3 MPC555 Address Map**. To find the submodule base address, refer to **Table 15-36**.

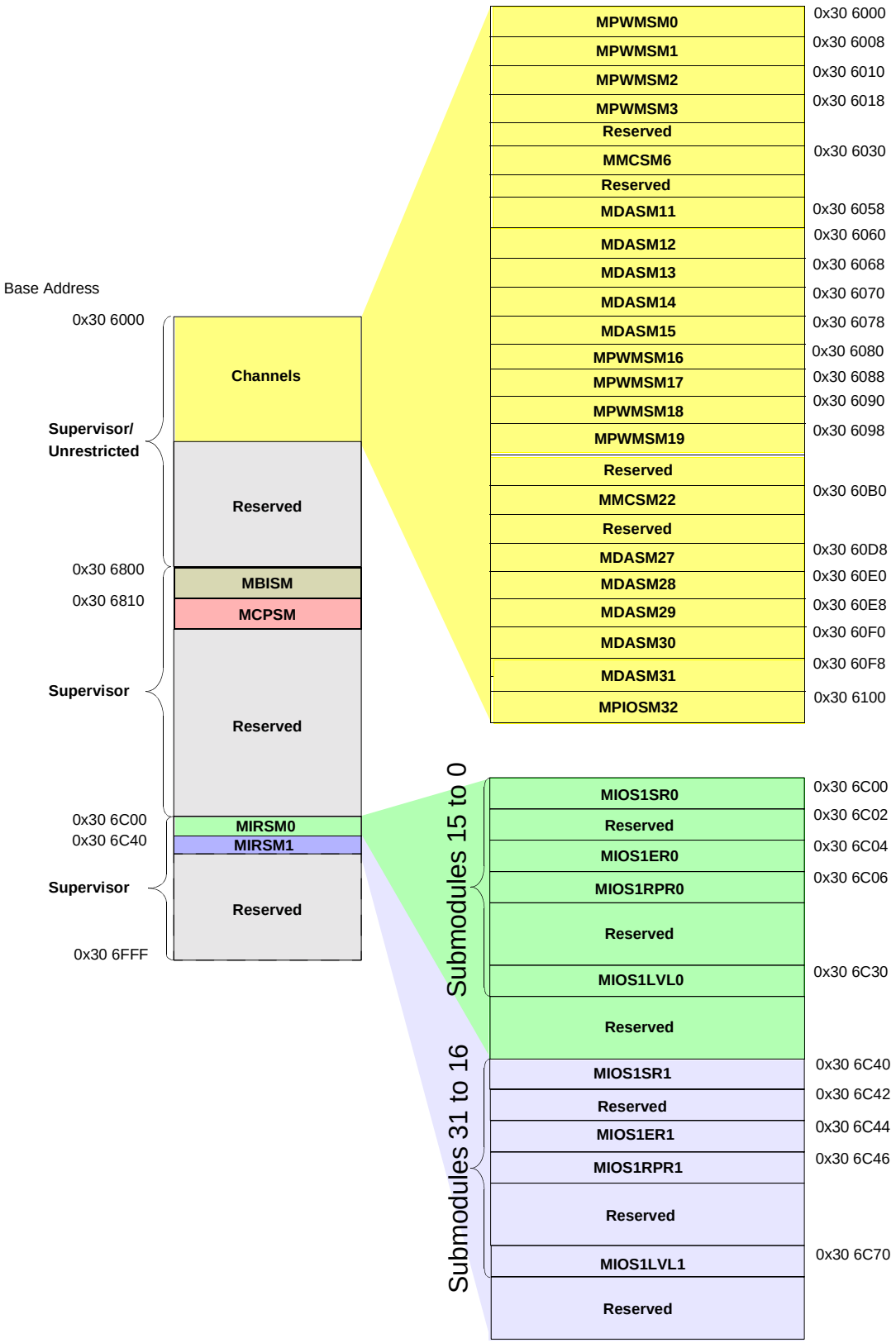

Figure 15-2 MIOS1 Memory Map

If a supervisor privilege address space is accessed in user mode, the module returns a bus error.

All MIOS1 unimplemented locations within the addressable range, return a logic 0 when accessed. In addition, the internal $\overline{\text{TEA}}$ (transfer error acknowledge) signal is asserted.

All unused bits within MIOS1 registers return a 0 when accessed.

15.7 MIOS1 I/O Ports

Each pin of each submodule can be used as an input, output, or I/O port:

Table 15-1 MIOS1 I/O Ports

Submodule	Number	Type
MPIOSM	16	I/O
MMCSM	2	Input
MDASM	1	I/O
MPWMSM	1	I/O

15.8 MIOS Bus Interface Submodule (MBISM)

The MIOS bus interface submodule (MBISM) is used as an interface between the MIOB (modular I/O bus) and the IMB3. It allows the CPU to communicate with the MIOS1 submodules.

15.8.1 MIOS Bus Interface (MBISM) Registers

Table 15-2 is the address map for the MBISM submodule.

Table 15-2 MBISM Address Map

Address	Register
0x30 6800	MIOS1 Test and Pin Control Register (MIOS1TPCR) See **Table 15-3** for bit descriptions.
0x30 6802	Reserved (MIOS1 Vector Register in some implementations
0x30 6804	MIOS1 Module Version Number Register (MIOS1VNR) See **Table 15-4** for bit descriptions.
0x30 6806	MIOS1 Module Control Register (MIOS1MCR) See **Table 15-4** for bit descriptions.
0x30 6808 – 0x30 680E	Reserved

15.8.1.1 MIOS1 Test and Pin Control Register

MIOS1TPCR — Test and Pin Control Register **0x30 6800**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
TEST	RESERVED													VF	VFLS
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register is used for MIOS1 factory testing and selecting between the MIOS1 pin functions for the MPIO32B[0:3] and the developement support pin functions of VFLS[0:1] and VF[0-2].

Table 15-3 MIOS1TPCR Bit Settings

Bit(s)	Name	Description
0	TEST	This bit is reserved for factory testing of the MIOS1. The test mode is disabled by reset.
1:13	—	Reserved
14	VF	Pin multiplex. This bit is used to determine the usage of the MIOS1 pins. Refer to the pad-ring specification of the chip for details about the usage of this bit. This bit is set to 0 by reset. 0 = the concerned pins are dedicated to the MIOS1. 1 = alternate function
15	VFLS	Pin multiplex. This bit is used to determine the usage of the MIOS1 pins. Refer to the pad-ring specification of the chip for details about the usage of this bit. This bit is set to 0 by reset. 0 = the concerned pins are dedicated to the MIOS1. 1 = alternate function

15.8.1.2 MIOS1 Vector Register

This register is used only in MCUs that use vectored interrupts. The MPC555 does not use this register.

15.8.1.3 MIOS1 Module and Version Number Register

This read-only register contains the hard-coded values of the module and version number.

MIOS1VNR — MIOS1 Module/Version Number Register **0x30 6804**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
MN								VN							

Table 15-4 MIOS1VNR Bit Settings

Bit(s)	Name	Description
0:7	MN	Module number = 1 on the MPC555. The MPC555 implements the MIOS1 module.
8:15	VN	Version number

15.8.1.4 MIOS1 Module Configuration Register

MIOS1MCR — MIOS1 Module Configuration Register **0x30 6806**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
STOP	0	FRZ	RST	RESERVED				SUPV	RESERVED			RESERVED (IARB)			
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 15-5 MIOS1MCR Bit Settings

Bit(s)	Name	Description
0	STOP	Stop enable. Setting the STOP bit activates the MIOB freeze signal regardless of the state of the IMB3 FREEZE signal. The MIOB freeze signal is further validated in some submodules with internal freeze enable bits in order for the submodule to be stopped. The MBISM continues to operate to allow the CPU access to the submodule's registers. The MIOB freeze signal remains active until reset or until the STOP bit is written to zero by the CPU (via the IMB3). The STOP bit is cleared by reset. 0 = Enables MIOS1 operation. 1 = Selectively stops MIOS1 operation.
1	—	Reserved
2	FRZ	Freeze enable. Setting the FRZ bit, activates the MIOB freeze signal only when the IMB3 FREEZE signal is active. The MIOB freeze signal is further validated in some submodules with internal freeze enable bits in order for the submodule to be frozen. The MBISM continues to operate to allow the CPU access to the submodule's registers. The MIOB freeze signal remains active until the FRZ bit is written to zero or the IMB3 FREEZE signal is negated. The FRZ bit is cleared by reset. 0 = Ignores the FREEZE signal on the IMB3, allowing MIOS1 operation. 1 = Selectively stops MIOS1 operation when the FREEZE signal appears on the IMB3.
3	RST	Module reset. The RST bit always returns 0 when read and can be written to 1. When the RST bit is written to 1, the MBISM activates the reset signal on the MIOB. This completely stops the operation of the MIOS1 and resets all the values in the submodules registers that are affected by reset. This bit provides a way of resetting the complete MIOS1 module regardless of the reset state of the CPU. The RST bit is cleared by reset. 0 = Writing a 0 to RST has no effect. 1 = Reset the MIOS1 submodules
4:7	—	Reserved
8	SUPV	Supervisor data space selector. The SUPV bit specifies whether the address space from 0x0000 to 0x07FF in the MIOS1 is accessed at the supervisor privilege level. When SUPV is cleared, these addresses are accessed at the Unrestricted privilege level. The SUPV bit is cleared by reset. 0 = Unrestricted data space. 1 = Supervisor data space.
9:15	—	Reserved. In implementations that use hardware interrupt arbitration, bits 12:15 represent the IARB field.

15.8.2 MBISM Interrupt Registers

Table 15-6 shows the MBISM interrupt registers.

Table 15-6 MBISM Interrupt Registers Address Map

Address	Register
0x30 6C30	MIOS1 Interrupt Level Register 0 (MIOS1LVL0) See **Table 15-7** for bit descriptions.
0x30 6C70	MIOS1 Interrupt Level Register 1 (MIOS1LVL1) See **Table 15-8** for bit descriptions.

15.8.2.1 MIOS1 Interrupt Level Register 0 (MIOS1LVL0)

This register contains the interrupt level that applies to the submodules number 15 to zero.

MIOS1LVL0 — MIOS1 Interrupt Level Register 0 **0x30 6C30**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
RESERVED					LVL			TM		RESERVED					
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 15-7 MIOS1LVL0 Bit Settings

Bit(s)	Name	Description
0:4	—	Reserved
5:7	LVL	Interrupt request level. This field represents one of eight possible levels.
8:9	TM	Time multiplexing. This field determines the multiplexed time slot
10:15	—	Reserved

15.8.2.2 MIOS1 Interrupt Level Register 1 (MIOS1LVL1)

This register contains the interrupt level that applies to the submodules number 31 to 16.

MIOS1LVL1 — MIOS1 Interrupt Level 1 Register **0x30 6C70**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
RESERVED					LVL			TM		RESERVED					
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 15-8 MIOS1LVL1 Bit Settings

Bit(s)	Name	Description
0:4	—	Reserved
5:7	LVL	Interrupt request level. This field represents one of eight possible levels.
8:9	TM	Time multiplexing. This field determines the multiplexed time slot.
10:15	—	Reserved

15.8.3 Interrupt Control Section (ICS)

The interrupt control section delivers the interrupt level to the CPU. The interrupt control section adapts the characteristics of the MIOB request bus to the characteristics of the interrupt structure of the IMB3.

When at least one of the flags is set on an enabled level, the ICS receives a signal from the corresponding IRQ pending register. This signal is the result of a logical “OR” between all the bits of the IRQ pending register.

The signal received from the IRQ pending register is associated with the interrupt level register within the ICS. This level is coded on five bits in this register: three bits represent one of eight levels and the two other represent the four time multiplex slots.

According to this level, the ICS sets the correct IRQ[7:0] lines with the correct ILBS[1:0] time multiplex lines on the peripheral bus. The CPU is then informed as to which of the thirty-two interrupt levels is requested.

Based on the interrupt level requested, the software must determine which submodule requested the interrupt. The software may use a find-first-one type of instruction to determine, in the concerned MIRSM, which of the bits is set. The CPU can then serve the requested interrupt.

15.9 MIOS Counter Prescaler Submodule (MCPSM)

The MIOS counter prescaler submodule (MCPSM) divides the MIOS1 clock (fSYS) to generate the counter clock. It is designed to provide all the submodules with the same division of the main MIOS1 clock (division of fSYS). It uses a 4-bit modulus counter. The clock signal is prescaled by loading the value of the clock prescaler register into the prescaler counter every time it overflows. This allows all prescaling factors between two and 16. Counting is enabled by asserting the PREN bit in the control register. The counter can be stopped at any time by negating this bit, thereby stopping all submodules using the output of the MCPSM (counter clock).

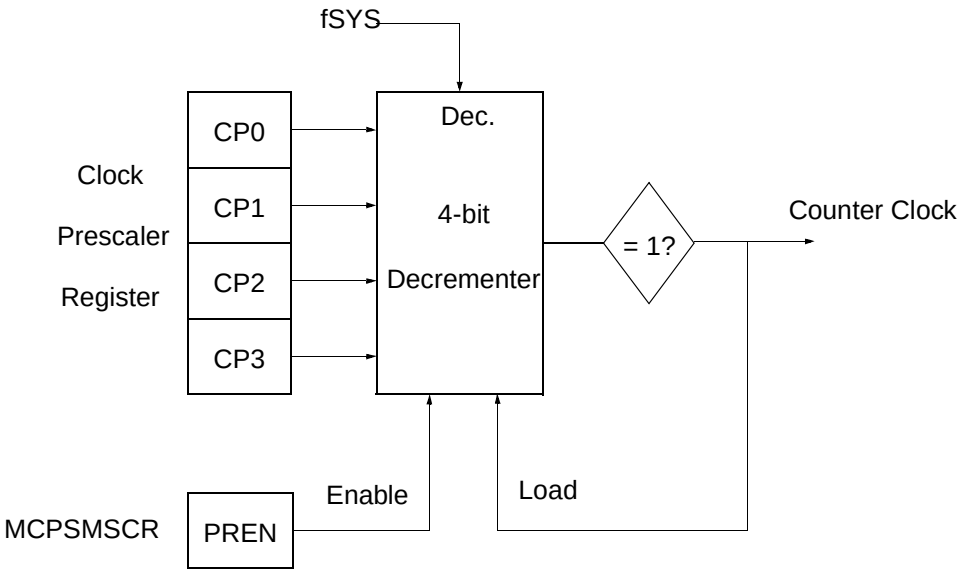

Figure 15-3 MCPSM Block Diagram

15.9.1 MIOS Counter Prescaler Submodule (MCPSM) Registers

Table 15-9 is the address map for the MCPSM submodule.

Table 15-9 MCPSM Address Map

Address	Register
0x30 6810 – 0x30 6814	Reserved
0x30 6816	MCPSM Status/Control Register (MCPSMSCR) See **Table 15-10** for bit descriptions.

15.9.1.1 MCPSM Status/Control Register (MCPSMCSCR)

This register contains status and control information for the MCPSM.

MCPSMSCR — MCPSM Status/Control Register **0x30 6816**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
PREN	FREN	RESERVED										PSL			
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 15-10 MCPSMSCR Bit Settings

Bit(s)	Name	Description
0	PREN	Prescaler enable. This active high read/write control bit enables the MCPSM counter. The PREN bit is cleared by reset. 0 = MCPSM counter disabled. 1 = MCPSM counter enabled.
1	FREN	Freeze enable. This active high read/write control bit when set make possible a freeze of the MCPSM counter if the MIOB freeze line is activated. Note that this line is active when the MIOS1MCR STOP bit is set or when the MIOS1MCR FREN bit and the IMB3 FREEZE line are set. When the MCPSM is frozen, it stops counting. Then when the FREN bit is reset or when the freeze condition on the MIOB is negated, the counter restarts from where it was before being frozen. The FREN bit is cleared by reset. 0 = MCPSM counter not frozen. 1 = Selectively stops MIOS1 operation when the FREEZE signal appears on the IMB3.
2:11	—	Reserved
12:15	PSL	Clock prescaler. This 4-bit read/write data register stores the modulus value for loading into the clock prescaler. The new value is loaded into the counter on the next time the counter equals one or when disabled (PREN bit = 0). Divide ratios are as follows: 0000 = 16 0001 = No counter clock output 0010 = 2 0011 = 3 . . . 1110 = 14 1111 = 15

15.10 MIOS Modulus Counter Submodule (MMCSM)

The MMCSM is a versatile counter submodule capable of performing complex counting and timing functions, including modulus counting, in a wide range of applications. The MMCSM may also be configured as an event counter, allowing the overflow flag to be set after a predefined number of events (internal clocks or external events), or as a time reference for other submodules. Note that the MMCSM can also operate as a free running counter by loading the modulus value of zero.

The main components of the MMCSM are an 8-bit prescaler counter, an 8-bit prescaler register, a 16-bit up-counter register, a 16-bit modulus latch register, counter loading and interrupt flag generation logic.

The contents of the modulus latch register is transferred to the counter under the following three conditions:

1. When an overflow occurs
2. When an appropriate transition occurs on the external load pin
3. When the program writes to the counter register. In this case, the value is first written into the modulus register and immediately transferred to the counter.

Software can also write a value to the modulus register for later loading into the counter with one of the two first criteria.

A software control register selects whether the clock input to the counter is the prescaler output or the corresponding input pin. The polarity of the external input pin is also programmable.

Refer to **Table 15-36** for the MMCSM relative I/O pin implementation.

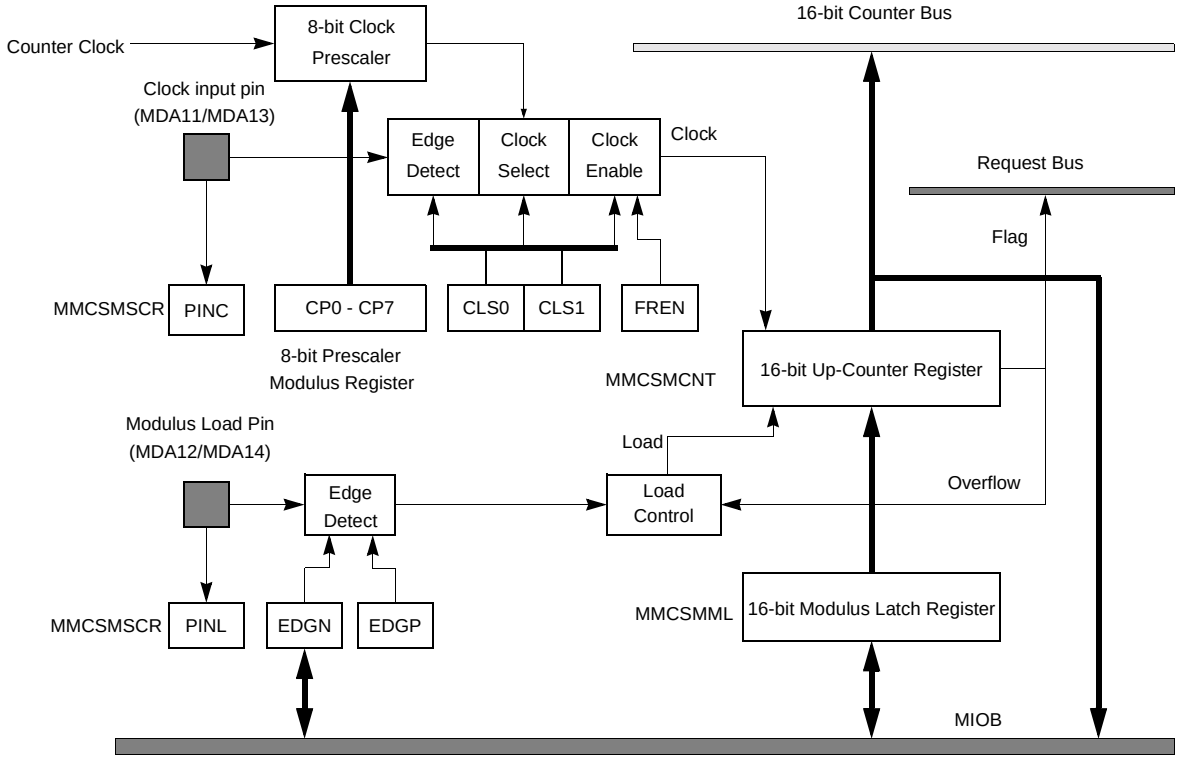

Figure 15-4 MMCSM Block Diagram

15.10.1 MIOS Modulus Counter Submodule (MMCSM) Registers

Each of the two MMCSM submodules in the MPC555 includes the register set shown in **Table 15-11**.

Table 15-11 MMCSM Address Map

Address	Register
MMCSM6	
0x30 6030	MMCSM6 Up-Counter Register (MMCSMCNT) See **Table 15-12** for bit descriptions.
0x30 6032	MMCSM6 Modulus Latch Register (MMCSMML) See **Table 15-13** for bit descriptions.
0x30 6034	MMCSM6 Status/Control Register Duplicated (MMCSMSCRD) See **15.10.1.3 MMCSM Status/Control Register (Duplicated)** for bit descriptions.
0x30 6036	MMCSM6 Status/Control Register (MMCSMSCR)
MMCSM22	
0x30 60B0	MMCSM Up-Counter Register (MMCSMCNT)
0x30 60B2	MMCSM Modulus Latch Register (MMCSMML)
0x30 60B4	MMCSM Status/Control Register Duplicated (MMCSMSCRD)
0x30 60B6	MMCSM Status/Control Register (MMCSMSCR)

15.10.1.1 MMCSM Up-Counter Register (MMCSMCNT)

The MMCSMCNT register contains the 16-bit value of the up counter. Note that writing to MMCSMCNT simultaneously writes to MMCSMML.

MMCSMCNT — MMCSM Up-Counter Register **0x30 6030**
0x30 60B0

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
CNT															
RESET:															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

U = Unaffected by reset

Table 15-12 MMCSMCNT Bit Settings

Bit(s)	Name	Description
0:15	CNT	Counter value. These read/write data bits represent the 16-bit value of the up-counter. CNT contains the value that is driven onto the 16-bit counter bus.

15.10.1.2 MMCSM Modulus Latch Register (MMCSMML)

The MMCSMML is a read/write register containing the 16-bit value of the up-counter.

MMCSMML — MMCSM Modulus Latch Register **0x30 6032**
0x30 60B2

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
ML															
RESET:															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

U = Unaffected by reset

Table 15-13 MMCSMML Bit Settings

Bit(s)	Name	Description
0:15	ML	Modulus latches. These bits are read/write data bits containing the 16-bit modulus value to be loaded into the up-counter. The value loaded in this register must be the two's complement of the desired modulus count. The up-counter increments from this two's complement value up to 0xFFFF to get the correct number of steps before an overflow is generated to reload the modulus value into the up-counter. A value of 0x0000 should be used for a free-running counter.

15.10.1.3 MMCSM Status/Control Register (Duplicated)

The MMCSMSCRD and the MMCSMSCR are the same registers accessed at two different addresses. Reading or writing to one of these two addresses has exactly the same effect.

NOTE

The user should not write directly to the address of the MMCSM-SCRD. This register's address may be reserved for future use and should not be accessed by the software to assure future software compatibility.

MMCSMSCRD — MMCSM Status/Control Register (Duplicated) **0x30 6034**
0x30 60B4

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
PINC	PINL	FREN	EDGN	EDGP	CLS		—	CP							
RESET:															
—	—	0	0	0	0	0	0	U	U	U	U	U	U	U	U

15.10.1.4 MMCSM Status/Control Register (MMCSMSCR)

This register contains both read-only status bits and read/write control bits.

MMCSMSCR — MMCSM Status/Control Register **0x30 6036**
0x30 60B6

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
PINC	PINL	FREN	EDGN	EDGP	CLS		—	CP							
RESET:															
—	—	0	0	0	0	0	0	U	U	U	U	U	U	U	U

Table 15-14 MMCSMSCR Bit Settings

Bit(s)	Name	Description
0	PINC	Clock input pin status. This read-only status bit reflects the logic state of the clock input pin MMCnC (MDA11 or MDA13).
1	PINL	Modulus load input pin status. This read-only status bit reflects the logic state of the modulus load pin MMCnL (MDA12 or MDA14).
2	FREN	Freeze enable. This active high read/write control bit enables the MMCSM to recognize the MIOB freeze signal.
3:4	EDGN, EDGP	Modulus load falling edge/rising edge sensitivity. These active high read/write control bits set falling-edge and rising edge sensitivity, respectively, for the MMCnL pin (MDA12 or MDA14). 00 = Disabled 01 = MMCSMCNT load on rising edges 10 = MMCSMCNT load on falling edges 11 = MMCSMCNT load on rising and falling edges
5:6	CLS	Clock select. These read/write control bits select the clock source for the modulus counter. 00 = Disabled 01 = Falling edge of MMCnC (MDA11 or MDA13) pin 10 = Rising edge of MMCnC (MDA11 or MDA13) pin 11 = MMCSM clock prescaler
7	—	—
8:15	CP	Clock prescaler. This 8-bit read/write data register stores the two's complement of the desired modulus value for loading into the built-in 8-bit clock prescaler. The new value is loaded into the prescaler counter when the next counter overflow occurs or when the CLS bits are set to select the clock prescaler as the clock source. **Table 15-15** gives the clock divide ratio according to the CP values

Table 15-15 MMCSMCR CP and MPWMSMSCR CP Values

Prescaler Value (CP in hex)	MIOS Prescaler Clock Divided by
FF	1
FE	2
FD	3
FC	4
FB	5
FA	6
F9	7
F8	8
.....	.....
02	254 (2^8 -2)
01	255 (2^8 -1)
00	256 (2^8)

15.11 MIOS Double Action Submodule (MDASM)

The MIOS double action submodule (MDASM) provides two consecutive 16-bit input captures or two consecutive 16-bit output compare functions that can occur automatically without software intervention. The input edge detector is programmable to trigger the capture function to occur on the desired edge. The output flip-flop is set by one of

the output compares and is reset by the other one. In all modes except disable mode, an optional interrupt is available to the software. Software selection is provided to select which of the incoming 16-bit counter buses is used for the input capture or the output compare.

The MDASM has six different software selectable modes:

- Disable mode
- Pulse width measurement
- Period measurement
- Input capture mode
- Single pulse generation
- Continuous pulse generation

The MDASM has three data registers that are accessible to the software from the various modes. For some of the modes, two of the registers are cascaded together to provide double buffering. The value in one register is transferred to the other register automatically at the correct time so that the minimum pulse (measurement or generation) is just one 16-bit counter bus count.

Refer to **Table 15-36** for the MDASM relative I/O pin implementation.

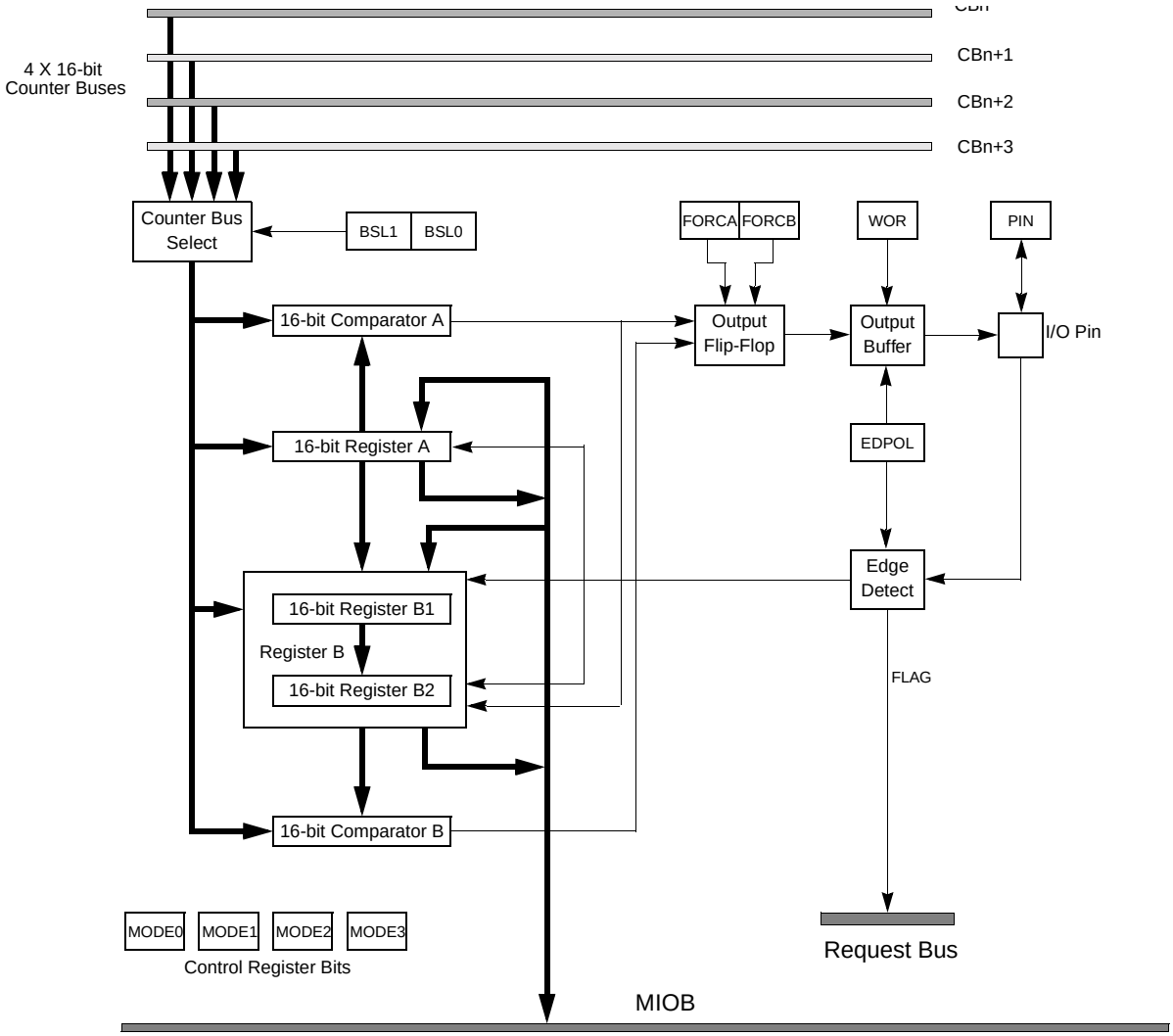

Figure 15-5 MDASM Block Diagram

15.11.1 MIOS Double Action Submodule (MDASM) Registers

One set of registers is associated with each MDASM submodule. The base address of the particular submodule is shown in the table below.

Table 15-16 MDASM Address Map

Address	Register
MDASM11	
0x30 6058	MDASM11 Data A Register (MDASMAR) See **15.11.1.1 MDASM Data A Register** for bit descriptions.
0x30 605A	MDASM11 Data B Register (MDASMBR) See **15.11.1.2 MDASM Data B Register (MDASMBR)** for bit descriptions.
0x30 605C	MDASM11 Status/Control Register Duplicated (MDASMSCRD) See **15.11.1.3 MDASM Status/Control Register (Duplicated)** for bit descriptions.
0x30 605E	MDASM11 Status/Control Register (MDASMSCR) See **Table 15-17** for bit descriptions.
MDASM12	
0x30 6060	MDASM12 Data A Register (MDASMAR)
0x30 6062	MDASM12 Data B Register (MDASMBR)
0x30 6064	MDASM12 Status/Control Register Duplicated (MDASMSCRD)
0x30 6066	MDASM12 Status/Control Register (MDASMSCR)
MDASM13	
0x30 6068	MDASM13 Data A Register (MDASMAR)
0x30 606A	MDASM13 Data B Register (MDASMBR)
0x30 606C	MDASM13 Status/Control Register Duplicated (MDASMSCRD)
0x30 606E	MDASM13 Status/Control Register (MDASMSCR)
MDASM14	
0x30 6070	MDASM14 Data A Register (MDASMAR)
0x30 6072	MDASM14 Data B Register (MDASMBR)
0x30 6074	MDASM14 Status/Control Register Duplicated (MDASMSCRD)
0x30 6076	MDASM14 Status/Control Register (MDASMSCR)
MDASM15	
0x30 6078	MDASM15 Data A Register (MDASMAR)
0x30 607A	MDASM15 Data B Register (MDASMBR)
0x30 607C	MDASM15 Status/Control Register Duplicated (MDASMSCRD)
0x30 607E	MDASM15 Status/Control Register (MDASMSCR)
MDASM27	
0x30 60D8	MDASM27 Data A Register (MDASMAR)
0x30 60DA	MDASM27 Data B Register (MDASMBR)
0x30 60DC	MDASM27 Status/Control Register Duplicated (MDASMSCRD)
0x30 60DE	MDASM27 Status/Control Register (MDASMSCR)
MDASM28	
0x30 60E0	MDASM28 Data A Register (MDASMAR)
0x30 60E2	MDASM28 Data B Register (MDASMBR)
0x30 60E4	MDASM28 Status/Control Register Duplicated (MDASMSCRD)
0x30 60E6	MDASM28 Status/Control Register (MDASMSCR)
MDASM29	
0x30 60E8	MDASM29 Data A Register (MDASMAR)

Table 15-16 MDASM Address Map (Continued)

Address	Register
0x30 60EA	MDASM29 Data B Register (MDASMBR)
0x30 60EC	MDASM29 Status/Control Register Duplicated (MDASMSCRD)
0x30 60EE	MDASM29 Status/Control Register (MDASMSCR)
MDASM30	
0x30 60F0	MDASM30 Data A Register (MDASMAR)
0x30 60F2	MDASM30 Data B Register (MDASMBR)
0x30 60F4	MDASM30 Status/Control Register Duplicated (MDASMSCRD)
0x30 60F6	MDASM30 Status/Control Register (MDASMSCR)
MDASM31	
0x30 60F8	MDASM31 Data A Register (MDASMAR)
0x30 60FA	MDASM31 Data B Register (MDASMBR)
0x30 60FC	MDASM31 Status/Control Register Duplicated (MDASMSCRD)
0x30 60FE	MDASM31 Status/Control Register (MDASMSCR)

15.11.1.1 MDASM Data A Register

MDASMAR is the data register associated with channel A. Its use varies with the mode of operation:

- In the DIS mode, MDASMAR can be accessed to prepare a value for a subsequent mode selection
- In the IPWM mode, MDASMAR contains the captured value corresponding to the trailing edge of the measured pulse
- In the IPM and IC modes, MDASMAR contains the captured value corresponding to the most recently detected dedicated edge (rising or falling edge)
- In the OCB and OCAB modes, MDASMAR is loaded with the value corresponding to the leading edge of the pulse to be generated. Writing to MDASMAR in the OCB and OCAB modes also enables the corresponding channel A comparator until the next successful comparison.
- In the OPWM mode, MDASMAR is loaded with the value corresponding to the leading edge of the PWM pulse to be generated

MDASMAR — MDASM Data A Register **0x30 6058***

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
AR															
RESET:															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

* Refer to **Table 15-16** for a complete list of all the base addresses for the MDASM registers.

15.11.1.2 MDASM Data B Register (MDASMBR)

MDASMBR is the data register associated with channel B. Its use varies with the mode of operation. Depending on the mode selected, software access is to register B1 or register B2.

- In the DIS mode, MDASMBR can be accessed to prepare a value for a subsequent mode selection. In this mode, register B1 is accessed in order to prepare a value for the OPWM mode. Unused register B2 is hidden and cannot be read, but is written with the same value when register B1 is written.
- In the IPWM mode, MDASMBR contains the captured value corresponding to the leading edge of the measured pulse. In this mode, register B2 is accessed; buffer register B1 is hidden and cannot be accessed.
- In the IPM and IC modes, MDASMBR contains the captured value corresponding to the most recently detected period edge (rising or falling edge). In this mode, register B2 is accessed; buffer register B1 is hidden and cannot be accessed.
- In the OCB and OCAB modes, MDASMBR is loaded with the value corresponding to the trailing edge of the pulse to be generated. Writing to MDASMBR in the OCB and OCAB modes also enables the corresponding channel B comparator until the next successful comparison. In this mode, register B2 is accessed; buffer register B1 is hidden and cannot be accessed.
- In the OPWM mode, MDASMBR is loaded with the value corresponding to the trailing edge of the PWM pulse to be generated. In this mode, register B1 is accessed; buffer register B2 is hidden and cannot be accessed.

MDASMBR — MDASM Data B Register **0x30 605A***

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
BR															
RESET:															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

* Refer to **Table 15-16** for a complete list of all the base addresses for the MDASM registers.

15.11.1.3 MDASM Status/Control Register (Duplicated)

The MDASMSCRD and the MDASMSCR are the same registers accessed at two different addresses. Reading or writing to either of these two addresses has exactly the same effect.

NOTE

The user should not write directly to the address of the MDASMSCRD. This register's address may be reserved for future use and should not be accessed by the software to assure future software compatibility.

MDASMSCRD — MDASM Status/Control Register (Duplicated) **0x30 605C***

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
PIN	WOR	FREN	0	ED-POL	FORCA	FORCB	RESERVED		BSL		0	MOD			
RESET:															
—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

* Refer to **Table 15-16** for a complete list of all the base addresses for the MDASM registers.

15.11.1.4 MDASM Status/Control Register

The status/control register contains a read-only bit reflecting the status of the MDASM pin as well as read/write bits related to its control and configuration.

MDASMSCR — MDASM Status/Control Register **0x30 605E***

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
PIN	WOR	FREN	0	ED-POL	FORCA	FORCB	RESERVED		BSL		0	MOD			
RESET:															
—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

* Refer to **Table 15-16** for a complete list of all the base addresses for the MDASM registers.

Table 15-17 MDASMSCR Bit Settings

Bit(s)	Name	Description
0	PIN	Pin input status. The pin input status bit reflects the status of the corresponding pin.
1	WOR	Wired-OR. In the DIS, IPWM, IPM and IC modes, the WOR bit is not used; reading this bit returns the value that was previously written. In the OCB, OCAB and OPWM modes, the WOR bit selects whether the output buffer is configured for open-drain or totem-pole operation. 0 = Output buffer is totem-pole. 1 = Output buffer is open-drain.
2	FREN	Freeze enable. This active high read/write control bit enables the MDASM to recognize the MIOB freeze signal. 0 = The MDASM is not frozen even if the MIOB freeze line is active. 1 = The MDASM is frozen if the MIOB freeze line is active.
3	—	0
4	EDPOL	Polarity. In the DIS mode, this bit is not used; reading it returns the last value written. In the IPWM mode, this bit is used to select the capture edge sensitivity of channels A and B. 0 = Channel A captures on a rising edge. Channel B captures on a falling edge. 1 = Channel A captures on a falling edge. Channel B captures on a rising edge. In the IPM and IC modes, the EDPOL bit is used to select the input capture edge sensitivity of channel A. 0 = Channel A captures on a rising edge. 1 = Channel A captures on a falling edge. In the OCB, OCAB and OPWM modes, the EDPOL bit is used to select the voltage level on the output pin. 0 = The output flip-flop logic level appears on the output pin: a compare on channel A sets the output pin, a compare on channel B resets the output pin. 1 = The complement of the output flip-flop logic level appears on the output pin: a compare on channel A resets the output pin; a compare on channel B sets the output pin.
5	FORCA	Force A. In the OCB, OCAB and OPWM modes, the FORCA bit allows the software to force the output flip-flop to behave as if a successful comparison had occurred on channel A (except that the FLAG line is not activated). Writing a one to FORCA sets the output flip-flop; writing a zero to it has no effect. In the DIS, IPWM, IPM and IC modes, the FORCA bit is not used and writing to it has no effect. FORCA is cleared by reset and is always read as zero. Writing a one to both FORCA and FORCB simultaneously resets the output flip-flop.
6	FORCB	Force B. In the OCB, OCAB and OPWM modes, the FORCB bit allows the software to force the output flip-flop to behave as if a successful comparison had occurred on channel B (except that the FLAG line is not activated). Writing a one to FORCB resets the output flip-flop; writing a zero to it has no effect. In the DIS, IPWM, IPM and IC modes, the FORCB bit is not used and writing to it has no effect. FORCB is cleared by reset and is always read as zero. Writing a one to both FORCA and FORCB simultaneously resets the output flip-flop.
7:8	—	Reserved
9:10	BSL	Bus select.These bits are used to select which of the four possible 16-bit counter bus passing nearby is used by the MDASM. Refer to **Table 15-36** to see how the MDASM is connected to the 16-bit counter buses in the MIOS1.
11	—	0
12:15	MOD	Mode select. These four mode select bits select the mode of operation of the MDASM. To avoid spurious interrupts, it is recommended that MDASM interrupts are disabled before changing the operating mode. It is also imperative to go through the disable mode before changing the operating mode. See **Table 15-18** for details.

Table 15-18 MDASM Mode Selects

MDASM Control Register Bits	Bits of Resolution	Counter Bus Bits Ignored	MDASM Mode of Operation
MOD			
0000	—	—	DIS – Disabled
0001	16	—	IPWM – Input pulse width measurement
0010	16	—	IPM – Input period measurement
0011	16	—	IC – Input capture
0100	16	—	OCB – Output compare, flag on B compare
0101	16	—	OCAB – Output compare, flag on A and B compare
0110	—	—	Reserved
0111	—	—	Reserved
1000	16	—	OPWM – Output pulse width modulation
1001	15	0	OPWM – Output pulse width modulation
1010	14	0,1	OPWM – Output pulse width modulation
1011	13	0-2	OPWM – Output pulse width modulation
1100	12	0-3	OPWM – Output pulse width modulation
1101	11	0-4	OPWM – Output pulse width modulation
1110	9	0-6	OPWM – Output pulse width modulation
1111	7	0-8	OPWM – Output pulse width modulation

15.12 MIOS Pulse Width Modulation Submodule (MPWMSM)

The purpose of the MIOS pulse width modulation submodule (MPWMSM) is to create a variable pulse width output signal at a wide range of frequencies, independent of other MIOS1 output signals. The MPWMSM includes its own 8-bit prescaler and counter and, thus, does not use the MIOS1 16-bit counter buses.

The MPWMSM pulse width can vary from 0.0% to 100.0%, with up to 16 bits of resolution. The finest output resolution is the MCU system clock time divided by two (for a fSYS of 40.0 MHz, the finest output pulse width resolution is 50 ns). With the full sixteen bits of resolution and the overall prescaler divide ratio varying from divide-by-2 to divide-by-4096, the period of the PWM output can range from 3.28 ms to 6.7 s (assuming a fSYS of 40 MHz). By reducing the counting value, the output signal period can be reduced. The period can be as fast as 205 µs (4.882 kHz) with twelve bits of resolution, as fast as 12.8 µs (78.125 kHz) with eight bits of resolution and as fast as 3.2 µs (312.500 kHz) with six bits of resolution (still assuming a fSYS of 40 MHz and a first stage prescaler divide-by-2 clock selection).

Refer to **Table 15-36** for the MPWMSM relative I/O pin implementation.

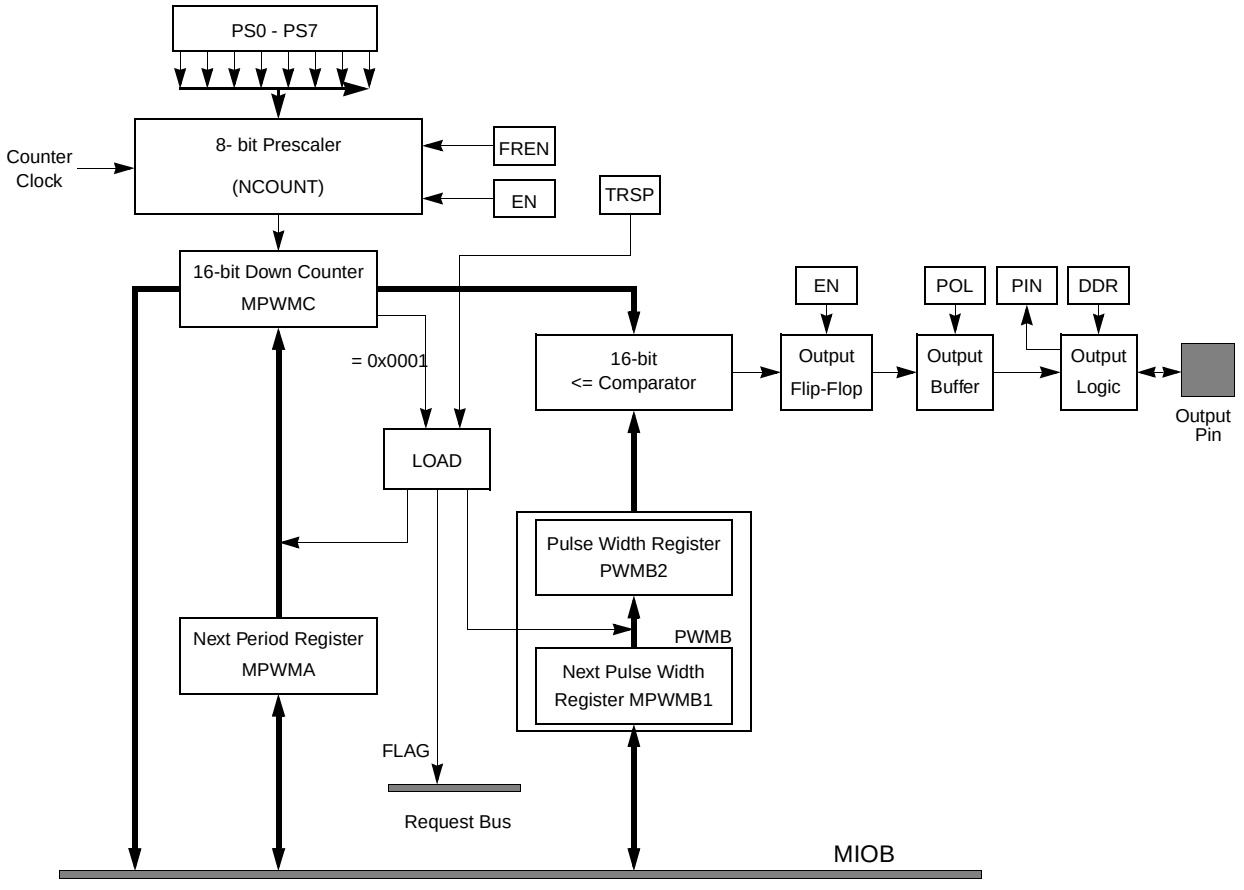

Figure 15-6 MPWMSM Block Diagram

15.12.1 MIOS Pulse Width Modulation Submodule (MPWMSM) Registers

One set of registers is associated with each MPWMSM submodule. The base address is given in the table below.

Table 15-19 MPWMSM Address Map

Address	Register
MPWMSM0	
0x30 6000	MPWMSM0 Period Register (MPWMSMPERR) See **Table 15-20** for bit descriptions.
0x30 6002	MPWMSM0 Pulse Register (MPWMSMPULR) See **Table 15-21** for bit descriptions.
0x30 6004	MPWMSM0 Count Register (MPWMSMCNTR) See **Table 15-22** for bit descriptions.
0x30 6006	MPWMSM0 Status/Control Register (MPWMSMSCR) See **Table 15-23** for bit descriptions.
MPWMSM1	
0x30 6008	MPWMSM1 Period Register (MPWMSMPERR)
0x30 600A	MPWMSM1 Pulse Register (MPWMSMPULR)
0x30 600C	MPWMSM1 Count Register (MPWMSMCNTR)
0x30 600E	MPWMSM1 Status/Control Register (MPWMSMSCR)
MPWMSM2	
0x30 6010	MPWMSM2 Period Register (MPWMSMPERR)
0x30 6012	MPWMSM2 Pulse Register (MPWMSMPULR)
0x30 6014	MPWMSM2 Count Register (MPWMSMCNTR)
0x30 6016	MPWMSM2 Status/Control Register (MPWMSMSCR)
MPWMSM3	
0x30 6018	MPWMSM3 Period Register (MPWMSMPERR)
0x30 601A	MPWMSM3 Pulse Register (MPWMSMPULR)
0x30 601C	MPWMSM3 Count Register (MPWMSMCNTR)
0x30 601E	MPWMSM3 Status/Control Register (MPWMSMSCR)
MPWMSM16	
0x30 6080	MPWMSM16 Period Register (MPWMSMPERR)
0x30 6082	MPWMSM16 Pulse Register (MPWMSMPULR)
0x30 6084	MPWMSM16 Count Register (MPWMSMCNTR)
0x30 6086	MPWMSM16 Status/Control Register (MPWMSMSCR)
MPWMSM17	
0x30 6088	MPWMSM17 Period Register (MPWMSMPERR)
0x30 608A	MPWMSM17 Pulse Register (MPWMSMPULR)
0x30 608C	MPWMSM17 Count Register (MPWMSMCNTR)
0x30 608E	MPWMSM17 Status/Control Register (MPWMSMSCR)
MPWMSM18	
0x30 6090	MPWMSM18 Period Register (MPWMSMPERR)
0x30 6092	MPWMSM18 Pulse Register (MPWMSMPULR)
0x30 6094	MPWMSM18 Count Register (MPWMSMCNTR)
0x30 6096	MPWMSM18 Status/Control Register (MPWMSMSCR)

Table 15-19 MPWMSM Address Map (Continued)

Address	Register
MPWMSM19	
0x30 6098	MPWMSM19 Period Register (MPWMSMPERR)
0x30 609A	MPWMSM19 Pulse Register (MPWMSMPULR)
0x30 609C	MPWMSM19 Count Register (MPWMSMCNTR)
0x30 609E	MPWMSM19 Status/Control Register (MPWMSMSCR)

15.12.1.1 MPWMSM Period Register (MPWMSMPERR)

The period register contains the binary value corresponding to the period to be generated.

MPWMSMPERR — MPWMSM Period Register **0x30 6000***

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
PER															
RESET:															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

* Refer to **Table 15-19** for a complete list of all the base addresses for the MPWMSM registers.

Table 15-20 MPWMSMPERR Bit Settings

Bit(s)	Name	Description
0:15	PER	Period. These bits contain the binary value corresponding to the period to be generated.

15.12.1.2 MPWMSM Pulse Width Register (MPWMSMPULR)

This register contains the binary value of the pulse width to be generated.

MPWMSMPULR — MPWMSM Pulse Width Register **0x30 6002***

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
PUL															
RESET:															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

* Refer to **Table 15-19** for a complete list of all the base addresses for the MPWMSM registers.

Table 15-21 MPWMSMPULR Bit Settings

Bit(s)	Name	Description
0:15	PUL	Pulse width. These bits contain the binary value of the pulse width to be generated.

15.12.1.3 MPWMSM Counter Register (MPWMSMCNTR)

This register reflects the actual value of the MPWMSM counter.

MPWMSMCNTR — MPWMSM Counter Register **0x30 6004***

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
CNT															
RESET:															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

* Refer to **Table 15-19** for a complete list of all the base addresses for the MPWMSM registers. A write to the MPWMSMCNTR register also writes the same value to MPWMSMPERR.

Table 15-22 MPWMSMCNTR Bit Settings

Bit(s)	Name	Description
0:15	CNT	Counter. These bits reflect the actual value of the MPWMSM counter.

15.12.1.4 MPWMSM Status/Control Register(MPWMSMCR)

This register contains read-only status bits and read/write control bits.

MPWMSMSCR — MPWMSM Status/Control Register **0x30 6006***

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
PIN	DDR	FREN	TRSP	POL	EN	RESERVED		CP							
RESET:															
—	0	0	0	0	0	0	0	U	U	U	U	U	U	U	U

* Refer to **Table 15-19** for a complete list of all the base addresses for the MPWMSM registers.

Table 15-23 MPWMSMSCR Bit Settings

Bit(s)	Name	Description
0	PIN	Pin input status. The PIN bit reflects the state present on the MPWMSM pin. The software can thus monitor the signal on the pin. The PIN bit is a read-only bit. Writing to the PIN bit has no effect.
1	DDR	Data direction register. The DDR bit indicates the direction for the pin when the PWM function is not used (disable mode). Note that when the PWM function is used, the DDR bit has no effect. **Table 15-24** lists the different uses for the polarity (POL) bit, the enable (EN) bit and the data direction register (DDR) bit. 0 = Pin is an input. 1 = Pin is an output.
2	FREN	Freeze enable. This active high read/write control bit enables the MPWMSM to recognize the freeze signal on the MIOB. 0 = MPWMSM not frozen even if the MIOB freeze line is active. 1 = MPWMSM frozen if the MIOB freeze line is active.
3	TRSP	Transparent mode. The TRSP bit indicates that the MPWMSM double buffers are transparent: when the software writes to either the MPWMA or MPWMB1 register the value written is immediately transferred to respectively the counter or register MPWMB2. 0 = Transparent mode de-activated. 1 = Transparent mode activated.
4	POL	Output polarity control. The POL bit works in conjunction with the EN bit and controls whether the MPWMSM drives the pin with the true or the inverted value of the output flip-flop **Table 15-24** lists the different uses for the polarity (POL) bit, the enable (EN) bit and the data direction register (DDR) bit.
5	EN	Enable PWM signal generation. The EN bit defines whether the MPWMSM generates a PWM signal or is used as an I/O channel: **Table 15-24** lists the different uses for the polarity (POL) bit, the enable (EN) bit and the data direction register (DDR) bit. 0 = PWM generation disabled (pin can be used as I/O). 1 = PWM generation enabled (pin is output only).
6:7	—	Reserved
8:15	CP	Clock Prescaler. This 8-bit read/write register stores the two's complement of the desired modulus value for loading into the built-in 8-bit clock prescaler. The value loaded defines the divide ratio for the signal that clocks the MPWMSM period counter. **Table 15-15** gives the clock divide ratio according to the CP values.

Table 15-24 PWMSM Output Pin Polarity Selection

Control Bits			Pin Direction (I/O)	Pin State	Periodic Edge	Variable Edge	Optional Interrupt On
POL	EN	DDR					
0	0	0	I	Low	—	—	—
0	0	1	O	Always Low	—	—	—
0	1	—	O	High Pulse	Rising Edge	Falling Edge	Rising Edge
1	0	0	I	High	—	—	—
1	0	1	O	Always High	—	—	—
1	1	—	O	Low Pulse	Falling Edge	Rising Edge	Falling Edge

15.13 MIOS 16-bit Parallel Port I/O Submodule (MPIOSM)

An MIOS 16-bit parallel port I/O submodule (MPIOSM) can handle up to 16 input/output pins. Its control register is composed of two 16-bit registers: the data register (DR) and the data direction register (DDR). Each pin of the MPIOSM may be programmed as an input or an output under software control. The direction of a pin is determined by the state of the corresponding bit in the DDR.

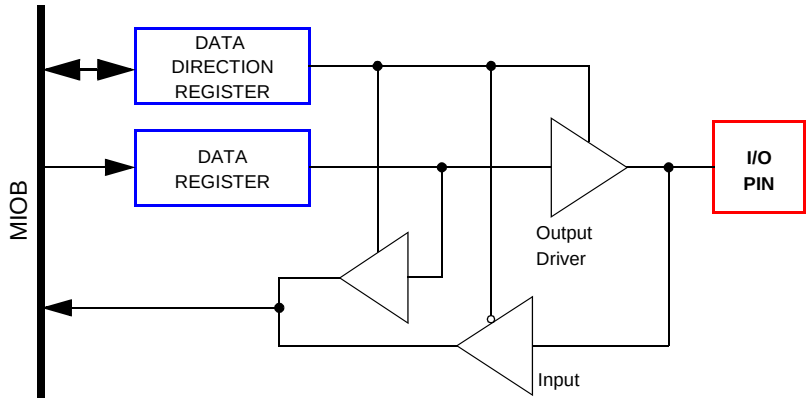

Figure 15-7 MPIOSM One-Bit Block Diagram

Refer to **Table 15-36** for the MPIOSM relative I/O pin implementation.

15.13.1 MIOS 16-bit Parallel Port I/O Submodule (MPIOSM) Registers

One set of registers is associated with the MPIOSM submodule. The base addresses of the submodules are given in the table below.

Table 15-25 MPIOSM Address Map

Address	Register
0x30 6100	MPIOSM Data Register (MPIOSMDR) See **Table 15-26** for bit descriptions.
0x30 6102	MPIOSM Data Direction Register (MPIOSMDDR) See **Table 15-27** for bit descriptions.
0x30 6104	Reserved
0x30 6106	Reserved

15.13.1.1 MPIOSM Data Register (MPIOSMDR)

This read/write register defines the value to be driven to the pad in output mode, for each implemented I/O pin of the MPIOSM.

MPIOSMDR — MPIOSM Data Register **0x30 6100**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RESET:															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

Table 15-26 MPIOSMDR Bit Settings

Bit(s)	Name	Description
0:15	D[15:0]	Data BITS. These bits are read/write data bits that define the value to be driven to the pad in output mode for each implemented I/O pin of the MPIOSM. While in output mode, a read returns the value of the pad. Note that, when little-endian bit ordering is used, bit 0 corresponds to D15 and bit 15 corresponds to D0.

NOTE

D[0:4] controls the signals MPIO32B[0:4]. These functions are shared on the MPC555 pins VF[0:2]/MPIO32B[0:2] VFLS[0:1]/ MPIO32B[3:4] and can be configured as the alternate function (VF[0:2] and VFLS[0:1]). See **15.8.1.1 MIOS1 Test and Pin Control Register**.

15.13.1.2 MPIOSM Data Direction Register (MPIOSMDDR)

This read/write register defines the data direction for each implemented I/O pin of the MPIOSM.

MPIOSMDDR — MPIOSM Data Direction Register **0x30 6102**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
DDR15	DDR14	DDR13	DDR12	DDR11	DDR10	DDR9	DDR8	DDR7	DDR6	DDR5	DDR4	DDR3	DDR2	DDR1	DDR0
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 15-27 MPIOSMDDR Bit Settings

Bit(s)	Name	Description
0:15	DDR[15:0]	Data direction. These bits are read/write data bits that define the data direction status for each implemented I/O pin of the MPIOSM. Note that, when little-endian bit ordering is used, bit 0 corresponds to D15 and bit 15 corresponds to D0. 0 = Corresponding pin is input. 1 = Corresponding pin is output.

15.14 MIOS1 Interrupts

The MIOS1 and its submodules are capable of generating interrupts to be transmitted to the CPU via the IMB3. Inside the MIOS1, all the information required for requesting and servicing the interrupts are treated in two different blocks:

- The interrupt control section (ICS)
- The MIOS interrupt request submodules (MIRSM).

The MIOS interrupt request submodule gathers service request flags from each group of up to 16 submodules and transfers those requests to the MIOS1 interrupt control section (ICS). **Figure 15-8** shows a block diagram of the interrupt architecture.

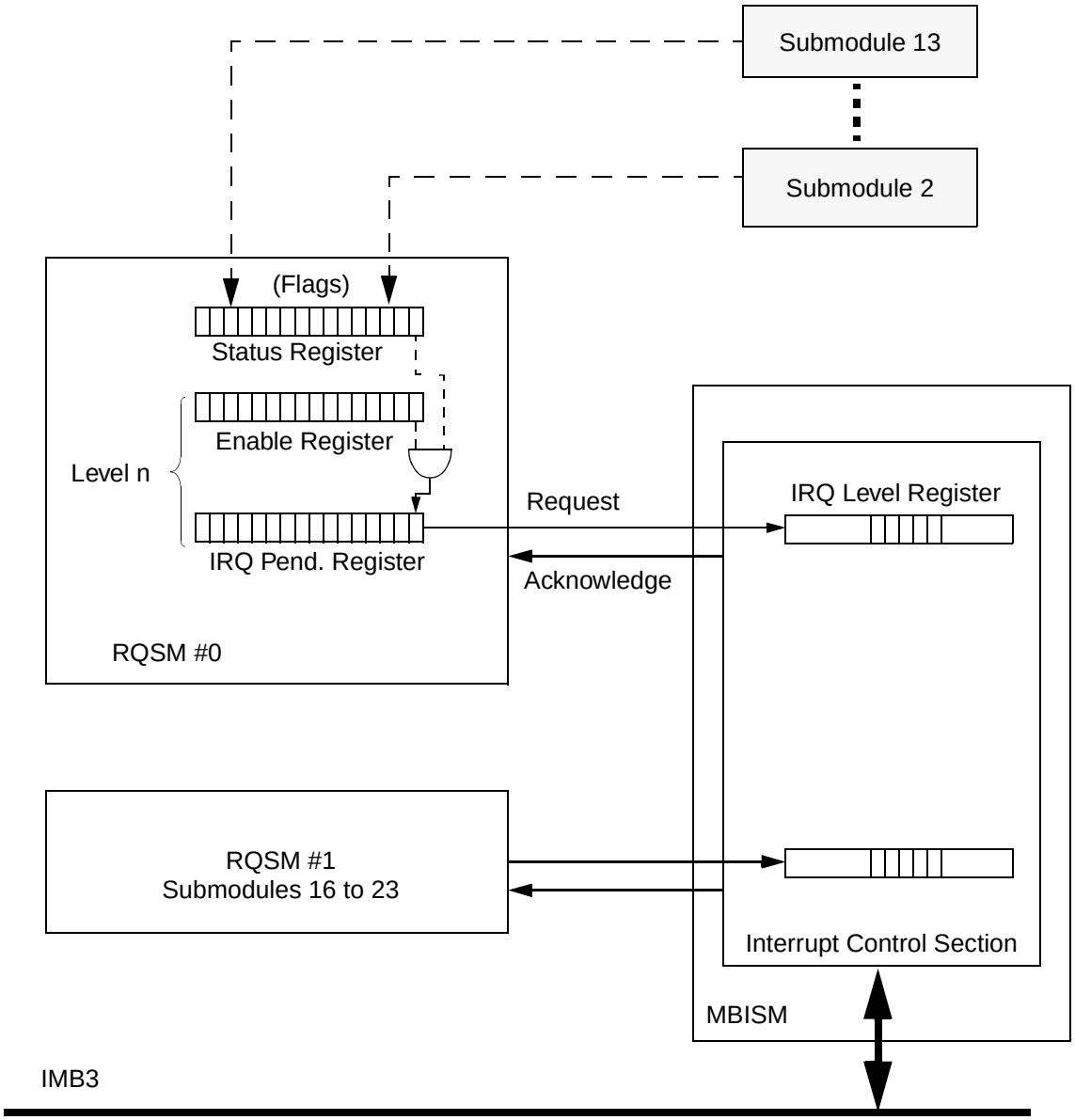

Figure 15-8 MIOS Interrupt Structure

15.14.1 MIOS Interrupt Request Submodule (MIRSM)

Each submodule that is capable of generating an interrupt can assert a flag line when an event occurs. In the MIOS1 configuration, there are eighteen flag lines and two MIRSMs are needed.

Within the MIOS1, each MIRSM includes:

- One 16-bit status register (for the flags)
- One 16-bit enable register
- One 16-bit IRQ pending register

One bit position in each of the above registers is associated with one submodule. Note that if a submodule in a group of 16 cannot generate interrupts, then its corresponding flag bit in the status register is inactive and reads as zero.

When an event occurs in a submodule that activates a flag line, the corresponding flag bit in the status register is set. The status register is read/write, but a flag bit can be reset only if it has previously been read as a one. Writing a one to a flag bit has no effect. When the software intends to clear only one flag bit within a status register, the software must write an 16-bit value of all ones except for a zero in the bit position to be cleared.

The enable register is initialized by the software to indicate whether each interrupt request is enabled for the level defined in the ICS.

Each bit in the IRQ pending register is the result of a logical “AND” between the corresponding bits in the status and in the enable registers. If a flag bit is set and the level enable bit is also set, then the IRQ pending bit is set and the information is transferred to the interrupt control section that is in charge of sending the corresponding level to the CPU. The IRQ pending register is read only.

NOTE

When the enable bit is not set for a particular submodule, the corresponding status register bit is still set when the corresponding flag is set. This allows the traditional software approach of polling the flag bits to see which ones are set. The status register makes flag polling easy, since up to sixteen flag bits are contained in one register.

The submodule number of an interrupting source defines the corresponding MIRSM number and the bit position in the status registers. To find the MIRSM number and bit position of an interrupting source, divide the interrupting submodule number by 16. The integer result of the division gives the MIRSM number. The remainder of the division gives the bit position.

Refer to **15.14.2 MIOS Interrupt Request Submodule 0 (MIRSM0) Registers** and to **15.14.3 MIOS Interrupt Request Submodule 1 (MIRSM1) Registers** for details about the registers in the MIRSM.

15.14.2 MIOS Interrupt Request Submodule 0 (MIRSM0) Registers

Table 15-28 shows the registers associated with the MIRSM0 submodule.

Table 15-28 MIRSM0 Address Map

Address	Register
0x30 6C00	MIRSM0 Interrupt Status Register (MIOS1SR0) See **Table 15-29** for bit descriptions.
0x30 6C02	Reserved
0x30 6C04	MIRSM0 Interrupt Enable Register (MIOS1ER0) See **Table 15-30** for bit descriptions.
0x30 6C06	MIRSM0 Request Pending Register (MIOS1RPR0) See **Table 15-31** for bit descriptions.

15.14.2.1 MIRSM0 Interrupt Status Register (MIOS1SR0)

This register contains flag bits that are set when the associated submodule generates an interrupt. Each bit corresponds to a submodule.

When an event occurs in a submodule that activates a flag line, the corresponding flag bit in the status register is set. The status register is read/write, but a flag bit can be reset only if it has previously been read as a one. Writing a one to a flag bit has no effect. When the software intends to clear only one flag bit within a status register, the software must write an 16-bit value of all ones except for a zero in the bit position to be cleared.

MIOS1SR0 — RQSM0 Interrupt Status Register **0x30 6C00**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
FLG15	FLG14	FLG13	FLG12	FLG11	RESERVED				FLG6	RESERVED		FLG3	FLG2	FLG1	FLG0
RESET:															
U	U	U	U	U	0	0	0	0	U	U	U	U	U	U	U

Table 15-29 MIOS1SR0 Bit Settings

Bit(s)	Name	Description
0	FLG15	MDASM15 flag bit
1	FLG14	MDASM14 flag bit
2	FLG13	MDASM13 flag bit
3	FLG12	MDASM12 flag bit
4	FLG11	MDASM11 flag bit
5:8	—	Reserved
9	FLG6	MMCSM6 flag bit
10:11	—	Reserved
12	FLG3	MPWMSM3 flag bit
13	FLG2	MPWMSM2 flag bit
14	FLG1	MPWMSM1 flag bit
15	FLG0	MPWMSM0 flag bit

15.14.2.2 MIRSM0 Interrupt Enable Register (MIOS1ER0)

This read/write register contains interrupt enable bits. Each bit corresponds to a submodule.

MIOS1ER0 — MIRSM0 Interrupt Enable Register **0x30 6C04**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
EN15	EN14	EN13	EN12	EN11	RESERVED				EN6	RESERVED		EN3	EN2	EN1	EN0
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 15-30 MIOS1ER0 Bit Settings

Bit(s)	Name	Description
0	EN15	MDASM15 interrupt enable bit
1	EN14	MDASM14 interrupt enable bit
2	EN13	MDASM13 interrupt enable bit
3	EN12	MDASM12 interrupt enable bit
4	EN11	MDASM11 interrupt enable bit
5:8	—	Reserved
9	EN6	MMCSM6 interrupt enable bit
10:11	—	Reserved
12	EN3	MPWMSM3 interrupt enable bit
13	EN2	MPWMSM2 interrupt enable bit
14	EN1	MPWMSM1 interrupt enable bit
15	EN0	MPWMSM0 interrupt enable bit

15.14.2.3 MIRSM0 Request Pending Register (MIOS1RPR0)

This read-only register contains interrupt pending bits. Each bit corresponds to a sub-module. A bit that is set indicates that the associated submodule set its flag and that the corresponding enable bit was set.

MIOS1RPR0 — MIRSM0 Request Pending Register **0x30 6C06**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
IRP15	IRP14	IRP13	IRP12	IRP11	RESERVED				IRP6	RESERVED		IRP3	IRP2	IRP1	IRP0
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 15-31 MIOS1RPR0 Bit Settings

Bit(s)	Name	Description
0	IRP15	MDASM15 IRQ pending bit
1	IRP14	MDASM14 IRQ pending bit
2	IRP13	MDASM13 IRQ pending bit
3	IRP12	MDASM12 IRQ pending bit
4	IRP11	MDASM11 IRQ pending bit
5:8	—	Reserved
9	IRP6	MMCSM6 IRQ pending bit
10:11	—	Reserved
12	IRP3	MPWMSM3 IRQ pending bit
13	IRP2	MPWMSM2 IRQ pending bit
14	IRP1	MPWMSM1 IRQ pending bit
15	IRP0	MPWMSM0 IRQ pending bit

15.14.3 MIOS Interrupt Request Submodule 1 (MIRSM1) Registers

Table 15-32 shows the base addresses of the registers associated with the MIRSM1 submodule.

Table 15-32 MIRSM1 Address Map

Address	Register
0x30 6C40	MIRSM1 Interrupt Status Register (MIOS1SR1) See **Table 15-33** for bit descriptions.
0x30 6C42	Reserved
0x30 6C44	MIRSM1 Interrupt Enable Register (MIOS1ER1) See **Table 15-34** for bit descriptions.
0x30 6C46	MIRSM1 Request Pending Register (MIOS1PR1) See **Table 15-35** for bit descriptions.

15.14.3.1 MIRSM1 Interrupt Status Register (MIOS1SR1)

This register contains flag bits that are set when the associated submodule generates an interrupt. Each bit corresponds to a submodule.

MIOS1SR1 — MIRSM1 Interrupt Status Register **0x30 6C40**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
FLG31	FLG30	FLG29	FLG28	FLG27	RESERVED				FLG22	RESERVED		FLG19	FLG18	FLG17	FLG16
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 15-33 MIOS1SR1 Bit Settings

Bit(s)	Name	Description
0	FLG31	MDASM31 flag bit
1	FLG30	MDASM30 flag bit
2	FLG29	MDASM29 flag bit
3	FLG28	MDASM28 flag bit
4	FLG27	MDASM27 flag bit
5:8	—	Reserved
9	FLG22	MMCSM22 flag bit
10:11	—	Reserved
12	FLG19	MPWMSM19 flag bit
13	FLG18	MPWMSM18 flag bit
14	FLG17	MPWMSM17 flag bit
15	FLG16	MPWMSM16 flag bit

15.14.3.2 MIRSM1 Interrupt Enable Register (MIOS1ER1)

This read/write register contains interrupt enable bits. Each bit corresponds to a submodule.

MIOS1ER1 — Interrupt Enable Register **0x30 6C44**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
EN31	EN30	EN129	EN28	EN27	RESERVED				EN22	RESERVED		EN19	EN18	EN17	EN16
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 15-34 MIOS1ER1 Bit Settings

Bit(s)	Name	Description
0	EN31	MDASM31 interrupt enable bit
1	EN30	MDASM30 interrupt enable bit
2	EN29	MDASM29 interrupt enable bit
3	EN28	MDASM28 interrupt enable bit
4	EN27	MDASM27 interrupt enable bit
5:8	—	Reserved
9	EN22	MMCSM22 interrupt enable bit
10:11	—	Reserved
12	EN19	MPWMSM19 interrupt enable bit
13	EN18	MPWMSM18 interrupt enable bit
14	EN17	MPWMSM17 interrupt enable bit
15	EN16	MPWMSM16 interrupt enable bit

15.14.3.3 MIRSM1 Request Pending Register (MIOS1RPR1)

This read-only register contains interrupt pending bits. Each bit corresponds to a submodule. A bit that is set indicates that the associated submodule set its flag and that the corresponding enable bit was set.

MIOS1RPR1 — MIRSM1 Request Pending Register **0x30 6C46**

MSB 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	LSB 15
IRP31	IRP30	IRP29	IRP28	IRP27	RESERVED				IRP22	RESERVED		IRP19	IRP18	IRP17	IRP16
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 15-35 MIOS1RPR1 Bit Settings

Bit(s)	Name	Description
0	IRP31	MDASM31 IRQ pending bit
1	IRP30	MDASM30 IRQ pending bit
2	IRP29	MDASM29 IRQ pending bit
3	IRP28	MDASM28 IRQ pending bit
4	IRP27	MDASM27 IRQ pending bit
5:8	—	Reserved
9	IRP22	MMCSM22 IRQ pending bit
10:11	—	Reserved
12	IRP19	MPWMSM19 IRQ pending bit
13	IRP18	MPWMSM18 IRQ pending bit
14	IRP17	MPWMSM17 IRQ pending bit
15	IRP16	MPWMSM16 IRQ pending bit

15.15 MIOS1 Function Examples

The versatility of the MIOS1 timer architecture is based on multiple counters and capture/compare channel units interconnected on 16-bit counter buses. This section includes some typical application examples to show how the submodules can be interconnected to form timing functions. The diagrams used to illustrate these examples show only the blocks utilized for that function.

To illustrate the timing range of the MIOS1 in different applications, many of the following paragraphs include time intervals quoted in microseconds and seconds. The assumptions used are that fSYS is at 40 MHz with minimum overall prescaling (50 ns cycle) and with the maximum overall prescaling (32 µs cycle). For other fSYS clock cycle rates and prescaler choices, the times mentioned in these paragraphs scale appropriately.

15.15.1 MIOS1 Input Double Edge Pulse Width Measurement

To measure the width of an input pulse, the MIOS double action submodule (MDASM) has two capture registers so that only one interrupt is needed after the second edge. The software can read both edge samples and subtract them to get the pulse width.

The leading edge sample is double latched so that the software has the time of one full period of the input signal to read the samples to be sure that nothing is lost. Depending on the prescaler divide ratio, pulse width from 50 ns to 6.7 s can be measured. Note that a software option is provided to also generate an interrupt after the first edge.

In the example shown in **Figure 15-9**, a counter submodule is used as the time-base for a MDASM configured in the input pulse width measurement mode. When the leading edge (programmed for being either rising or falling) of the input signal occurs, the state of the 16-bit counter bus is saved in register B1. When the trailing edge occurs, the 16-bit counter bus is latched into register A and the content of register B1 is transferred to register B2. This operation leaves register B1 free for the next leading edge to occur on the next clock cycle. When enabled, an interrupt is provided after the trailing edge, to notify the software that pulse width measurement data is available for a new pulse. After the trailing edge, the software has one cycle time of the input signal to obtain the values for each edge. When software attention is not needed for every pulse, the interrupt can be disabled. The software can read registers A and B2 coherently (using a 32-bit read instruction) at any time, to get the latest edge measurements. The software work is less than half that needed with a timer that requires the software to read one edge and save the value and then wait for the second edge.

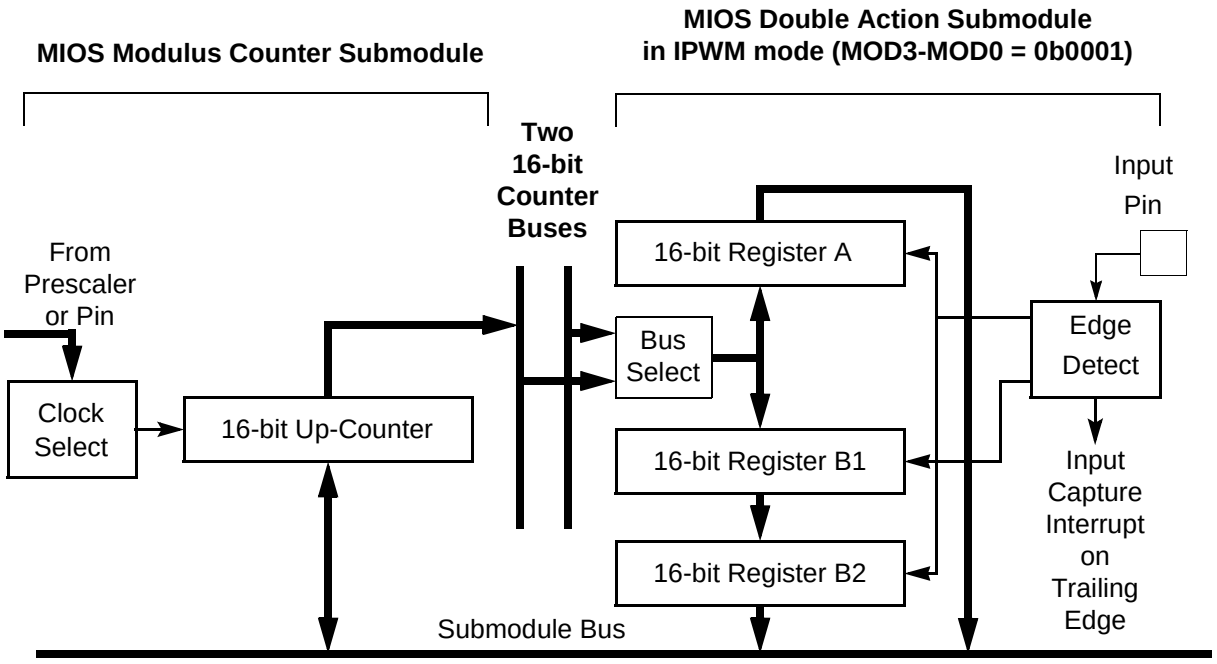

Figure 15-9 MIOS1 Example: Double Capture Pulse Width Measurement

15.15.2 MIOS1 Input Double Edge Period Measurement

Two samples are available to the software from an MIOS double action submodule for period measurement. The software can read the previous and the current edge samples and subtract them. As with pulse width measurement, the software can be sure not to miss samples by ensuring that the interrupt response time is faster than the fastest input period. Alternately, when the software is just interested in the latest period measurement, one 32-bit coherent read instruction can get both the current and the previous samples. Depending on the prescaler divide ratio, period times can be measured from 50 ns to 6.7 s.

Figure 15-10 shows a counter submodule and a DASM combination as an example of period measurement. The software designates whether the rising or falling edge of the input signal is to be used for the measurements. When the edge is detected, the state of the 16-bit counter bus is stored in register A and the content of register B1 is transferred to register B2. After register B2 is safely latched, the content of register A is transferred to register B1. This procedure gives the software coherent current and previous samples in registers A and B2 at all times. An interrupt is available for the cases where the software needs to be aware of each new sample. Note that a software option is provided to also generate an interrupt after the first edge.

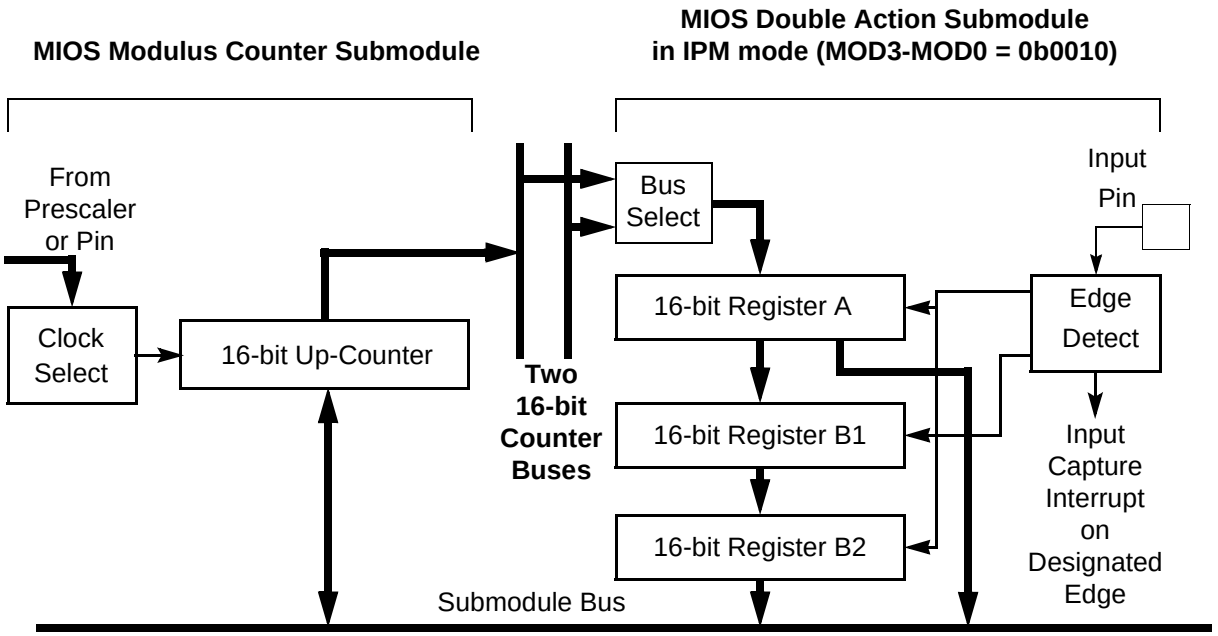

Figure 15-10 MIOS1 Example: Double Capture Period Measurement

15.15.3 MIOS1 Double Edge Single Output Pulse Generation

Software can initialize the MIOS1 to generate both the rising and the falling edge of an output pulse. With a MDASM, pulses as narrow as 50 ns can be generated since software action is not needed between the edges. Pulses as long as 2.1 s can be generated. When an interrupt is desired, it can be selected to occur on every edge or only after the second edge.

Figure 15-11 shows how a counter submodule and a MDASM can be used to generate both edges of a single output pulse. The software puts the compare value for one edge in register A and the other one in register B2. The MDASM automatically creates both edges and the pulse can be selected by software to be a high-going or a low-going. After the trailing edge, the MDASM stops to await further commands from the software. Note that a single edge output can be generated by writing to only one register.

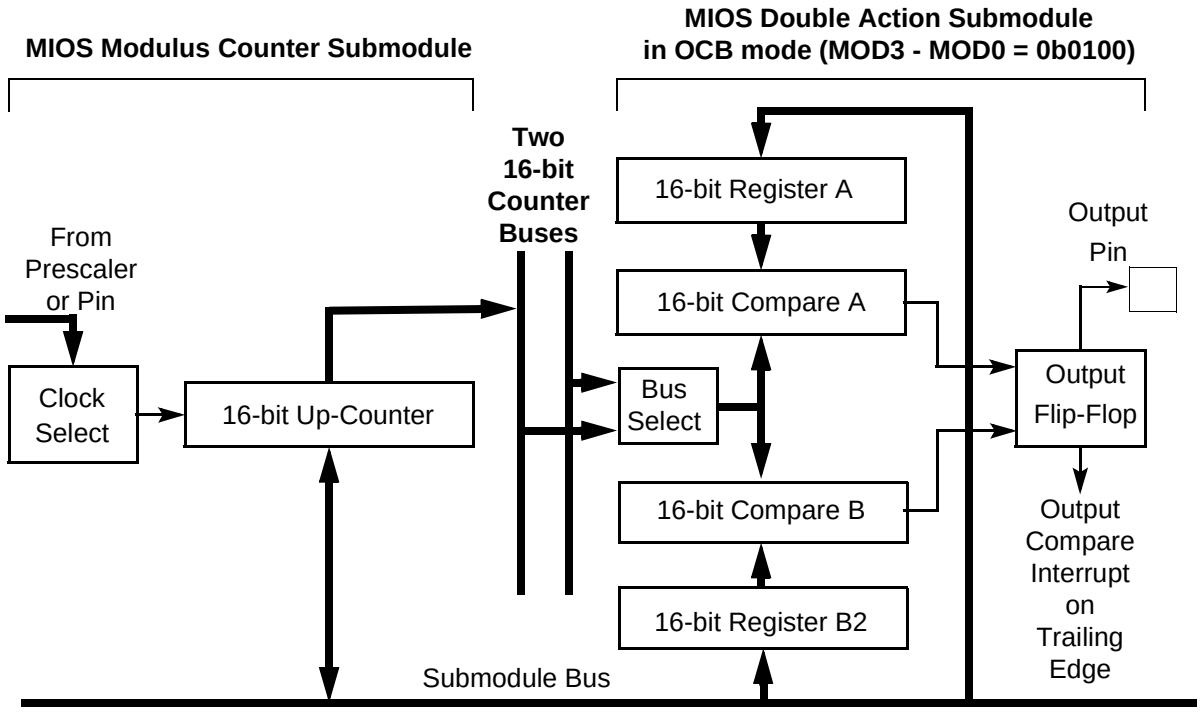

Figure 15-11 MIOS1 Example: Double Edge Output Compare

15.15.4 MIOS1 Output Pulse Width Modulation With MDASM

Output waveforms can be generated with any duty cycle without software involvement. The software sets up a MDASM with the compare times for the rising and falling edges and they are automatically repeated. The software does not need to respond to interrupts to generate continuous pulses. The frequency may be selected as the frequency of a free-running counter time-base, times a binary multiplier selected in the MDASM. Multiple PWM outputs can be created from multiple MDASMs and share one counter submodule, provided that the frequencies of all of the output signals are a binary multiple of the time-base and that the counter submodule is operating in a free-running mode. Each MDASM has a software selectable “don’t care” on high-order bits of the time-base comparison so that the frequency of one output can be a binary multiple of another signal. Masking the time-base serves to multiply the frequency of the time-base by a binary number to form the frequency of the output waveform. The duty cycle can vary from one cycle to 64-Kbyte cycles. The frequency can range from 0.48 Hz to 156 kHz, though the resolution decreases at the higher frequencies to as low as 7 bits. The generation of output square wave signals is of course the special case where the high and low times are equal.

When an MMCSM is used to drive the time-base, the modulus value is the period of the output PWM signal. **Figure 15-12** shows such an example. The polarity of the leading edge of an output waveform is programmable for a rising or a falling edge. The software selects the period of the output signal by programming the MMCSM with a modulus value. The leading edge compare value is written into register A by software and the trailing edge time is written into register B1. When the leading edge value is reached, the content of register B1 is transferred to register B2, to form the next trailing edge value. Subsequent changes to the output pulse width are made by writing a new time into register B1. Updates to the pulse width are always synchronized to the leading edge of the waveform.

It is typical to use the pulse width modulation mode of the MDASM without interrupts, although an interrupt can be enabled to occur on the leading edge. When the output is an unchanging repetitive waveform, the MDASM continuously generates the signal without any software intervention. When the software needs to change the pulse width, a new trailing edge time is written to the MDASM. The output is changed on the next full pulse. When the software needs to change the output at a regular rate, such as an acceleration curve, the leading edge interrupt gives the software one period time to update the new trailing edge time.

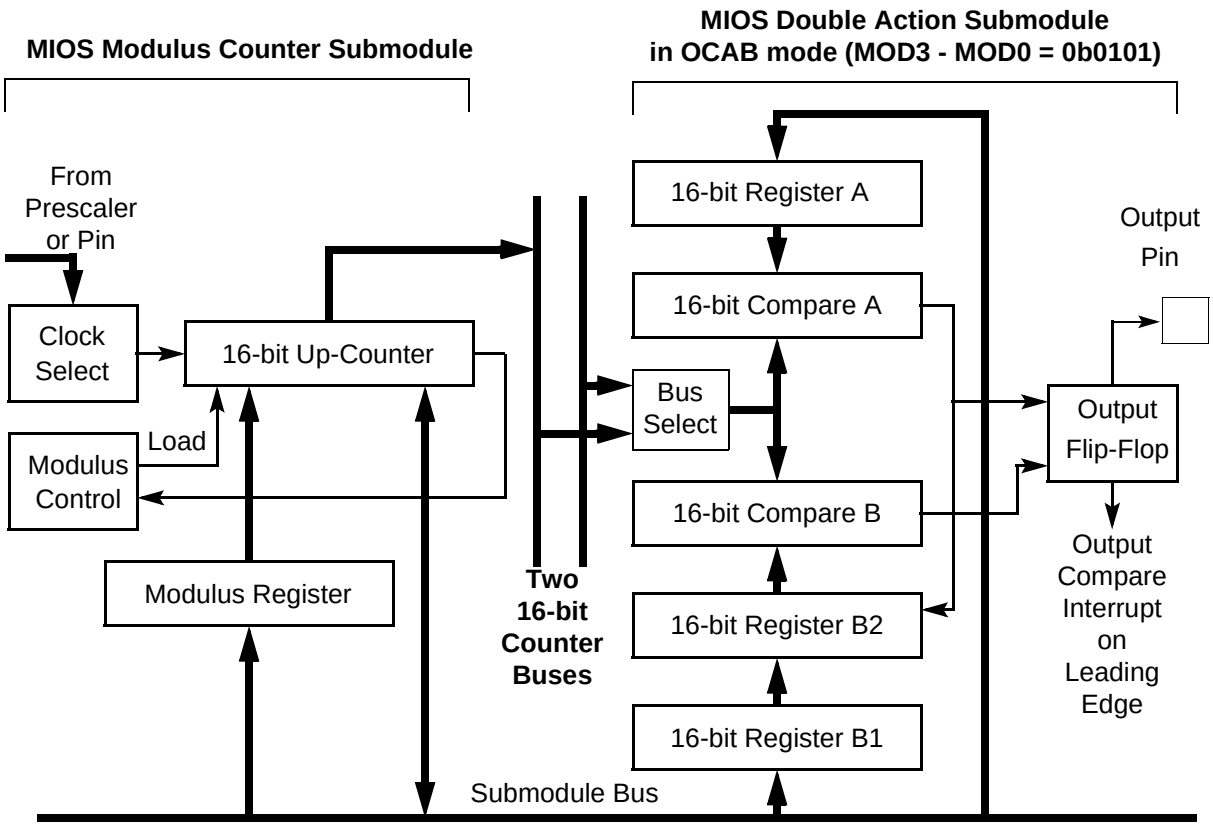

Figure 15-12 MIOS1 Example: Pulse Width Modulation Output

15.15.5 MIOS1 Input Pulse Accumulation

Counting the number of pulses on an input signal is another capability of the MIOS1. Pulse accumulation uses an MMCSM. Since the counters in the counter submodules are software accessible, pulse accumulation does not require the use of an action submodule. The pulse accumulation can operate continuously, interrupting only on binary overflow of the 16-bit counter. When an MMCSM is used, an interrupt can instead be created when the pulse accumulation reaches a preprogrammed value. To do that, the two's complement of the value is put in the modulus register and the interrupt occurs when the counter overflows.

15.16 MIOS1 Configuration

The complete MIOS1 submodule and pin configuration is shown in **Table 15-36**.

Table 15-36 MIOS1 Configuration

Submodule type	Submodule Number	connected to: CBA BSL=00	CBB BSL=01	CBC BSL=10	CBD BSL=11	RQSM Number	RQSM Bit Position	Base Address	Pin Function	Input Pin Name	Output Pin Name	Alternate Pin Function
MPWMSM	0					0	0	0x30 6000	PWM, I/O	MPWM0	MPWM0	
MPWMSM	1					0	1	0x30 6008	PWM, I/O	MPWM1	MPWM1	
MPWMSM	2					0	2	0x30 6010	PWM, I/O	MPWM2	MPWM2	
MPWMSM	3					0	3	0x30 6018	PWM, I/O	MPWM3	MPWM3	
Reserved	4-5											
MMCSM	6	CB6				0	6	0x30 6030	Clock In	MDA11		
									Load In	MDA12		
Reserved	7-10											
MDASM	11	CB6	CB22			0	11	0x30 6058	Channel I/O	MDA11	MDA11	
MDASM	12	CB6	CB22			0	12	0x30 6060	Channel I/O	MDA12	MDA12	
MDASM	13	CB6	CB22			0	13	0x30 6068	Channel I/O	MDA13	MDA13	
MDASM	14	CB6	CB22			0	14	0x30 6070	Channel I/O	MDA14	MDA14	
MDASM	15	CB6	CB22			0	15	0x30 6078	Channel I/O	MDA15	MDA15	
MPWMSM	16					1	0	0x30 6080	PWM, I/O	MPWM16	MPWM16	
MPWMSM	17					1	1	0x30 6088	PWM, I/O	MPWM17	MPWM17	
MPWMSM	18					1	2	0x30 6090	PWM, I/O	MPWM18	MPWM18	
MPWMSM	19					1	3	0x30 6098	PWM, I/O	MPWM19	MPWM19	
Reserved	20-21											
MMCSM	22		CB22			1	6	0x30 60B0	Clock In	MDA13		
									Load In	MDA14		
Reserved	23-26											
MDASM	27	CB6	CB22			1	11	0x30 60D8	Channel I/O	MDA27	MDA27	
MDASM	28	CB6	CB22			1	12	0x30 60E0	Channel I/O	MDA28	MDA28	
MDASM	29	CB6	CB22			1	13	0x30 60E8	Channel I/O	MDA29	MDA29	
MDASM	30	CB6	CB22			1	14	0x30 60F0	Channel I/O	MDA30	MDA30	
MDASM	31	CB6	CB22			1	15	0x30 60F8	Channel I/O	MDA31	MDA31	
MPIOSM	32							0x30 6100	GP I/O[1]	MPIO32B0	MPIO32B0	VF0
									GP I/O	MPIO32B1	MPIO32B1	VF1
									GP I/O	MPIO32B2	MPIO32B2	VF2
									GP I/O	MPIO32B3	MPIO32B3	VFLS0
									GP I/O	MPIO32B4	MPIO32B4	VFLS1
									GP I/O	MPIO32B5	MPIO32B5	
									GP I/O	MPIO32B6	MPIO32B6	
									GP I/O	MPIO32B7	MPIO32B7	
									GP I/O	MPIO32B8	MPIO32B8	
									GP I/O	MPIO32B9	MPIO32B9	

Table 15-36 MIOS1 Configuration (Continued)

Submodule type	Submodule Number	connected to: CBA BSL=00	CBB BSL=01	CBC BSL=10	CBD BSL=11	RQSM Number	RQSM Bit Position	Base Address	Pin Function	Input Pin Name	Output Pin Name	Alternate Pin Function
									GP I/O	MPIO32B10	MPIO32B10	
									GP I/O	MPIO32B11	MPIO32B11	
									GP I/O	MPIO32B12	MPIO32B12	
									GP I/O	MPIO32B13	MPIO32B13	
									GP I/O	MPIO32B14	MPIO32B14	
									GP I/O	MPIO32B15	MPIO32B15	
Reserved	33-255											
MBISM	256							0x30 6800				
Reserved	257											
MCPSM	258							0x30 6810				
Reserved	259											
RQSM0	384-391							0x30 6C00				
RQSM1	392-399							0x30 6C40				
Reserved	400-511											

NOTES:

1. GP = General purpose.