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MODEL P104-DIO-96

USER MANUAL

FILE: mp104-dio-96.A1j

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WARNING!!

ALWAYS CONNECT AND DISCONNECT YOUR FIELD CABLING WITH THE COMPUTER POWER OFF. ALWAYS TURN COMPUTER POWER OFF BEFORE INSTALLING A CARD. CONNECTING AND DISCONNECTING CABLES, OR INSTALLING CARDS INTO A SYSTEM WITH THE COMPUTER OR FIELD POWER ON MAY CAUSE DAMAGE TO THE I/O CARD AND WILL VOID ALL WARRANTIES, IMPLIED OR EXPRESSED.

Warranty

Prior to shipment, ACCES equipment is thoroughly inspected and tested to applicable specifications. However, should equipment failure occur, ACCES assures its customers that prompt service and support will be available. All equipment originally manufactured by ACCES which is found to be defective will be repaired or replaced subject to the following considerations.

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If a unit is suspected of failure, contact ACCES' Customer Service department. Be prepared to give the unit model number, serial number, and a description of the failure symptom(s). We may suggest some simple tests to confirm the failure. We will assign a Return Material Authorization (RMA) number which must appear on the outer label of the return package. All units/components should be properly packed for handling and returned with freight prepaid to the ACCES designated Service Center, and will be returned to the customer's/user's site freight prepaid and invoiced.

Coverage

First Three Years: Returned unit/part will be repaired and/or replaced at ACCES option with no charge for labor or parts not excluded by warranty. Warranty commences with equipment shipment.

Following Years: Throughout your equipment's lifetime, ACCES stands ready to provide on-site or in-plant service at reasonable rates similar to those of other manufacturers in the industry.

Equipment Not Manufactured by ACCES

Equipment provided but not manufactured by ACCES is warranted and will be repaired according to the terms and conditions of the respective equipment manufacturer's warranty.

General

Under this Warranty, liability of ACCES is limited to replacing, repairing or issuing credit (at ACCES discretion) for any products which are proved to be defective during the warranty period. In no case is ACCES liable for consequential or special damage arriving from use or misuse of our product. The customer is responsible for all charges caused by modifications or additions to ACCES equipment not approved in writing by ACCES or, if in ACCES opinion the equipment has been subjected to abnormal use. "Abnormal use" for purposes of this warranty is defined as any use to which the equipment is exposed other than that use specified or intended as evidenced by purchase or sales representation. Other than the above, no other warranty, expressed or implied, shall apply to any and all such equipment furnished or sold by ACCES.

Table of Contents

Chapter 1: Introduction

Each I/O line of this board is buffered and capable of sourcing 32mA or sinking 64mA. The board simulates Programmable Peripheral Interface chips (PPI) to provide a computer interface to digital I/O lines. Each PPI supports two 8-bit ports (A, B) and two 4-bit ports (C_{hi}, C_{low}). Each port can be configured to function as either inputs or output latches. The I/O line buffers (types 74ABT240 and 74ABT245) are configured automatically by hardware logic for input or output according to the PPI Control Register direction software assignment.

The board may be shipped with a register map optimized for a higher speed than the pure i8255 port/address map. See the Programming section for an explanation of how a 25% increase in I/O speed is achieved.

Outputs of the I/O buffers are pulled up through 10KΩ resistors to +5VDC. On power-up all I/O pins are inputs. This means that the lines are at a logic HIGH. The user may request the factory to remove these 10KΩ resistors so that the I/O lines will not be driven on power-up (10 uA leakage per pin).

I/O wiring connections are via 50-pin headers on the board. This provides compatibility with OPTO-22, Gordos, Potter & Brumfield, Western Reserve Controls, etc. module mounting racks. Every second conductor of the flat cables is grounded to minimize crosstalk. If needed for external circuits, +5VDC power is available on each I/O connector at pin 49. If you use this power, we recommend that you include a 1A fast blow fuse in your circuits in order to avoid possible damage to the host computer.

The board occupies 32 bytes within the PCI I/O space. The base address is assigned by the system. Refer to the Option Selection Section of this manual for a detailed description.

Specification

Data Transfer Rate, I/O Mapped, 33MHz bus
- From I/O connector to PCI bus: 7.37M bytes per second in 8255 emulation mode
- From PCI bus to I/O connector: 14.74M bytes per second in 8255 emulation mode
- From I/O connector to PCI bus: 9M bytes per second with Fast PPI port map
- From PCI bus to I/O connector: 18M bytes per second with Fast PPI port map

Data Transfer Rate, Memory Mapped, 33MHz bus
- From I/O Connector to PCI bus: 12M bytes per second in 8255 emulation mode
- From PCI bus to I/O connector: 24M bytes per second in 8255 emulation mode
- From I/O connector to PCI bus: 28M bytes per second with Fast PPI port map
- From PCI bus to I/O connector: 18M bytes per second with Fast PPI port map

Digital Inputs (TTL Compatible)
- Logic High: 2.0 to 5.0 VDC
- Logic Low: -0.5 to +0.8 VDC
- Input Load (High):   10uA
- Input Load (Low):   -10uA

Digital Outputs
- Logic High: 2.5 VDC min., source 32 mA
- Logic Low: 0.5 VDC max., sink 64 mA
- Power Output: +5 VDC from computer bus (onboard resettable 0.5A fuse) on each digital group's I/O connector
- Power Required: 290 mA typical at 5V (all I/O pins disconnected, all I/O ports set as inputs)

Environmental
- Operating Temperature: -20°C to +70°C
- Storage Temperature: -50°C to +120°C
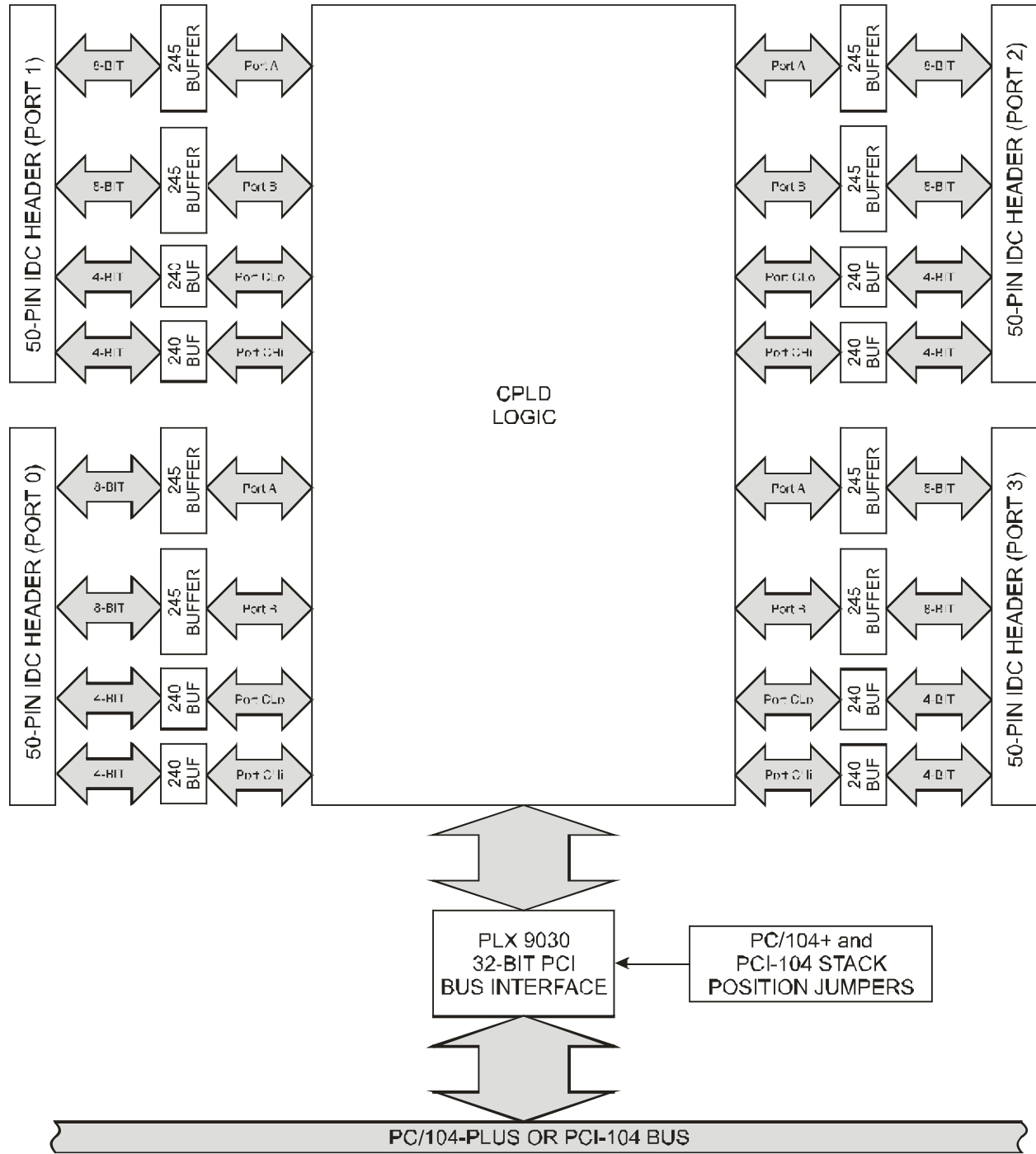- Humidity: 0 to 90% RH, non-condensing

Figure 1-1: Block Diagram

Chapter 2: Installation

A printed Quick-Start Guide (QSG) is packed with the board for your convenience. If you've already performed the steps from the QSG, you may find this chapter to be redundant and may skip forward to begin developing your application.

The software provided with this PC/104-Plus Board is on CD and must be installed onto your hard disk prior to use. To do this, perform the following steps as appropriate for your operating system. Substitute the appropriate drive letter for your CD-ROM where you see d: in the examples below.

CD Installation
The following instructions assume the CD-ROM drive is drive "D". Please substitute the appropriate drive letter for your system as necessary.

DOS
1. Place the CD into your CD-ROM drive.
2. Type `D : Enter` to change the active drive to the CD-ROM drive.
3. Type `I N S T A L L Enter` to run the install program.
4. Follow the on-screen prompts to install the software for this board.

WINDOWS
1. Place the CD into your CD-ROM drive.
2. The system should automatically run the install program. If the install program does not run promptly, click START | RUN and type `D : I N S T A L L`, click OK or press `Enter`.
3. Follow the on-screen prompts to install the software for this board.

LINUX
1. Please refer to linux.htm on the CD-ROM for information on installing under linux.

Installing the Hardware
Before installing the board, please run Setup.exe. The Setup program can be used to assist in configuring the two switches on the board. Our setup program will lead the user through the process of setting the options on the board (the program does not set the options on the board).

The PCI bus clock trace length from the CPU to the cards in the stack is tuned so that the clock edge arrives at the interface when data is valid. Since boards in the PC/104 stack are at different distances from the CPU, provision is made on the CPU board to supply four clock signals with compensating trace lengths. Two signals from other groups must be likewise selected: IDSEL and INT. When the PCI bus is being initialized, the operating system will enable each card with a hard-wired select line and read it's configuration registers. An address is assigned, space in the memory map and I/O map is reserved, etc. Similarly, the CPU's interrupt controller resources (INTA, INTB, INTC, INTD) will be distributed among the cards in the stack. A set of four-to-one multiplexers and two slide switches are used to select which PCI clock, IDSEL and INT lines are routed to the board's PCI bus interface.

Only four boards are allowed in a PCI-Plus stack, each board must get a specific set of signals. These signals are selected with two slide switches, labeled SEL-1 and SEL-2, which form a binary value to control the mux (SEL-1 is the least significant bit and SEL-2 is the most significant bit). If the board is closest to the CPU, slide both switches to the right. This will select the signal with the longest trace on the CPU board (signal group 0). If this product is the farthest board from the CPU, slide both switches to the left. This will select the signal with the shortest trace on the CPU board (signal group 3). Place the SEL-1 switch to the left and SEL-2 to the right to select signal group 1, place the SEL-1 switch to the right and SEL-2 to the left to select signal group 2.

Manual P104-DIO-96

To install the board:

1. Turn off the computer power.
2. Position the slide switches to select the clock, IDSEL, and interrupt signal group.
3. Install the card in a PC/104-Plus stack.
4. Install I/O cables at P1 and P2.
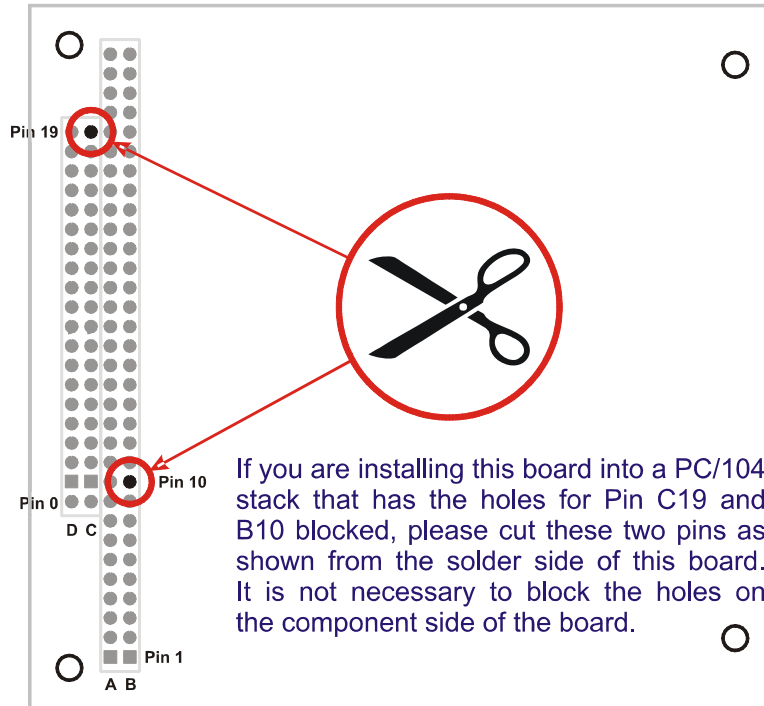5. Inspect for proper fit of the card and cable and then tighten the screws

Pin 19

Pin 10

Pin 0

D C

If you are installing this board into a PC/104 stack that has the holes for Pin C19 and B10 blocked, please cut these two pins as shown from the solder side of this board. It is not necessary to block the holes on the component side of the board.

Pin 1

A B

Figure 2-1: PC/104 Key Information

Chapter 3: Option Selection

Most PCI bus signals are common to all four boards in the PCI stack. However, there are four unique signal groups, one for each board. The slide switches select which signal group goes to each card. The card in the stack closest to the CPU board must get signal group 0.
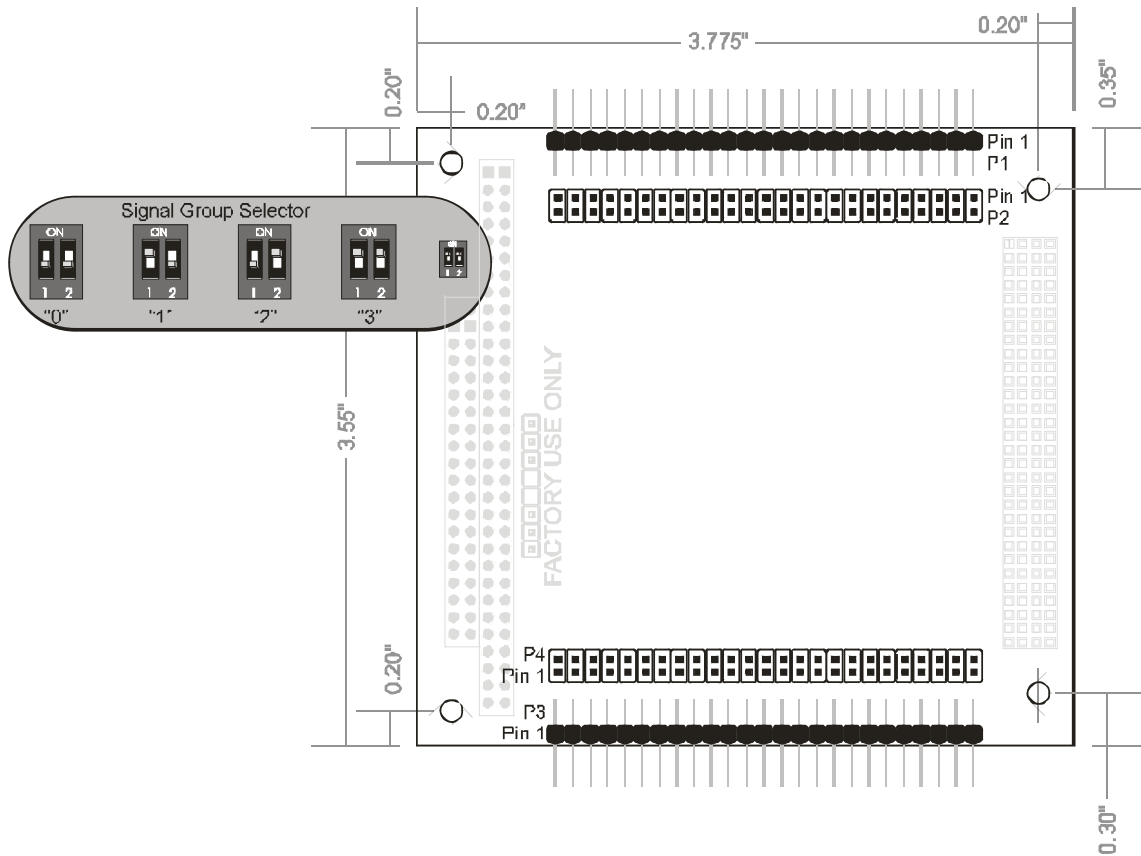

Figure 3-1: Option Selection Map

Chapter 4: Address Selection

The system BIOS or operating system will assign the address. This board occupies 32 bytes of I/O space.

PCI architecture is Plug-and-Play. This means that the BIOS or Operating System determines the resources assigned to PCI cards rather than you selecting those resources with switches or jumpers. As a result, you cannot set or change the card's base address. You can only determine what the system has assigned.

To determine the base address that has been assigned, run the PCIFind.EXE, or PCINT utility program provided. This utility will display a list of all of the cards detected on the PCI bus, the addresses assigned to each function on each of the boards, and the respective IRQs (if any) allotted.

Alternatively, some operating systems (Windows 95/98/2000) can be queried to determine which resources were assigned. In these operating systems, you can use either PCIFind (DOS), PCINT (Windows95/98/NT), or the Device Manager utility from the System Applet of the control panel. The board is installed in the Data Acquisition class of the Device Manager list. Selecting the card, clicking Properties, and then selecting the Resources Tab will display a list of the resources allocated to the card.

The PCI bus supports 64K of I/O space. Your board's addresses may be located anywhere in the 0400 to FFE0 hex range.

PCIFind uses the Vendor ID and Device ID to search for your board, then reads the base address and IRQ.

If you want to determine the base address and IRQ yourself, use the following information.

> The Vendor ID for the board is 494F. (ASCII for "IO")
> The Device ID for the board is 0x0C69.

Chapter 5: Programming

The board is an I/O mapped device that is easily configured from any language and any language can easily perform digital I/O through the board's ports. This is especially true if the form of the data is byte or word wide. All references to the I/O ports would be in absolute port addressing. However, a table could be used to convert the byte or word data ports to a logical reference.

Developing Your Own Software

If you wish to gain a better understanding of the programs listed in the previous section, then the information in the following paragraphs will be of interest to you.

Four register locations are required per 24-bit group. Thus the 96 uses a total of 16 registers for groups 0 through 3.

Offset	Standard 8255 Compatibility Option Write	Read	Improved Speed Option Write	Read
Base+0	Group 0 Port A	Group 0 Port A	Group 0 Port A	Group 0 Port A
Base+1	Group 0 Port B	Group 0 Port B	Group 0 Port B	Group 0 Port B
Base+2	Group 0 Port C	Group 0 Port C	Group 0 Port C	Group 0 Port C
Base+3	Group 0 CMD		Group 1 Port A	Group 1 Port A
Base+4	Group 1 Port A	Group 1 Port A	Group 1 Port B	Group 1 Port B
Base+5	Group 1 Port B	Group 1 Port B	Group 1 Port C	Group 1 Port C
Base+6	Group 1 Port C	Group 1 Port C	Group 2 Port A	Group 2 Port A
Base+7	Group 1 CMD		Group 2 Port B	Group 2 Port B
Base+8	Group 2 Port A	Group 2 Port A	Group 2 Port C	Group 2 Port C
Base+9	Group 2 Port B	Group 2 Port B	Group 3 Port A	Group 3 Port A
Base+A	Group 2 Port C	Group 2 Port C	Group 3 Port B	Group 3 Port B
Base+B	Group 2 CMD		Group 3 Port C	Group 3 Port C
Base+C	Group 3 Port A	Group 3 Port A	Group 0 CMD	
Base+D	Group 3 Port B	Group 3 Port B	Group 1 CMD	
Base+E	Group 3 Port C	Group 3 Port C	Group 2 CMD	
Base+F	Group 3 CMD		Group 3 CMD	
Base+10 through Base+1E	Reserved	Reserved	Reserved	Reserved
Base+1F	Reset Card		Reset Card	

Table 5-1: Base Registers

The board is designed to use each of these PPI's in mode 0 wherein:

     a.   There are two 8-bit ports (A and B) and two 4-bit ports (C Hi and C Lo).
     b.   Any port can be configured as an input or an output.
     c.   Outputs are latched.
     d.   Inputs are not latched.

Each PPI contains a control register. This Write-only, 8-bit register is used to set the mode and direction of the ports. At Power-Up or Reset, all I/O lines are set as inputs. Output buffers are automatically set by hardware logic according to the control register states. Control registers are located at base addresses +3, +7, +B, and +F. Bit assignments in each of these control registers are as follows:

Bit	Assignment	Function
D0	Port C Lo (C0-C3)	1 = Input, 0 = Output
D1	Port B	1 = Input, 0 = Output
D2	Backward Compatible	Must be 0
D3	Port C Hi (C4-C7)	1 = Input, 0 = Output
D4	Port A	1 = Input, 0 = Output
D5,D6	Backward Compatible	Must be 0
D7	Mode Set Flag & Tristate	1 = Active

Table 5-2: Control Register Bit Assignments

Note
Because all I/O pins are buffered, the 8255 individual bit control feature is not available. The hardware uses the control registers to manage buffer direction on this board.

The board emulates four Intel 8255 PPIs. The bit assignments and functionality of the control register has been kept to maintain backward compatibility with existing software. The emulated 8255 chips differ from the original in that when a port is configured to be outputs, the I/O pins default to a HIGH state rather than a LOW state. A port that is programmed to be inputs may have a value written to it. A READ of the port will return the state of the I/O pins in that case. When that port is configured to be an output latch the value previously written to it will be driven on the I/O pins.

The board will occupy two spaces in memory. One space is I/O mapped and burst READs or WRITEs will not work. The other space is memory mapped and should be found below the 1 megabyte boundary (to facilitate DOC programs) and bursts of four double words are possible. The PCIFIND.EXE program will display the board's locations in memory.

The user may specify one of two register mappings (see the Base Registers table in the Programming chapter): 8255 standard, or an enhanced speed map. The latter allows the user to read from or write to more ports with a single operation (32 bits versus 24 bits).

Because many motherboard's reset circuits do not accurately wait for the 3.3V power supply to finish the power-on sequence, before using the board at each power-up it is necessary to issue a single "Write to Base +1F" to "Reset" the onboard circuitry.

Programming Example

The following programming example is provided as a guide to assist you in developing your working software. In this example, the board base address is 2D00 hex and I/O lines of Port 0 are to be setup as follows:

port A	=	Input
port B	=	Output
port C hi	=	Input
port C lo	=	Output

Configure bits of the Control Register as:

D7	1	Active Mode Set
D6	0	0
D5	0	0
D4	1	Port A = input
D3	1	Port C Hi = input
D2	0	0
D1	0	Port B = output
D0	0	Port C Lo = output

This corresponds to 98 hex. If the card base address is 2D00 hex, use the BASIC OUT command to write to the control register as follows:

```
10      BASEADDR=&H2D00
20      OUT BASEADDR+3,&H98
```

To read the inputs at Port A and the upper nybble of Port C, use the BASIC INPUT command:

```
30      X=INP(BASEADDR)'Read Port A
40      Y=INP(BASEADDR+2)/16'Read Port C Hi
```

To set outputs high ("1") at Port B and the lower nybble of Port C:

```
50      OUT BASEADDR+1,&HFF'Turn on all Port B bits
60      OUT BASEADDR+2,&HF'Turn on all bits of Port C Lo
```

Chapter 6: Connector Pin Assignments

Note that the board uses four 50-pin Headers, each with equitable pinouts.

Assignment		Pin		Assignment	Pin
Port C Hi	PC7	1			2
	PC6	3			4
	PC5	5			6
	PC4	7			8
Port C Lo	PC3	9			10
	PC2	11			12
	PC1	13			14
	PC0	15			16
Port B	PB7	17			18
	PB6	19			20
	PB5	21		All Even Numbered Pins are GROUND	22
	PB4	23			24
	PB3	25			26
	PB2	27			28
	PB1	29			30
	PB0	31			32
Port A	PA7	33			34
	PA6	35			36
	PA5	37			38
	PA4	39			40
	PA3	41			42
	PA2	43			44
	PA1	45			46
	PA0	47			48
+5 VDC		49			50

Customer Comments

If you experience any problems with this manual or just want to give us some feedback, please email us at: *manuals@accesio.com.* Please detail any errors you find and include your mailing address so that we can send you any manual updates.

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