Technical Information Manual

Revision n. 2

9 June 2000

MOD. V 550 - V 550A

2 CHANNEL
C-RAMS

WARNING

Before inserting the module in a V430 Crate, if the -5 V from Jaux option is selected via internal jumpers, please verify the existence of the -5 V supply on the crate itself. If this is missing, the V550 will not operate correctly and might show a non-reversible failure in the ADC.

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1. DESCRIPTION

1.1. FUNCTIONAL DESCRIPTION

The model V550 CAEN Readout for Analog Multiplexed Signals (C-RAMS) is a 1-unit wide VME module housing 2 independent Analog to Digital Conversion blocks to be used for the readout of analog multiplexed signals coming from some of well known front-end chips (Amplex, Gasplex, Viking, etc.).

Each block of the module accepts positive, negative or differential input signals; the signals are amplified and fed to an ADC. The sensitivity (mV/bit) can be selected among 4 different values (with relative ratios of 1, 2, 5 and 10) by means of internal jumpers. The module has the following features:

- conversion rate up to 5 MHz.
- differential input with selectable amplification.
- 10 bit (V 550) / 12 bit (V 550 A) linear conversion.
- zero suppression and pedestal subtraction.
- diagnostics and self-test capabilities.

With the occurrence of an external CONVERT signal, the input signal is sampled by the ADC and its digital value is compared to a threshold value, if the signal is over threshold, the pedestal is subtracted and the result is stored in a Output Buffer arranged in FIFO logic 2K x 32 bit. For this purpose each block of the module houses two memories for the storage of the thresholds and the pedestals of each detector channel. The pedestal and threshold values are independent for each channel and the pedestal/threshold memory, which is arranged in 2K x 24 bit, can be filled (and read back) via VME with the desired values.

The number N of detector channels to be read out can be programmed via VME between 32 and 2016 in steps of 32. At the end of a conversion cycle (N CONVERT pulses), with the last word stored in the FIFO, if there are data in the FIFO, the module channel goes in the Data Ready state signaling that the data must be read via VME. A positive open-collector signal ("DRDY") is available for each channel on the front panel and is provided with two bridged connectors for daisy chaining. A fast CLEAR signal is also available for cycle abort.

It is possible to operate the module also in TEST mode (VME selectable) by simulating some input patterns, which can be written via VME, as if they were coming from the ADC.

The module houses a VME RORA INTERRUPTER[1]: via VME it is possible to program the interrupt generation on the logical OR of the two DRDY signals in a board.

The V550 Model uses the P1 and P2 connectors of VME and, optionally, the auxiliary connector for the CERN V430 VMEbus crate (Jaux Dataway) [1, 2]. With the Jaux connector it is possible to send via backplane the CONVERT, CLEAR and DRDY signals.

The module works in A24/A32 mode. The data transfer occurs in D32 mode. Block Transfer mode is also available.

The V550 Model can be controlled by the CAEN Model V551B C-RAMS SEQUENCER.
A single V551B Module can control up to 19 C-RAMS modules in a complete VME crate.

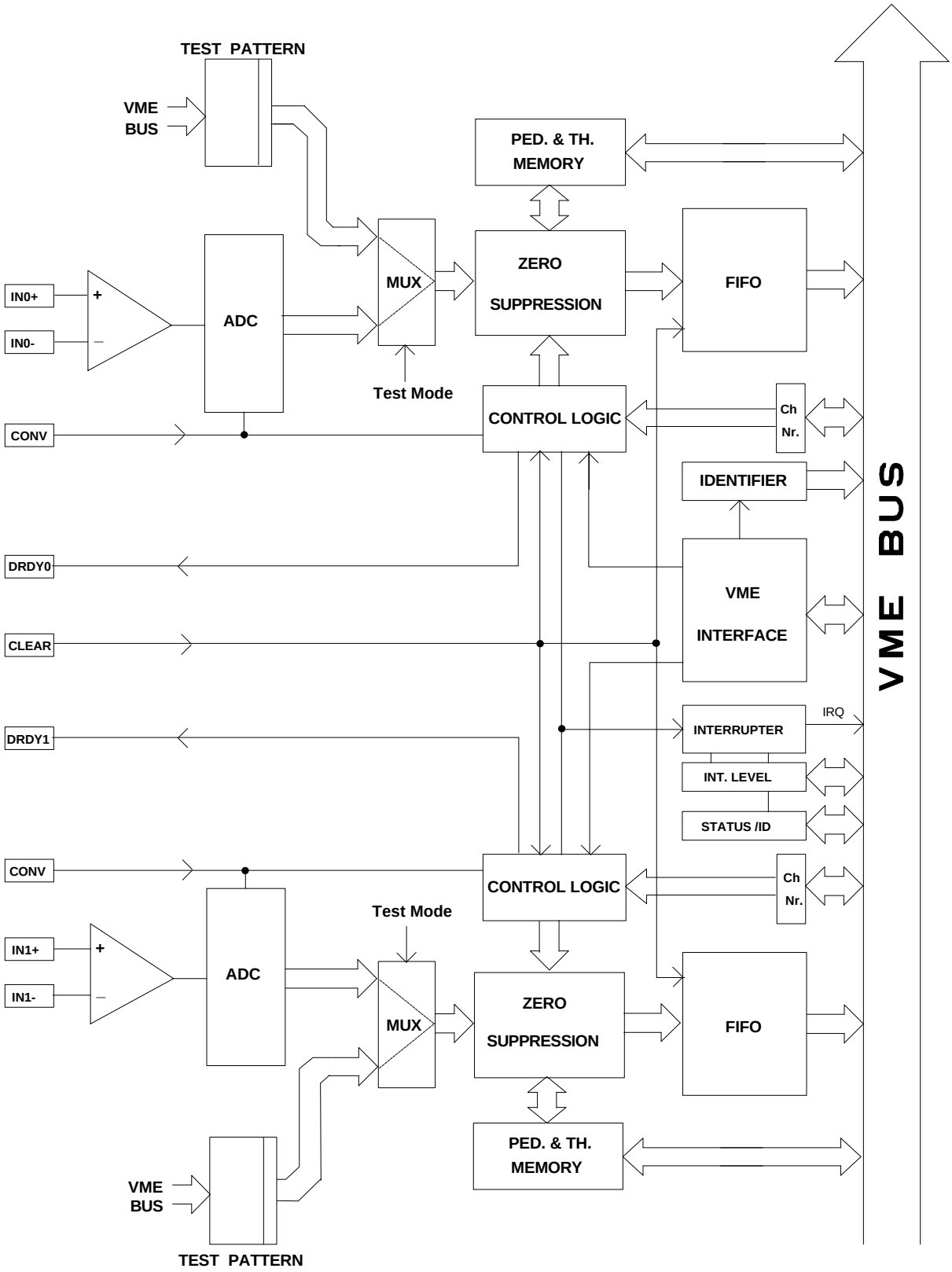

Fig. 1.1: Block Diagram

2. SPECIFICATIONS

2.1. INPUTS

- INPUT CHANNELS: Positive, negative or differential inputs on
  LEMO 00 type connectors; 50 Ω impedance;
  Input ranges: 150 mV, 300 mV, 750 mV and 1.5 V.

- CONVERT(1): Std. NIM level, high impedance, on two LEMO 00 type
  bridged connectors (for daisy chaining); requires termination
  if not chained, see note (1) here below.
  ECL differential on Jaux connector.
  Min. width 100 ns; Maximum sampling frequency: 5 MHz.
  A green LED lights up during a convert cycle or
  a Test Pattern injection.

- CLEAR(1): Std. NIM level, high impedance, on two LEMO 00 type
  bridged connectors (for daisy chaining); requires termination
  if not chained, see note (1) here below.
  ECL differential on Jaux connector.
  Min. width 50 ns.

2.2. OUTPUTS

- DATA READY: Std. TTL Open Collector on two LEMO 00 type
  bridged connectors (for daisy chaining);
  active high (the same on Jaux).
  A green LED lights up when the DRDY signal is asserted.

(1) High impedance input provided with two bridged connectors for daisy chaining. Note that the chain has to be terminated on 50 Ω on the last module; the same is needed also if only one module is used, whose input has thus to be properly matched.

2.3. PERFORMANCES AND TEST RESULTS

Integral Non Linearity:	± 0.1%
DC Pedestal:	10 ± 2 counts (V 550 for all input ranges).
	40 ± 8 counts (V 550A for all input ranges).

N.B.: The "DC Pedestal" is the digital value stored in the FIFOs when there is no input signal and the threshold is set to zero (Zero Suppression is disabled).

2.4. POWER REQUIREMENTS

+ 12 V	100 mA
– 12 V	200 mA (100 mA if Jaux is used)
+ 5 V	2.5 A
– 5 V	100 mA (only if Jaux is used)

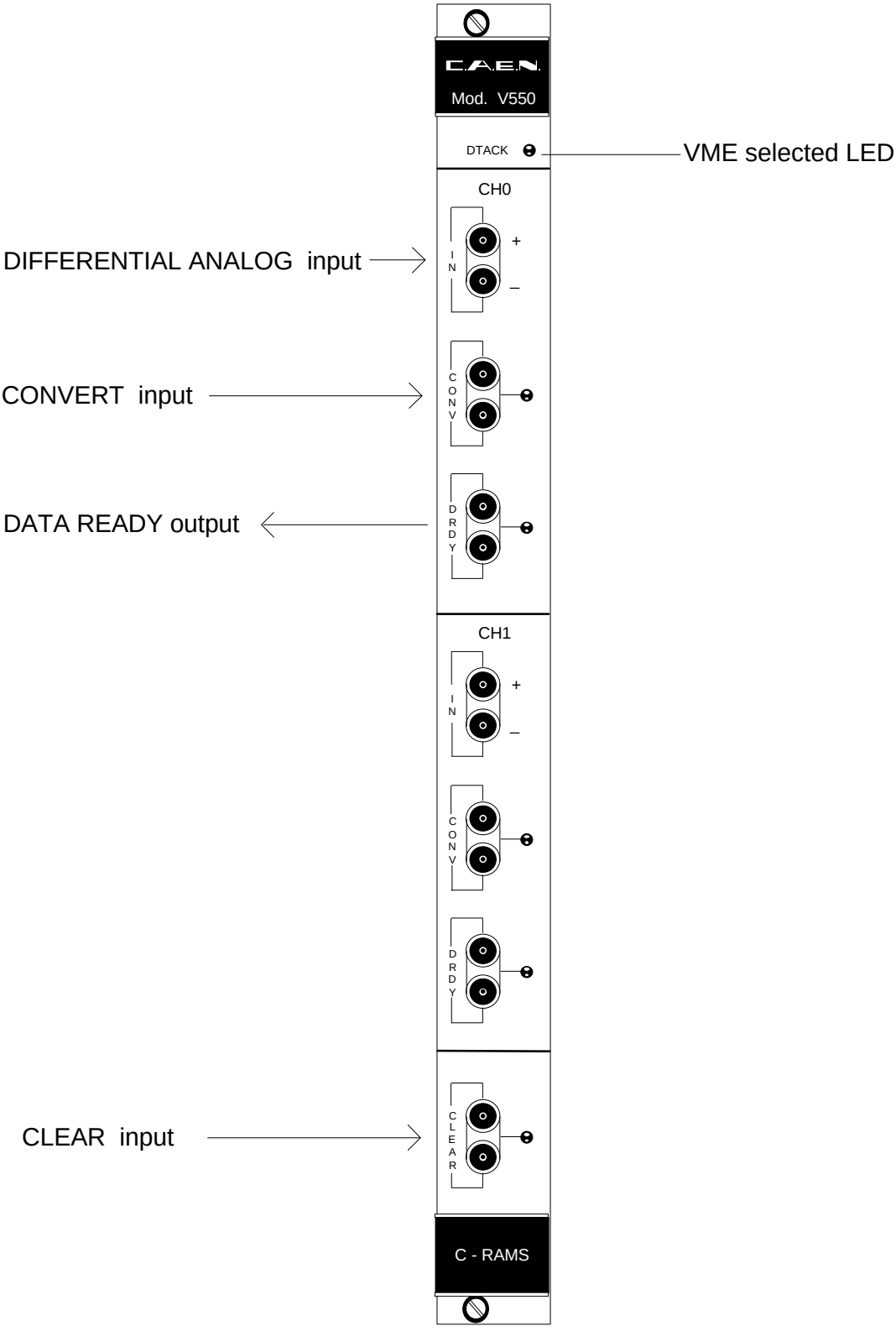

Fig. 2.1: Front Panel

2.5. INTERNAL COMPONENTS AND SETTINGS

(refer to fig. 2.2, 2.3)

SWITCHES, JUMPERS

- "JP1..JP8" jumpers; for the channel 0 sensitivity selection.

- "JP9..JP16" jumpers; for the channel 1 sensitivity selection:

for each channel, four different Full Scale Voltage Ranges are available by setting simultaneously JP1..JP4 for channel 0 Pedestal adjust, and JP5..JP8 for channel 0 Gain adjust (JP9..JP12 and JP13..JP16 respectively for channel 1). The four different levels of sensitivity are indicated with the numbers 1, 2, 3 and 4 which are printed close to the jumpers on the soldering side of the board, and correspond to the following full scale voltage ranges (e.g. for Channel 0):

Number 1 → 150 mV (JP4 and JP8 inserted)
Number 2 → 300 mV (JP3 and JP7 inserted)
Number 3 → 750 mV (JP2 and JP6 inserted)
Number 4 → 1.5 V (JP1 and JP5 inserted)

- "JP17" jumper; for the -5 V power selection:

by setting the jumper named JP17 is possible to choose the -5 V power supply coming from the -12 V VME (VEE position) power supply or directly from the -5 V Jaux (AUX position) power supply. Like the sensitivity selection jumpers JP1..JP16, this jumper is placed in the soldering side of the board.

- "S1", 2 DIP switches to enable/disable the CONV detection via the Jaux backplane signals CK and CK*.

- "S2", 2 DIP switches to enable/disable the CLEAR detection via the Jaux backplane signals CL and CL*.

- "S3" DIP switch to enable/disable the DRDY generation on the Jaux backplane signal SG.

By setting the three DIP switches S1, S2 and S3 in the OFF position, is possible to disable the CONV, CLEAR and DRDY signals handling via Jaux backplane. In this case the CK, CK*, CL, CL* and SG Jaux lines are disconnected.

- 1, socket strip housing a removable package resistor for the CK, CK*, CL, CL* Jaux lines termination (the resistor's common pin is shown in fig. 2.3). An alternative electrically isolated socket strip has been provided with the component side of the board: the removable package termination may be plugged here in case it is not used.

- 4 rotary switches for the module's VME Base Address selection.

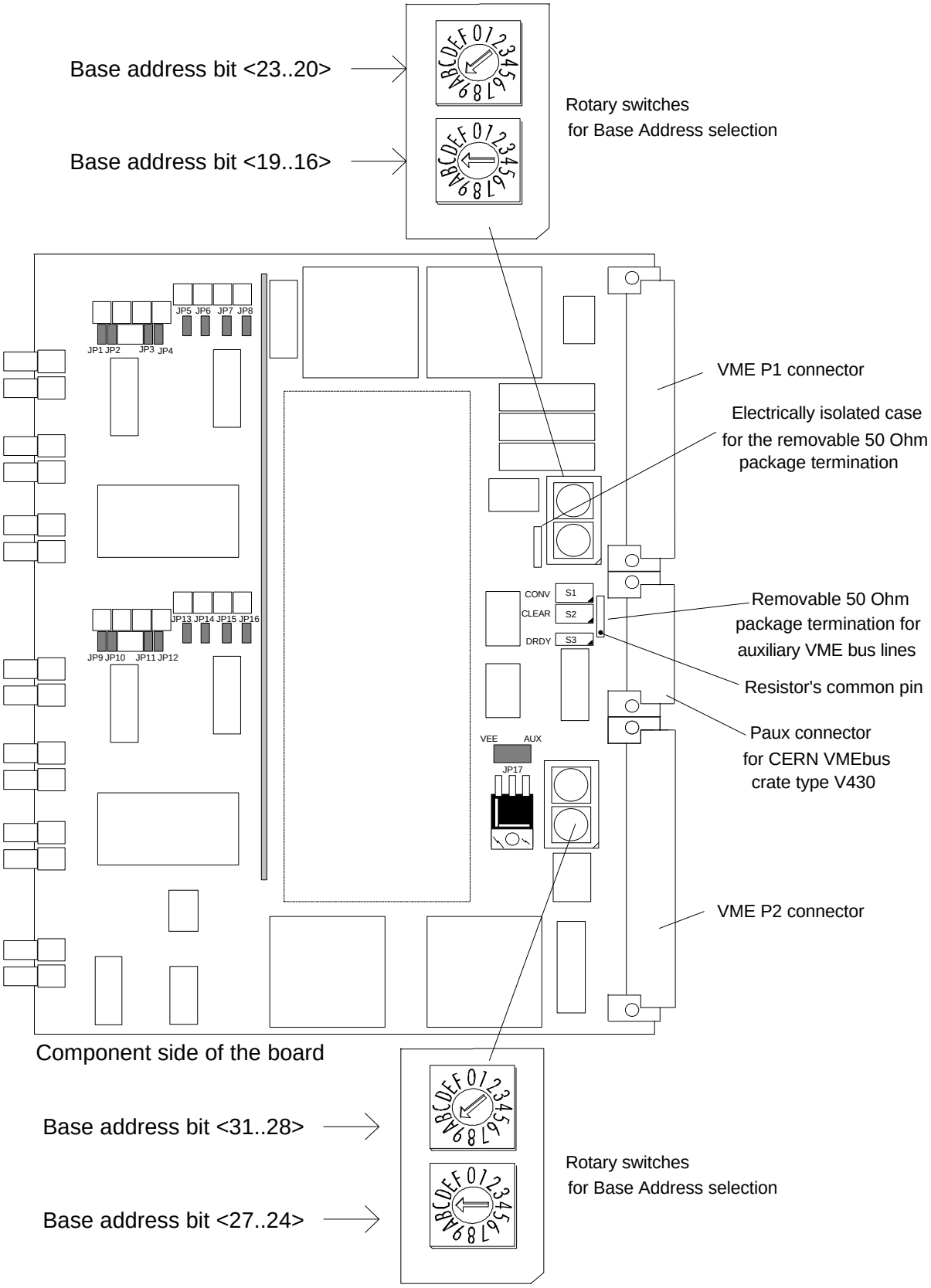

Fig. 2.2: Components Locations (component side)

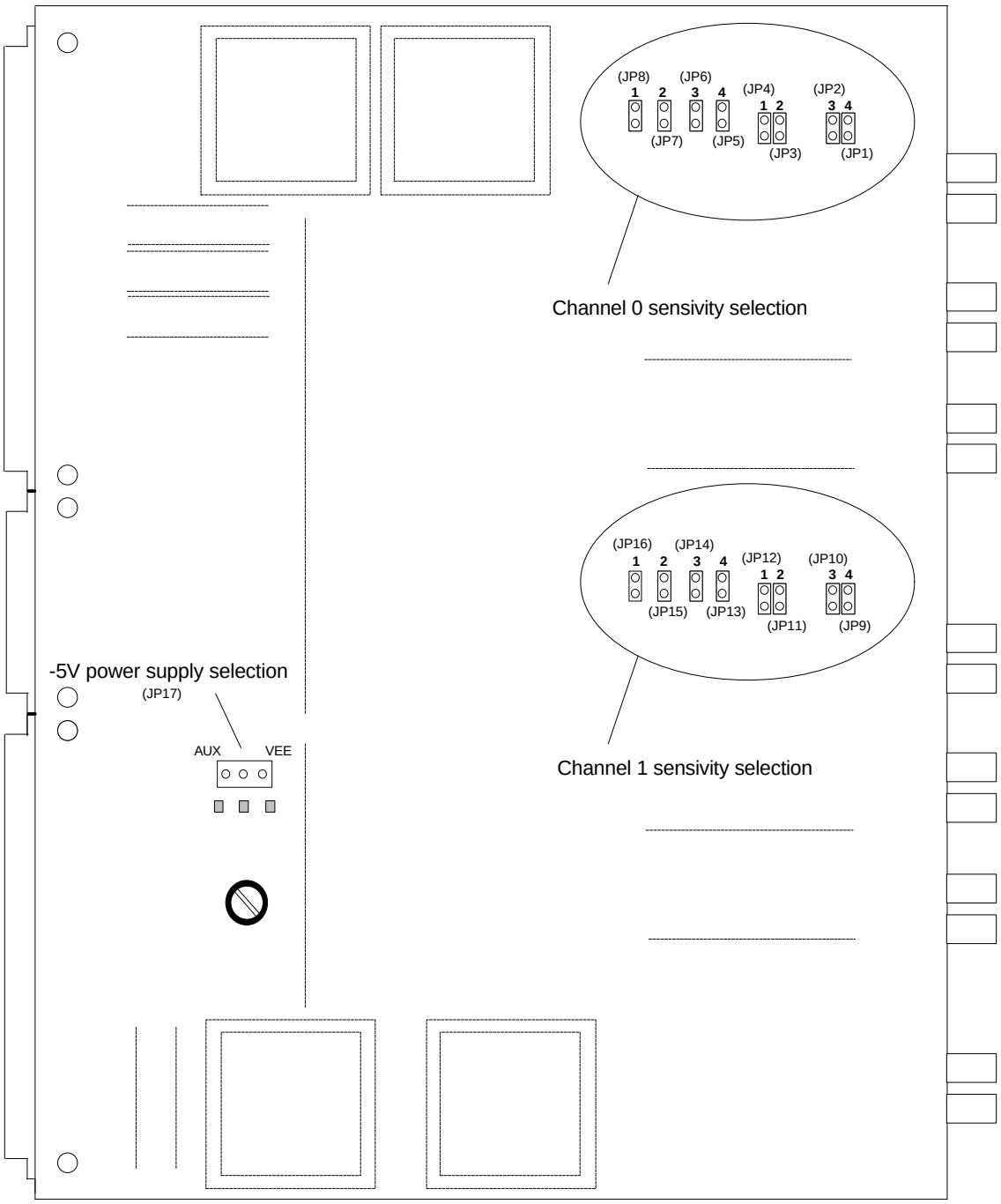

Fig. 2.3: Components Locations (soldering side)

3. VME INTERFACE

3.1. ADDRESSING CAPABILITY

The module works in A24/A32 mode. This implies that the module's address must be specified in a field of 24 or 32 bits. The Address Modifiers code recognized by the module are:

AM = %3F	A24 supervisory block transfer (BLT);
AM = %3D	A24 supervisory data access;
AM = %3B	A24 non privileged block transfer (BLT);
AM = %39	A24 non privileged data access;
AM = %0F	A32 supervisory block transfer (BLT);
AM = %0D	A32 supervisory data access;
AM = %0B	A32 non privileged block transfer (BLT);
AM = %09	A32 non privileged data access;

The module's Base Address is fixed by 4 internal rotary switches housed on two piggy-back boards plugged into the main printed circuit board (see Fig. 2.2).

The Base Address can be selected in the range:

% 00 0000	<->	% FF 0000	A24 mode
% 0000 0000	<->	% FFFF 0000	A32 mode

The Address Map of the page is shown in Table 3.1.

3.2. DATA TRANSFER CAPABILITY

The internal registers are accessible in D16 mode, while the FIFO and the Pedestal/Threshold memory are only accessible in D32 mode.

ADDRESS	REGISTER/CONTENT	TYPE
Base + %5FFC • • • Base + %4000	Pedestal/Threshold memory channel 1 • • • Pedestal/Threshold memory channel 1	read/write
Base + %3FFC • • • Base + %2000	Pedestal/Threshold memory channel 0 • • • Pedestal/Threshold memory channel 0	read/write
Base + %FE Base + %FC Base + %FA	Version & Series Manufacturer & module type Fixed code	read only read only read only
Base + %16 Base + %14 Base + %12 Base + %10 Base + %0C Base + %08 Base + %06 Base + %04 Base + %02 Base + %00	Test pattern channel 1 Test pattern channel 0 Word count channel 1 Word count channel 0 FIFO channel 1 FIFO channel 0 Module clear Number of channels Status Register Interrupt Register	write only write only read only read only read only read only write only read/write read/write write only

Table 3.1: Address Map

3.3. MODULE IDENTIFIER WORDS

(Base address + %FA, + %FC, + %FE, read only)

Three words located at the address Base + %FA,+ %FC, + %FE of the page are used to identify the module, as shown in figure 3.2:

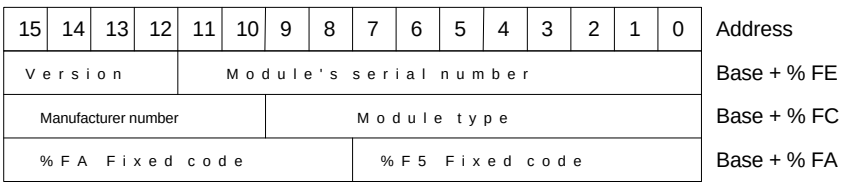

Fig. 3.2: Module Identifier Words

At the address Base + %FA the two particular bytes allow the automatic localization of the module.
For the Mod. V550 the word at address Base + %FC has the following configuration:

Manufacturer N°= 000010 b
Type of module= 00000110100 b

The word located at the address Base + %FE identifies the single module via a serial number, and any change in the hardware (for example the use of faster Conversion Logic) will be shown by the Version number.

3.4. TEST PATTERN REGISTERS

(Base address + %16, write only channel 1)
(Base address + %14, write only channel 0)

The Test Pattern registers have the following structure:

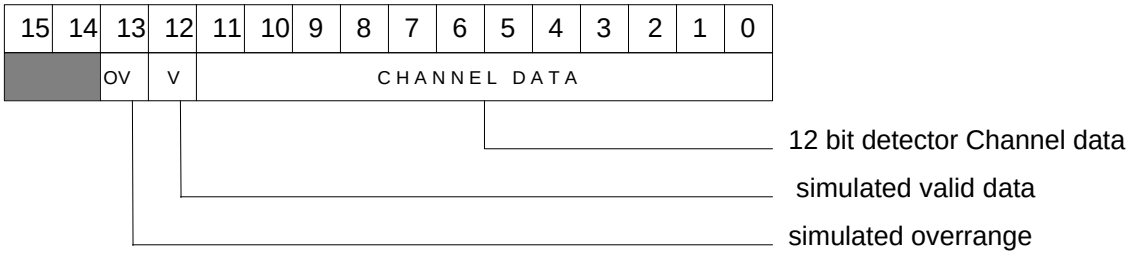

Fig. 3.3: Test Pattern Register

3.5. WORD COUNTER REGISTERS

(Base address + %12, read only channel 1)
(Base address + %10, read only channel 0)

The Word counter registers have the following structure:

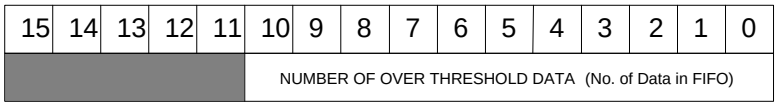

Fig. 3.4: Word Counter Register

3.6. FIFO CHANNEL 0 AND 1

(Base address + %0C, read only channel 1)
(Base address + %08, read only channel 0)

The FIFO data have the following structure:

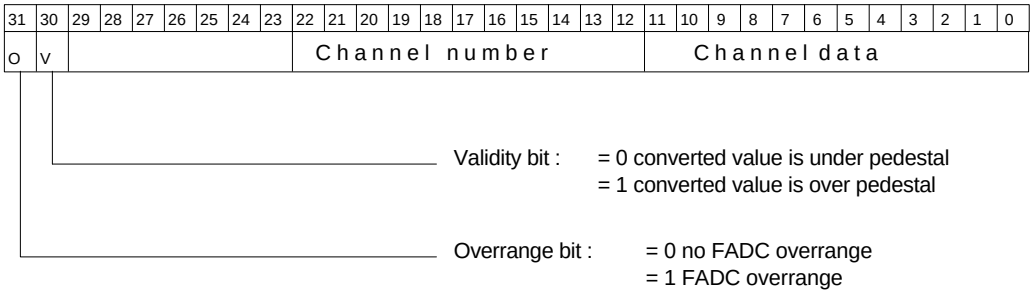

Fig. 3.5: FIFO structure

The two FIFOs are also accessible in block transfer mode.

3.7. CLEAR MODULE

(Base address + %06, write only)

A VME write access to this location causes the following:

- Aborts the conversion process (if active);
- clears the FIFOs;
- clears the word counters.

3.8. NUMBER OF CHANNELS

(Base address + %04, read/write)

This register allows to program the number of detector channels to be read out in step of 32.

This number ranges from 32 (DCN=1) to 2016 (DCN=63), DCN=0 means 1 detector channel only.

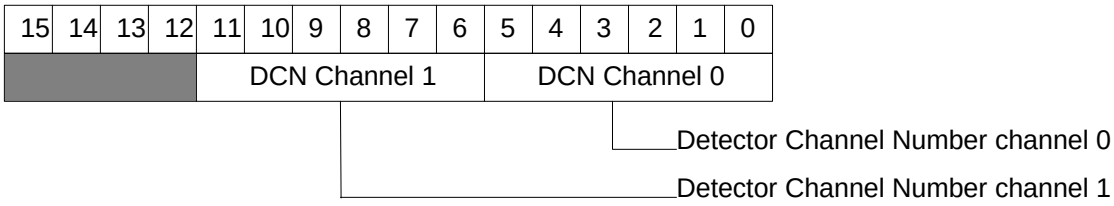

Fig. 3.6: Number of channels

3.9. STATUS REGISTER

(Base address + %02, read/write)

Contains information on the status and allows a few settings on the module.

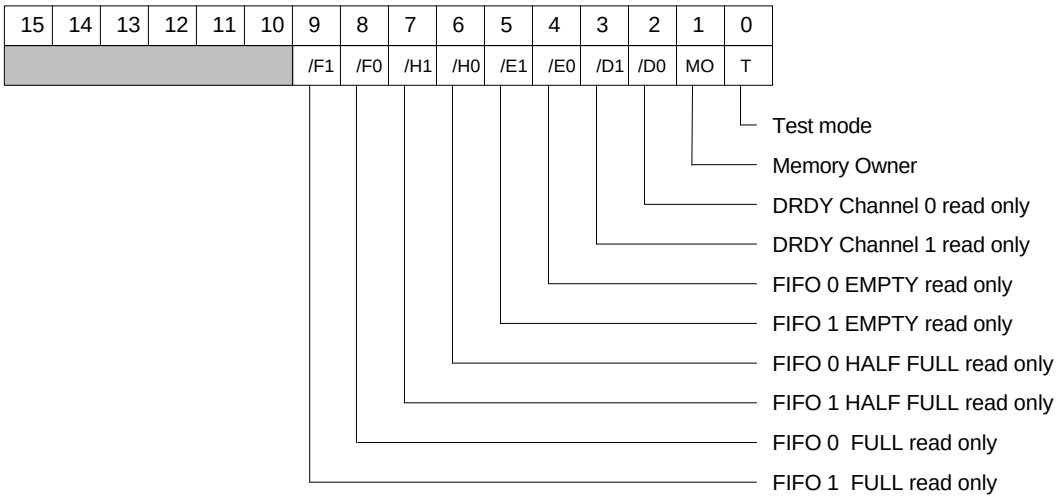

Fig. 3.7: Status Register

T Test mode.
= 0 no Test mode;
= 1 Test mode;

MO Pedestal Threshold memory owner.
= 0 memory owned by VME;
= 1 memory owned by the Conversion logic;

/D0 Channel 0 Data Ready bit, read only.
= 0 data ready;

/D1 Channel 1 Data Ready bit, read only.
= 0 data ready;

/E0 FIFO channel 0 empty bit, read only.
= 0 empty;

/E1 FIFO channel 1 empty bit, read only.
= 0 empty;

/H0 FIFO CHANNEL 0 half full bit, read only.
= 0 half full;

/H1 FIFO CHANNEL 1 half full bit, read only.
= 0 half full;

/F0 FIFO CHANNEL 0 full bit, read only.
= 0 full;

/F1 FIFO CHANNEL 1 full bit, read only.
= 0 full;

3.10. INTERRUPT REGISTER

(Base address + %0, write only)

This register contains the value of the Interrupt Level and the STATUS/ID that the V550 INTERRUPTER places on the VME data bus during the Interrupt Acknowledge cycle.

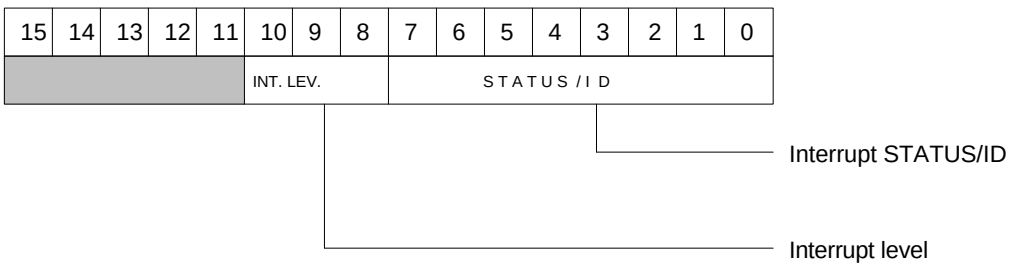

Fig. 3.8: Interrupt Register

3.11. PEDESTAL AND THRESHOLD MEMORIES

(Base address + %2000..5FFE, read/write)

These memories are accessible via VME only if the Memory owner bit is set to 0 (default mode).

They have the following structure:

CHANNEL 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	ADDRESS
								Pedestal detector channel 0												Threshold detector channel 0												Base + % 2000
								Pedestal detector channel 1												Threshold detector channel 1												Base + % 2004
								Pedestal detector channel 2047												Threshold detector channel 2047												Base + % 3FFC

CHANNEL 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	ADDRESS
								Pedestal detector channel 0												Threshold detector channel 0												Base + % 4000
								Pedestal detector channel 1												Threshold detector channel 1												Base + % 4004
								Pedestal detector channel 2047												Threshold detector channel 2047												Base + % 5FFC

Fig. 3.9: Pedestal/Threshold memories

The memories size is 2048 words but only 2016 are actually used by the conversion logic (2016 is the maximum number of channels).

4. OPERATING MODES

4.1. CONNECTION SCHEMES

(refer to fig. 4.1)

The Model V551B CAEN C-RAMS Sequencer has been designed in order to control more C-RAMS (CAEN Readout for Analog Multiplexed Signals) Mod. V550 in single acquisition systems. When a Mod. V551B C-RAMS Sequencer controls more than one V550 channel, the CONVERT signal is the same for each channel, so that each multiplexer is controlled by a single CLOCK.
Some connections must be made among the C-RAMS modules and the Sequencer module to let them work properly: the V551B CONVERT and CLEAR OUT signals must be distributed towards the C-RAMS acquisition cards and the V550 and V551B DATA READY signals must be connected together to perform a wired-OR. All this involves the use of a large number of 50 Ω cables, especially if there are a lot of V550 modules to be controlled; the Sequencer uses the P1 and P2 VME connectors and optionally the auxiliary connector for the CERN V430 VMEbus crate (Jaux Dataway), thus, if the VME auxiliary bus is available, it is possible to send via backplane the CONVERT, CLEAR OUT and DRDY signals and all these connections can be avoided.

4.1.1. USING MOD. V550 AND V551B WITH JAUX DATAWAY

By means of DIP switches, either on the V550 boards or V551B board, it is possible to enable the Jaux Dataway (see § 2.3), so that:
1.) The CONVERT signal coming from the V551B module is distributed to the V550 channels.

2.) The CLEAR signal coming from the V551B module is distributed to the V550 channels.

3.) The wired-OR of the V550 DATA READY signals is performed and received by the V551B.

If on the backplane there is no termination on the CK, CK*, CL and CL* auxiliary VME bus lines, it is possible to insert it on the last C-RAMS module. For this purpose, on the V550 board, it is possible to install a removable termination package (50 Ω to V_{TT}) for the CLEAR and CONVERT signals termination. As the DATA READY signal is TTL, if there is a termination on the SG auxiliary VMEbus line, it must be removed from the backplane.

N.B.: With the layout shown in Fig. 4.1, it is convenient to set the -5 V power supply selection jumper to AUX. This allows to reduce the power consumption on the -12 V power supply.

4.1.2. USING MOD. V550 AND V551B WITHOUT JAUX DATAWAY

If the auxiliary VME bus is not available or you don't want to use it (in this case the Jaux Dataway DIP switches must be disabled), the following connections must be made:

-Convert signal:

CONV(V551B) → CONV(V550) → CONV(V550) .... → CONV(V550) → 50 Ω termination.

-Clear signal:

CLOUT(V551B) → CLEAR(C550) → CLEAR(V550) ... → CLEAR(V550) → 50 Ω termination.

-Data Ready signal:

DRDY(V550) → DRDY(V550) .... → DRDY(V550) → DRDY(V551B) → 50 Ω termination.

N.B.: Without the V430 crate, the -5 V power supply selection jumper must be set to VEE. This allows to obtain the -5 V from the -12 V power supply.

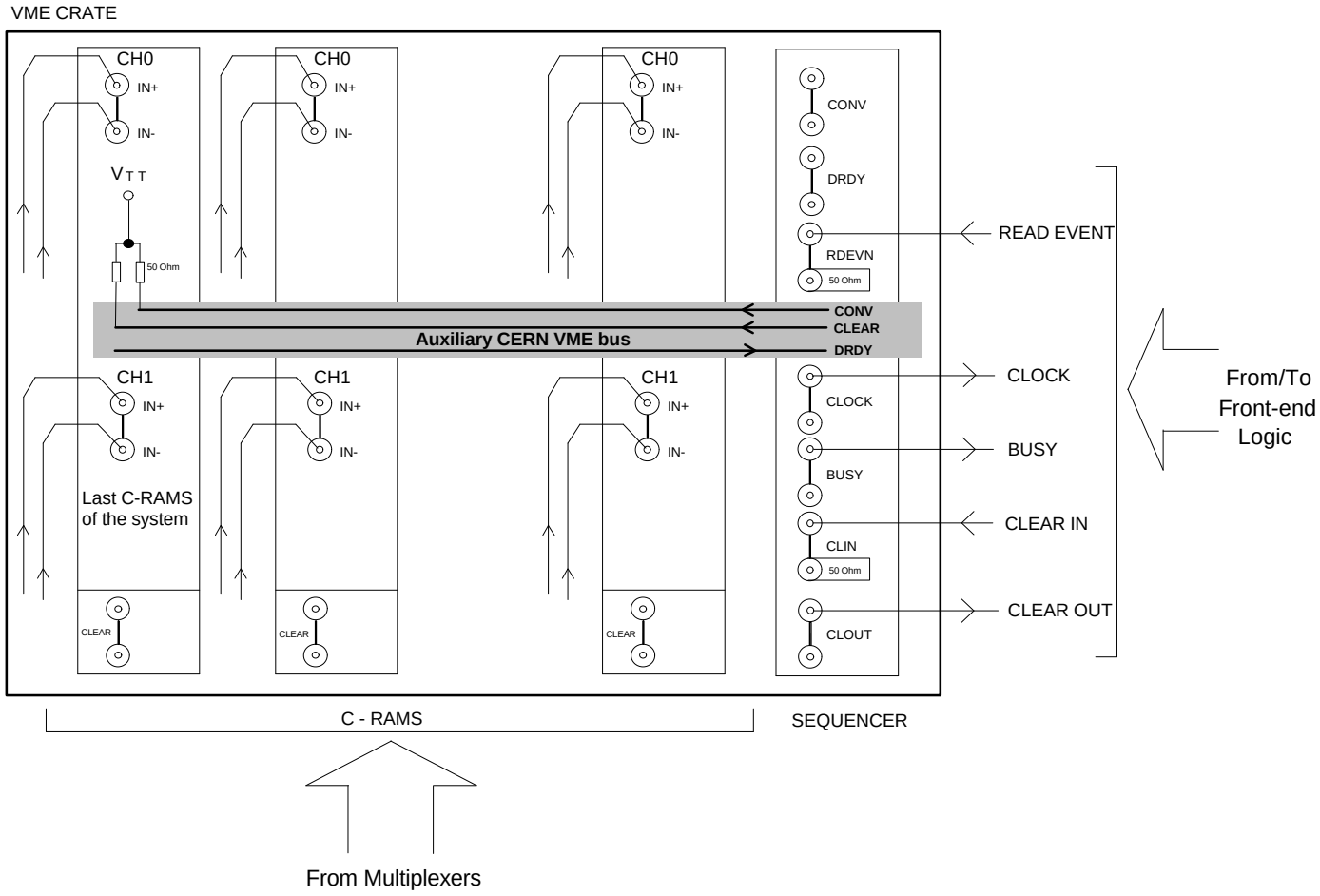

Fig. 4.1: System Layout with connections via Auxiliary VME bus.

4.2. OPERATION SEQUENCE

Each channel of the unit accepts 2 analog signals via front panel connectors. The difference between the two signals is amplified and fed to the FADC. The sensitivity (mV/bit) can be selected among 4 different values (with relative ratios of 1, 2, 5 and 10) by means of internal jumpers (see § 2.3).

The channel needs an external CONVERT pulse whose leading edge indicates that the analog signal must be sampled. This signal (ECL level) can be provided via the pins CK and CK* of the Jaux backplane connector of the V430 VME crate, or via front panel (NIM level, 2 bridged connectors for daisy chaining).

The number N of detector channels (between 32 and 2016) can be programmed via VME. In addition, the pedestal/threshold memory must be filled via VME with the chosen values. This memory can be accessed by VME only when the acquisition is stopped and the switching can be performed by means of the CONTROL REGISTER.

With the occurrence of the leading edge of the CONVERT signal the analog signal is sampled by the FADC ad its digital value is compared to the threshold of the current channel. If the channel is over threshold, the pedestal is subtracted and the result is stored in the FIFO. The word in the FIFO has the following format:

d<31>	**d<30>**	**d<29..23>**	**d<22..12>**	**d<11..0>**
Overrange	Data Valid	Reserved	Channel #	Channel pulse height

The D31 bit indicates a FADC overrange, while the D30 bit indicates that the field PULSE HEIGHT is valid (positive value after pedestal subtraction). The bits from D23 to D29 are not specified.
After N CONVERT pulses the data readout of an event is over. When the last CONVERT pulse has been processed and the FIFO is not empty, the card channel goes in DATA READY state, signaling that the data must be read. The DATA READY state is signaled by the following:

- a bit of the status word (DRDY).
- a positive open collector signal DRDY supplied via 2 front panel bridged connectors (for daisy chaining) or via the SG pin of the Jaux backplane connector of the V430 VME crate.

The daisy chain connection performs the wired-OR of the DRDY signals of different channels. When a channel is in DATA READY state the signal CONVERT has no effect on the card. After the last VME read from the FIFO, the DRDY signal goes low and the channel is ready for other acquisitions.

The readout from the FIFO can be performed in the following ways:

1) random VME read for each FIFO.

2) block transfer for each FIFO. For this mode a word counter for each FIFO is available, in order to know the number of word stored in FIFO.

The beginning of the reading phase is triggered in the following ways:

- by software polling of the DRDY bits.
- by interrupt raised by the card on the condition that at least one of the DRDY of the 2 channels goes high.

- by interrupt raised by the control card (V551B) on the condition that the wired-OR of the DRDY signals goes high.

The system housed in a single crate (one VME CPU, one control card and M acquisition cards) can handle up to 4032*M detector channels.

A general RESET can be performed via VME or by means of an external pulse. The CLEAR signal (ECL level) can be provided via the pins CL and CL* of the Jaux backplane connector of the V430 VME crate, or via front panel connector (2 per module, bridged for daisy chaining, NIM level). The CLEAR can be used as FAST CLEAR to reject the current event. In this case the CLEAR is sent when the acquisition is active: this causes the FIFO to be cleared and the logic circuitry reset.

4.3. THRESHOLDS AND PEDESTALS

The module can be used to calculate the values of the thresholds and the pedestals. For this purpose the threshold/pedestal memory must be filled via VME by zero. In this way the zero suppression and pedestal subtraction functions are disabled and the words written in the FIFO are the true converted values.

The readout is performed in the ways as already described above; the VME CPU can compute the mean values and the variances that can be used to determine the thresholds and pedestals to be written back into the threshold/pedestal memory.

This memory has the following format:

address	bit<0..11>	bit<12..23>
0	channel 0 threshold	channel 0 pedestal
n	channel n threshold	channel n pedestal
2047	channel 2047 threshold	channel 2047 pedestal

The Memory Owner bit (MO) of the status register is used to switch the pedestal & threshold memory access between the VME bus (MO=0) and the channels Control Logic.
At power_on, the memorized pedestal and threshold values are not specified, that's to say that the pedestal and threshold memory must be initialized by the user.

4.4. DIAGNOSTICS AND TEST

In addition to the normal operating mode, a TEST mode is available (selected via VME). In TEST MODE it is possible to simulate some input patterns as they were coming from the FADC. The 14 bit patterns (12 bit converted data, 1 bit overrange, 1 bit data valid) can be written via VME. The VME hand-shake protocol ensures that the rate does not exceed the maximum. In TEST MODE the CONVERT signal is ignored. Moreover, it is possible to read back via VME the threshold/pedestal memory, and the FIFO status flags (Empty, Half full, Full).

4.5. INTERRUPT GENERATION

The operations of the V550 VME RORA INTERRUPTER are fully programmable; via VME it is possible:

- to set the VME Interrupt level;
- to program the VME Interrupt Vector (STATUS/ID);

The interrupt is generated on the logical OR of the two DRDY signals (at least one channel has ended the programmed N conversion cycles and its FIFO is not empty) and released when the two DRDY signals are low (the two FIFOs have been completely read out).

REFERENCES

[1] VMEbus Specification Manual Revision C.1, October 1985.

[2] G. Bianchetti et al., "Specification for VMEbus CRATE Type V430", CERN-EP, January1990