



# CML Marine AIS

(Automatic Identification System)

## Product Information Pack

[Home](#)

[Introduction](#)

[System](#)

[CMX910](#)

[CMX7032/42](#)

[Promotion](#)

[Resources](#)



# Marine AIS – Automatic Information System

## Introduction

The Automatic Identification System (AIS) as specified by the International Marine Organisation (IMO), is a ship and shore based broadcast system, operating in the VHF maritime band.

A radio aid to navigation and safety, an AIS transponder repetitively broadcasts its host vessel's positional and status information. This enables other similarly equipped vessels in the vicinity to receive, decode and display that information, along with information from other navigational systems (radar, GPS, depth recorders), to provide a comprehensive picture of the maritime traffic in the local area.

Using the transfer of formatted wireless-data, an AIS system employs two simultaneous Rx channels and a single frequency-switched Tx channel. AIS transactions employ GMSK modulation with a back-up DSC channel using FSK modulation for system control and management.

An AIS network normally operates in an autonomous continuous mode and adapts to transponders moving into and out of range. Using Self Organising Time Division Multiple Access (SOTDMA) technology, AIS messages occupy over-air time slots that are accurately synchronized to either a GNSS or a local timebase. An AIS network can handle over 2000 reports per minute using individual 26.6ms time slots. Each network determines its own transmission schedule based upon data-link traffic history and knowledge of future actions by other stations.

AIS Class A was originally conceived for Safety Of Life At Sea (SOLAS) and large ships. Today AIS Class A carriage is mandatory on all SOLAS class vessels.



# Marine AIS – Automatic Information System

## Introduction (continued)

AIS Class B specification is now released and is a simplified version of the AIS Class A specification. AIS Class B specifies the use of Carrier Sensing TDMA (CSTDMA) to resolve whether and when to transmit. The carrier sensing enables a listen-before-transmit methodology and allows Class A and Class B devices to co-exist whilst giving Class A devices priority. AIS Class B opens up a completely new, potentially large market of smaller vessels, including the leisure craft market.

The Rx-only market is another potentially large market currently in its infancy. Low cost receivers can provide location information of larger vessels on displays and chart plotters. This enables accurate automatic collision avoidance systems to be implemented down to leisure craft level. Rx-only devices also serve on-shore hobbyists who only track craft activity.

Aids To Navigation (AToN) buoys indicating shipping hazards and traffic channels are generally anchored to a fixed position near the hazard but installing them can be difficult and the hazard can shift and require the buoy to be moved. A shifted hazard presents risk to craft until its marking buoy is moved.

AIS can eliminate the difficulty of physically placing and moving buoys by allowing a transponder in a fixed location, even on shore, to emulate an AIS AToN buoy at the hazard location. The AIS AToN emulated location can also be remotely updated so buoys need not be moved when hazards shift. Remote updating is very quick and so reduces risk compared to physically relocating a buoy.

AIS SART/EPIRB standards are emerging to take advantage of the AIS real time pin-point positioning to personal safety at sea.







# Marine AIS

## System Introduction

[Home](#)[Introduction](#)[System](#)[CMX910](#)[CMX7032/42](#)[Promotion](#)[Resources](#)

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COMMUNICATION SEMICONDUCTORS

Slide 4

## Marine AIS System Overview

# SOLAS: The driving factor

- ❖ AIS allows vessels and base stations to communicate their position and other data to each other without the need for a centralised controller or base stations.
- ❖ This allows vessels to “see” each other and take appropriate action to avoid collisions and so improve marine safety.
- ❖ The system uses a GMSK 9600 baud data link in the Marine VHF frequency band.
- ❖ The system requirements are defined in ITU-M 1371-1 standard.
- ❖ AIS was originally defined for SOLAS (Safety Of Life At Sea) vessels and large ships but it is also applied to security applications.
- ❖ Mandatory use by international treaty on SOLAS vessels and other large ships above a specified tonnage
- ❖ Local regulations may apply to smaller vessels
- ❖ International standards apply
- ❖ The safety/security aspect is driving the use into smaller vessels and ultimately down to leisure-craft level

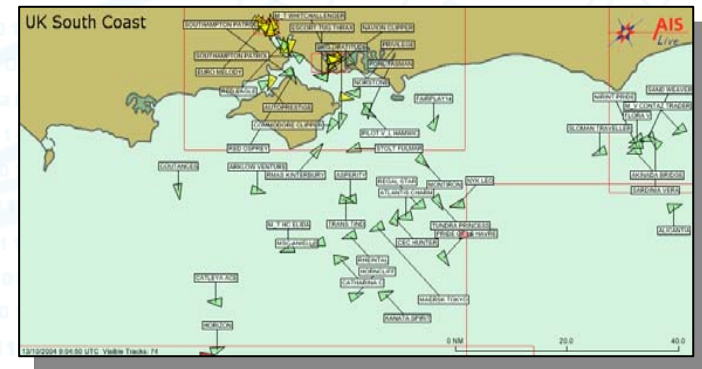




## Marine AIS System Overview

# AIS (Automatic Identification System)

- ❖ Wireless real time network that identifies ships, their location, heading, status and other info, even when out of sight
- ❖ Aids navigation, collision avoidance and support for traffic management and surveillance systems
- ❖ GNSS receiver provides location etc. for the AIS terminal
- ❖ Two standards are fully released: AIS Class A and AIS Class B
- ❖ Gives more detailed information that complements radar
- ❖ Compatible with common graphic and text displays
- ❖ Self synchronising TDMA air link
- ❖ Operates autonomously
- ❖ AToN (Aids To Navigation) standard will also be available soon



# Marine AIS System Overview

## AIS class A

- ❖ Mandatory on SOLAS and other large vessels
- ❖ Uses SOTDMA (Self Organising Time Division Multiple Access)
- ❖ Requires 3 parallel receivers and one transmitter
  - Rx - Two AIS 9600baud GMSK and one DSC 1200baud FSK
  - Tx - Single Tx switches between AIS channels 1 and 2
- ❖ Relays detailed vessel location and status information
- ❖ Transmission rate varies with vessel speed – every 10 seconds <14 knots
- ❖ High performance requirements
  - Higher Tx power
  - Longer range
  - Faster data update rate





# Marine AIS System Overview

## AIS class B

- ❖ AIS Class B is not currently mandatory but moving in this direction due to the safety/security advantages
- ❖ Uses CSTDMA (Carrier Sensing Time Division Multiple Access)
  - SOTDMA variety of the standard is scheduled for release
- ❖ Requires two parallel receivers and one transmitter
  - Rx - One for AIS 9600 baud GMSK, the other shared by AIS 9600 baud GMSK and DSC 1200 baud FSK Rx
  - Tx – Single Tx switching between AIS channel 1 and 2
- ❖ Vessel location and minimal status information relayed
- ❖ Reporting rate every 30 seconds <14 knots
- ❖ Market drivers against AIS Class A
  - Lower cost
  - Smaller size
  - Lower power consumption
  - Reduced design complexity
  - Larger potential market size

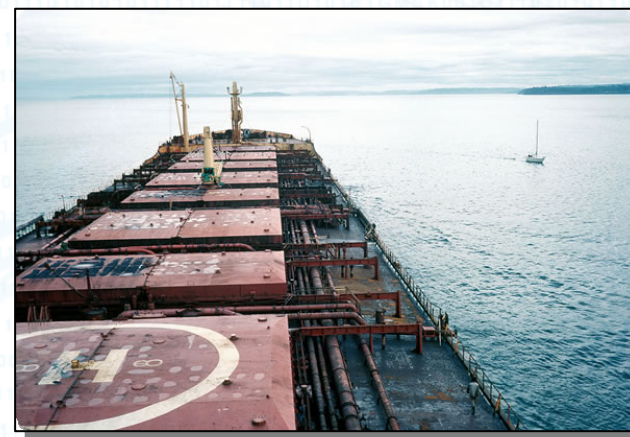




## Marine AIS System Overview

# AIS Rx only units

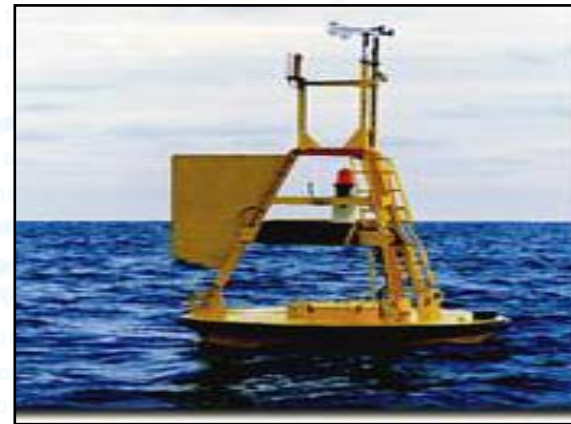
- ❖ Large market potential
- ❖ Ideally suited to the leisure craft and hobby markets
- ❖ Not constrained by AIS class (A and B)
- ❖ Window of opportunity prior to Class B being mandatory
- ❖ Requires only Rx channel reception
  - Rx – Single or dual Rx AIS 9600 baud GMSK
- ❖ Market drivers
  - Very low cost
  - Small size
  - Lower power consumption
  - Reduced design complexity
  - Very large potential market size



## Marine AIS System Overview

# AIS AToN (Aids To Navigation)

- ❖ AIS Tx only application
- ❖ Transmitting exact position of a bouy
- ❖ Market drivers
  - Very low cost
  - Small size
  - Lower power consumption
  - Reduced design complexity

[Home](#)[Introduction](#)[System](#)[CMX910](#)[CMX7032/42](#)[Promotion](#)[Resources](#)

Slide 10



# Marine AIS System Overview

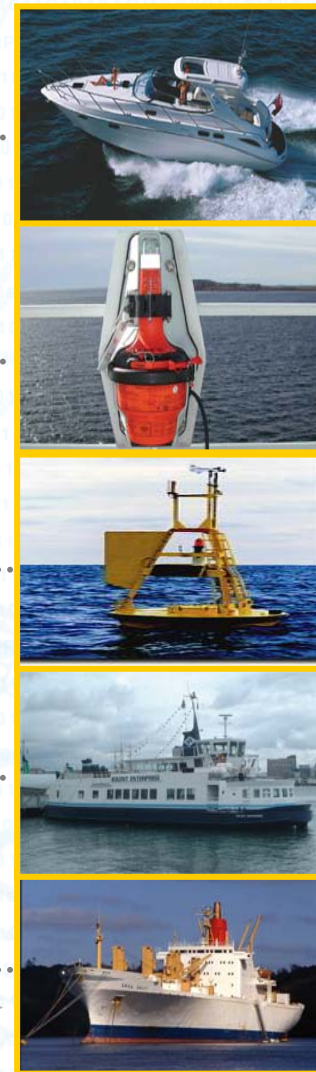
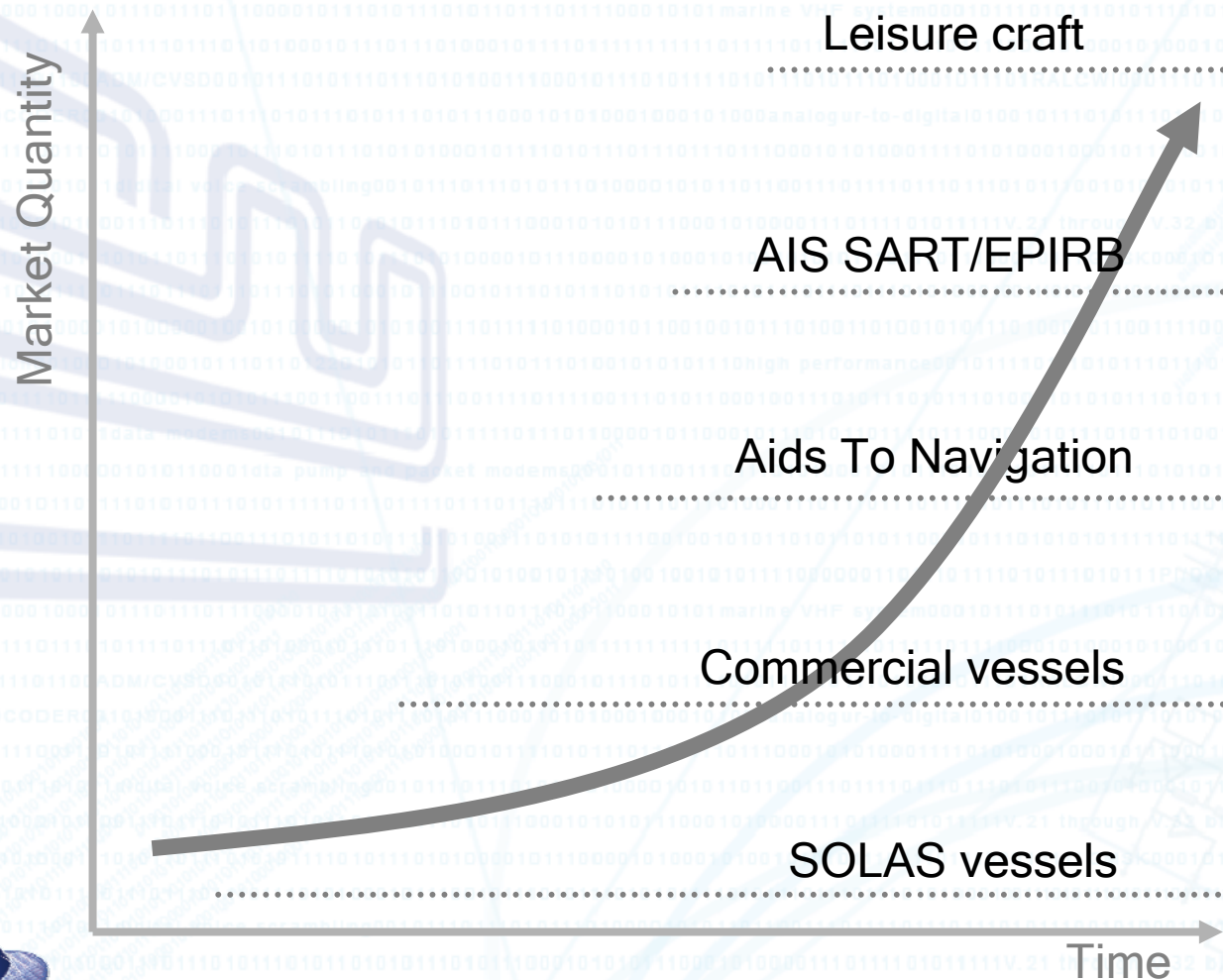
## AIS SART/EPIRB

- ❖ Emerging standards for AIS SART and AIS EPIRB
- ❖ AIS SART
  - Search and Rescue Transponder
  - AIS signal is used to pin-point its position to local crafts or emergency services
- ❖ AIS EPIRB
  - Emergency Position Indicating Radio Beacon
  - An extra radio beacon is included to signal its position to satellites to alert the emergency services
  - Also includes an AIS SART function to direct emergency services when they are in AIS range



# Marine AIS System Overview

## Market evolution/growth



[Home](#)

[Introduction](#)

[System](#)

[CMX910](#)

[CMX7032/42](#)

[Promotion](#)

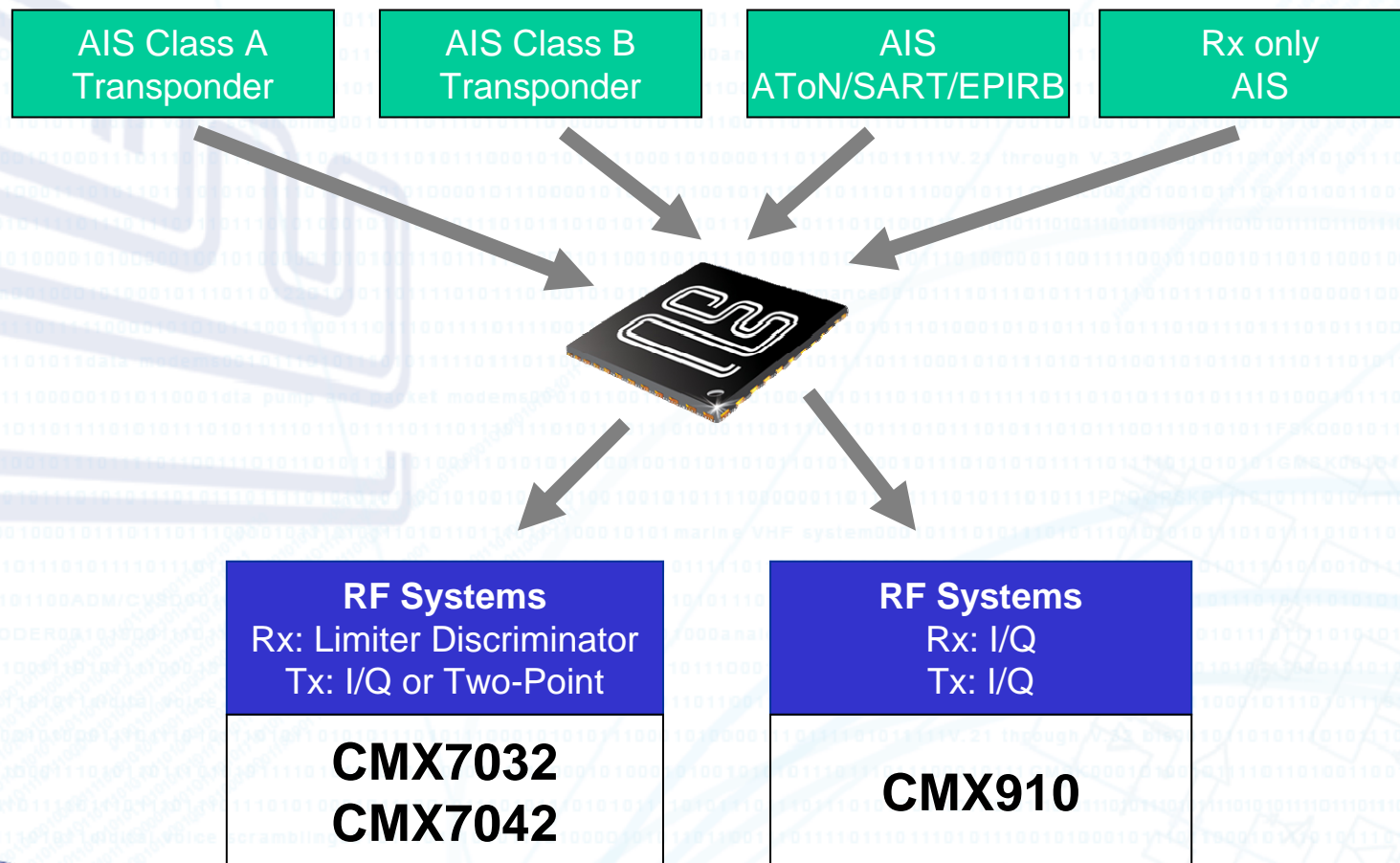
[Resources](#)

Slide 12



## Marine AIS System Overview

# CML's AIS processors

[Home](#)[Introduction](#)[System](#)[CMX910](#)[CMX7032/42](#)[Promotion](#)[Resources](#)

# CML's AIS Processors

## Product Summary

AIS IC Product Selector			
	CMX910	CMX7032	CMX7042
Modulation	GMSK and FSK	GMSK and FSK	GMSK and FSK
AIS Support	A and B	B	B
On-Chip AIS Data Handling Modes	AIS Burst and Raw	AIS Burst and Raw	AIS Burst and Raw
On-chip AIS Data Formatting	HDLC and NRZI	HDLC and NRZI	HDLC and NRZI
AIS Signal Timing	Slot and Sample	Sample	Sample
Peripheral Timing	Sequenced, timed control of external circuits	2 x System Clocks	2 x System Clocks
Rx Modes	AIS and DSC	AIS and DSC	AIS and DSC
Tx Modes	AIS and DSC	AIS	AIS
RF Channel Bandwidth	12.5 and 25 kHz	25kHz	25kHz
Rx Interface	I and Q	Differential Limiter-Discriminator	Differential Limiter-Discriminator
Tx Interface	I and Q	Two-Point Modulation I and Q	Two-Point Modulation I and Q
Auxiliary ADCs and DACs	5 x 10-bit (Mux) ADCs 5 x 10-bit DACs	4 x 10-bit (Mux) ADCs 4 x 10-bit DACs	4 x 10-bit (Mux) ADCs 4 x 10-bit DACs
Auxiliary System Clocks	None	2 x System Clocks	2 x System Clocks
RF Synthesisers	None	2 x Individual (100 to 600 MHz)	None
Control Interface	C-BUS and Expansion Port	C-BUS	C-BUS
AIS System Format Compatibility	SOTDMA CSTDMA	SOTDMA CSTDMA	SOTDMA CSTDMA
Device Configuration via:	Configuration File	Function Image™	Function Image™
Supply Requirements	3.0 to 3.6 V		
Packages	64-lead LQFP (L9) 64-lead VQFN (Q1)	64-lead LQFP (L9) 64-lead VQFN (Q1)	48-lead LQFP (L4) 48-lead VQFN (Q3)
Evaluation	EV9100 EvKit	PE0201 EvKit PE0001 Interface Card	PE0401 EvKit PE0001 Interface Card


[Home](#)
[Introduction](#)
[System](#)
[CMX910](#)
[CMX7032/42](#)
[Promotion](#)
[Resources](#)



# CMX910 and CMX7032/CMX7042 AIS Processors

## The CML edge

- ❖ Reduced component count – removing
  - Up to 3 DSPs
  - DSP Memory (SDRAM, Flash)
  - 2 ADC for Rx Channels
  - 1 DAC for Tx
- ❖ No “Glue Logic” and/or FPGA required for serial bus expansion and connection of multiple ADC/DAC/DSP
  - Auxiliary ADC and DAC
  - Op-amps to drive RF and monitoring circuits
  - PA Ramping generation / control
  - Reduced RF filtering (CMX910)
- ❖ Only requires a low cost, low speed host microcontroller
- ❖ I/Q and limiter discriminator based products
- ❖ Reduces system:
  - Cost and size
  - Supply current
  - Design time and risk
- ❖ RF system demonstrator and design support available

[Home](#)[Introduction](#)[System](#)[CMX910](#)[CMX7032/42](#)[Promotion](#)[Resources](#)

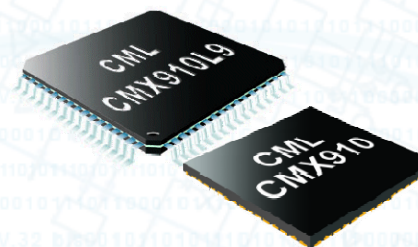
Slide 15



# CMX910

AIS processor for I/Q based systems

## Product Summary



[Home](#)

[Introduction](#)

[System](#)

[CMX910](#)

[CMX7032/42](#)

[Promotion](#)

[Resources](#)

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## CMX910 AIS Processor with I/Q Interface

# Product features

- ❖ I/Q radio interface
- ❖ Half-Duplex GMSK, FSK and DSC capabilities
- ❖ Flexible signal channels
  - Two Simultaneous Rx
  - One Tx
  - Optional-FSK Interface
- ❖ AIS formatted and raw data modes
- ❖ Digital IF filter
- ❖ Slot/sample timer counter/sequencer with UTC timing interface
- ❖ High performance GMSK decoding
- ❖ Optimal co-channel and adjacent channel performance
- ❖ Supports both SOTDMA and CSTDMA operation
- ❖ C-BUS serial control interface

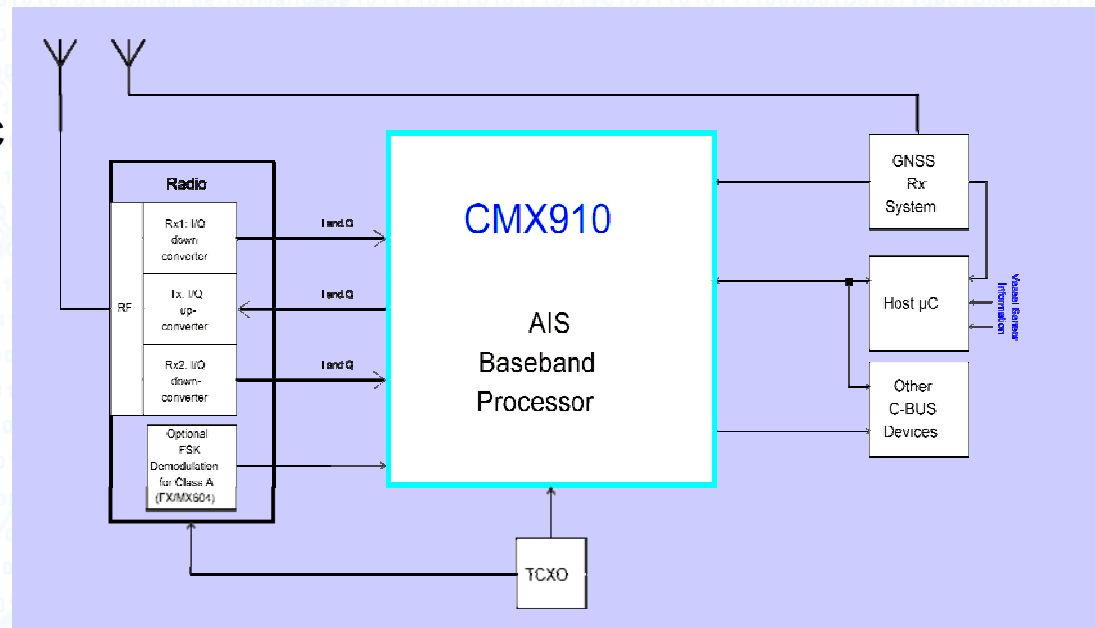




# CMX910 AIS Processor with I/Q Interface

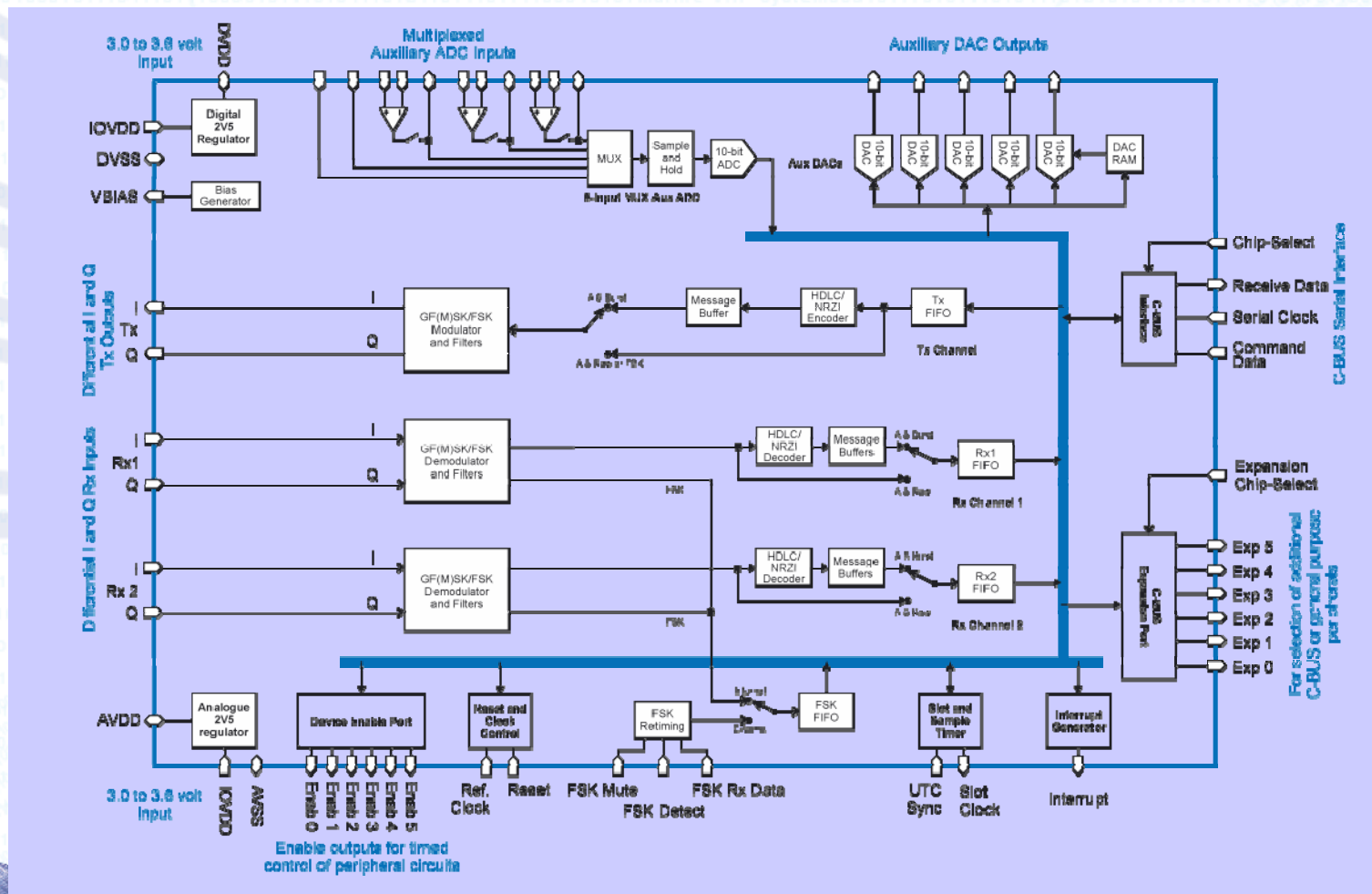
## Product features

- ❖ Serial bus expansion port
- ❖ RF device-enable facilities
- ❖ Small footprint VQFN and LQFP packages
- ❖ 'Sleep' and dynamic powersave
- ❖ Auxiliary ADC and DAC
  - 5 (10-bit) DACs
  - 5-Input MUX (10-bit) ADC
- ❖ Low-power 3.3 V operation
- ❖ PA Ramping function



# CMX910 AIS Processor with I/Q Interface

## Block diagram



Home

Introduction

System

CMX910

CMX7032/42

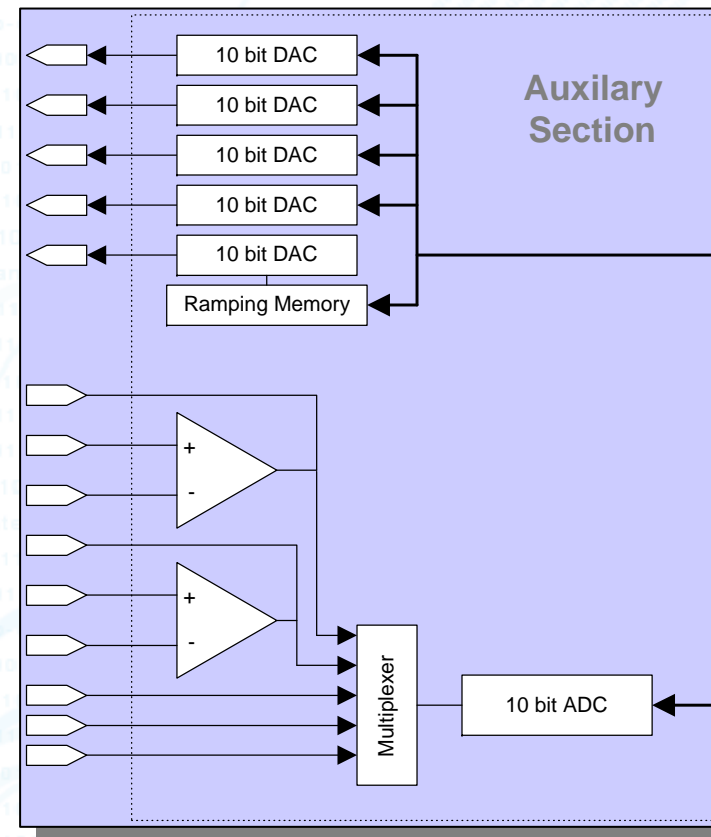
Promotion

Resources

## CMX910 AIS Processor with I/Q Interface

# Auxiliary ADCs and DACs

- ❖ Typical applications
- ❖ 5 channel multiplexed 10bit ADCs
  - Temperature
  - Battery voltage
  - Forward power
  - Reverse power
  - RSSI
- ❖ 5 channel 10bit DACs
  - AGC Rx1
  - AGC Rx2
  - PA ramp
  - PA bias
  - Front end Filter tuning

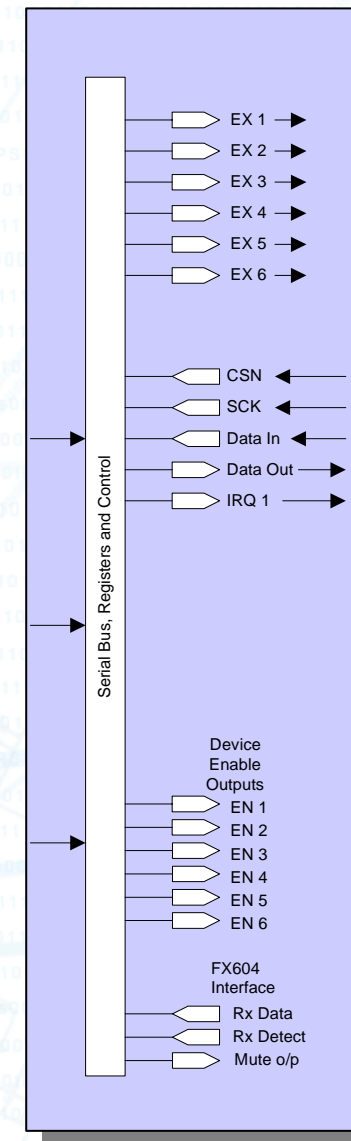




# CMX910 AIS Processor with I/Q Interface

## Expansion port

- ❖ Typical Applications
- ❖ Select outputs to enable peripherals
  - PLL Rx1
  - PLL Rx2
  - PLL Rx3
  - IQ receiver Rx1
  - IQ receiver Rx2
  - Tx PLL
- ❖ Timed enable outputs
  - RF
  - Rx1
  - Rx2
  - Rx3
  - Tx
  - PA



## CMX910 AIS Processor with I/Q Interface

# The I/Q advantage

- ❖ I/Q demodulators generally cost more than limiter discriminator ICs but the I/Q approach has the overall advantage:
- ❖ Accurate Tx modulation without using two point modulation
- ❖ High performance, phase linear, 2nd IF digital filters for both 12.5kHz and 25kHz modes are in the CMX910 to avoid using 'tricky' (and very expensive) external discrete filters
- ❖ Integrated carrier (slot busy) detect, needed for Class B CS-TDMA mode
- ❖ Supports both Tx and Rx for both AIS and DSC signal types
- ❖ CMX910 automatically trims for I and Q demodulator errors



## CMX910 AIS Processor with I/Q Interface

# The CMX910 advantage

- ❖ Utilising the CMX910 in an application simplifies the overall system design by eliminating:
  - Two AIS Rx data demodulators
  - One AIS Tx data modulator
  - One DSC Tx/Rx data modulator/demodulator
  - One or more 'busy'  $\mu$ Cs (low level AIS protocol engines)
  - The need for more than one RF reference oscillator
  - Tricky discrete AIS IF filters
  - Tricky Rx path calibration
  - Tricky balance of Tx two point modulation
  - A host of auxiliary ADCs and DACs
  - Fast PA power control DAC and its sequencer
  - The complexity of user developed hardware and software to reliably and accurately perform slot-timed actions





# CMX910 AIS Processor with I/Q Interface

## Deliverables

### ❖ Products

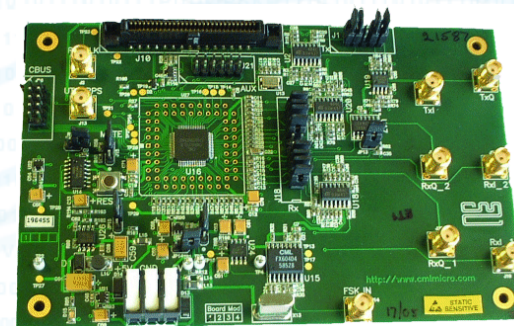
- CMX910 – Marine AIS processor with I and Q RF interface
  - CMX910Q1 – 64 pin VQFN package
  - CMX910L9 – 64 pin LQFP package

### ❖ Technical Data

- CML Website [www.cmlmicro.com](http://www.cmlmicro.com)
  - Product overview
  - Datasheet
  - 'Innovations'
- CML Technical Portal (MyCML)
  - Configuration file

### ❖ Evaluation Support

- EV9100 evaluation kit





# CMX7032

# CMX7042

**AIS processors for Limiter Discriminator based Rx RF systems**

## Product Summary



[Home](#)

[Introduction](#)

[System](#)

[CMX910](#)

[CMX7032/42](#)

[Promotion](#)

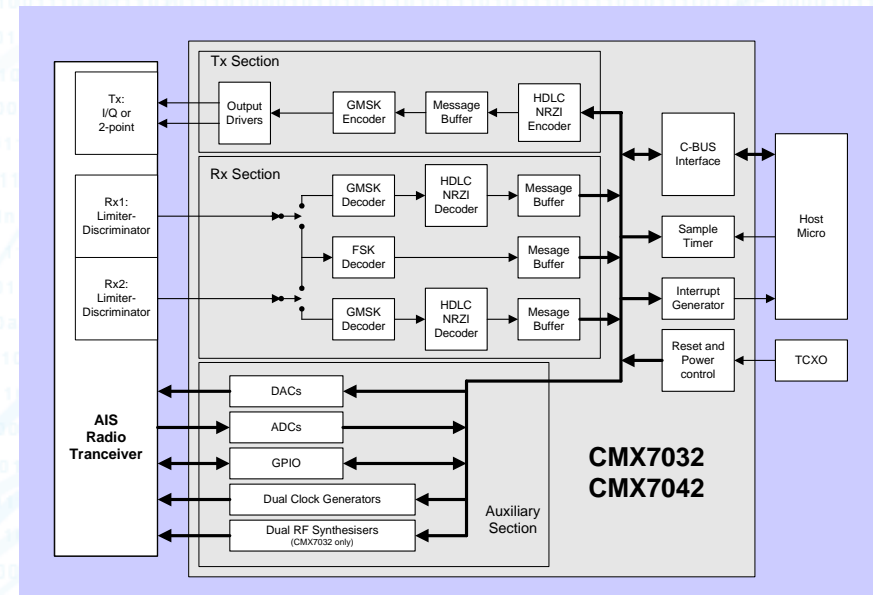
[Resources](#)



# CMX7032/CMX7042 Limiter Discriminator AIS Processors

## Product Features

- ❖ Designed for use in Class B AIS units utilising Limiter-Discriminator Rx RF systems
- ❖ The CMX7032 and CMX7042 have identical core functionality
  - CMX7032 provides maximum integration with the inclusion of two auxiliary RF synthesisers on chip.
  - CMX7042, without RF synthesisers, offers maximum RF system flexibility and the smallest foot-print package
- ❖ Half duplex in operation
  - Two parallel Rx paths Limiter-Discriminator
  - One AIS Tx path, I/Q or two-point modulation
- ❖ On-chip auxiliary functions for control and management of the RF section





# CMX7032/CMX7042 Limiter Discriminator AIS Processors

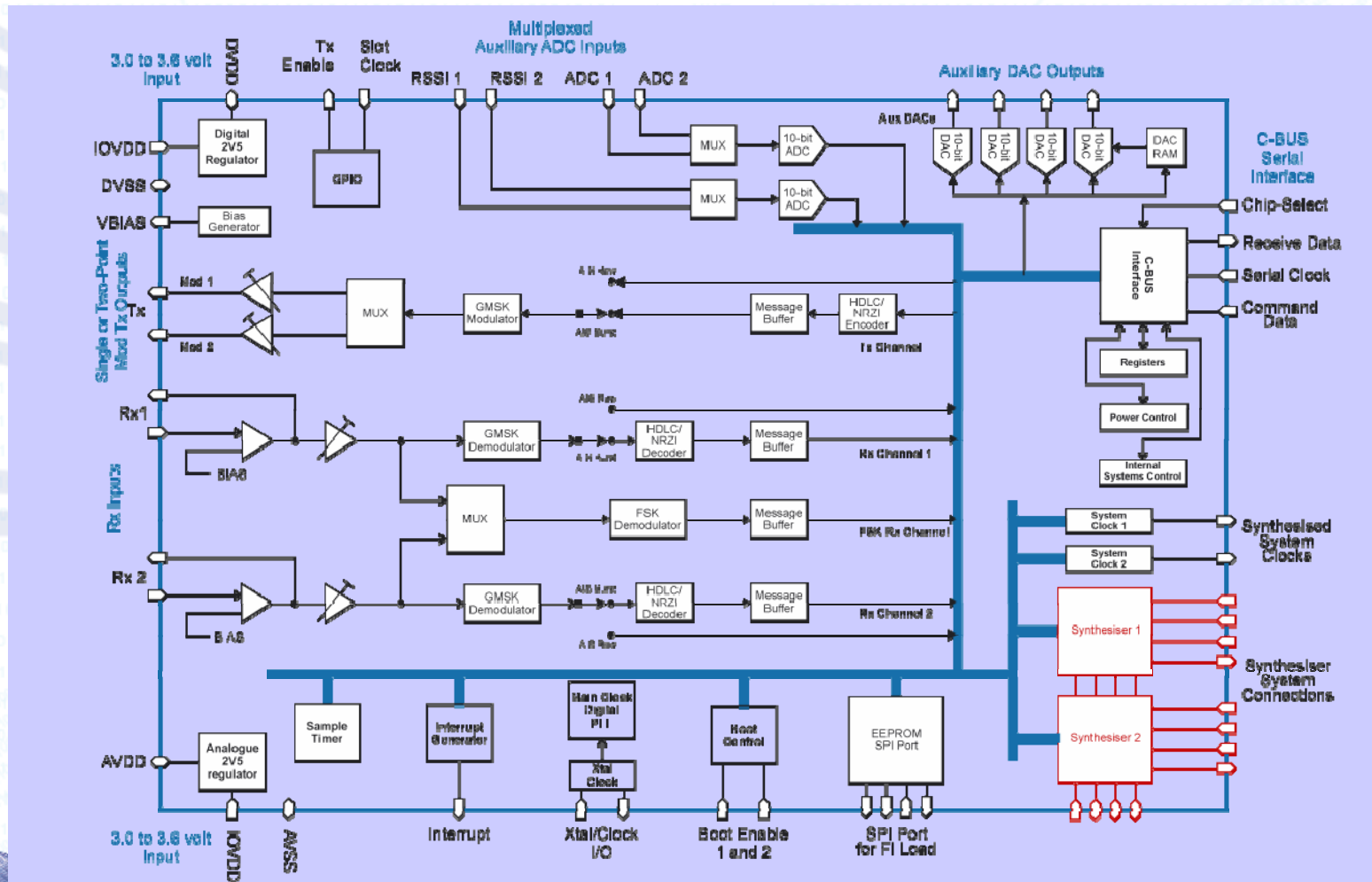
## Product Features

- ❖ Signal modulation/demodulation with associated AIS functions
  - Training sequence detection
  - NRZI conversion
  - HDLC processing (flags, bit stuffing/de-stuffing, CRC generation/checking)
- ❖ Integrated Tx/Rx data buffers reduce overall host  $\mu$ C processing requirements
- ❖ Auxiliary ADCs and DACs functions are provided to further simplify the system hardware design reducing the overall equipment size and cost
- ❖ Built on FirmASIC<sup>®</sup> Technology offering maximum flexibility and upgradeability
- ❖ C-BUS serial control interface



# CMX7032/CMX7042 Limiter Discriminator AIS Processors

## Block Diagram



Home

Introduction

System

CMX910

CMX7032/42

Promotion

Resources

# CMX7032/CMX7042 Limiter Discriminator AIS Processors

## Specification

- ❖ Limiter-discriminator Rx interface
- ❖ Half-Duplex GMSK AIS modem and DSC FSK demodulator
- ❖ Marine AIS Tx/Rx and DSC Rx data formatting
- ❖ Flexible channel configuration
  - Two simultaneous Rx
  - One Tx (two-point modulation or I/Q)
- ❖ Supports carrier-sensing channel access (CSTDMA)
- ❖ Optimal Co-channel performance
- ❖ Auxiliary functions
  - 4 x (10bit) DACs
  - 2 x (10bit) ADCs
  - 2 x RF synthesisers (CMX7032 only)
  - 2 x programmable system clock outputs
  - Tx enable output for external hardware
  - Slot clock input from host microcontroller
- ❖ Low-power 3.3V operation
- ❖ Low profile VQFN and LQFP package options





# CMX7032/CMX7042 Limiter Discriminator AIS Processors

## Function Image™ availability

	Marine AIS AIS Class B Transponder	Marine AIS AIS Rx Only	
Function Image™	7032/7042FI-1.x.x.x	7032/7042FI-2.x.x.x	
Basic Configuration	Half duplex operation <i>Dual Rx Channels Two-Point modulation Tx drivers C-BUS Interface</i>	Half duplex operation <i>Dual Rx Channels RS232 Interface</i>	
Core Systems	AIS class B operation in accordance with IEC62287	Complete autonomous dual channel receiver operation with NMEA interface	
Auxiliary Systems	DACs <i>Raised Cosine and Programmable ramp</i> ADCs <i>Spot reading Level thresholds Averaging modes</i> Clock PLL System Clocks GPIO	DACs <i>Raised Cosine and Programmable ramp</i> ADCs <i>Spot reading Level thresholds Averaging modes</i> Clock PLL System Clocks GPIO	


[Home](#)
[Introduction](#)
[System](#)
[CMX910](#)
[CMX7032/42](#)
[Promotion](#)
[Resources](#)

# CMX7032/CMX7042 Limiter Discriminator AIS Processors

## Target applications

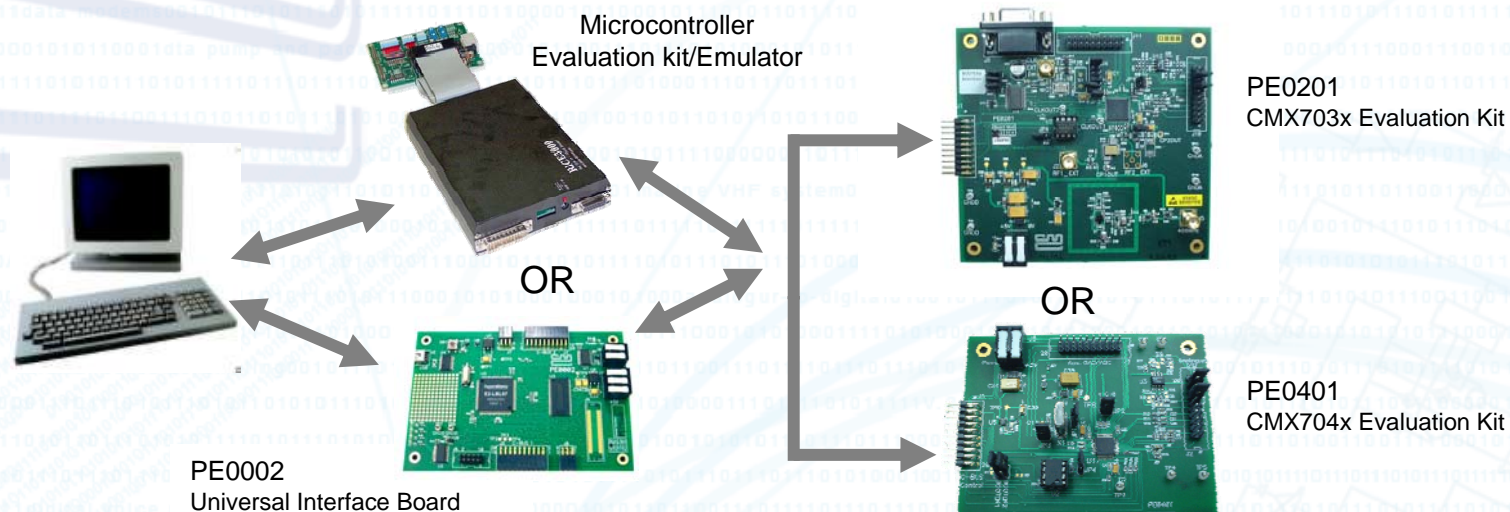
- ❖ Class B AIS systems based on a Limiter-Discriminator Rx RF interface
- ❖ AIS Class B transponders
- ❖ AIS Rx-only units
- ❖ AIS Tx-only modules
- ❖ AIS Aids-To-Navigation (AToN) systems
- ❖ AIS SART Beacons
- ❖ AIS EPIRB Beacons

[Home](#)[Introduction](#)[System](#)[CMX910](#)[CMX7032/42](#)[Promotion](#)[Resources](#)

# CMX7032/CMX7042 Limiter Discriminator AIS Processors

## Evaluation support

- ❖ PE0002 – Universal interface board
- ❖ GUI program from the CML Technical Portal (MyCML)
- ❖ PE0201 – CMX703x series – Evaluation board
- ❖ PE0401 – CMX704x series – Evaluation board

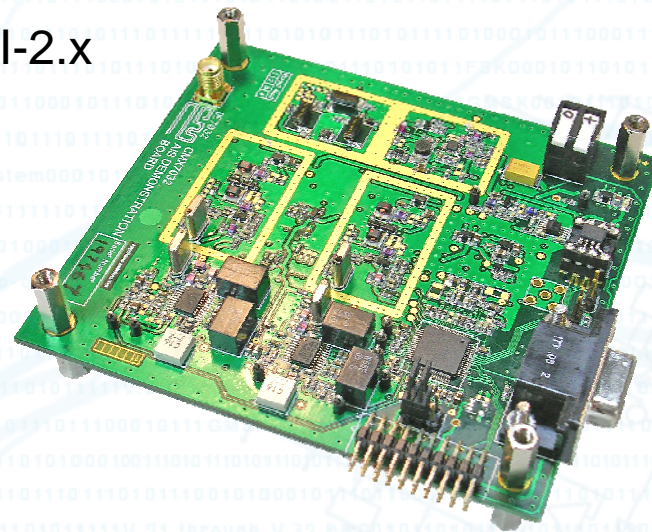




## Class B Transponder/Dual Channel Rx Only

# DE70321 demonstrator

- ❖ AIS class B transceiver demonstrator via 7032/7042FI-1.x
  - Designed to meet IEC62287
  - 2 W Tx operation
  - Serial bus (C-BUS) to host
  - Schematics and BOM available
- ❖ Dual channel AIS receiver via 7032FI-2.x
- ❖ Fully operational autonomous unit
- ❖ RS232 NMEA output



# CMX7032/CMX7042 Limiter Discriminator AIS Processors

## Deliverables

### ❖ Products

- CMX7032 – Marine AIS processor including two RF synthesisers
  - CMX7032Q1 – 64 pin VQFN package
  - CMX7032L9 – 64 pin LQFP package
- CMX7042 - Marine AIS data processor
  - CMX7042Q3 – 48 pin VQFN package
  - CMX7042L4 – 48 pin LQFP package

### ❖ Evaluation/Demonstration

- PE0201/PE0401/PE0002
- DE70321

### ❖ Technical Data

- CML Website [www.cmlmicro.com](http://www.cmlmicro.com)
  - Product overview
  - Datasheet
  - 'Innovations'
- CML Technical Portal (MyCML)
  - Combined User Manual and Datasheet
  - Function Image™ download
  - Application notes and FAQs

[Home](#)[Introduction](#)[System](#)[CMX910](#)[CMX7032/42](#)[Promotion](#)[Resources](#)



# CML Marine AIS Products Resources



Information on CML's website [www.cmlmicro.com](http://www.cmlmicro.com)

- Overview
- Datasheet
- Evaluation kit
- Register to download datasheets
- Sign up to get product update mailings



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Home

Introduction

System

CMX910

CMX7032/42

Promotion

Resources

