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MIP405

USERS MANUAL

MPL Industrial PC with IBM PowerPC™ Processor

The MIP405 is a highly integrated industrial single board computer in PC/104 form factor. Build around the PPC405 IBM PowerPC™ Processor it is well suited for applications requiring small size, high performance and Low Power. The MIP405 can be used in a standard operating environment without the necessity of a fan.

All major components required to build a industrial PC system are implemented on a single PC/104 sized board. It features two E-IDE, one 10/100Base TX Ethernet, two USB Ports, four serial ports, speaker output, and a real time clock. The 16-bit PC/104 and the PC/104+ (PCI) interface offers easy and flexible expansion capabilities.

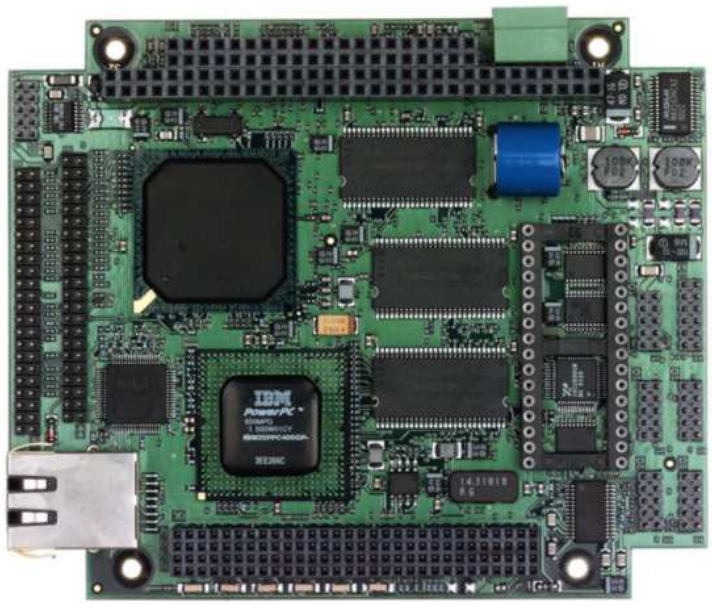
Integration of the MIP405 into a system is facilitated by the fact of offering standard connectors E-IDE (44 pin header) and LAN (2mm 12pin header or RJ45). The serial interfaces can be accessed through 2mm 10pin headers. Particular precaution has been taken to the EMC so that an entire system can fulfill the CE and FCC requirements.

The SDRAM is soldered on board and is available with ECC.

All these features make the MIP405 to the ideal solution for any low-cost embedded control application where a flexible industrial PC is needed.

Features

- Low Power IBM PPC405 Processor
- Processor clock 266 / 400 MHz
- Up to 128MByte ECC SDRAM on board.
- Integrated 10/100 Mbit/s Ethernet Controller
- PC/104 and PC/104 Plus interface
- 2 USB Ports
- Two EIDE HDD ports
- Four RS232 ports
- Low power consumption



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1. Introduction

1.1 About this manual

This manual assists the installation and initialization procedure by providing all hardware related information necessary to handle and configure the MIP405.
For all bootloader related information please refer to the “U-Boot User Manual for MPL SBC (MEH-10082-002)” supplied by MPL AG or your local MIP405 supplier. The U-Boot User Manual for MPL SBC” is also available on the internet under http://www.mpl.ch in PDF format.
The manual is written for technical personnel responsible for integrating the MIP405 into their system.

1.2 MIP405 Variants

Since the MIP405 is available in various population options, the information in this Manual about Memory size, Processor speed etc. may vary with your MIP405. The table below lists the actual (as of July 2003) variants, for an actual table please consult http://www.mpl.ch.

Variants	CPU	SDRAM	Flash	Ethernet	Temperature Range
MIP405-1	PPC405GP/266MHz	128MByte ECC	4MByte	RJ45	0°C ... 60°C
MIP405-2	PPC405GP/266MHz	64MByte ECC	4MByte	Header	-40°C ... 85°C
MIP405-3	PPC405GPr/400MHz	128MByte ECC	8MByte	Header	0°C ... 60°C
MIP405-4	PPC405GP/266MHz	128MByte ECC	4MByte	Header	0°C ... 60°C

Table 1.2.1 MIP405 Variants

Note: Not all of the variants may be available. Please consult for http://www.mpl.ch available variants.

1.3 Safety precautions and handling

For personal safety and safe operation of the MIP405, follow all safety procedures described here and in other sections of the manual.

- Power must be removed from the system before installing (or removing) the MIP405 to prevent the possibility of personal injury (electrical shock) and/or damage to the product.
- Handle the product carefully, i.e., dropping or mishandling the MIP405 can cause damage to assemblies and components.
- Do not expose the equipment to moisture.

WARNING

There are no user-serviceable components on the MIP405

1.4 Electrostatic discharge (ESD) protection

Various electrical components within the product are sensitive to static and electrostatic discharge (ESD). Even a non-sensible static discharge can be sufficient to destroy or degrade a component's operation!

1.5 Equipment safety

Great care is taken by MPL that all its products are thoroughly and rigorously tested before leaving the factory to ensure that they are fully operational and conform to specification. However, no matter how reliable a product, there is always the remote possibility that a defect may occur. The occurrence of a defect on this device may, under certain conditions, cause a defect to occur in adjoining and/or connected equipment. It is the user’s responsibility to ensure that adequate protection for such equipment is incorporated when installing this device. MPL accepts no responsibility whatsoever for such kind of defects, however caused.

2. General information and specifications

This chapter provides a general overview over the MIP405 and its features. It outlines the electrical and physical specifications of the product, its power requirements and a list of related publications.

2.1 Specifications

2.1.1 Electrical

Processor:
- IBM PPC405GP/PPC405GPr PowerPC™ 32Bit RISC Processor
- Separate, configurable, two-way set-associative instruction (16 kByte) and data (8/16 kByte) cache units
- Clock frequency 266/400 MHz
- Very low power consumption

Bootloader ROM:
- Up to 4/8MB Flash EEPROM
- 512kB U-Boot (open source) boot loader
- Easy boot loader update

Memory:
- up to 128MByte SDRAM on board
- ECC Support

Multi Purpose Socket:
- Supports different SRAM/FLASH/EPROM, 32 Pin DIL memory components
- Memory sizes up to 2MByte (EPROM)

RTC:
- Backed with onboard battery
- Year 2000 compliant

PC/104 /Plus Interface:
- ISA bridge Intel 82371EB (Southbridge)
- 16 Bit PC/104 interface
- 32 Bit PC/104 Plus Interface (PCI Host)

USB:
- 2 USB 1.0 ports for serial transfers at 12 or 1.5 Mbit/s
- ESD protected

Serial ports:
- Four serial Ports 16C550 compatible
- Two serial ports with RS232 signaling (SER0 and SER1).
- Two serial port with TTL signaling (COMA and COMB)
- Standard transfer rates up to 460 kBaud
- Optional transfer rates up to 1.15 MBaud
- 3 ports with full modem handshake (SER0, COMA and COMB)
- Available on four 10pin 2mm headers

E-IDE ports:
- 2 separate channels for up to 4 drives
- available on 44 pin header, 2 mm pitch, for 2,5” Notebook hard disk.
- PIO Mode 4 and Bus Master IDE, transfers up to 14 Mbytes/s
- Ultra DMA/33 mode, synchronous DMA mode transfers up to 33 Mbytes/s
- Activity indicator on board

Ethernet:
- PPC405GP/PPC405GPr integrated 10/100 MBit/s Ethernet Controller
- IEEE802.3 10BASE-T and 100BASE-TX compatible
- IEEE 802.3u Autonegotiation Support
- IEEE 802.3x 100BASE-TX Flow Control support
- Activity indicators for link detection/network traffic and 100 Mbit/s operation on board
- ESD protected

Speaker:
- Available on a 10-pin 2mm header

Indicators:
- Power LED (green)
- Reset / Power Fail LED (red)
- Error LED (red)
- HDD activity LED (green)
- LAN LED (green)
- 1 user programmable LED (green)

2.1.2 Physical / Power

Form factor:
PC/104, with connectors in defined I/O connectors overhang regions
Length: 95.9 mm (3.775 inches)
Width: 115.6 mm (4.550 inches)
Height: 14.0 mm (0.550 inch) (excluding PC/104 bus connectors)

Weight:
Typical 110g (fully equipped, without memory module)

Power supply:
Over PC/104 bus interface or through separate 3-pin Mini-Combicon power connector.

Input Power requirement:
+5V: +5VDC ± 5%

Power consumption:
PPC405GP @266MHz:
Typical. 800mA@5V (with Ethernet, USB and 128MB SDRAM)
PPC405GPr @400MHz:
Typical. 600mA@5V (with Ethernet, USB and 128MB SDRAM)

2.1.3 Environment

Temperature range:
0°C to +60°C (+32°F to +140°F) @ 266/400 MHz CPU speed without heat sink
extended temperature range available

Relative humidity:
10% ... 90% non condensing

2.2 Dimensions

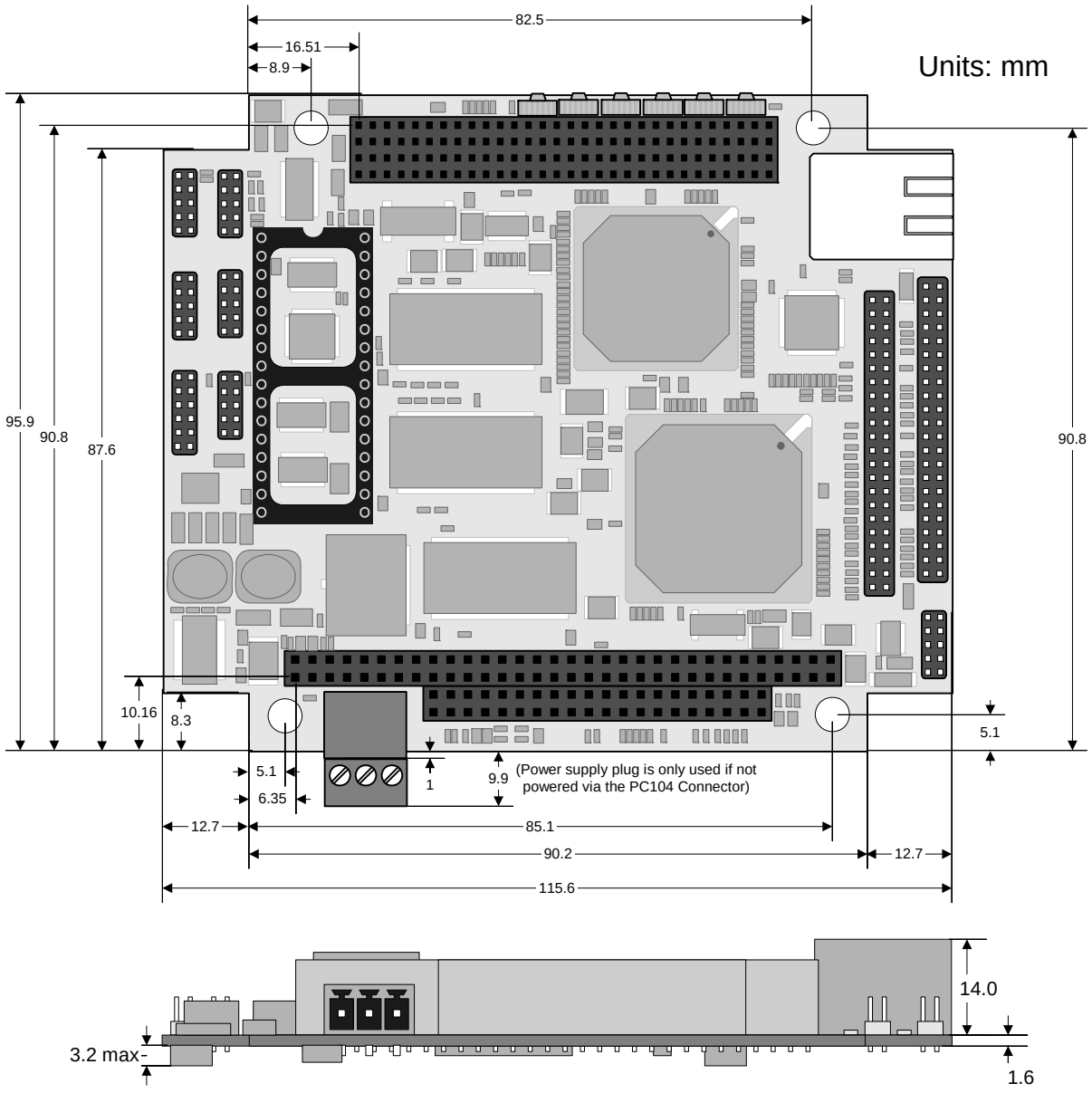


Figure 2.2.1 Dimensions MIP405

Drawing not to scale.

Since the PC104 Plus of the MIP405 is implemented as PCI Host, the MIP405 is **not** a stack-through board. Please see Chapter 5 Module Stack for further information.

3. Preparation for use

3.1 Parts location

3.1.1 Top view

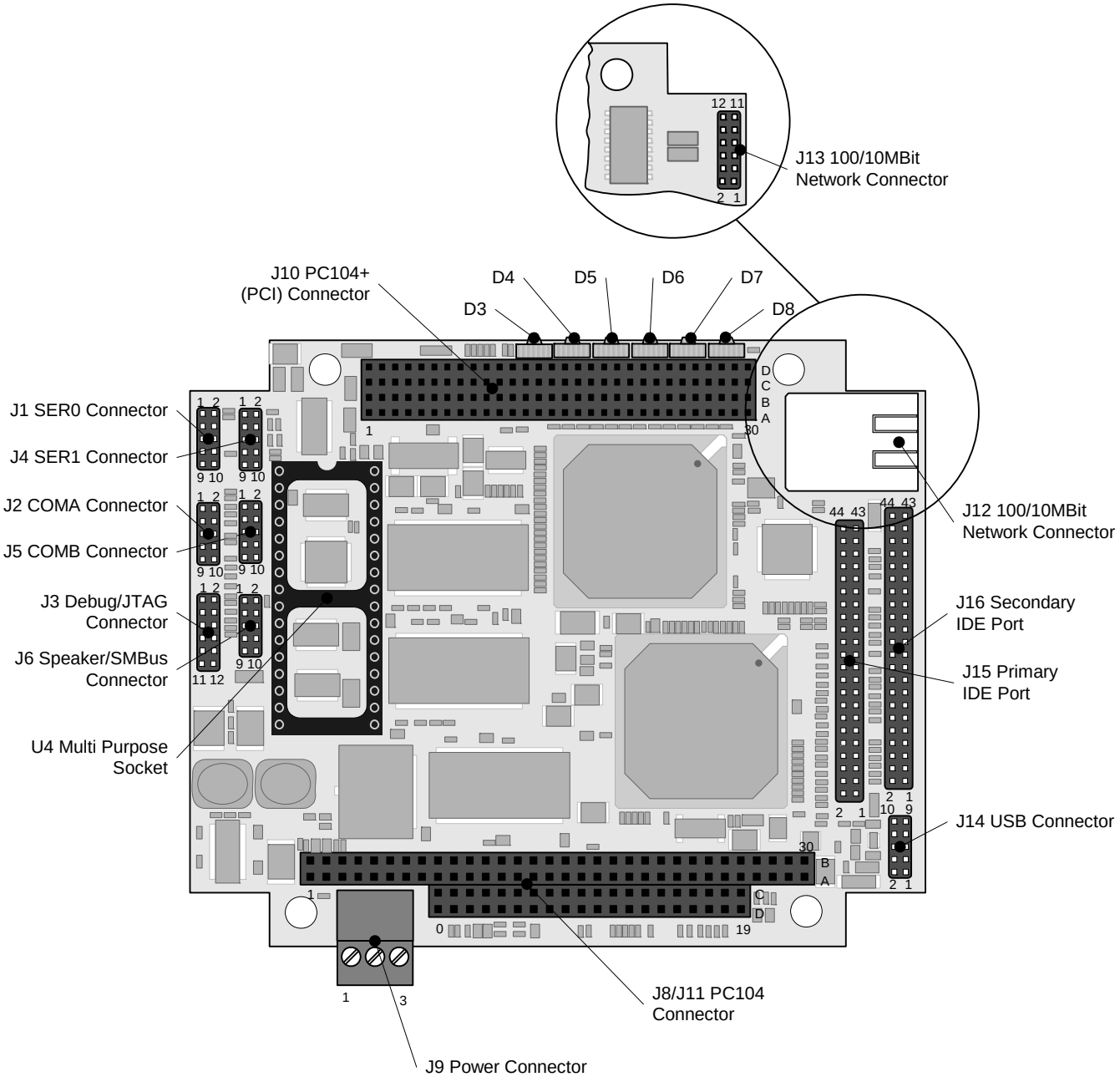


Figure 3.1.1 Parts location Top view

3.1.2 Bottom view

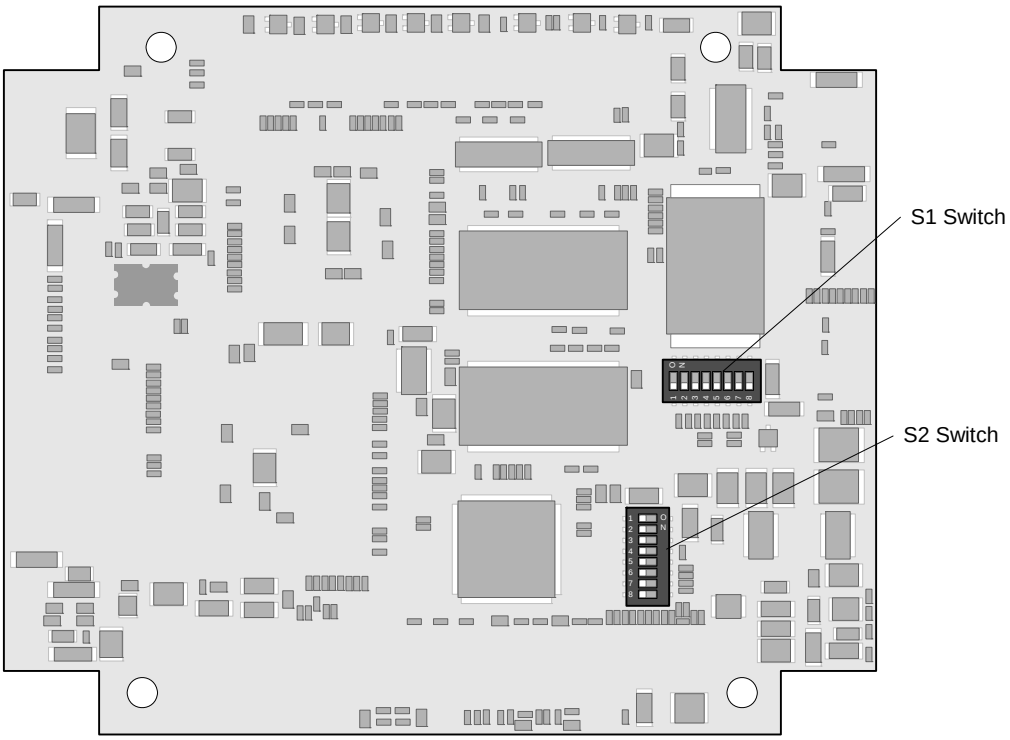


Figure 3.1.2 Parts location Bottom view MIP405

3.2 Switch settings

Default switch settings are bold.

3.2.1 DIP switch S1 – Software Configuration switch

The Software configuration switch is readable by reading the register EXT_REG.

Switch	On	Off	S1
S1-1	Console assignment from Environment	**Console is serial line 1**	
S1-2	not yet defined	**not yet defined**	
S1-3	not yet defined	**not yet defined**	
S1-4	not yet defined	**not yet defined**	
S1-5	not yet defined	**not yet defined**	
S1-6	not yet defined	**not yet defined**	
S1-7	not yet defined	**not yet defined**	
S1-8	not yet defined	**not yet defined**	

Table 3.2.1 S1: Software Configuration Switch

Notes:

- *A switch in ON Position will be read back as High*

3.2.2 DIP switch S2 – Hardware Configuration Switch

Switch	On	Off	S2
S2-1	**Battery backup enabled**	Battery backup disabled	
S2-2	**Boot Flash VPP enabled**	Boot Flash VPP disabled	
S2-3	Boot Flash Write protected	**Boot Flash Write enabled**	
S2-4	**EEPROM Write enabled**	EEPROM Write protected	
S2-5	Boot from MPS	**Boot from Boot Flash**	
S2-6	MPS CFG0 (Off)		
S2-7	MPS CFG1 (Off)		
S2-8	MPS CFG2 (On)		

Table 3.2.2 S2: Hardware Configuration Switch

Notes:

- *Boot Flash VPP and WP works only with some Boot flash Devices.*
- *Switch S2-6 to S2-8 are used to configure the device used on the MPS. Refer to 3.5* U4 - Multi purpose socket *for details.*

3.3 Indicators

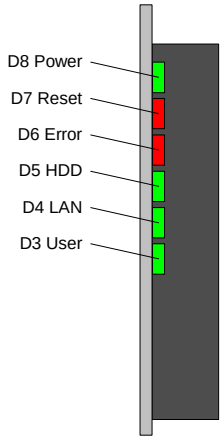
Ref	Color	Description		LEDs
D8	green	Power	Lit when 5V is Ok	
D7	red	Reset	Lit when PPC405 is in Reset	
D6	red	Error	Lit when PPC405 has detected an Error (Sys_Error)	
D5	green	HDD	Lit when IDE activity	
D4	green	LAN	Lit when Network activity	
D3	green	USER	Lit if bit ULED in Register COM_Mode is set	

Table 3.3.1 Indicators

3.4 Connectors

3.4.1 J1 – Serial port SER0 connector

The serial port SER0 is implemented as RS232 full Modem Handshake interface. For reference the pin numbering on a DB9 male connector has been included.

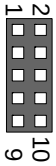
Number	Signal	Description	DB9 male	Pinout
1	DCD0	Carrier detect	1	
2	DSR0	Data set ready	6	
3	RXD0	Receive data	2	
4	RTS0	Request to send	7	
5	TXD0	Transmit data	3	
6	CTS0	Clear to send	8	
7	DTR0	Data terminal ready	4	
8	RI0	Ring indicator	9	
9	GND	Ground	5	
10	EARTH	Earth	Shield	

Table 3.4.1 J1 Serial port SER0 connector

3.4.2 J2 – Serial port COMA connector

The serial port COMA is implemented as a full Modem Handshake interface with TTL level signaling.

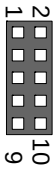
Number	Signal	Description	Pinout
1	DCDA	Carrier detect	
2	DSRA	Data set ready	
3	RXDA	Receive data	
4	RTSA	Request to send	
5	TXDA	Transmit data	
6	CTSA	Clear to send	
7	DTRA	Data terminal ready	
8	RIA	Ring indicator	
9	GND	Ground	
10	VCC5	5V power supply	

Table 3.4.2 J2 Serial port COMA connector

3.4.3 J3 – Debug/JTAG connector

The Debug JTAG Connector uses a non standard Pinout on a 12Pin 2mm Header.

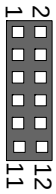
Number	Signal	Description	Pinout
1	VCC5	5V power supply	
2	GND	Ground	
3	CPU_TDO	CPU JTAG Data Out	
4	CPU_TDI	CPU JTAG Data In	
5	CPU_TRST#	CPU JTAG Reset	
6	CPU_TCK	CPU JTAG Clock	
7	CPU_TMS	CPU JTAG Mode Select	
8	CPU_HALT#	CPU Halt	
9	PLD_TDI	PLD JTAG Data In	
10	PLD_TDO	PLD JTAG Data Out	
11	PLD_TMS	PLD JTAG Mode Select	
12	PLD_TCK	PLD JTAG Clock	

Table 3.4.3 J3 Debug/JTAG connector

3.4.4 J4 – Serial port SER1 connector

The serial port SER1 is implemented as RS232 Interface. Since the PPC405 supports only CTS/RTS or DSR/DTR hardware handshake, others hardware handshake signals are not available. To switch between the CTS/RTS to DSR/DTR handshake, set the bit SER1_ALT in the COM_MODE register, clear the Bit DCS, and set the bit RDS in the Register CHCR0 of the PPC405.
For reference the pin numbering on a DB9 male connector has been included.

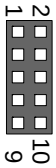
Number	Signal	Description	DB9 male	Pinout
1	NC	Not connect	1	
2	DSR1	Data set ready	6	
3	RXD1	Receive data	2	
4	RTS1	Request to send	7	
5	TXD1	Transmit data	3	
6	CTS1	Clear to send	8	
7	DTR1	Data terminal ready	4	
8	NC	Not connect	9	
9	GND	Ground	5	
10	EARTH	Earth	Shield	

Table 3.4.4 J4 Serial port SER1 connector

3.4.5 J5 – Serial port COMB connector

The serial port COMB is implemented as a full Modem Handshake interface with TTL level signaling.

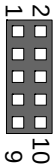
Number	Signal	Description	Pinout
1	DCDB	Carrier detect	
2	DSRB	Data set ready	
3	RXDB	Receive data	
4	RTSB	Request to send	
5	TXDB	Transmit data	
6	CTSB	Clear to send	
7	DTRB	Data terminal ready	
8	RIB	Ring indicator	
9	GND	Ground	
10	VCC5	5V power supply	

Table 3.4.5 J5 Serial port COMB connector

3.4.6 J6 – Speaker / SMBus connector

For system expansions the System Management Bus (SMBus), some General Purpose In/Output Signals along with the speaker signals are available on the connector J6.

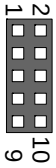
Number	Signal	Description	Pinout
1	VCC3	3.3V Power supply	
2	SMBCLK	SMBus clock	
3	SMBDATA	SMBus data	
4	GPI11	General Purpose Input 11	
5	GPI13	General Purpose Input 13	
6	GND	Ground	
7	GPO27	General Purpose Output 27	
8	GPO28	General Purpose Output 28	
9	VCC5	5V power supply (for the Speaker)	
10	SPKR	Speaker	

Table 3.4.6 J6 Speaker/SMBus connector

Notes: **All the Signals on the J6 are connected to the SouthBridge PIIX4E 82371EB. So the General Purpose Inputs/Outputs are the GPIO of the PIIX4E and not of the CPU. The names of the GPIOs correspond with the names of the ones of the PIIX4E.**
The Speaker Signal is the buffered Output (open-drain) to the SPRK Signal of the PIIX4E, which is driven by the Counter 2 of the PIIX4E.
For further information please refer to the SouthBridge Manual.

J9 - Power Connector

This connector is needed if no power via PC104 bus is provided. No other inputs than this and the power inputs on PC104 bus must be used to power the board.

3-pin power connector Phoenix Contact AG type MC1,5/3-G-3.81 pinout:

Pin number	Signal	Description	Pinout
1	V_{IN}	Input voltage (+5 V_{DC})	
2	GND	Ground	
3	SRESET#	System Reset Input (active low)	

Table 3.4.7 J9 Power connector

Counterpart is the Phoenix Contact AG connector type MC1,5/3-ST-3.81 (5-10A).

WARNING
Be aware of the input voltage polarization !
Wrong polarization of the input voltage can cause serious damage to the MIP405 and attached peripherals!

3.4.6.1 Connecting an external Reset Switch

On the SRESET# input on the External Power Connector exists the possibility to mount an external Reset Switch for system reset, see Figure 3-3. The SRESET# input is active low and can be connected directly to an open drain output (internal 10kΩ pull up resistor to 3.3V).

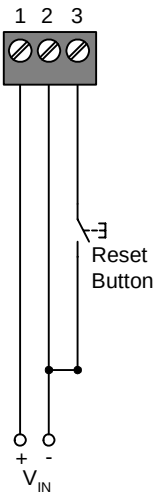


Figure 3-3 Mounting an External Reset Switch

WARNING
Do not apply other voltages than Vin- or tristate to the SRESET# input!
Exceeding these limits can cause serious damage to the MIP405!

3.4.7 J8/J11 - PC104 interface pin numbers

Number	Row A	Row B	Row C	Row D
0	--	--	GND	GND
1	/IOCHCK	GND	/SBHE	/MEMCS16
2	SD7	RSTDRV	LA23	/IOCS16
3	SD6	+5V	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	(-5V)[1]	LA20	IRQ12
6	SD3	DRQ2	LA19	IRQ15
7	SD2	(-12V)[1]	LA18	IRQ14
8	SD1	/ENDXFR	LA17	/DACK0
9	SD0	(+12V)[1]	/MEMR	DRQ0
10	IOCHRDY	NC	/MEMW	/DACK5
11	AEN	/SMEMW	SD8	DRQ5
12	SA19	/SMEMR	SD9	/DACK6
13	SA18	/IOW	SD10	DRQ6
14	SA17	/IOR	SD11	/DACK7
15	SA16	/DACK3	SD12	DRQ7
16	SA15	DRQ3	SD13	+5V
17	SA14	/DACK1	SD14	(/MASTER)[1]
18	SA13	DRQ1	SD15	GND
19	SA12	/REFRESH	NC	GND
20	SA11	SYSCLK	--	--
21	SA10	IRQ7	--	--
22	SA9	IRQ6	--	--
23	SA8	IRQ5	--	--
24	SA7	IRQ4	--	--
25	SA6	IRQ3	--	--
26	SA5	/DACK2	--	--
27	SA4	TC	--	--
28	SA3	BALE	--	--
29	SA2	+5V	--	--
30	SA1	OSC	--	--
31	SA0	GND	--	--
32	GND	GND	--	--

Pinout

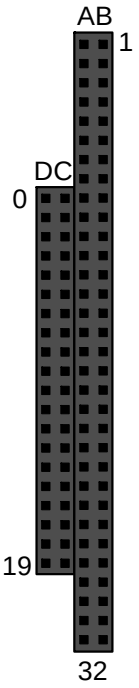


Table 3.4.8 PC/104 connector

Notes:

[1] *Signal not available. (-5V, +12V and -12V are not connected and /MASTER is pulled-down to GND)*

3.4.8 J10 - PC104+ Interface pin numbers

Number	Row A	Row B	Row C	Row D
1	GND	NC	+5V	AD0
2	+5V	AD2	AD1	+5V
3	AD5	GND	AD4	AD3
4	C/BE0	AD7	GND	AD6
5	GND	AD9	AD8	GND
6	AD11	+5V	AD10	(M66EN)[1]
7	AD14	AD13	GND	AD12
8	(+3.3V)[2]	C/BE1	AD15	(+3.3V)[2]
9	SERR	GND	(SBO)[1]	PAR
10	GND	PERR	(+3.3V)[2]	(SDONE)[1]
11	STOP	(+3.3V)[2]	(LOCK)[1]	GND
12	(+3.3V)[2]	TRDY	GND	DEVSEL
13	FRAME	GND	IRDY	(+3.3V)[2]
14	GND	AD16	(+3.3V)[2]	C/BE2
15	AD18	(+3.3V)[2]	AD17	GND
16	AD21	AD20	GND	AD19
17	(+3.3V)[2]	AD23	AD22	(+3.3V)[2]
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3	+5V	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0	GND	REQ1	+5V
24	GND	REQ2	+5V	GNT0
25	GNT1	+5V	GNT2	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD	+5V	RST
29	(+12V)[1]	INTA	INTB	INTC
30	(-12V)[1]	NC	NC	GND

Pinout

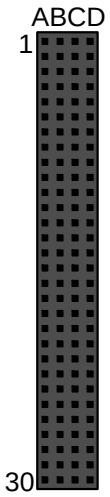


Table 3.4.9 J10 PC/104 Plus connector

Notes:

[1] *Signal not available. (SBO, SDONE and LOCK are pull-up to 5V, M66EN is connected to GND and +12V and -12V are not connected).*

[2] *3.3V pins are connected to a plane, but due to Power supply constrains, they are not connected to the 3.3V of the Power Supply.*

3.4.9 J12 - 10/100BASETX RJ45 Connector (only for Variants with Ethernet on RJ45)

Standard RJ45 Connector for a 100 Ohm Cable

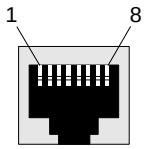
Pin number	Signal	Description	Pinout
1	TX+	Transmit data +	
2	TX-	Transmit data -	
3	RX+	Receive data +	
4	NC	Not connected	
5	NC	Not connected	
6	RX-	Receive data -	
7	NC	Not connected	
8	NC	Not connected	

Table 3.4.10 10/100Base TX connector

3.4.10 J13 – 10/100BASETX Header Connector (only for Variants with Ethernet on Header)

12Pin 2mm Header.

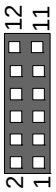
Number	Signal	Description	Pinout
1	TX+	Transmit Data +	
2	TX-	Transmit Data -	
3	RX+	Receive Data +	
4	TERM1	Termination 1	
5			
6	RX-	Receive Data -	
7	TERM2	Termination 2	
8			
9	NC		
10	NC		
11	EARTH	Shield	
12	EARTH	Shield	

Table 3.4.11 J13 10/100Base TX Header

3.4.11 J14 - USB Connector

The USB connector is a 10 pin 2mm pitch header. It has the signals for two USB ports on it.

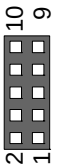
Pin number	Signal	Description	Pinout
1	VCC	Cable Power +5VDC Port1	
2	VCC	Cable Power +5VDC Port2	
3	Data1-	Balanced Data Line– Port1	
4	Data2-	Balanced Data Line– Port2	
5	Data1+	Balanced Data Line+ Port1	
6	Data2+	Balanced Data Line+ Port2	
7	GND	Cable Ground Port1	
8	GND	Cable Ground Port2	
9	NC	Not connected	
10	NC	Not connected	

Table 3.4.12 J14 USB connector

3.4.12 E-IDE connectors

There are two 44 pin header / 2 mm pitch E-IDE connectors on the MIP405. Physically each connector works as an independent IDE channel. J15 is connected to the primary and J16 is connected to the secondary port.

3.4.12.1 J23 - Standard E-IDE connector

Pin	Signal	Description	Pin	Signal	Description
1	/RESET	Reset	2	GND	Ground
3	D7	Data bit 7	4	D8	Data bit 8
5	D6	Data bit 6	6	D9	Data bit 9
7	D5	Data bit 5	8	D10	Data bit 10
9	D4	Data bit 4	10	D11	Data bit 11
11	D3	Data bit 3	12	D12	Data bit 12
13	D2	Data bit 2	14	D13	Data bit 13
15	D1	Data bit 1	16	D14	Data bit 14
17	D0	Data bit 0	18	D15	Data bit 15
19	GND	Ground	20	KEY	Key / not connected
21	DRQ	DMA request	22	GND	Ground
23	IOW	I/O write strobe	24	GND	Ground
25	IOR	I/O read strobe	26	GND	Ground
27	IORDY	I/O ready	28	HDBALE	Spindle sync / cable select
29	DACK	DMA acknowledge	30	GND	Ground
31	IRQ	Interrupt request	32	IOCS16	I/O chipselect16
33	A1	Address 1	34	NC	Not connected
35	A0	Address 0	36	A2	Address 2
37	CS0	Chipselect 0	38	CS1	Chipselect 1
39	ACTLED	Activity LED	40	GND	Ground
41	VCC	+5V	42	VCC	+5V
43	GND	Ground	44	GND	Ground

Table 3.4.13 EIDE connectors

3.5 U4 - Multi purpose socket

The Multi Purpose Socket allows to add various Memory devices to the MIP405:

- SRAM (with or without Battery backup) up to 4MBit (512kByte).
- Flash (bulk or sector erase) up to 4MBit (512kByte).
- EPROM/ROM up to 8MBit (1MByte).
- Disk On Chip

As a special feature the MIP405 allows to boot directly from the MPS.

3.5.1 Mounting Memory Modules

When selecting a component for the MPS, please check out first, if the pin-out is compatible with one of the pin configuration modes (refer to Table 3.5.1 MPS configuration).).
When mounting a Memory Device on the socket, remind the markers on the socket and the module for pin 1.

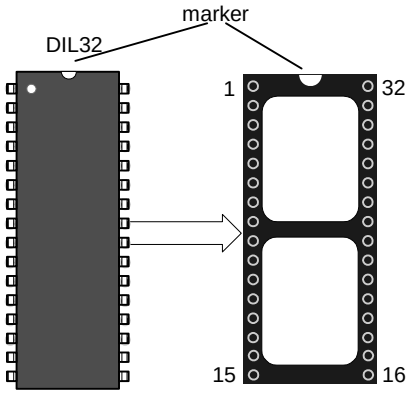


Figure 3.5.1 Multi Purpose Socket mounting

3.5.2 Switch settings for the Multi Purpose Socket

With the DIP switch S2-6 to S2-8 the Pins of the MPS are configurable. The following Table shows all possible Pin mappings:

Device	No	SW2			Pins				
		6	7	8	1	3	29	30	31
DIL32 1MBit SRAM	0	On	On	On		A14	WE#	CE2	A15
DIL32 4MBit SRAM	1	On	On	Off	A18	A14	WE#	A17	A15
DIL32 2MBit Flash (bulk)	2	On	Off	On	VCC3	A15	A14	A17	WE#
DIL32 4MBit Flash (sector)	3	On	Off	Off	A18	A15	A14	A17	WE#
DIL32 2MBit EPROM (default)	4	Off	On	On	PU	A15	A14	A17	PU
DIL32 8MBit EPROM	**5..7**	**Off**	**X**	**Off**	**A19**	**A15**	**A14**	**A17**	**A18**

Table 3.5.1 MPS configuration

3.5.3 Required module properties

- '5V only' types
- 8 bit data width
- TTL compatible signaling
- Access time should not exceed 250ns
- 32 pin, 600 mil wide DIL case
- MPS compatible pin-out (refer to Table 3.5.1 MPS configuration)
- Since the MIP405 delivers only 3.3V (max 12mA) VPP Flash programming may not be possible with some Devices.

3.5.4 Device types Examples for the Multi Purpose Socket:

Configuration	No	Type	No	Manufacturer	V_{IH}
DIL32 1MBit SRAM	**0**	1MBit SRAM 5V	S62C1024L	ISSI	2.2V
	0	1MBit SRAM 5V	KM681000C	Samsung	2.2V
DIL32 4MBit SRAM	**1**	4MBit SRAM	KM684000	Samsung	2.2V
	1	4MBit nonVolatile SRAM	DS1250Y/AB	Dallas	2.2V
DIL32 2MBit Flash (bulk)	**2**	2MBit Flash Bulk Erase 12V	P28F020	Intel	2.0V
	2	1MBit Flash Bulk Erase 12V	P28F010	Intel	2.0V
	2	2MBit Flash Bulk Erase 12V	Am28F020	AMD	2.0V
	2	1MBit Flash Bulk Erase 12V	Am28F010	AMD	2.0V
DIL32 Disc On Chip	**2**	DoC 2000 / Millenium		M-Systems	2.0V
DIL32 4MBit Flash (sector)	**3**	4MBit Flash Sector Erase 5V Only	Am29F040	AMD	2.0V
DIL32 2MBit EPROM	**4**	2MBit EPROM	Am27C020	AMD	2.0V
	4	1MBit EPROM	HN27C101AG	Hitachi	2.2V
DIL32 8MBit EPROM	**5**	4MBit EPROM	Am27C040	AMD	2.0V
	5	4MBit EPROM	NH27C4001G	Hitachi	2.2V
	5	8MBit EPROM	Am27C080	AMD	2.0V

Table 3.5.2 Device Types for MPS

Note:

- *Since the MIP405 delivers no 12V Vpp, only the 4MBit AMD Flash is erasable and writeable on Board. All other Flash types are read only.*
- *For the Disk On Chip use Mode 3*

3.5.5 External bootloader

It is also possible to boot from the MPS. The device containing the bootloader must be stuffed on the MPS and the switch S2 must be set according the 3.5.2 Switch settings for the Multi Purpose Socket.
If the Switch S2-5 is switched on, the PPC405 will boot out of the MPS (please refer to3.2.2 DIP switch S2 – Hardware Configuration Switch).
This feature is useful if a boot flash update has failed.

4. Operation

4.1 Block diagram

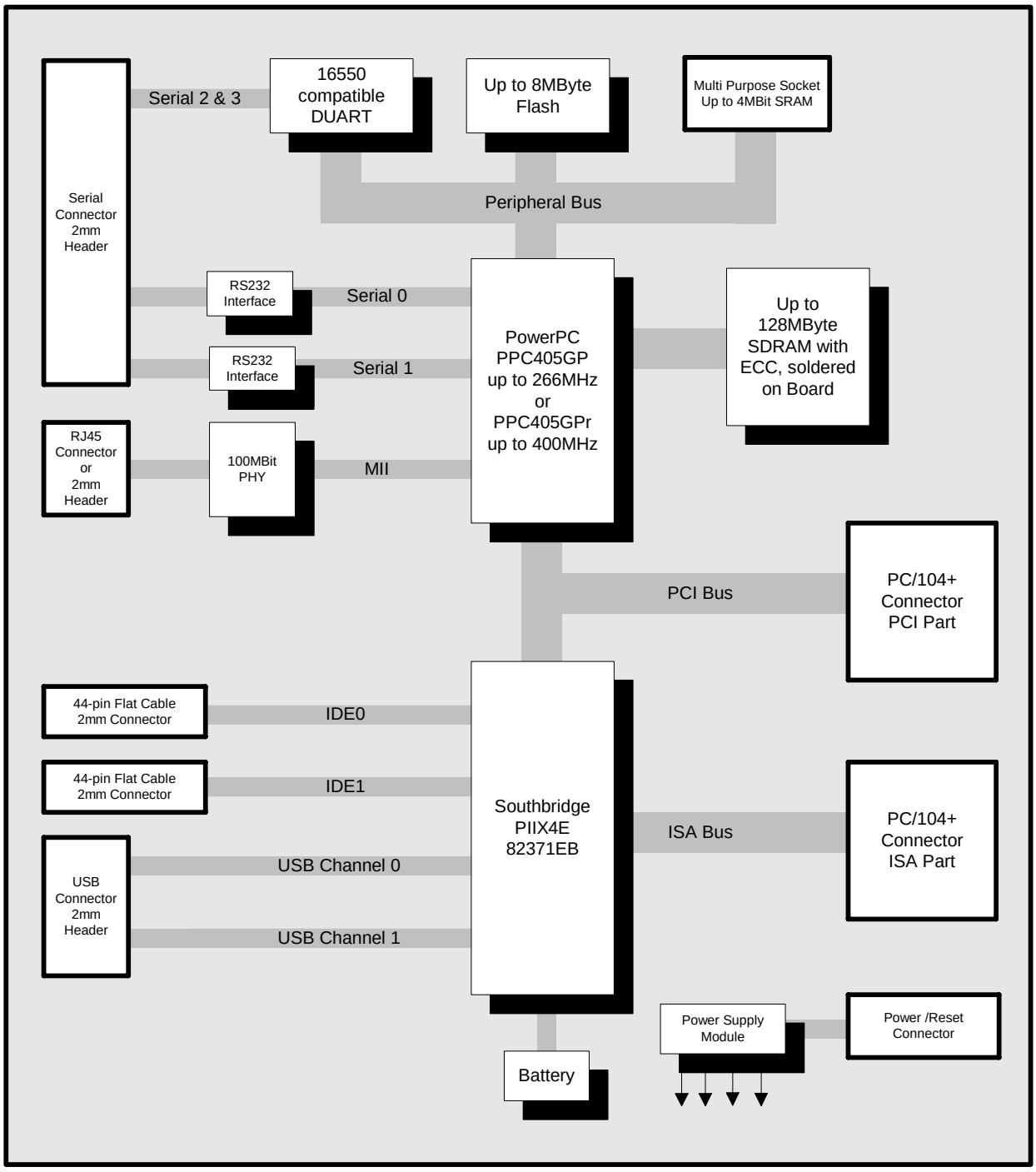


Figure 4.1.1 MIP405 Block Diagram

4.2 Memory Map

4.2.1 PPC405 System Mapping

Function	Sub Function	Start	End	Size
Local Memory/Peripherals 1		00000000	7FFFFFFF	2GB
PCI	Total	80000000	EF5FFFFF	1.74GB
	PCI Memory	80000000	E7FFFFFF	1.63GB
	PCI I/O	E8000000	E800FFFF	64KB
	Reserved	E8010000	E87FFFFF	
	PCI I/O	E8800000	EBFFFFFF	56MB
	Reserved	EC000000	EEBFFFFF	
	PCI Configuration Registers	EEC00000	EEC00007	8B
	Reserved	EEC00008	EECFFFFF	
	PCI Interrupt Acknowledge	EED00000	EEDFFFFF	1MB
	Reserved	EEE00000	EF3FFFFF	
	PCI local Configuration Registers	EF400000	EF40003F	64B
	Reserved	EF400040	EF5FFFFF	
Internal Peripherals	Total	EF600000	EFFFFFFF	10MB
	UART0	EF600300	EF600307	8B
	Reserved	EF600308	EF6003FF	
	UART1	EF600400	EF600407	8B
	Reserved	EF600408	EF6004FF	
	IIC0	EF600500	EF60051F	32B
	Reserved	EF600520	EF6005FF	
	OPB Arbiter	EF600600	EF60063F	64B
	Reserved	EF600640	EF6006FF	
	GPIO Controller Registers	EF600700	EF60077F	128B
	Reserved	EF600780	EF6007FF	
	Ethernet Controller Registers	EF600800	EF6008FF	256B
	Reserved	EF600900	EFFFFFFF	
Expansion ROM 2		F0000000	FFDFFFFF	254MB
Boot ROM 2, 3		FFE00000	FFFFFFFF	2MB

Table 4.2.1 PPC405 System Mapping

Notes:

1. *The Local Memory/Peripheral area of the memory map can be configured for SDRAM, ROM or Peripherals.*
2. *The Boot ROM and Expansion ROM area of the memory map are intended for use by ROM or Flash-type devices. While locating volatile SDRAM and SRAM in this region is supported by the controller it is not recommended that these regions be used for this purpose.*
3. *When the optional boot from PCI Memory is selected, the PCI Boot ROM address space begins at FFFE 0000 (size is 128KB).*

4.3 MIP405 Memory Mapping

The mapping of the MIP405 is setup by the U-Boot bootloader as follows:

Function	Start	End	Size	Notes
SDRAM	00000000	7FFFFFFF	32..128MB	depends on population
PCI Memory Area 1	80000000	9FFFFFFF	512MB	see 4.4 Local bus to PCI Mapping
PCI Memory Area 2	A0000000	BFFFFFFF	512MB	
PCI I/O 1	E8000000	E800FFFF	64KB	
PCI I/O 2	E8800000	EBFFFFFF	56MB	
Extensions Register (CS7)	F4000000	F40FFFFF	1MB	see 4.7 Extension registers
External UART0 (CS2)	F4100000	F41FFFFF	1MB	see 4.5 DUART Operation
External UART1 (CS3)	F4200000	F42FFFFF	1MB	
MPS (CS1)	F8000000	F83FFFFF	4MB	see 3.5 U4 - Multi purpose socket
Flash (CS0)	FFC00000	FFFFFFFF	4MB	depends on population

Table 4.3.1 MIP405 Mapping

Notes:

- The PPC405 is setup with the values of “Start”, “End” and “Size”. If the connected device may not use the entire Area. So the external UART0 uses only 8Byte not 1MByte.
- Since the PPC405 fetches its reset vector from address FFFFFFFC the flash has to end on FFFFFFFF. Depending on the flash size, the start address may vary.

4.4 Local bus to PCI Mapping

The CPU internal PLB to PCI bridge maps the 4 local bus areas to 4 PCI areas. The U-Boot sets following local bus to PCI memory mapping:

Area	Local Bus		PCI MemoryAddress		Size	Notes
	Start	End	Start	End		
PCI Memory Area 1	80000000	9FFFFFFF	80000000	9FFFFFFF	512MB	Free for expansions cards
PCI Memory Area 2	A0000000	BFFFFFFF	00000000	00FFFFFF	16MB	ISA Memory (hard wired)

Table 4.4.1 Local bus to PCI Memory Mapping

The local bus to PCI I/O mapping is initialized as follows:

Area	Local Bus		PCI I/O Address		Size	Notes
	Start	End	Start	End		
PCI I/O 1	E8000000	E800FFFF	00000000	0000FFFF	64KB	ISA I/O (hard wired)
PCI I/O 2	E8800000	EBFFFFFF	00800000	03FFFFFF	56MB	PCI I/O

Table 4.4.2 Local bus to PCI I/O Mapping

The local bus address has to be added to access a device on the PCI bus. For example, to access the registers of the first IDE port (ISA I/O 0x1F0) you have to access the local address 0xE80001F0.

4.5 DUART Operation

The 16C550 is connected to the PPC405 peripheral bus on CS2 and CS3.

4.5.1 Baudrate Clock

The Baudrate Clock for the 16C550 is derived from the main clock generator. With the bits S0..S2 in the COM_MODE Register, 8 different clocks can be selected.

S2	S1	S0	No	Clock nom.	Clock eff.	Error ppm	Max Baud	
							MCR.7=1	MCR.7=0
0	0	0	0	7.3728 MHz	7.3977 MHz	3381	115200	460800
0	0	1	1	11.0592 MHz	11.064 MHz	438	172800	691200
0	1	0	2	12 MHz	12.002 MHz	167	187500	750000
0	1	1	3	18.432 MHz	18.435 MHz	144	288000	1152000
1	0	0	4	22.1184 MHz	22.114 MHz	215	345600	1382400
1	0	1	5	24 MHz	23.996 MHz	158	375000	1500000
1	1	0	6	36.864 MHz	36.869 MHz	144	576000	2304000
1	1	1	7	40 MHz	39.992 MHz	196	625000	2500000

Table 4.5.1 Baudrate Clocks

The Baudrate is calculated according the following formula:

```
BaudRate=InputClock/16/Divisor
```

If the bit7 in the MCR of the 16C550 is set, the baudrate is divided by 4.
Following tables shows the divisors for the most common baudrates for all baudrate clocks.

Baud Rate	No. 0 (7.3977MHz)				No. 1 (11.064MHz)				No. 2 (12.002MHz)				No. 3 (18.435MHz)			
	MCR.7 = 1		MCR.7 = 0		MCR.7 = 1		MCR.7 = 0		MCR.7 = 1		MCR.7 = 0		MCR.7 = 1		MCR.7 = 0	
	div	%	div	%	div	%	div	%	div	%	div	%	div	%	div	%
50	2312	-0.01	9247	0.00	3458	-0.01	13830	0.00	3751	-0.01	15003	0.00	5761	0.00	23043	0.00
75	1541	0.01	6165	0.00	2305	0.00	9220	0.00	2500	0.02	10002	0.00	3841	-0.01	15362	0.00
110	1051	-0.02	4203	0.01	1572	-0.03	6286	0.01	1705	-0.01	6819	0.00	2619	-0.02	10474	0.00
150	771	-0.05	3082	0.01	1153	-0.04	4610	0.00	1250	0.02	5001	0.00	1920	0.01	7681	0.00
300	385	0.08	1541	0.01	576	0.04	2305	0.00	625	0.02	2500	0.02	960	0.01	3841	-0.01
600	193	-0.18	771	-0.05	288	0.04	1153	-0.04	313	-0.14	1250	0.02	480	0.01	1920	0.01
1200	96	0.34	385	0.08	144	0.04	576	0.04	156	0.18	625	0.02	240	0.01	960	0.01
2400	48	0.34	193	-0.18	72	0.04	288	0.04	78	0.18	313	-0.14	120	0.01	480	0.01
3600	32	0.34	128	0.34	48	0.04	192	0.04	52	0.18	208	0.18	80	0.01	320	0.01
4800	24	0.34	96	0.34	36	0.04	144	0.04	39	0.18	156	0.18	60	0.01	240	0.01
9600	12	0.34	48	0.34	18	0.04	72	0.04			78	0.18	30	0.01	120	0.01
14400	8	0.34	32	0.34	12	0.04	48	0.04	13	0.18	52	0.18	20	0.01	80	0.01
19200	6	0.34	24	0.34	9	0.04	36	0.04			39	0.18	15	0.01	60	0.01
38400	3	0.34	12	0.34			18	0.04							30	0.01
57600	2	0.34	8	0.34	3	0.04	12	0.04			13	0.18	5	0.01	20	0.01
115200	1	0.34	4	0.34			6	0.04							10	0.01
230400			2	0.34			3	0.04							5	0.01
460800			1	0.34												
1152000															1	0.01

Table 4.5.2 Baudrate for Configuration 0 to 3

Baud Rate	No. 4 (22.114MHz)				No. 5 (23.996 MHz)				No. 6 (36.869 MHz)				No. 7 (39.992 MHz)			
	MCR.7 = 1		MCR.7 = 0		MCR.7 = 1		MCR.7 = 0		MCR.7 = 1		MCR.7 = 0		MCR.7 = 1		MCR.7 = 0	
	div	%	div	%	div	%	div	%	div	%	div	%	div	%	div	%
50	6911	-0.01	27642	0.00	7499	0.00	29995	0.00	11522	0.00	46087	0.00	12498	0.00	49990	0.00
75	4607	0.00	18428	0.00	4999	0.00	19997	0.00	7681	0.00	30724	0.00	8332	0.00	33327	0.00
110	3141	0.00	12565	0.00	3409	-0.01	13634	0.00	5237	0.00	20948	0.00	5681	-0.01	22723	0.00
150	2304	-0.02	9214	0.00	2500	-0.02	9998	0.00	3841	-0.01	15362	0.00	4166	0.00	16663	0.00
300	1152	-0.02	4607	0.00	1250	-0.02	4999	0.00	1920	0.01	7681	0.00	2083	0.00	8332	0.00
600	576	-0.02	2304	-0.02	625	-0.02	2500	-0.02	960	0.01	3841	-0.01	1041	0.04	4166	0.00
1200	288	-0.02	1152	-0.02	312	0.14	1250	-0.02	480	0.01	1920	0.01	521	-0.05	2083	0.00
2400	144	-0.02	576	-0.02	156	0.14	625	-0.02	240	0.01	960	0.01	260	0.14	1041	0.04
3600	96	-0.02	384	-0.02	104	0.14	417	-0.10	160	0.01	640	0.01	174	-0.24	694	0.04
4800	72	-0.02	288	-0.02	78	0.14	312	0.14	120	0.01	480	0.01	130	0.14	521	-0.05
9600	36	-0.02	144	-0.02	39	0.14	156	0.14	60	0.01	240	0.01	65	0.14	260	0.14
14400	24	-0.02	96	-0.02	26	0.14	104	0.14	40	0.01	160	0.01	43	0.92	174	-0.24
19200	18	-0.02	72	-0.02			78	0.14	30	0.01	120	0.01			130	0.14
38400	9	-0.02	36	-0.02			39	0.14	15	0.01	60	0.01			65	0.14
57600	6	-0.02	24	-0.02			26	0.14	10	0.01	40	0.01			43	0.92
115200	3	-0.02	12	-0.02			13	0.14	5	0.01	20	0.01				
230400			6	-0.02							10	0.01				
460800			3	-0.02							5	0.01				
1152000											2	0.01				
1250000															2	-0.02
1500000							1	-0.02								
2304000											1	0.01				
2500000															1	-0.02

Table 4.5.3 Baudrate for Configuration 4 to 7

4.6 Interrupts

4.6.1 CPU Interrupts

The PPC405 provides 7 Interrupts. They are distributed as follows:

CPU IRQ	IRQ Source	Source
0	INTR# (PIIX Interrupt Controller)	EPLD
1	COMA_INT# COMB_INT#	EPLD
2	SMI# and NMI#	EPLD
3	PCI_INTA#	PCI Bus
4	PCI_INTB#	PCI Bus
5	PCI_INTC#	PCI Bus
6	PCI_INTD#	PCI Bus / USB

Table 4.6.1 CPU Interrupts

Note:

- *The 3 Interrupts from the EPLD are routed as follows:*
- *INTR# is the inverted INTR Signal form the PIIX Interrupt Controller*
- *COM_INT0# and COM_INT1# are the pulsed Interrupt signals from the DUART*
- *NMI# is the inverted NMI Signal from the PIIX*
- *SMI# is the PIIX SMI# Signal*

4.6.2 ISA Interrupts

The ISA Interrupts are routed as follows:

IRQs	Device	Remarks
IRQ0	Timer	PIIX Internal, not available
IRQ1	Free	
IRQ2	2nd IRQ Controller	PIIX Internal, not available
IRQ3	Free	
IRQ4	Free	
IRQ5	Free	
IRQ6	Free	
IRQ7	Free	
IRQ8	RTC	PIIX Internal, not available
IRQ9	Free	
IRQ10	Free	
IRQ11	Free	
IRQ12	Free	
IRQ13	Free	
IRQ14	Primary IDE	Not Maskable
IRQ15	Secondary IDE	Not Maskable

Table 4.6.2 ISA Interrupts

4.7 Extension registers

The PLD is located at the CS7# on the peripheral local bus. The bit notations are in big Endian Format (That is D0 MSB, D7 LSB)

Offset	Name	Type	Function
5	EXT_REG	Read only	Config Register
4	COM_MODE	Read/Write	Communication Mode Register
3	IRQ_REG	Read only	IRQ Register
2	BOARD_REV	Read only	Board Revision and populated Configuration
1	PLD_VERS	Read only	Versions Number of the PLDs
0	PLD_PART	Read only	Part Number of the PLDs

Table 4.7.1 Extensions Registers

4.7.1 PLD Partnumber Register

PLD_PART					PLD_CS# + 0x00		Read Only	
	D0	D1	D2	D3	D4	D5	D6	D7
Read	MIPID	PLD Part Number						
Default	0	0	0	0	0	0	0	0

Table 4.7.2 PLD Partnumber register

PLD Part Number is the Part Index of the PLD. This is currently 00.

4.7.2 PLD Version Register

PLD_VERS					PLD_CS# + 0x01		Read Only	
	D0	D1	D2	D3	D4	D5	D6	D7
Read	PLD Version Number							
Default	0	0	0	0	0	0	0	1

Table 4.7.3 PLD Version Register

PLD Version Number is the Version Number of the PLD. This is currently 0x01.

4.7.3 Board Revision and Config Register

BOARD_REV					PLD_CS# + 0x02		Read Only	
	D0	D1	D2	D3	D4	D5	D6	D7
Read	PCB0	PCB1	PCB2	PCB3	CFG0	CFG1	CFG2	CFG3
Default	0	0	0	0	X	X	X	X

Table 4.7.4 Board Revision and Config Register

PCBx: Binary decoded PCB Revision. Add an ASCII 'A' to this number to get the PCB Revision. Currently PCB3..0 = 0010 => 'C'.

CFGx: Config Inputs. Used to distinguish different population or other Options. Connected to VCC or GND via Config Resistors. Currently following populations Options are valid:

PCB0..3	CFG0..3	Variants
0000	1111	MIP405-1
0000	0111	MIP405-2
0000	0011	MIP405-4
0001	1111	MIP405-3 (only prototypes)
0010	1111	MIP405-3

Table 4.7.5 Config bits

4.7.4 IRQ Register

IRQ_REG					PLD_CS# + 0x03		Read Only	
	D0	D1	D2	D3	D4	D5	D6	D7
Read	INTR#	C_INT0#	C_INT1#	SMI#	INIT#	NMI#	Reserved	Reserved
Default	1	1	1	1	1	1	1	1

Table 4.7.6 IRQ Register

INTR#: Interrupt from PIIX. (Low Active) Will be forwarded to the PPC405 on INT0#
C_INT0#: Interrupt 0 from DUART. (Low Active) Will be forwarded as pulsed IRQ to the PPC405 on INT1#
C_INT1#: Interrupt 1 from DUART. (Low Active) Will be forwarded as pulsed IRQ to the PPC405 on INT1#
SMI#: System Management Interrupt from PIIX. (Low Active) Will be forwarded to the PPC405 on INT2#
INIT#: Init Output from PIIX. (Low Active) Will be forwarded to the PPC405 on INT2#
NMI#: Non maskable Interrupt from PIIX. (Low Active) Will be forwarded to the PPC405 on INT2#

Note: *C_INT0# and C_INT1# will be forwarded to the PPC405 as pulsed IRQ.*

4.7.5 Communication Mode Register

COM_MODE					PLD_CS# + 0x04		Read / Write	
	D0	D1	D2	D3	D4	D5	D6	D7
Read	SER1ALT	S0	S1	S2	Reserved	ULED	Reserved	IDERST
Write	SER1ALT	S0	S1	S2	Reserved	ULED	Reserved	IDERST
Default	0	0	0	0	0	0	0	0

Table 4.7.7 communication Mode Register

SER1ALT: Alternate SER1 Hardware Handshake. If set, the SER1 uses DTR, DSR Handshaking instead of CTS, RTS. If this Bit is set, clear the Bit DCS, and set the bit RDS in the Register CHCR0 of the PPC405.
Sx: Binary encoded value for the baudrate of the DUART and the clock on the UARTSERCLK Input of the PPC405GP. See chapter 4.5.1 Baudrate Clock for details.
ULED: If set, the User LED is switched on.
IDERST: Reset of the IDE Port. If set the IDE Reset is asserted (Low)

5. Module Stack

The clock signals of the PCI devices on the PC104 Plus must have all the same length. Since the MIP405 is the PCI Host in the PC104 Plus stack, the MIP405 compensate the clock length differences for all PCI devices, as specified by the PCI and the PC104 Plus Specification. Therefore the MIP405 **must** be the most bottom module. That is why the MIP405 is equipped with non Stack-Through connectors. If the MIP405 is used within a PC104 Plus stack, please pay attention to following points:

- The MIP405 must be the most bottom Module.
- If other PC104 Plus Modules are used, they must be the next in order.
- All PC104 Plus Modules must have a different slot address (refer to the documentation of the PC104 Plus Module for more information)
- The slot address of the module directly on the top of the MIP405 must be 0, the following must be 1 etc.
- Please note that the Modules with the slot address 3 and 4 cannot both be bus masters.
- If PC104 Modules are also used, they have to be placed above the PC104 Plus stack.

6. Debug Cable for MIP405

To connect the MIP405 to an IBM RISCWatch (or similar Debuging Tools) an atapter cable must be made. Please use the following wiring:

MIP405 J3 12pin 2mm Header female. Pin Number	Signal	RISCWatch Connector 16pin 2.54mm Header female Pin Number
1	5V (see Note)	6
2	GND	16
3	TDO	1
4	TDI	3
5	TRST#	4
6	TCK	7
7	TMS	9
8	HALT#	11
9	NC	
10	NC	
11	NC	
12	NC	

Notes:

- Pin 3 of the MIP405 J3 Connector is hardwired to 5V. IBM recommends to connect it either to 3.3V or 5V via an 1K resistor. For some debug tools (eg. OCDemon RAVEN) it must be hardwired to 5V. Please consult the documentation of your debug tool for the correct wiring.
- NC means Do not Connect

7. Support information

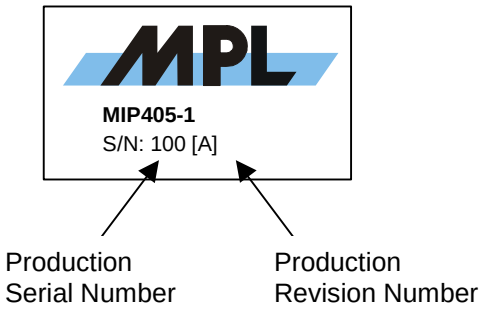
7.1 MPL AG

In case of questions contact MPL AG or your local distributor.

MPL AG homepage: www.mpl.ch
Email address: support@mpl.ch

7.2 Production serial and revision number

To get the actual production revision number of your device, please see the label on MIP405 Board.



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Copyright and revision history

This manual reflects Revision C of the MIP405.

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