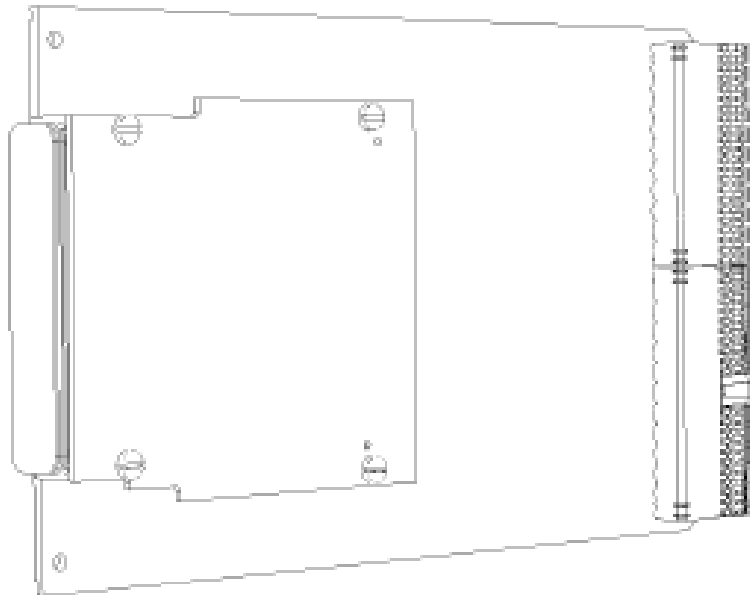


FMC230 User Manual



4DSP, USA

www.4dsp.com/forum

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Revision History

| Date | Description | Revision |
|------------|--|----------|
| 2012-12-19 | Release | 1.0 |
| 2013-02-05 | Corrected pin assignments in Appendix A | 1.1 |
| 2013-03-22 | Updated analog output range in Table 2 and added a FMC700 requirement information for KC705 | 1.2 |
| 2013-08-15 | Updated analog output bandwidth in Table 2. Added a signal description in Appendix A. | 1.3 |
| 2014-01-30 | Removed incorrect reference to analog input gain and over range in Chapter 2 | 1.4 |
| 2014-04-07 | Revised some descriptions and fixed typos. Changed external reference input characteristics. | 1.5 |
| 2014-05-30 | Corrected analog output power range in Table 2 | 1.6 |
| 2014-07-03 | Added DACx_SYNC signals in Appendix A | 1.7 |
| 2014-10-02 | Updated external reference input characteristics | 1.8 |
| 2015-02-27 | Clarified external clock frequency range | 1.9 |
| 2015-06-22 | Updated analog output and external sample clock input characteristics | 1.10 |

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1 Acronyms and related documents

1.1 Acronyms

| | |
|--------|--|
| ADC | Analog-to-Digital Converter |
| DDR | Double Data Rate |
| DSP | Digital Signal Processing |
| EPROM | Erasable Programmable Read-Only Memory |
| FBGA | Fineline Ball Grid Array |
| FMC | FPGA Mezzanine Card |
| FPGA | Field Programmable Gate Array |
| JTAG | Joint Test Action Group |
| LED | Light Emitting Diode |
| LVTTTL | Low Voltage Transistor Logic level |
| LSB | Least Significant Bit(s) |
| LVDS | Low Voltage Differential Signaling |
| MGT | Multi-Gigabit Transceiver |
| MSB | Most Significant Bit(s) |
| PCB | Printed Circuit Board |
| PCI | Peripheral Component Interconnect |
| PCIe | PCI Express |
| PLL | Phase-Locked Loop |
| PMC | PCI Mezzanine Card |
| PSSR | Power Supply Rejection Ratio |
| QDR | Quadruple Data rate |
| SDRAM | Synchronous Dynamic Random Access memory |
| SRAM | Synchronous Random Access memory |
| TTL | Transistor Logic level |
| XMC | PCIe Mezzanine card |

Table 1: Glossary

1.2 Related Documents

- FPGA Mezzanine Card (FMC) standard ANSI/VITA 57.1-2010
- Datasheet AD9129, Rev C, Analog Devices
- Datasheet AD9517 Rev A, Analog Devices
- Datasheet AD7291 Rev B, Analog Devices
- FMC700 User Manual, 4DSP

2 General description

The FMC230 is a two channel DAC FMC daughter card. The card provides two 14-bit up to 5.7 GSPS DAC channels which can be clocked by an internal clock source (optionally locked to an external reference) or an externally supplied sample clock. There is one trigger input for customized sampling control. The FMC daughter card is mechanically and electrically compliant to FMC standard (ANSI/VITA 57.1). The FMC has a high-pin count connector, front panel I/O, and can be used in a conduction-cooled environment.

The design is based on Analog Devices AD9129 single-channel 14-bit 5.7 GSPS DAC with DDR LVDS inputs. The analog output signals are AC-coupled and connect to MMCX coax connectors on the front panel.

The FMC allows flexible control of sampling frequency through serial communication busses. Furthermore, the card is equipped with power supply and temperature monitoring, and it offers several power-down modes to switch off unused functions or protect the card from overheating.

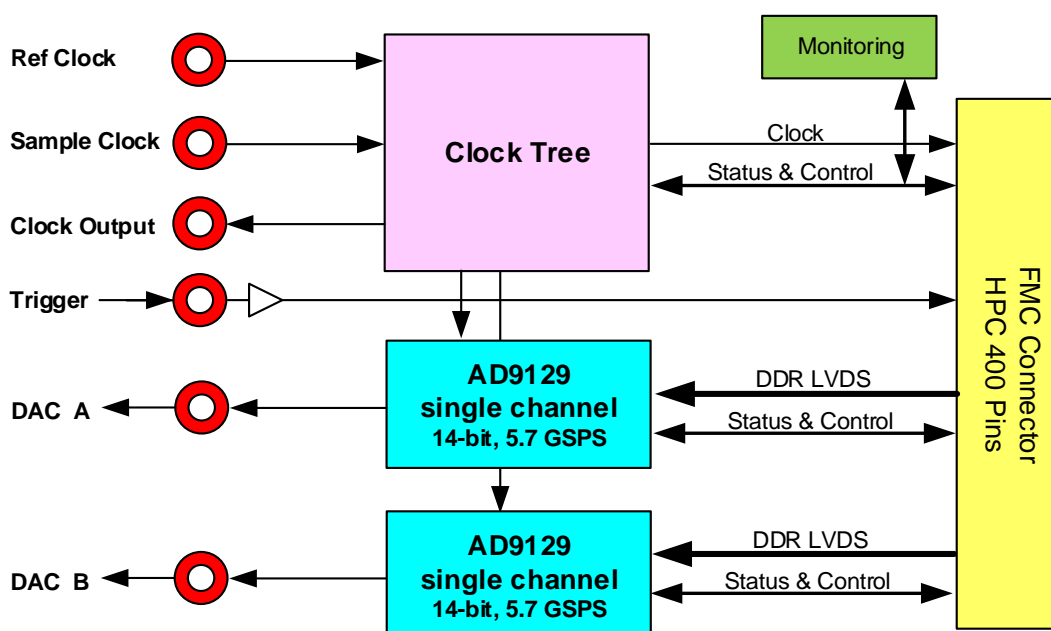


Figure 1: FMC230 block diagram

3 Installation

3.1 Requirements and handling instructions

- Prevent electrostatic discharges by observing ESD precautions when handling the card.
- Do not flex the card.
- The FMC daughter card must be installed on a carrier card compliant to the FMC standard.
- The FMC carrier card must support the high-pin count connector (400-pins) to support all channels. A low-pin count connector is supported but may result in limited features.
- The FMC carrier card may support a VADJ/VIO_B voltage of +1.2V to +3.3V.
- The FMC700 is required in order to use the FMC230 on KC705.

4 Design

4.1 Physical specifications

4.1.1 Board Dimensions

The FMC card complies with the FMC standard known as ANSI/VITA 57.1. The card is a single-width, conduction-cooled mezzanine module (with region 1 and front panel I/O). There may be a mechanical conflict with the front rib on a carrier card. The stacking height is 10mm, and the PCB thickness is 1.6mm.

4.1.2 Front panel

There are six MMCX connectors available from the front panel. From top to bottom:

- Analog outputs B (D1) and A (D0)
- Trigger in (TR)
- Clock Input (CI)
- Reference Input (RI)
- Clock Output (CO)

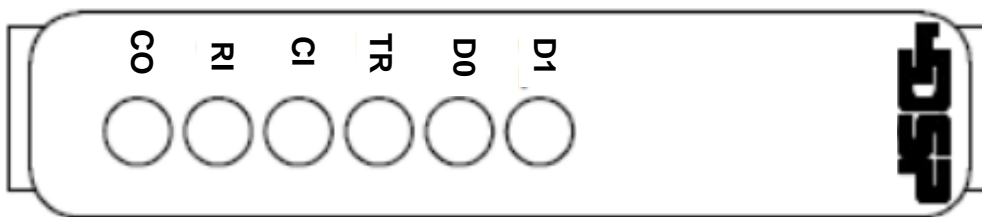


Figure 2: Front panel layout

4.2 Electrical specifications

The DAC devices use DDR LVDS signals mapped to the regular FMC pins. Each channel has two 14-bit wide DDR LVDS busses.

Control signals operate in LVCMOS mode. A VADJ range of 1.2V to 3.3V is supported. The voltage on VIO_B pins will follow the voltage on VADJ.

The CLKx pins are required to be LVDS by the FMC standard. CLK2 and CLK3 are not used for best compatibility with Xilinx development platforms. CLK0 is connected to a spare clock output of the clock tree. CLK1 is connected to the external trigger.

4.2.1 EEPROM

The FMC card has a small serial EEPROM (M24C02) which is accessible from the carrier card through the I²C bus. The EEPROM is powered by 3P3VAUX. The standby current is only 0.01µA when SCL and SDA are kept at 3P3VAUX level. These signals may also be left floating since pull-up resistors are present on the FMC. The EEPROM is write-protected by default.

4.2.1 FMC Connector

FMC Top Connector

The top connector is the main connector to the FMC carrier board. The pin-out is defined in the appendix. The connector is a HPC connector.

FMC Bottom Connector

The high-pin count connector enables FMC card stacking. The following connections are available between the top and bottom FMC connector:

- Unused gigabit data signals (DP[4..9]_M2C_P/N, DP[0..9]_C2M_P/N)
- All gigabit reference clocks (GBTCLK[0..1]_M2C_P/N)
- RES0
- 3P3VAUX, 3P3V, 12P0V, VADJ
- JTAG (see section 4.2.1)

The bottom connector is not mounted by default.

4.2.1 JTAG

In a stacked environment, the TDI pin will be decoupled from the TDO pin by the PRST_M2C_L signal coming from the bottom connector. TRST#, TCK, TMS, TDI, and TDO are directly connected between top to bottom connector.

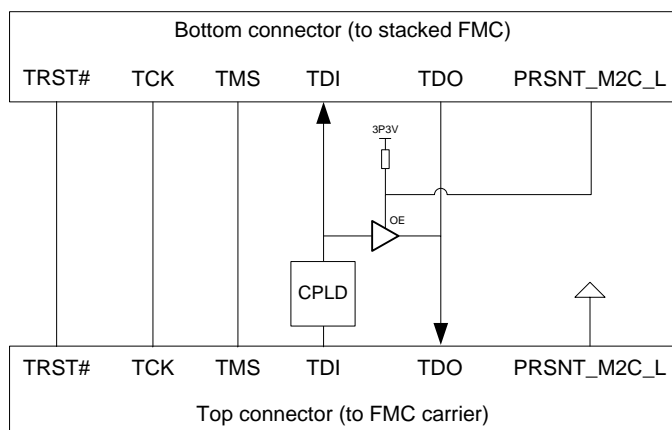


Figure 3: JTAG Connection

4.3 Main characteristics

| Analog outputs | |
|----------------------|---|
| Number of channels | 2 |
| Channel resolution | 14-bit |
| Output voltage range | 1.12 V _{pp} (5 dBm) |
| Output impedance | 50Ω (optimized output impedance for mixed-mode operation) |

| | |
|--|--|
| Analogue output bandwidth | 1.4GHz, please refer to AD9129 datasheet for details |
| External sampling clock input | |
| Input Level | -10dBm < Clock In Level < 10dBm 0dBm typical (LVTTTL level supported ¹) |
| Input impedance | 50Ω |
| Input range | 4.5 MHz to 2850 MHz ² |
| External reference clock input | |
| Serial numbers FMC230-0000 to FMC230-0186 | |
| Input Level | LVTTL: $3.6 > V_{IH} > 2.0V$, $-0.3 < V_{IL} < 0.8V$ |
| Input impedance | 50Ω (DC-coupled) |
| Input range | 0MHz to 250MHz |
| Serial numbers FMC230-0187 and above | |
| Input Level | LVTTL: $3.6 > V_{IH} > 2.0V$, $-0.3 < V_{IL} < 0.8V$ Input is DC-coupled and self-biased to 1.5V, refer to 4.7 |
| Input impedance | 5KΩ |
| Input range | 0MHz to 250MHz |
| External clock output | |
| Output Level | 800mV _{p-p} into 50Ω typical (LVCMOS output available as build option, contact 4DSP) |
| External Trigger input | |
| Format | LVTLL/LVCMOS33 Logic ‘0’ → max 0.8V / Logic ‘1’ → min 2.0V |
| Frequency range | Up to 300 MHz |
| Internal sampling clock | |
| Format | LVPECL |
| Frequency Range | DAC: up to 5300MHz (Software selectable, contact 4DSP for frequencies higher frequencies up to 5700MHz) |

Table 2 : FMC daughter card main characteristics

4.4 Analog output channels

The DAC output circuit is constructed such that different build options are available. The default configuration is a wideband balun ETC1-1-13 (MACOM; 4.5 to 3000MHz) as shown in Figure 4. This configuration is the recommended output circuit for mixed-mode operation of the DAC, for details refer to the AD9129 datasheet.. Please contact 4DSP for custom configurations.

¹ 3.3V LVTTTL into 50Ohm would result in 14dBm, a 1A Schottky diode in the clock input circuit protects the clock input from overvoltage when driving the input with a LVTTTL signal.
² AD9517 device does support up to 2850MHz with a clock input level of 0dB and higher.

The clock tree has a PLL and clock distribution section. The PLL ensures locking of the internal VCO clock to an external supplied reference. There is an onboard reference which is used if no external reference is present. The onboard reference is a QuartzCom TX3-801 30.72MHz.

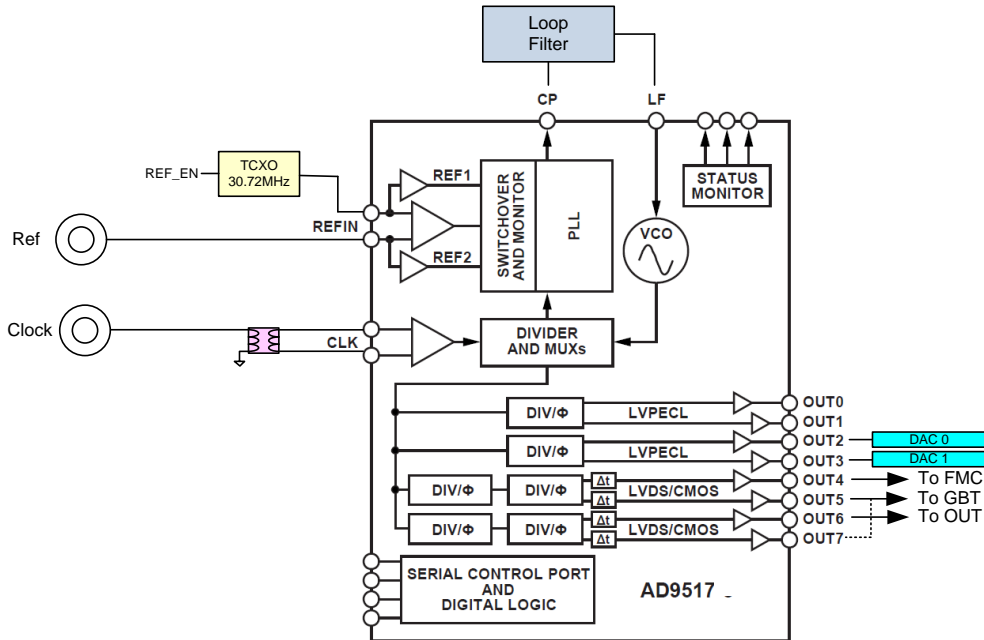


Figure 5: Clock tree

The AD9517 has four LVPECL outputs. OUT2 and OUT3 are used for clocking the DAC devices. The other four clock outputs can be programmed either as LVDS or LVCMOS33. These outputs have the ability to enable a programmable delay. OUT4 is connected to the FMC connector for test and monitoring purposes. OUT5 connects to the gigabit transceiver reference clock on the FMC connector (as a build option it can be connected to OUT7). OUT6 connects to the clock output on a MMCX connector.

4.9.1 PLL design

The PLL functionality of the AD9517 is used to operate from an internal sampling clock to enable flexibility in frequency selection while maintaining high performance.

The default loop filter is designed for a phase detector frequency of 7.68MHz ($f_{ref}/4$), loop bandwidth of 10KHz, phase margin of 45 deg, and a charge pump of 4.8mA.

Lower phase detector frequencies might be required to achieve the required output clock frequency (phase detector frequency equals the VCO tuning step size). Whether the loop filter design still works for other configurations should be investigated case by case.

| Card Type | Device | VCO Range | VCO | DAC Clock |
|-----------|----------|-------------------|------------|------------|
| FMC230 | AD9517-1 | 2300MHz - 2650MHz | 2457.60MHz | 2457.60MHz |

Table 3: FMC default clock configurations

Note: Higher DAC clock frequencies (2850MHz for sampling up to 5700Mps) can be achieved using external clock.

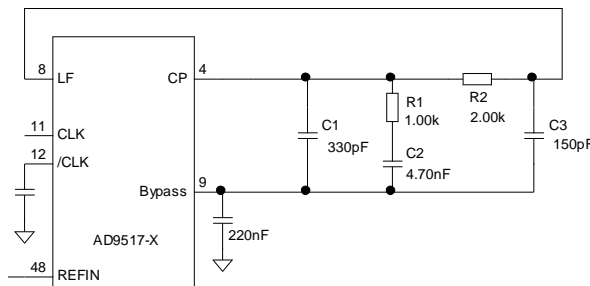


Figure 6: Loop filter design

4.10 Power supply

Power is supplied to the FMC card through the FMC connector. The pin current rating is 2.7A, but the overall maximum is limited according to Table 4.

| Voltage | # Pins | Max Amps | Max Watt |
|--------------|--------|----------|----------|
| +3.3V | 4 | 3 A | 10 W |
| +12V | 2 | 1 A | 12 W |
| VADJ | 4 | 4 A | 10 W |
| VIO_B (VADJ) | 2 | 1.15 A | 2.3 W |

Table 4: FMC standard power specification

The power provided by the carrier card can be very noisy. Special care is taken with the power supply generation on the FMC card to minimize the effect of power supply noise on clock generation and data conversion.

Clean +1.8V is derived from +3.3V with linear regulators. Clean +3.3V is derived from +12V in two steps for maximum efficiency. The first step uses a highly efficient switched regulator to generate a +3.8V power rail. From this power rail each analog supply is derived with separate low dropout, low noise, and linear regulators.

The regulators have sufficient copper area to dissipate the heat in combination with proper airflow (see section 6.3 Cooling).

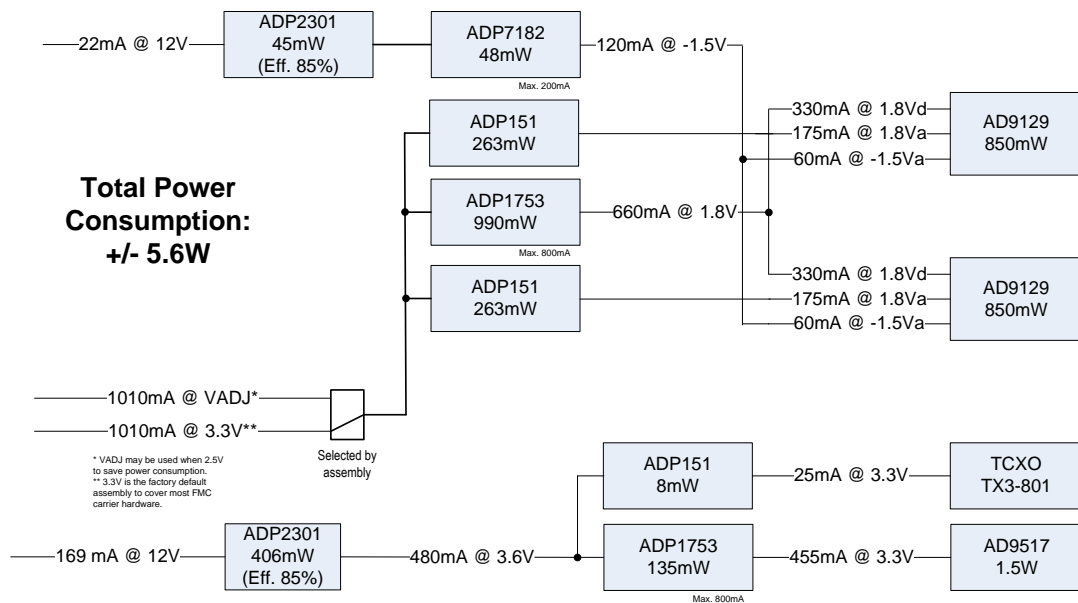


Figure 7: Power supply tree

| Power plane | Typical | Maximum |
|---------------------|---------------------|-----------|
| VADJ | $0.2A + I_{VIO_B}$ | - |
| 3P3V | 1.0A | 1.1A |
| 12P0V | 0.2A | 0.3A |
| 3P3VAUX (Operating) | 0.1 mA | 3 mA |
| 3P3VAUX (Standby) | 0.01 μ A | 1 μ A |

Table 5: Typical / Maximum current drawn from FMC carrier card

5 Controlling the FMC230

5.1 Architecture

The data interface of one DAC channel occupies 31 differential pairs on the FMC connector. Since one DAC channel is available on the LPC connections, there are only six signals left on the LPC connections to control the board. Therefore, the FMC will be controlled from a single SPI interface connecting to an onboard CPLD (Xilinx Coolrunner-II XC2C64A-QFG). Four connections are available between the FMC connector and the CPLD. The CPLD acts as a SPI distribution device and level translator and comes factory programmed. The two remaining signals on the FMC connector are reserved.

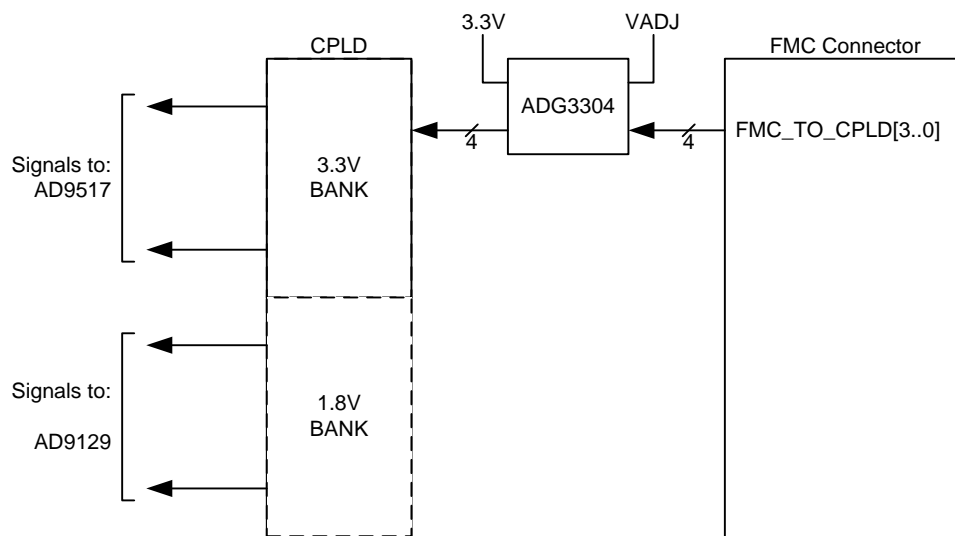


Figure 8: FMC control interface

The FMC is controlled from the carrier hardware through a single SPI communication bus. The SPI communication bus is connected to a CPLD which has the following tasks:

- Distribute SPI access from the carrier hardware along the local devices:
 - 2x AD9129 (D/A converters)
 - 1x AD9517 (Clock Tree)
- Enable/disable internal reference based on a SPI command from the carrier hardware (REF_EN)
- Generate SPI reset for AD9517 (CLK_N_RESET) and both AD9129 (DAC_RST)
- Collect local status signals and store them in a register which can be accessed from the carrier hardware
- Drive a LED according to the level of the status signals

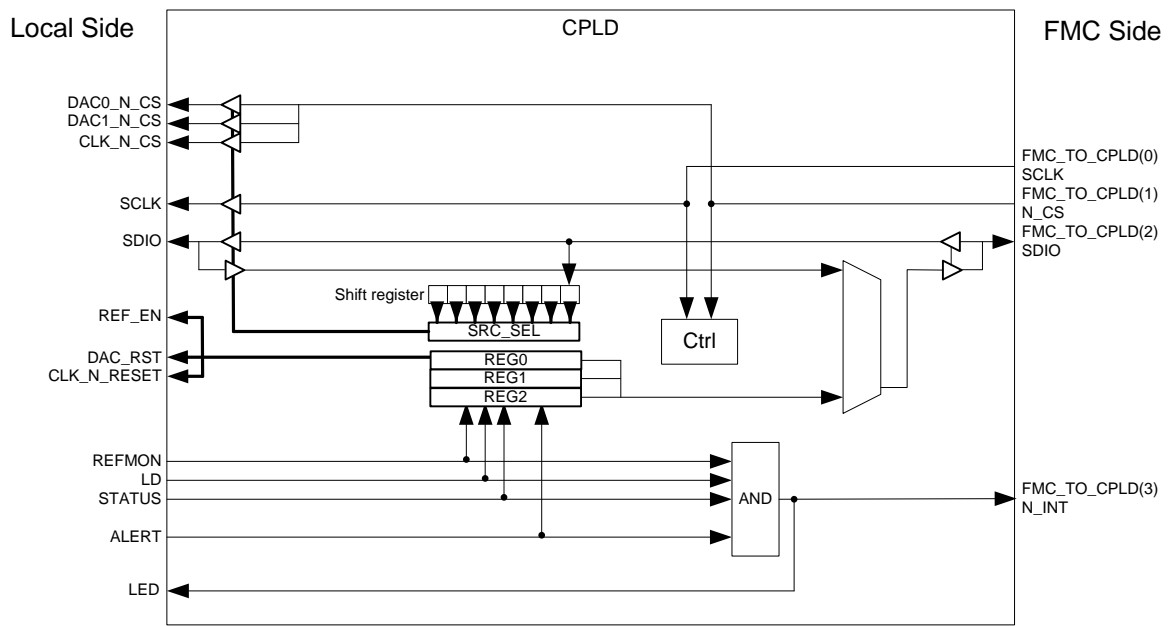


Figure 9: CPLD architecture

Notes:

- SDO on the AD9517 and AD9129 devices is not connected. SDIO is used bidirectional (3-wire SPI).

5.2 SPI Programming

The SPI programmable devices on the FMC can be accessed as described in their datasheet, but each SPI communication cycle needs to be preceded with a pre-selection byte. The pre-selection byte is used by the CPLD to forward the SPI command to the right destination. The pre-selection bytes are defined as follows:

- CPLD 0x00
- AD9129 #1 0x82
- AD9129 #2 0x83
- AD9517 0x84

The CLPD has three internal registers which are described in the Appendix. The registers of the other devices are transparently mapped.

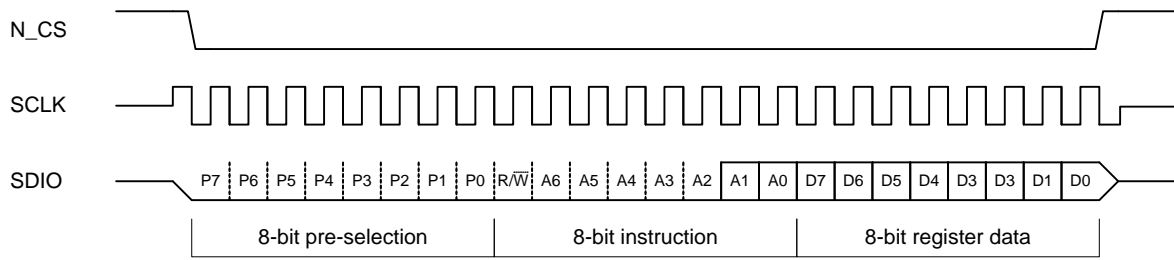


Figure 10: Write instruction to CPLD registers A1:A0

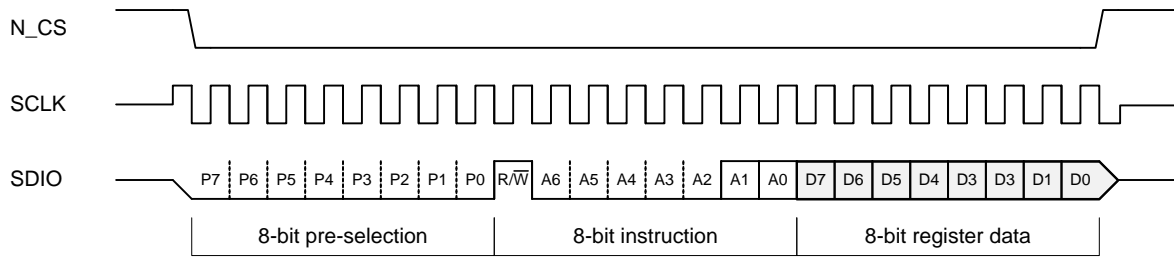


Figure 11: Read instruction to CPLD registers A1:A0

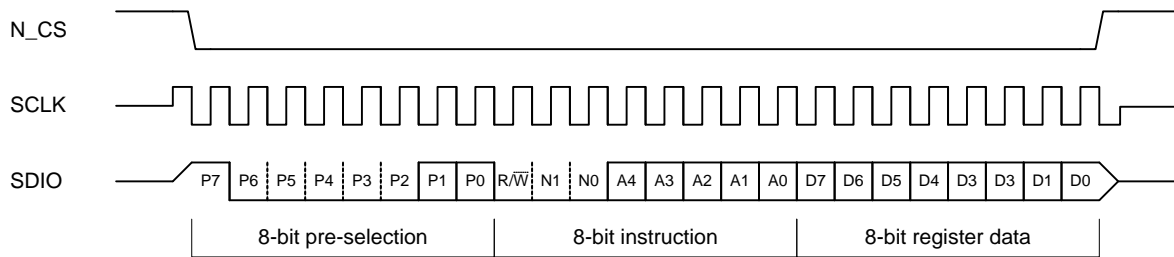


Figure 12: Write instruction to AD9129 registers A4:A0

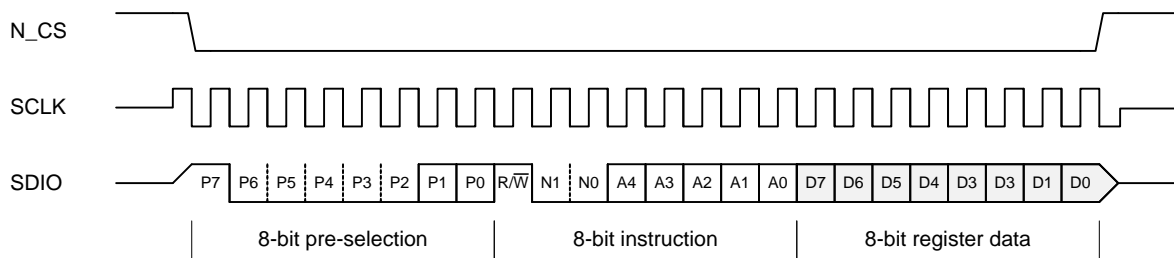


Figure 13: Read instruction to AD9129 registers A4:A0

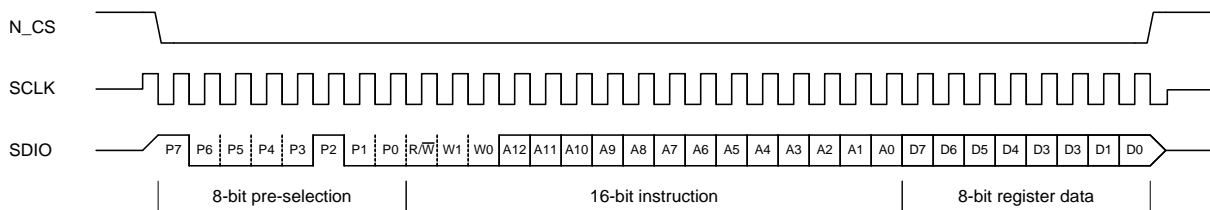


Figure 14: Write instruction to AD9517 registers A12:A0

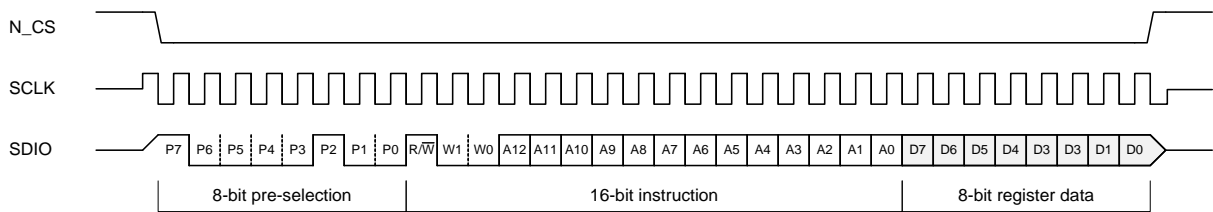


Figure 15: Read instruction to AD9517 registers A12:A0

6 Environment

6.1 Temperature

Operating temperature

- 40°C to +85°C (Industrial)

Storage temperature:

- 40°C to +120°C

6.2 Monitoring

The FMC holds an AD7291 device for monitoring several power supply voltages on the board as well as the temperature. The device can be programmed and read out through the I²C bus. Continuously operating the I²C bus might interfere with the conversion process and result in signal distortion. It is recommended to program the minimum and maximum limits in the monitoring devices and only read from the devices when the interrupt line is asserted. It is recommended that the carrier card and/or host software uses the power-down features in the case the temperature is too high.

| Parameter: | Device 1 address 010 1111 (GA=00) address 010 1100 (GA=01) address 010 0011 (GA=10) address 010 0000 (GA=11) | Formula |
|---------------------|--|----------------|
| On-chip temperature | | |
| External VIN0 | 1.8Va DAC | VIN0 * 1 |
| External VIN1 | 1.8Vd DAC | VIN1 * 1 |
| External VIN2 | 1.8Va | VIN2 * 1 |
| External VIN3 | 1.8Vd | VIN3 * 1 |
| External VIN4 | 3V3 CLK | VIN4 * 2 |
| External VIN5 | 3V3 TCXO | VIN5 * 2 |
| External VIN6 | VADJ | VIN6 * 2 |
| External VIN7 | -1V5 | 3.3 - 2 * VIN7 |

Table 6: Temperature and voltage parameters

6.3 Cooling

Two different types of cooling are available for the FMC.

6.3.1 Convection cooling

The air flow provided by the fans of the chassis the FMC is enclosed in will dissipate the heat generated by the on board components. A minimum airflow of 300 LFM is recommended.

For standalone operations (such as on a Xilinx development kit), it is highly recommended to blow air across the FMC and ensure that the temperature of the devices is within the allowed range. 4DSP's warranty does not cover boards on which the maximum allowed temperature has been exceeded.

6.3.2 Conduction cooling

In demanding environments, the ambient temperature inside a chassis could be close to the operating temperature defined in this document. It is very likely that in these conditions the junction temperature of power consuming devices will exceed the operating conditions recommended by the device manufacturers (mostly +85°C). While a low profile heat sink coupled with sufficient air flow might be sufficient to maintain the temperature within operating boundaries, some active cooling would yield better results and would certainly help with resuming operations much faster in the case the devices were disabled because of a temperature "over range".

7 Safety

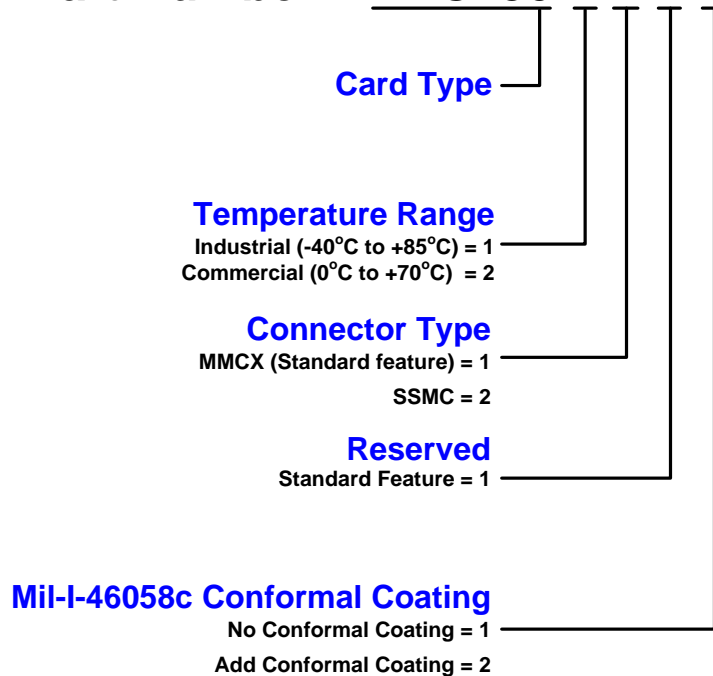
This module presents no hazard to the user.

8 EMC

This module is designed to operate within an enclosed host system built to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system. This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the system.

9 Ordering information

Part Number: FMC230-2-1-1-1



10 Warranty

| | <i>Hardware</i> | <i>Software/Firmware</i> |
|------------------------------|-------------------------------|-------------------------------|
| Basic Warranty (included) | 1 Year from Date of Shipment | 90 Days from Date of Shipment |
| Extended Warranty (optional) | 2 Years from Date of Shipment | 1 Year from Date of Shipment |

Appendix A LPC / HPC pin-out

- Note that FMC700 is required to use the FMC230 on KC705

| AV57.1 | HPC Pin | FMC230 Signal | AV57.1 | HPC Pin | FMC230 Signal | AV57.1 | HPC Pin | FMC230 Signal |
|--------------|---------|----------------|-----------|---------|----------------|-----------|---------|----------------|
| CLK0_M2C_N | H5 | CLK_TO_FPGA_N | HA00_N_CC | F5 | DAC1_DCO_N | HB00_N_CC | K26 | DAC1_P1_DP05_N |
| CLK0_M2C_P | H4 | CLK_TO_FPGA_P | HA00_P_CC | F4 | DAC1_DCO_P | HB00_P_CC | K25 | DAC1_P1_DP05_P |
| CLK1_M2C_N | G3 | EXT_TRIGGER_N | HA01_N_CC | E3 | DAC1_DCI_N | HB01_N | J25 | DAC1_P1_DP04_N |
| CLK1_M2C_P | G2 | EXT_TRIGGER_P | HA01_P_CC | E2 | DAC1_DCI_P | HB01_P | J24 | DAC1_P1_DP04_P |
| CLK2_BIDIR_N | K5 | N.C. | HA02_N | K8 | DAC1_FRM_N | HB02_N | F23 | DAC1_P1_DP03_N |
| CLK2_BIDIR_P | K4 | N.C. | HA02_P | K7 | DAC1_FRM_P | HB02_P | F22 | DAC1_P1_DP03_P |
| CLK3_BIDIR_N | J3 | N.C. | HA03_N | J7 | DAC1_PO_DP00_N | HB03_N | E22 | DAC1_P1_DP02_N |
| CLK3_BIDIR_P | J2 | N.C. | HA03_P | J6 | DAC1_PO_DP00_P | HB03_P | E21 | DAC1_P1_DP02_P |
| LA00_N_CC | G7 | DACO_DCO_N | HA04_N | F8 | DAC1_PO_DP01_N | HB04_N | F26 | DAC1_P1_DP01_N |
| LA00_P_CC | G6 | DACO_DCO_P | HA04_P | F7 | DAC1_PO_DP01_P | HB04_P | F25 | DAC1_P1_DP01_P |
| LA01_N_CC | D9 | DACO_DCI_N | HA05_N | E7 | DAC1_PO_DP02_N | HB05_N | E25 | DAC1_P1_DP00_N |
| LA01_P_CC | D8 | DACO_DCI_P | HA05_P | E6 | DAC1_PO_DP02_P | HB05_P | E24 | DAC1_P1_DP00_P |
| LA02_N | H8 | DACO_FRM_N | HA06_N | K11 | DAC1_PO_DP04_N | HB06_N_CC | K29 | DAC1_P1_DP06_N |
| LA02_P | H7 | DACO_FRM_P | HA06_P | K10 | DAC1_PO_DP04_P | HB06_P_CC | K28 | DAC1_P1_DP06_P |
| LA03_N | G10 | DACO_PO_DP00_N | HA07_N | J10 | DAC1_PO_DP03_N | HB07_N | J28 | DAC1_P1_DP07_N |
| LA03_P | G9 | DACO_PO_DP00_P | HA07_P | J9 | DAC1_PO_DP03_P | HB07_P | J27 | DAC1_P1_DP07_P |
| LA04_N | H11 | DACO_PO_DP01_N | HA08_N | F11 | DAC1_PO_DP05_N | HB08_N | F29 | DAC1_P1_DP09_N |
| LA04_P | H10 | DACO_PO_DP01_P | HA08_P | F10 | DAC1_PO_DP05_P | HB08_P | F28 | DAC1_P1_DP09_P |
| LA05_N | D12 | DACO_PO_DP02_N | HA09_N | E10 | DAC1_PO_DP06_N | HB09_N | E28 | DAC1_P1_DP08_N |
| LA05_P | D11 | DACO_PO_DP02_P | HA09_P | E9 | DAC1_PO_DP06_P | HB09_P | E27 | DAC1_P1_DP08_P |
| LA06_N | C11 | DACO_PO_DP03_N | HA10_N | K14 | DAC1_PO_DP09_N | HB10_N | K32 | DAC1_P1_DP11_N |
| LA06_P | C10 | DACO_PO_DP03_P | HA10_P | K13 | DAC1_PO_DP09_P | HB10_P | K31 | DAC1_P1_DP11_P |
| LA07_N | H14 | DACO_PO_DP04_N | HA11_N | J13 | DAC1_PO_DP08_N | HB11_N | J31 | DAC1_P1_DP10_N |
| LA07_P | H13 | DACO_PO_DP04_P | HA11_P | J12 | DAC1_PO_DP08_P | HB11_P | J30 | DAC1_P1_DP10_P |
| LA08_N | G13 | DACO_PO_DP05_N | HA12_N | F14 | DAC1_PO_DP07_N | HB12_N | F32 | DAC1_P1_DP13_N |
| LA08_P | G12 | DACO_PO_DP05_P | HA12_P | F13 | DAC1_PO_DP07_P | HB12_P | F31 | DAC1_P1_DP13_P |
| LA09_N | D15 | DACO_PO_DP06_N | HA13_N | E13 | DAC1_PO_DP10_N | HB13_N | E31 | DAC1_P1_DP12_N |
| LA09_P | D14 | DACO_PO_DP06_P | HA13_P | E12 | DAC1_PO_DP10_P | HB13_P | E30 | DAC1_P1_DP12_P |
| LA10_N | C15 | DACO_PO_DP09_N | HA14_N | J16 | DAC1_PO_DP11_N | HB14_N | K35 | |
| LA10_P | C14 | DACO_PO_DP09_P | HA14_P | J15 | DAC1_PO_DP11_P | HB14_P | K34 | |
| LA11_N | H17 | DACO_PO_DP08_N | HA15_N | F17 | DAC1_PO_DP12_N | HB15_N | J34 | |
| LA11_P | H16 | DACO_PO_DP08_P | HA15_P | F16 | DAC1_PO_DP12_P | HB15_P | J33 | |
| LA12_N | G16 | DACO_PO_DP07_N | HA16_N | E16 | DAC1_PO_DP13_N | HB16_N | F35 | |
| LA12_P | G15 | DACO_PO_DP07_P | HA16_P | E15 | DAC1_PO_DP13_P | HB16_P | F34 | |
| LA13_N | D18 | DACO_PO_DP10_N | HA17_N_CC | K17 | DAC1_SYNC | HB17_N_CC | K38 | |
| LA13_P | D17 | DACO_PO_DP10_P | HA17_P_CC | K16 | DACO_SYNC | HB17_P_CC | K37 | |
| LA14_N | C19 | DACO_PO_DP13_N | HA18_N | J19 | | HB18_N | J37 | |
| LA14_P | C18 | DACO_PO_DP13_P | HA18_P | J18 | | HB18_P | J36 | |
| LA15_N | H20 | DACO_PO_DP12_N | HA19_N | F20 | | HB19_N | E34 | |
| LA15_P | H19 | DACO_PO_DP12_P | HA19_P | F19 | | HB19_P | E33 | |
| LA16_N | G19 | DACO_PO_DP11_N | HA20_N | E19 | | HB20_N | F38 | |
| LA16_P | G18 | DACO_PO_DP11_P | HA20_P | E18 | | HB20_P | F37 | |
| LA17_N_CC | D21 | DACO_P1_DP00_N | HA21_N | K20 | | HB21_N | E37 | |
| LA17_P_CC | D20 | DACO_P1_DP00_P | HA21_P | K19 | | HB21_P | E36 | |

| | | | | | | | | |
|-----------|-----|----------------|--------|-----|--|---------|-----|---------|
| LA18_N_CC | C23 | DACO_P1_DP01_N | HA22_N | J22 | | | | |
| LA18_P_CC | C22 | DACO_P1_DP01_P | HA22_P | J21 | | | | |
| LA19_N | H23 | DACO_P1_DP03_N | HA23_N | K23 | | | | |
| LA19_P | H22 | DACO_P1_DP03_P | HA23_P | K22 | | | | |
| LA20_N | G22 | DACO_P1_DP02_N | | | | | | |
| LA20_P | G21 | DACO_P1_DP02_P | | | | | | |
| LA21_N | H26 | DACO_P1_DP05_N | | | | | | |
| LA21_P | H25 | DACO_P1_DP05_P | | | | | | |
| LA22_N | G25 | DACO_P1_DP04_N | | | | | | |
| LA22_P | G24 | DACO_P1_DP04_P | | | | | | |
| LA23_N | D24 | DACO_P1_DP06_N | | | | | | |
| LA23_P | D23 | DACO_P1_DP06_P | | | | | | |
| LA24_N | H29 | DACO_P1_DP10_N | | | | | | |
| LA24_P | H28 | DACO_P1_DP10_P | | | | | | |
| LA25_N | G28 | DACO_P1_DP09_N | | | | | | |
| LA25_P | G27 | DACO_P1_DP09_P | | | | | | |
| LA26_N | D27 | DACO_P1_DP07_N | | | | | | |
| LA26_P | D26 | DACO_P1_DP07_P | | | | | | |
| LA27_N | C27 | DACO_P1_DP08_N | | | | | | |
| LA27_P | C26 | DACO_P1_DP08_P | | | | | | |
| LA28_N | H32 | DACO_P1_DP12_N | | | | | | |
| LA28_P | H31 | DACO_P1_DP12_P | | | | | | |
| LA29_N | G31 | DACO_P1_DP11_N | | | | | | |
| LA29_P | G30 | DACO_P1_DP11_P | | | | | | |
| LA30_N | H35 | DACO_P1_DP13_N | | | | | | |
| LA30_P | H34 | DACO_P1_DP13_P | | | | | | |
| LA31_N | G34 | FMC_TO_CPLD(1) | | | | | | |
| LA31_P | G33 | FMC_TO_CPLD(0) | | | | CLK_DIR | B1 | |
| LA32_N | H38 | FMC_TO_CPLD(3) | | | | PG_C2M | D1 | PG_C2M |
| LA32_P | H37 | FMC_TO_CPLD(2) | | | | PG_M2C | F1 | PG_M2C |
| LA33_N | G37 | | | | | I2C_SCL | C30 | I2C_SCL |
| LA33_P | G36 | | | | | I2C_SDA | C31 | I2C_SDA |

Table 7: FMC230 Pinout

| Signal | Group | Direction | I/O standard | Description |
|------------|-------|-----------|--------------|---|
| DACO_DCO_P | D/A 0 | Output | LVDS | Clock coming from the 1st D/A converter. |
| DACO_DCO_N | | | | |
| DACO_SYNC | D/A 0 | Output | 1.8V CMOS | Sync output, when enabled this output is DACCLK/8. Only available on r1.2 boards or later |
| DACO_DCI_P | D/A 0 | Input | LVDS | Clock going to the 1st D/A converter. |
| DACO_DCI_N | | | | |
| DACO_FRM_P | D/A 0 | Input | LVDS | Frame going to the 1st D/A converter. |
| DACO_FRM_N | | | | |

| | | | | |
|-------------------|---------|--------|-----------|---|
| DAC0_P0_P<13..0> | D/A 0 | Input | LVDS | Data bus 0 going to the 1st D/A converter. |
| DAC0_P0_N<13..0> | | | | |
| DAC0_P1_P<13..0> | D/A 0 | Input | LVDS | Data bus 1 going to the 1st D/A converter. |
| DAC0_P1_N<13..0> | | | | |
| DAC1_DCO_P | D/A 1 | Output | LVDS | Clock coming from the 2nd D/A converter. |
| DAC1_DCO_N | | | | |
| DAC1_SYNC | D/A 1 | Output | 1.8V CMOS | Sync output, when enabled this output is DACCLK/8. Only available on r1.2 boards or later |
| DAC1_DCI_P | D/A 1 | Input | LVDS | Clock going to the 2nd D/A converter. |
| DAC1_DCI_N | | | | |
| DAC1_FRM_P | D/A 1 | Input | LVDS | Frame going to the 2nd D/A converter. |
| DAC1_FRM_N | | | | |
| DAC1_P0_P<13..0> | D/A 1 | Input | LVDS | Data bus 0 going to the 2nd D/A converter. |
| DAC1_P0_N<13..0> | | | | |
| DAC1_P1_P<13..0> | D/A 1 | Input | LVDS | Data bus 1 going to the 2nd D/A converter. |
| DAC1_P1_N<13..0> | | | | |
| CLK_TO_FPGA_P | I/O | Output | LVDS | Clock coming from the clock tree. Typically used for debug and monitoring purposes. |
| CLK_TO_FPGA_N | | | | |
| EXT_TRIGGER_P | I/O | Output | LVDS | Representation of the external trigger signal. |
| EXT_TRIGGER_N | | | | |
| FMC_TO_CPLD<3..0> | CONTROL | Bidir | CMOS VIO | SPI bus to CPLD on the FMC176: FMC_TO_CPLD(0): SPI Clock FMC_TO_CPLD(1): SPI Chip Select (low active) FMC_TO_CPLD(2): SPI Data In/Out FMC_TO_CPLD(3): SPI Alert/Interrupt |
| CLK_DIR | CONTROL | Output | LVTTTL | CLK_DIR is not connected. CLK2 and CLK3 are unused. |
| PG_C2M | STATUS | Input | LVTTTL | Power good indicator from carrier to module. |
| PG_M2C | STATUS | Output | LVTTTL | Power good indicator from module to carrier. |
| I2C_SCL | I2C | Input | LVTTTL | I2C clock line. |
| I2C_SDA | I2C | Bidir | LVTTTL | I2C data line. |

Table 8: FMC230 Signal Description

Appendix B CPLD Register map

| Register | | Description |
|-------------|----------|---|
| 0x00 | | Control register 0 |
| | Bit 0 | '0' for internal reference clock '1' for external reference clock (disable internal reference) |
| | Bit 1 | Reserved |
| | Bit 2 | '0' Release DAC reset '1' Assert DAC reset |
| | Bit 3 | '0' Release CLK reset (AD9517) '1' Assert CLK reset (AD9517) |
| | Bit 4 | '0' Release CLK sync (AD9517) '1' Assert CLK sync (AD9517) |
| | Bit 6..5 | Reserved |
| | Bit 7 | EEPROM write enable. Recommended to write '0'. |
| 0x01 | | Control register 1 |
| | Bit 0 | Reserved |
| R/O | Bit 1 | Reserved |
| R/O | Bit 2 | Reserved |
| | Bit 3 | Reserved |
| R/O | Bit 4 | Reserved |
| R/O | Bit 5 | Reserved |
| | Bit 6 | '0' for CLK power enable (AD9517) '1' for CLK power down (AD9517) |
| | Bit 7 | '0' for MONITORING power enable (AD7291 rst_) '1' for MONITORING power down (AD7291 rst_) |
| 0x02 | | Status register |
| | Bit 0 | REFMON (AD9517) |
| | Bit 1 | LD (AD9517) |
| | Bit 2 | STATUS (AD9517) |
| | Bit 3 | ALERT (AD7291) |
| | Bit 4 | IRQ (DAC) |
| | Bit 7..5 | CPLD revision (current = b'001') |

Table 9: CPLD Register Map