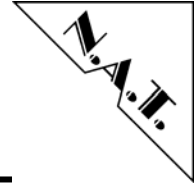**NAMC-STM1/4**
Telecom AMC Module
Technical Reference Manual V1.3
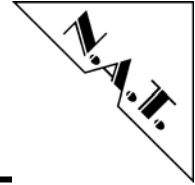**HW Revision 1.4**

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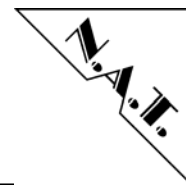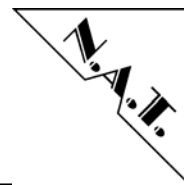
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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.

Table 1 gives a list of the abbreviations used in this document:

Table 1: List of used abbreviations

Abbreviation	Description
b	Bit, binary
B	byte
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
DDR	Dual Data Rate
DMA	Direct Memory Access
DRAM	Dynamic RAM
E1	2.048 Mbit G.703 Interface
FLASH	Reprogrammable ROM
FPGA	Field Programmable Gate Array
H.110	Time-Slot Interchange Bus
iTDM	internal TDM
J1	1,544 Mbit G.703 Interface (Japan)
LIU	Line Interface Unit
MCH	µTCA Carrier Hub
MPC8560	Embedded Processor from Freescale
µTCA	Micro Telecommunications Computing Architecture
PCIe	PCI Express
PCI-X	Extended PCI
RAM	Random Access Memory
ROM	Read Only Memory
SDRAM	Synchronous Dynamic RAM
SMC	Serial Communication Controller of the MPC8560
T1	1,544 Mbit G.703 Interface (USA)
TDM	Time Division Multiplex
TSI	Time Slot Interchange
TSA	Time Slot Assigner
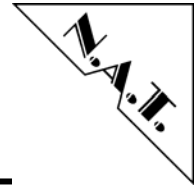
1 Introduction

The **NAMC-STM1/4** is a high performance standard Advanced Mezzanine Card, single width, double height for SDH/Sonet applications. It can be plugged onto any ATCA carrier board supporting AMC standards. It is also designed to meet the requirements of µTCA systems.

General features:
- Dual Optical Interface for STM1/4 / OC3/12 at 155/622 Mbit/sec
- Add/Drop Multiplexer for up to 4*63=252E1 / 4*84=336T1 Channels
- 63 E1 Framers or 84 T1 Framers per Temux device (up to 4 assembled)
- Multiplexer cross connect between STM1/4 E1/T1 payload timeslots and iTDM timeslots (capacity limited to one STM4)
- 1 Lane PCI Express Interface Rev. 1.1
- 1000BaseBX iTDM Interface
- H.110 alike Backplane TDM bus
- Configuration/Control via PCIe or via Ethernet

Features of the Line Interface Circuits:
- Clock recovery and jitter attenuation
- Line and path performance monitoring

Features of the iTDM circuit:
- Flexible routing of any time slot between each of the framers and the iTDM controller
- Capacity of up to 8192 timeslots

Options:
- Single or Dual Optical Interface
- Single – or Multi-Mode optical Transceiver
- Monitoring Version (dual add/drop multiplexer) for concurrent Rx/Tx monitoring
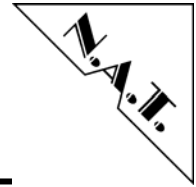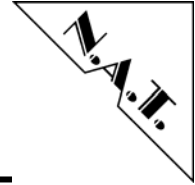
Figure 1 shows a detailed block diagram of the NAMC-STM1/4.

Figure 1:   NAMC-STM1/4 Block Diagram
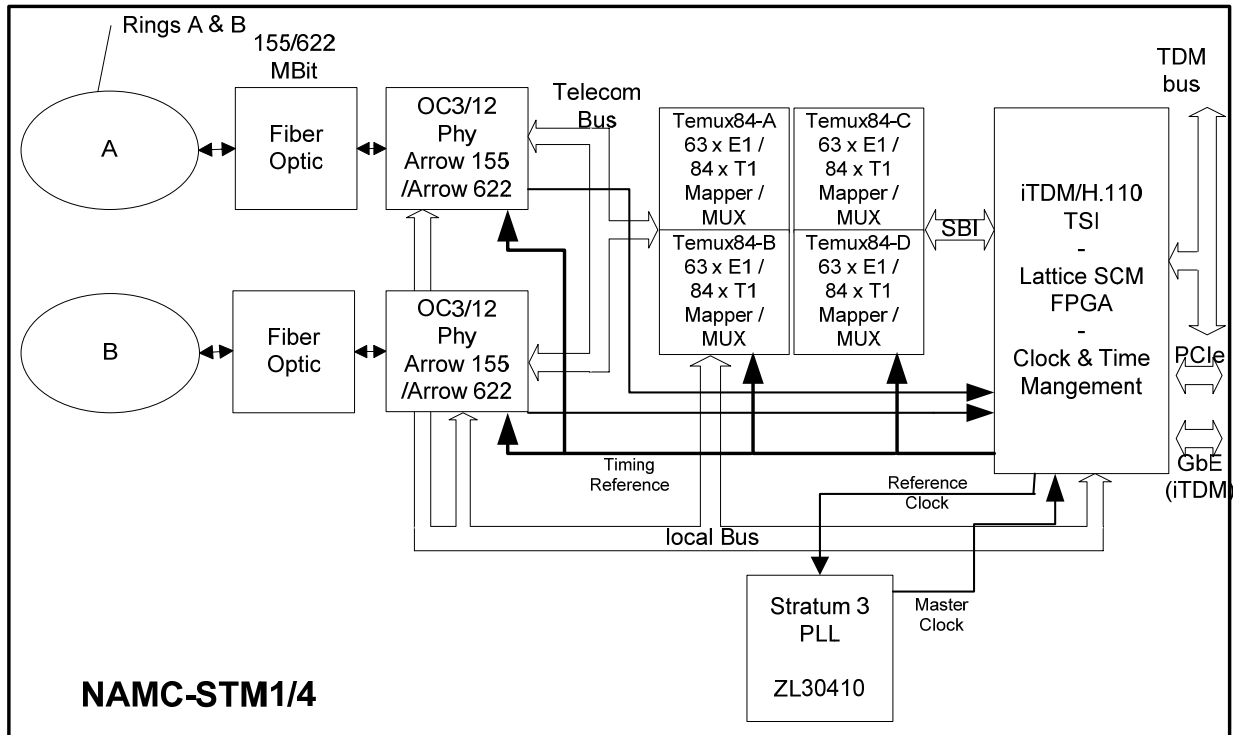
1.1 Board Features

1.1.1 FPGA

The central component on the **NAMC-STM1/4** is a Lattice SCM FPGA (SCM40 or SCM80). This device features built-in SerDes units used to realize the physical layer of the PCIe and the GbE interfaces, as well as a structured ASIC region used to implement the higher layers of the PCIe interface.
The logic resources are used to realize the iTDM engine along with the management interface and further functionality related to the SDH chipset.

1.1.2 SDH Interfaces

The STM1/4 / OC3/12 interface consists of the Fiber Optic interface and the Sonet/SDH framer. The PMC-Sierra device Arrow-155 is used as Sonet/SDH framer for the STM1 option, the Arrow-622 as framer for the STM4 option.
The Arrow-155 is a single port Sonet/SDH framer supporting the OC-3 (STM-1) data rates. The Arrow-155 terminates section, line and path overhead of both the STS-n (AU-4) level and the TU-3 level. On the line side it incorporates a SERDES, allowing it to mate directly to an optics module. The system side interface is an 8-bit multi-drop parallel Telecom bus, allowing multiple devices to share a single bus. The Arrow-155 maps/demaps up to three channels of DS3, E3, or EC-1 with bi-directional monitoring of traffic. The traffic may be multiplexed either into the system side or line side interfaces.
For the STM4 option, the board is equipped with an Arrow-622 device.

1.1.3 Backplane Interfaces

PCIe: The **NAMC-STM1/4** includes a x1-PCI Express interface. This is implemented in the Lattice FPGA. The PCI Express interface connects to Port 4/8 of the Fat Pipe Region of the AMC backplane connector (can be switched over to support redundant system setups). The implementation of PCIe conforms to the AMC.1 specification.

GbE: The **NAMC-STM1/4** implements a serial Type P Control Path, the physical layer of which is 1000BaseX. The Type P Control Path connects to Port 0/1 of the Common Options Region of the AMC backplane connector (can be switched over to support redundant system setups). The Control Path is connected to the iTDM FPGA, and shares the port with iTDM.

iTDM: The **NAMC-STM1/4** implements a serial iTDM backplane interface, the physical layer of which is 1000BaseX. The iTDM interface connects to Port 0/1 of the Common Options Region of the AMC backplane connector, and shares the port with the Type P Control Path. The iTDM
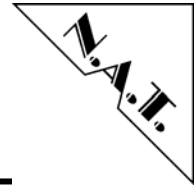
interface is implemented in FPGA logic and conforms to the SFP.0 and SFP.1 specifications.

IPMB: The **NAMC-STM1/4** implements an IPMB interface which conforms to the AMC.0 specification.

TDM: The **NAMC-STM1/4** implements an 8 bit TDM interface, similar to H.110. The same throughput as with a complete H.110 bus is achieved by clocking the 8 backplane TDM lines with 32,768 MHz. Thus, every frame consists of 512 timeslots per line. The purpose of this TDM backplane bus is to establish 'private' TDM links to adjacent modules. The TDM interface is implemented in FPGA logic. The TDM interface connects to ports 12, 13 (data), and port 14 (Sync) of the Common Options Region of the AMC connector.
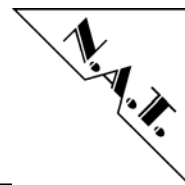
1.2 Board Specification

Table 2: NAMC-STM1/4 Features

AMC-Module	standard Advanced Mezzanine Card, single width, double height
Front-I/O	Two optical 155/622Mbps OC-3/12 STM-1 line interfaces
Power consumption	12V 1.3A max.

Environmental conditions	Temperature (operating):	0°C to +50°C with forced cooling
	Temperature (storage):	-40°C to +85°C
	Humidity:	10 % to 90 % rh noncondensing
Standards compliance	PICMG AMC.0 Rev. 2.0	
	PICMG AMC.1 Rev. 1.0	
	PCI Express Base Specification Rev. 1.1	
	PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format)	
	PICMG SFP.1 Rev. 1.0 (Internal TDM)	
	IPMI Specification v2.0 Rev. 1.0	
	PICMG µTCA.0 Rev. 1.0	
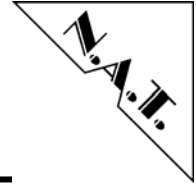
2 Installation

2.1 Safety Note

To ensure proper functioning of the **NAMC-STM1/4** during its usual lifetime take the following precautions before handling the board.

CAUTION

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime.

- Before installing or uninstalling the **NAMC-STM1/4** read this installation section
- Before installing or uninstalling the **NAMC-STM1/4**, read the Installation Guide and the User's Manual of the carrier board used, or of the uTCA system the board will be plugged into.
- Before installing or uninstalling the **NAMC-STM1/4** on a carrier board or both in a rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power.
  - Take those steps.
  - Finally turn on or off the power if necessary.
  - Make sure the part to be installed / removed is hot swap capable, if you don't switch off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NAMC-STM1/4** is connected to the carrier board or to the uTCA backplane with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing
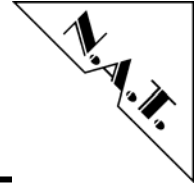
2.2 Installation Prerequisites and Requirements

IMPORTANT

Before powering up
- check this section for installation prerequisites and requirements

2.2.1 Requirements

The installation requires only
- an ATCA carrier board, or a µTCA backplane for connecting the **NAMC-STM1/4**
- power supply
- cooling devices

2.2.2 Power supply

The power supply for the **NAMC-STM1/4** must meet the following specifications:
- required for the module:
  +12V / 1.3A max.
  + 3,3V / 0.15A max.

2.2.3 Automatic Power Up

In the following situations the **NAMC-STM1/4** will automatically be reset and proceed with a normal power up.

Voltage sensors

The voltage sensor generates a reset
- when +12V voltage level drops below 8V
- when +3.3V voltage level drops below 3.08V

or when the carrier board / backplane signals a PCIe Reset.
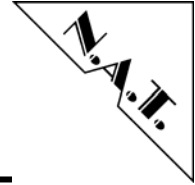
2.3 Statement on Environmental Protection

2.3.1 Compliance to RoHS Directive

Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

2.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.
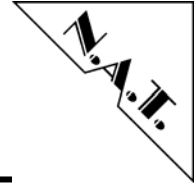
As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

2.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

2.3.4 Product Safety

The board complies with EN60950 and UL1950.

3   Functional Blocks

The **NAMC-STM1/4** can be divided into a number of functional blocks, which are described in the following paragraphs.

3.1.1 FPGA

The FPGA implements the following functional blocks:
- Logic to interface the SBI bus; clock management for the SDH chipset
- iTDM controller with GbE.
- PCIe interface for management
- Management over GbE
- Legacy TSI between SBI timeslots and backplane TDM bus

3.1.2 PCI Express Interface

The **NAMC-STM1/4** includes a 1 lane PCI Express interface. This is implemented in the Lattice SCM FPGA. The PCIe interface may receive its reference clock either from the Clock 3 port of the AMC backplane connector, or from a local 100 MHz oscillator circuitry (default). The clock source is programmable.

3.1.3 Backplane Ethernet

The backplane Ethernet interface implemented within the FPGA can be switched to operate on AMC Port 0 or Port 1 for redundant operation. Within FPGA logic the Type P Control Path data is multiplexed with the iTDM data and transferred through the same physical port. By default, the LIU is programmed to connect to Port 0 of the Common Options Region of the AMC backplane connector. It can also be programmed to connect to Port 1, in order to support a redundant µTCA system.

3.1.4 iTDM

The iTDM controller within the FPGA can be used to transfer any of the SDH timeslots via GbE packets. It supports mixed operation in either 125µs mode or 1ms mode. The capacity is limited to 8192 timeslots, due to the available bandwidth of the GbE link.

Figure 2:   Organisation of the iTDM FPGA
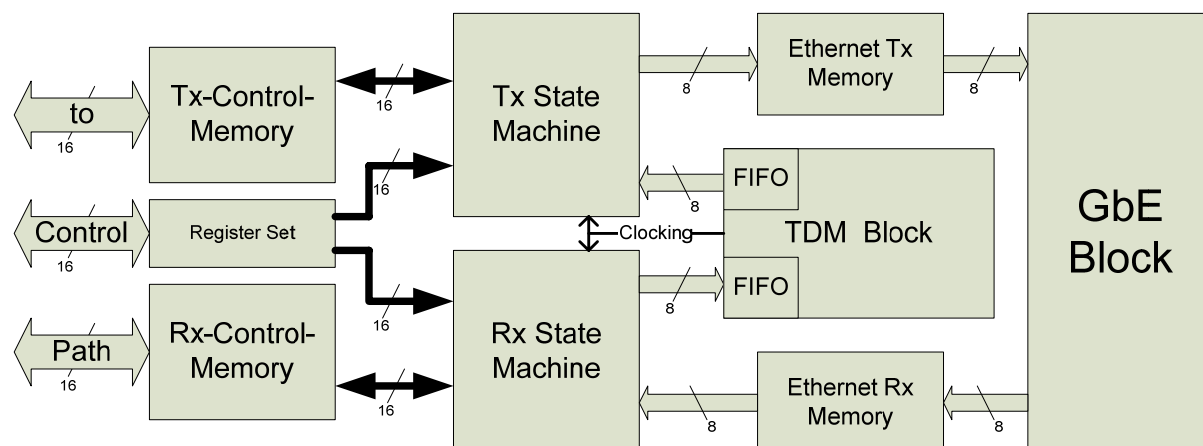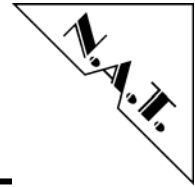
3.1.5 Backplane TDM

The **NAMC-STM1/4** implements an 8 bit TDM interface, similar to H.110. The same throughput as with a complete H.110 bus is achieved by clocking the 8 backplane TDM lines with 32,768 MHz. Thus, every frame consists of 512 timeslots per line. The purpose of this TDM backplane bus is to establish 'private' TDM links to adjacent modules. The TDM interface is implemented in FPGA logic. The TDM interface connects to ports 12, 13 (data), and port 14 (Sync) of the Extended Options Region of the AMC connector.

3.2 SDH Line Interfaces

The two optical 155/622Mbps OC-3/12 STM-1 line interfaces are available on two standard OC-3/12 SDH/STM-1 SC-connectors at the front panel.

3.3 AMC Clock Interface

The **NAMC-STM1/4** implements a very flexible clocking functionality concerning the AMC backplane clock ports Clock 1 – Clock 3.

AMC backplane clock port Clock 1 is connected to the FPGA, in order to be used as a Telecom standard clock. Clock 1 is only received.

AMC backplane clock port Clock 2 is connected to the FPGA, in order to be used as a Telecom standard reference. Clock 2 may be received from or transmitted to the backplane, in order to become the reference clock for the entire system.

AMC backplane clock port Clock 3 is connected to the PCIe interface, in order to be used as a reference clock for PCI Express. Clock 3 is only received. Clock 3 is routed to a multiplexer, which allows programming the clock source of the PCIe line to be either Clock 3, or an internal differential 100 MHz reference clock.

In case clock 3 is to be used for a different functionality, it also feeds the FPGA and may be used there for any suitable purpose.
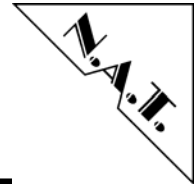
3.4 IPMB Interface

The **NAMC-STM1/4** implements an IPMB interface consisting of an ATMega168 microcontroller and a couple of I2C devices, such as a temperature sensor, and an EEPROM. The IPMB controller manages also the hot swap functionality and the geographical address as requested by the AMC specification.

3.4.1 I^{2}C Devices

Three I^{2}C busses connect to the IPMI controller. The first one is the IPMB bus of the AMC connector, and the two other interface various local devices. The local devices, all powered by IPMB power, are an EEPROM (24C08) for storage of board-specific information, and a temperature sensor, which is capable of reading the FPGA's die temperature. The third local I²C device is the hotswap controller of the NAMC-STM1/4.

Figure 3: I²C Structure of the NAMC-STM1/4
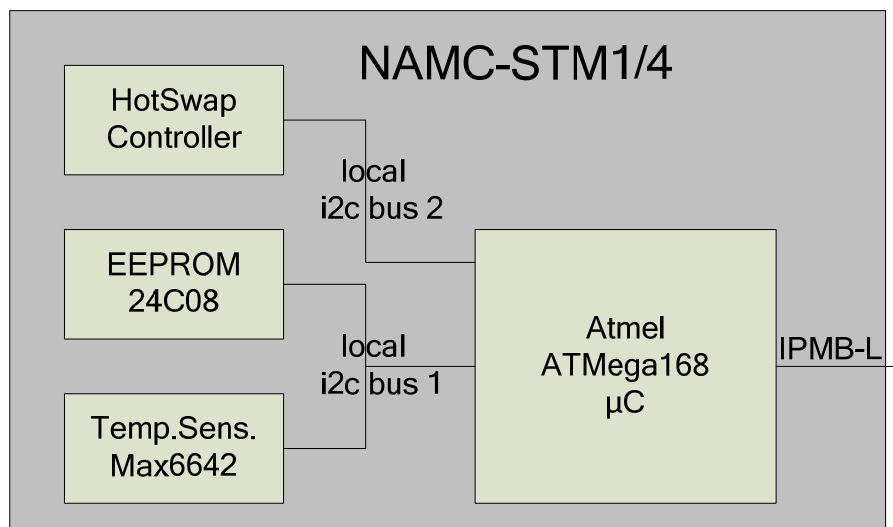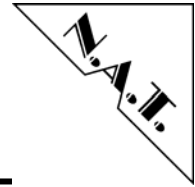
4 Hardware

4.1 AMC Port Definition

Table 3: AMC Port Definition

	Port No.	AMC Port Mapping Strategy	Ports used as
Basic Connector	CLK1	Clocks	Reference Clock 1
	CLK2		Reference Clock 2
	CLK3		Reference Clock 3
	0	Common Options Region	1000BaseX Ethernet Channel 1 (iTDM and Type P), default
	1		1000BaseX Ethernet Channel 2 (iTDM and Type P), redundant
	2		unassigned
	3		unassigned
	4	Fat Pipes Region	PCI Express Lane 0, default
	5		unassigned
	6		unassigned
	7		unassigned
Extended Connector	8		PCI Express Lane 0, redundant
	9		unassigned
	10		unassigned
	11		unassigned
	12	Extended Options Region	TDM Bus D0-3 (H.110 extended)
	13		TDM Bus D4-7 (H.110 extended)
	14		optional clock lines (H.110 extended)/ unassigned
	15		Unassigned
	CLK4/5		Unassigned
	17		Unassigned
	18		Unassigned
	19		Unassigned
	20		Unassigned

4.2 Front Panel and LEDs

The **NAMC-STM1/4** module is equipped with 4 LEDs, which are software programmable. They are mounted between the SDH connectors.
Additionally it features the standard four AMC LEDs, with the red and blue LED being controlled by the IPMB-µC, and the green and yellow one being controlled via FPGA registers.

Figure 4:   Front Panel
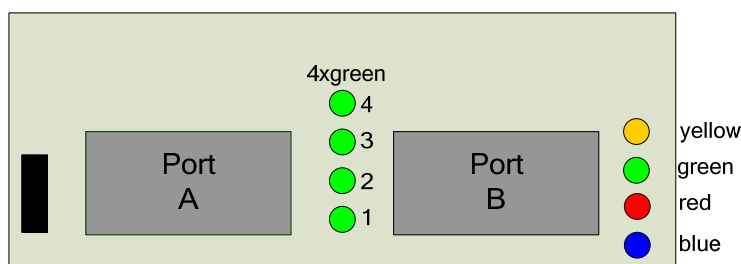
Table 4: LED Functionality

LED	Function
1	no default functionality; can be controlled by software
2	no default functionality; can be controlled by software
3	no default functionality; can be controlled by software
4	no default functionality; can be controlled by software
blue	AMC Hotswap LED
red	AMC Error LED
green	default: Lock Status PLL; can be overridden by software
yellow	default: Activity Ethernet; can be overridden by software
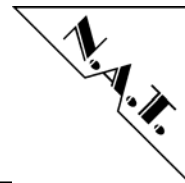
5 Connectors

5.1 Connector Overview

Figure 5:   Connectors of the NAMC-STM1/4
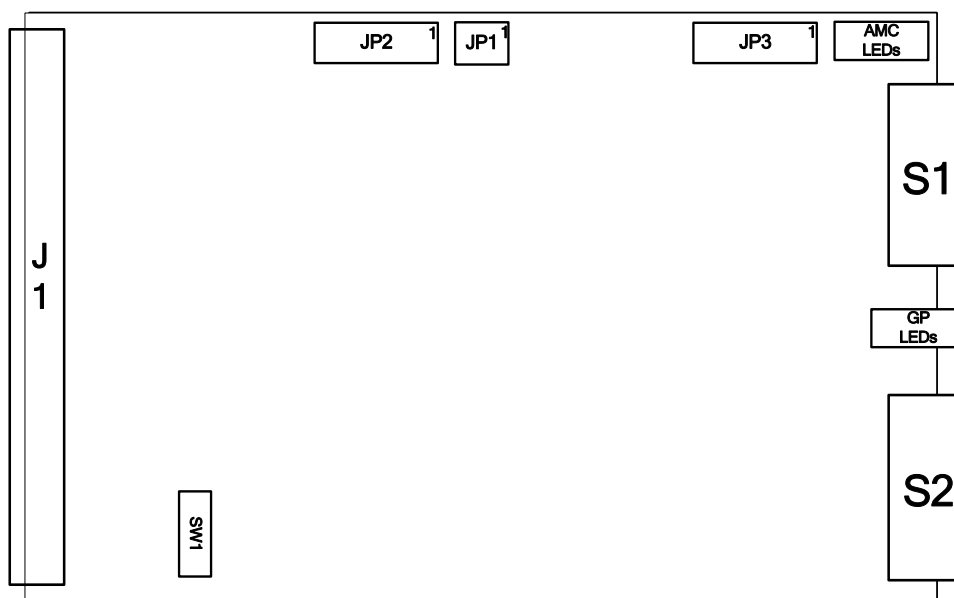
Please refer to the following tables to look up the connector pin assignment of the **NAMC-STM1/4**.
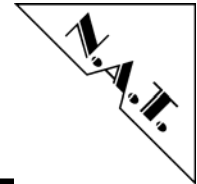
5.2   AMC Connector J1

Table 5: AMC Connector J1

Pin No.	AMC-Signal	AMC-Signal	Pin No.
1	GND	GND	170
2	PWR	TDI	169
3	/PS1	TDO	168
4	PWR_IPMB	/TRST	167
5	GA0	TMS	166
6	RESVD	TCK	165
7	GND	GND	164
8	RESVD	/SPISEL	163
9	PWR	SPICLK	162
10	GND	GND	161
11	XLINK1_P	SPIMOSI	160
12	XLINK1_N	SPIMISO	159
13	GND	GND	158
14	RLINK1_P	PORT19TX_P	157
15	RLINK1_N	PORT19TX_N	156
16	GND	GND	155
17	GA1	PORT19RX_P	154
18	PWR	PORT19RX_N	153
19	GND	GND	152
20	XLINK2_P	PORT18TX_P	151
21	XLINK2_N	PORT18TX_N	150
22	GND	GND	149
23	RLINK2_P	PORT18RX_P	148
24	RLINK2_N	PORT18RX_N	147
25	GND	GND	146
26	GA2	NC	145
27	PWR	NC	144
28	GND	GND	143
29	NC	NC	142
30	NC	NC	141
31	GND	GND	140
32	NC	NC	139
33	NC	NC	138
34	GND	GND	137
35	NC	NC	136
36	NC	NC	135
37	GND	GND	134
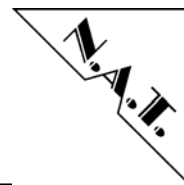
Pin No.	AMC-Signal	AMC-Signal	Pin No.
38	NC	NC	133
39	NC	NC	132
40	GND	GND	131
41	/ENABLE	NC	130
42	PWR	NC	129
43	GND	GND	128
44	PET0_P_P4	RESVD	127
45	PET0_N_P4	TDM_REF	126
46	GND	GND	125
47	PER0_P_P4	TDM_FS	124
48	PER0_N_P4	TDM_CLK	123
49	GND	GND	122
50	NC	TDM7	121
51	NC	TDM6	120
52	GND	GND	119
53	PER1_P	TDM5	118
54	PER1_N	TDM4	117
55	GND	GND	116
56	IPMB_SCL	TDM3	115
57	PWR	TDM2	114
58	GND	GND	113
59	NC	TDM1	112
60	NC	TDM0	111
61	GND	GND	110
62	NC	NC	109
63	NC	NC	108
64	GND	GND	107
65	NC	NC	106
66	NC	NC	105
67	GND	GND	104
68	NC	NC	103
69	NC	NC	102
70	GND	GND	101
71	IPMB_SDA	NC	100
72	PWR	NC	99
73	GND	GND	98
74	CLK_1_P	NC	97
75	CLK_1_N	NC	96
76	GND	GND	95
77	CLK_2_P	NC	94
78	CLK_2_N	NC	93

Pin No.	AMC-Signal	AMC-Signal	Pin No.
79	GND	GND	92
80	CLK_3_P	PET0_P_P8	91
81	CLK_3_N	PET0_N_P8	90
82	GND	GND	89
83	/PS0	PER0_P_P8	88
84	PWR	PER0_N_P8	87
85	GND	GND	86

5.3 Connector JP1: IPMI-µC Programming Port

Connector JP1 connects the programming-port of the Atmel AVR µC device.

Table 6: Atmel AVR Programming Port

Pin No.	Signal
1	MISO
2	VCC_IPMB
3	SCK
4	MOSI
5	/RST_IMPI
6	GND

5.4 Connector JP2: Lattice FPGA programming port

Connector JP2 connects the JTAG- or programming-port of the Lattice FPGA device.

Table 7: Lattice programming port

Pin No.	Signal	Signal	Pin No.
1	+3.3V	TDO	2
3	TDI	/PROGRAM	4
5	nc	TMS	6
7	GND	TCK	8
9	DONE_LAT	/INIT_LAT	10

5.5 Connector JP3: JTAG connector

This JTAG port connects to the JTAG interfaces of the Arrow and Temux devices, which are configured in a daisy chain.

Table 8: JTAG Connector Pinout

Pin No.	Signal	Signal	Pin No.
1	TCK	GND	2
3	TDO	+3,3V	4
5	TMS	nc	6
7	nc	nc	8
9	TDI	GND	10

5.6 Hot Swap Switch SW1

Switch SW1 is used to support hot swapping of the module. It conforms to PICMG AMC.0.

5.7   The Front Panel Connectors (S1 – S2)

The two optical front panel connectors have standard SC-plugs, and can be equipped with either singlemode or multimode transceivers.
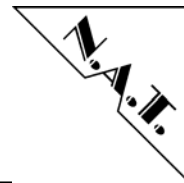
6 NAMC-STM1/4 Programming Notes

The FPGA on the **NAMC-STM1/4** realizes the interface to the onboard devices and an iTDM-to-TDM conversion engine. The table below shows the memory map for the logical sub-blocks of the design. Refer to the following sub-chapters for detailed information.

All devices shown in this memory map can be accessed either via PCIe or via the so called Ethernet Control Interface. This Interface uses a N.A.T. proprietary protocol based on Layer2 Ethernet frames to perform memory mapped accesses via Ethernet. Please refer to the Ethernet Control Interface Technical Reference Manual for further information [9].

The MAC address of the NAMC-STM1/4 is build with the following scheme:

00:40:42:14:XX:XX with XXXX being the boards serial number in hexadecimal representation

Table 9: FPGA Memory Map

Address Offset	Logical Block
0x00000	General Purpose Status (read-only)
0x00100	General Purpose Registers
0x01000	Interface to SPI FPGA PROM
0x08000	Arrow Framer 0
0x0c000	Arrow Framer 1
0x10000	Temux 0
0x14000	Temux 2
0x18000	Temux 1
0x1c000	Temux 3
0x20000	GbE-Interface Block
0x80000	iTDM Block

The FPGA-Design consists of four main blocks:

- Misc. board control- and status registers, and a register-interface to access the FPGA's PROM
- Ethernet Control Interface
- Interface to Arrow and Temux Devices
- GbE-MAC and frame preprocessing block
- iTDM block
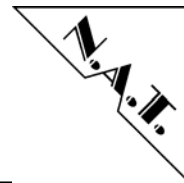
6.1.1 FPGA GP Registers/Status

This chapter describes the basic board control registers implemented within the FPGA. Further register description will follow up in future versions of this manual.

6.1.1.1 PCB Version Register

The Version Register holds the PCB Revision, encoded in two nibbles.

Table 10: PCB Version Register

PCB Version - Address 0x00			
Default value 0x0011			
Bit	15..8	7..4	3..0
Access	R	R	R
Func	reserved	Version Major	Version Minor

6.1.1.2 FPGA Version Register

The Version Register holds the FPGA Revision, encoded in two nibbles.

Table 11: FPGA Version Register

FPGA Version - Address 0x02			
Default value 0x0015			
Bit	15..8	7..4	3..0
Access	R	R	R
Func	reserved	Version Major	Version Minor

6.1.1.3 FPGA ID_1 Register

This read only register can be used by the device driver to probe register access.

Table 12: FPGA ID_1 Register

FPGA ID_1 - Address 0x04	
Default value 0xAA55	
Bit	15..0
Access	R
Func	ID_1

6.1.1.4 FPGA ID_2 Register

This read only register can be used by the device driver to probe register access.

Table 13: FPGA ID_2 Register

FPGA ID_2 - Address 0x06	
Default value 0xDEAD	
Bit	15..0
Access	R
Func	ID_2

6.1.1.5 FPGA BOARD_ID Register

This read only register can be used by the device driver to probe register access. It holds the N.A.T. internal board-id of the **NAMC-STM1/4.**
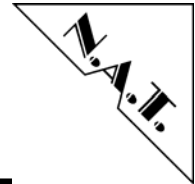
Table 14: FPGA BOARD_ID Register

FPGA BOARD_ID - Address 0x08	
Default value 0x0B06	
Bit	15..0
Access	R
Func	BOARD_ID

6.1.1.6 PLL Status Register

The bits within this register show the logical value of the Zarlink ZL304010 PLL status outputs. Please refer to the ZL304010 manual for detailed information.

Table 15: PLL Status Register

PLL Status – Address Offset 0x0A				
Default value 0x0000				
Bit	15..4	3	2	1	0
Access	R	R	R	R	R
Func	reserved	SECOR	PRIOR	HLDOV	LOCK

6.1.1.7 IRQ Status Register

This register displays the interrupt status line of all interrupt capable devices on the NAMC-STM1/4. A value of '1' means that the respective interrupt is pending. An IRQ transmitted via ECI (Ethernet Control Interface) is acknowledged and re-armed by writing a '1' to the corresponding bit.

Table 16: IRQ Status Register
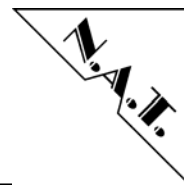
IRQ Status - Address 0x0C								
Default value 0x0000								
Bit	15..8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R
Func	reserved	ZPLL	iTDM	Temux 3	Temux 2	Temux 1	Temux 0	Arrow 1	Arrow 0

6.1.1.8 IRQ Enable Register

This register holds the bits to enable the interrupts being present in the IRQ Status Register.

Table 17: IRQ Enable Register

IRQ Enable - Address 0x10C								
Default value 0x0000								
Bit	15..8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	reserved	ZPLL	iTDM	Temux 3	Temux 2	Temux 1	Temux 0	Arrow 1	Arrow 0

6.1.1.9 FPGA Reset Register

The Reset Register is used to trigger a reset to the whole FPGA logic, FPGA blocks, or external devices. Writing a '1' to a bit triggers the reset. After reset, the bit is self-cleared to '0'.

Table 18: FPGA Reset Register

Reset – Address Offset 0x100							
Default value 0x0000							
Bit	15	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	Board global	IPMI-µC	Eth-Cntr-Int.	SPI-Interf.	SBI-bus	GbE	iTDM	Arrow Temux

6.1.1.10   GP LEDs Register

This register is used to control the four general purpose LEDs on the AMC module front panel between the optical connectors. The GP LEDs can be configured to the functionality listed below:

Table 19: GP LEDs Register

GP LEDs - Address 0x102			
Default value 0x0000			
Bit	15..12	11..8	7..4	3..0
Access	R/W	R/W	R/W	R/W
Func	GP LED 4	GP LED 3	GP LED 2	GP LED 1

Table 20: GP LEDs Values

Value	GP-LED Functions
0x0	off
0x1	on
0x2	slow blink
0x3	fast blink
others	reserved

6.1.1.11   AMC LEDs Register

This register is used to control the AMC LEDs 3 (most upper; yellow) and 2 (second from top; green) on the AMC module front panel.
Note: the other two AMC LEDs (LED 1 and LED blue) are controlled by the IPMI-µC.

Table 21: AMC LEDs Register

AMC LEDs - Address 0x104		
Default value 0x0054		
Bit	15..8	7..4	3..0
Access	R/W	R/W	R/W
Func	reserved	LED AMC 3	LED AMC 2
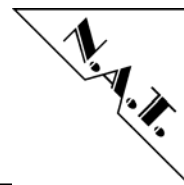
Table 22: AMC LED Values

| Value	AMC-LED Functions
0x0	off
0x1	on
0x2	slow blink
0x3	fast blink
0x4	TDM-PLL Lock Status
0x5	Ethernet activity
others	reserved

6.1.1.12   PLL Control Register

The PLL Control Register configures the main 77.76 MHz Telecom clock configuration.
The status of the PLL can be read on the PLL Status register. Please refer to the ZL304010 manual for detailed information.

Table 23: PLL Control Register

PLL Control - Address 0x106															
Default value 0x0028															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	Ref1_Sel				Ref0_Sel				/DS3	/OC3	OE	FCS	Ref All	Mode		Ref Sel

Table 24: PLL Control - Register Bits

Bit	Name	Function
[15..12]	Ref1_Sel	Selectors for each PLL's Reference Input: 0x0 – 77,76MHz Oscillator 0x1 – Arrow_0
[11..8]	Ref0_Sel	0x2 – Arrow_1 0x3 – AMC_Clk_3 / FCLK_A 0x4 – AMC_Clk_1 / TCLK_A 0x5 – AMC_Clk_2 / TCLK_B 0x6 – TCLK_C 0x7 – TCLK_D
[2..1]	Mode	Main PLL Mode Selection 0x0 – Normal Mode 0x1 – Holdover Mode 0x2 – Free running Mode 0x3 – reserved
[0]	RefSel	Select Reference Input of PLL (Input 0 or 1)
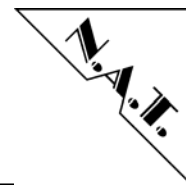
6.1.1.13   Misc Clock Config Register

This register holds the bits to select from which source the Arrow framer chips shall take its reference and the configuration bit for the AMC clock setup.

Table 25: Misc Clock Config Register

Misc Clock Config - Address 0x108															
Default value 0x0001															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	reserved								reserved						Arrow RefClock	

Table 26: Misc Clock Config - Register Bits

Bit	Name	Function
[1..0]	Arrow RefClock	Select Reference Clock for Arrow devices: 0x0: Local 77,76MHz oscillator 0x1: 77,76MHz from PLL

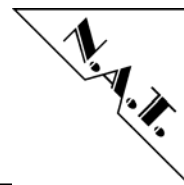### 6.1.1.14   SBI-bus Mode Register

This register holds the configuration bits for the SBI-bus interface within the FPGA.

Table 27: SBI-bus Mode Register

SBI-bus Mode - Address 0x10a															
Default value 0x0000															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	reserved															T1_Enable

Table 28: SBI-bus Mode - Register Bits

Bit	Name	Function
[1]	SBI_T1_Enable	Writing this bit to '1' makes the SBI-bus timeslot accessible that are used in T1 mode. A '0' makes the E1 timeslots accessible.

6.1.1.15   AMC-Clock Output Register

Each nibble within this register controls whether one of the four telecom AMC clocks is being driven and with which source. Note the different naming schemes: TCLKA equals AMC_CLK1; TCLKB equals AMC_CLK2.

Table 29: AMC-Clock Output Register

ACM-Clk Output - Address 0x10e															
Default value 0x0000															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	TCLKD_OSEL				TCLKC_OSEL				TCLKB_OSEL (AMC_CLK2_OSEL)				TCLKA_OSEL (AMC_CLK1_OSEL)			

Table 30: AMC-Clock Output Register Bits

Bit	Name	Function
[15..12] [11..8] [7..4] [3..0]	TCLKx_OSEL	Selector for the respective clock output: 0x0 – do not drive clock 0x1 – drive with 8kHz 0x2 – drive with 19,44MHz 0x3 – drive with 2,048MHz others – drive with 8kHz

6.1.1.16   AMC Site Number

This register displays the AMC Site number the module is in. This information is written into the FPGA upon power-up by the IPMI-µC.

Table 31: AMC Site Number

AMC LEDs - Address 0x01e	
Default value 0x0000	
Bit	15..8	7..0
Access	R	R
Func	reserved	AMC Site Number
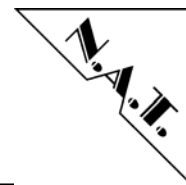
6.1.2 FPGA GbE/iTDM Configuration

Figure 4 shows a block diagram of the iTDM FPGA implemented on the NAMC-STM1/4.
For configuration and programming of the GbE/iTDM block please refer to the N.A.T.
iTDM-FPGA Manual (Appendix A, [4], NDA required).

Figure 6:   Organisation of the (i)TDM FPGA
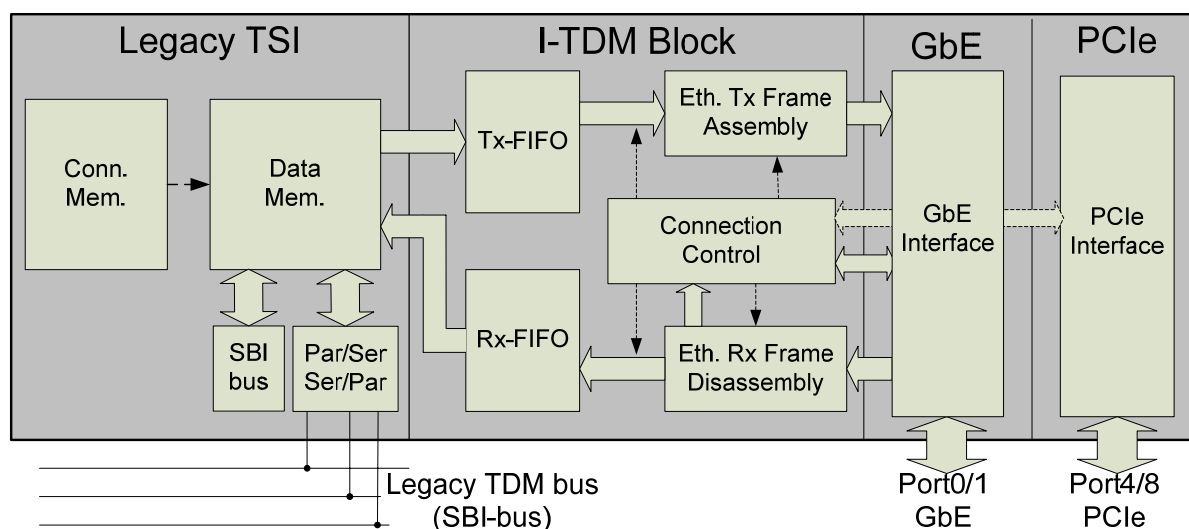
The iTDM Channel-ID for a certain E1 timeslot is calculated the following way:
ch_id = (E1_TS# * 63 + E1#) * 4 + STM#

If the SBI-bus logic is configured for T1 mode, the Channel-ID for a certain T1 timeslot is calculated this way:
ch_id = (T1_TS# * 84 + T1#) * 4 + STM#

Table 32: SBI-bus Timeslot Parameter

| Parameter	Function
E1#	Number of the E1 Link; Ranging from 0 to 62
T1#	Number of the T1 Link; Ranging from 0 to 83
E1_TS#	Number of the Timeslot within a E1 Link; Ranging from 0 to 31
T1_TS#	Number of the Timeslot within a T1 Link; Ranging from 0 to 23
STM#	Number of the four byte interleaved STM-1 Links present on the SBI-bus; Ranging from 0 to 3
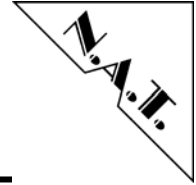
7 Known Bugs / Restrictions
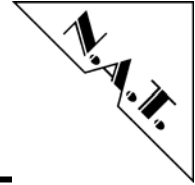
Appendix A: Reference Documentation

[1]   Atmel, Atmega48/88/168/V Product Data, Rev. 2545G, 06/06
[2]   Zarlink, ZL30410 System Synchronizer, Data Sheet, 11/2005
[3]   Traco Power DC/DC Converters, TOS Series, POL Converter, Rev. 10/05
[4]   N.A.T., iTDM-FPGA Technical Reference Manual, October 2006, Ver. 1.0
[5]   PMC Sierra: PM8316 - TEMUX84 Register Description, Issue March 2004
[6]   PMC Sierra: PM8316 - TEMUX84 Programmers Guide, Issue No. 4: Sep. 2003
[7]   PMC Sierra: PM5318/5320 - Arrow622/155 Operation and Configuration Guide
        Issue No.2, Jul 2004
[8]   PMC Sierra: PM5318/5320 - Arrow155 Register Description, Issue No.2, Jul 2004
[9]   N.A.T.: Ethernet Control Interface Technical Reference Manual, Ver. 1.0, Dez 2007
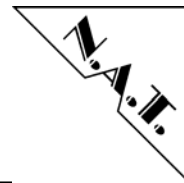
Appendix B: Document's History

Revision	Date	Description	Author
1.0	02.08.2007	initial revision	te
1.1	21.12.2007	added register descriptions	te
1.2	31.03.2008	further register descriptions; updated pin descriptions and locations for programming jumper	te
1.3	28.08.09	fixed description mismatch for JP1 in chapter 5.3	te