



STK-MBa35 User's Manual

STK-MBa35 UM 103
28.03.2013



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Revision history

Rev.	Date	Name	Pos.	Modification
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101	01.08.2011	Petz	Illustration 2 Table 39 7.1.1 7.1.2 8.1.1 8.1.2	Replaced Remarks corrected 7.1 7.2 8.1 8.2 Typo
102	24.05.2012	Petz	Section 5	Link to Wiki added
103	28.03.2013	Petz	All 9.4.2	Signal description of WP and CD# corrected Updated

1. ABOUT THIS MANUAL

1.1 Copyright

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1.2 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.


1.3 Symbols and Typographic Conventions

Table 1: Terms and conventions


Symbol / Visual Cue	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
Command	A font with fixed-width is used to denote commands, file names, or menu items.

1.4 Handling and ESD tips

General handling of your TQ-products

	<p>The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations.</p> <p>A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off.</p> <p>Violation of this guideline may result in damage / destruction of the module and be dangerous to your health.</p> <p>Improper handling of your TQ-product would render the guarantee invalid.</p>
---	--

Proper ESD handling

	<p>The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD).</p> <p>Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.</p>
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1.5 Registered trademarks

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1.6 Imprint

TQ-Systems GmbH

Gut Delling, Mühlstraße 2

82229 Seefeld

Tel: +49 (0)8153 9308-0

Fax: +49 (0)8153 9308-134

Email: info@tqs.de

Web: <http://www.tq-group.com/>

1.7 Disclaimer

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1.8 Copyright and licence expenses

The drivers and utilities for the components used as well as the BIOS are subject to the copyrights of the respective manufacturers. The licence conditions of the respective manufacturer are to be adhered to.

Bootloader-licence expenses are paid by TQ and are included in the price.

Licence expenses for the operating system and applications are not taken into consideration and must be separately calculated / declared.

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**

These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**

The manufacturer's specifications of the components used, for example Compact-Flash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ.
- **Chip errata:**

It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**

No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**

Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

1.10 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 2: Acronyms

Acronym	Meaning
AC	Alternating Current
AGND	Analog Ground
ARM®	Advanced RISC Machine
CAN	Controller Area Network
CPU	Central Processing Unit
DC	Direct Current
DCE	Data Communication Equipment (e.g. modem)
DGND	Digital Ground
DIN	Deutsche Industrie Norm
DIP	Dual In-line Package
DTE	Data Terminal Equipment (e.g. PC)
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electromagnetic Compatibility
EMMC	embedded MultiMediaCard (Flash)
EN	Europäische Norm (European Standards)
FET	Field Effect Transistor
FFC	Flat Flex Cable
FPC	Flexible Printed Circuit
FR-4	Flame Retardant-4
GND	Ground
GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output
HD-D-sub	High Density D-sub
I/O	Input/Output
I/P	Input/Power
IEEE	Institute of Electrical and Electronics Engineers
IP00	Ingress Protection 00
I ² C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display

Table 2: Acronyms (continued)

Acronym	Meaning
LED	Light Emitting Diode
LVDS	Low Voltage Differential Signal
MIC	Microphone
MII	Media-Independent Interface
MMC	Multimedia Card
MOZI	Module extractor (Modulzieher)
NC	Not Connected
OTG	On-The-Go
PCB	Printed Circuit Board
PHY	Physical (Interface)
PMIC	Power Management IC
PWM	Pulse Width Modulation
RAM	Random Access Memory
RCA	Radio Corporation of America
RFU	Reserved for Future Use
RGB	Red Green Blue
RJ	Registered Jack
RoHS	Restriction of (the use of certain) Hazardous Substances
RS232	Recommended Standard (serial interface)
RTC	Real-Time Clock
SD	Secure Digital
SDHC	Secure Digital High Capacity
SPI	Serial Peripheral Interface
SPS	Speicherprogrammierbare Steuerung Programmable Logic Controller (PLC)
THD+N	Total Harmonic Distortion + Noise
UART	Universal Asynchronous Receiver/Transmitter
UN	United Nations
USB	Universal Serial Bus
VGA	Video Graphics Array (640 × 480)
WEEE	Waste Electrical and Electronic Equipment
WEIM	Wireless External Interface Module
WP	Write-Protect

2. BRIEF DESCRIPTION

The STK-MBa35 is designed to be driven by TQ modules based on the Freescale ARM CPU MCIMX35 (i.MX35). In combination with a module and a display with touchscreen it offers PC core functionalities and standard interfaces.

By using the functionalities of the Starterkit STK-MBa35 this carrier board forms together with the TQMa35 a modular system to develop own product ideas.

3. TECHNICAL DATA

3.1 System architecture and system functionality

3.1.1 Block diagram

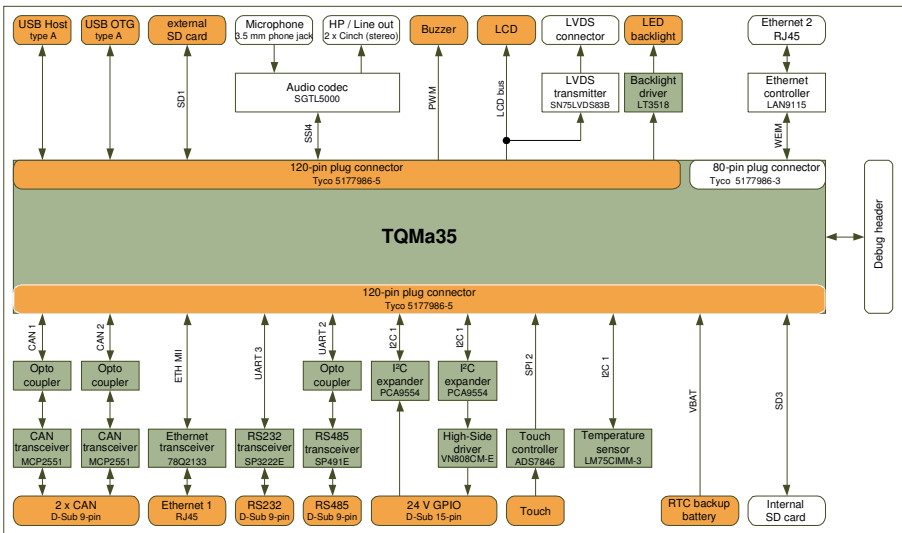


Illustration 1: Block diagram STK-MBa35

3.1.2 System functionality

The interfaces and system components listed in the following are implemented on the STK-MBa35. Due to the fact that the STK-MBa35 can be installed in a casing the interfaces are divided into external and internal interfaces.

3.1.2.1 External interfaces

- 2 × Ethernet 10/100 Mbit
- 1 × RS485
- 1 × RS232
- 2 × CAN
- 1 × USB 2.0 Hi Speed Host interface
- 1 × USB 2.0 Hi Speed On-The-Go device interface
- 1 × GPIO (8 × OUT / 4 × IN)
- 1 × SD card
- 2 × Audio output
- 1 × Microphone input
- 1 × Power supply

3.1.2.2 Internal interfaces

- 1 × TQMa35
- 1 × JTAG
- 2 × LCD (model dependent)
- 2 × LCD backlight (model dependent)
- 2 × Touchscreen (model dependent)
- 1 × LCD via LVDS (optional)
- 1 × SD card (optional)
- 1 × Power-On button
- 5 × Pin headers and 1 × power supply (Starterkit function / optional)

3.1.2.3 User's interfaces

- 1 × Reset button
- 3 × Status LEDs (external)
- 5 × Status LEDs (internal)
- 2 × DIP switch

3.1.2.4 System components

- Backup battery
- Buzzer
- Temperature sensor
- Power supply
- Voltage supervision and reset concept

3.1.3 Technical data mechanics, design

Dimensions PCB (W × D × H):	175 × 120 × 2 mm ³
Overall dimensions (W × D × H):	175 × 130 × 32 mm ³ (app.)
Weight:	261 g

4. ELECTRONICS SPECIFICATION

4.1 External interfaces

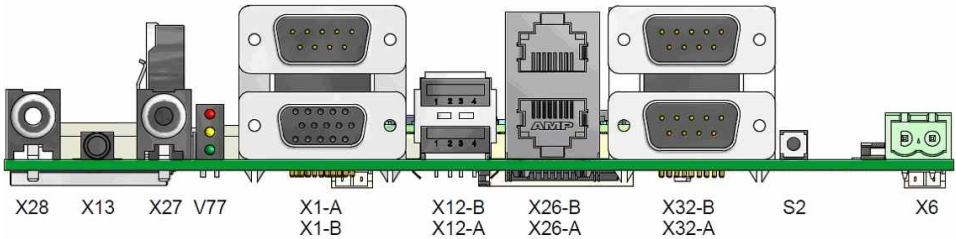


Illustration 2: External interfaces of the STK-MBa35

4.1.1 Function specification

4.1.1.1 Ethernet 1 (X26B)

The MII interface of the TQMa35 drives the Ethernet 1 interface. The Teridian78Q2133 is used as PHY.

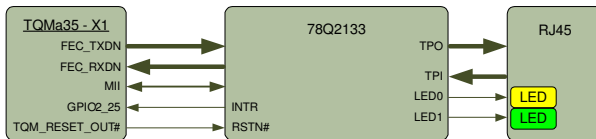


Illustration 3: Block diagram Ethernet 1

LED configuration see Table 9 on page 20.

Further LED configurations are programmable.

4.1.1.2 Ethernet 2 (X26A)

The Ethernet 2 interface is implemented by using the SMSC WEIM-PHY LAN9115. This interface is only available if the TQMa35 is equipped with connector X3.

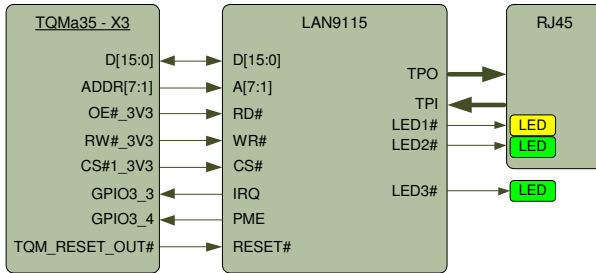


Illustration 4: Block diagram Ethernet 2

LED configuration see Table 12 on page 22.

4.1.1.3 RS485 (X32A)

The UART2 of the TQMa35 drives the RS485 interface of the STK-MBa35. The optocouplers Avago HCPL0631 and HCPL0601 are used for galvanic separation. The Recom RSS-0505/HP serves as the power supply for the galvanically separated part of the RS485 interface. The Exar SP491EEN-L is used as RS485 transceiver.

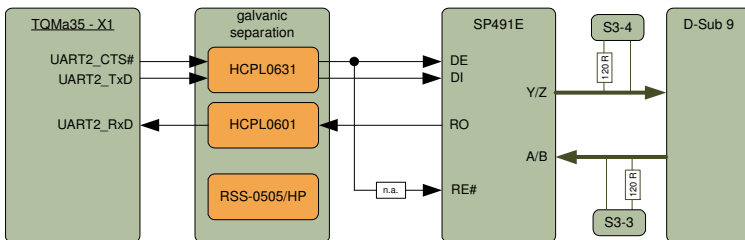


Illustration 5: Block diagram RS485

The RS485 signals can be terminated with 120 Ω with either DIP switch S3 or cable-sided by bridging pins 8 / 9 (RxD) and 1 / 7 (TxD). Details can be found in Table 72 on page 60.

4.1.1.4 RS232 (X32B)

The UART3 interface of the TQMa35 drives the RS232 interface of the STK-MBa35 by default. The Exar SP3222EEA-L is used as a driver. The RS232 interface driver on the TQMa35 can be used as an alternative. This uses UART1 of the TQMa35. It is however not recommended due to EMC reasons.

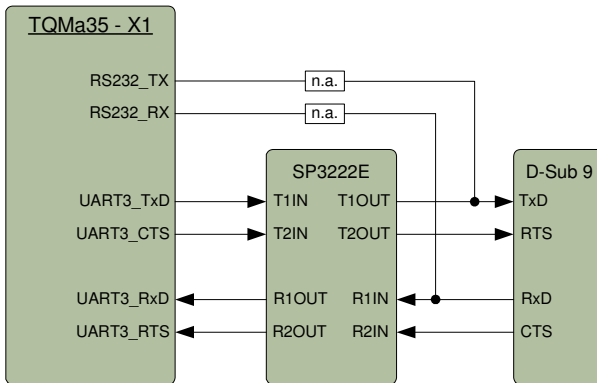


Illustration 6: Block diagram RS232

The CPU i.MX35 on the TQMa35 is designed as data communication equipment (DCE). The signals RTS and CTS do therefore not behave as in data terminal equipment (DTE, e.g., PC). The signal UART3_RTS of the TQMa35 is an input, the signal UART3_CTS of the TQMa35 is an output.

To compensate for this behaviour of the i.MX35, the signals RTS and CTS are crossed on the STK-MBa35:

- the CTS signal coming from an external source via (X32_8B) is routed as signal UART3_RTS on the STK-MBa35 to pin X1_108 of the TQMa35
- the RTS signal going to an external receiver via (X32_7B) comes as signal UART3_CTS on the STK-MBa35 from pin X1_109 of the TQMa35

4.1.1.5 CAN 1 / CAN 2 (X1A)

The two CAN ports of the TQMa35 directly drive both CAN interfaces on the STK-MBa35. Optocouplers of type Avago HCPL0601 are used for galvanic separation. The Recom RTS-0505/P serves as the power supply for the galvanically separated part of the CAN interface. Microchip MCP2551T-I/SN are used as CAN transceivers.

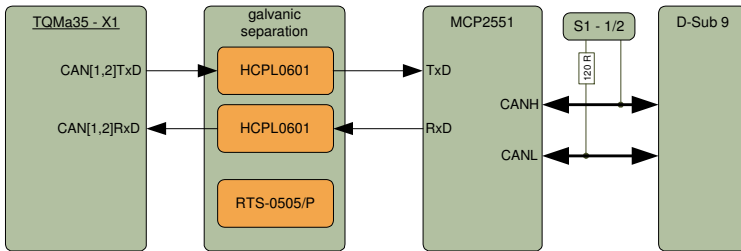


Illustration 7: Block diagram CAN

The CAN signals can be terminated with $120\ \Omega$ by using DIP switch S1 (see Table 71 on page 60).

4.1.1.6 GPIO (X1B)

Eight GPIO outputs and four GPIO inputs are made available at an external connector.

A voltage of $24\text{ V} \pm 20\%$ at the GPIO connector serves as the power supply. Due to the placement option the supply voltage of the STK-MBa35 can alternatively be used as the power supply. In this case the user has to ensure the correct level of the input voltage.

Two NXP (PCA9554D) 8 bit I²C bus I/O port circuits generate the GPIOs. This circuit offers eight bidirectional GPIO ports, which can drive and sink 10 mA.

The I²C addresses of both I²C I/O ports are listed in section 4.4.1 on page 61.

The basic circuit of the GPIO connection on the STK-MBa35 is shown in Illustration 8. The remaining four I/O ports are used for two user-LEDs (yellow and red) at V77, to switch on the backlight via connector X5 and to switch on the LVDS transmitter (LVDS Display).

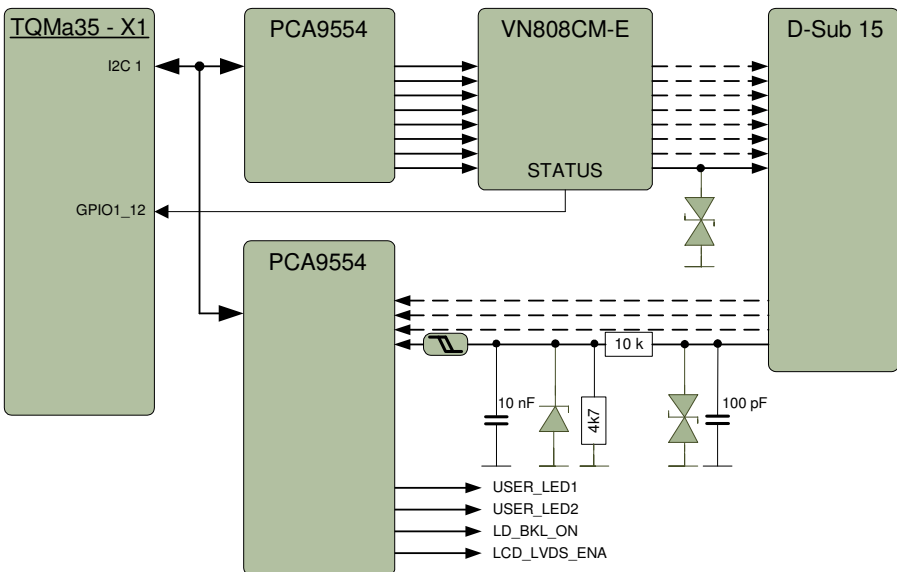


Illustration 8: Block diagram GPIO

Table 3: Allocation of the GPIOs

Signal	I ² C base address	I/O port	Direction
GPO1	0x20	IO0	O
GPO2		IO1	O
GPO3		IO2	O
GPO4		IO3	O
GPO5		IO4	O
GPO6		IO5	O
GPO7		IO6	O
GPO8		IO7	O
GPI1	0x21	IO0	I
GPI2		IO1	I
GPI3		IO2	I
GPI4		IO3	I
USER_LED1		IO4	O
USER_LED2		IO5	O
LD_BKL_ON		IO6	O
LCD_LVDS-ENA		IO7	O

4.1.1.7 USB 2.0 Hi-Speed Host (X12-A)

The USB host interface of the TQMa35 is routed directly to the USB-A jack X12-A, including the protection circuit. The over-current protection is implemented with a Texas Instruments TPS2042B.

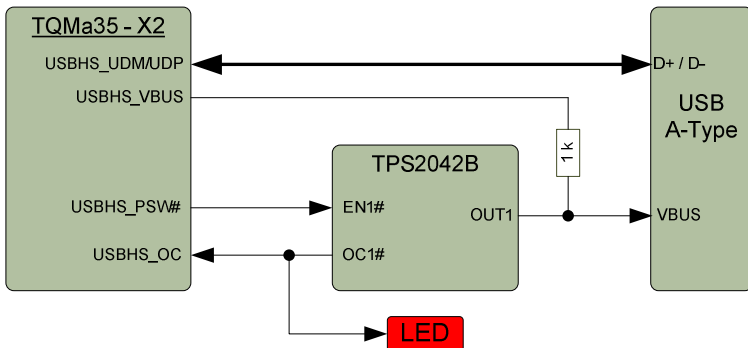


Illustration 9: Block diagram USB Host

4.1.1.8 USB 2.0 Hi-Speed OTG (X12-B)

The USB OTG interface is configured as the host by default and cannot be connected to a PC as device.

To offer OTG functionality it is possible to provide a USB-Mini-AB jack or Mini-B by a placement option.

However, as a result the USB 2.0 Hi Speed interface falls away.

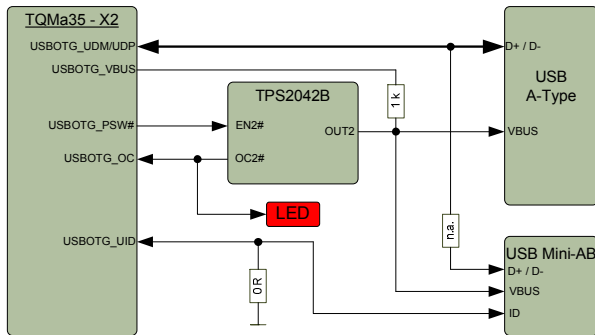


Illustration 10: Block diagram USB OTG

4.1.1.9 Audio-output right (X27) and left (X28), microphone input (X13)

The audio-functionality is implemented with a Freescale SGTL5000 on the STK-MBa35.

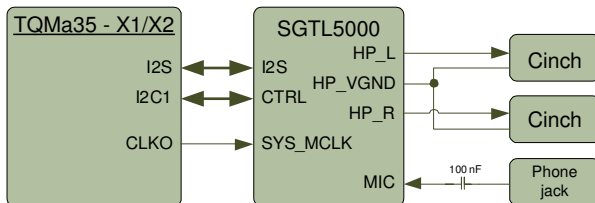


Illustration 11: Block diagram audio

The SGTL5000 can be accessed via I²C base address 0x0A.

4.1.1.10 Buzzer (N10)

The PWM output of the TQMa35 controls the buzzer.

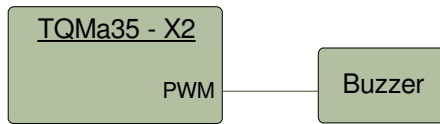


Illustration 12: Block diagram buzzer

4.1.1.11 SD card (X4)

The external SD card is connected to the SD1 bus of the TQMa35. Card-Detect and Write-Protect of the card are connected to GPIOs of the TQMa35.

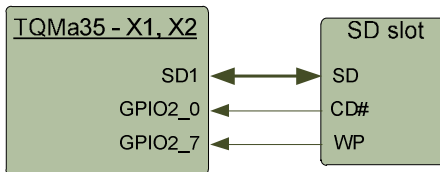


Illustration 13: Block diagram external SD card

4.1.1.12 Power-IN (X6)

For protective and EMC reasons the supply input of the STK-MBa35 is designed very robustly.

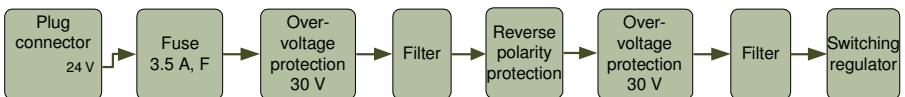


Illustration 14: Block diagram Power-IN

4.1.2 Electrical characteristics

4.1.2.1 Ethernet 1 (X26B)

Type of media:	10/100 Mbit
Interface on module:	MII interface (controller on the module TQMa35)
Status LEDs:	See Table 9 on page 20
Signal characteristic:	Compatible with the IEEE-802.3 standard

4.1.2.2 Ethernet 2 (X26A)

Type of media:	10/100 Mbit
Interface on module:	External memory bus (WEIM) / controller on the STK-MBa35
Status LEDs:	See Table 12 on page 22
Signal characteristic:	Compatible with the IEEE-802.3 standard

4.1.2.3 USB 2.0 Hi-Speed Host (X12-A)

Type of media:	USB 2.0 Hi-Speed, 5 V bus voltage (limited to 500 mA)
Interface on module:	USB Host physical
Signal characteristic:	Compatible with the Universal Serial Bus Specification Rev. 2.0
ESD protection:	±15 kV human body model

4.1.2.4 USB 2.0 Hi-Speed OTG (X12-B)

Type of media:	USB 2.0 OTG Hi-Speed, 5 V bus voltage (limited to 500 mA)
Interface on module:	USB OTG physical (only OTG / cannot be used as device)
Signal characteristic:	Compatible with the Universal Serial Bus Specification Rev. 2.0
ESD protection:	±15 kV human body model

4.1.2.5 RS485 (X32A)

Transfer rate:	Up to 4 Mbit/s (full-duplex)
Interface on module:	UART2
Handshake:	Used for clearing the transmission direction
Signal characteristic:	Compatible with the EIA/TIA-485 standard / galvanically separated
ESD protection:	±15 kV human body model

4.1.2.6 RS232 (X32B)

Transfer rate:	Up to 120 Kbit/s
Interface on module:	UART3 resp. RS232 (optional)
Handshake:	RTS/CTS (via UART3) resp. none (via RS232 from module / optional)
Signal characteristic:	Compatible with the EIA/TIA-232 standard
ESD protection:	±15 kV human body model

4.1.2.7 CAN 1/CAN 2 (X1A)

Transfer rate:	Up to 1 Mbit/s
Interface on module:	CAN1 resp. CAN2
Signal characteristic:	Compatible with the ISO-11898 standard (CAN 2.0B) / galvanically separated
ESD protection:	6 kV human body model

4.1.2.8 GPIO (X1B)

Type of media:	24 V GPIOs (according to the SPS standard)
Interface on module:	I2C1
Signal characteristic:	See Table 4 / <u>not</u> galvanically separated
ESD protection:	600 W pulse power (10 / 1 ms, 0.01 % duty cycle)

Table 4: Electrical characteristics of the GPIOs

Parameter	Min.	Typ.	Max.	Unit
Input frequency (hardware limitation)			15	kHz
Input voltage V_{IN}	0		28	V
Input current ($V_{IN} = 28 V$)			2.5	mA
Positive trigger level (LOW-to-HIGH)	4.4	5.3	7.5	V
Negative trigger level (HIGH-to-LOW)	2.2	3.1	5.3	V

Depending on the operating system and its workload the maximum input frequency can be significantly lower than the value specified by the hardware.

Table 5: Electrical characteristics of the GPOs

Parameter	Min.	Typ.	Max.	Unit
Output frequency			3	kHz
Supply voltage (V_{CC24V_EX})	12	24	30	V
Output voltage (depending on R_{Load})	$<V_{CC24V_EX}$			V
Load resistance R_{Load}	48			Ω
Load inductance ($V_{CC24V_EX} = 24 V$, $R_{Load} = 48 \Omega$)			2	H
Output current of a single output			700	mA
Output current of all outputs together			5	A
Short circuit current ($V_{CC24V_EX} = 24 V$, $R_{Load} = 10 m\Omega$)	0.7		1.7	A

4.1.2.9 SD card (X4)

Type of media:	SD / SDHC card
Interface on module:	SD 4-bit
Signal characteristic:	Compatible with the SD Host Controller Standard Specification version 2.0 Support for high capacity SD memory cards

4.1.2.10 Audio-output right (X27) and left (X28)

SNR (–60 dB Input):	98 dB
THD+N:	–86 dB
Load:	16 Ω
Power output:	58 mW

4.1.2.11 Microphone input (X13)

Input:	Mono
Gain:	Programmable (0, +20, +30, +40 dB)

4.1.2.12 Power-IN (X6)

Table 6: Electrical characteristics of the power supply

Parameter	Min.	Typ.	Max.	Unit
Input voltage	15	24	30	V
Input current		190		mA
Power consumption		4.56		W
Rated current of the fuse		3.5		A
Voltage drop in the fuse			0.13	V
Melting time of the fuse ($t < 10$ ms)		3.9		A ² s
Melting time of the fuse ($I = 10 * I_N$)		3.3		A ² s

The specified standard power supply for the STK-MBa35 is the following:

IPCX86MM NT REV. 100 18 V (max. 3.9 A)

With the abovementioned power supply the low voltage directives according to EN 60950 are met. In the case where another power supply is used or if the device is supplied from a 24 V power grid, it is the customer's responsibility to make sure the specified maximum ratings and standards are met.

Table 7: Overview of the function groups of the power supply

Parameter	Min.
Reverse voltage protection	Yes, actively via serial FET (max. 30 V for both polarities allowed)
Excess voltage protection	Yes, voltage limitation to 30 V. With lasting excess voltage the assembly can be damaged!
Short circuit protection	Yes. Passive over current protection by soldered ceramic fuse.
Filter	Integrated filters for the power supply input.

4.1.3 Connectors and pin assignments

4.1.3.1 Ethernet 1 (X26B)

Table 8: Ethernet 1 connector (X26B)

Manufacturer / number	Description
Tyco / 6368011-3	Type: 2 × RJ45 jack Eight contacts each LEDs: green and yellow –40 °C to +80 °C

The following table shows the configuration of the Ethernet 1 connector.

Table 9: Pin assignment Ethernet 1 connector (X26B)

Pin	Signal	Type	Remark
1	TX+	O	Galvanically separated
2	TX–	O	Galvanically separated
3	RX+	I	Galvanically separated
4	Termplane	–	75 Ω, AC coupled to DGND
5	Termplane	–	Connected to pin 4
6	RX–	I	Galvanically separated
7	Termplane	–	75 Ω, AC coupled to DGND
8	Termplane	–	Connected to pin 7
M	DGND	P	Ground housing
LED1	Link_Activity	–	See Table 10 on page 21
LED2	Speed_Indicator	–	See Table 10 on page 21

Two LEDs are used for diagnosis of the interface. The LEDs are visible from the outside and can be configured via the register MR23 of the Ethernet transceiver.

Table 10: Status LEDs Ethernet 1

Register MR23	Status display	Remark
0000	Link OK	Standard for yellow LED
0001	RX/TX activity	Standard for green LED
0010	TX activity	
0011	RX activity	
0100	Collision	
0101	100 BASE-TX mode	
0110	10 BASE-T mode	
0111	Full-duplex	
1000	LED on: Link OK Blinking: RX/TX activity	

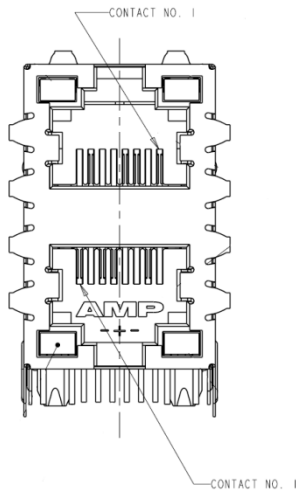


Illustration 15: Wiring of connector X26B

4.1.3.2 Ethernet 2 (X26A)

Table 11: Ethernet 2 connector (X26A)

Manufacturer / number	Description
Tyco / 6368011-3	Type: 2 × RJ45 jack Eight contacts each LEDs: green and yellow -40 °C to +80 °C

Two LEDs are used for diagnosis of the interface. The LEDs are visible from the outside and have predefined functions.

The following table shows the configuration of the Ethernet 2 connector.

Table 12: Pin assignment Ethernet 2 connector (X26A)

Pin	Signal	Type	Remark
1	TX+	O	Galvanically separated
2	TX-	O	Galvanically separated
3	RX+	I	Galvanically separated
4	Termination	-	75 Ω, AC coupled to DGND
5	Termination	-	75 Ω, AC coupled to DGND
6	RX-	I	Ethernet 1; galvanically separated
7	Termination	-	75 Ω, AC coupled to DGND
8	Termination	-	75 Ω, AC coupled to DGND
M	DGND	P	Ground housing
LED1	Link_Activity	-	Link activity (green LED) LED on: Valid link and network cable plugged in LED off: No valid link, network cable not plugged in Blinking: Packet transmission (transmission or reception)
LED2	Speed_Indicator	-	Speed indicator (yellow LED) LED on: 100 Mbit/s, disconnected resp. autonegotiation LED off: 10 Mbit/s
LED3 V78	Duplex_Indicator	-	Duplex indicator (green LED) LED on: Full-duplex LED off: Half-duplex LED V78 is visible from outside (positioned on the right hand side of the RJ45 jack)

Wiring of X26A see Illustration 15 on page 21.

4.1.3.3 RS485 (X32A)

Table 13: RS485 connector (X32A)

Manufacturer / number	Description
Yamaichi / DDP-01151	Dual standard D-sub connector 9-pin each -55 °C to +105 °C

The following table shows the configuration of the RS485 connector.

Table 14: Pin assignment RS485 connector (X32A)

Pin	Signal	Type	Remark
1	RS485_Y	O	Non inverted output / galvanically separated
2	NC	-	Not connected
3	NC	-	Not connected
4	RS485_A	I	Non inverted input / galvanically separated
5	GND_S2	P	Ground / galvanically separated
6	RS485_Z	O	Inverted output / galvanically separated
7	120R_TX	-	Bridge to pin 1 for 120 Ω termination
8	120R_RX	-	Bridge to pin 9 for 120 Ω termination
9	RS485_B	I	Inverted input / galvanically separated
M	DGND	P	Ground housing

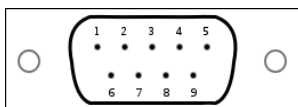


Illustration 16: Wiring of connector X32A

Attention: Destruction or malfunction!



Due to three physically identical 9-pin D-sub connectors there is the danger of confusion between RS232, RS485 and CAN.

The exact arrangement of the interfaces is shown in Illustration 2 on page 9.

4.1.3.4 RS232 (X32B)

Table 15: RS232 connector (X32B)

Manufacturer / number	Description
Yamaichi / DDP-01151	Dual Standard D-sub connector 9-pin each -55 °C to +105 °C

The following table shows the configuration of the RS232 connector.

Table 16: Pin assignment RS232 connector (X32B)

Pin	Signal	Type	Remark
1	NC	–	Not connected
2	RS232_RxD	I	Received Data
3	RS232_TxD	O	Transmitted Data
4	NC	–	Not connected
5	DGND	P	Ground
6	NC	–	Not connected
7	RS232_RTS	O	Request To Send
8	RS232_CTS	I	Clear To Send
9	NC	–	Not connected
M	DGND	P	Ground

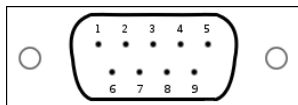


Illustration 17: Wiring of connector X32B

Attention: Destruction or malfunction!



Due to three physically identical 9-pin D-sub connectors there is the danger of confusion between RS232, RS485 and CAN.
The exact arrangement of the interfaces is shown in Illustration 2 on page 9.

4.1.3.5 CAN 1/CAN 2 (X1A)

Table 17: CAN 1 and CAN 2 connector (X1A)

Manufacturer / number	Description
Yamaichi / DDPXR-E9P/E15S-C4N-CT	Dual Standard D-sub connector / jack Top: 9-pin jack Bottom: 15-pin jack -55 °C to +105 °C

The following table shows the configuration of the connector for both CAN interfaces.

Table 18: Pin assignment CAN 1 and CAN 2 connector (X1A)

Pin	Signal	Type	Remark
1	CANL_2	I/O	CAN Low-Level I/O of CAN 2 / galvanically separated
2	CANL_1	I/O	CAN Low-Level I/O of CAN 1 / galvanically separated
3	GND_CAN	P	Ground / galvanically separated
4	CANH_2	I/O	CAN High-Level I/O of CAN 2 / galvanically separated
5	NC	-	Not connected
6	NC	-	Not connected
7	CANH_1	I/O	CAN High-Level I/O of CAN 1 / galvanically separated
8	NC	-	Not connected
9	NC	-	Not connected
M	DGND	P	Ground housing

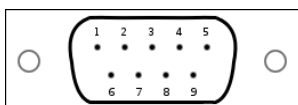


Illustration 18: Wiring of connector X1A

Attention: Destruction or malfunction!



Due to three physically identical 9-pin D-sub connectors there is the danger of confusion between RS232, RS485 and CAN.
The exact arrangement of the interfaces is shown in Illustration 2 on page 9.

4.1.3.6 GPIO (X1B)

Table 19: GPIO connector (X1B)

Manufacturer / number	Description
Yamaichi / DDPXR-E9P/E15S-C4N-CT	Dual Standard D-sub connector / jack Top: connector 9-pin Bottom: jack 15-pin -55 °C to +105 °C

The following table shows the configuration of the GPIO connector.

Table 20: Pin assignment GPIO connector (X1B)

Pin	Signal	Type	Remark
1	IN0	I	Input 0
2	IN1	I	Input 1
3	IN2	I	Input 2
4	IN3	I	Input 3
5	GND_EX	P	Ground
6	VCC24V_EX	P	Supply input for the outputs
7	GND_EX	P	Ground
8	OUT7	O	Output 7
9	OUT6	O	Output 6
10	OUT5	O	Output 5
11	OUT4	O	Output 4
12	OUT3	O	Output 3
13	OUT2	O	Output 2
14	OUT1	O	Output 1
15	OUT0	O	Output 0
M	DGND	P	Ground housing

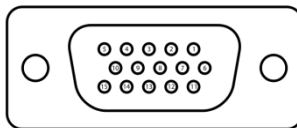


Illustration 19: Wiring of connector X1B

Attention: Destruction or malfunction!



The 15-pin HD-D-sub connector for GPIO (X1B) looks like a VGA-monitor output. No monitor may be connected there!

4.1.3.7 USB 2.0 Hi-Speed Host (X12-A)

Table 21: USB Host connector (X12-A)

Manufacturer / number	Description
Yamaichi / USB-A-002A	Dual USB jack, type A $U_N = 30 \text{ V AC (rms)} / I_N = 1 \text{ A}$ $U_{\text{max}} = 500 \text{ V AC for 1 minute}$ $-55 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$

The following table shows the configuration of the USB Host interface connector.

Table 22: Pin assignment USB Host connector (X12-A)

Pin	Signal	Type	Remark
1	VBUS	P	5 V supply (current limitation to 0.5 A) / 100 μF
2	DM	I/O	Negative differential data line
3	DP	I/O	Positive differential data line
4	DGND	P	Ground
M	DGND	P	Ground housing

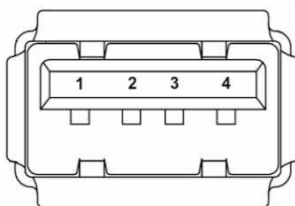


Illustration 20: Wiring of connector X12-A

4.1.3.8 USB 2.0 Hi-Speed OTG (X12-B)

Table 23: USB OTG connector (X12-B)

Manufacturer / number	Description
Yamaichi / USB-A-002A	Dual USB jack, type A $U_N = 30 \text{ V AC (rms)} / I_N = 1 \text{ A}$ $U_{\text{max}} = 500 \text{ V AC for 1 minute}$ $-55^\circ \text{C to } +85^\circ \text{C}$

The following table shows the configuration of the USB OTG interface connector.

Table 24: Pin assignment USB OTG connector (X12-B)

Pin	Signal	Type	Remark
1	VBUS	P	5 V supply (current limitation to 0.5 A) / 100 μF
2	DM	I/O	Negative differential data line
3	DP	I/O	Positive differential data line
4	DGND	P	Ground
M	DGND	P	Ground housing

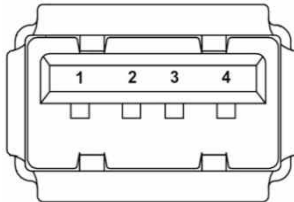


Illustration 21: Wiring of connector X12-B

4.1.3.9 Audio-output right (X27) and left (X28)

Table 25: Audio output right (X27) and left (X28)

Manufacturer / number	Description
Kycon / KLPX-0848A-2-B	RCA phono jack $U_{\max} = 500 \text{ V AC}$ for 1 minute $-25 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$

The following table shows the configuration of the right audio-output connector.

Table 26: Pin assignment audio output right (X27) and left (X28)

Pin	Signal	Type	Remark
1	GND	P	Ground
2	OUTR	AO	Analog audio output right

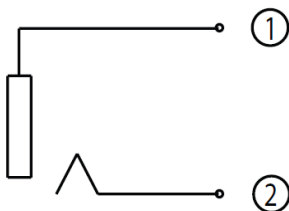


Illustration 22: Wiring of connector X27 / X28

4.1.3.10 Microphone input (X13)

Table 27: Microphone connector (X13)

Manufacturer / number	Description
Yamaichi / AJ330-4T-SMT	3.5 mm stereo jack 5,000 mating cycles $U_{\max} = 500 \text{ V AC}$ for 1 minute

The following table shows the configuration of the microphone input connector.

Table 28: Pin assignment microphone connector (X13)

Pin	Signal	Type	Remark
1	AGND	P	Ground
2	AGND	P	22 k Ω to ground
3	MIC_IN	AI	Analog microphone input
4	NC	–	Not connected

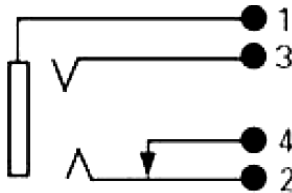


Illustration 23: Wiring of connector X13

4.1.3.11 SD card (X4)

Table 29: External SD card connector (X4)

Manufacturer / number	Description
Yamaichi / FPS009-2405-0	SD card and MMC reader 10,000 mating cycles $U_{\max} = 500 \text{ V AC}$ for 1 minute

The following table shows the configuration of the external SD card connector.

Table 30: Pin assignment external SD card connector (X4)

Pin	Signal	Type	Remark
1	DAT3	I/O	Data line 3, 100 k Ω \uparrow
2	CMD	I/O	Command / response Signal
3	DGND	P	Ground
4	VCC3V3	P	3.3 V supply
5	CLK	I	Clock input 50 MHz
6	DGND	P	Ground
7	DAT0	I/O	Data line 0, 100 k Ω \uparrow
8	DAT1	I/O	Data line 1, 100 k Ω \uparrow
9	DAT2	I/O	Data line 2, 100 k Ω \uparrow
CD	CD#	I	Card Detect
WP	WP	I	Write Protect, 10 k Ω \uparrow
COM	DGND	P	Ground

- low active signal, \uparrow - element to VCC5V (pull up), \downarrow - element to ground (pull down), \rightarrow - element in series

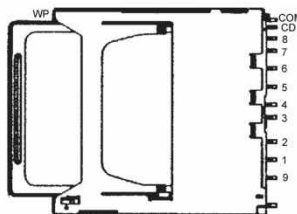


Illustration 24: Wiring of connector X4

4.1.3.12 Power-IN (X6)

Table 31: Power-IN connector (X6)

Manufacturer / number	Description
Phoenix Contact / MSTBA 2.5/ 2-G-5.08	Basic package 5.08 mm pitch 2-pin $U_N = 250 \text{ V} / I_N = 12 \text{ A}$

The following table shows the configuration of the 15–30 V power supply connector.

Table 32: Pin assignment Power-IN connector (X6)

Pin	Signal	Type	Remark
1	VCC24V	P	Input supply voltage
2	GND	P	Ground

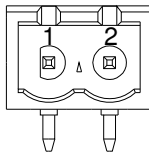


Illustration 25: Wiring of connector X6
(View on contacts from outside)

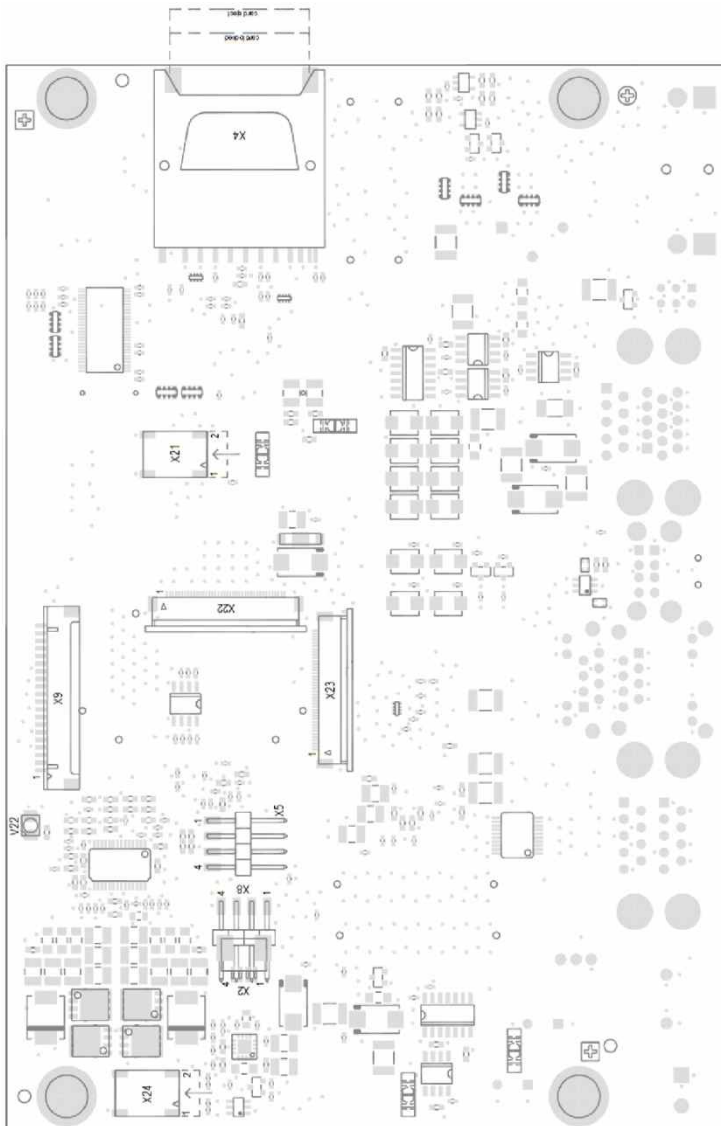


Illustration 27: Component placement bottom

4.2.1 Function specification

4.2.1.1 Module interface (D10)

The module interface of the TQMa35 module on which the module is plugged consists of two or three connectors.

Attention: Destruction or malfunction!



To avoid damages caused by mechanical stress, the TQMa35 may only be extracted from the carrier board by using the extraction tool MOZI8XXL. 2.5 mm should be kept free on the carrier board, along the longitudinal edges on both sides of the module for the extraction tool MOZI8XXL.

4.2.1.2 JTAG (X16)

On the TQMa35 the CPUs' JTAG interface is routed directly to a 2.54 mm pitch pin header.

Attention: Destruction or malfunction!



The JTAG signals at the connector are directly routed to the CPU. No ESD measures are taken, as it is an internal interface.

4.2.1.3 LCD (X22, X23)

On the STK-MBa35 the LCD bus of the TQMa35 is conditioned by a Texas Instruments driver 74LVC541 and routed to two FFC connectors (placement option). For EMC reasons every signal of the LCD bus is terminated with 22 Ω .

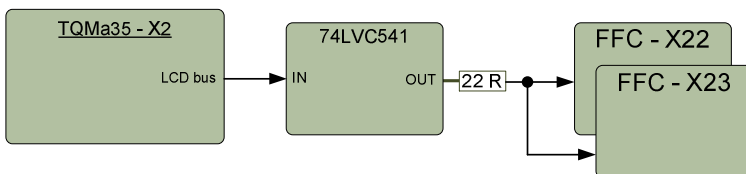


Illustration 28: Block diagram LCD

4.2.1.4 LCD backlight (X21, X24, X5)

As a placement option the STK-MBa35 offers a driver for displays with LED backlight. A Linear Technology LT3518 is used for this purpose. A 12 V supply of up to 2 A, as well as the signals LD_BKL_ON and LD_CONTRAST are available at another connector.

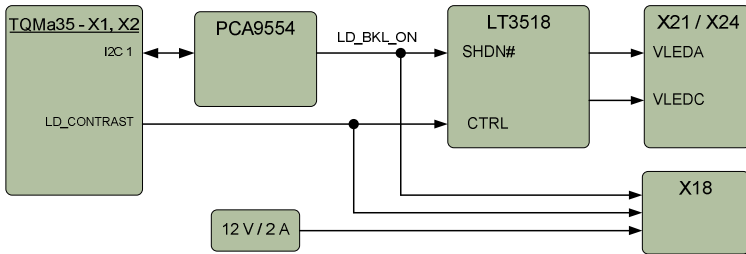


Illustration 29: Block diagram LCD backlight

In Table 3 on page 14 the mapping of the signal LD_BKL_ON is described.

4.2.1.5 Touchscreen (X2, X8)

A Texas Instruments ADS7846N touch controller is integrated on the STK-MBa35, which is routed to the SPI2 interface of the TQMa35. In this way a 4-wire touchscreen can be connected to the STK-MBa35. The lines of the touchscreen are equipped with protective ESD diodes, as well as a CLC filter.

Two connectors are available as placement option: an FFC connector with 1.25 mm pitch, or a pin header with 2.54 mm pitch.

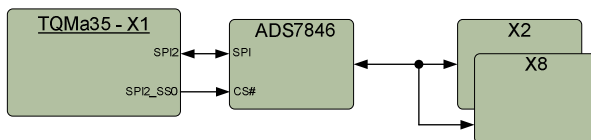


Illustration 30: Block diagram touchscreen

In Table 3 on page 14 the mapping of the signal LCL_LVDS-ENA is described.

4.2.1.6 LVDS Display (X9)

An LVDS transmitter, which transforms the data signals of the LCD bus to LVDS level, is implemented on the STK-MBa35 as a placement option. A Texas Instruments SN75LVDS83B is used for this.

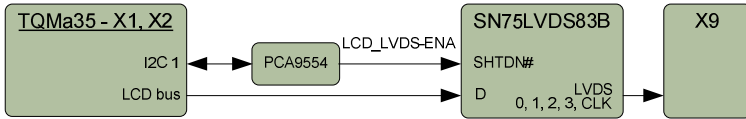


Illustration 31: Block diagram LVDS Display

Table 33: Allocation of RGB signals on LVDS lines

Input SN75LVDS83B	TQMa35 signal	Remark
D0	LD16	
D1	LD17	
D2	LD18	
D3	LD19	
D4	LD20	
D5	LD23	
D6	LD21	
D7	LD8	
D8	LD9	
D9	LD10	
D10	LD14	
D11	LD15	
D12	LD11	
D13	LD12	
D14	LD13	
D15	LD0	
D16	LD6	
D17	LD7	
D18	LD1	
D19	LD2	
D20	LD3	
D21	LD4	
D22	LD5	
D23	-	Pull-down
D24	LD_HSYNC	
D25	LD_VSYNC	
D26	LD_DRDY	
D27	LD22	
CLKIN	LD_CLK	
CLKSEL		Pull-down

In the i.MX35 Reference Manual the assignment of the RGB signals on the LCD bus of the i.MX35 can be looked up.

4.2.1.7 SD card (X25)

The internal SD card is connected to the SD3 bus of the TQMa35. Card-Detect and Write-Protect of the card are routed to GPIOs of the TQMa35.

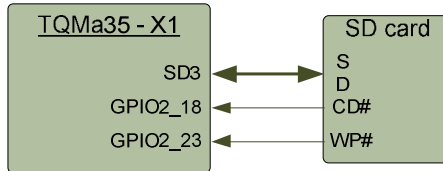


Illustration 32: Block diagram internal SD card

Attention: Usage of SD interface



The internal SD card may only be used if a TQMa35 module without eMMC flash is used.

4.2.1.8 Power-On (X19)

The power-on interface can be used to wake up the TQMa35 from standby and sleep state by a keystroke. The input at the TQMa35 must be configured accordingly.

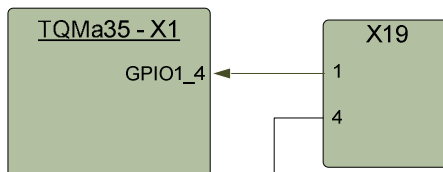



Illustration 33: Block diagram Power-On

4.2.1.9 Starterkit interfaces (X7, X10, X14, X15, X18, X31)

In order to be able to use all applicable processor signals several pin headers are assembled on the STK-MBa35 when it is used as a Starterkit.

Attention: Destruction or malfunction!	
	<p>The signals on the Starterkit interfaces are directly routed to the CPU. No ESD measures are taken as these are internal interfaces.</p>

4.2.2 Electrical characteristics

4.2.2.1 LCD (X22, X23)

Type of interface:	RGB, 18 bit
Control signals:	Clock, Data enable
Configuration:	The configuration of the LCD interface can be looked up in the i.MX35 Reference Manual

The following displays are supported by the STK-MBa35:

■ PowerView	T070W2D2
■ Data Image	FG0700K5DSSWBG01
■ Admatec	NLC800T70D480CTMK

4.2.2.2 LCD backlight (X21, X24, X5)

4.2.2.2.1 LED driver (X21, X24)

Output current: 200 mA (app. 10 V)

The LED driver is designed for the supported displays (Admatec, PowerView).

4.2.2.2.2 Backlight power supply (X5)

Type:	Buck regulator
Voltage:	12 V
Current _{max} :	2 A



4.2.2.3 Touchscreen (X2, X8)

Interface on module:	SPI2
Interface touchscreen:	4-wire
ESD protection:	±15 kV AD, ±8 kV CD

4.2.2.4 LVDS Display (X9)

Type of interface:	LVDS 18 bit / 24 bit
Differential pairs:	3 × data, 1 × clock
Control signals:	Clock, HSYNC, VSYNC, and DRDY
Configuration:	The configuration of the LCD interface can be looked up in the i.MX35 Reference Manual
ESD protection:	±5 kV human body model

4.2.2.5 SD card (X25)

Type of media:	SD / SDHC card
Interface on module:	SD 4-bit
Signal characteristic:	Compatible with the SD Host Controller Standard Specification version 2.0 Support for High Capacity SD memory cards

4.2.2.6 Starterkit interfaces (X7, X10, X14, X15, X18, X31)

All signals are 3.3 V compatible (except for the RS232 signals) at the Starterkit interfaces.

4.2.3 Connectors and pin assignment

4.2.3.1 Module interface (D10)

Table 34: Module interface connector (D10)

Manufacturer / number	Description
Tyco:	Pin header 120-pin, resp. 80-pin
X1, X2: 5177986-5	Stack height 5 mm
X3: 5177986-3	$U_{\max} = 100 \text{ V} / I_{\max} = 0.5 \text{ A}$
	100 mating cycles

The arrangement of the module connectors is shown in the following illustration.

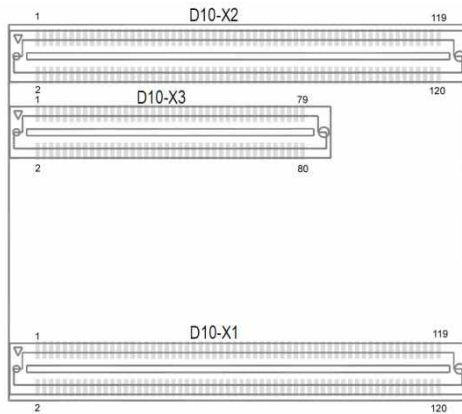


Illustration 34: Wiring of connector D10

The configuration of the module connectors is shown in the following three tables.

Table 35: Pin assignment module connector (D10-X1)

Group	Signal	I/O			I/O	Signal	Group	
Power	VCC3V3	P	1		2	P	VCC3V3	Power
Power	VCC3V3	P	3		4	P	VCC3V3	Power
Power	VCC3V3	P	5		6	P	VCC3V3	Power
Power	VCC3V3	P	7		8	P	VCC3V3	Power
Power	VBAT	P	9		10	P	DGND	Power
Power	DGND	P	11		12	P	DGND	Power
General clock	CLKO	O	13		14	P	DGND	Power
Power	DGND	P	15		16	P	DGND	Power
GPIO	GPIO1_4	I/O	17		18	P	DGND	Power
	GPIO1_5	I/O	19		20	I/O	GPIO1_12	GPIO
Power	DGND	P	21		22	I/O	GPIO1_22	
GPIO	GPIO2_7	I/O	23		24	I/O	GPIO2_0	Power
	GPIO2_18	I/O	25		26	P	DGND	
	GPIO2_23	I/O	27		28	I/O	COL0	
	GPIO2_25	I/O	29		30	I/O	COL1	
Power	DGND	P	31		32	I/O	COL2	4x4 keypad
4x4 keypad	ROW0	I/O	33		34	I/O	COL3	
	ROW1	I/O	35		36	P	DGND	
	ROW2	I/O	37		38	I/O	GPIO3_3	GPIO
ROW3	I/O	39		40	I/O	GPIO3_4		
Power	DGND	P	41		42	I/O	GPIO3_5	
1-Wire	OWDAT	I/O	43		44	I/O	SPI2_S50	SPI 2
SPI 1	SPI1_S50	I/O	45		46	P	DGND	Power
	SPI1_S51	I/O	47		48	I/O	SPI2_CLK	SPI 2
	SPI1_S53	I/O	49		50	I/O	SPI2_MISO	
Power	DGND	P	51		52	I/O	SPI2_MOSI	
SPI 1	SPI1_CLK	I/O	53		54	I	SPI2_RDY	Power
	SPI1_MISO	I/O	55		56	P	DGND	
	SPI1_MOSI	I/O	57		58	I/O	I2C1_SCL	
SPI1_RDY	I	59		60	I/O	I2C1_SDA		
Power	DGND	P	61		62	I/O	I2C2_SCL	I ² C 2
Timer	TIM_CAPIN1	I	63		64	I/O	I2C2_SDA	
	TIM_CMPOUT1	O	65		66	P	DGND	Power
SD card 3	SD3_CMD	I/O	67		68	I/O	SD3_DAT0	SD card 3
	SD3_CLK	O	69		70	I/O	SD3_DAT1	
Power	DGND	P	71		72	I/O	SD3_DAT2	
SD card 3	SD3_DAT4	I/O	73		74	I/O	SD3_DAT3	
	SD3_DAT5	I/O	75		76	P	DGND	Power
	SD3_DAT6	I/O	77		78	O	FEC_TXD0	Ethernet MII
	SD3_DAT7	I/O	79		80	O	FEC_TXD1	
Power	DGND	P	81		82	O	FEC_TXD2	
Ethernet MII	FEC_TXD3	O	83		84	I	FEC_TX_CLK	
	FEC_TX_ER	O	85		86	P	DGND	Power
	FEC_TX_EN	O	87		88	I	FEC_RXD0	Ethernet MII
	FEC_RXD1	I	89		90	I	FEC_RXD2	
Power	DGND	P	91		92	P	DGND	Power
Ethernet MII	FEC_RXD3	I	93		94	I	FEC_RX_CLK	Ethernet MII
	FEC_RX_ER	I	95		96	P	DGND	Power
	FEC_RX_DV	I	97		98	I/O	FEC_MDIO	Ethernet MII
	FEC_MDC	O	99		100	I	FEC_CRS	
Power	DGND	P	101		102	I	FEC_COL	
CAN 2	CAN2_TX	O	103		104	I	CAN2_RX	CAN 2
CAN 1	CAN1_TX	O	105		106	P	DGND	Power
	CAN1_RX	I	107		108	I	UART3_RTS#	UART 3
UART 3	UART3_CTS#	O	109		110	O	UART3_TXD	
Power	DGND	P	111		112	I	UART3_RXD	
UART 2	UART2_RTS#	I	113		114	O	UART2_CTS#	UART 2
	UART2_TXD	O	115		116	P	DGND	Power
	UART2_RXD	I	117		118	O	RS232_TXD	RS232
Power	DGND	P	119		120	I	RS232_RXD	

Table 36: Pin assignment module connector (D10-X2)

Group	Signal	I/O		I/O	Signal	Group	
Power	DGND	P	1	2	I	FLASH_RESET#	NOR-Flash-CTRL
Reserve	NC	-	3	4	I	WP#_ACC	
	NC	-	5	6	P	DGND	Power
Power Management	VSTBY	I	7	8	I	WDOG_RST#	Reset
Timer	PWM	O	9	10	I	JTAG_RESET#	
Power	DGND	P	11	12	I	RESET_IN#	
SSI 4	SSI_TXD	I/O	13	14	O	POR#	Power
	SSI_RXD	I/O	15	16	P	DGND	
	SSI_TXC	I/O	17	18	O	LD0	
	SSI_TXFS	I/O	19	20	O	LD1	
Power	DGND	P	21	22	O	LD2	IPU-LCD
	LD3	O	23	24	O	LD4	
IPU-LCD	LD5	O	25	26	P	DGND	Power
	LD7	O	27	28	O	LD6	IPU-LCD
	LD9	O	29	30	O	LD8	
Power	DGND	P	31	32	O	LD10	
IPU-LCD	LD11	O	33	34	O	LD12	Power
	LD13	O	35	36	P	DGND	
	LD15	O	37	38	O	LD14	
	LD17	O	39	40	O	LD16	
Power	DGND	P	41	42	O	LD18	IPU-LCD
	LD19	O	43	44	O	LD20	
IPU-LCD	LD21	O	45	46	P	DGND	Power
	LD23	O	47	48	O	LD22	IPU-LCD
	LD_DRDY	O	49	50	O	LD_SPL	
Power	DGND	P	51	52	O	LD_REV	
IPU-LCD	LD_HSYNC	O	53	54	O	LD_CLS	Power
	LD_VSYNC	O	55	56	P	DGND	
Power	DGND	P	57	58	O	LD_CONTRAST	IPU-LCD
IPU-LCD	LD_CLK	O	59	60	I	USBHS_OC	USB Host Hi-Speed
Power	DGND	P	61	62	O	USBHS_PSW#	
USB Host Hi-Speed	USBHS_UID	I	63	64	I/O	USBHS_VBUS	
Power	DGND	P	65	66	P	DGND	Power
USB Host Hi-Speed	USBHS_UDP	I/O	67	68	I	USB_OTG_OC	USB OTG Hi-Speed
	USBHS_UDM	I/O	69	70	O	USB_OTG_PWR	
Power	DGND	P	71	72	I	USB_OTG_UID	
USB OTG Hi-Speed	USB_OTG_DM	I/O	73	74	I/O	USB_OTG_VBUS	
	USB_OTG_DP	I/O	75	76	P	DGND	Power
Power	DGND	P	77	78	I/O	SD1_DAT0	SD card 1
SD card 1	SD1_CLK	O	79	80	I/O	SD1_DAT1	
Power	DGND	P	81	82	I/O	SD1_DAT2	
SD card 1	SD1_CMD	I/O	83	84	I/O	SD1_DAT3	
IPU-CSI	CSI_D1	I	85	86	P	DGND	Power
	CSI_D3	I	87	88	I	CSI_D0	IPU-CSI
	CSI_D5	I	89	90	I	CSI_D2	
Power	DGND	P	91	92	I	CSI_D4	
IPU-CSI	CSI_D7	I	93	94	I	CSI_D6	Power
	CSI_D9	I	95	96	P	DGND	
	CSI_D11	I	97	98	I	CSI_D8	
	CSI_D13	I	99	100	I	CSI_D10	
Power	DGND	P	101	102	I	CSI_D12	IPU-CSI
	CSI_D15	I	103	104	I	CSI_D14	
IPU-CSI	CSI_VSYNC	I	105	106	P	DGND	Power
	CSI_HSYNC	I	107	108	O	CSI_MCLK	IPU-CSI
	CSI_PIXCLK	I	109	110	I/O	DE#	CPU-JTAG
Power	DGND	P	111	112	O	RTCK	
CPU-JTAG	TCK	I	113	114	I	JTAG_MOD	
	TMS	I	115	116	P	DGND	Power
	TDI	I	117	118	O	TDO	CPU-JTAG
Power	DGND	P	119	120	I	TRST#	



Table 37: Pin assignment module connector (D10-X3)

Group	Signal	I/O			I/O	Signal	Group
Power	DGND	P	1	X3	2	I/O D0	16 Bit data bus
16 Bit data bus	D1	I/O	3		4	I/O D2	
	D3	I/O	5		6	P DGND	Power
	D5	I/O	7		8	I/O D4	16 Bit data bus
	D7	I/O	9		10	I/O D6	
Power	DGND	P	11		12	I/O D8	
16 Bit data bus	D9	I/O	13		14	I/O D10	16 Bit data bus
	D11	I/O	15		16	P DGND	
	D13	I/O	17		18	I/O D12	16 Bit data bus
	D15	I/O	19		20	I/O D14	
Power	DGND	P	21		22	O A0	26 Bit address bus
26 Bit address bus	A1	O	23		24	O A2	
	A3	O	25		26	P DGND	Power
	A5	O	27		28	O A4	26 Bit address bus
	A7	O	29		30	O A6	
Power	DGND	P	31		32	O A8	
26 Bit address bus	A9	O	33		34	O A10	
	A11	O	35		36	P DGND	Power
	A13	O	37		38	O A12	26 Bit address bus
	A15	O	39		40	O A14	
Power	DGND	P	41		42	O A16	
26 Bit address bus	A17	O	43		44	O A18	
	A19	O	45		46	P DGND	Power
	A21	O	47		48	O A20	26 Bit address bus
	A23	O	49		50	O A22	
Power	DGND	P	51		52	O A24	
26 Bit address bus	A25	O	53		54	O LBA#	
Bus-CTRL	DTACK#	I	55		56	P DGND	Power
Power	DGND	P	57	58	O RW#	Bus-CTRL	
Bus-CTRL	BUS_CLK	O	59	60	O OE#		
Power	DGND	P	61	62	I ECB#		
Bus-CTRL	EB1#	O	63	64	O EBO#		26 Bit address bus
	CS1#	O	65	66	P DGND	Power	
	CS5#	O	67	68	- DNC	Factory test only	
Factory test only	DNC	-	69	70	- DNC		
Power	DGND	P	71	72	- DNC		
Factory test only	DNC	-	73	74	- DNC		26 Bit address bus
	DNC	-	75	76	P DGND	Power	
	DNC	-	77	78	- NC	Reserve	
Power	DGND	P	79	80	- NC		

4.2.3.2 JTAG (X16)

Table 38: JTAG connector (X16)

Manufacturer / number	Description
Samtec / TSM-107-01-L-DV	Pin header 2.54 mm, 7 × 2-pin

The following table shows the configuration of the JTAG connector.

Table 39: Pin assignment JTAG connector (X16)

Pin	Signal	Type	Remark
1	VCC3V3	P	Supply voltage 3.3 V
2	DGND	P	Ground
3	JTAG_TRST#	I	Test Reset
4	DGND	P	Ground
5	JTAG_TDI	I	Test Data In
6	NC	–	(Not connected)
7	JTAG_TMS	I	Test Mode Select
8	MR_RESET#	I	0 Ω, not assembled
9	JTAG_TCK	I	Test Clock
10	JTAG_MOD	I	0 Ω, not assembled
11	JTAG_TDO	O	Test Data Out
12	JTAG_RST#	I	Global module reset
13	JTAG_DE#	I/O	Debug Request, 0 Ω, not assembled
14	JTAG_RTCK	O	Return Clock, 0 Ω, not assembled

- low active signal, ↑ - element to VCC5V (pull up), ↓ - element to ground (pull down), → - element in series

Polarity see Illustration 26 on page 33.

4.2.3.3 LCD (X22, X23)

Table 40: LCD connectors (X22, X23)

Manufacturer / number	Description
Yamaichi / FPC-98210-4021	FPC connector 0.5 mm pitch $U_N = 50 \text{ V} / I_N = 0.5 \text{ A}$ Minimum 30 mating cycles -20 °C to +85 °C

Table 41: Pin assignment LCD connectors (X22, X23)

PowerView Data Image (X22)	Admatec (X23)	Signal	Type	Remark
1	-	GND	P	Ground
2	-	GND	P	Ground
3	-	PowerView: NC Data Image: ADJ	- O	PowerView: 100 kΩ Data Image: LCD_CONTRAST (PWM)
4	40	PowerView/Admatec: VCC3V3 Data Image: VCC5V	P P	Supply voltage
5	39	PowerView/Admatec: VCC3V3 Data Image: VCC5V	P P	Supply voltage
6	38	PowerView/Admatec: VCC3V3 Data Image: VCC5V	P P	Supply voltage
7	37	VCC3V3	P	Supply voltage
8	-	PowerView: NC Data Image: VCC3V3	- P	PowerView: not connected Data Image: Supply voltage
9	35	DATA Enable	O	LCD_OE, 22 Ω →
10	34	GND	P	Ground
11	32	GND	P	Ground
12	30	GND	P	Ground
13	29	Blue 5	O	LCD_D5, 22 Ω →
14	28	Blue 4	O	LCD_D4, 22 Ω →
15	27	Blue 3	O	LCD_D3, 22 Ω →
16	26	GND	P	Ground
17	25	Blue 2	O	LCD_D2, 22 Ω →
18	24	Blue 1	O	LCD_D1, 22 Ω →

PowerView Data Image (X22)	Admatec (X23)	Signal	Type	Remark
19	23	Blue 0	O	LCD_D0, 22 Ω →
20	22	GND	P	Ground
21	21	Green 5	O	LCD_D11, 22 Ω →
22	20	Green 4	O	LCD_D10, 22 Ω →
23	19	Green 3	O	LCD_D9, 22 Ω →
24	18	GND	P	Ground
25	17	Green 2	O	LCD_D8, 22 Ω →
26	16	Green 1	O	LCD_D7, 22 Ω →
27	15	Green 0	O	LCD_D6, 22 Ω →
28	14	GND	P	Ground
29	13	Red 5	O	LCD_D17, 22 Ω →
30	12	Red 4	O	LCD_D16, 22 Ω →
31	11	Red 3	O	LCD_D15, 22 Ω →
32	10	GND	P	Ground
33	9	Red 2	O	LCD_D14, 22 Ω →
34	8	Red 1	O	LCD_D13, 22 Ω →
35	7	Red 0	O	LCD_D12, 22 Ω →
36	5	GND	P	Ground
37	4	GND	P	Ground
38	3	DCLK	O	LCD_SCLK, 22 Ω → / 10 pF↓
39	2	GND	P	Ground
40	1	GND	P	Ground
-	6	NC	-	not connected
-	31	NC	-	not connected
-	33	NC	-	not connected
-	36	NC	-	not connected

- low active signal, ↑ - element to VCC5V (pull up), ↓ - element to ground (pull down), → - element in series

4.2.3.4 LCD backlight (X21, X24, X5)

Table 42: LCD backlight connectors (X21, X24)

Manufacturer / number	Description
JST / SM02B-BHSS-1-TB	Crimp connector $U_N = 1,400 \text{ V} / I_N = 1 \text{ A}$ $-25 \text{ }^\circ\text{C}$ to $+85 \text{ }^\circ\text{C}$

Table 43: Pin assignment LCD backlight connectors (X21, X24)

Pin	Signal	Type	Remark
1	VLEDA	P	Anode of LED backlight
2	VLEDC	P	Cathode of LED backlight



Illustration 35: Wiring of connector connectors X21, X24

Table 44: LCD backlight connector (X5)

Manufacturer / number	Description
Harwin / M20-8900405	Pin header 2.54 mm, 1 × 4-pin $I_N = 3 \text{ A}$ $-40 \text{ }^\circ\text{C}$ to $+105 \text{ }^\circ\text{C}$

Table 45: Pin assignment LCD backlight connector (X5)

Pin	Signal	Type	Remark
1	VCC12V	P	Supply voltage 12 V, alternative 5 V
2	LD_BKL_ON	O	GPIO from PCA9554D to switch the backlight
3	LD_CONTRAST	O	PWM contrast
4	DGND	P	Ground

Wiring see Illustration 27 on page 34.

4.2.3.5 Touchscreen (X2, X8)

Table 46: Touchscreen connector (X2)

Manufacturer / number	Description
JST / 04FFS-SP-TF	FFC connector Pitch 1.25 mm $U_N = 50 \text{ V}$, $I_N = 0.5 \text{ A}$ -25 °C to +85 °C

Table 47: Touchscreen connector (X8)

Manufacturer / number	Description
Harwin / M20-8900405	Pin header 2.54 mm 4 × 1-pin $I_N = 3 \text{ A}$ -40 °C to +105 °C

Table 48: Pin assignment touchscreen connector (X2, X8)

Pin	Signal	Type	Remark
1	Y-	I/P	Touchscreen Bottom
2	X+	I/P	Touchscreen Right
3	Y+	I/P	Touchscreen Top
4	X-	I/P	Touchscreen Left

Wiring see Illustration 27 on page 34.

4.2.3.6 LVDS Display (X9)

Table 49: LVDS Display connector (X9)

Manufacturer / number	Description
Hirose / DF14-20P-1.25H(25)	Crimp connector $U_N = 150 \text{ V}$, $I_N = 1 \text{ A}$ $-35 \text{ }^\circ\text{C}$ to $+85 \text{ }^\circ\text{C}$

Table 50: Pin assignment LVDS Display connector (X9)

Pin	Signal	Type	Remark
1	DGND	P	Ground
2	DGND	P	Ground
3	LVDS3+	O	Data pair 3 positive
4	LVDS3-	O	Data pair 3 negative
5	DGND	P	Ground
6	LVDSCLK+	O	Clock pair positive
7	LVDSCLK-	O	Clock pair negative
8	DGND	P	Ground
9	LVDS2+	O	Data pair 2 positive
10	LVDS2-	O	Data pair 2 negative
11	DGND	P	Ground
12	LVDS1+	O	Data pair 1 positive
13	LVDS1-	O	Data pair 1 negative
14	DGND	P	Ground
15	LVDS0+	O	Data pair 0 positive
16	LVDS0-	O	Data pair 0 negative
17	DGND	P	Ground
18	DGND	P	Ground
19	VCC3V3	P	Supply voltage 3.3 V, alternatively 5 V
20	VCC3V3	P	Supply voltage 3.3 V, alternatively 5 V

Wiring see Illustration 27 on page 34.

4.2.3.7 SD card (X25)

Table 51: Internal SD card connector (X25)

Manufacturer / number	Description
Yamaichi / FPS009-2405-0	SD card and MMC reader 10,000 mating cycles $U_{\max} = 500 \text{ V AC}$ for 1 minute

The following table shows the configuration of the internal SD card connector.

Table 52: Pin assignment internal SD card connector (X25)

Pin	Signal	Type	Remark
1	DAT3	I/O	Data line 3, 100 k Ω \uparrow
2	CMD	I/O	Command/Response signal
3	DGND	P	Ground
4	VCC3V3	P	3.3 V supply
5	CLK	I	Clock input 50 MHz
6	DGND	P	Ground
7	DAT0	I/O	Data line 0, 100 k Ω \uparrow
8	DAT1	I/O	Data line 1, 100 k Ω \uparrow
9	DAT2	I/O	Data line 2, 100 k Ω \uparrow
CD	CD#	I	Card Detect
WP	WP	I	Write Protect, 10 k Ω \uparrow
COM	DGND	P	Ground

- low active signal, \uparrow - element to VCC5V (pull up), \downarrow - element to ground (pull down), \rightarrow - element in series

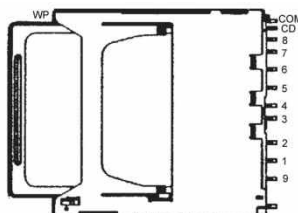


Illustration 36: Wiring of connector X25

4.2.3.8 Power-On (X19)

Table 53: Power-On connector (X19)

Manufacturer / number	Description
Samtec / TSM-104-01-LM-SV-P-TR	Pin header 2.54 mm 4 × 1-pin $I_N = 3 \text{ A}$ -55 °C to +125 °C

Table 54: Pin assignment touchscreen connectors (X2, X8)

Pin	Signal	Type	Remark
1	WAKEUP#	I	TQMa35 GPIO1_4
2	NC	-	RFU
3	NC	-	RFU
4	RFU	P	Ground

- low active signal, ↑ - element to VCC5V (pull up), ↓ - element to ground (pull down), → - element in series

Wiring see Illustration 27 on page 34.

4.2.3.9 Starterkit interfaces (X7, X10, X14, X15, X18, X31)

Almost every signal of the i.MX35 has two or more functions at the Starterkit interfaces. These can be taken from the i.MX35 Reference Manual.

4.2.3.9.1 Starterkit interface (X7)

Table 55: Starterkit interface connector (X7)

Manufacturer / number	Description
Fischer Elektronik / SL11-SMD-052-10-S	Pin header 2.54 mm 5 × 2-pin -40 °C to +105 °C

Table 56: Pin assignment Starterkit interface connector (X7)

Pin	Signal	Type	Remark
1	VCC3V3	P	Supply voltage 3.3 V
2	VCC5V	P	Supply voltage 5 V
3	VCC3V3	P	Supply voltage 3.3 V
4	VCC5V	P	Supply voltage 5 V
5	VCC12V	P	Supply voltage 12 V
6	VCC12V	P	Supply voltage 12 V
7	DGND	P	Ground
8	DGND	P	Ground
9	DGND	P	Ground
10	DGND	P	Ground

Wiring see Illustration 27 on page 34.

4.2.3.9.2 Starterkit interface (X10)

Table 57: Starterkit interface connector (X10)

Manufacturer / number	Description
Molex / 87759-3075	Pin header 2.00 mm, 15 × 2-pin -55 °C to +105 °C

Table 58: Pin assignment Starterkit interface connector (X10)

Pin	Signal	Type	Remark
1	DGND	P	Ground
2	DGND	P	Ground
3	WEIM_A0	O	External memory bus (WEIM bus) address line 0
4	WEIM_A1	O	External memory bus (WEIM bus) address line 1
5	WEIM_A2	O	External memory bus (WEIM bus) address line 2
6	WEIM_A3	O	External memory bus (WEIM bus) address line 3
7	WEIM_A4	O	External memory bus (WEIM bus) address line 4
8	WEIM_A5	O	External memory bus (WEIM bus) address line 5
9	WEIM_A6	O	External memory bus (WEIM bus) address line 6
10	WEIM_A7	O	External memory bus (WEIM bus) address line 7
11	WEIM_A8	O	External memory bus (WEIM bus) address line 8
12	WEIM_A9	O	External memory bus (WEIM bus) address line 9
13	WEIM_A10	O	External memory bus (WEIM bus) address line 10
14	WEIM_A11	O	External memory bus (WEIM bus) address line 11
15	WEIM_A12	O	External memory bus (WEIM bus) address line 12
16	WEIM_A13	O	External memory bus (WEIM bus) address line 13
17	WEIM_A14	O	External memory bus (WEIM bus) address line 14
18	WEIM_A15	O	External memory bus (WEIM bus) address line 15
19	WEIM_A16	O	External memory bus (WEIM bus) address line 16
20	WEIM_A17	O	External memory bus (WEIM bus) address line 17
21	WEIM_A18	O	External memory bus (WEIM bus) address line 18
22	WEIM_A19	O	External memory bus (WEIM bus) address line 19
23	WEIM_A20	O	External memory bus (WEIM bus) address line 20
24	WEIM_A21	O	External memory bus (WEIM bus) address line 21
25	WEIM_A22	O	External memory bus (WEIM bus) address line 22
26	WEIM_A23	O	External memory bus (WEIM bus) address line 23
27	WEIM_A24	O	External memory bus (WEIM bus) address line 24
28	WEIM_A25	O	External memory bus (WEIM bus) address line 25
29	DGND	P	Ground
30	DGND	P	Ground

Wiring see Illustration 27 on page 34.

4.2.3.9.3 Starterkit interface (X14)

Table 59: Starterkit interface connector (X14)

Manufacturer / number	Description
Molex / 87759-3075	Pin header 2.00 mm, 15 × 2-pin –55 °C to +105 °C

Table 60: Pin assignment Starterkit interface connector (X14)

Pin	Signal	Type	Remark
1	DGND	P	Ground
2	DGND	P	Ground
3	WEIM_D0	I/O	External memory bus (WEIM bus) data line 0
4	WEIM_D1	I/O	External memory bus (WEIM bus) data line 1
5	WEIM_D2	I/O	External memory bus (WEIM bus) data line 2
6	WEIM_D3	I/O	External memory bus (WEIM bus) data line 3
7	WEIM_D4	I/O	External memory bus (WEIM bus) data line 4
8	WEIM_D5	I/O	External memory bus (WEIM bus) data line 5
9	WEIM_D6	I/O	External memory bus (WEIM bus) data line 6
10	WEIM_D7	I/O	External memory bus (WEIM bus) data line 7
11	WEIM_D8	I/O	External memory bus (WEIM bus) data line 8
12	WEIM_D9	I/O	External memory bus (WEIM bus) data line 9
13	WEIM_D10	I/O	External memory bus (WEIM bus) data line 10
14	WEIM_D11	I/O	External memory bus (WEIM bus) data line 11
15	WEIM_D12	I/O	External memory bus (WEIM bus) data line 12
16	WEIM_D13	I/O	External memory bus (WEIM bus) data line 13
17	WEIM_D14	I/O	External memory bus (WEIM bus) data line 14
18	WEIM_D15	I/O	External memory bus (WEIM bus) data line 15
19	WEIM_DTACK#	I	External memory bus (WEIM bus) Data transfer acknowledge / wait
20	WEIM_LBA#	O	External memory bus (WEIM bus) Load burst address
21	WEIM_BUSCLK	O	External memory bus (WEIM bus) Burst Clock
22	WEIM_RW#	O	External memory bus (WEIM bus) Read / Write
23	WEIM_ECB#	I	External memory bus (WEIM bus) End current burst / wait
24	WEIM_OE#	O	External memory bus (WEIM bus) Out Enable
25	WEIM_EB0#	O	External memory bus (WEIM bus) Byte Enable 0
26	WEIM_CS1#	O	External memory bus (WEIM bus) Chip Select 1
27	WEIM_EB1#	O	External memory bus (WEIM bus) Byte Enable 1
28	WEIM_CS5#	O	External memory bus (WEIM bus) Chip Select 5
29	DGND	P	Ground
30	DGND	P	Ground

- low active signal, ↑ - element to VCC5V (pull up), ↓ - element to ground (pull down), → - element in series

Wiring see Illustration 27 on page 34.

4.2.3.9.4 Starterkit interface (X15)

Table 61: Starterkit interface connector (X15)

Manufacturer / number	Description
Molex / 87759-3075	Pin header 2.00 mm, 15 × 2-pin -55 °C to +105 °C

Table 62: Pin assignment Starterkit interface connector (X15)

Pin	Signal	Type	Remark
1	DGND	P	Ground
2	DGND	P	Ground
3	CSI_D0	I	Camera Sensor Interface data line 0
4	CSI_D1	I	Camera Sensor Interface data line 1
5	CSI_D2	I	Camera Sensor Interface data line 2
6	CSI_D3	I	Camera Sensor Interface data line 3
7	CSI_D4	I	Camera Sensor Interface data line 4
8	CSI_D5	I	Camera Sensor Interface data line 5
9	CSI_D6	I	Camera Sensor Interface data line 6
10	CSI_D7	I	Camera Sensor Interface data line 7
11	CSI_D8	I	Camera Sensor Interface data line 8
12	CSI_D9	I	Camera Sensor Interface data line 9
13	CSI_D10	I	Camera Sensor Interface data line 10
14	CSI_D11	I	Camera Sensor Interface data line 11
15	CSI_D12	I	Camera Sensor Interface data line 12
16	CSI_D13	I	Camera Sensor Interface data line 13
17	CSI_D14	I	Camera Sensor Interface data line 14
18	CSI_D15	I	Camera Sensor Interface data line 15
19	CSI_HSYNC	I	Camera Sensor Interface HSYNC
20	CSI_VSYNC	I	Camera Sensor Interface VSYNC
21	DGND	P	Ground
22	DGND	P	Ground
23	CSI_MCLK	O	Camera Sensor Interface Master Clock
24	CSI_PIXCLK	I	Camera Sensor Interface Pixel Clock
25	DGND	P	Ground
26	DGND	P	Ground
27	RS232_TX	O	RS232 Transmit (UART1)
28	RS232_RX	I	RS232 Receive (UART1)
29	DGND	P	Ground
30	DGND	P	Ground

Wiring see Illustration 27 on page 34.

4.2.3.9.5 Starterkit interface (X18)

Table 63: Starterkit interface connector (X18)

Manufacturer / number	Description
Molex / 87759-3075	Pin header 2.00 mm, 15 × 2-pin -55 °C to +105 °C

Table 64: Pin assignment Starterkit interface connector (X18)

Pin	Signal	Type	Remark
1	DGND	P	Ground
2	DGND	P	Ground
3	LD_BKL_ON	O	GPIO from PCA9554D to switch the backlight
4	LCD_LVDS-ENA	O	GPIO from PCA9554D to switch on the LVDS transmitter
5	LD_CONTRAST	O	PWM contrast
6	LD_REV	I/O	REV Signal for Sharp displays / GPIO1_3
7	LD_SPL	I/O	SPL Signal for Sharp displays / GPIO1_5
8	LD_CLS	I/O	CLS Signal for Sharp displays / GPIO1_4
9	DGND	P	Ground
10	DGND	P	Ground
11	USER_LED1	O	LED V77 red
12	DGND	P	Ground
13	USER_LED2	O	LED V77 yellow
14	I2C2_SCL	O	I ² C bus 2 clock
15	DGND	P	Ground
16	I2C2_SDA	I/O	I ² C bus 2 data
17	TIMER_CAPIN1	I	Timer Capture
18	DGND	P	Ground
19	DGND	P	Ground
20	I2C1_SCL	O	I ² C bus 1 clock
21	TIMER_CMPOUT1	O	Timer Compare
22	I2C1_SDA	I/O	I ² C bus 1 data
23	DGND	P	Ground
24	DGND	P	Ground
25	CAN1_RxD	I	CAN bus 1 receive
26	CAN2_RxD	I	CAN bus 2 receive
27	CAN1_TxD	O	CAN bus 1 transmit
28	CAN2_TxD	O	CAN bus 2 transmit
29	DGND	P	Ground
30	DGND	P	Ground

Wiring see Illustration 27 on page 34.

4.2.3.9.6 Starterkit interface (X31)

Table 65: Starterkit interface connector (X31)

Manufacturer / number	Description
Molex / 87759-3075	Pin header 2 00 mm, 15 × 2-pin -55 °C to +105 °C

Table 66: Pin assignment Starterkit interface connector (X31)

Pin	Signal	Type	Remark
1	DGND	P	Ground
2	DGND	P	Ground
3	COL0	I/O	4 × 4 KEYPAD
4	ROW0	I/O	
5	COL1	I/O	
6	ROW1	I/O	
7	COL2	I/O	
8	ROW2	I/O	
9	COL3	I/O	
10	ROW3	I/O	
11	DGND	P	Ground
12	DGND	P	Ground
13	DGND	P	Ground
14	OWDAT	I/O	Requires external pull-up resistor
15	SPI1_CLK	O	SPI1 clock
16	DGND	P	Ground
17	SPI1_MISO	I	SPI1 Master In Slave Out
18	VSTBY	O	Standby request to an external PMIC, switches after getting into a standby / low-power mode
19	SPI1_MOSI	O	SPI1 Master Out Slave In
20	DGND	P	Ground
21	SPI1_RDY	O	SPI1 Ready
22	GPIO3_5	I/O	GPIO
23	SPI1_SS0	O	SPI1 Slave Select 0
24	WD0G_RST#	I	Watchdog Reset
25	SPI1_SS1	O	SPI1 Slave Select 1
26	FLASH_RST#	O	Reset signal of the flash memory on the TQMa35
27	SPI1_SS3	O	SPI1 Slave Select 3
28	WP_ACC	O	WP/ACC signal of the flash memory on the TQMa35
29	DGND	P	Ground
30	DGND	P	Ground

- low active signal, ↑ - element to VCC5V (pull up), ↓ - element to ground (pull down), → - element in series

Wiring see Illustration 27 on page 34.

4.3 User's interfaces

4.3.1 Reset button (S2)

The reset button resets the CPU, the flash and the USB Host controller on the TQMa35. As a result the CPU generates a reset signal, which resets all other devices (RAM, Ethernet, etc.).

Table 67: Reset button (S2)

Manufacturer / number	Description
Knitter switch / TMSE 10 J-RA	Miniature pushbutton Minimum 100,000 operations Operating force 3 N \pm 1 N Max. 1.27 mm path -55 °C to +125 °C

4.3.2 Status-LEDs external (V77)

Table 68: External Status-LEDs (V77)

Manufacturer / number	Description
VS Optoelectronic / WU-2301	3-fold LED Red / green / yellow 0 °C to +80 °C

Three LEDs are implemented in addition to the status LEDs of both Ethernet jacks. Their function can be taken from the following table.

Table 69: Overview external LEDs

LED	Colour	Function / display
V77A	Green	User can define function
V77B	Yellow	User can define function
V77C	Red	Power-On (Voltage regulator indicates power-good)

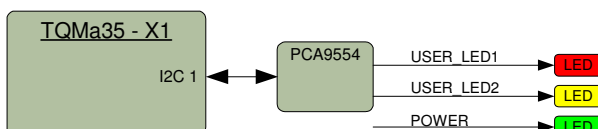


Illustration 37: Block diagram LED

For the control of the LEDs see Table 3 on page 14.

4.3.3 Status-LEDs internal (V22, V24, V25, V46, V78)

Internal LEDs are available to display other functions or status messages. The functions of the LED displays are listed in the following table.

Table 70: Overview internal LEDs

LED	Colour	Function / display
V22	Blue	Power-On (Voltage VCC5V is OK)
V24	Red	Over-current at the USB Host interface
V25	Red	Over-current at the USB OTG interface
V46	Green	Reset to module is active
V78	Green	Ethernet 1 works in full-duplex mode

4.3.4 DIP switch (S1, S3)

The STK-MBa35 possesses two DIP switches whose functions are listed in the following tables.

Table 71: DIP switch S1

Switch	ON	OFF (default)
S3-1	Termination CAN1 (120 Ω)	CAN1 not terminated
S3-2	Termination CAN2 (120 Ω)	CAN2 not terminated
S3-3 ⁽¹⁾	Slew rate configuration for CAN1 disabled	Slew rate configuration for CAN1 enabled
S3-4 ⁽¹⁾	Slew rate configuration for CAN2 disabled	Slew rate configuration for CAN2 enabled

Table 72: DIP switch S3

Switch	ON	OFF (default)
S3-1	No function	No function
S3-2	No function	No function
S3-3	RS485 RxD terminated (120 Ω)	RS485 RxD not terminated
S3-4	RS485 TxD terminated (120 Ω)	RS485 TxD not terminated

¹ To be able to use the switch functions, resistors ≥ 10 k Ω must be equipped for R45 or R50.

4.4 System components

4.4.1 Temperature sensor (D22)

Near the LCD connectors on the bottom side of the STK-MBa35 is a National Semiconductor LM75 temperature sensor. It can be read out via I²C1. The base address can be taken from the following table.

4.4.2 I²C address allocation

Table 73: I²C address allocation

I ² C bus	Position	Device	Address
1	STK-MBa35	Audio codec – SGLT5000	0x0A
1	STK-MBa35	GPO – PCA9554D	0x20
1	STK-MBa35	GPI, USERLED – PCA9554D	0x21
1	STK-MBa35	Temperature sensor – LM75	0x49
2	TQMa35	Temperature sensor – LM75	0x48
2	TQMa35	EEPROM – M24C46*	0x50
2	TQMa35	RTC – DS1339U-33	0x68

*) TQMa35 model dependent

4.4.3 Battery

To supply the RTC of the TQMa35, a lithium battery with very low self-discharge is used. The battery is socketed and, therefore, can be exchanged easily.

Table 74: RTC battery

Manufacturer / number	Description
e.g. Sony / CR2032	Lithium battery, typical capacity approx. 200 mAh / 3 V

Attention: Destruction or malfunction!



Reverse polarity of the battery can damage or destroy the device. Attention must be paid to the correct polarity of the battery.

5. SOFTWARE SPECIFICATION

No software is required for the STK-MBa35.

Suitable software is only required on the module TQMa35. It is not a part of this specification.

More information can be found in the [Support Wiki for the TQMa35](#).

6. MECHANICS SPECIFICATION

6.1 Construction

6.1.1 PCB outlines STK-MBa35

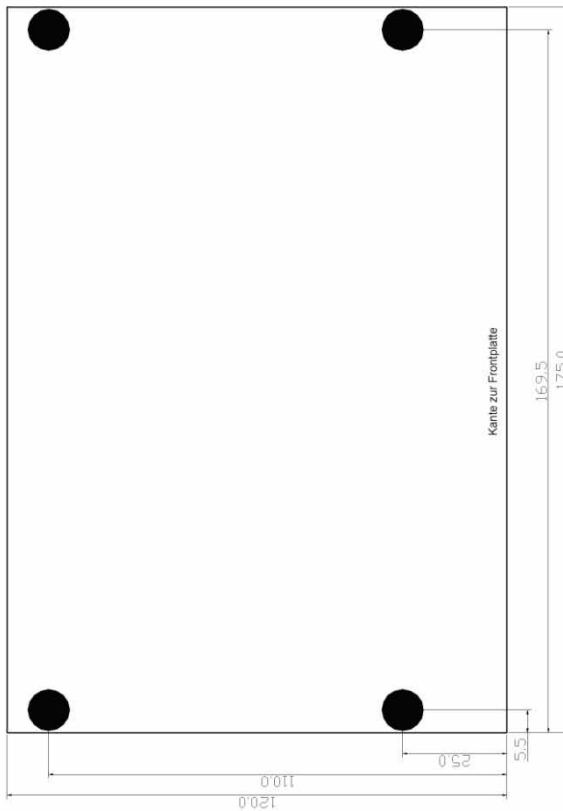


Illustration 38: PCB outlines STK-MBa35

6.1.2 STK-MBa35 top view

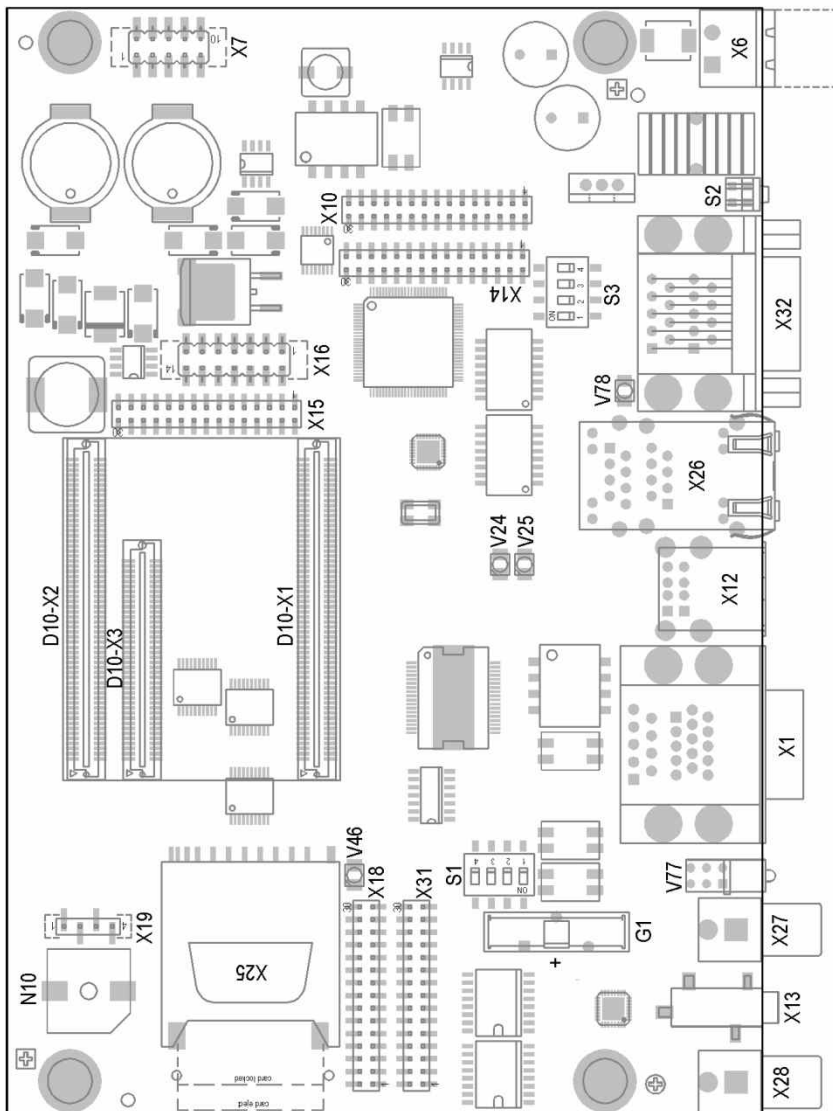


Illustration 39: Top view

6.1.3 STK-MBa35 bottom view

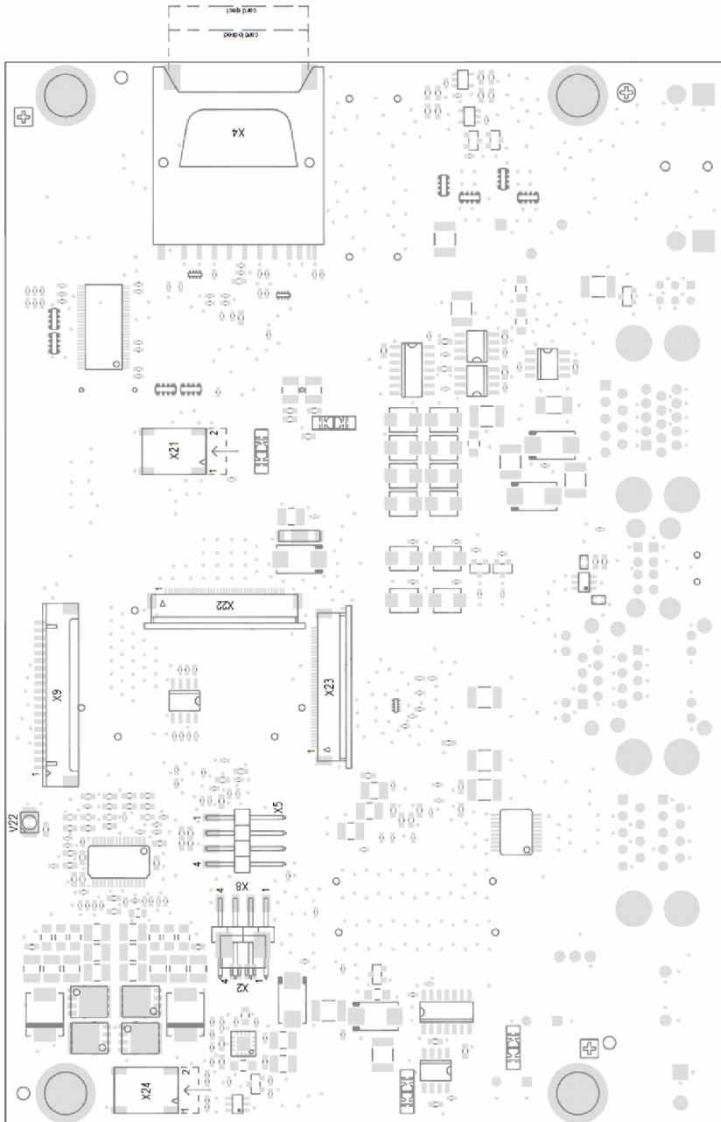


Illustration 40: Bottom view



7. REQUIREMENTS FOR THE SUPERIOR SYSTEM

7.1 Protection against external effects

The STK-MBa35 is not protected against dust, external impact and contact (IP00). An adequate protection has to be guaranteed by the surrounding system.

7.2 Thermal management

The main heat source is the TQMa35. Information to the cooling of the TQMa35 is to be taken from his specification.

8. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

8.1 EMC characteristics

The assembly TQMa35/STK-MBa35 is EMC tested in a TQ Blue-IPC. Current technical concepts were taken into consideration during the development to avoid or reduce EMC interference.

The STK-MBa35 meets the following EMC rules and EMC standards:

- EMC-Interference radiation:
Measurement of the electrically radiated emission for standard, residential, commercial and light industrial environments in the range of 30 MHz to 1 GHz according to DIN EN 61000-6-3 respective DIN EN 55022.
- EMC-Interference radiation:
Measurement of the electrically radiated emission for industrial environments in the range of 30 MHz to 1 GHz according to DIN EN 61000-6-4 respective DIN EN 55011.
- EMC-Immunity according to EN 61000-4-2²):
Electrostatic discharge immunity (ESD).
- EMC-Immunity according to EN 61000-4-3²):
Radiated radio frequency, electromagnetic field immunity.
- EMC-Immunity to fast transients according to EN 61000-4-4²):
Electrical fast transient (BURST).
- EMC-Immunity to surge according to EN 61000-4-5²):
Surge immunity test (SURGE).
In DC networks an inlet length of less than 10 m is assumed.
For the audit a reference power supply has to be defined / supplied.
Signal and I/O lines > 30 m must be checked for SURGE.
- EMC-Immunity according to EN 61000-4-6²):
Immunity to conducted disturbances, induced by radio-frequency fields.
- EMC-Immunity according to EN 61000-4-11²):
Immunity to voltage dips, voltage variation and short interruptions in the mains supply (VOLTAGE DIPS).
- EMC-Immunity according to EN 61000-4-29³):
Immunity to voltage dips and short interruptions on the DC input power supply.

8.2 Operational safety and personal security

Due to the occurring voltages (≤ 36 V DC), tests with respect to the operational and personal safety have not been carried out.

² The test level and test criteria are taken from the generic standards EN 61000-6-1 and EN 61000-6-2.

³ The test criteria are not fixed here yet, because there are still no generic standards or product standards on which to base this standard. When required the test criteria have to be defined with the customer.

9. CLIMATIC AND OPERATIONAL CONDITIONS

Permitted component temperature:	0 °C to +70 °C
Permitted storage temperature:	-40 °C to +100 °C
Relative air humidity (operation / storing):	10 % to 90 % (not condensing)
Protection class:	IP00

9.1 Protection against external effects

See section 7.1 Protection against external effects on page 65.

9.2 Reliability and product life

The device is designed for a typical product life of five years.

Connectors of middle grade, which guarantee at least 100 mating cycles, are used for all external accessible interfaces.

9.3 Displays used

The display manufacturers permit a number of pixel defects. These vary depending on the manufacturer and type of display. The permissible error of the pixel display manufacturers (warranty claims) is usually set very high. TQ-Systems GmbH allows pixel errors in the display.

9.4 Batteries

9.4.1 General notes

Due to technical reasons a battery is necessary for this product. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used. To allow a separate disposal, batteries are generally only mounted in sockets.

9.4.2 Lithium battery

The requirements concerning special provision 188 of the ADR (section 3.3) are complied with for Lithium batteries. There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 g (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 g per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2 g (except for lithium ion batteries for which a lithium content of not more than 8 g per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.
- During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

9.5 Environment protection

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.

To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.

The energy consumption of this subassembly is minimised by suitable measures.

Printed pc-boards are delivered in reusable packaging. Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material.

Because now there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (**polychlorinated biphenyls**).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
(source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
(source of information: BGBl I 1996, 1382, (1997, 2860)
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
(source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
(source of information: BGBl I 2001, 3379)

This information is to be seen as notes.

Tests or certifications were not carried out with respect to that.

9.6 RoHS compliance

The STK-MBa35 is manufactured RoHS compliant. TQ-Systems GmbH issues the RoHS conformity declaration.

9.7 WEEE regulation

TQ-Systems GmbH, which markets the product, is responsible for the observance of the WEEE regulation.

TQ-Systems GmbH

Mühlstraße 2 | Gut Delling | 82229 Seefeld
info@tq-group.com | www.tq-group.com

Technology in Quality

