User's Manual

R-IN32M3 Series

User's Manual (Board design edition)

- R-IN32M3-EC
- R-IN32M3-CL

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Document number : R18UZ0021EJ0204
Issue date : Dec 25, 2014

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Instructions for the use of product

In this section, the precautions are described for over whole of CMOS device.
Please refer to this manual about individual precaution.
When there is a mention unlike the text of this manual, a mention of the text takes first priority

1.Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

-The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2.Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

-The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3.Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

-The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4.Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

-When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

How to use this manual

1. Purpose and target readers

This manual is intended for users who wish to understand the functions of Industrial Ethernet network LSI "R-IN32M3-EC/CL" for designing application of it.

It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.
The mark "<R>" means the updated point in this revision. The mark "<R>" let users search for the updated point in this document.

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such. Please be understanding of this beforehand. In addition, because we make document at development, planning of each core, the related document may be the document for individual customers. Last four digits of document number(described as ****) indicate version information of each document. Please download the latest document from our web site and refer to it.

The document related to R-IN32M3 Series

Document name	Document number
R-IN32M3 Series Datasheet	R18DS0008EJ****
R-IN32M3-EC User's Manual	R18UZ0003EJ****
R-IN32M3-CL User's Manual	R18UZ0005EJ****
R-IN32M3 Series User's Manual Peripheral functions	R18UZ0007EJ****
R-IN32M3 Series Programming Manual (Driver edition)	R18UZ0009EJ****
R-IN32M3 Series Programming Manual (OS edition)	R18UZ0011EJ****
R-IN32M3 Series User's Manual TCP/IP stack	R18UZ0019EJ****
R-IN32M3 Series User's Manual Peripheral Board design edition	This manual

The document related to OS

Document name	Document number
µITRON 4.0 Specification Ver.4.00.00 (ITRON Committee, TRON ASSOCIATION)	-

"µITRON 4.0 Specification" is the open real-time kernel specification developed led by TRON ASSOCIATION.

The µITRON 4.0 specification of this document is the extract from "µITRON 4.0 Specification Ver.4.00.00". Please refer to "µITRON 4.0 Specification Ver.4.00.00" about the whole aspect of specifications.

In addition, You can obtain "µITRON 4.0 Specification" from website of TRON ASSOCIATION

2. Notation of Numbers and Symbols

Weight in data notation: Left is high-order column, right is low-order column

Active low notation:

xxxZ (capital letter Z after pin name or signal name)

or xxx_N (capital letter _N after pin name or signal name)

or xxnx (pin name or signal name contains small letter n)

Note:

explanation of (Note) in the text

Caution:

Item deserving extra attention

Remark:

Supplementary explanation to the text

Numeric notation:

Binary ⋯ xxxx , xxxxB or n'bxxxx (n bits)

Decimal ⋯ xxxx

Hexadecimal ⋯ xxxxH or n'hxxxx (n bits)

Prefixes representing powers of 2 (address space, memory capacity):

K (kilo)⋯ $2^{10} = 1024$

M (mega)⋯ $2^{20} = 1024^2$

G (giga)⋯ $2^{30} = 1024^3$

Data Type:

Word ⋯ 32 bits

Halfword ⋯ 16 bits

Byte ⋯ 8 bits

Contents

1. Outline

This manual is intended for being used by engineers that work on a circuit and PCB design that is equipped with an Ethernet communication LSI from the R-IN32M3 series made by Renesas Electronics. Target devices are the R-IN32M3-EC and R-IN32M3-CL devices.

It is recommended to study this manual carefully and to follow the recommendations during the circuit and board design.

2. Power/Reset pins

2.1 Power-on/off sequence

Power structure of the R-IN32M3 series is internal power (VDD10 : 1.0V) and I/O power (VDD33 : 3.3V) and PHY power supply (VDD15 : 1.5V) . (PHY power is subject only R-IN32M3-EC.)

Power is recommended to put the I/O power after switching on the internal power supply. In addition, power-off is recommend internal power-off after cut-off of I/O power.

In the case of supplying internal power after I/O power,

Please note that I/O value becomes an indefinite due to uncertain mode while I/O is powered on but internal power isn't , regardless of an input(output)mode. Also, 3.3 V must be applied to the I/O pins only after applying the power supply voltages.

Power on/off time difference, that regardless of the power-on sequence, it does not matter which power supply is applied to (or removed from) the device first (VDD1/IVDD or VDD3/EVDD), but it is recommended to ensure 100ms or less time difference between the application or removal of each power supply. The 100ms or less time measurement is based on the period from 10% to 90% of each voltage range.

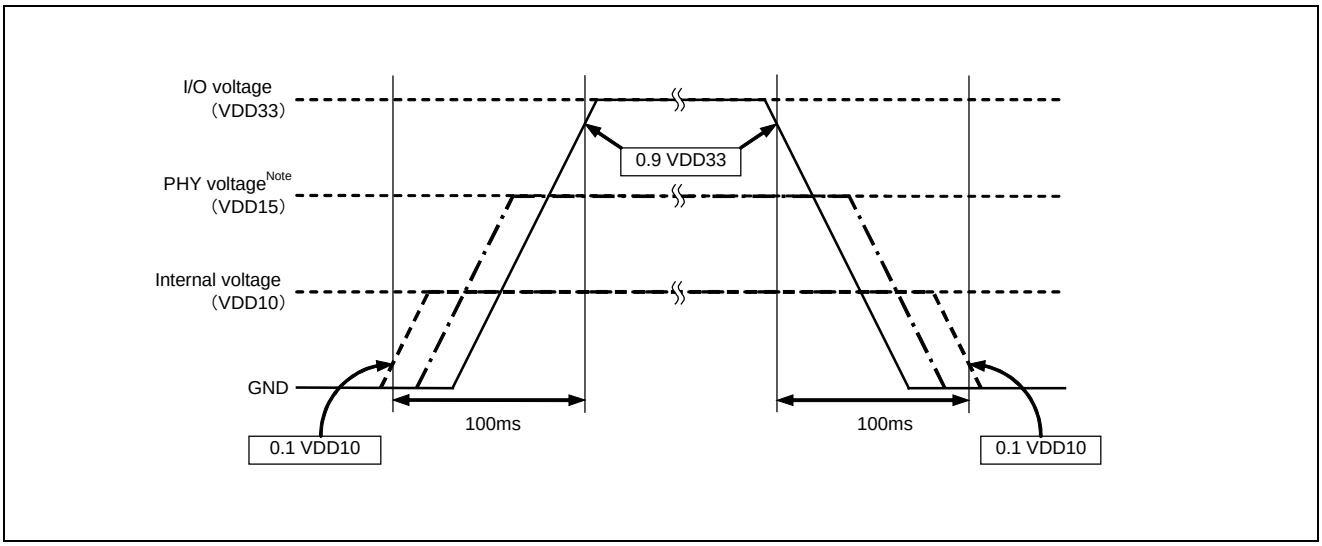


Figure 2.1 Recommended sequence of Power-on/off

Note The timing for PHY power supply voltage VDD15 only needs to be observed, when the internal regulator in the R-IN32M3-EC device is not used.

2.2 Power supply pins

This is a power supply pins list of R-IN32M3.
Please connect these pins according to the description given in the “Connection example” column.

Terminal name	Feature	Connection example
PLL_VDD	PLL voltage (VDD) (1.0V)	Refer to “4. PLL power pins”.
PLL_GND	PLL GND potential (GND)	Refer to “4. PLL power pins”.
VDD33	I/Os voltage (3.3V)	Supply a power supply from the power unit such as a regulator or DC-DC converter.
VDD10	Internal voltage (1.0V)	Supply a power supply from the power unit such as a regulator or DC-DC converter.
GND	GND potential (GND)	Connect GND of system board.
VDDQ_MII[Note2]	Ethernet I/Os voltage (3.3V)	Supply a power supply from the power unit such as a regulator or DC-DC converter.
LX[Note1]	Built-in regulator 1.5V output	Refer to “5.1 Built-in regulator used”.
AVDD_REG[Note1]	Analog power supply for built-in regulator (3.3V)	
AGND_REG[Note1]	Analog GND potential for built-in regulator (GND)	
BVDD[Note1]	Power supply for built-in regulator (3.3V)	
BGND[Note1]	GND potential for built-in regulator (GND)	
FB[Note1]	Feedback input for built-in regulator	
EXTRES[Note1]	Reference resistance joining pin for Ethernet PHY	Connect to AGND through 12.4kΩ±1%.
P0VDDARXTX[Note1]	Analog power supply for Rx/Tx pin (1.5V) - Port 0	Refer to “7.1 Ethernet PHY power supply pin”.
P1VDDARXTX[Note1]	Analog power supply for Rx/Tx pin (1.5V) - Port 1	
VDDACB[Note1]	Analog power suppuly for Ethernet PHY (3.3V)	
AGND[Note1]	Analog GND potential for PHY (3.3V)	
VDD15[Note1]	Core voltage for Ethernet PHY (1.5V)	
VDDAPLL[Note1]	Analog power supply for Ethernet PHY (1.5V)	
VSSAPLLCB[Note1]	Analog GND potential for Ethernet PHY (GND)	
VDD33ESD[Note1]	Analog test power supply for Ethernet PHY (3.3V)	
VDDQ_PECL_B0[Note1]	PECL buffer power supply (3.3V)	
VDDQ_PECL_B1[Note1]	PECL buffer power supply (3.3V)	

Note1. R-IN32M3-EC only
2. R-IN32M3-CL only

2.3 Reset pins

Terminal name	Feature	Connection example
RESETZ	Reset input	–
HOTRESETZ[note]	Hot reset input	–
PONRZ	Power-on reset input for built in RAM	–
TRSTZ	JTAG reset signal	Refer to “17.JTAG/trace pins”
RSTOUTZ	Reset output to outside	–

note R-IN32M3-CL only

3. Clock input pins

3.1 Features of pins

The following table shows the pin functions for clock supply to the device.

Pin name	I/O	Features
XT1	IN	・External resonator connection pin. ・When external clock input mode is used(OSCTH = 1), please set XT1 to the low level.
XT2	IN/OUT	・External resonator connection pins. ・When “OSCTH = 0”, this pin is the output. ・When external clock input mode is used (OSCTH = 1), please input the clock from an external oscillator to XT2.
OSCTH	IN	・Select the clock source to be connected to the clock pin. Low level : Connect the resonator XT2 and XT1. High level : Connect the oscillator XT2.

3.2 Note the oscillation circuit configuration

The R-IN32M3 devices have an internal oscillator and the user can build the required clock supply simply from an external crystal and some fixed components (or alternatively with an external oscillator driving XT2). As the oscillation circuit operates at high frequencies is should be designed according to the rules for analog circuits. To achieve stable operation of the oscillation circuit, it may be required to try several combinations of fixed components based on the recommendations of the crystal or resonator manufacturer. Generally the following points should be observed

The clock supply circuit including the fixed components should be placed near to the clock input pins of the R-IN32M3 (XT1, XT2). All clock related connections should be as short as possible.

Ground connections of the load capacitors should be as short and wide as possible.

The clock supply circuit should be separated from other sensitive signal and communication lines.

Preferably the clock supply circuit is surrounded with a DGND pattern.

The used devices for the external clock may have their own design recommendations. They should also be considered.

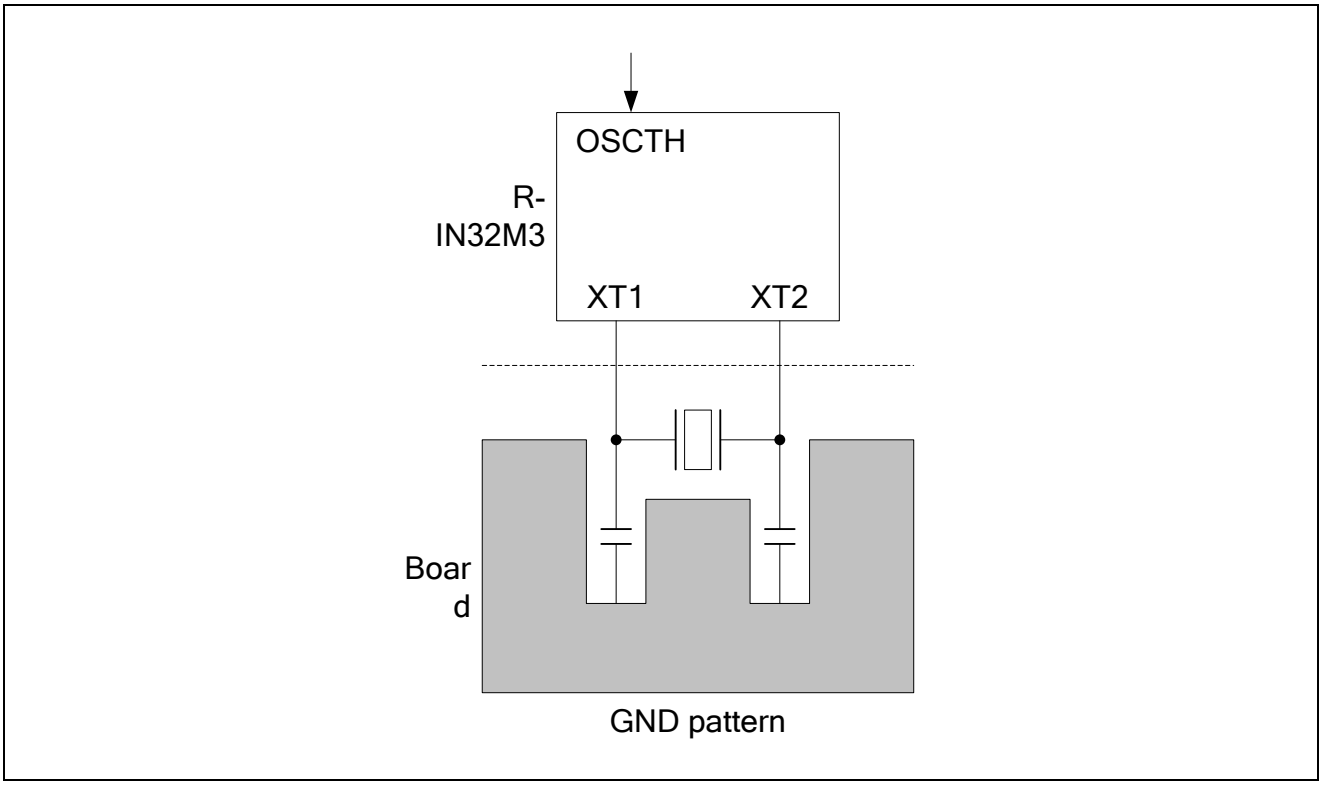


Figure 3.1 GND pattern example of external constant part

The values for the external components should be evaluated based on the actual PCB design and on the actually used oscillator respectively resonator. Typically a “safe” operation area can be found over several boards and different combinations of external components; then component selection for production should be done in such a way that operation is always safe.

3.3 Oscillation circuit configuration example

The following figure shows typical examples of oscillation circuits.

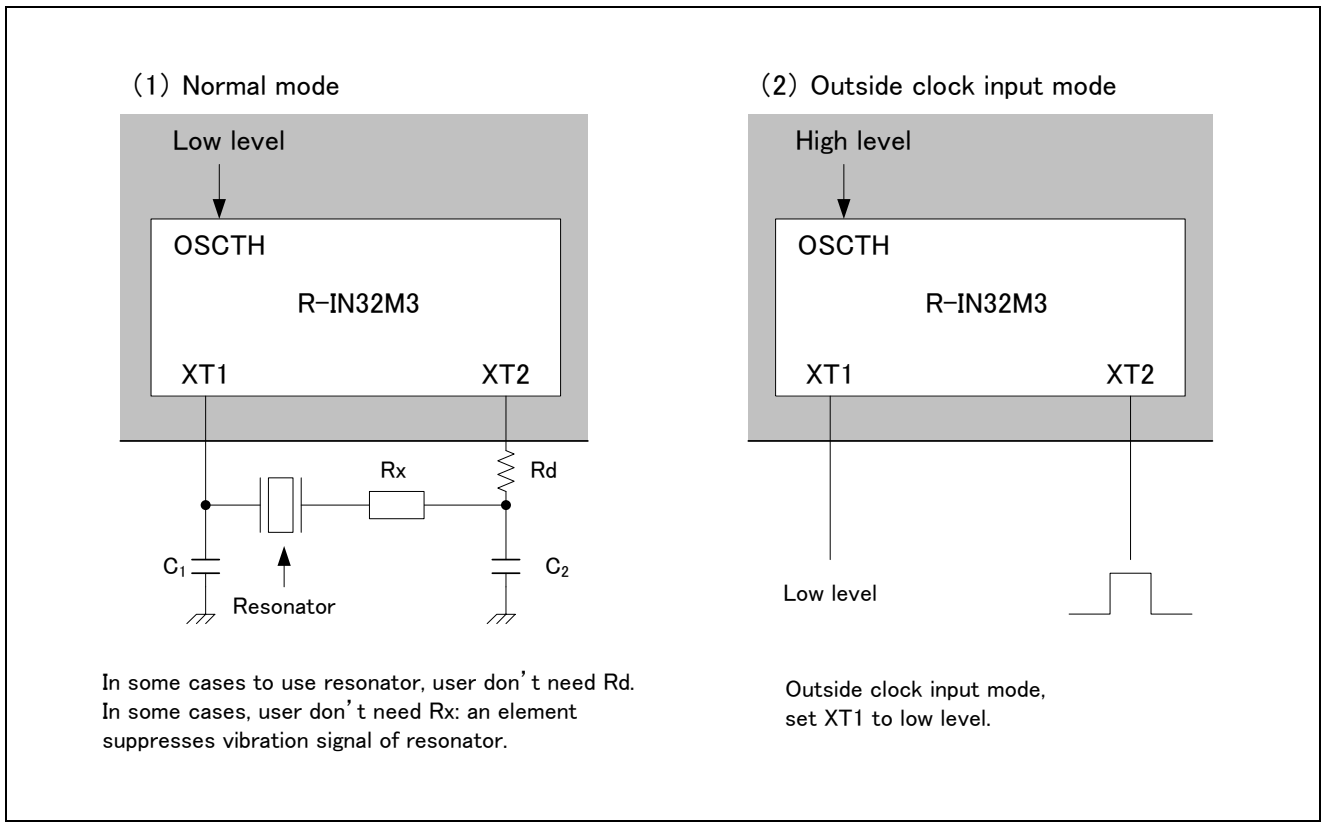


Figure 3.2 Configuration example of the oscillation circuit

Caution R-IN32M3's input is fixed 25MHz. Load of resonator should be 8pF or lower. But it depends on the resonator and the design situation. Please consult the design information given by the resonator manufacturer

4. PLL power pins

The PLL circuit is susceptible to noise. To reduce the influence of noise, it is recommended to place filters in the power supply pin of the PLL. Also if user avoid the interference noise of the PLL board and power supply, the usage of user user ferrite beads(FB).

4.1 Recommended FILTER composition

Figure 4.1 shows recommended FILTER composition.

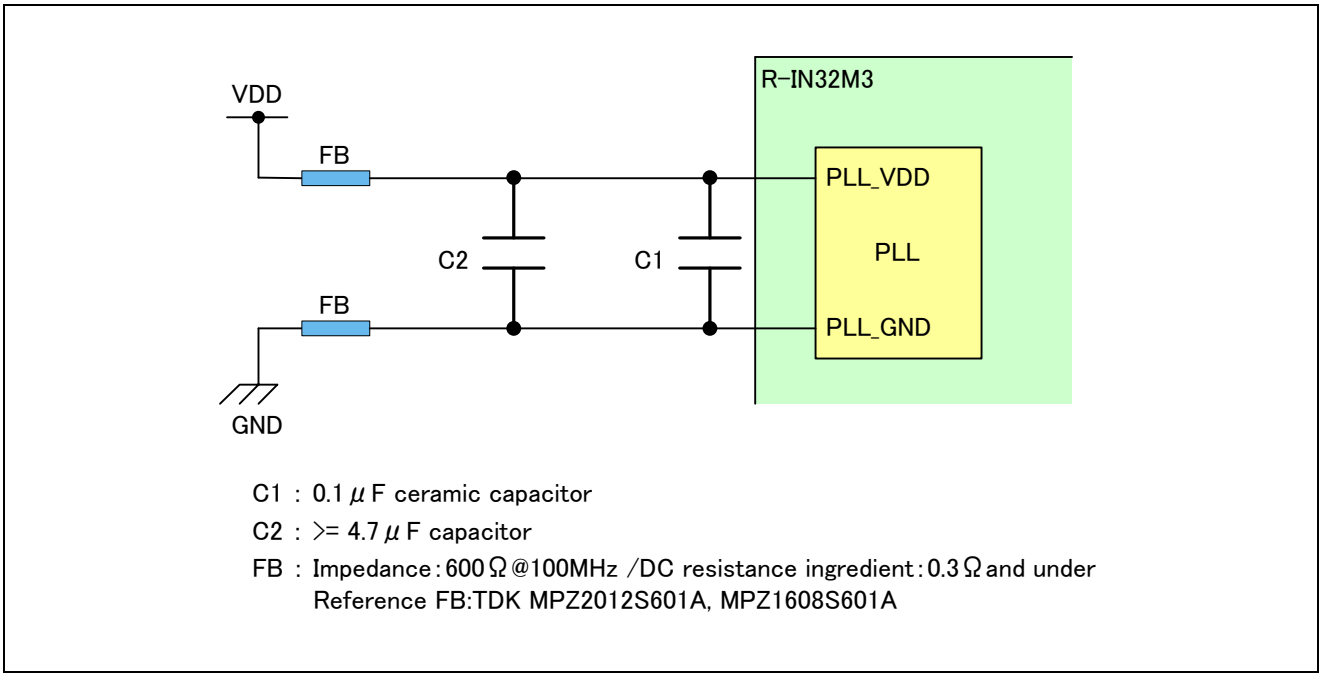


Figure 4.1 Recommended FILTER composition

Caution Put C1 as close as possible to the PLL_VDD and PLL_GND pins. .
C2 placement is less critical and there is no problem even if it can't be arranged as close to the R-IN32M3 as C1.

4.2 Notes on placement of FILTER components

Figure 4.2 is a image seen from the back of the board and shows the recommended placement and layout for the PLL power supply components.

Ceramic capacitor C1 (0.1µF) should be placed in immediate vicinity of the PLL_VDD and PLL_GND pins. A direct via connection from the related signal pads to the bottom layer of the board is recommended so that C1 can be placed below R-IN32M3.The PLL_VDD and PLL_GND signals should then be routed to the C2 position and then connected to VDD respectively GND via the ferrite beads FB. The coupling of the ferrite beads to VDD and GND should have as low resistance as possible. We therefore propose connect the related FB pads to VDD and GND with several (parallel) vias as shown in Figure 4.2.

It should be avoided to route high-frequency signal lines parallel to the PLL_VDD and PLL_GND lines.

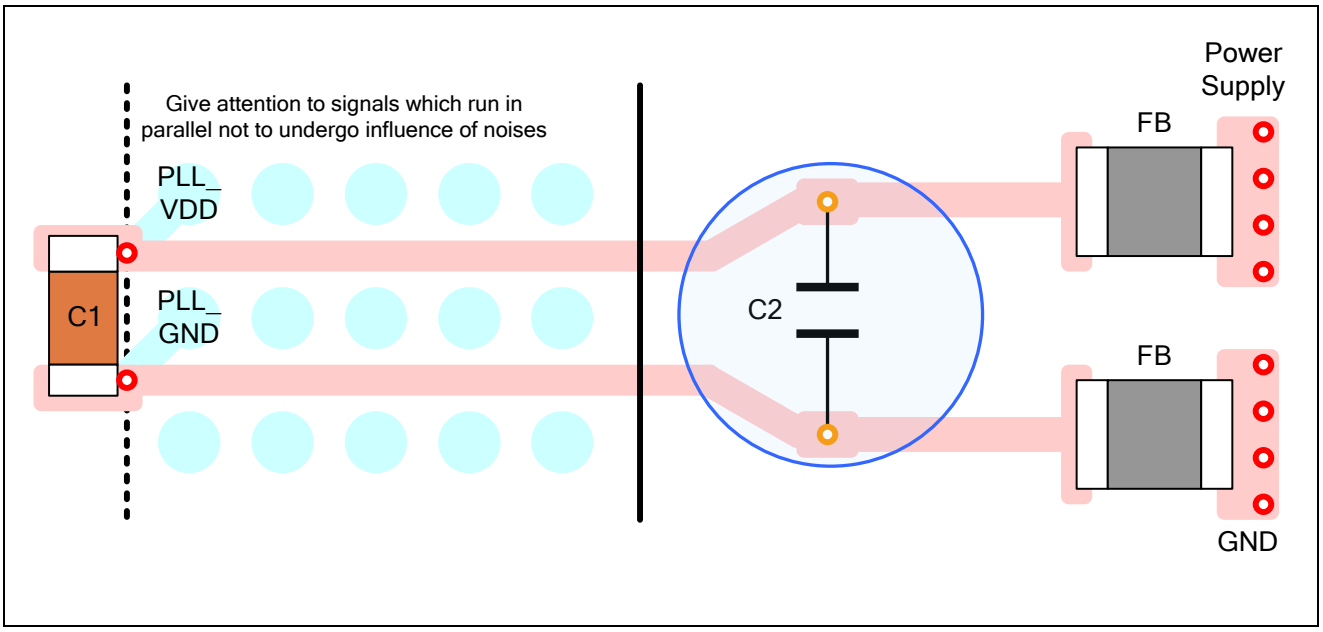


Figure 4.2 Image viewd from the back of the board

Caution PLL_VDD and PLL_GND lines should be as short and thick as possible in PCB wiring.
If wires are long, effects of Xtalk can easily occur because the LC portion of wiring increase.

5. Built-in regulator pin

R-IN32M3-EC needs 1.5V supply to VDD15, VDDAPLL, PxVDDARXTX pin as the inner power supply for Ethernet PHY.

Power supply generation at outside is equipped with a regulator inside R-IN32M3-EC, and unnecessary. When not using a built-in regulator, refer to "5.2 Built-in regulator unused" and design.

5.1 Built-in regulator used

Make wiring and layout as follows at the time of the built-in regulator use.

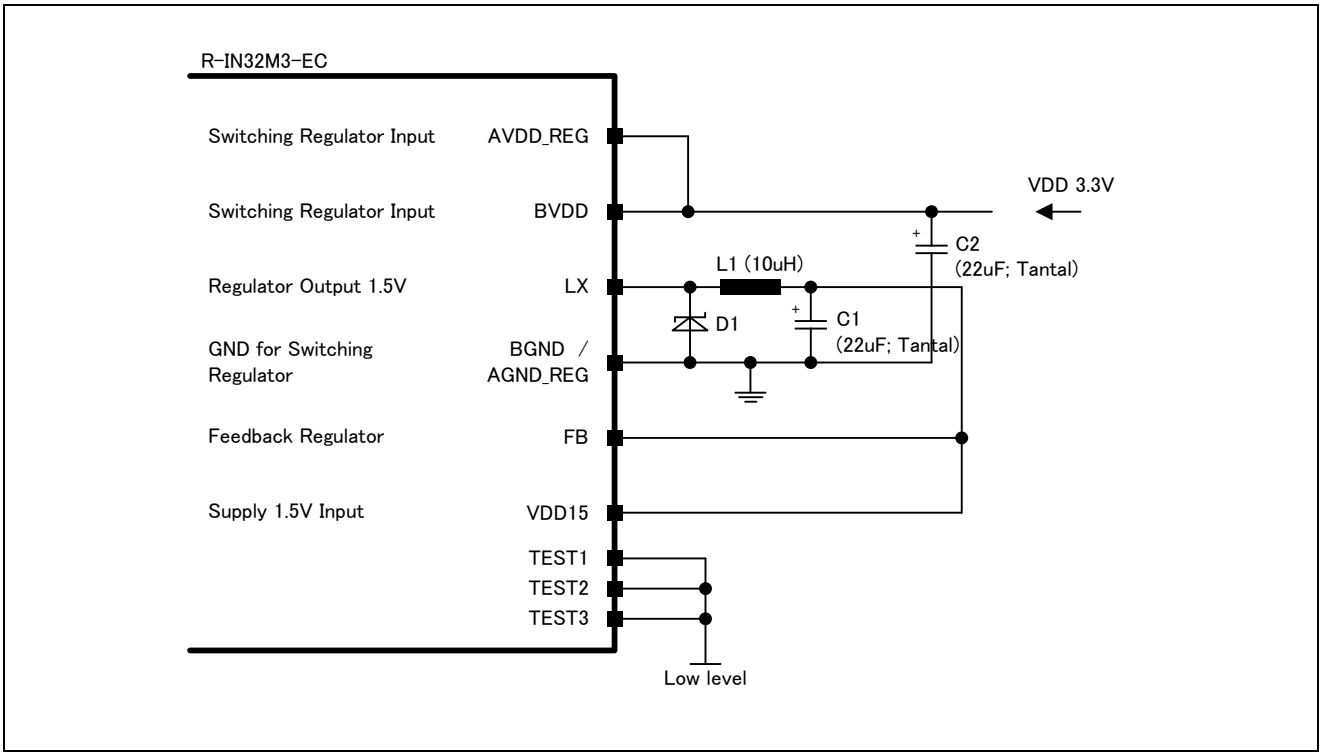


Figure 5.1 Wiring example of the regurator unit (internal regulator used)

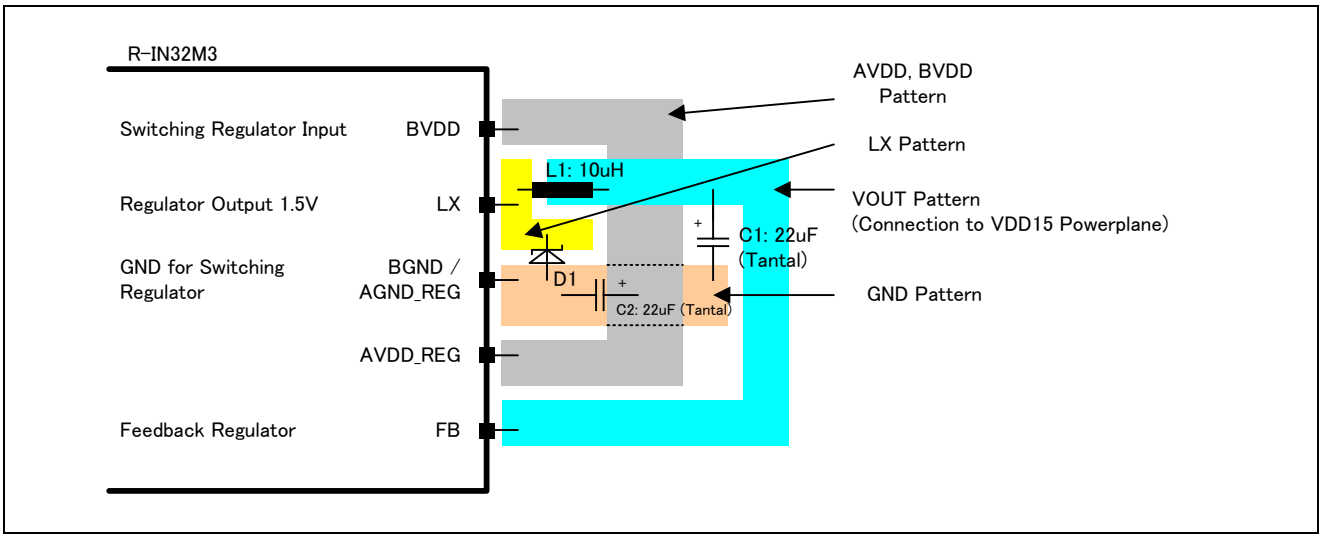


Figure 5.2 Layout example of the regulator section

Use recommended parts

- D1 : Schottky diode (STPS1L30UPBF, Vishay)
- L1 : Inductor 10 μ H (VLCF5028T provided by TDK)
- C1, C2 : Capacitor 22 μ F Tantal (ESR = 300m Ω), PSLB21A226M, NEC Tokin

5.2 Built-in regulator unused

The built-in regulator when not in user, wiring as follows.

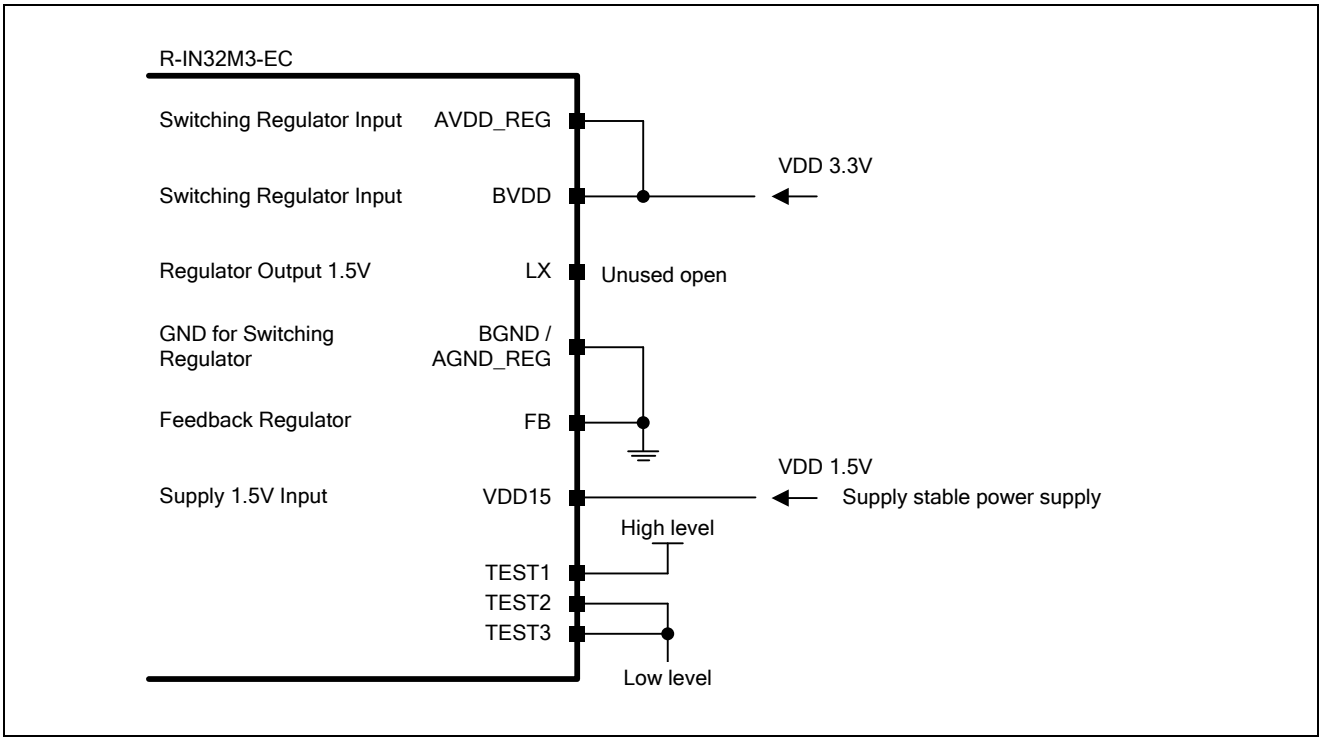


Figure 5.3 Wiring example of the regulator unit (internal regulator is not used)

6. GPIO port pins

GPIO is general purpose IO port. Regarding internal structure, please refer below document.

R-IN32M3-EC: User's Manual R-IN32M3-EC 2.3.5 Port Signals
R-IN32M3-CL: User's Manual R-IN32M3-CL 2.5.5 Port Signals

7. Ethernet PHY pins

7.1 Ethernet PHY power supply pins

Analog power supply pin for the built-in Ethernet PHY of R-IN32M3-EC recommends power separation by ferrite beads(FB), filters and configuration as follows.

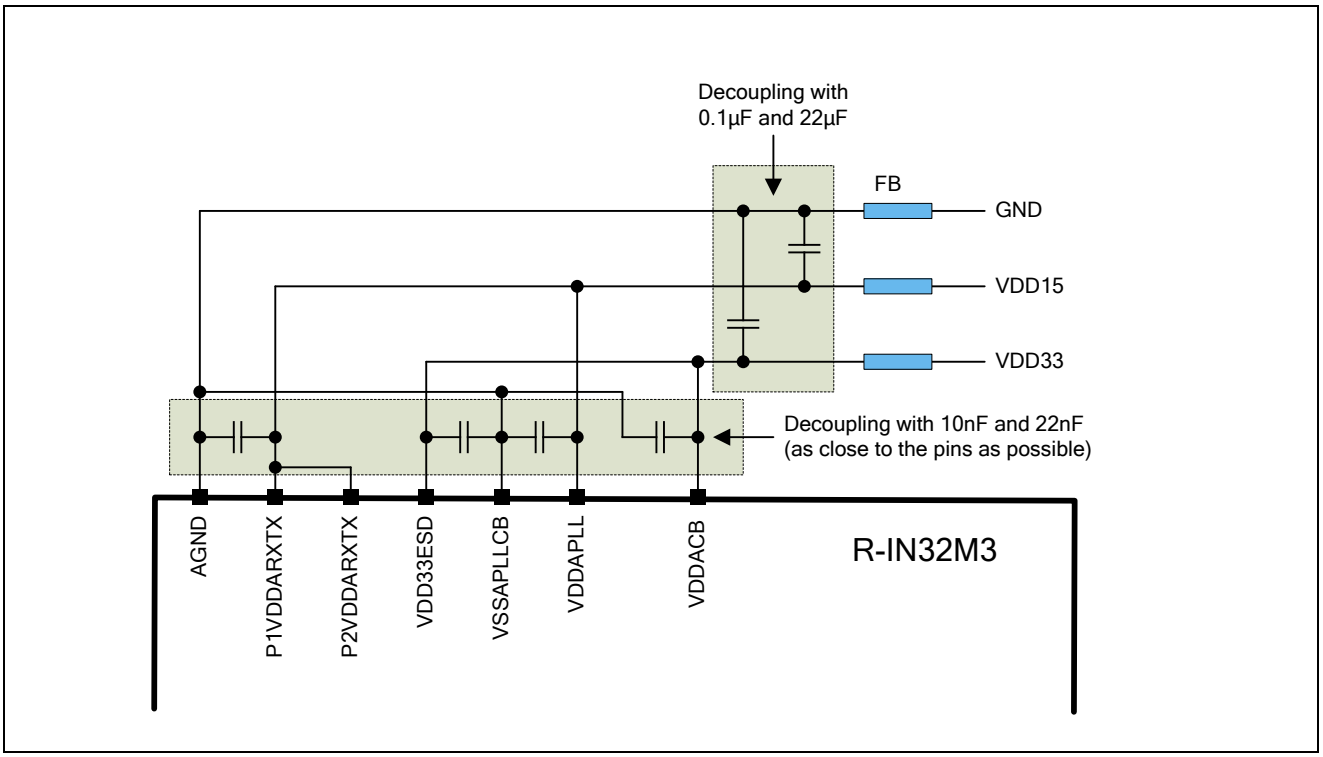


Figure 7.1 Wiring example of the regulator unit

7.2 100Base -TX pins

This is an example of connection using the pulse transformer.

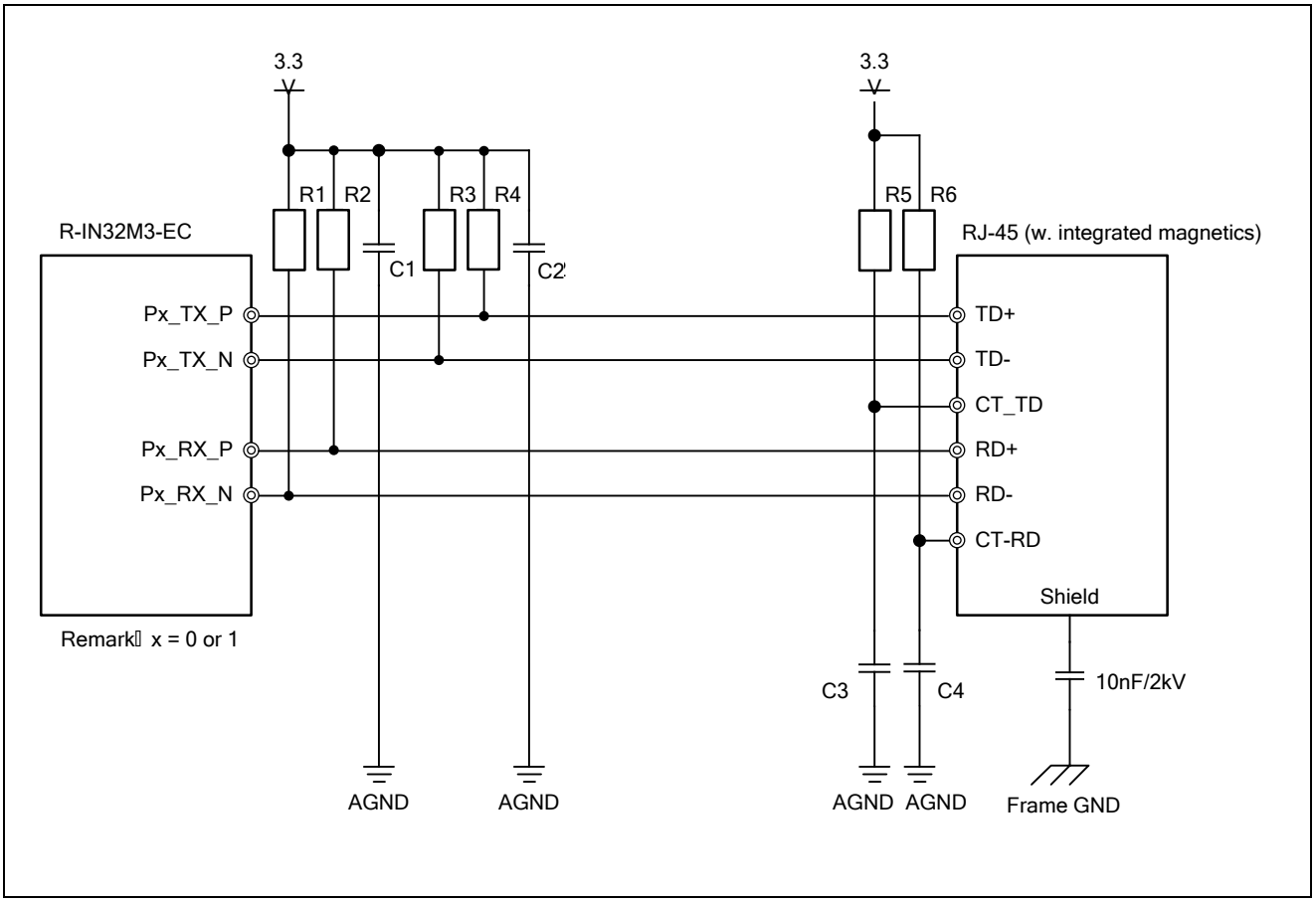


Figure 7.2 Connection example R-IN32M3-EC and RJ-45 connector(pulse transformer built-in)

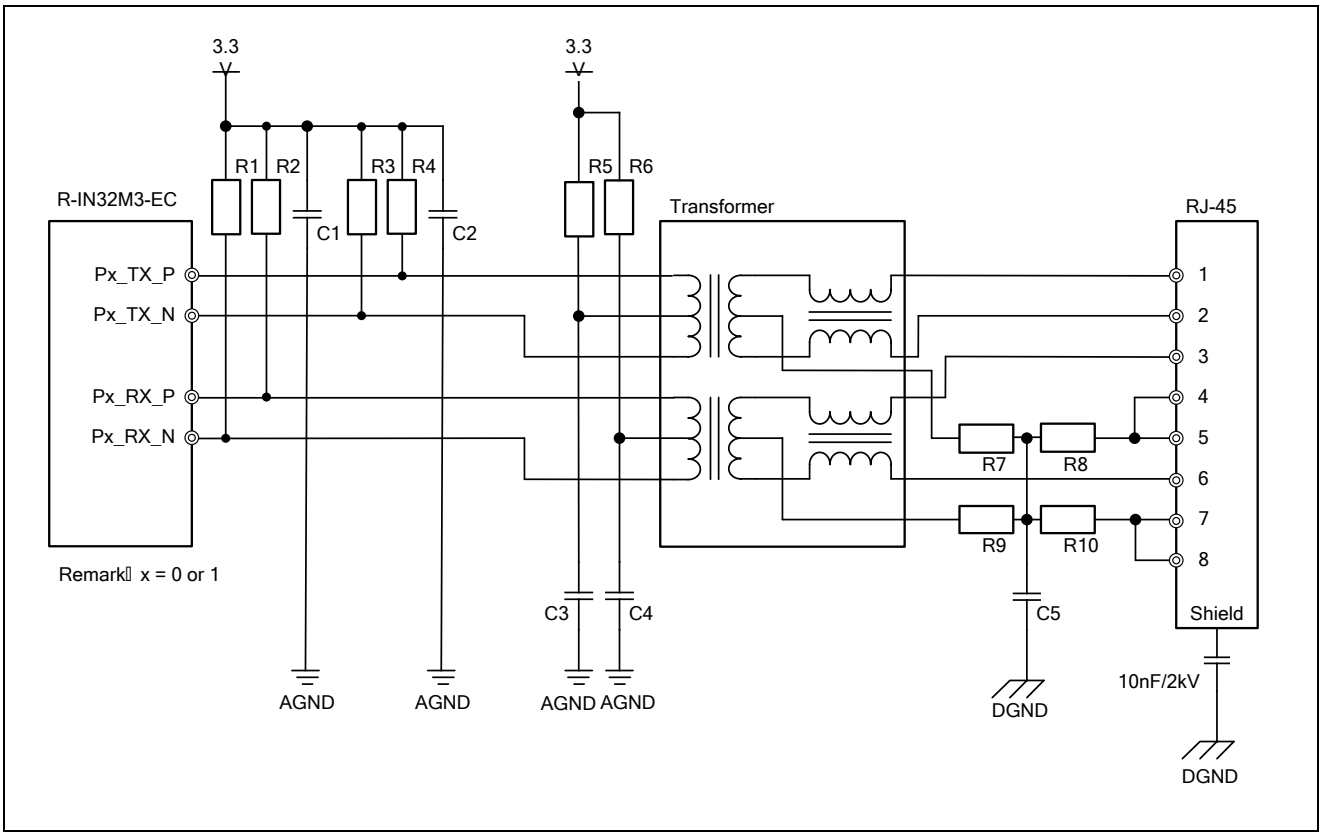


Figure 7.3 Connection example R-IN32M3-EC and Pulse transformer and RJ-45 connector

Table 7.1 Parts list (100Base-TX interface)

Part	Type	Characteristics	Recommended components
R1, R2, R3, R4	Resistor	49.9Ω ±1% 1/16W	–
R5, R6	Resistor	10Ω ±1% 1/16W	–
R7, R8, R9, R10	Resistor	75Ω ±1% 1/16W	–
C1	Capacitor	10nF - 100nF	–
C2	Capacitor	10nF - 100nF	–
C3	Capacitor	10nF - 22nF	–
C4	Capacitor	10nF - 22nF	–
C5	Capacitor	4.7nF±10%	–
Transformer		One channel	Pulse Electronics H1012NL, H1102NL
		Twochannel	Pulse Electronics H1270N+, HX1294
RJ45 with integrated magnetics		Two channel	Pulse Electronics JG0-0031NL

The wiring on the board, note the following.

- Long wires should be avoided. R-IN32M3 and, the transformer, and the connector should be placed together as close as possible.
- Crossing of differential traces with other lines and among each other should be avoided. The components should be placed that way that crossing of differential pairs of TxP/N and RxP/N is not necessary.
- Differential lines should be routed straight and as short as possible.
- Lines should bend with 135 degree angle or more. (Figure 7.4)
- Traces between R-IN32M3-EC, transformer and RJ-45 connector should be designed with a differential impedance of 100Ω±10% and with an impedance of 50Ω related to GND.
- The traces of a differential pair should match in length. 0.5mm is the maximum deviation. Adjustments of the length should be done at the connector, device or transformer.
- Additional to the length the single traces should be designed symmetrical. They should be parallel and routed in the same layer with continuous width and a preferable fixed spacing. Components, vias and connections should also be symmetrical.
- Stubs should be avoided.
- Preferable is a large edge gap at differential pairs (‘g’ in Figure 7.2). An empty space of five times of the trace width between differential pair and other signals, planes or components is recommended.
- Differential lines should not cross edges of the GND/supply plane, other planes or voids in the layer below. For continuous impedance a GND plane in the layer below is preferable.
- Beneath the magnetics no lines or planes should be routed.
- Preferable differential pairs should be routed via as little vias as possible. If vias are necessary please note the following:

(a) Vias of the related plane (e.g. AGND) should be placed near the signal vias. The distance between signal via and GND via should be equal to the distance between the layers to avoid a discontinuity of the impedance. (See “Figure 7.6”)

(b) Void and no planes between and around the signal vias (see Figure 7.3). Metal of planes close to the differential vias could influence the impedance.

(c) The diameter of the vias should be almost equal to the trace width. (See ‘w’ in Figure 7.3)

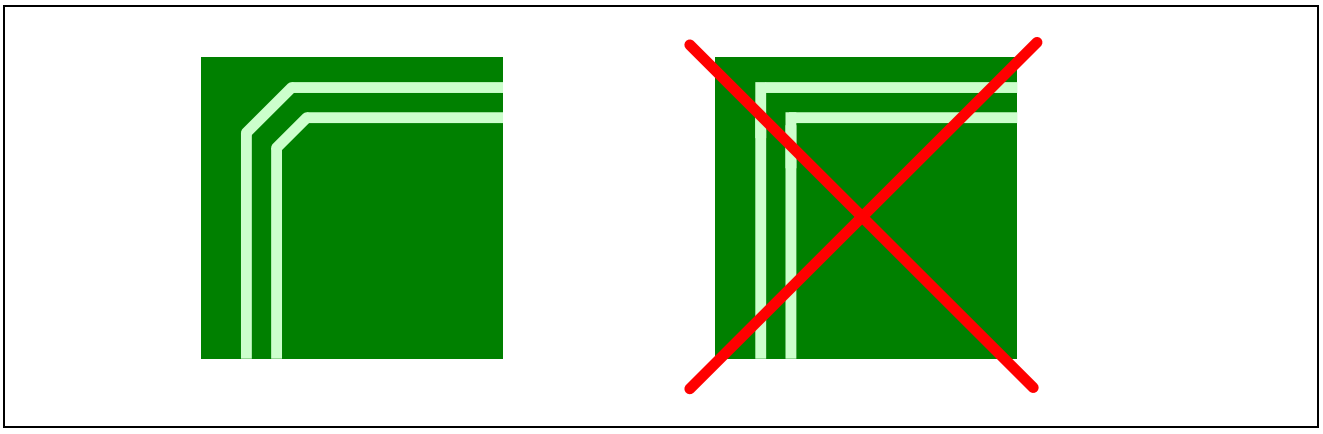


Figure 7.4 Wiring example of the differential signal transmission line (1)

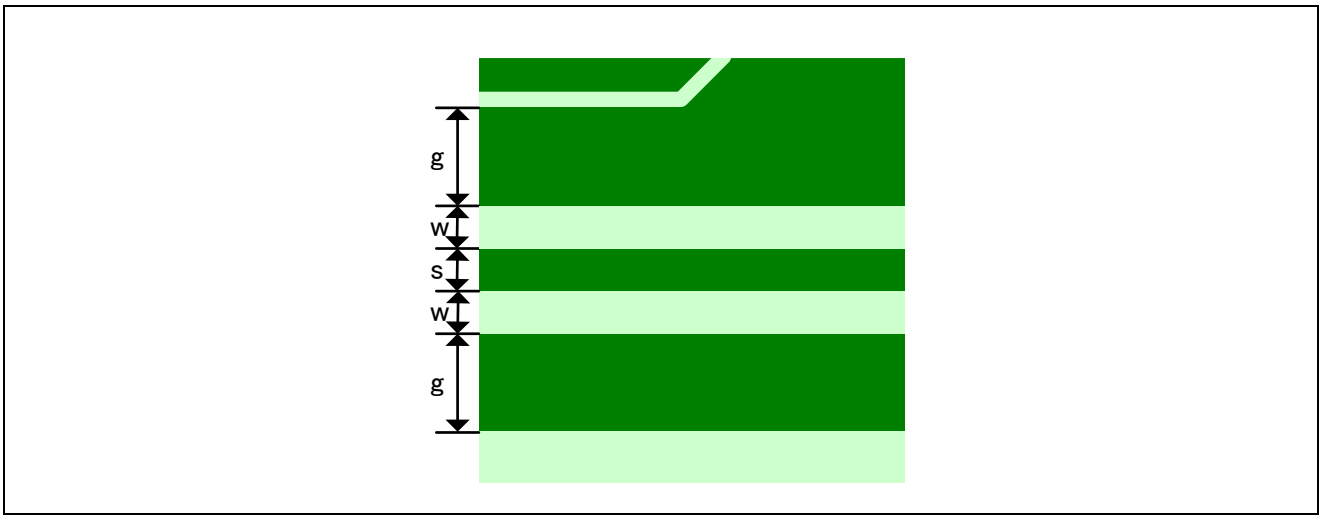


Figure 7.5 Wiring example of the differential signal transmission line (2)

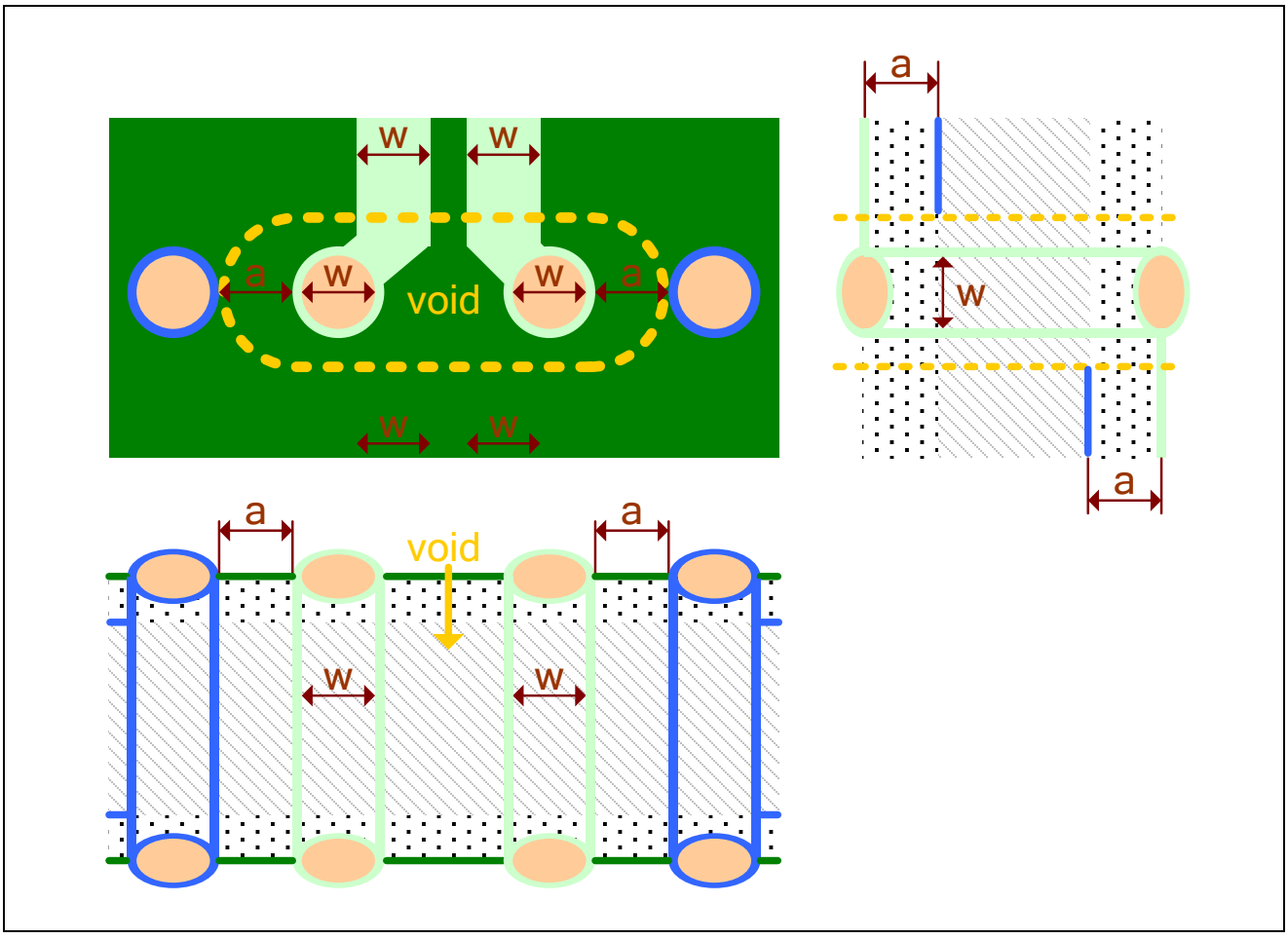


Figure 7.6 Wiring example of the differential signal transmission line (3)

7.3 100Base-FX pins (Optical fiber)

Connection example with an optical fiber module is indicated below.

Notes of the differential signal transmission line, please refer to "7.2 100Base -TX pins".

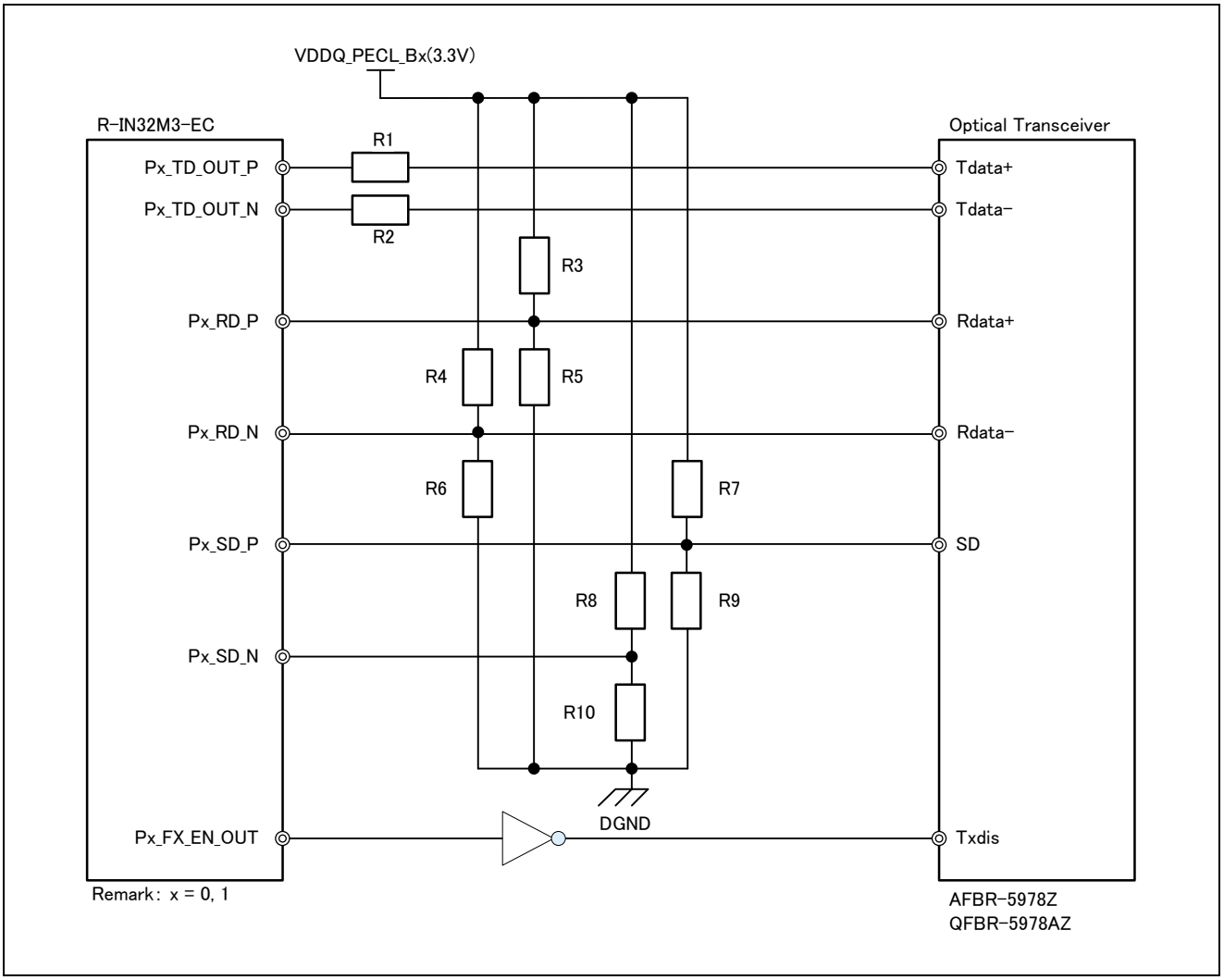


Figure 7.7 Interface circuit with optical transceiver

Table 7.2 Part list (100Base-FX interface)

Part	Type	Characteristics	Recommended components
R1, R2	Resistor	150Ω ±1%	−
R3, R4, R7	Resistor	130Ω ±1%	−
R5, R6, R9	Resistor	82Ω ±1%	−
R8	Resistor	86.6Ω ±1%	−
R10	Resistor	127Ω ±1%	−
Optical Transceiver		One channel	AvagoTechnologies AFBR-5978Z, QFBR-5978AZ

8. GMII pins (R-IN32M3-CL only)

Figure 8.1 shows a connection image of R-IN32M3-CL and Gigabit Ethernet PHY.

The damping register value should be 33 ohm within a tolerance of 5%, and the damping resistors should be put in the nearest point of R-IN32M3-CL. And wires of target pins (which is GTXC, TXDx, TXEN and TXER) are recommended to be short and the same length.

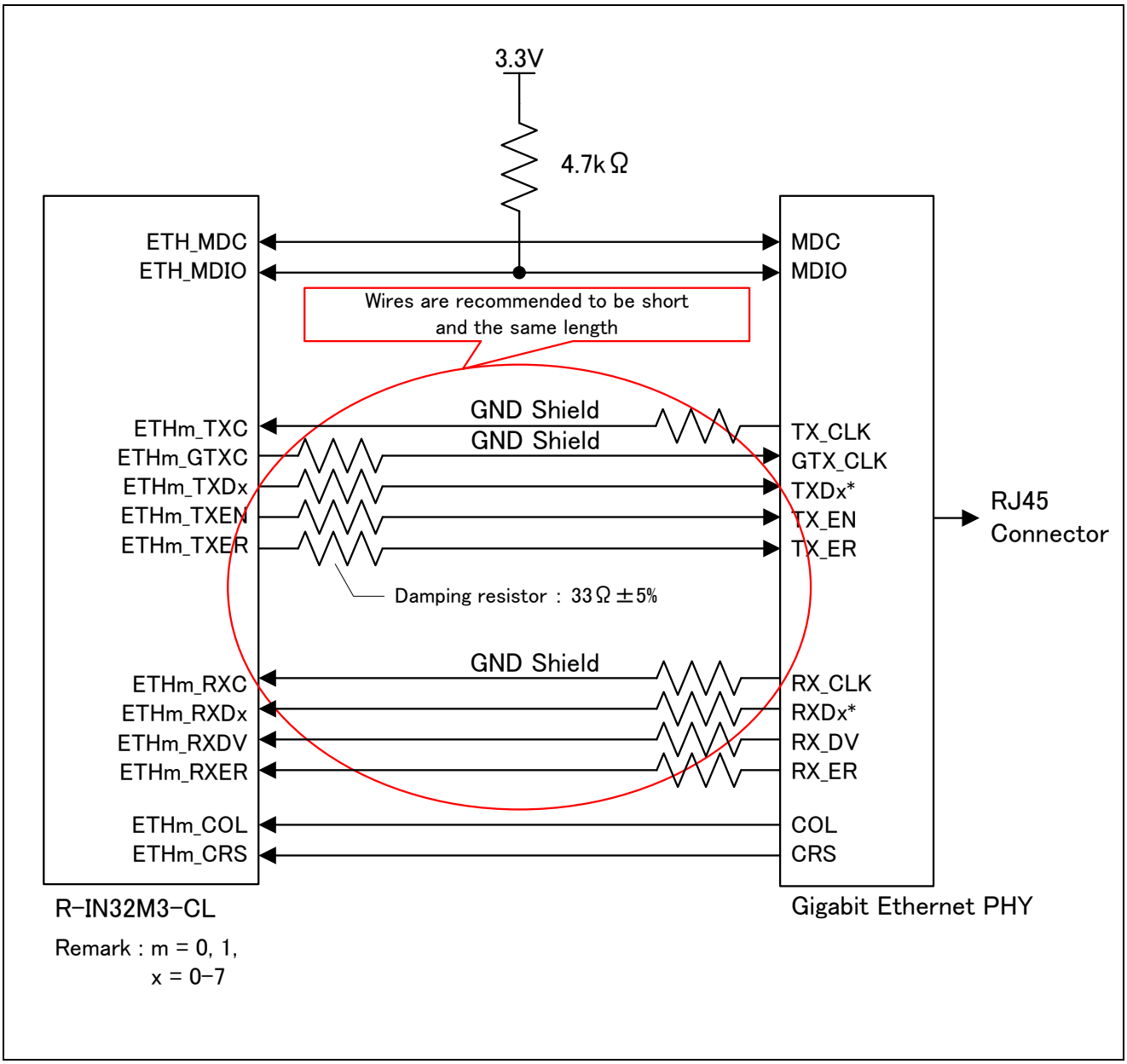


Figure 8.1 Connection image of R-IN32M3-CL and PHY

8.1 Selection of GMII peripheral components

Please select the parts with care to the following.

Selection of PHY

Full-duplex products IEEE802.3 1000BASE-T.

Pe parts that has the auto-negotiation function.

Parts with a GMII interface.

Parts that has the auto MDI/MDIX negotiation function.

Operable parts at 125MHz about MDC clock frequency.

Selection of the crystal cscillator for PHY

Regarding Jitter and frequency, select the parts to adapt to the requirement of the PHY

8.2 Circuit design around GMII

Please design the GMII peripheral circuits with care to the following.

Wiring of GMII

Please put the damping resistor of overshoot/undershoot protection.

For PHY address

Please be set to the same address as the port mumber of the R-IN32M3-CL and The PHY address.

Connect to the PHY assigned address1 to MAC port1, And Connect to the PHY assigned address2 to MAC port2

8.3 Pattern desing around GMII

Please design the GMII peripheral circuits pattern with care to the following. And t]he wiring pattern should be the shortest and choose width and layer thickness to be 50Ω。

Do not bend at 45 degrees or less to signal pattern.

The power /GND pattern, please be wired with a thick pattern as much as possible.

9. CC-Link pins

The connection example for CC-Link Remote device station is shown in Figure 9.1. <R>

Notes on the implementation of the CC-Link, so be found in the CC-Link Association issued "CC-Link specification (implementation defined Edition)" in (BAP-05027), please look there.
Please contact (CLPA) CC-Link Association about the claim of the material.

http://www.cc-link.org/jp/support/material/index.html
For document requests, contact :
CC-Link Partner Association (CLPA) TEL : 052-919-1588 / FAX : 052-916-8655
Email : info@cc-link.org

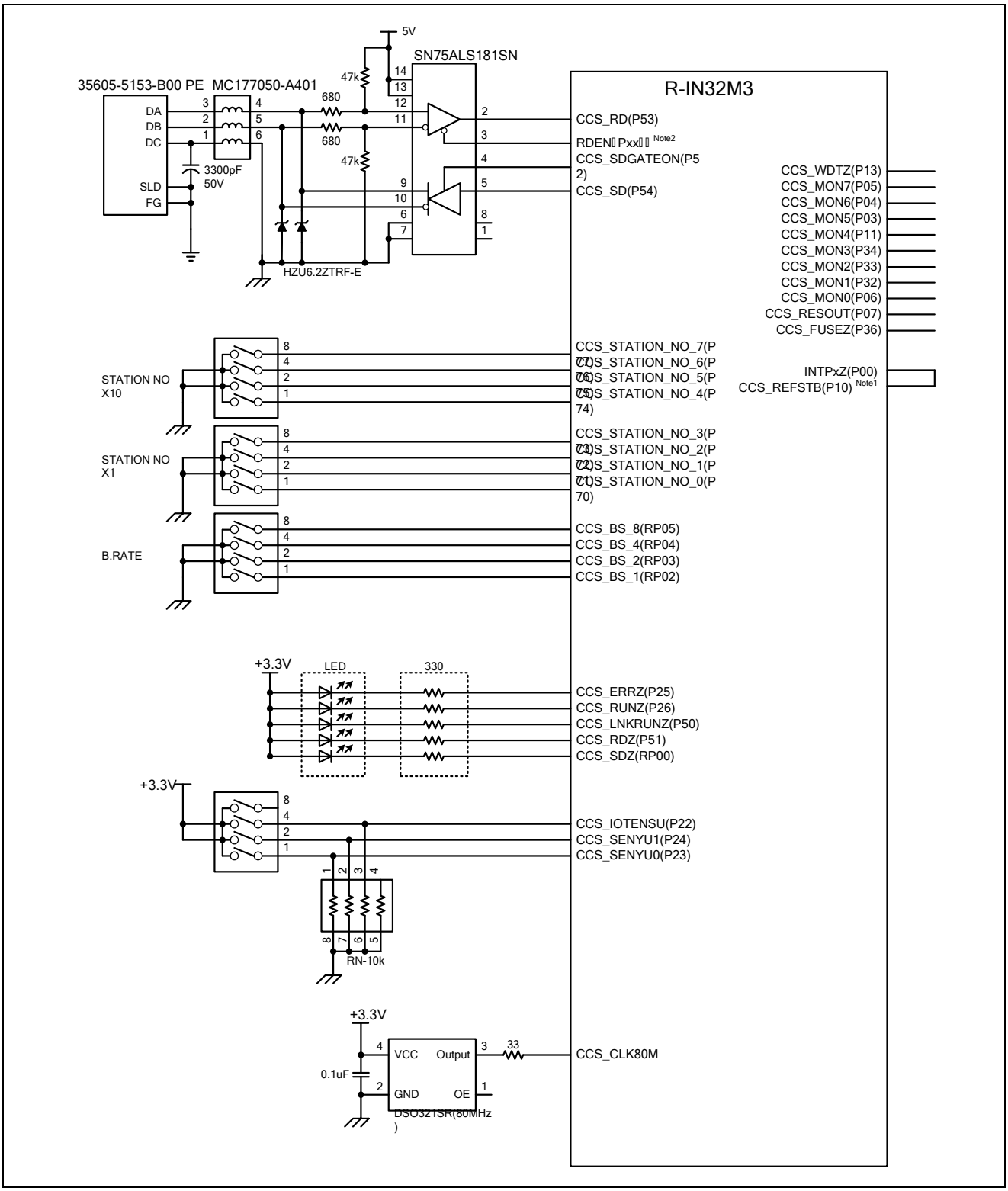


Figure 9.1 The connection example for CC-Link Remote device station <R>

Note1 CCS_REFSTB(P10) pin is needed to connect to the port pin which has external interrupt function (INTPZ).

Note2 RZEN pin should be connected to a general output port.

10. Notes of CC-Link IE Field use (only R-IN32M3-CL)

When user does boot with the external memory boot mode, external serial flash ROM boot mode and instruction RAM boot mode, please input high level to P33 and P34 pin during reset.

If you enter a low-level to P33, P34 pin during reset, you can not access the CC-Link IE Field from the CPU of the R-IN32M3.

11. External MPU/memory interface pins

This LSI is able to connect to an external MPU or memory.

The connection mode is decided as Table 11.1 by the signal level of the MEMIFSEL pin, MEMCSEL pin and HIFSYNC pin.

Table 11.1 The mode selecton of external MPU/memory connection

Mode setting			The connection mode to external parts
MEMIFSEL	MEMCSEL	HIFSYNC	
Low	Low	-	External memory interface Asynchronous SRAM MEMC
	High	-	External memory interface Synchronous SRAM MEMC
High	Low	Low	External MPU interface Asynchronous SRAM interface
		High	External MPU interface Synchronous SRAM interface
	High	Low	Prohibition of a setup
		High	External MPU interface Synchronous SRAM type transmission mode

From the next section, the connection example for each modes is shown.

11.1 External MPU interface

In order to use the internal resource of external host MPU to R-IN32M3, the external microcomputer interface is established.

External MPU I/F is interface to connect external MPU. External MPU I/F's signal is assigned same ports to both use with an external memory interface, and can be used as External MPU interface in case of setting MEMIFSEL to High level.

The external microcomputer interface is equivalent to the asynchronous SRAM interface and the synchronous SRAM interface. When the level of a HIFSYNC pin is high-level, it becomes a synchronous SRAM interface, and when HIFSYNC is a low level, it becomes an asynchronous SRAM interface. (Please refer the Table 11.1.)

Moreover, an external microcomputer interface supports the synchronous SRAM type transmission of a clock synchronizer type so that mass data can be accessed at high speed. MEMIFSEL pin and MEMCSEL pin can be used by making it high-level.

11.1.1 Asynchronous SRAM interface

The following figure shows a general connection example with the asynchronous SRAM interface mode, when the external MPU connects as the host.

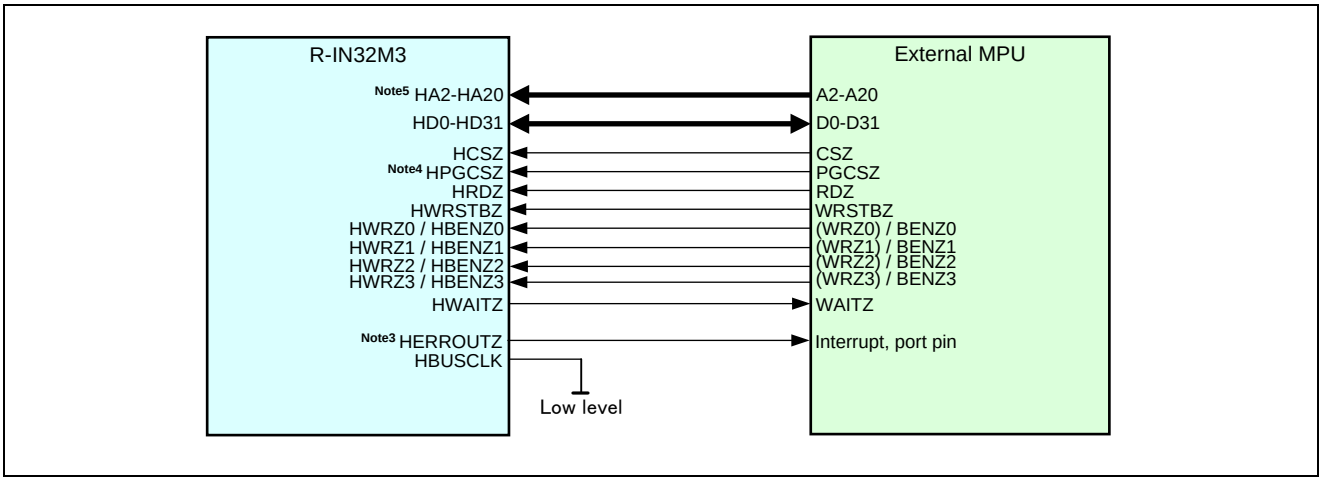


Figure 11.1 The connection example with external MPU (32bit bus, asynchronous SRAM interface mode)

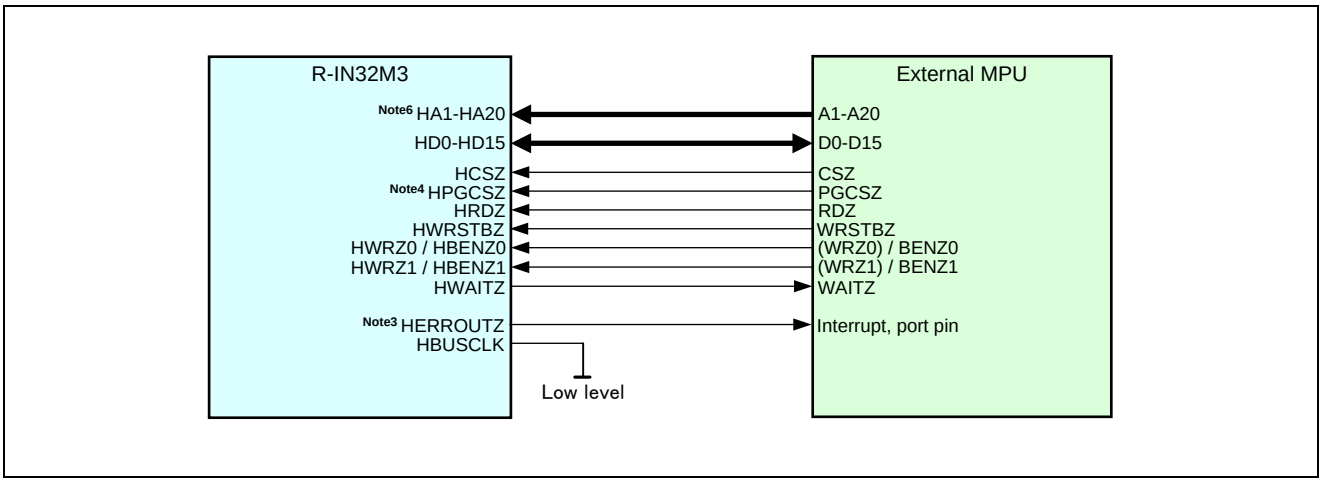


Figure 11.2 The connection example with external MPU (16bit bus, asynchronous SRAM interface mode)

Note1 The detail of signal connection is depend on the bus interface spec of the host MPU. Please confirm the product spec of MPU which is connected to this LSI.

Note2 HWRZ0-HWRZ3 and HBENZ0-HBENZ3 is assigned to the same pin. The function is decided by the signal level of HWRZSEL pin.

Note3 The connection of the HERROUTZ signal is not indispensable. Please connect this signal to a interrupt or general port pin etc., according to the need.

Note4 PGCSZ signal is a chip select signal which can do page access. Please connect this signal according to the need.

Note5 HA2 pin should be connected to the signal which is as the 4 byte boundary address of the external MPU.

Note6 HA1 pin should be connected to the signal which is as the 2 byte boundary address of the external MPU.

11.1.2 Synchronous SRAM interface mode

The following figure shows a general connection example with the synchronous SRAM interface mode, when the external MPU connects as the host.

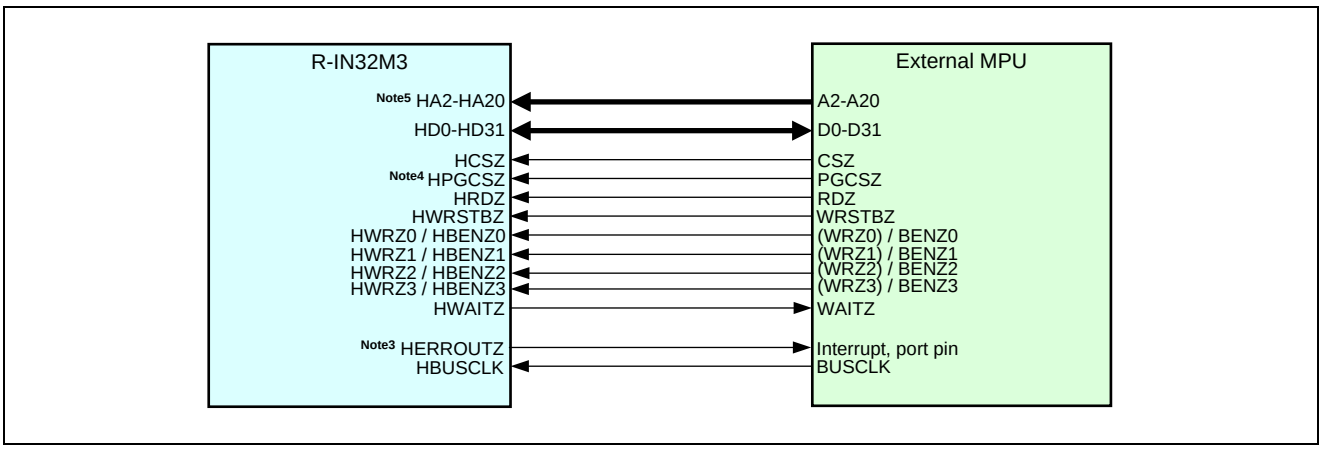


Figure 11.3 The connection example with external MPU (32bit bus, synchronous SRAM interface mode)

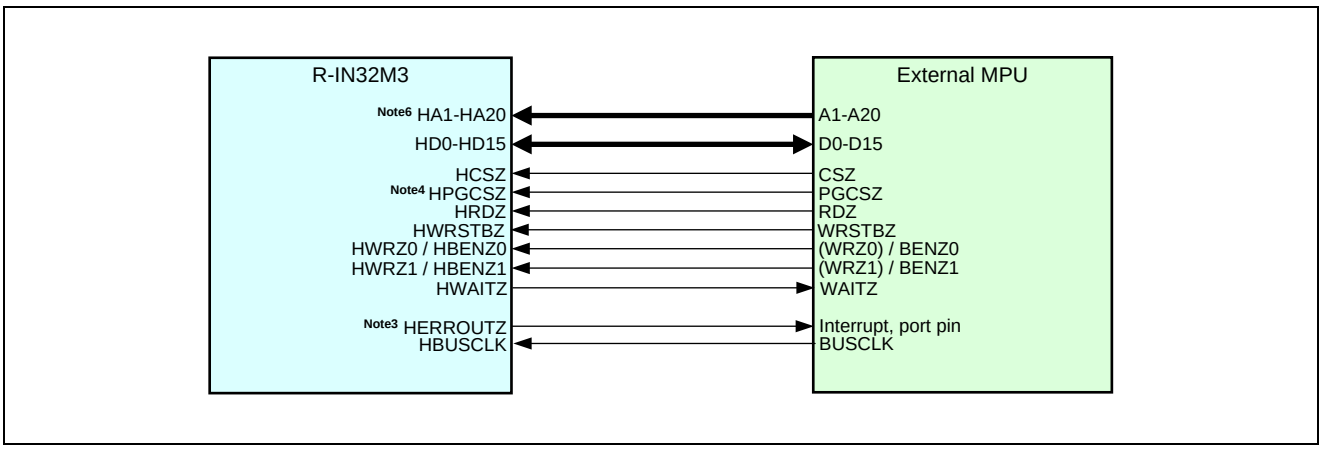


Figure 11.4 The connection example with external MPU (16bit bus, synchronous SRAM interface mode)

Note1 The detail of signal connection is depend on the bus interface spec of the host MPU. Please confirm the product spec of MPU which is connected to this LSI.

Note2 HWRZ0-HWRZ3 and HBENZ0-HBENZ3 is assigned to the same pin. The function is decided by the signal level of HWRZSEL pin.

Note3 The connection of the HERROUTZ signal is not indispensable. Please connect this signal to a interrupt or general port pin etc., according to the need.

Note4 PGCSZ signal is a chip select signal which can do page access. Please connect this signal according to the need.

Note5 HA2 pin should be connected to the signal which is as the 4 byte boundary address of the external MPU.

Note6 HA1 pin should be connected to the signal which is as the 2 byte boundary address of the external MPU.

11.1.3 Synchronous SRAM type transmission mode

The following figure shows a general connection example with the synchronous SRAM type transmission mode, when the external MPU connects as the host.

When user uses this mode, please enable “address/data multiplex” function (ADMUXMODE pin should be set to high level).

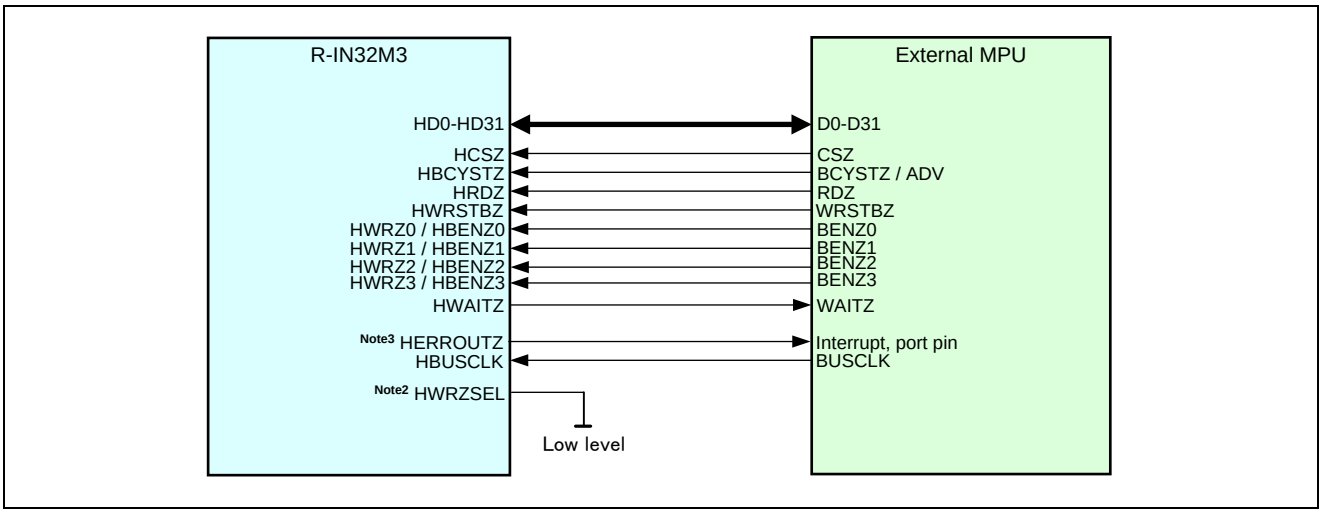


Figure 11.5 The connection example with external MPU (32bit bus, synchronous SRAM type transmission mode) <R>

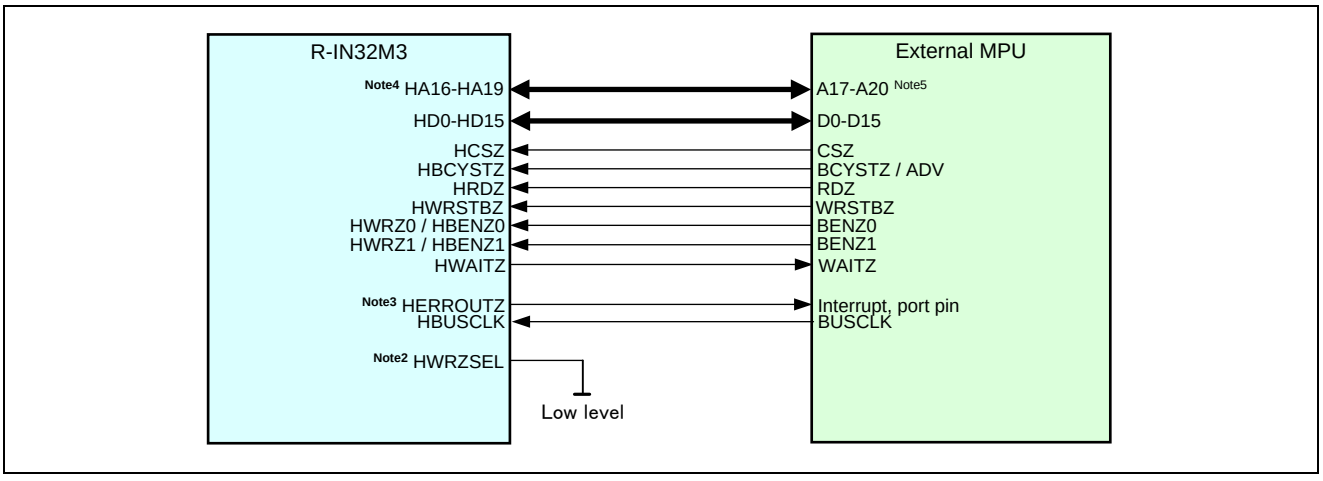


Figure 11.6 The connection example with external MPU (16bit bus, synchronous SRAM type transmission mode) <R>

Note1 The detail of signal connection is depend on the bus interface spec of the host MPU. Please confirm the product spec of MPU which is connected to this LSI.

Note2 In this mode, the HWRZSEL pin has to be set to low level. <R>

Note3 The connection of the HERROUTZ signal is not indispensable. Please connect this signal to a interrupt or general port pin etc., according to the need.

Note4 HA16 pin should be connected to the signal which is as the 128 Kbyte boundary address of the external MPU. <R>

Note5 This access is with byte addressing. <R>

11.2 External memory interface

This section describes about the connection to an external memory.

The connection mode of the external memory interface depends on the signal levels of the MEMCSEL pin and MEMIFSEL pin. (Please refer the Table 11.1.)

11.2.1 Asynchronous SRAM MEMC

Asynchronous SRAM MEMC can connect Paige ROM/ROM/SRAM outside by a 16-bit or 32-bit bus. Peripheral devices compliant with the SRAM interface can also be connected.

Asynchronous SRAM MEMC is carrying out the pin combination of the synchronous method burst access MEMC and the external microcomputer interface, and when both a MEMCSEL pin and a MEMIFSEL pin are low levels, it can use them as asynchronous SRAM MEMC.

11.2.1.1 SRAM connection example

An example of connection with SRAM is shown as follows.

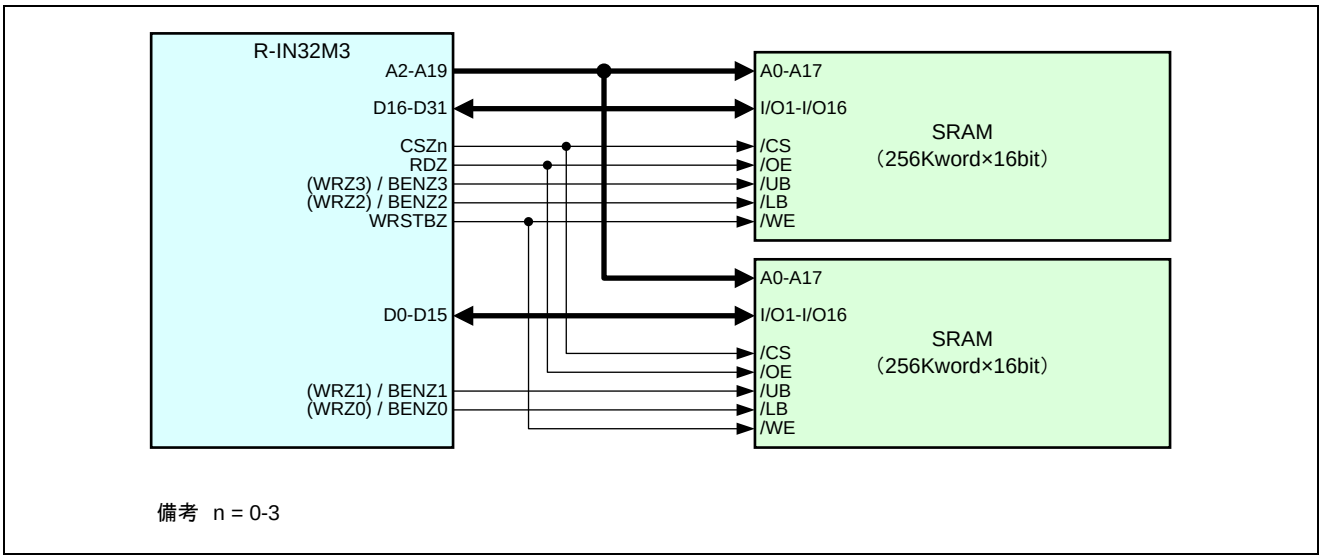


Figure 11.7 Example of Connection with SRAM (32bit bus, asynchronous SRAM MEMC)

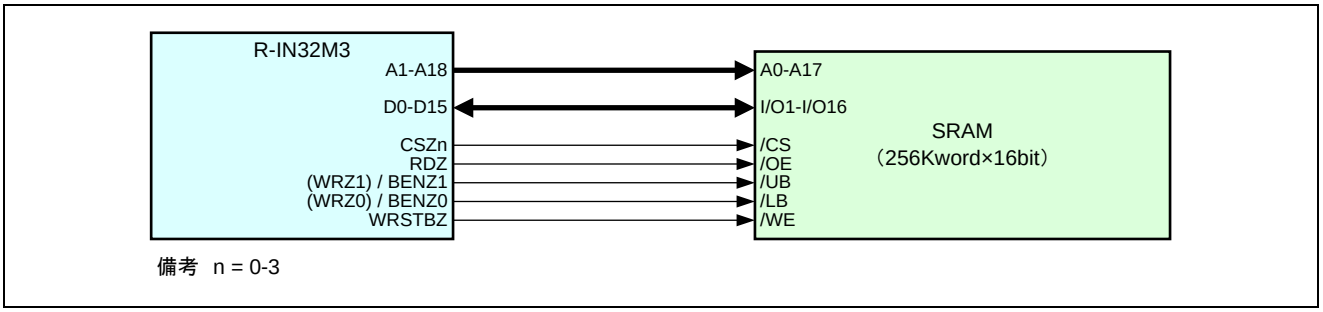


Figure 11.8 Example of Connection with SRAM (16bit bus, asynchronous SRAM MEMC)

11.2.1.2 Page ROM Connection Example

An example of connection with page ROM is shown as follows.

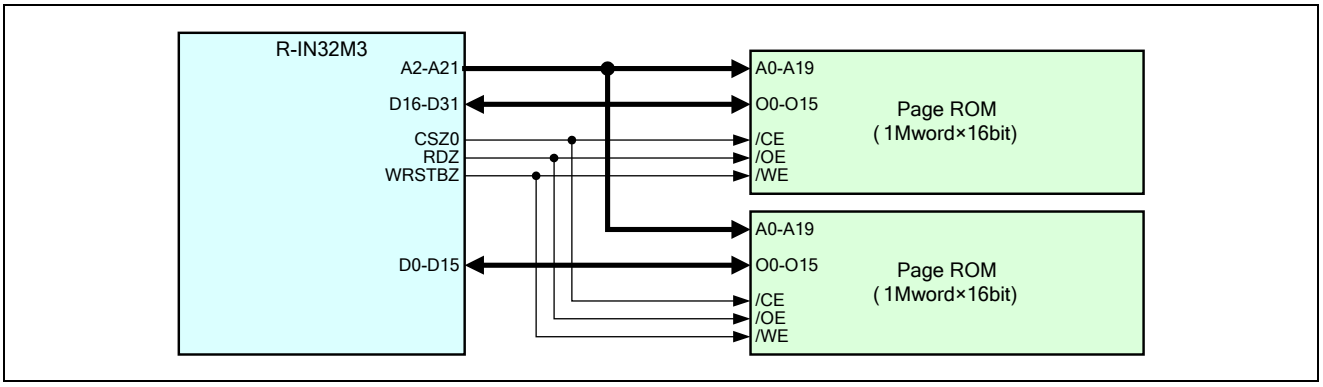


Figure 11.9 Example of Connection with Page ROM (32bit bus, asynchronous SRAM MEMC)

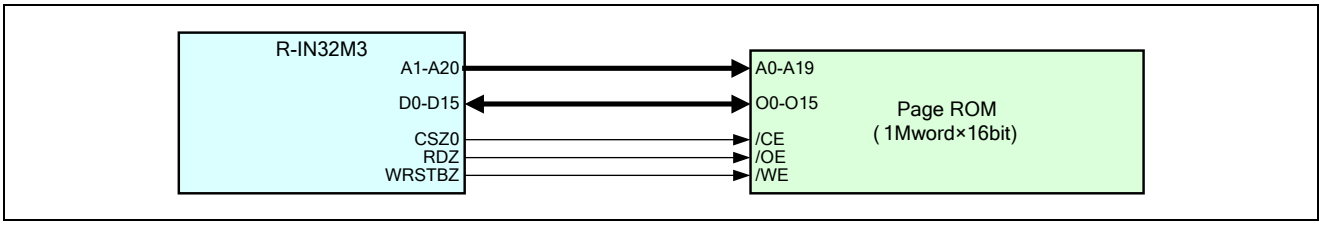


Figure 11.10 Example of Connection with Page ROM (16bit bus, asynchronous SRAM MEMC)

Caution The on-page mode of page ROM is available only when the ROM is connected to CSZ0.

11.2.2 Synchronous burst access MEMC

The synchronous burst access MEMC can be used to connect external page ROM, ROM, SRAM, PSRAM, NOR-Flash, and peripheral devices with an interface similar to the SRAM interface via the 32/16-bit bus.

By setting the ADMUXMODE pin to high level, the address signals can be multiplexed to be output from data pins.

The synchronous burst access MEMC and asynchronous SRAM MEMC share external microcontroller interface pins. Using these pins for the synchronous burst access MEMC is selected when the MEMCSEL pin outputs a high level and the MEMIFSEL pin outputs a low level.

11.2.2.1 SRAM connection example

An example of connection with SRAM is shown as follows.

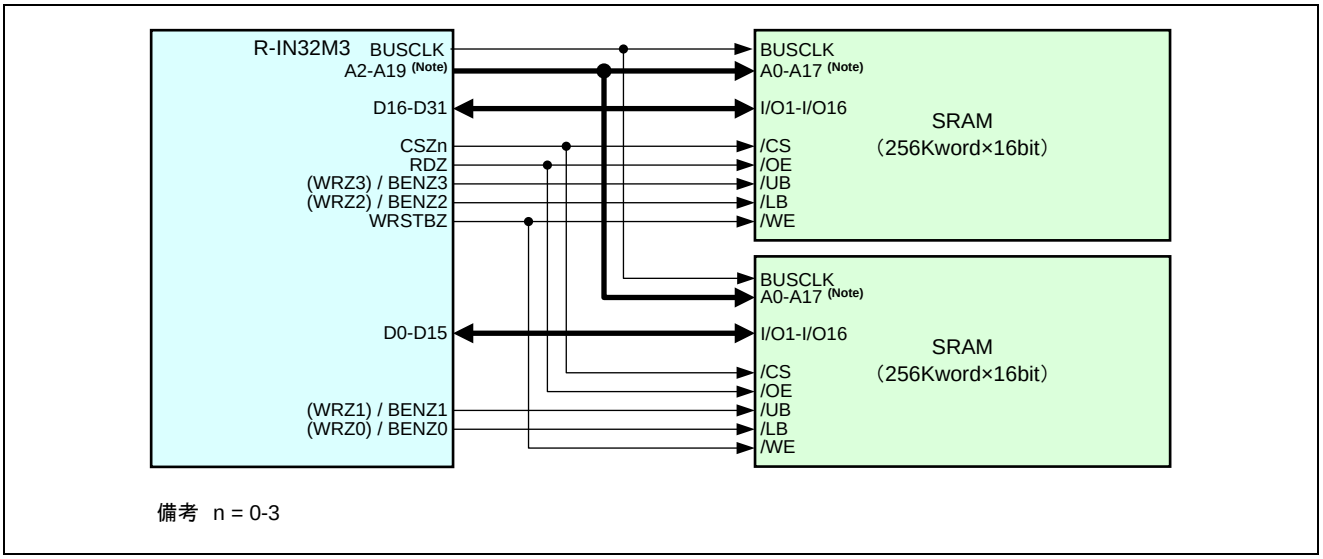


Figure 11.11 Example of Connection with SRAM (32bit bus, synchronous burst access MEMC)

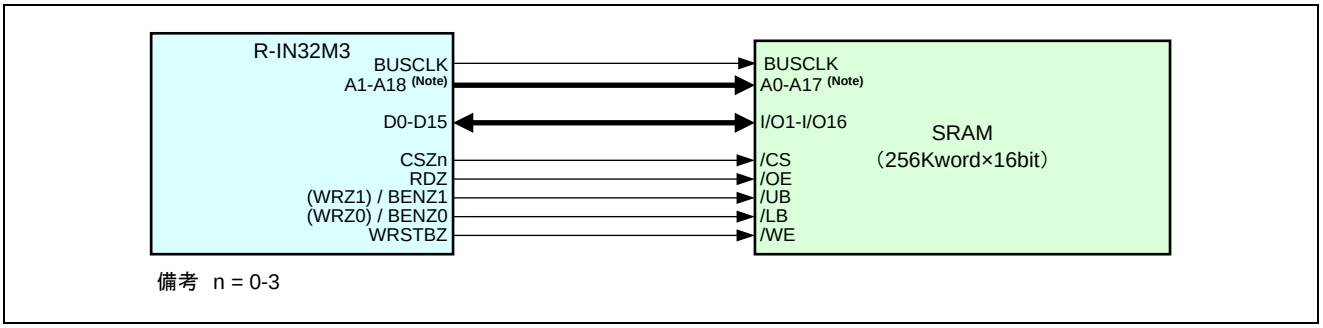


Figure 11.12 Example of Connection with SRAM (16bit bus, synchronous burst access MEMC)

Note When the “address/data multiprexing” mode is enable (the ADMUZMODE pin is high level), the connection of the address buses don’t need.

11.2.2.2 Page ROM Connection Example

An example of connection with page ROM is shown as follows.

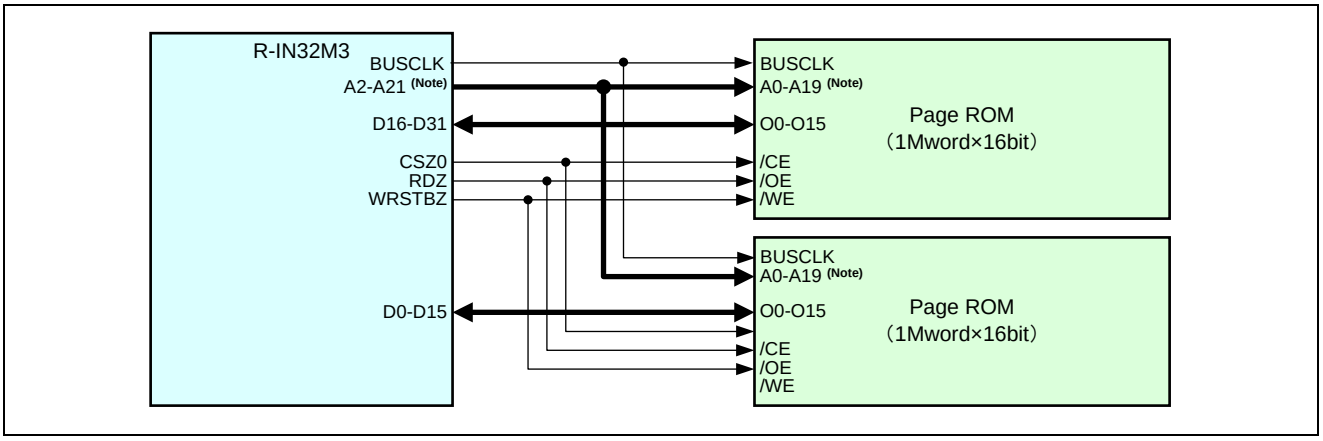


Figure 11.13 Example of Connection with Page ROM (32bit bus, synchronous burst access MEMC)

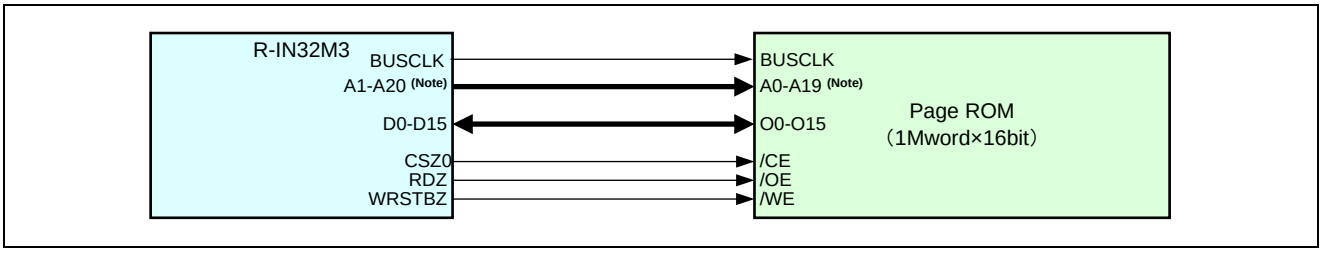


Figure 11.14 Example of Connection with Page ROM (16bit bus, synchronous burst access MEMC)

Caution The on-page mode of page ROM is available only when the ROM is connected to CSZ0.

Note When the "address/data multiprexing" mode is enable (the ADMUZMODE pin is high level), the connection of the address buses don't need.

12. Serial flash ROM connection pins

R-IN32M3 is connected with the serial flash ROM as shown below.

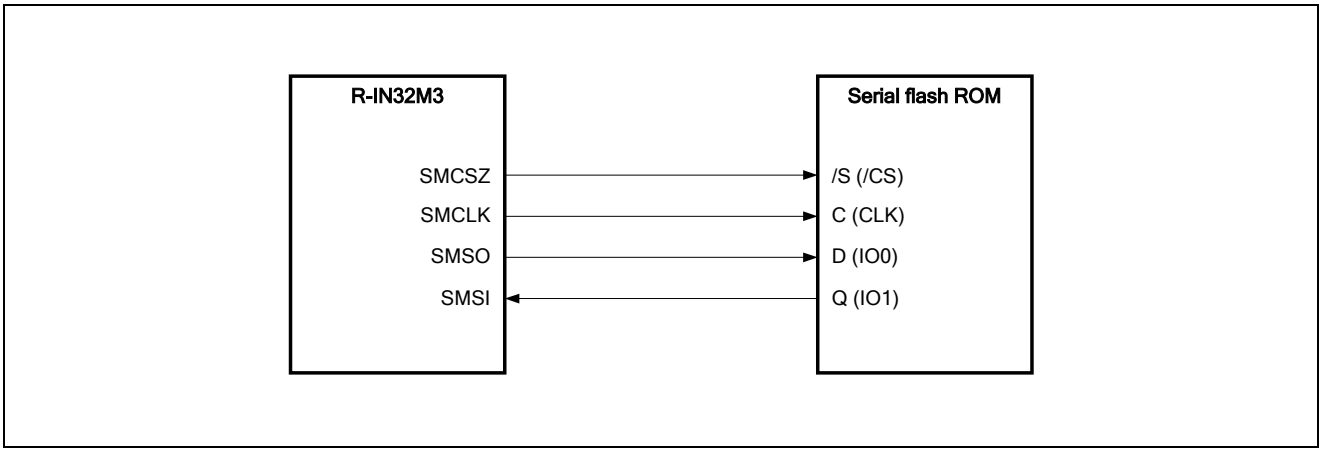


Figure 12.1 Connection with Serial Flash ROM

13. Asynchronous Serial Interface J(UARTJn) connection pins

Figure 13.1 shows a connection example between R-IN32M3 and Asynchronous Serial Interface J(UARTJn) device.

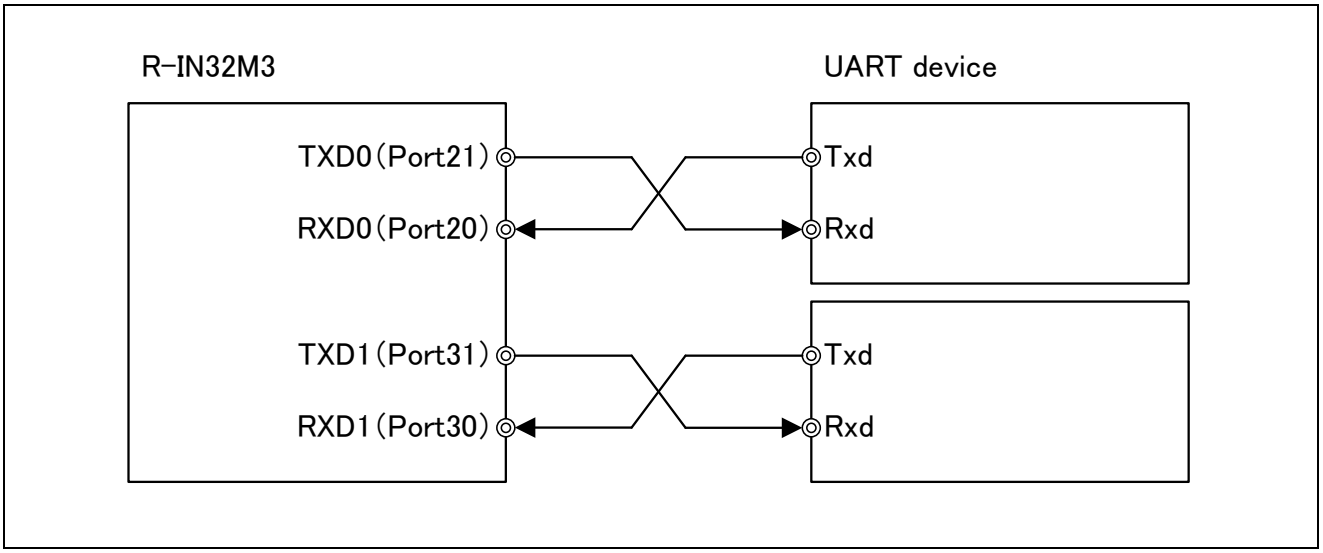


Figure 13.1 Connection example with the UART device

14. I^2C connection pins

Figure 14.1 shows a connection example between R-IN32M3 and I^2C Slave device. The serial clock line and the serial data line are a kind of N-ch open drain output, so user needs to connect a pull-up register.

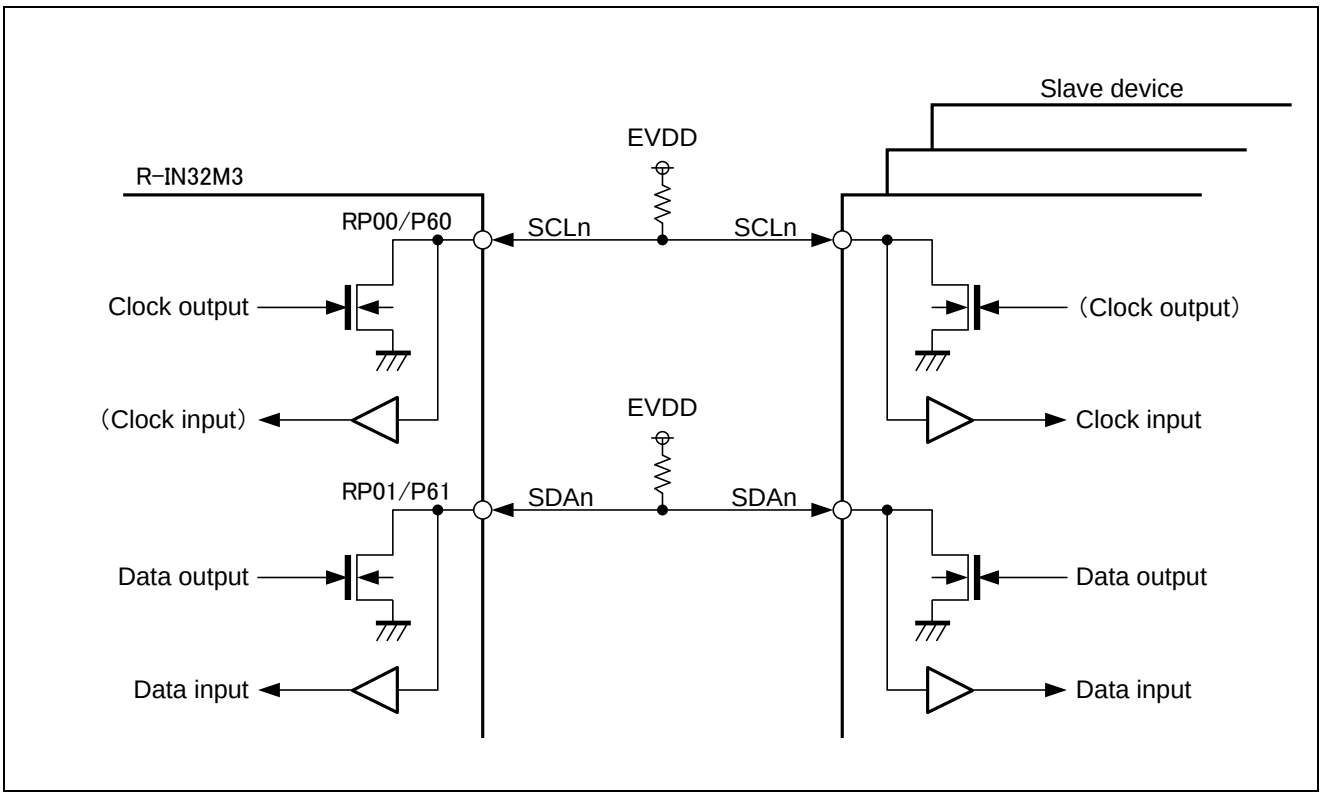


Figure 14.1 Connection example with the I^2C Slave device

15. EtherCAT EEPROM I^2C connection pins (only R-IN32M3-EC)

In the case of using the EtherCAT protocol, user needs to connect to the external EEPROM with the dedicated EEPROM I^2C connection pins.

The pins for EEPROM I^2C connection are the following pins.

- CATI2CCLK pin (shared with the P22 function) : EtherCAT EEPROM I^2C clock output
- CATI2CDATA pin (shared with the P23 function) : EtherCAT EEPROM I^2C data

Figure 15.1 shows a connection example between R-IN32M3-EC and EEPROM. The serial clock line and the serial data line are a kind of N-ch open drain output, so user needs to connect a pull-up register.

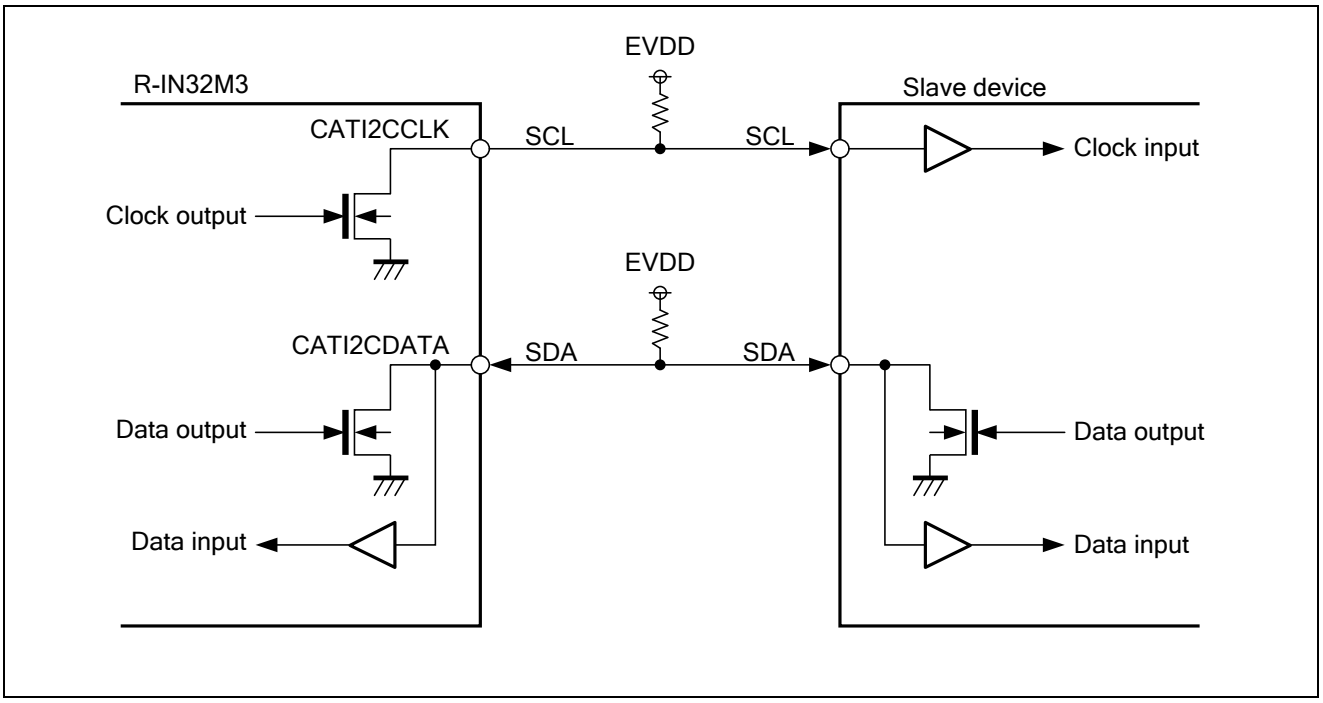


Figure 15.1 Connection example with the EtherCAT EEPROM

16. CAN pins

Figure 16.1 shows a connection example between R-IN32M3 and CAN Transceiver.

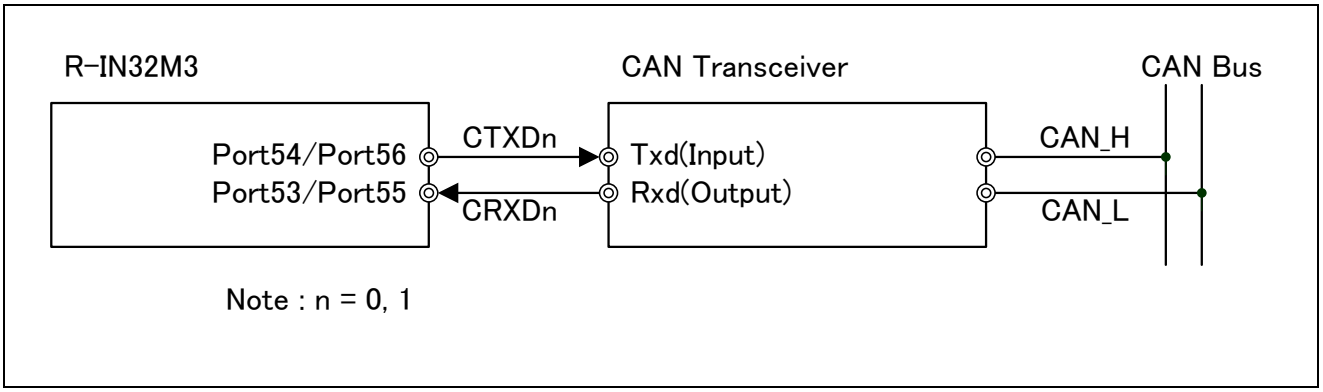


Figure 16.1 Connection example with the CAN Transceiver

17. JTAG/trace pins

A connection example with a connector of ICE (In Circuit Emulator) is indicated.

A connection example of the 20pin half pitch connector and the 20pin full pitch connector which are a standard connector is indicated.

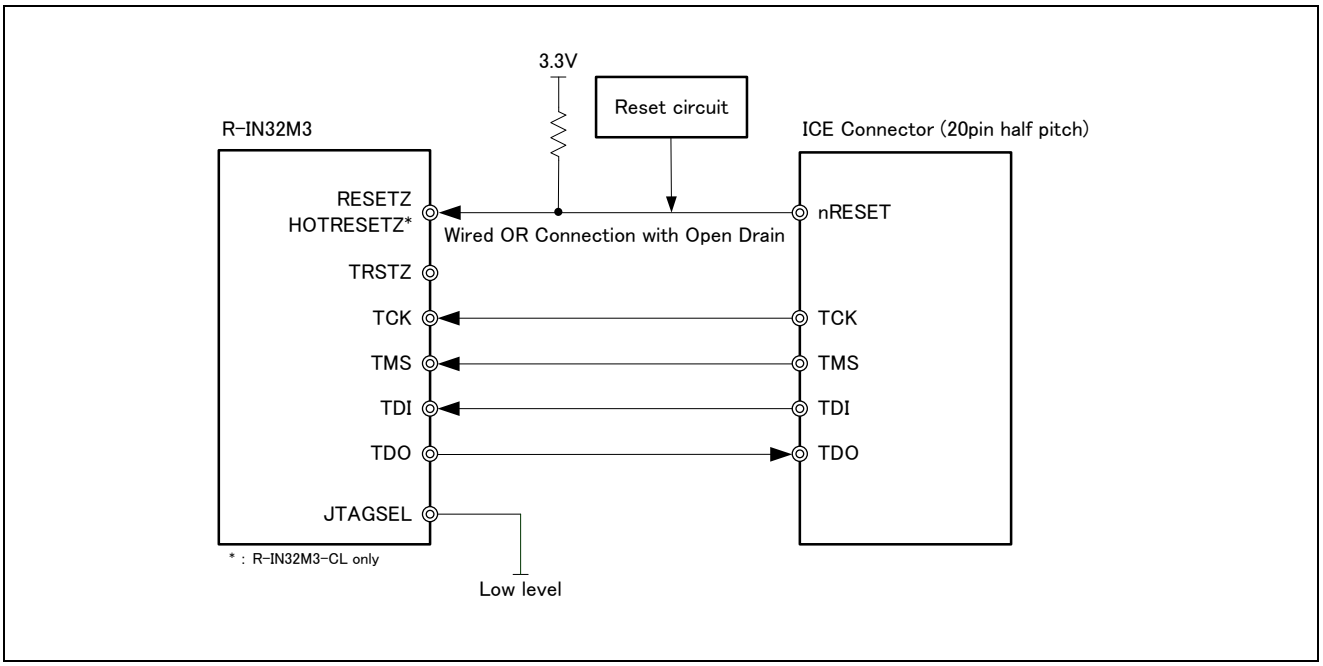


Figure 17.1JTAG interface connection example (20pin half pitch without trace)

As long as nRESET is input to RESETZ, nRESET is not required to input to HOTRESET.

RESRTZ resets the entire LSI, but the internal PLL is not reset in the case of only HOTRESETZ. Please use it to meet your needs. And nRESET should not connect to PONRZ.

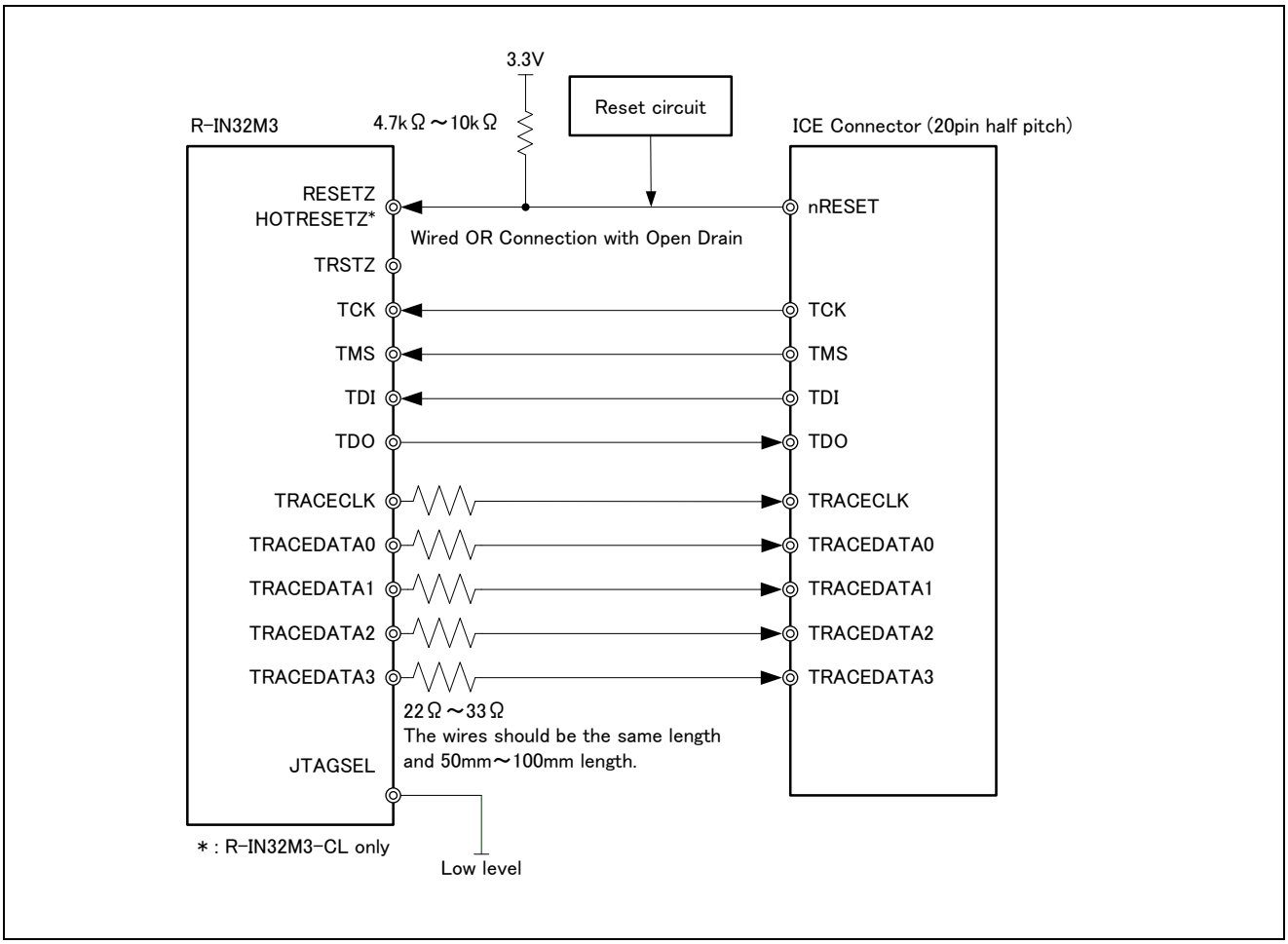


Figure 17.2JTAG interface connection example (20pin half pitch with trace)

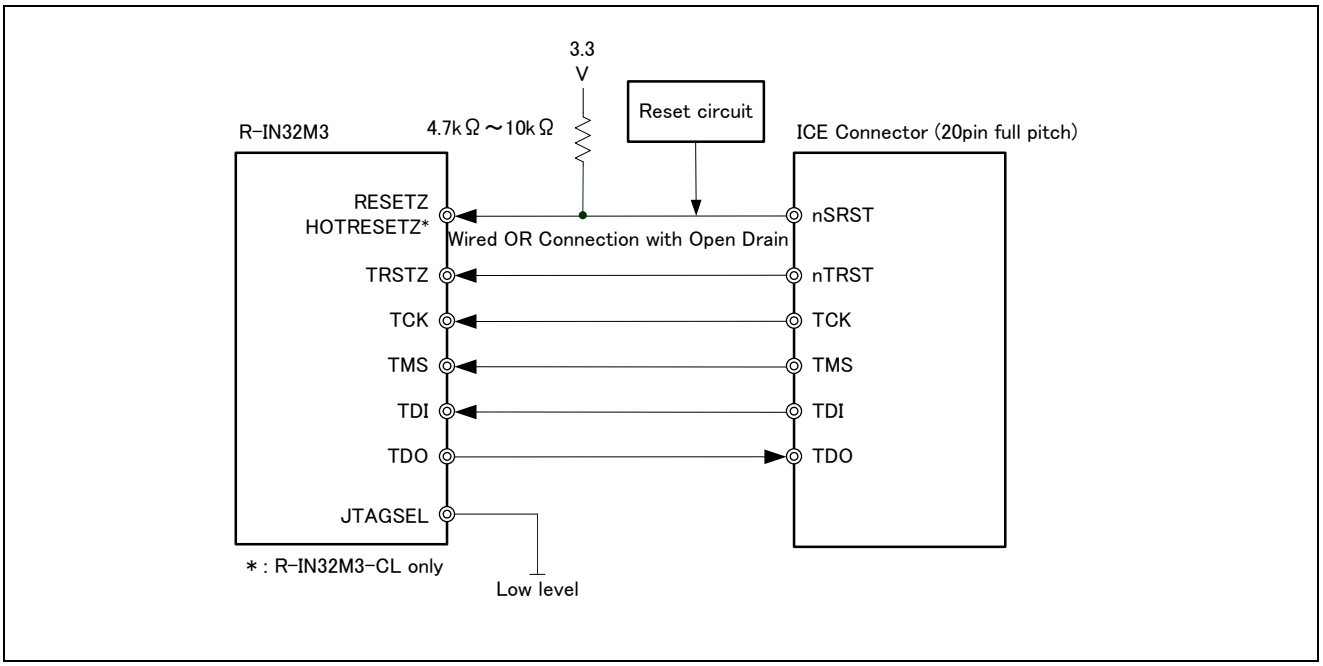


Figure 17.3JTAG interface connection example (20pin full pitch)

18. Implementation conditions

Figure 18.1 and Figure 18.2 show implementation conditions.

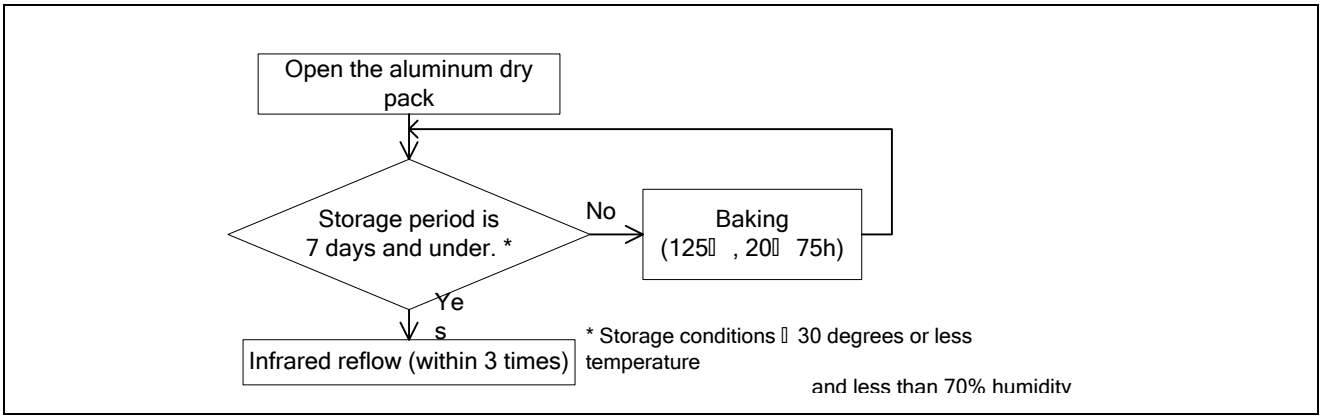


Figure 18.1 Implementation flow

- Maximum temperature (package surface temperature) : 260℃ and under
- Time of Maximum temperature : 10s and under
- Time which temperature is more than 220℃ : 60s and under
- Time of p reheat temperature (160-180℃) : 60～120s
- Number of maximum reflow times : 3times
- The chloric content of the rosinous flux. (the weight parcentage) : 0.2% and under
- Safekeeping restriction period after opening the dry pack : 7 days and under

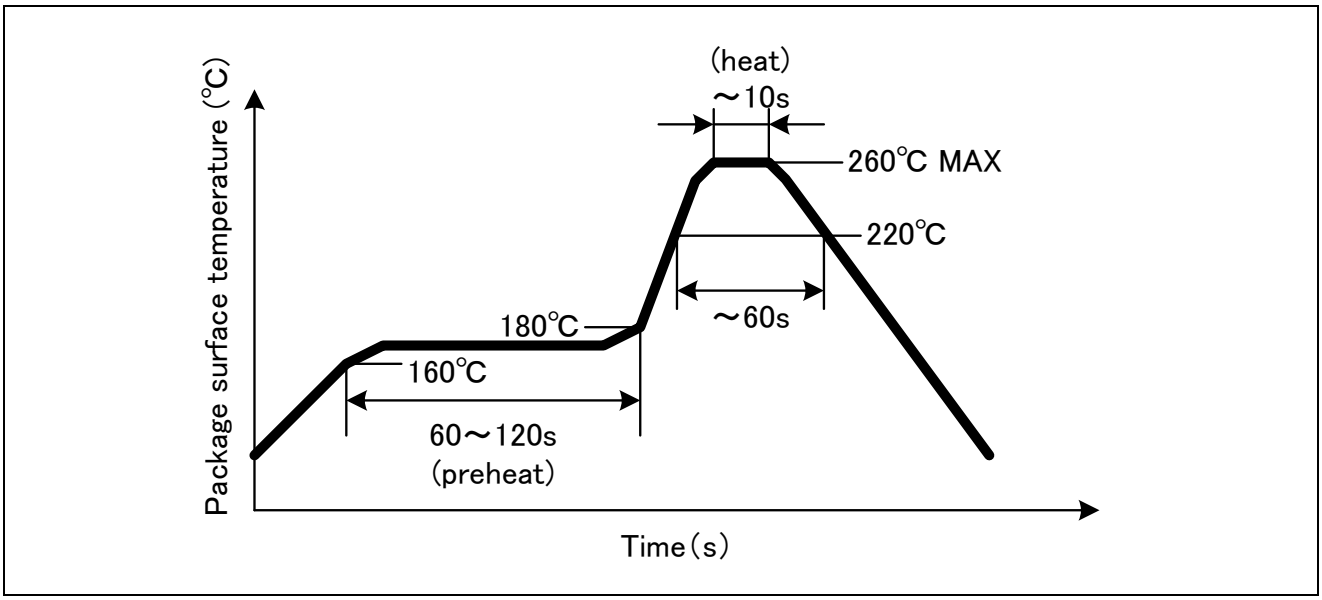
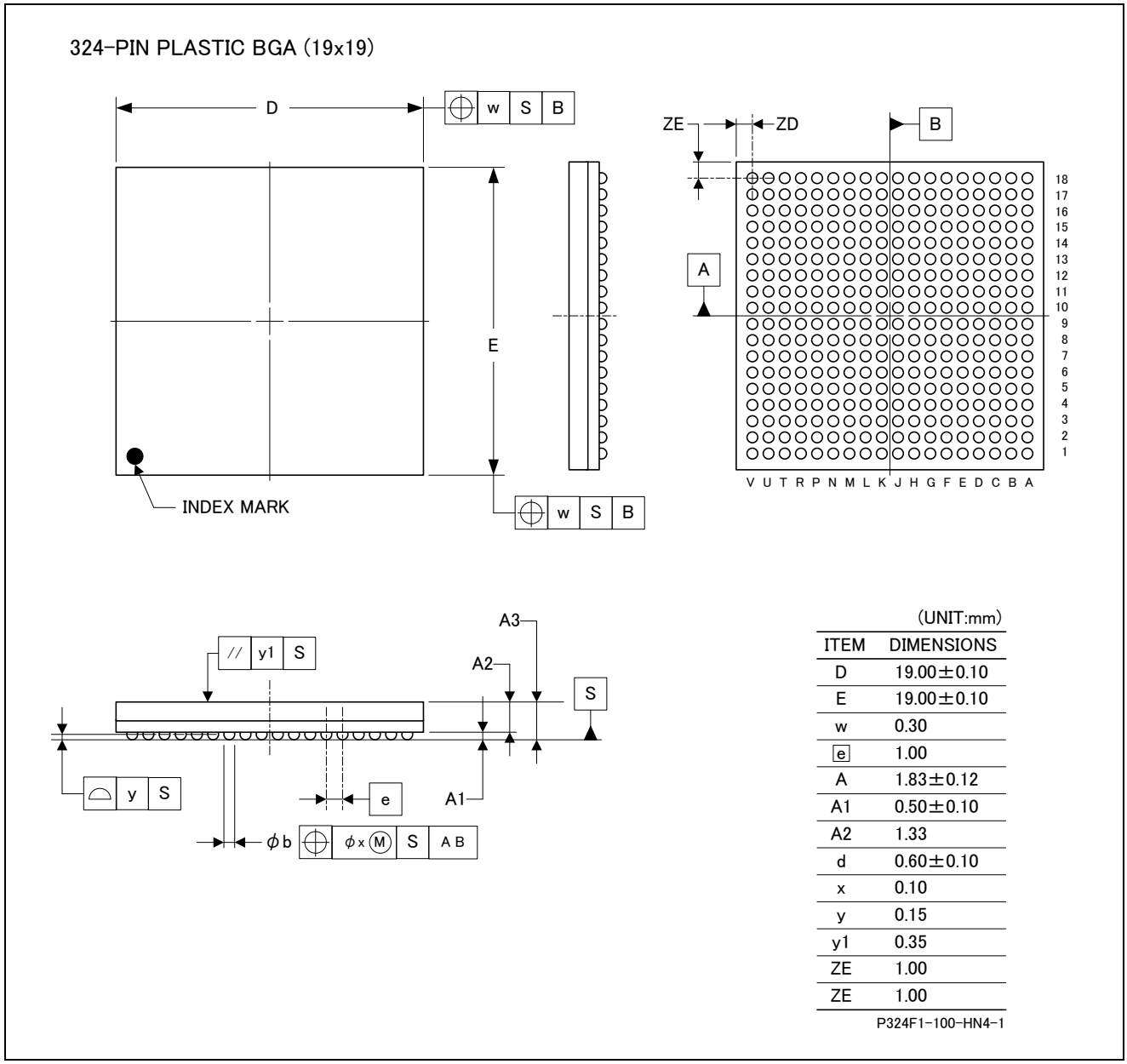


Figure 18.2 Infrared reflow temperature profile

19. Package informations

Figure 19.1 shows Package informations.



(UNIT:mm)

ITEM	DIMENSIONS
D	19.00±0.10
E	19.00±0.10
w	0.30
e	1.00
A	1.83±0.12
A1	0.50±0.10
A2	1.33
d	0.60±0.10
x	0.10
y	0.15
y1	0.35
ZE	1.00
ZE	1.00

P324F1-100-HN4-1

Figure 19.1 Package informations

20. Mount pad informations

Figure 20.1 shows mout pad informations.

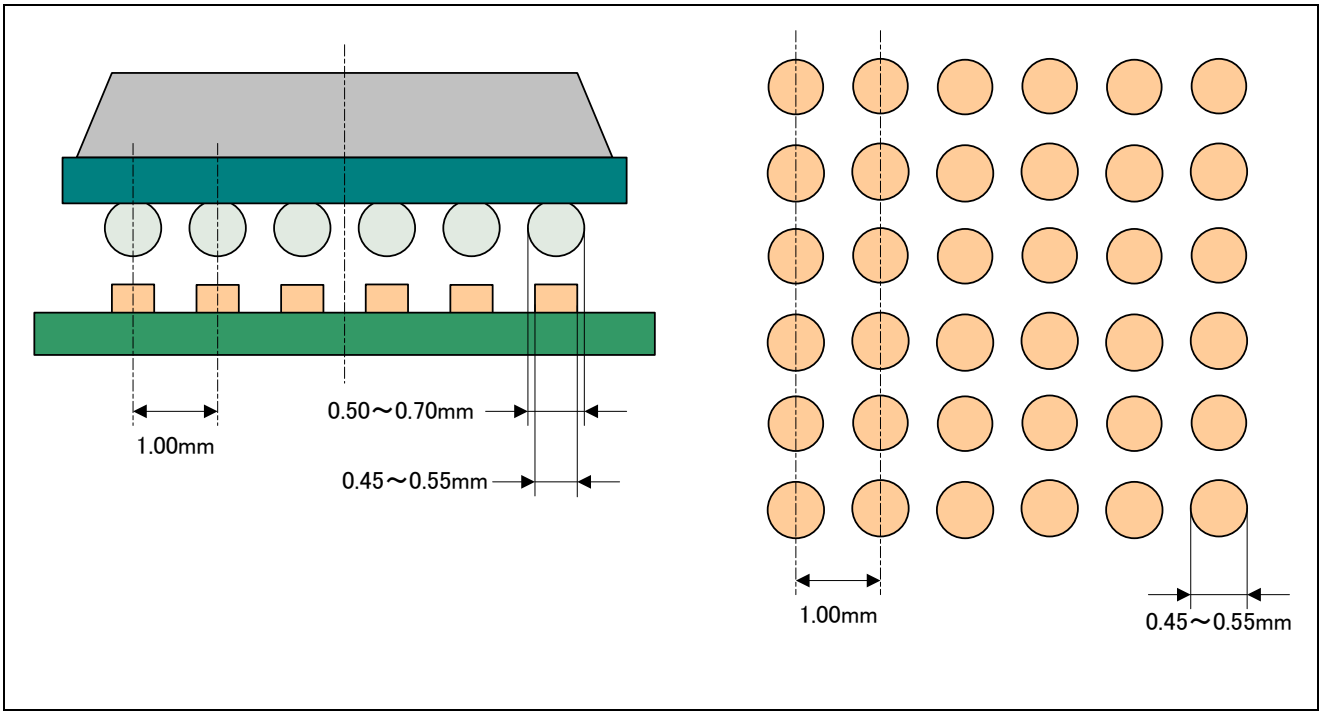


Figure 20.1 Mount pad sizes

21. BSCAN information

R-IN32M3 are available with BSDL file.

Caution If an opposite device connects to a input pin which doesn't have pull-up/pull-down, clamp the device on the board or fix logic as opposite device.
There is a possibility that a floating current flows when 3st pin or others is Hi-z state.

21.1 BSCAN operating prevision

Fix the level of the pins as follows.

- JTAGSEL : high level
- TMODE0 : low level
- TMODE1 : low level
- TMODE2 : low level

21.2 Maximum operating frequency of TCK

The maximum operating frequency of TCK is 10MHz.

21.3 IDCODE

IDCORE is as follows.

(1) R-IN32M3-CL

IDCODE 0x081A3447	
<breakdown>	
version	0000
part number	1000000110100011
Manufacturer number : Renesas Electronics	01000100011
Fixed code	1

(2) R-IN32M3-EC

IDCODE 0x081A4447	
<breakdown>	
version	0000
part number	1000000110100100
Manufacturer number : Renesas Electronics	01000100011
Fixed code	1

21.4 BSCAN non-correspondence pin

The following pin is not supported in BSCAN.

Table 21.1 List of pins which is not supported in BSCAN

R-IN32M3-CL	R-IN32M3-EC
XT1	XT1
XT2	XT2
PONRZ	PONRZ
JTAGSEL	JTAGSEL
TMODE0	TMODE0
TMODE1	TMODE1
TMODE2	TMODE2
TMS	TMS
TDI	TDI
TDO	TDO
TRSTZ	TRSTZ
TCK	TCK
TMC1	TMC1
TMC2	TMC2
	P0_RX_P
	P0_RX_N
	P1_RX_P
	P1_RX_N
	P0_TX_P
	P0_TX_N
	P1_TX_P
	P1_TX_N
	TEST1
	TEST2
	TEST3
	ATP
	LX
	EXTRES

21.5 How to get BSDL

With regard to obtain BSDL file, please contact your sales representative.

22. IBIS Information

Please obtaion from the following website IBIS information.

http://japan.renesas.com/products/soc/assp/fa_lsi/multi_protocol_communication/r-in32m3/peer/documents.jsp

23. Impress information

23.1 R-IN32M3-EC

Product name: MC-10287F1-HN4-M1-A

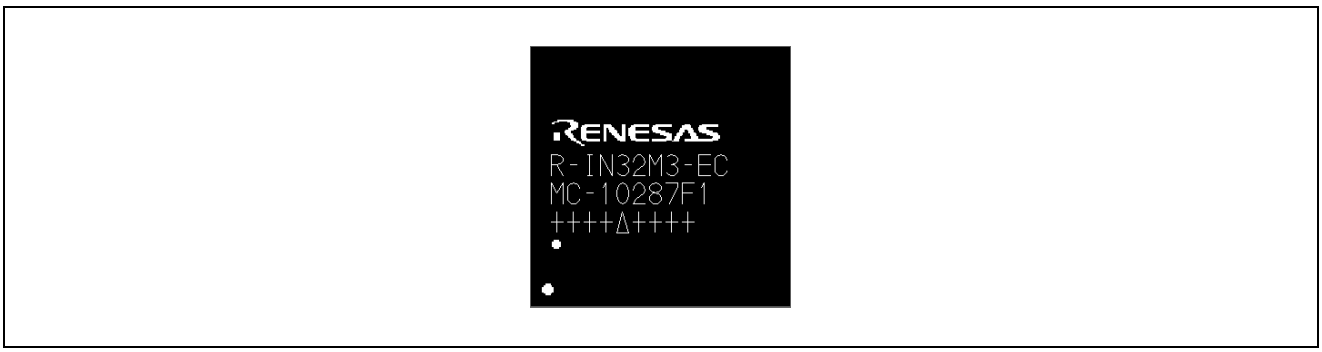


Figure 23.1 R-IN32M3-EC Impress information

23.2 R-IN32M3-CL

Product name: UPD60510F1-HN4-M1-A

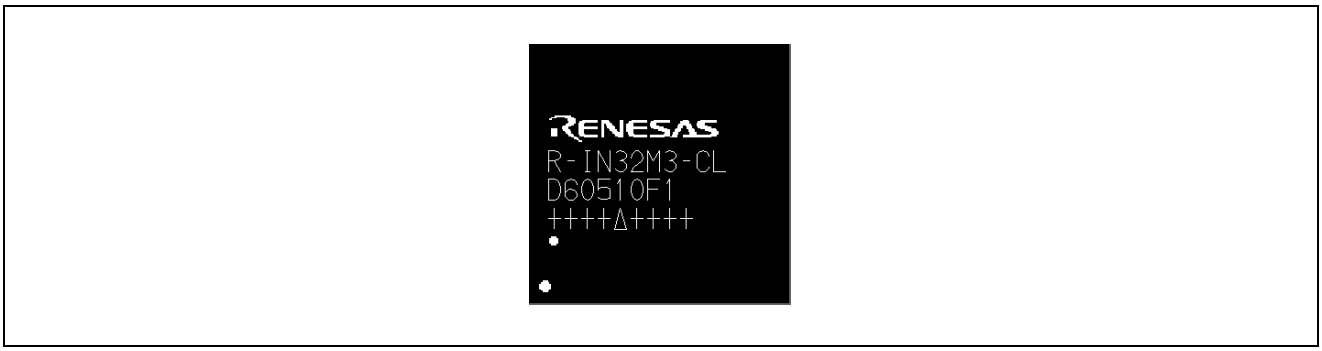


Figure 23.2 R-IN32M3-CL Impress information

REVISION HISTORY	R-IN32M3 Series User's Manual (Board design edition)

Rev.	Date	Description	
		Page	Summary
1.00	Jul 26, 2013	-	First edition issued
1.01	Dec 02, 2013	10,12	Add the TEST pin processing
		22	Add " 9. Notes of CC-Link IE FIeld user (only R-IN32M3-CL)"
2.00	Dec 26, 2013	11	Add a description of 6.GPIO port pins
		20	Add a description of 8.GMII pins
		23	Modify a description of 10. Notes of CC-Link IE Field use
		24	Add a description of "11. External MPU/memory interface pins"
		33	Add a description of "12. Serial Flash ROM memory connection pins"
		34	Add a description of "13. Asynchronous Serial Interface J(UARTJ) connection pins"
		35	Add a description of "14. I^2C connection pins"
		36	Add a description of "15. EtherCAT EEPROM I^2C connection pins"
		37	Add a description of "16. CAN pins"
		38	Add a description of "17.JTAG/trace pins"
2.01	Feb 07, 2014	24	Modify the mode description of the case of MEMCSEL=High and HIFSYNC=Low.
		25,26	Delete HBCYSTZ pin connection of "Fig 11.1" and "Fig 11.2" Modifiy the width of data bus of "Fig 11.2" Add the description of Note4-6 of "Fig 11.1" and "Fig 11.2"
		27,28	Delete HBCYSTZ pin connection of "Fig 11.3" and "Fig 11.4" Modifiy the width of data bus of "Fig 11.4" Modifiy the width of address bus of "Fig 11.4" Add the description of Note4-6 of "Fig 11.3", "Fig 11.4"
		29, 30	Separete and add the description about "synchronous SRAM type transmission mode"
2.02	May 30, 2014	2	Add a notes of "2.1 Power-on-off sequence"
		1-9	Modify Eglish expression about capter 1-4
2.03	Sep 30, 2014	11	Modify part name of inductor VLC5028T to VLCF5028T in "5.1Built-in regulator used" Modify ESR value of condenser 300 ohm to 300 mohm in "5.1Built-in regulator used"
		25-29	Fig.11.1-11.6 Modify signal name BUSCLK to HBUSCLK
		40	Add a description in "17.JTAG/trace pins"
2.04	Dec 25, 2014	22, 23	Add Fig. 9.1 in ***9.CC-Link pins***
		29, 30	Modify Fig.11.5, 11.6 to add HBCYSTZ connection, modify Adress bus number, and delete HHPGCSZ connection. And modify Note2, 4, 5 description in ***11.1.3 Synchronous SRAM type transmission mode***

[Memo]

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