NAR-3041/3061 Series
Communication Appliance

User's Manual

Revision: 010

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Chapter 1 Introduction

1.1 About This Manual

This manual contains all required information for setting up and using the NAR-3041/3061 series.

NAR-3041/3061 series provides the essential platform for delivering optimal performance and functionality in the value communications appliance market segment. This manual should familiarize you with NAR-3041/3061 series operations and functions. NAR-3041/3061 series has up to eight on-board Ethernet ports to serve communication appliances like Firewall, requiring three Ethernet ports to connect external network (internet), demilitarized zone and internal network.

Feature of NAR-3041/NAR-3061 series includes:

- Versatile networking and I/O capabilities: 4, 6 or 8 Ethernet ports (NAR-3041-410, NAR-3061-610 and NAR-3061-810)
- Two USB ports and two COM ports
- Up to 512 MB of 168-pin DIMM memory
- One on-board DMA/33/66/100 IDE channel to support up to four IDE devices
- Two PCI slots for ease of connectivity to the PCI bus
- One Mini PCI Interface

1.2 Manual Organization

This manual describes how to configure your NAR-3041/NAR-3061 series system to meet various operating requirements. It is divided into three chapters, with each chapter addressing the basic concept and operation of this system.

Chapter 1: Introduction. This section describes how this document is organized. It includes brief guidelines and overview to help find necessary information.

Chapter 2: Hardware Configuration Setting and Installation. This chapter demonstrated the hardware assembly procedure, including detailed information. It shows the definitions and locations of Jumpers and Connectors that can be used to configure the system. Descriptions on how to properly mount the CPU and main memory are also included to help perform a safe installation. This chapter will provide detailed instruction on how to set up NAR-3041/NAR-3061 series.

Chapter 3: Operation Information. This section provides illustrations and information on the system architecture and how to optimize its performance.

Any updates to this manual, technical clarification and answers to frequently asked questions would be posted on the web site: ***http://isc.portwell.com.tw***

1.3 Technical Support Information

Users may find helpful tips or related information on Portwell's web site: ***http://www.portwell.com.tw.*** A direct contact to Portwell's technical person is also available. For further support, users may also contact Portwell's headquarter in Taipei or local distributors.

Chapter 2 Getting Started

This section describes how the hardware installation and system settings should be done.

2.1 Included Hardware

The following hardware is included in package:

- PPAP-250 Communication Appliance System Board
- One null serial port cable

2.2 Before You Begin

To prevent damage to any system board, it is important to handle it with care. The following measures are generally sufficient to protect your equipment from static electricity discharge:

When handling the board, use a grounded wrist strap designed for static discharge elimination and touch a grounded metal object before removing the board from the antistatic bag. Handle the board by its edges only; do not touch its components, peripheral chips, memory modules or gold contacts.

When handling processor chips or memory modules, avoid touching their pins or gold edge fingers. Restore the communications appliance system board and peripherals back into the antistatic bag when they are not in use or not installed in the chassis.

Some circuitry on the system board can continue operating even though the power is switched off. Under no circumstances should the Lithium battery cell used to power the real-time clock be allowed to be shorted. The battery cell may heat up under these conditions and present a burn hazard.

WARNING!

1. **"CAUTION: DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED. REPLACE ONLY WITH SAME OR EQUIVALENT TYPE RECOMMENDED BY THE MANUFACTURER. DISCARD USED BATTERIES ACCORDING TO THE MANUFACTURER'S INSTRUCTIONS"**
2. **This guide is for technically qualified personnel who have experience installing and configuring system boards. Disconnect the system board power supply from its power source before you connect/disconnect cables or install/remove any system board components. Failure to do this can result in personnel injury or equipment damage.**
3. **Avoid short-circuiting the lithium battery; this can cause it to superheat and cause burns if touched.**
4. **Do not operate the processor without a thermal solution. Damage to the processor can occur in seconds.**
5. **Do not block air vents. Minimum 1/2-inch clearance required.**

2.3 The Chassis

The system is integrated in a customized 1U chassis (***Fig. 2-1, Fig. 2-2***). On the front panel you will find a 4-push-button LCD module (EZIO), four LAN ports and a COM port. The back panel has two USB ports.

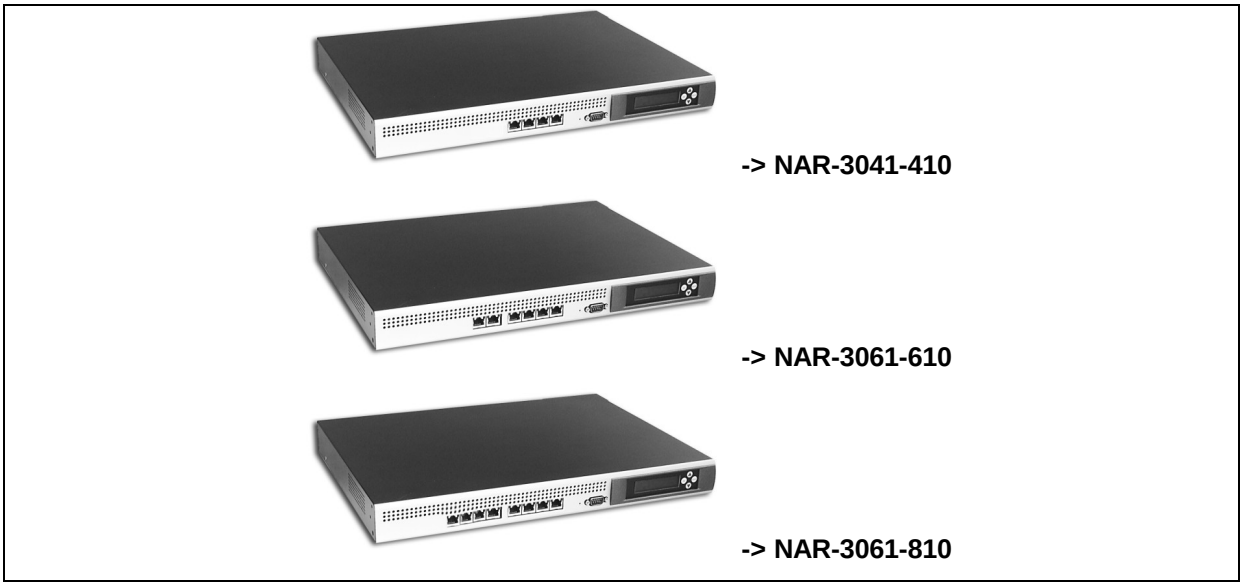


Fig. 2-1 *Front view of the chassis*

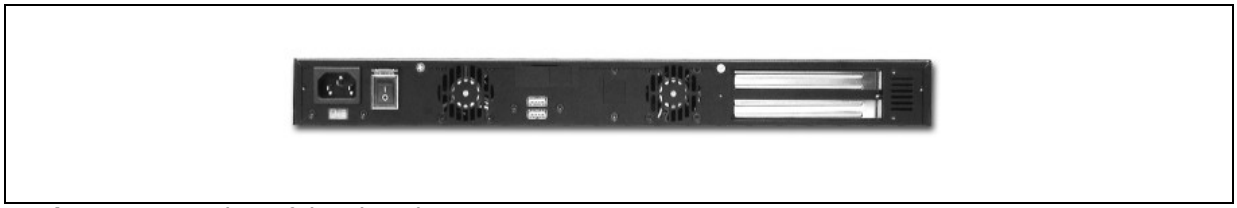


Fig. 2-2 *Rear view of the chassis*

2.4 Open the Chassis

1. Loosen the ten screws of the chassis, four on each side and the rest two on the back, to remove the top lead (***Fig. 2-3***).

Fig. 2-3 *Take off ten screws*

2. The top lead (***Fig. 2-4***) can be removed from the base stand (***Fig. 2-5***).

Fig. 2-4 *The top lead*

Fig. 2-5 *The base stand*

2.5 Remove and Install DIMM

Follow these steps to upgrade RAM module:

1. Install the system memory by pulling the socket's arm and pressing it into the slot gently. (***Fig. 2-6, 2-7***)

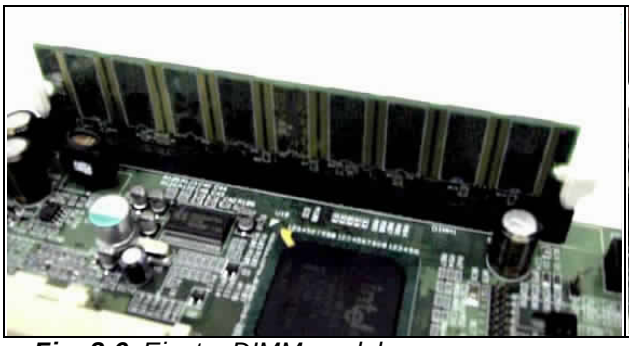


Fig. 2-6 *Eject a DIMM module*

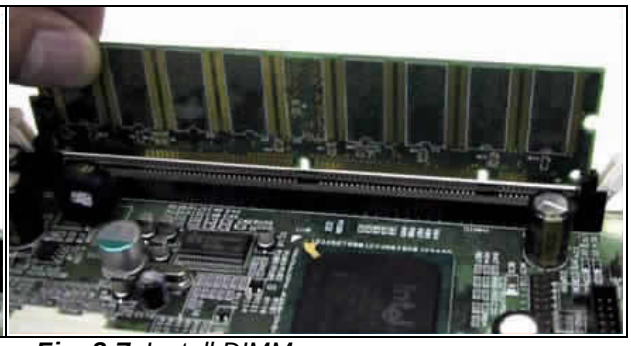


Fig. 2-7 *Install DIMM*

2.6 Remove and Install DOM

1. Insert the DOM (***Fig. 2-8***) into the IDE interface (***Fig. 2-9***).

Fig. 2-8 *DiskOnModule*

Fig. 2-9 *Insert DOM into IDE interface*

2. Connect the power source to DOM (***Fig. 2-10, 2-11***).

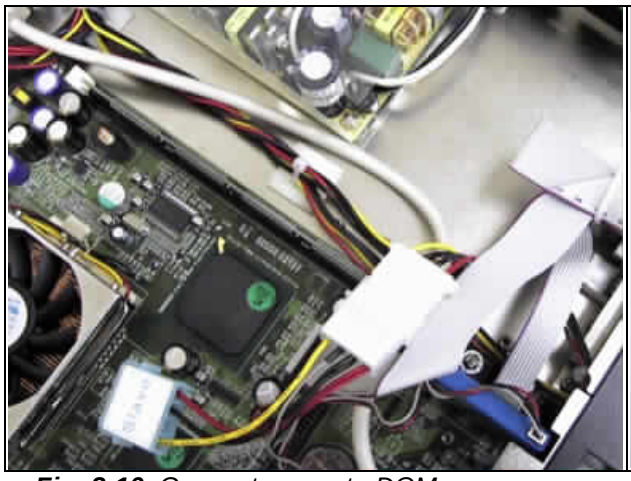


Fig. 2-10 *Connect power to DOM*

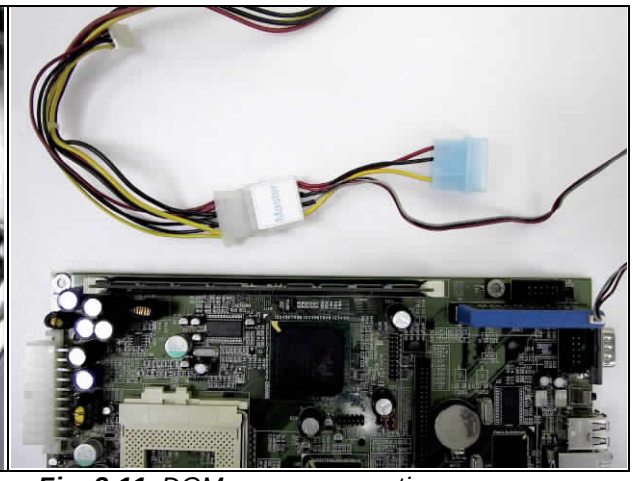


Fig. 2-11 *DOM power connection*

3. The completed installation of DOM is shown as ***Fig. 2-12***.

Fig. 2-12 *Completion of DOM power connection*

2.7 Remove and Install Battery

1. Press the metal clip back to eject the button battery (***Fig. 2-13***).
2. Replace it with a new one by pressing the battery with fingertip to restore the battery (***Fig. 2-14***).

Fig. 2-13 *Eject the battery*

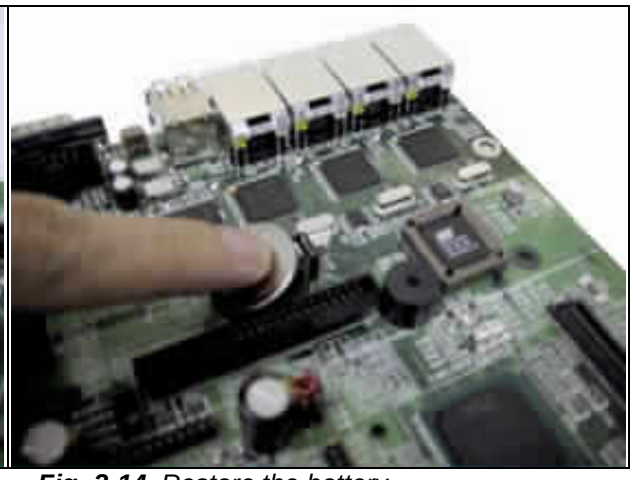


Fig. 2-14 *Restore the battery*

2.8 Install HDD

The system has an internal drive bay for one 2.5" hard disk drive. If the HDD is not pre-installed, you can install it by yourself. Follow the steps below to install the HDD:

1. Fasten the four screws to lock HDD and bracket together (***Fig. 2-15a, 2-15b***).

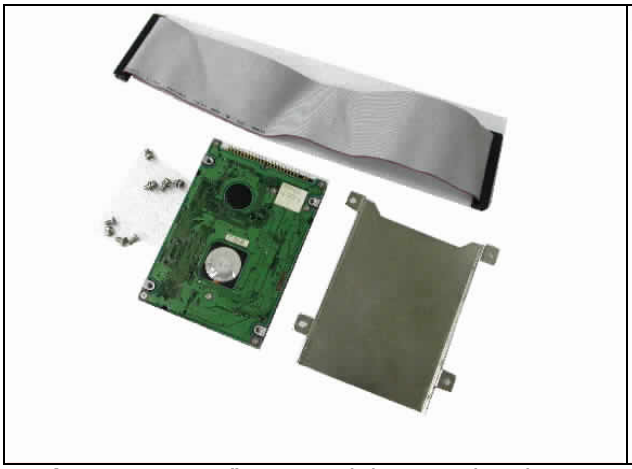


Fig. 2-15a *A 2.5" HDD and the HDD bracket*

Fig. 2-15b *Fix HDD to the bracket*

2. Connect the IDE cable to HDD (***Fig. 2-16***).
3. Connect IDE cable to PPAP-250 (***Fig. 2-17***).

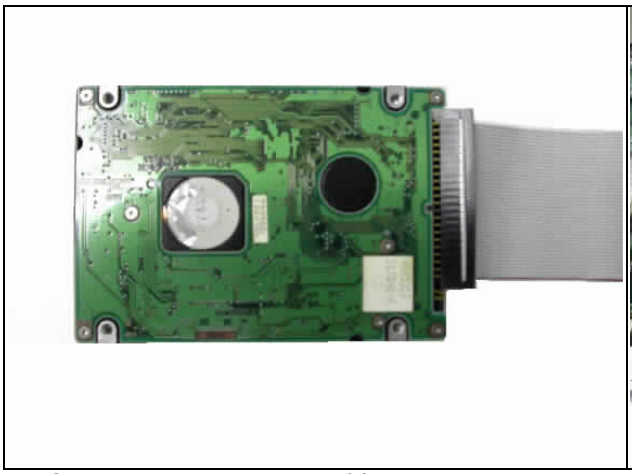


Fig. 2-16 *Connect IDE cable to HDD*

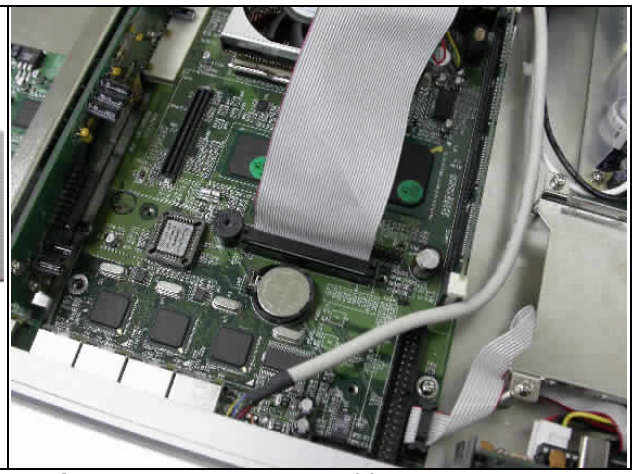


Fig. 2-17 *Connect IDE cable to PPAP-250*

4. Fix all four screws back (***Fig. 2-18***).

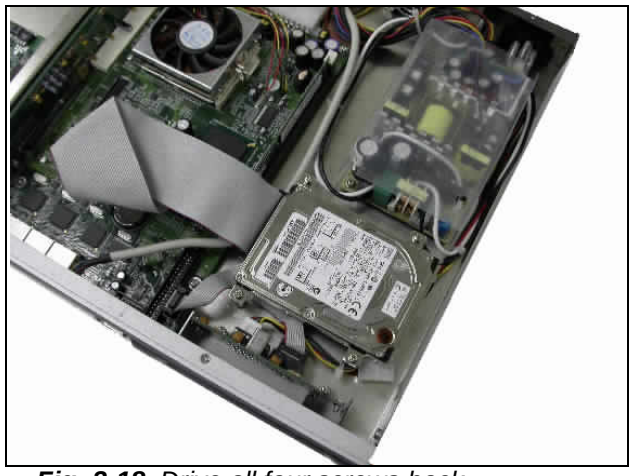


Fig. 2-18 *Drive all four screws back*

2.9 Remove and Install PCI card

One PCI slot is available to NAR-3041/3061 series. Follow the steps below for installation:

1. First, loosen the ten screws of the chassis, four on each side and the rest two on the back, to remove the top lead (***Fig. 2-19***). Then, remove the screw from the side (***Fig. 2-20***).

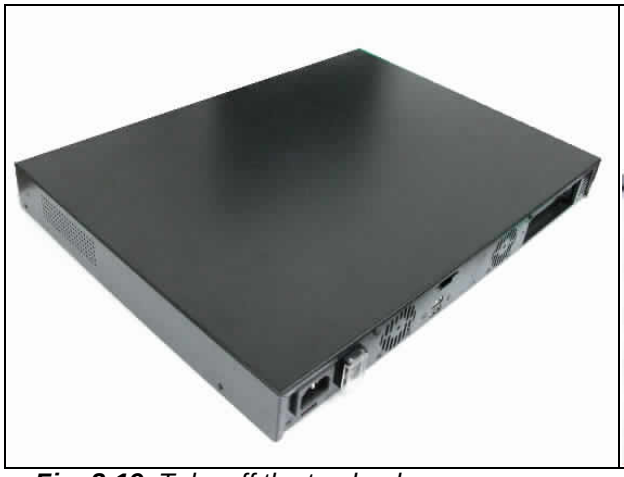


Fig. 2-19 *Take off the top lead*

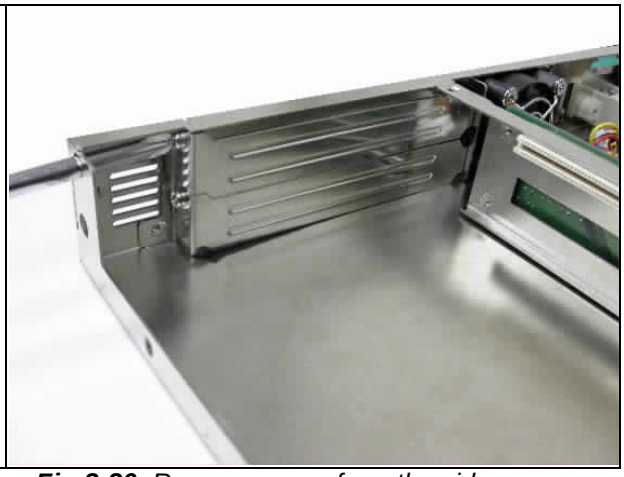


Fig.2-20 *Remove screw from the side.*

2. Push the PCI add-on card into the PCI slot (***Fig. 2-21***).
3. Fasten the screw back to the side (***Fig. 2-22***).

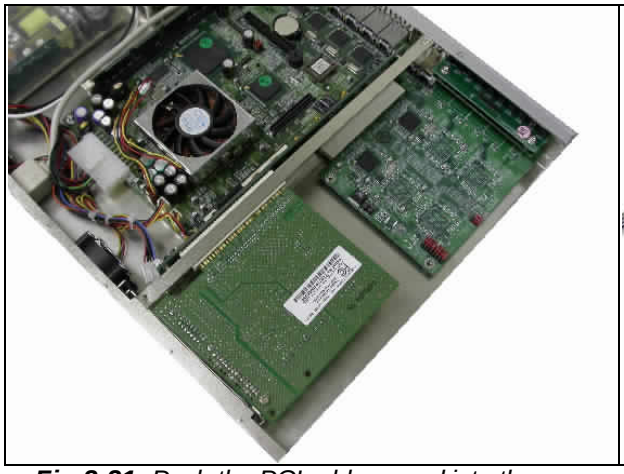


Fig.2-21 *Push the PCI add-on card into the PCI slot*

Fig.2-22 *Fasten the screw back to the side*

4. Drive the screws back to fasten the top lead (***Fig. 2-23***).

Fig. 2-23 *Drive the screws back to lock the top lead*

2.10 Product Specifications

Model:	**NAR-3041/NAR-3061 series**
Main Processor:	• Intel® socket 370 FC-PGA Celeron®/Pentium® III processors (66, 100 or 133MHz system bus)
BIOS:	• Award system BIOS with 512KB flash ROM to support DMI, PnP, APM function
Main Memory:	• One 168-pin DIMM socket supports up to 512MB of 3.3V DIMM
L2 Cache Memory:	• 128KB/256KB PBSRAM built in (Celeron/Pentium III) CPU module
Chipset:	• Intel® 815E
PCI IDE Interface:	• One 2.5” hard disk bay for DMA/33/66/100 IDE hard disk
Serial Ports:	• Support two high-speed 16550C compatible UARTs with 16-byte T/R FIFOs • (Optional) Support LCD/Key pad module (Portwell proprietary)
USB Interface:	• Support two USB ports for high speed I/O peripheral devices
Auxiliary I/O Interfaces:	• System reset switch, power okay LED, general purpose LED and HDD LED interface
Power Input:	• Support one AC input jack (power requirement: 110V ~ 220V)
PCI Slot:	• Two (for NAR-3041) / One (for NAR-3061) PCI slots for add-on PCI card
Mini PCI:	• One Mini PCI interface for mini PCI card
On-board Ethernet:	• Three (for NAR-3041-410) / Five (for NAR-3061-610) / Seven (for NAR-3061-810) Intel® 82559ER 10/100 Base-T Fast Ethernet controller with RJ-45 interface • One Intel® 82801BA (Internal MAC) + 82562ET (PHY) 10/100 Base-T Fast Ethernet controller with RJ-45 interface
Main Memory:	• One 168-pin DIMM socket supports up to 512MB of 3.3V DIMM
Hardware Monitor:	Support on-board hardware monitor for • CPU fan x 1 • Chassis fan x 3 • System voltages: Vcore, 3.3V, +5V and +12V
Power Good:	• On-board power good interval: 100ms ~ 500ms
Environmental Requirements:	• Operating Temperature: 5°C ~ 45°C • Storage Temperature: 5°C ~ 70°C • Relative Humidity: 5% 95%, non-condensing
Dimension:	• 12"(L) x 16.89"(W) x 1.74“(H)

2.11 Hardware Configuration Setting

This section gives the definitions and shows the positions of jumpers, headers and connectors. All of the configuration jumpers on PPAP-250 are in the proper position. The default settings set by factory are marked with a star (★).

Jumpers

In general, jumpers on PPAP-250 system board are used to select options for certain features. Some of the jumpers are configurable for system enhancement. The others are for testing purpose only and should not be altered. To select any option, cover the jumper cap over (Short) or remove (NC) it from the jumper pins according to the following instructions. Here NC stands for "Not Connected". (Please refer to ***Fig. 2-43*** for detailed jumper positions.)

LED-GPIO Table

LED	LED color	Which GPIO control?	Function	S/W programmable	Default status by BIOS programming
LED10	Green	N/A	HDD active indicator: *On: HDD activated* *Off: HDD*	No	N/A
LED9	Red	N/A	Non-activated power OK indicator: *On: OK* *Off: Bad*	No	N/A
LED8	Green	83.627 HF~GP17	GP_LED7	Yes	Turn on
LED7	Green	83.627 HF~GP16	GP_LED6	Yes	Turn on
LED6	Green	83.627 HF~GP15	GP_LED5	Yes	Turn on
LED5	Green	83.627 HF~GP14	GP_LED4	Yes	Turn on
LED4	Green	83.627 HF~GP13	GP_LED3	Yes	Turn on
LED3	Green	83.627 HF~GP12	GP_LED2	Yes	Turn on
LED2	Green	83.627 HF~GP11	GP_LED1	Yes	Turn on
LED1	Green	83.627 HF~GP10	GP_LED0	Yes	Turn on

Jumper Table

Jumper	Function	Default Setting
JP1	WDT function: *In: Enable* *Out: Disable*	Out: Disable
JP2	Clear CMOS RAM: *1-2: Normal* *2-3: Clear CMOS RAM*	1-2: Normal
JP3	FWH top block lock: *In: Top block unlock* *Out: Top block lock*	In: Unlock
JP4	CPU frequency strapping: *In: Force CPU frequency to safe mode* *Out: Use CPU frequency strapping in ICH2 register*	Out: by ICH2 Reg

J1/J9 Serial port connector

J1: 2x 5-pin header, J9: D-SUB9 male

PIN No.	Signal Description
1	DCD
2	RXD
3	TXD
4	DTR
5	SGND
6	DSR
7	RTS
8	CTS
9	RI
10	N/C (J1 only)

J3: Reset push button (Momentary)

PIN No.	Signal Description
1	Reset signal
2	Ground

J4: Dual USB port connector

PIN No.	Signal Description	PIN No.	Signal Description
1	+5VP0	3	+5VP0
2	USBD0-	4	USBD1-
3	USBD0+	6	USBD1+
4	Ground	8	Ground

J5-J8: Ethernet RJ45 (8P8C) connector

PIN No.	Signal Description	PIN No.	Signal Description
1	TX+	2	TX-
3	RX-	4	Term plane
5	Term plane	6	RX-
7	Term plane	8	Term plane

J13: VGA board VGA (6x2) connector

PIN No.	Signal Description	PIN No.	Signal Description
1	VID_RED	2	Ground
3	VID_GREEN	4	V1P8
5	VID_BLUE	6	Ground
7	Ground	8	3VDDCDA
9	3VDDCCL	10	CRT_HSYNC
11	CRT_VSYNC	12	V5P0

J11/J12: IDE (20x2 & 22x2) connector

PIN No.	Signal Description	PIN No.	Signal Description
1	RESET#	**2**	Ground
3	Data 7	**4**	Data 8
5	Data 6	**6**	Data 9
7	Data 5	**8**	Data 10
9	Data 4	**10**	Data 11
11	Data 3	**12**	Data 12
13	Data 2	**14**	Data 13
15	Data 1	**16**	Data 14
17	Data 0	**18**	Data 15
19	Ground	**20**	N/C ★
21	DMA REQ	**22**	Ground
23	IOW#	**24**	Ground
25	IOR#	**26**	Ground
27	IOCHRDY	**28**	Ground
29	DMA ACK#	**30**	Ground
31	IRQ15/14	**32**	N/C
33	SA1	**34**	PD1A#CSEL
35	SA0	**36**	SA2
37	HDC CS0#	**38**	HDC CS1#
39	HDD Active#	**40**	Ground

★ N/C for Proto-01
: V5P0 for Proto-02

J16/J17/J18: Tachometer fan connector

PIN No.	Signal Description
1	Ground
2	V12P0
3	Tachometer signal

J20: PCI bus connector

PIN No.	Signal Description	PIN No.	Signal Description
B1	N/C	**A1**	PTRST#
B2	PTCK	**A2**	V12P0
B3	Ground	**A3**	PTMS
B4	N/C	**A4**	PTD1
B5	V5P0	**A5**	V5P0
B6	V5P0	**A6**	PIRQ#B
B7	PIRQ#c	**A7**	PIRQ#D
B8	PIRQ#A	**A8**	V5P0
B9	N/C	**A9**	N/C
B10	N/C	**A10**	V5P0
B11	N/C	**A11**	N/C
B12	Ground	**A12**	Ground
B13	Ground	**A13**	Ground
B14	N/C	**A14**	N/C
B15	Ground	**A15**	PCIRST#
B16	PCICLK	**A16**	V5P0
B17	Ground	**A17**	PGNT#0
B18	PREQ#0	**A18**	Ground
B19	V5P0	**A19**	N/C
B20	AD31	**A20**	AD30
B21	AD29	**A21**	N/C
B22	Ground	**A22**	AD28
B23	AD27	**A23**	AD26
B24	AD25	**A24**	Ground
B25	N/C	**A25**	AD24
B26	C_BE#3	**A26**	IDSEL
B27	AD23	**A27**	N/C
B28	Ground	**A28**	AD22
B29	AD21	**A29**	AD20
B30	AD19	**A30**	Ground
B31	N/C	**A31**	AD18
B32	AD17	**A32**	AD16
B33	C_BE#2	**A33**	N/C
B34	Ground	**A34**	FRAMEN
B35	IRDY#	**A35**	Ground
B36	N/C	**A36**	TRDY#
B37	DEVSEL#	**A37**	Ground
B38	Ground	**A38**	STOP#
B39	PLOCK#	**A39**	N/C
B40	PERR#	**A40**	SDONE
B41	N/C	**A41**	SBO#
B42	SERR#	**A42**	Ground

43	N/C	**A43**	PAR
B44	C_BE#1	**A44**	AD15
B45	AD14	**A45**	N/C
B46	Ground	**A46**	AD13
B47	AD12	**A47**	AD11
B48	AD10	**A48**	Ground
B49	Ground	**A49**	AD9
	KEY		KEY
	KEY		KEY
B52	AD8	**A52**	C_BE#0
B53	AD7	**A53**	N/C
B54	N/C	**A54**	AD6
B55	AD5	**A55**	AD4
B56	AD3	**A56**	Ground
B57	Ground	**A57**	AD2
B58	AD1	**A58**	AD0
B59	V5P0	**A59**	V5P0
B60	ACK64#	**A60**	REQ64#
B61	V5P0	**A61**	V5P0
B62	V5P0	**A62**	V5P0

2.12 Install a Different Processor

Install CPU

1. Lift the handling lever of CPU socket outwards and upwards to the other end.
2. Align the processor pins with holes on the socket. Make sure that the notched corner or dot mark (pin 1) of the CPU corresponds to the socket's bevel end. Then press the CPU gently until it fits into place. If this operation is not easy or smooth, don't do it forcibly. You need to check and rebuild the CPU pin uniformly.
3. Push down the lever to lock processor chip into the socket.
4. Follow the installation guide of cooling fan or heat sink to mount it on CPU surface and lock it on the socket 370.
5. Be sure to follow particular CPU speed and voltage type to adjust the jumper settings properly for all boards.

Remove CPU

1. Unlock the cooling fan first.
2. Lift the lever of CPU socket outwards and upwards to the other end.
3. Carefully lift up the existing CPU to remove it from the socket.
4. Follow the steps of CPU installation to change to another one or place handling bar to close the opened socket.

Configure Processor Speed

The system was designed to self-detect its CPU speed. So it does not require any system adjustment.

2.13 Use a Client Computer

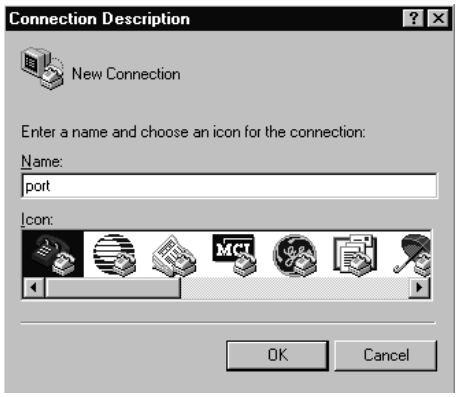
Connection Using Hyper Terminal

If users use a headless NAR-3041/3061 series, which has no mouse/keyboard and VGA output connected to it, the console may be used to communicate with NAR-3041/3061 series.

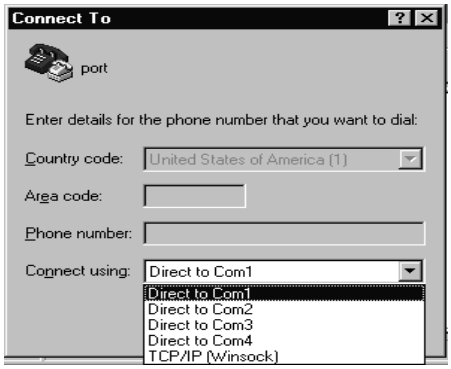
To access NAR-3041/3061 series via the console, Hyper Terminal is one of many choices. Follow the steps below for the setup:

***Note**: Terminal software may need to update for correct console output.*

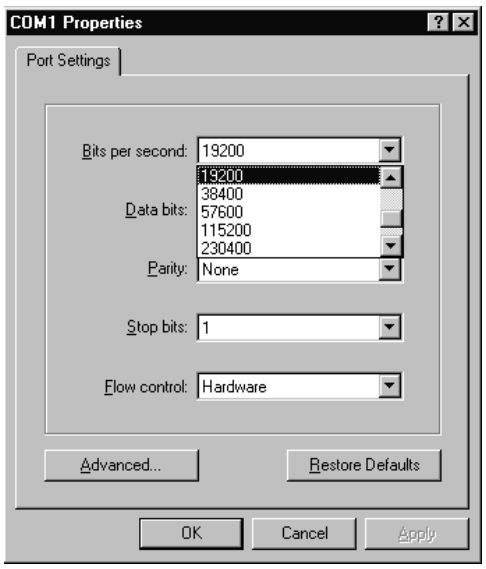
1. Execute HyperTerminal under C:\Program Files\Accessories\HyperTerminal
2. Enter a name to create new dial



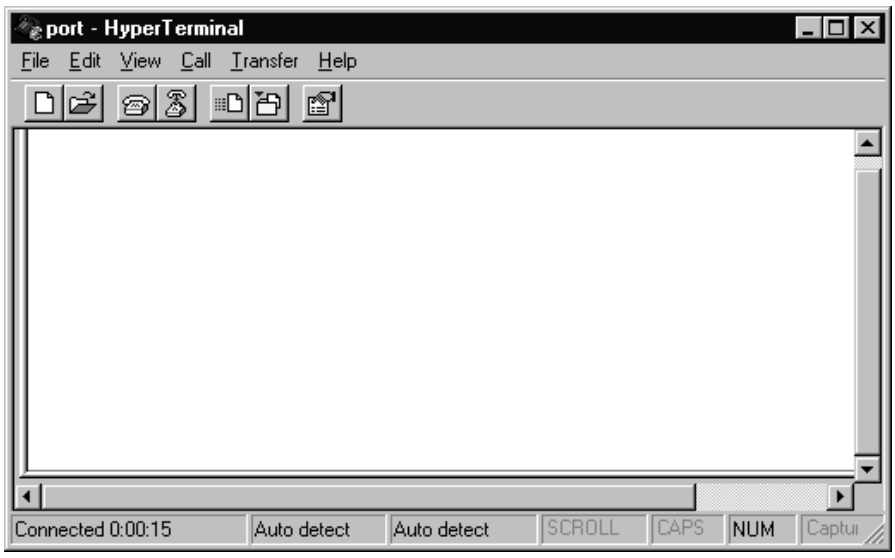
3. For the connection settings, make it Direct to Com1.



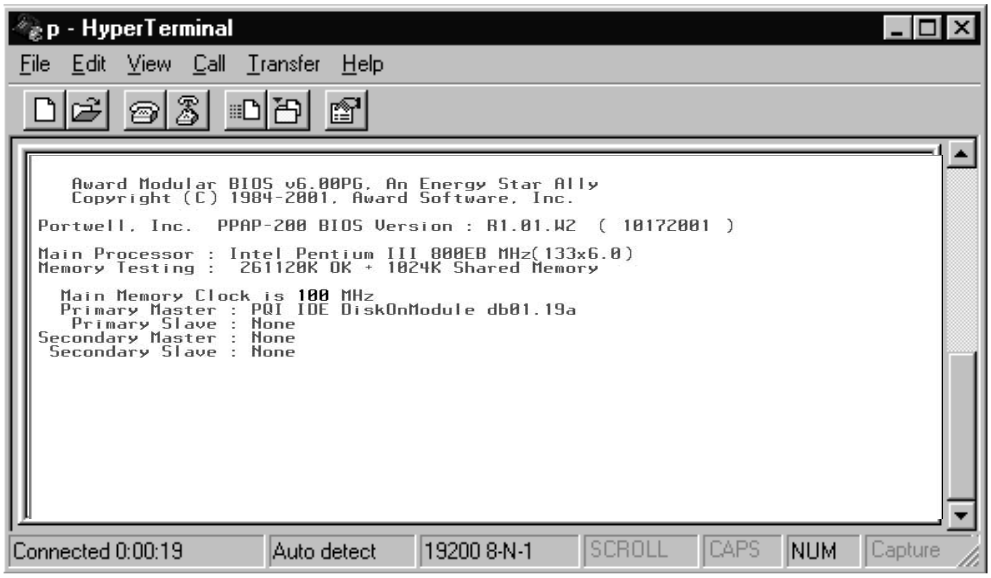
4. Please make the port settings to Baud rate 19200, Parity None, Data bits 8, Stop bits 1



5. Turn on the power of NAR-3041/3061 series, after following screen was shown:



6. You can then see the boot up information of NAR-3041/3061 series.



This is the end of this section. If the terminal did not port correctly, please check the previous steps.

2.14 BIOS Setup Information

NAR-3041/3061 series is equipped with the Award BIOS within Flash ROM. The BIOS has a built-in setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it still retains during power-off periods. When system is turned on, NAR-3041/3061 series communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. Whenever an error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the Setup program. Some errors are significant enough to abort the start-up.

Entering Setup

When message “Hit <DEL> if you want to run Setup” appear during POST, after turning on or rebooting the computer, press <Del> key ***immediately*** to enter BIOS setup program.

To enter Setup but fail to respond before the message disappears, please restart the system either by first turning it off and followed by turning it on (COLD START) or simply press the "RESET" button. “WARM START” (press <Ctrl>, <Alt>, and <Delete> keys simultaneously) will do as well.

When no setting is stored in BIOS or the setting is missing, a message “Press <F1> to run Setup” will appear. Then press <F1> to run Setup or resume HIFLEX BIOS Setup. User can use the keyboard to choose among options or modify the system parameters to match the options with your system. The table shown on next page will navigate through all of keystroke functions in BIOS Setup.

Keys to navigate within Setup menu

Key	Function
Up (↑)	Move to the previous item
Down (↓)	Move to the next item
Left (→)	Move to the item on the left (menu bar)
Right (←)	Move to the item on the right (menu bar)
Enter	Enter the item you desired
PgUp	Increase the numeric value or make changes
PgDn	Decrease the numeric value or make changes
+	Increase the numeric value or make changes
—	Decrease the numeric value or make changes
Esc	**Main Menu:** Quit and not save changes into CMOS **Status Page Setup Menu and Option Page Setup Menu:** Exit current page and return to Main Menu
F1	General help on SETUP navigation keys
F5	Load previous values from CMOS
F6	Load the fail-safe defaults from BIOS default table
F7	Load the optimized defaults
F10	Save all the CMOS changes and exit

Main Menu

Within NAR-3041/3061 series Award BIOS CMOS Setup utility, user should start with the Main Menu. The Main Menu allows to select from eleven setup functions and two exit choices. Use arrow keys to switch among items and press <Enter> to accept or bring up the sub-menu.

Phoenix – Award BIOS CMOS Setup Utility

CMOS Setup Utility	
Standard CMOS Features Advanced BIOS Features Advanced Chipset Features Integrated Peripherals Power Management Setup PnP/PCI Configurations PC Health Status	Frequency /Voltage Control Load Fail/Safe Defaults Load Optimized Defaults Set Supervisor Password Set User Password Save & Exit Setup Exit Without Saving
ESC: Quit F10: Save & Exit Setup	↑ ↓ ← →: Select Item (Shift) F2: Change Color
Time, Date, Hard Disk Type ...	

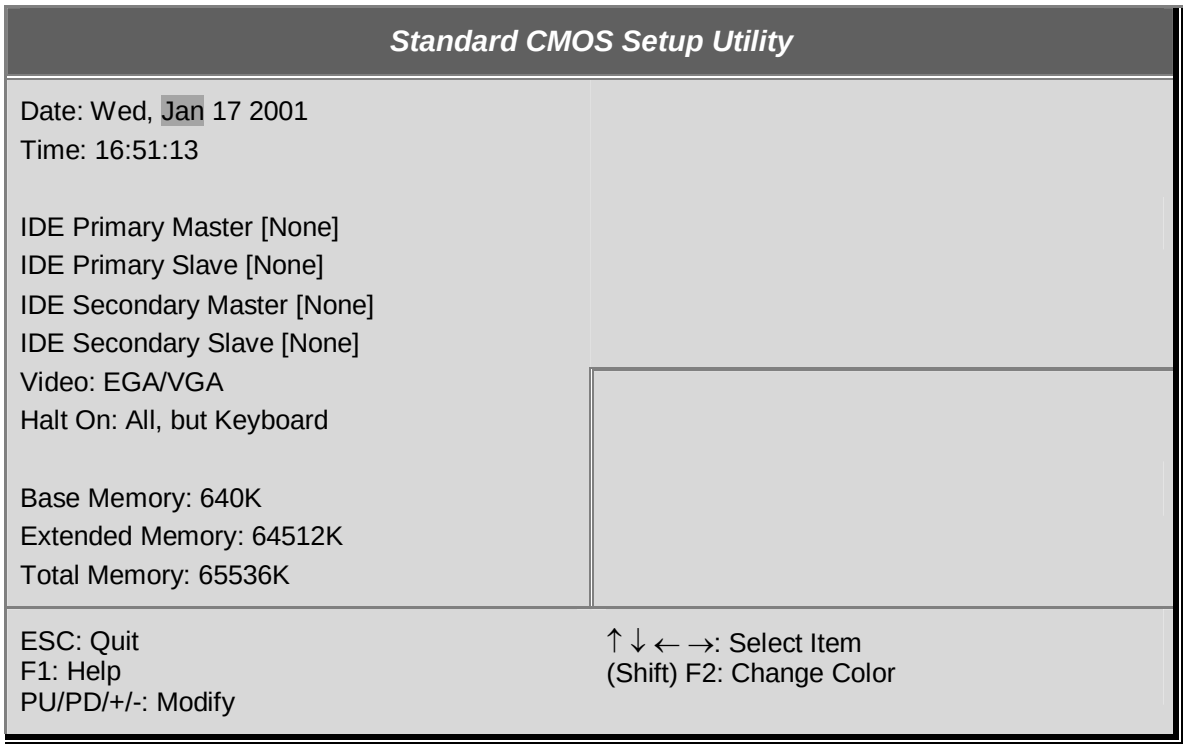
NOTE: It is strongly recommended to reload the optimized default setting if CMOS is lost or BIOS is updated.

Standard CMOS Setup Menu

This setup page includes all the items within standard compatible BIOS. Use the arrow keys to highlight the item and then use the <PgUp>/<PgDn> or <+>/<-> keys to select the value or number you want in each item and press <Enter> to certify it.

Follow command keys in CMOS Setup table to change *Date, Time, Drive type and Boot Sector Virus Protection Status*.

Screen Shot: Phoenix – Award BIOS CMOS Setup Utility



Menu Selections

Item	Options	Description
Date	mm:dd:yy	Set the system date. Note that the 'Day' automatically changes when you set the date
Time	hh:mm:ss	Set the system time
Video	EGA/VGA CGA 40CGA 80MONO	Select the default video device
Halt On	All Errors No Errors All, but Keyboard All, but Diskette All, but Disk/Key	Select the situation in which you want the BIOS to stop the POST process and notify you
Base Memory	N/A	Display the amount of conventional memory detected during boot up
Extended Memory	N/A	Display the amount of extended memory detected during boot-up
Total Memory	N/A	Display the total memory available in the system

BIOS Features Setup

This section allows you to configure your system for basic operation. You are able to select the system's default speed, boot-up sequence, keyboard operation, shadowing and security.

Screen Shot: Phoenix – Award BIOS CMOS Setup Utility

Advanced BIOS Features	
Virus Warning CPU Internal Cache: Enabled External Cache: Enabled CPU L2 Cache ECC Checking: Enabled Quick Power On Self Test: Enabled First Boot Device: USB-FDD Second Boot Device: HDD-0 Third Boot Device: LS-120 Boot Up NumLock Status: On Gate A20 Option: Normal Typematic Rate Setting: Disabled Typematic Rate (Chars/Sec): 6 Typematic Delay (Msec): 250 Security Option: Setup PCI/VGA Palette Snoop: Disabled OS Select for DRAM > 64MB: Non-OS2 Console Redirection: Enabled Baud Rate: 19200 Agent Connect via: Null Agent Wait Time (min.): 1 Agent after boot: Enable	Console Redirection: Disabled Agent connect via: NULL Agent wait time (min.): 1 Agent after boot: Disabled ESC: Quit ↑ ↓ ← →: Select Item F1: Help (Shift) F2: Color F5: Old Values F6: Load BIOS Default F7: Load Setup Default PU/PD/+/-: Modify

Internal Cache/External Cache

These two categories speed up memory access. However, it depends on CPU/chipset design.

Enabled	Enable cache
Disabled	Disable cache

Quick Power On Self Test

This category speeds up Power On Self Test (POST) after you power up the computer. If it is set to Enable, BIOS will shorten or skip some check items during POST.

Enabled	Enable quick POST
Disabled	Normal POST

Boot Up NumLock Status

Select power on state for NumLock.

The choice: Enabled/Disabled.

Gate A20 Option

This entry allows you to select how the gate A20 is handled. The gate A20 is a device used to address memory over 1 Mbytes. Originally, the gate A20 was handled via a pin on the keyboard. But now, though keyboards still provide this support, it is more common, and much faster, for the system chipset to provide support for gate A20.

Normal	Keyboard
Fast	Chipset

Typematic Rate Setting

Keystrokes repeat at a rate determined by the keyboard controller. When enabled, the typematic rate and typematic delay can be selected.

The choice: Enabled/Disabled.

Typematic Rate (Chars/Sec)

Set the how many number of times a second to repeat a keystroke when you hold the key down.

The choice: 6, 8, 10, 12, 15, 20, 24 and 30.

Typematic Delay (Msec)

Set the delay time after the key is held down before it begins to repeat the keystroke.

The choice: 250, 500, 750 and 1000.

Security Option

Select whether the password is required every time the system boots or only when entering setup.

System	The system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.
Setup	The system will boot and access to Setup will be denied if the correct password is not entered at the prompt.

Note: To disable security, select PASSWORD SETTING at Main Menu and then you will be asked to enter password. Do not type anything and simply press <Enter>, it will disable security. Once the security is disabled, the system will boot up and you can enter Setup freely.

OS Select for DRAM > 64MB

Select the operating system that is running with more than 64MB of RAM on the system.

The choice: Non-OS2, OS2.

Console Redirection

Set the UNIX Console redirect to the terminal from COM1**.**

The choice: Enabled/Disabled.

Baud Rate

Set the RS-232 baud rate speed.

The choice: 9600, 19200, 38400, 57600 and 115200.

Chapter 3 Operation Guide

3.1 Brief Guide of PPAP-250

PPAP-250 is a Communication Appliance computing board based on Intel 815E chipset technology. PPAP-250 has four on-board LAN ports to serve communication appliances, such as Firewall, which needs three Ethernet ports to connect external network (internet), demilitarized zone and internal network. Different I/O management policies can be applied respectively to individual network to achieve the highest security level. The target market segment is communication appliance including Virtual Private Network, Load Balancing, Quality of Service, Intrusion Detection, Virus Detection, Firewall and Voice Over IP.

This PPAP-250 system board is utilized with Intel® FC-PGA Celeron® and Intel® FC-PGA Pentium® III processors, and 168-pin DIMM up to 512MB DRAM. The enhanced on-board PCI IDE interface supports 2 drives up to PIO mode 4 timing and Ultra DMA/100 synchronous mode feature. The on-board super I/O chipset integrates two serial ports driven by two high performance 16C550-compatible UARTs to provide 16-byte send/receive FIFOs. In addition, the two Universal Serial Bus ports provide high-speed data communication between peripherals and PC.

The on-board flash ROM is used to make the BIOS update easier. The high precision Real Time Clock/Calendar is built to support Y2K for accurate scheduling and storing configuration information. All of these features make PPAP-250 excellent in stand-alone applications.

If any of these items is damaged or missing, please contact your vendor and save all packing materials for future replacement and maintenance.

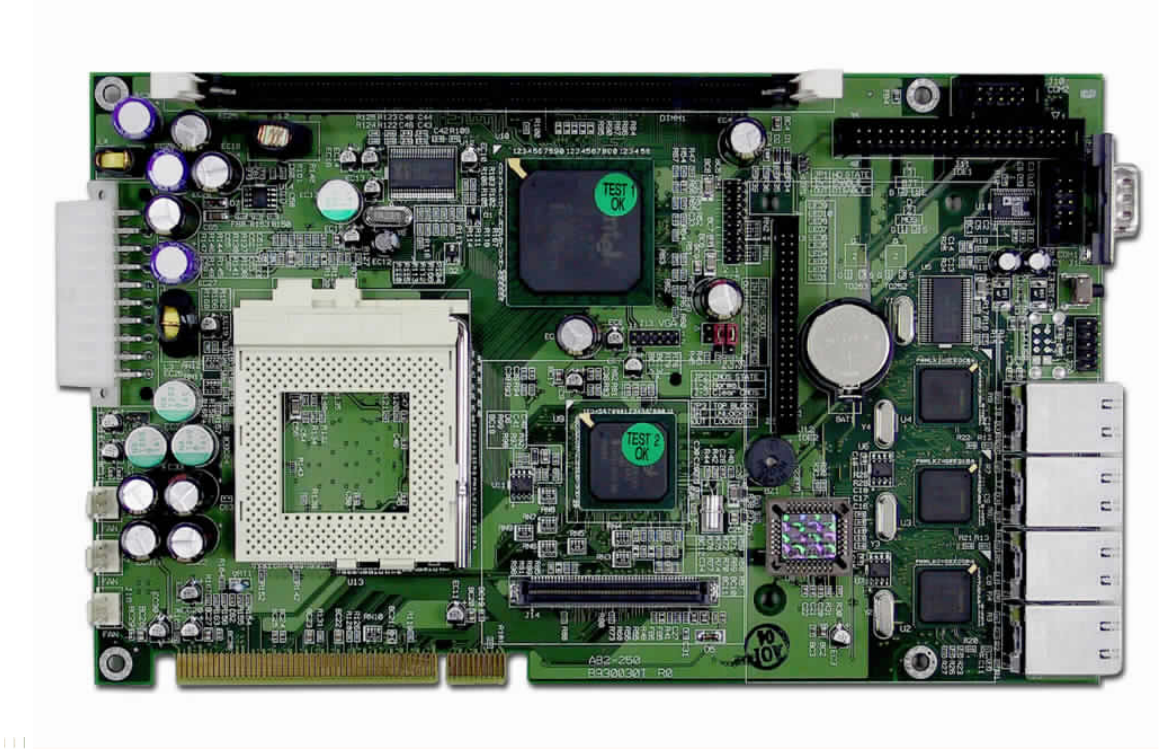


Figure 3-1 PPAP-250 Board

3.2 System Architecture

The following illustration of block diagram illustrated basic design reference of PPAP-250, a highly integrated system solution. The most up-to-date system architecture of PPAP-250 includes two main VLSI chips. It contains 82815GMCH and 82801BA ICH2 to support FC-PGA Celeron/Pentium III processor, DIMM, PCI bus interface, USB port, SMBus communication, and Ultra DMA/100 IDE Master. The on-board super I/O chip Winbond W83627HF supports two UARTs, and hardware monitoring.

PPAP-250 has built-in Socket 370 to support Intel FC-PGA Celeron/Pentium III processor (66, 100 or 133MHz system bus) for cost-effective and high performance application. However, the FC-PGA Coppermine-256 (Pentium III) processor provides twice the Celeron L2 Cache.

The 82815 GMCH provides a completely integrated solution for the system controller and data path components in a Celeron/Pentium III processor system. It provides optimized 64-bit DRAM interface with one 168 pin 3.3V DIMM.

The 82801BA ICH2 provides a highly integrated multifunction for the best industry applications. It supports 2-channel dedicated Ultra ATA/33/66/100 IDE master interface, Universal Serial Bus (**USB)** controllers and one 32-bit PCI bus interface.

All detailed operating relations are shown in ***Fig. 3-2*** (PPAP-250 System Block Diagram).

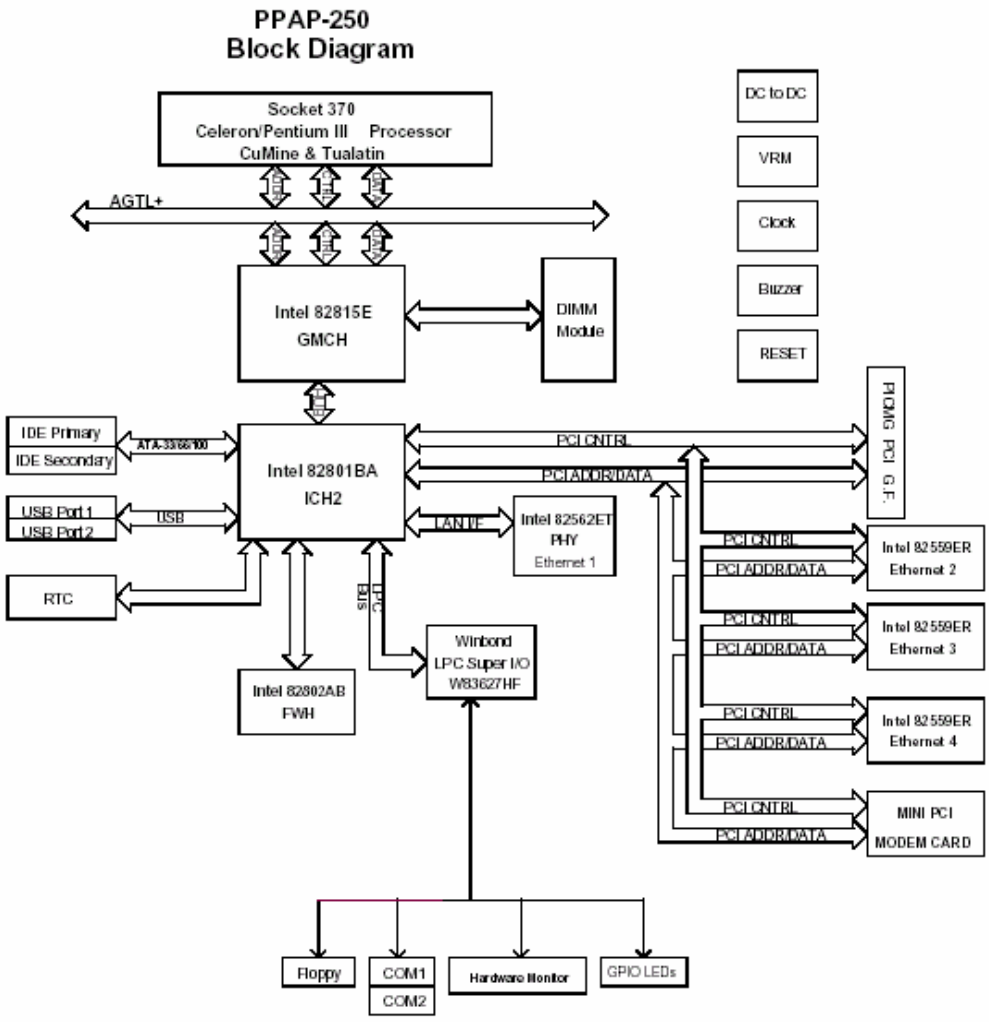


Figure 3-2 PPAP-250 815E Block Diagram