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Organisation Européenne pour des Recherches Astronomiques dans l'Hémisphère Austral
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LA SILLA OBSERVATORY

FEROS ADC CONTROL ELECTRONICS

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CHANGE RECORD

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Issue 1.0	18/04/2004	All	First Issue
Issue 2.0	10/01/2005	Section 3 Section 4 Section 6 Section 6 Section 5.5	Tables updated. Tables corrected after testing of the hardware. Several schematic diagrams corrected. PCBs drawings added. VME4SA-I components settings added.

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1. INTRODUCTION

Since the move of the Fibre-fed Extended Range Optical Spectrograph (FEROS) from the 1.52m to the 2.2m telescope the need of adding an Atmospheric Dispersion Corrector (ADC) stir up.
We believe that the overall performance of FEROS will be substantially improved with the ADC in the whole wavelength range from 350 to 920nm and thus realizing the full potential of the instrument.

1.1. PURPOSE AND SCOPE

This document is intended to serve as a design document, construction guide and service manual for the counter rotating prisms FEROS ADC control electronics. Starting from a general description and block diagram it goes all the way down to the schematic diagrams, function tables and connection tables.

1.2. REFERENCE DOCUMENTS

[RE1] http://www.ls.eso.org/lasilla/sciops/feros/Projects/ADC/index.html
[RE2] FEROS-II User Requirements LSO-URS-ESO-22400-0002 Issue 1.0 J. Pritchard June 23, 2003.
[RE3] FEROS on 2p2 Telescope New ADC Design Technical Report LSO-TRE-ESO-75441-005 Issue 2.0 A. Gilliotte May 7, 2003.
[RE4] FEROS on 2p2 Telescope Final ADC Design Technical Report LSO-TRE-ESO-75441-005 Issue 3.0 A. Gilliotte September 4, 2003.
[RE5] FEROS ADC Optical Design 2p2-DSD-ESO-60400-0003 Issue 1.2 08-December-2004.
[RE6] FEROS ADC Conceptual Design 2p2-DSD-ESO-60400-0002 Issue 1.0 J. Alonso W. Eckert A. Gilliotte February 28, 2004.

1.3. APPLICABLE DOCUMENTS

[AP1] ESO VME4SA-X1 4-Channel DC Servo Amplifier Technical Manual VLT-MAN-ESO-17130-0273 Issue 3.0
[AP2] ESO VME4SA BACKPLANE Technical Manual VLT-MAN-ESO-17130-0274 Issue 3.0
[AP3] ACROMAG Series 948x Digital I/O Boards User's Manual
[AP4] USER-Manual MACCONTROLLER MAC4-INC Version 4.2
[AP5] FAULHABER Miniature Drive Systems Manual (2001-2002).
[AP6] ADC Prism Drive Error Analysis J. Alonso July 8, 2004.
[AP7] Degradation of ADC correction due to positioning errors of the prisms Ivo Saviane July 19, 2004.

[AP8] VLT-SPE-ESO-10000-0015 VLT Electronic Design Specification Issue 4.0 09/12/96.

1.4. ACRONYMS & ABBREVIATIONS

ADC	Atmospheric Dispersion Corrector
DC	Direct Current
VME	Versa Module Europe
FEROS	Fibre-fed Extended Range Optical Spectrograph
TBD	To Be Defined
TBM	To Be Measured
VLT	Very Large Telescope
WFI	Wide Field Imager
LCU	Local Control Unit
NTT	New Technology Telescope
PCB	Printed Circuit Board
SCSM	Sliding Calibration Selection Mirror
TTL	Transistor Transistor Logic
ZD	Zenith Distance

2. ADC MOTION CONTROL

2.1. Motion Control Concept

The concept developed for the motion control of the FEROS ADC prisms is based on the standard motion control components used by ESO to build instruments. This approach brings various advantages like: reduced development and manufacturing costs, past proven experience, standardised components and shared spare parts.

The ADC arm uses the same torque drive control circuit specially designed, and actually in use, for the WFI/FEROS M3 selector mirror arm. A lower power, but functionally identical, version of the board was assembled.

2.2. Motion Control Components

The motion control electronic components used for the ADC are:

- MACC4/INC [AP4] and VME-4SA [AP1] VLT standard modules.
- La Silla "Torque Drive Control" standard module (low power version).

Two Faulhaber motor/incremental encoder units combined with init switches for defining the zero angular position are use for the ADC prism drives.

One Faulhaber motor combined with two status switches is used for the ADC swing arm.

Custom signal-conditioning electronic built over three small Printed Circuit Board (PCB) is used for converting the incremental encoder single ended signals to balanced differential and conditioning the init switches signals. Additionally these PCBs, mounted directly over the ADC main block, serve as three centralize tie points for all the ADC motion control signal connections. From this PCBs three flat cables with crimped header connectors on one end and crimped D-sub connectors on the other are use to do all the connections to the ADC inside the adapter. The three D-subs are mounted over the adapter external connector panel and the headers are plugged into the respective PCBs.
From the panel mounted D-subs two 20 meter shielded cables fitted with "HARTING Hart-Pack" and 15 pin DSUB CANNON connectors and one 20 meter shielded cable fitted with 9 pin DSUB CANNON connectors do the link to the FEROS LCU.

2.3. Motion Control Functions

The motion control functions of the ADC comprises two incremental Direct Current (DC) position servo drives without limit switches for the counter rotating doublet prisms and one DC torque drive with status switches for the swing arm.

Additionally a hardware interlocking circuit for the ADC swing arm and the Sliding Calibration Selector Mirror (SCSM) is provided. The status output of the interlock circuit is reported to the Local Control Unit (LCU) software via dedicated Acromag module input bits. Note that the interlocking between the two potentially interfering functions is done at the lowest level by a dedicated, simple and safe circuit. The LCU software has no control over this circuitry except for the fact of reading the reported status, see Figure 1 below.

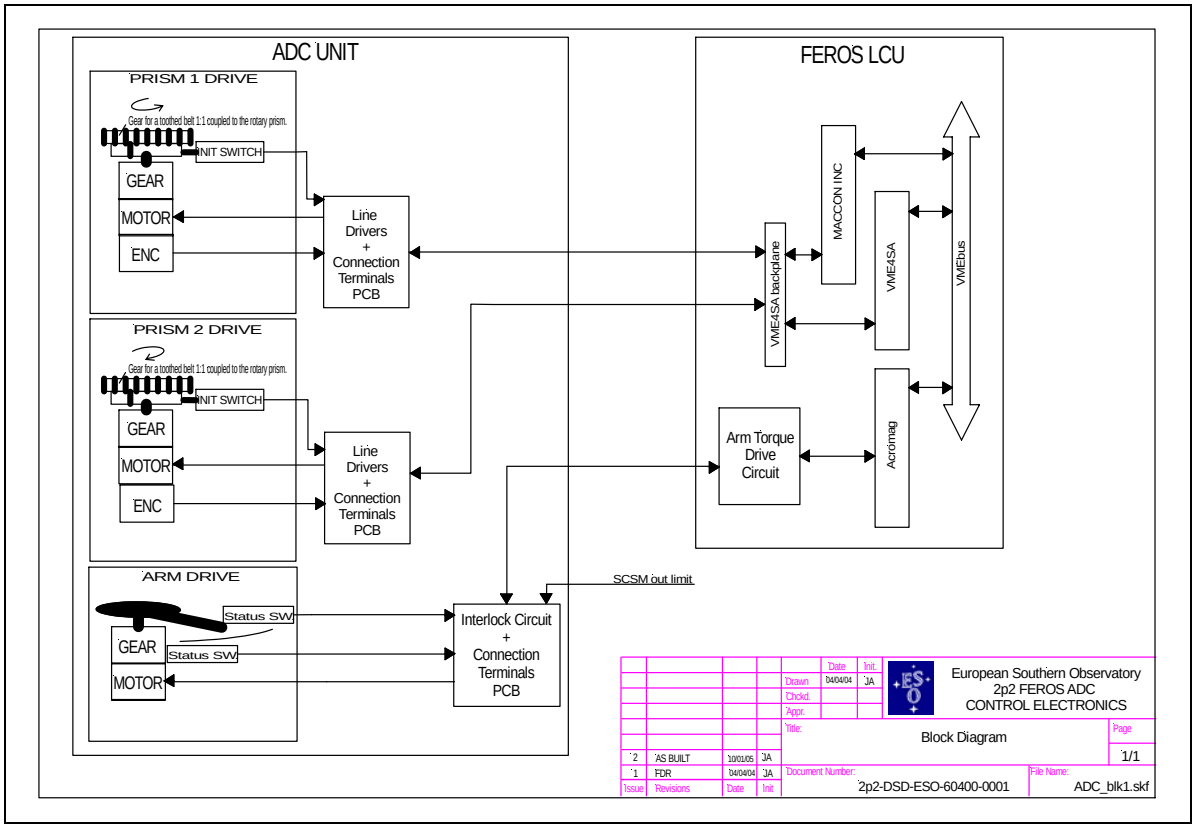


Figure 1: ADC Control Electronics Block Diagram

2.4. Prism Position and speed control loop

The rotation and angular positioning of the ADC prisms is performed by means of a position control loop.

The main loop is the position control loop, starting with an incremental encoder, directly coupled to the DC motor, to sense the relative angular position. A dedicated VME motion controller MAC4/INC [AP4] compares the sensed position with the position command value calculated by the main instrument control software and generates a corrective action (+/-10Vdc range) to the VME4SA servo-amplifier. The configuration software sets the position controller parameters like integration gain, maximum speed, software limits, initialization point, etc.

The corrective output signal (± 10V) generated by the position control loop is sent to the VME servo-amplifier VME4SA [AP1] controlling the motor speed. The motor speed is measured by means of the same encoder used for measuring the position. This error signal is power amplified inside the VME4SA [AP1] to drive the DC motor.

The prisms have no limit switches they can rotate endlessly. Motor current limitation is provided as a hardware protection against high drive-mechanism friction. The current limit is defined by a resistor inside the VME4SA and can be read back by the LCU with 8 bit resolution.

2.5. Arm Position Torque Control

The in-out positioning of the ADC arm is accomplished by a dedicated torque drive card, the same used for the WFI/FEROS M3 selection mirror.

Basically this circuit drives the arm motor via an adjustable current source with 24V compliance. When the arm is freely moving, only the friction of the mechanism is drawing current, the voltage in the motor terminals is 24V. As soon as the arm reaches the hard limit-stop the voltage on the motor terminals drops and the current reaches the set constant value with the motor-arm effectively stuck against the limit and finally the current is shut off automatically by the circuitry.

The mechanism of the arm uses two cascaded reduction gear stages, one is over the motor and the other is a self-blocking worm gear combination. Additionally the self-blocking gear and the arm are connected together by a torsion coupling and the in-out positions of the arm are defined by two stable hard-limit mechanical stops.

Being possible to adjust the constant current source by the aid of a trim-pot mounted over the card, effectively and accurately defines the degree of force exerted by the arm over the stops, or equally the degree of torsion exerted over the coupling and thus keeping the arm mechanically stable on position. The in and out positions are monitored by status switches, this switches report back the status and are part of the interlock circuit between the arm and the SCSM.

3. ADC DRIVES ELECTROMECHANICAL COMPONENTS

3.1. Prism Drive

Both prisms drives are identical and therefore use the same electromechanical components.

Reduction gear type		FAULHABER-16/7
Gear ratio		246:1
Maximum speed	Rpm	5000
Nominal static torque	Nm	0.3

Table 1: Prism Drive Gear Head

Manufacturer		FAULHABER
Type		1724T024SR
Maximal speed	Rpm	8600
Nominal output torque	mNm	11.5
Maximal power	W	4
Voltage	V	24
Maximal current	mA	180
Winding resistance	Ohm	55
EMF	mV/rpm	2.8
Operating temperature	ºC	-30 +85

Table 2: Prism Drive DC Motor

Type		FAULHABER Series IE2-16 (Magnetic)
Lines per revolution		16
Supply voltage	V	4.5 to 5.5
Current consumption	mA	5
Max output current	mA	-
Output		Two quadrature TTL 50% duty cycle signals

Table 3: Prism Drive Incremental Encoder

The initialization position switch is a BAUMER type “My-Com g”

3.2. Arm Drive

Reduction gear type		FAULHABER-23/1
Gear ratio		415:1
Maximum speed	Rpm	4000
Nominal static torque	Nm	0.7

Table 4: Arm Drive Gear Head

Manufacturer		FAULHABER
Type		2338S024S
Maximal speed	Rpm	7600
Nominal output torque	mNm	17.6
Maximal power	W	3.5
Voltage	V	24
Maximal current	mA	300
Winding resistance	Ohm	38
EMF	mV/rpm	3.03
Operating temperature	ºC	-30 to +85

Table 5: Arm Drive DC Motor

The limit-switches are MICRO type “ISX48-T”. The arm “out position” uses two stacked units. The “arm in” position uses a single unit.

The self blocking worm gear driving the arm has a 25:1 ratio.

3.3. Gear Ratio and Encoder Resolution

3.3.1. Prism Drive

The requirement for the prism angular positioning is within 1 deg, the prism tracking speed shall be 2.5deg/min and the presetting speed 90deg/min.

Presetting speed = 0.25rpm.
Motor speed at full MAC4 INC output = 5000rpm (loaded by the gear-head).
Gear-head ratio = 20000:1

We choose the 246:1 gear-head from [AP5] and Table 1 we get:

Maximum presetting speed = 20rpm.
Angular resolution = 1’17” (including the MACC4 INC X4 interpolation factor).

The prism tracking speed resolution could be down to 0HZ in steps of 1'17". Although we choose the lowest resolution encoder, 16pulses/rev, due to the reduction gear and the MACC interpolation factor we get a fairly high resolution for the application (15744 counts per prism revolution at the MACCON).

The gear-head is preloaded to zero backslash so we can assume safely an angular positioning accuracy for the prism better than 1 deg. We do not have information concerning the periodic errors of the gear-head. This information could be requested if required. Please refer to [AP6] and [AP7] for further details.

3.3.2. Arm Drive

The required overhead for the ADC is 2 minutes time maximum.

The worst case is when the SCSM is in the optical path, the ADC prisms are 180deg away from the desire position and the ADC arm is out.

Prism 180deg turn time = 3.2sec
SCSM out time < 60sec

We choose the 415:1 gear-head from [AP5] Table 4: Arm Drive Gear Head and considering the 25:1 worm gear we get a ninety deg. arm swing time of 20.5 sec.

4. FEROS LCU ACROmag DIGITAL I/O

The FEROS LCU uses a single ACROmag digital I/O module. Refer to [AP3] for a full description and data of this VME module.

The ACRO signals used by the ADC are:

- ADC ARM IN\ (active low) ACRO input
- ADC ARM OUT\ (active low) ACRO input
- ADC ARM REM (active high) ACRO input
- SCSM OUT (active high) ACRO input
- ADC ARM OUT (active high) ACRO output (command signal)

4.1. SCSM and ARM Interlock Reporting

	STATE	ADC ARM OUT\ (ACRO input bit)	SCSM OUT (ACRO input bit)
1	Arm out & SCSM out	0	1
2	Arm in & SCSM out	1	1
3	Arm out & SCSM in	0	0
4	Invalid (collision)	1	0

Table 6: ADC Arm and SCSM States Status Reporting

The LCU software cannot drive these functions to state 4 of Table 6 above, any attempt by the software to do so will result in an error because they are interlocked by hardware. This is because physically both the ADC arm and the SCSM live in the same place when operative.
The LCU software shall always check the state before attempting to move the functions.
If state 4 is ever read-in by the software an error message shall be issued requesting hardware service.
Refer to Table 9 below for the VLT bit assignation of the signals. The trailing backslash at the signal name indicates active low.

4.2. Arm Status

	STATE	ADC ARM OUT\ (ACRO input bit)	ADC ARM IN\ (ACRO input bit)	ADC ARM REM (ACRO input bit)
1	Arm out (remote)	0	1	1
2	Arm in (remote)	1	0	1
3	Arm moving (remote)	1	1	1
4	Arm moving	0	0	1
5	Arm out (local)	0	1	0
6	Arm in (local)	1	0	0
7	Arm moving (local)	1	1	0
8	Arm moving	0	0	0

Table 7: ADC Arm States Status Reporting

Refer to Table 9 below for the VLT bit assignation of the signals. The trailing backlash at the signal name indicates active low.
If the arm is under local control all the statuses, Table 7, are still readable and valid.

4.3. Arm Command

	STATE	ADC ARM OUT (ACRO output bit)	ADC ARM REM (ACRO input bit)
1	Arm moves in (remote)	0	1
2	Arm moves out (remote)	1	1
3	Arm under local control	X	0

Table 8: ADC Arm Control

If the arm is under local control all the statuses, Table 7, are still readable and valid. Refer to Table 9 below for the VLT bit assignation of the signals.

4.4. P2 Pin-out and Bit Assignment

ACRO Pin	Direction	Signal	VLT BIT
B32	IN	P0 bit 0 OUT\ (M3 ARM)	0
B31	IN	P0 bit 1 IN\ (M3 ARM)	1
B30	IN	P0 bit 2 REM (M3 ARM)	2
B29	OUT	P0 bit 3 OUT (M3 ARM)	3
B28		P0 bit 4	4
B27		P0 bit 5	5
B26		P0 bit 6	6
B25		P0 bit 7	7
B24	OUT	P1 bit 0 FFon (Flat Field Lamp)	8
B23	OUT	P1 bit 1 WC1on (Wave length Calibration)	9
B22	OUT	P1 bit 2 XX (Lamp X)	10
B21	IN	P1 bit 3 FFon feedback	11
B20	IN	P1 bit 4 WC1on feedback	12
B19	IN	P1 bit 5 Lamp X feedback	13
B18		P1 bit 6	14
B17		P1 bit 7	15
A32	OUT	P2 bit 0 REDon (CCD Illumination)	16
A31	IN	P2 bit 1 REDon feedback	17
A30	OUT	P2 bit 2 GREENon (CCD Illumination)	18
A29	IN	P2 bit 3 GREEN feedback	19
A28	OUT	P2 bit 4 BLUEon (CCD Illumination)	20
A27	IN	P2 bit 5 BLUE feedback	21
A26	OUT	P2 bit 6 220V switching	22
A25	IN	P2 bit 7 feedback 220V switching	23
A24		P3 bit 0	24
A23		P3 bit 1	25
A22		P3 bit 2	26
A21		P3 bit 3	27
A20		P3 bit 4	28
A19		P3 bit 5	29
A18		P3 bit 6	30
A17		P3 bit 7	31

C32		P4 bit 0	32
C31		P4 bit 1	33
C30		P4 bit 2	34
C29		P4 bit 3	35
C28		P4 bit 4	36
C27		P4 bit 5	37
C26		P4 bit 6	38
C25		P4 bit 7	39
C24		P5 bit 0	40
C23		P5 bit 1	41
C22		P5 bit 2	42
C21		P5 bit 3	43
C20		P5 bit 4	44
C19		P5 bit 5	45
C18		P5 bit 6	46
C17		P5 bit 7	47
A1		P6 bit 0	48
A2		P6 bit 1	49
A3		P6 bit 2	50
A4		P6 bit 3	51
A5		P6 bit 4	52
A6		P6 bit 5	53
A7		P6 bit 6	54
A8		P6 bit 7	55
A9	**INPUT**	**P7 bit 0 ADC ARM OUT\ (JP3)**	**56**
A10	**INPUT**	**P7 bit 1 ADC ARM IN\ (JP5)**	**57**
A11	**INPUT**	**P7 bit 2 ADC ARM REM**	**58**
A12	**OUTPUT**	**P7 bit 3 ADC ARM OUT**	**59**
A13	**INPUT**	**P7 bit 4 SCSM OUT (JP1)**	**60**
A14		P7 bit 5	61
A15		P7 bit 6	62
A16		P7 bit 7	63
B9	-	5 Volts	-
B13	-	GND M3	-
B14	-	GND M3	-
B15	-	GND M3	-
B16	-	GND M3	-
B12	-	REF Ports 0 & 1	-
B11	-	Pullup Ports 0 & 1	-
B10	-	Protect Ports 0 & 1	-
B1	-	5 Volts	-
B5	-	GND lamps	-
B6	-	GND lamps	-
B7	-	GND	-
B8	-	GND	-
B4	-	REF Ports 2 & 3	-
B3	-	Pullup Ports 2 & 3	-
B2	-	Protect Ports 2 & 3	-
C9	-	5 Volts CCD Illumination	-
C15	-	GND CCD Illumination	-
C16	-	GND CCD Illumination	-
C13	-	GND CCD Illumination	-
C14	-	GND CCD Illumination	-

C12	-	REF Ports 4 & 5	-
C11	-	Pullup Ports 4 & 5	-
C10	-	Protect Ports 4 & 5	-
C1	**-**	**5 Volts ADC ARM**	**-**
C5	**-**	**GND ADC ARM**	**-**
C6	**-**	**GND ADC ARM**	**-**
C7	**-**	**GND ADC ARM**	**-**
C8	**-**	**GND ADC ARM**	**-**
C4	-	REF Ports 6 & 7	-
C3	-	Pullup Ports 6 & 7	-
C2	-	Protect Ports 6 & 7	-

Table 9 : ACRO digital I/O pin-out and bit assignment

5. ADC CABLING

5.1. ADC

Three small PCB cards are mounted over the ADC main block refer to 6.1 for a global view.

Two of them are identical and correspond to prism drive 1 and 2. Over these cards all the necessary conditioning circuits and cable soldering pads are provided to directly connect the motor, encoder and init switch. Refer to 6.5 and 6.6 for detailed connection point numbering-naming and circuit diagram. Additionally over the PCB a 14 pin male header connector serve as link to the outside world for the particular function.

The third PCB corresponds to the SCSM-Arm interlock circuit and additionally serves the same purpose, as explained above for the prism drive, but this time for the arm drive. Over the PCB a 10pin male header connector serve as link to the outside world for the particular function. Refer to 6.7 and 6.8 for detailed connection point numbering-naming and circuit diagram.

5.2. ADC to Adapter connector panel

Three flat cables with crimped, one to one, header and Cannon D-sub connectors are used to bring the function signals to the adapter connector panel.

	Header Sex – Pin#	Cannon Sex – Pin#	Length cm
Prism 1	Female 14	Male 15	TBM
Prism 2	Female 14	Male 15	TBM
Arm	Female 10	Male 9	TBM

Table 10 : Adapter internal cabling

5.3. Adapter connector panel to LCU

Three separate shielded cables link the adapter connector panel to the FEROS LCU. Refer to 6.3 and 6.4 for the detailed schematic diagram, length and construction details of these cables.

5.4. Inside the LCU

Refer to 6.2 for details on the wiring inside the LCU chassis.

Please note that the prism functions only need the mounting of a VME4SA-MACC-INC backplane plus the standard wiring specified on [AP2] (Vx = 5V). The cable ends of the prism functions are directly plugged onto the HARTING connectors of the new backplane.

5.5. VME4SA-I Component Adapter Configuration

For each channel the VME4SA has an eight pin dual in line socket for plugging a small carrier whose components are dependent on the application, refer to [AP1] page 8 for a detailed explanation.
In this application the configuration for channels 1 and 2 is identical and as shown in the table below.

Pin # row 1	Pin # row 2	Component
1	8	Open
2	7	150K
3	6	Wire Jumper
4	5	Open

Table 11 : VME4SA Component Adapter Configuration

6. DRAWING and SCHEMATIC DIAGRAM APPENDIX

The drawings and circuit schematic diagrams are listed below and annexed to this document as eleven A4 format sheets.

6.1. Block Diagram

6.2. ARM Torque Drive LCU Layout

6.3. Prism Servo Cable (LCU to Adapter)

6.4. ARM Cable (LCU to Adapter)

6.5. Prism Drive Connection Block

6.6. Prism Drive Line Drivers Schematic

6.7. Arm Connection Block

6.8. ARM-SCSM Interlock Schematic

6.9. Arm Torque Drive Connection Block

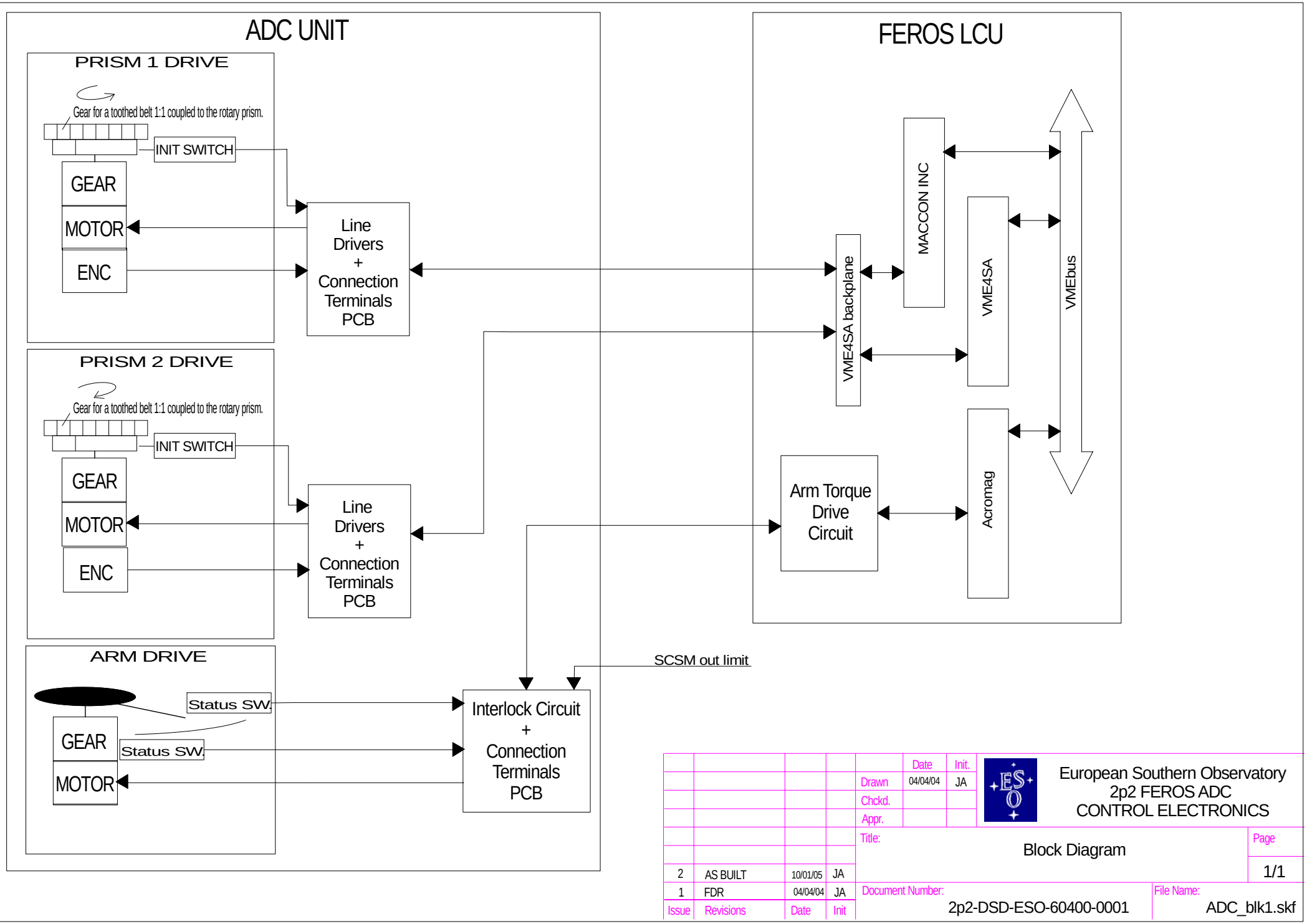
6.10. Arm Torque Drive Module Schematic 1

6.11. Arm Torque Drive Module Schematic 2

6.12. FEROS ADC prism drive connection PCB

6.13. FEROS ADC arm interlock PCB

6.14. FEROS/WFI mirror selector and ADC arm circuit PCB



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Title: Block Diagram

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Issue	Revisions	Date	Init
2	AS BUILT	10/01/05	JA
1	FDR	04/04/04	JA

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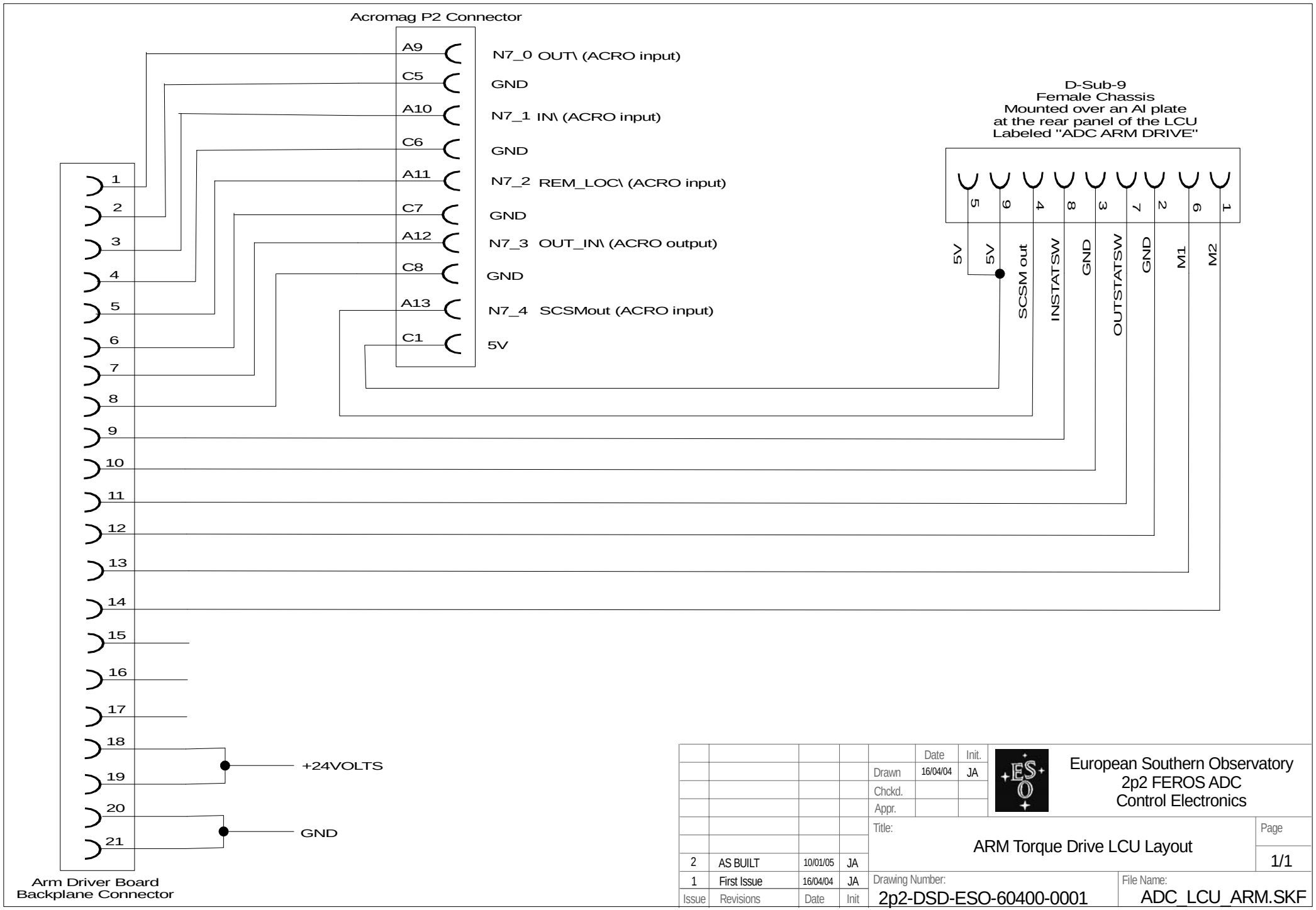

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Control Electronics

Title: ARM Torque Drive LCU Layout

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Issue	Revisions	Date	Init
2	AS BUILT	10/01/05	JA
1	First Issue	16/04/04	JA

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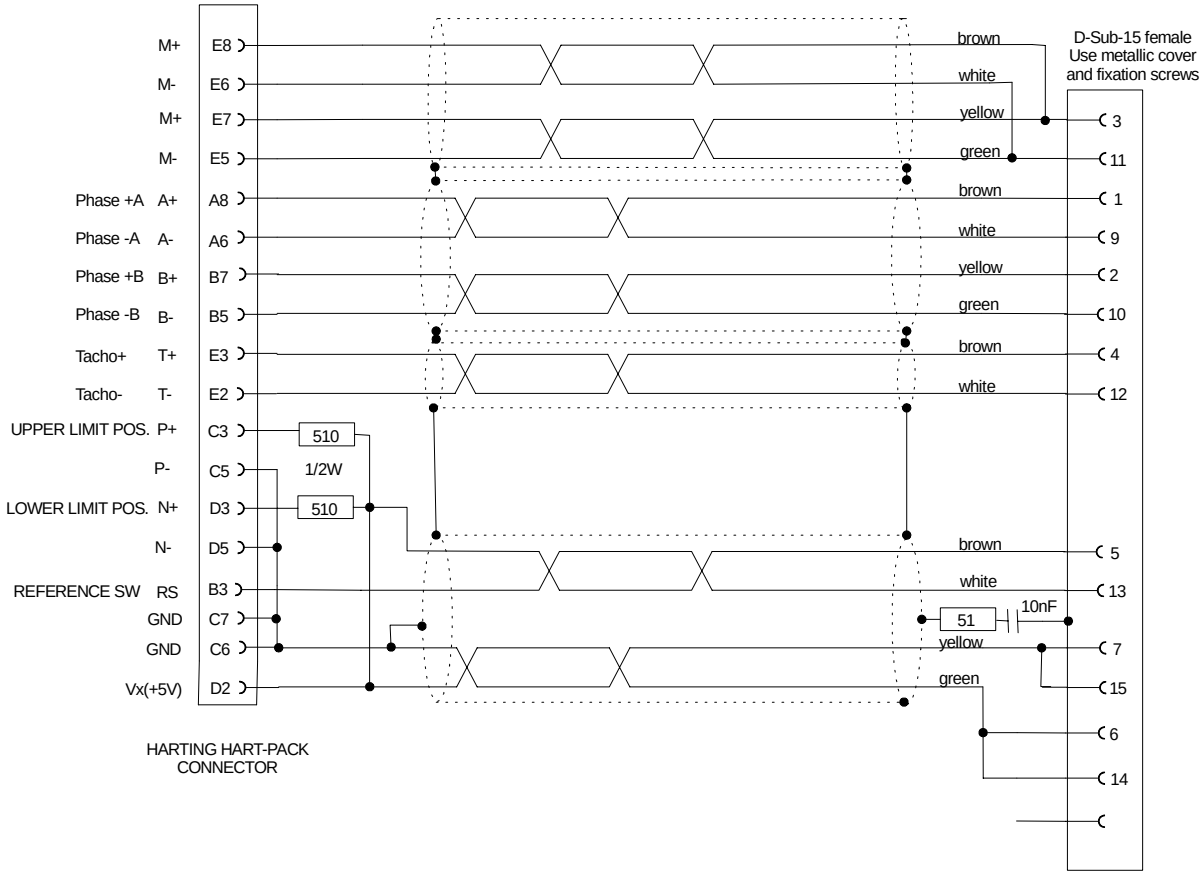

NOTES:

- Lenght 20m
- Quantity 2 units
- Complete double electrical test, pin to pin and chek for shorts between lines.
- At the Harting connector side the cables must point downward when plugged in the VME4SA backplane.
- The 510 Ohm resistors shall be inside the Harting connector cover properly insulated.
- Use heat shrinkable tube at the Harting side to fix the cables firmly to the cover and have EFECTIVE strain relief.
- House the 51 Ohm resistor and the capacitor inside the connector cover.
- At the D-sub side the shield must be insulated and connected to the connector housing as shown.

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2	AS BUILT	10/01/05	JA
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	Date	Init.
Drawn	17/04/04	JA
Chckd.		
Appr.		

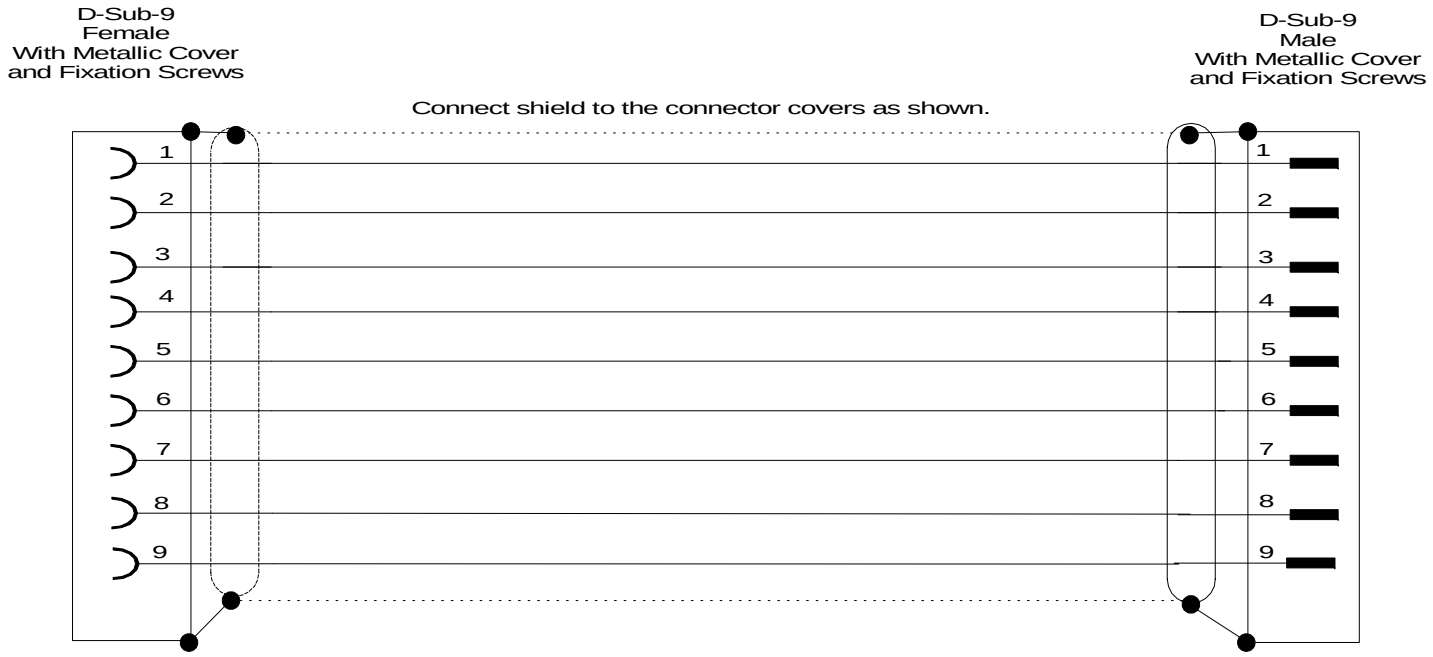
European Southern Observatory
2p2 FEROS ADC
Control Electronics

Title: Prism Servo Cable (LCU to ADAPTER)

Page: 1/1

Document Number: 2p2-DSD-ESO-60400-0001

File Name: ADC_P_CABLE.SKF



NOTES

- Cable type 15 x 0.25sqmm shielded
- Lenght 20 meters
- Quantity 1

					Date	Init.
				Drawn	16/04/04	JA
				Chckd.		
				Appr.		

European Southern Observatory
2p2 FEROS ADC
Control Electronics

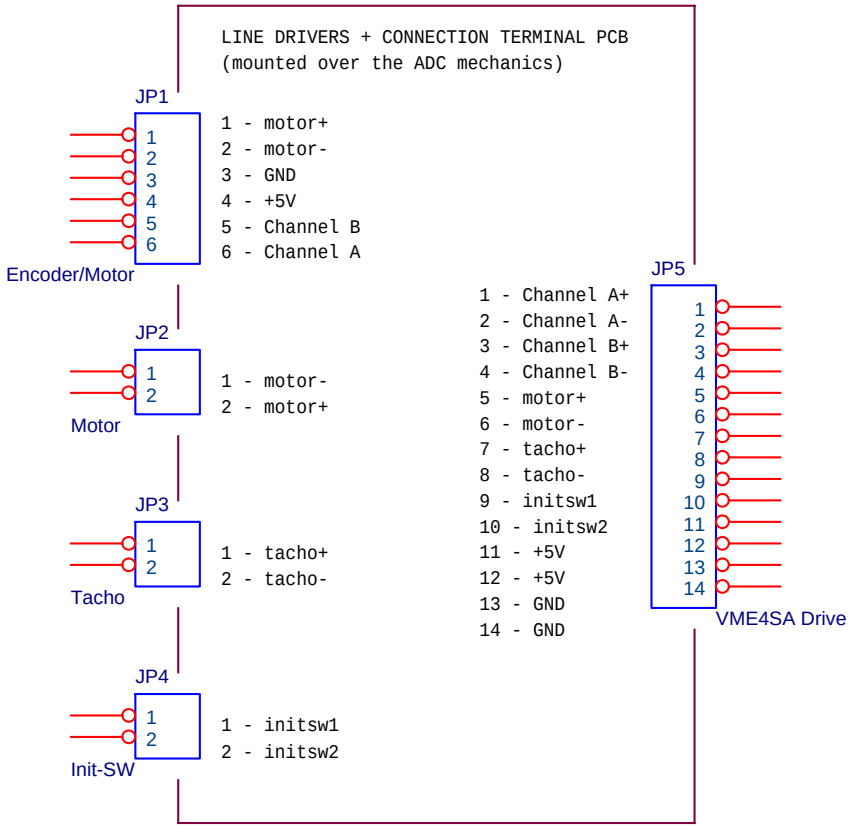
Title: ARM Cable (LCU to ADAPTER)

Page: 1/1

Issue	Revisions	Date	Init
1	AS BUILT	10/01/05	JA
1	First Issue	16/04/04	JA

Drawing Number: 2p2-DSD-ESO-60400-0001

File Name: ADC_A_CABLE.skf

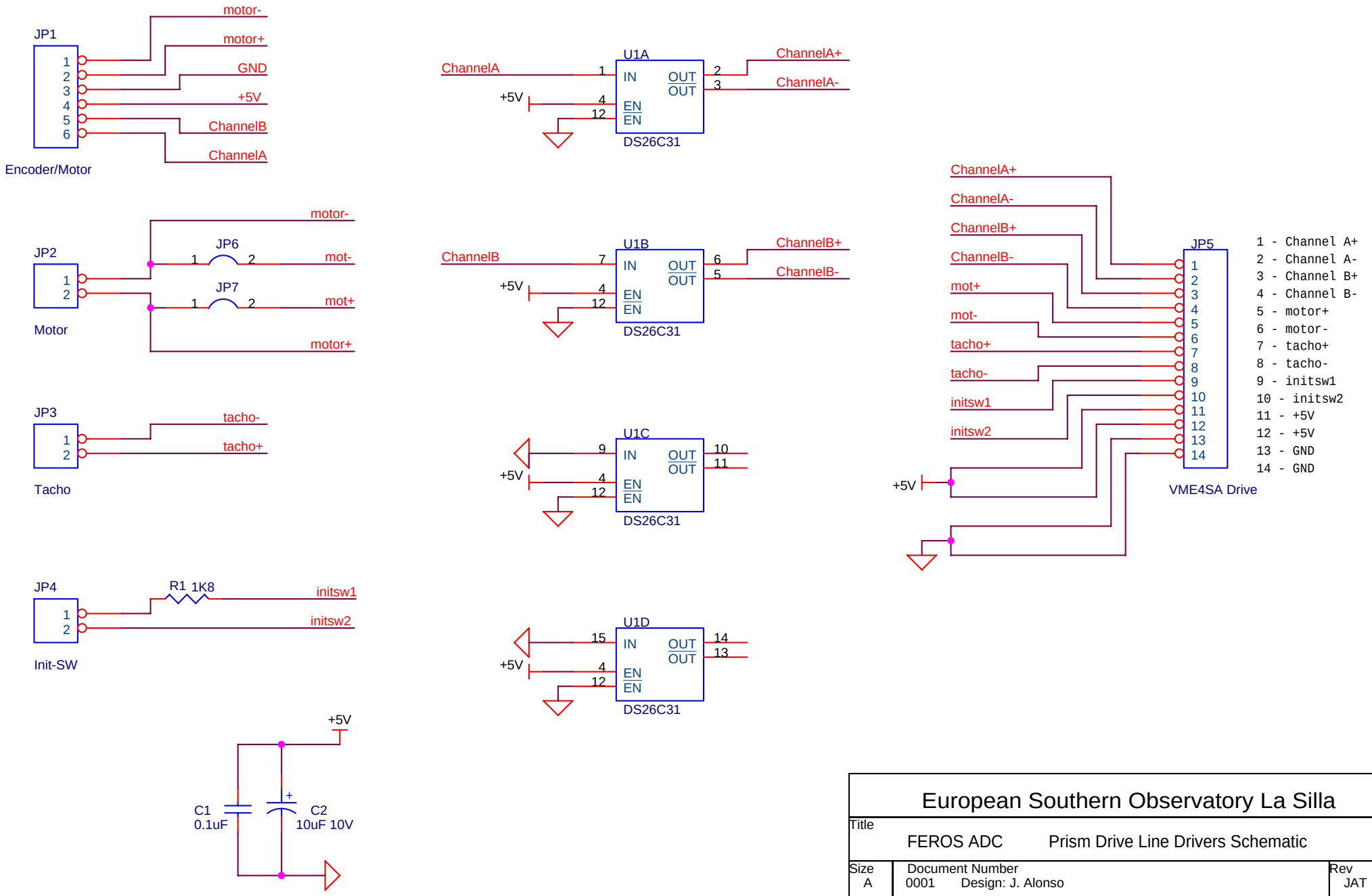


European Southern Observatory La Silla

Title: FEROS ADC Prism Drive Connection Block

Size	Document Number	Rev
A	0001 Design: J. Alonso	JAT

Date: Monday, January 10, 2005 Sheet 1 of 3



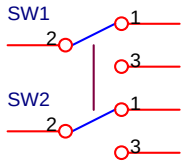
European Southern Observatory La Silla

Title: FEROS ADC Prism Drive Line Drivers Schematic

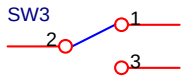
Size	Document Number	Rev
A	0001 Design: J. Alonso	JAT

Date: Sunday, August 22, 2004 Sheet 1 of 1

ADC ARM STATUS SWITCHES
(arm at mid travel)



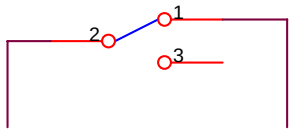
ARM OUT STAT SW



ARM IN STAT SW

SCSM PARK SWITCH

SCSM park switch



To JP1 (contacts shown in parked position)

INTERLOCK CIRCUIT + CONNECTION TERMINAL PCB
(mounted over the ADC mechanics)

JP1
2
1
1 - switch
2 - switch

SCSM park

JP2
4
3
2
1
1 - SW2 3
2 - SW2 2
3 - SW1 1
4 - SW1 2

ARM OUT STAT SW

JP6
2
1
1 - SW3 1
2 - SW3 2

ARM IN STAT SW

JP5
2
1
1 - motor+
2 - motor-

ARM motor

JP3
2
1
1 - G1
2 - G2

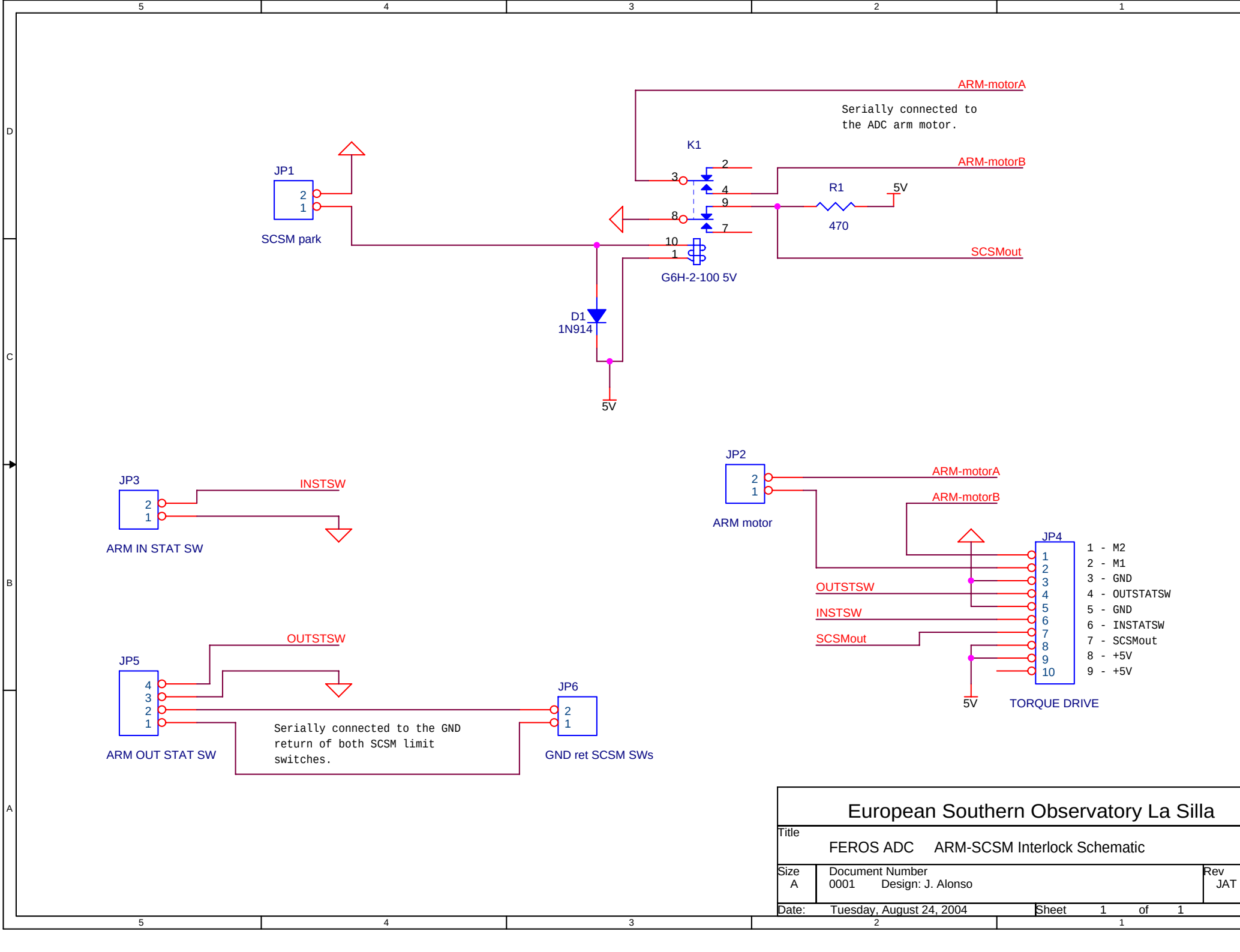
GND ret SCSM SWs

Serially connected to the GND return of both SCSM limit switches.

JP4
1 - M2
2 - M1
3 - GND
4 - OUTSTATSW
5 - GND
6 - INSTATSW
7 - SCSMout
8 - +5V
9 - +5V
10

Torque Drive

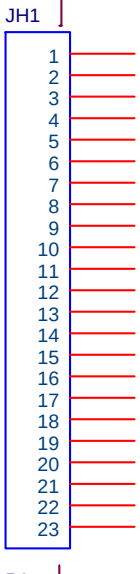
European Southern Observatory La Silla		
Title: FEROS ADC Arm Connection Block		
Size: A	Document Number: 0002 Design: J. Alonso	Rev: JAT
Date: Monday, January 10, 2005	Sheet 2 of 3	


ARM-motorA
Serially connected to
the ADC arm motor.
K1
JP1
2
1
SCSM park
3
2
4
9
8
7
10
1
G6H-2-100 5V
ARM-motorB
R1
5V
470
SCSMout
D1
1N914
5V
JP3
INSTSW
2
1
ARM IN STAT SW
JP2
2
1
ARM motor
ARM-motorA
ARM-motorB
JP4
1
2
3
4
5
6
7
8
9
10
1 - M2
2 - M1
3 - GND
4 - OUTSTATSW
5 - GND
6 - INSTATSW
7 - SCSMout
8 - +5V
9 - +5V
OUTSTSW
INSTSW
SCSMout
5V
TORQUE DRIVE
OUTSTSW
JP5
4
3
2
1
ARM OUT STAT SW
Serially connected to the GND
return of both SCSM limit
switches.
JP6
2
1
GND ret SCSM SWs
European Southern Observatory La Silla
Title
FEROS ADC ARM-SCSM Interlock Schematic
Size
A
Document Number
0001 Design: J. Alonso
Rev
JAT
Date: Tuesday, August 24, 2004
Sheet 1 of 1

FEROS ADC ARM TORQUE DRIVE CIRCUIT (CARD)
(plugged into the FEROS LCU)

1 - Arm Out Status (output) OUT\
2 - Signal GND
3 - Arm In Status (output) IN\
4 - Signal GND
5 - Remote / Local Status (output) REMLOC\
6 - Signal GND
7 - Arm In / Out Command (input) OUTIN\
8 - Signal GND
9 - In Status Switch Connection
10 - In Status Switch Return
11 - Out Status Switch Connection
12 - Out Status Switch Return
13 - Motor Terminal 1
14 - Motor Terminal 2
15 - N.C
16 - N.C.
17 - N.C..
18 - +24 Volts Power Supply
19 - +24 Volts Power Supply
20 - Power Supply 0 Volts
21 - Power Supply 0 Volts

- Power Supply Consumption 1 Ampere Maximum
- Output Signals 0 - 5V level 10mA source/sink.
- Input Signal 0-5V level 1K internal pull-up.



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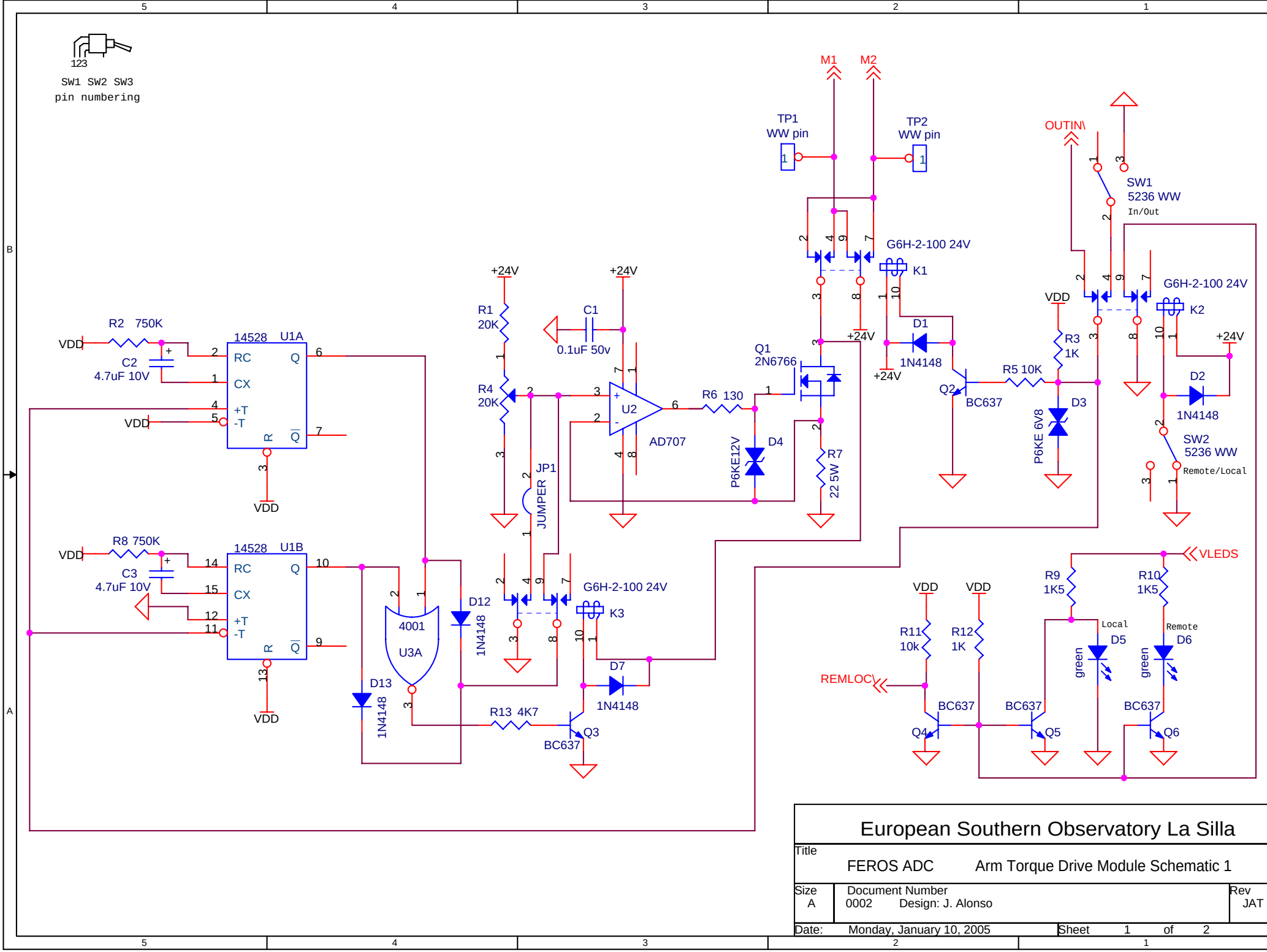
Title: FEROS ADC Arm Torque Drive Connection Block

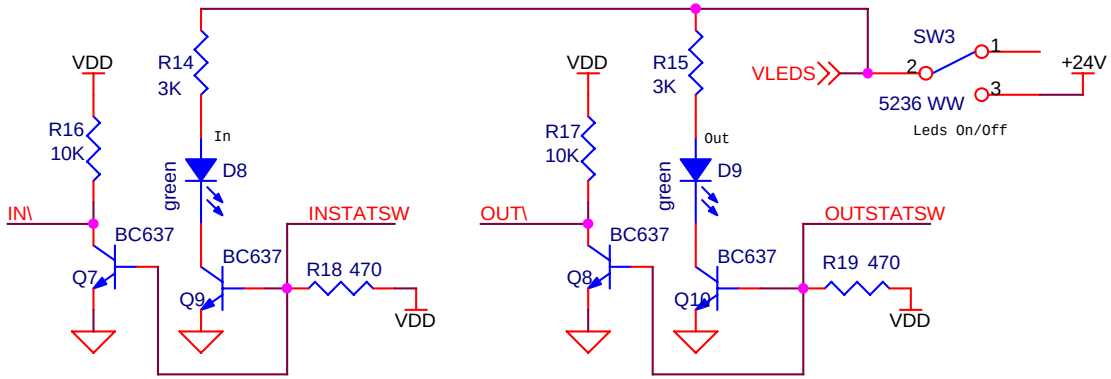
Size	Document Number	Rev
A	0002 Design: J. Alonso	JAT

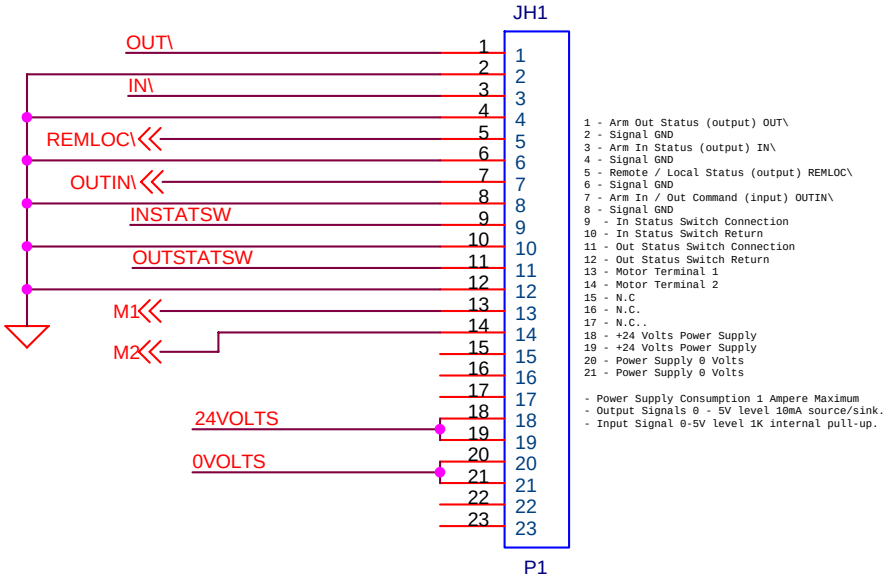
Date: Monday, January 10, 2005 Sheet 3 of 3



European Southern Observatory La Silla

Title	FEROS ADC	Arm Torque Drive Module Schematic 1
Size A	Document Number 0002 Design: J. Alonso	Rev JAT
Date: Monday, January 10, 2005	Sheet 1 of 2	

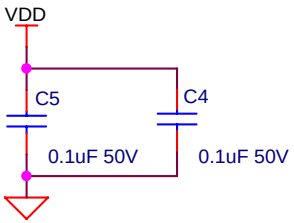


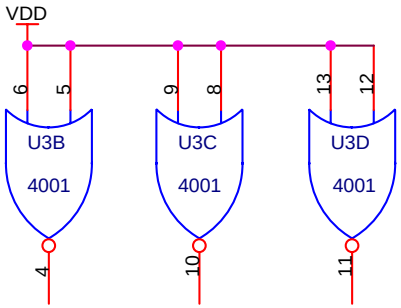


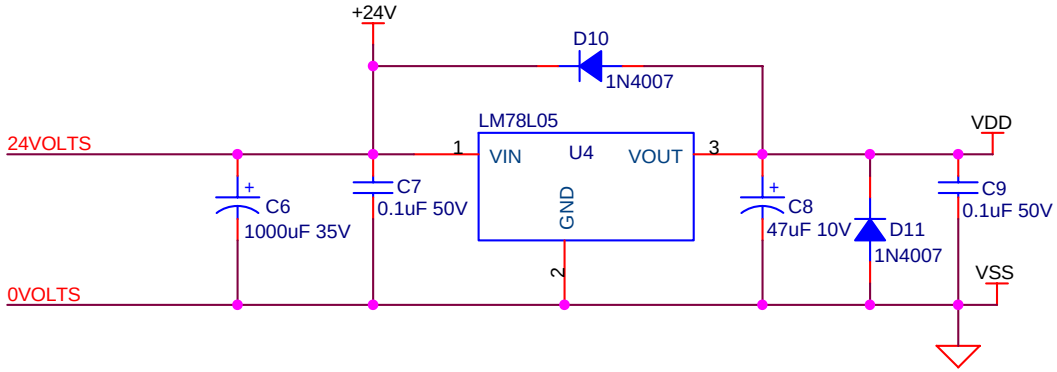
1 - Arm Out Status (output) OUT\
2 - Signal GND
3 - Arm In Status (output) IN\
4 - Signal GND
5 - Remote / Local Status (output) REMLOC\
6 - Signal GND
7 - Arm In / Out Command (input) OUTIN\
8 - Signal GND
9 - In Status Switch Connection
10 - In Status Switch Return
11 - Out Status Switch Connection
12 - Out Status Switch Return
13 - Motor Terminal 1
14 - Motor Terminal 2
15 - N.C
16 - N.C.
17 - N.C..
18 - +24 Volts Power Supply
19 - +24 Volts Power Supply
20 - Power Supply 0 Volts
21 - Power Supply 0 Volts

- Power Supply Consumption 1 Ampere Maximum
- Output Signals 0 - 5V level 10mA source/sink.
- Input Signal 0-5V level 1K internal pull-up.

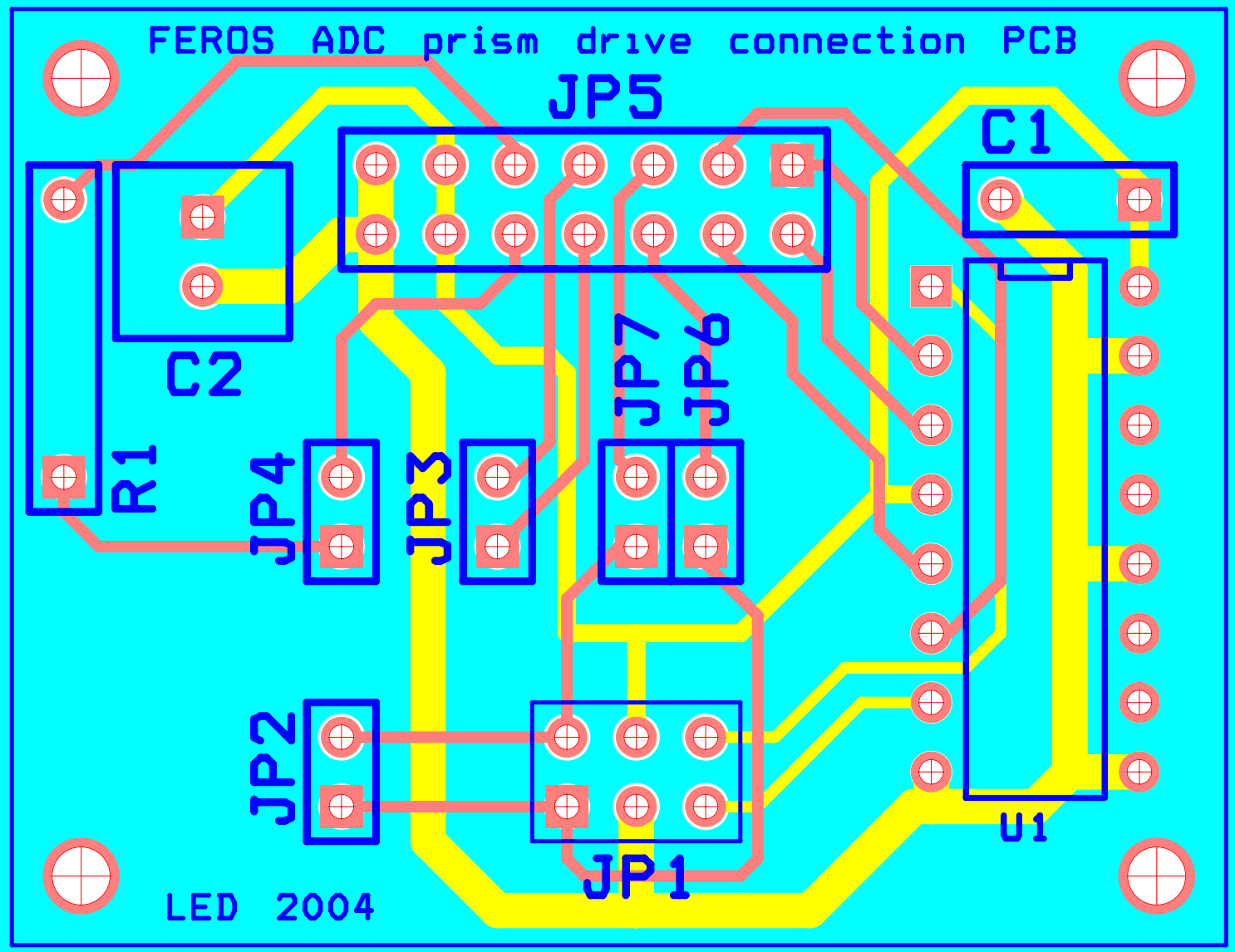
From back plane connector to 9 pin female D sub mounted on VME crate back. From this connector a 20m long cable links the arm mechanism itself at the FEROS adapter.

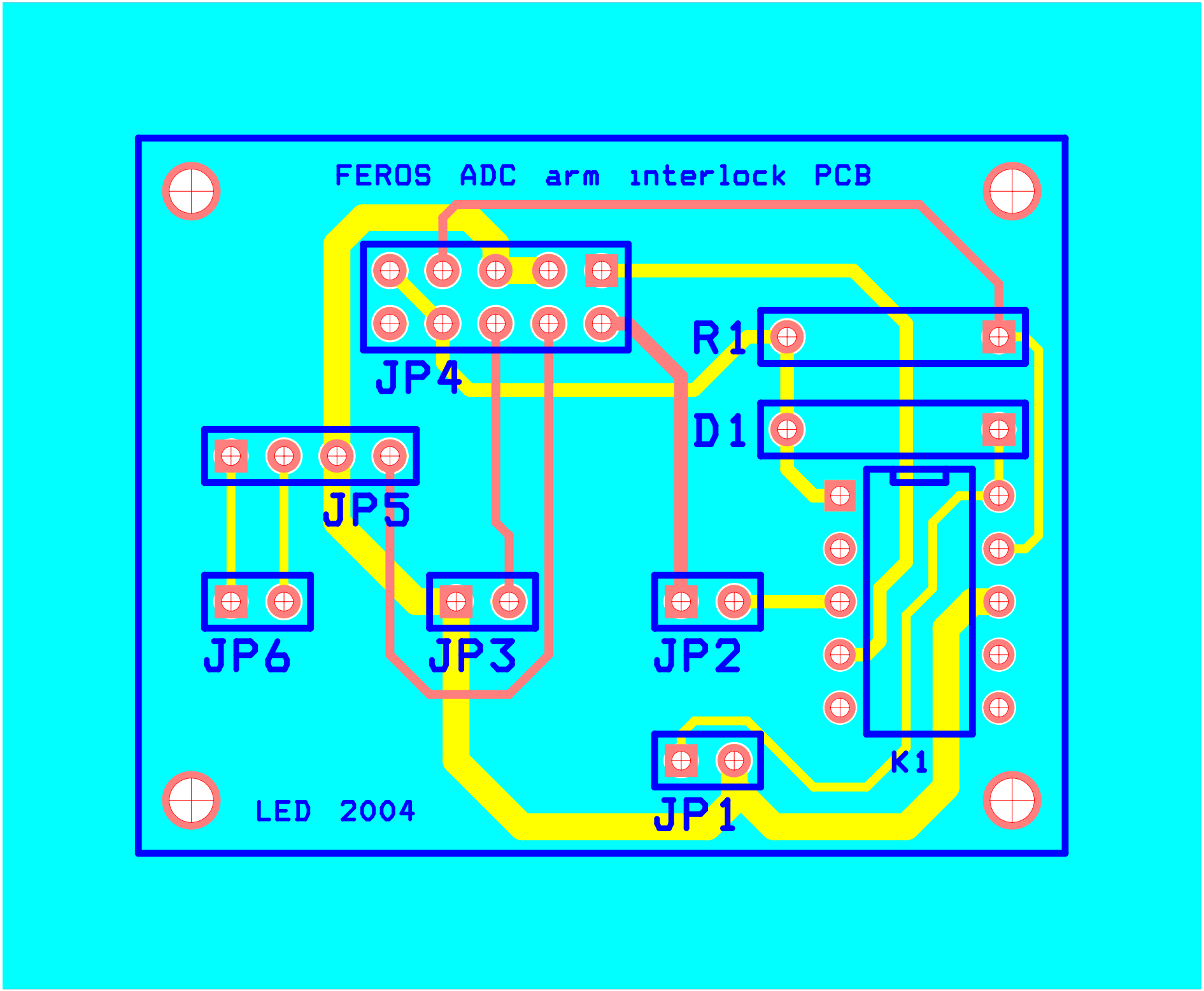


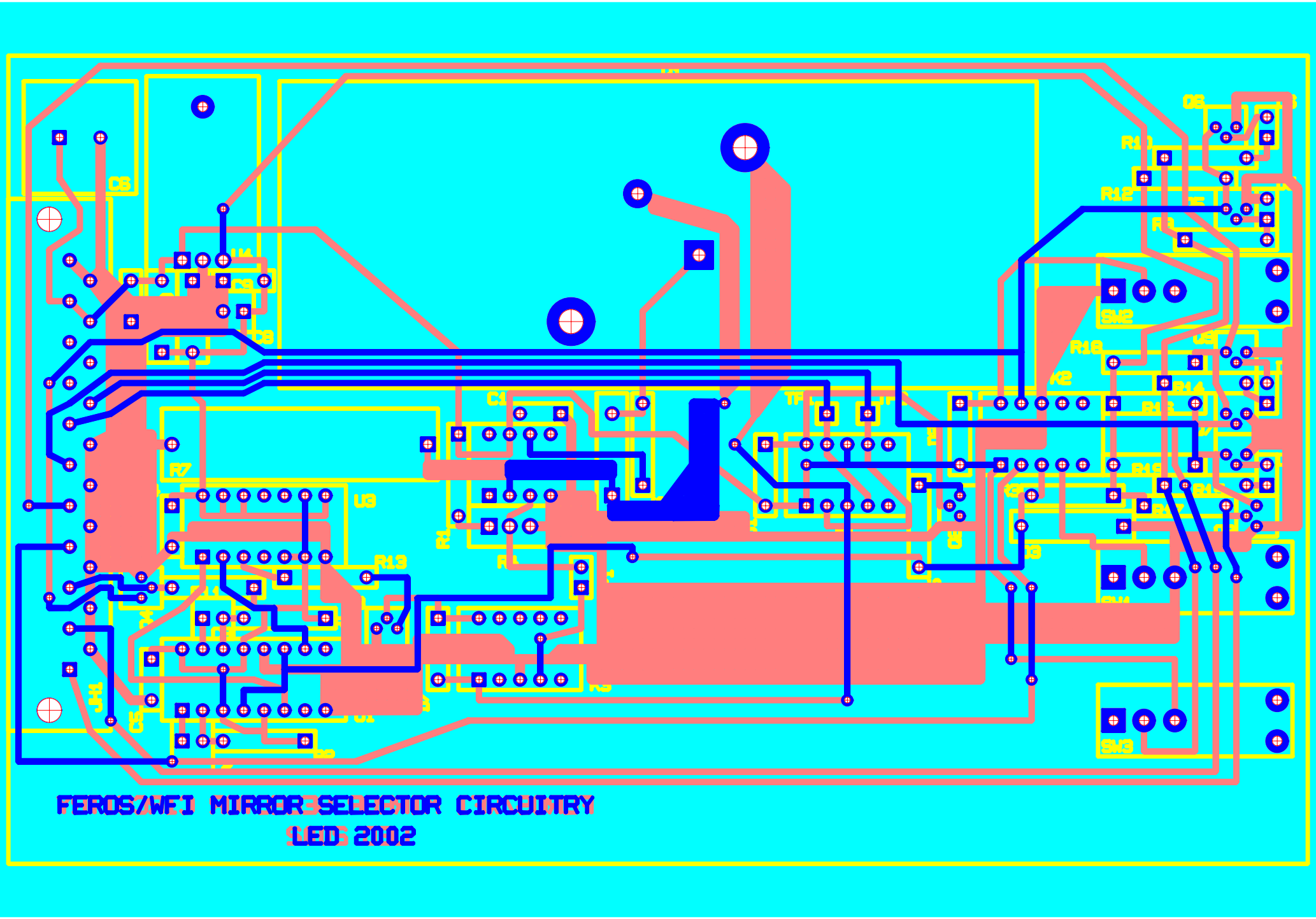




European Southern Observatory La Silla		
Title: FEROS ADC — Arm Torque Drive Module Schematic 2		
Size: A	Document Number: 0001 Design: J. Alonso	Rev: JAT
Date: Monday, January 10, 2005	Sheet 2 of 2	


FEROS ADC prism drive connection PCB
JP5
C1
C2
R1
JP4
JP3
JP7
JP6
JP2
JP1
U1
LED 2004


FEROS ADC arm interlock PCB
JP4
R1
D1
JP5
JP6
JP3
JP2
K1
JP1
LED 2004


FEROS/WFI MIRROR SELECTOR CIRCUITRY
LED 2002