San Diego State Astronomy :

Optical and Infrared Camera Electronics

User's Manual

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GENERAL INFORMATION

The Astronomy Department at San Diego State University has developed a set of versatile camera electronics designed to control a wide variety of optical and infrared imaging arrays. Originally designed for operating CCDs in a slow scanned readout mode, the electronics have been broadened to operate optical CCDs in a fast readout mode of up to one microsec per pixel that efficiently supports many simultaneous readouts. In conjunction with Infrared Laboratories, Inc. of Tucson AZ two new boards have been developed to operate infrared arrays in this fast readout mode that are suitable for operating HgCdTe, InSb and other infrared arrays. The large dynamic range of CCDs and infrared arrays is maintained through the use of low noise techniques and 16-bit A/D converters. These controllers are usable for a variety of both optical and infrared image sensors and have been operated by a number of groups worldwide. There are presently thirty institutions worldwide using these controllers for a wide variety of sensors, including Tek 1024 and 2048 square CCDs, Loral 2048 square and 2048 x 4096 CCDs, and infrared NICMOS III arrays. The operation of CCD and infrared arrays are so similar that the controller electronics will be described for both cases interchangeably except where differences arise, and the generic term 'array' will refer to both CCD and infrared array imaging detectors.

The camera electronics described here is targeted to operate one or more CCD or infrared arrays, each containing one or more readout circuits, at readout times as fast as one microsec per pixel, or one megapixel per second. From one to about 16 readouts can be operated efficiently with one set of camera electronics. The arrays will normally be cooled thermoelectrically or cryogenically to reduce thermal dark current generation. Considerable flexibility has been built into the design to allow operation of a variable number of readouts, as well as operation of a wide variety of both optical and infrared arrays in such modes as staring, drift scan, shuttered and frame transfer. They can be programmed by the user to meet a wide variety of applications, and several programs are supplied to handle simple configurations and to provide the user with a starting point in customizing their systems.

This manual describes in detail the electronics and software elements of the camera system , including hardware and software preparation, system installation, theory of operation, and performance. To improve the utility of this document, its chapters are updated from time to time, and the most recent revision dates of each chapter are written at the bottom of each page. Backup copies are kept in an archival directory as significant changes are made and copies are accessible on the Web at -

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http://mintaka.sdsu.edu/ccdlab

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Files are available via ftp on suicide.sdsu.edu, username anonymous, password 'your e-mail address', directory pub. The revision number of the software and circuit boards that is described are listed at the top of each chapter.

SYSTEM COMPONENTS

Below are listed the major components available, with a short description of each -

Timing board (fiber optics)   Provides digital timing (or sequencing) signals for controlling the array, and communications with the host computer interface board over fiber optic cable.

Timing board (parallel cable)	Provides digital timing (or sequencing) signals for controlling the array, and communications with the host computer interface board over a parallel data cable.
Clock driver board	Translates digital timing signals from the sequencer to controlled voltage levels for driving array clock lines.
CCD video processor board	Amplifies and digitizes video signals from CCD arrays with a correlated double sample circuit.
IR video processor board	Amplifies and digitizes video signals from infrared arrays.
Utility board	Provides miscellaneous system support functions.
SBus interface board	Interfaces the timing board via fiber optics to SBus computers.
VMEbus interface board	Interfaces the timing board via fiber optics to VMEus computers.
Parallel cable interface board	Interfaces the timing board via parallel cable to PCI bus computers.
Controller housing	Consists of a box and backplane.
Power control board	Monitors and gently turns on analog power to the backplane.
Power supply	Linear and robust power supply for all required power.
Host computer and control program	

This section describes the major system components in moderate detail. The electronics board are described first, followed by the mechanical, power supply, dewar and host computer software components. Detailed chapters about the major components follows.

Timing Board (fiber optics)

The heart of the digital timing board is the Motorola DSP56002, a monolithic, integer digital signal processor with a 24-bit data word. It has a 16-bit address space, a fast ALU, extensive on-chip peripheral support and a Reduced Instruction Set Computer (RISC) architecture that executes most instructions in one clock cycle of 40 nanosec. The DSP has separate address spaces for on-chip program and data memory, a synchronous serial interface, boot logic and a simple interface to an external data bus. It functions as a timing generator by writing 24-bit data words from memory to its external bus every 40 nanosec, which are decoded by timing board circuitry to enable various hardware functions. Eight of the 24 bits enable a delay function that halts processor operation for intervals ranging from 100 nanosec to 20.4 microsec in 20 nanosec increments to implement programmable delay timing. The remaining 16 bits are written to the backplane for decoding by the clock driver and video processor boards. Synchronous serial communication provided by the DSP is used to communicate with the utility board and to send digital voltage data to all the DACs in the system.

On power-up or reset the DSP program is read in from a boot ROM, which is a single byte-wide socketed device for easy re-programming external to the controller. Programming is done on a cross compiler supplied by Motorola in native DSP56002 assembly language. The supplied DSP program consists of initialization code to configure the DSP in the desired mode, a command processor, testing and diagnostic routines, routines to read from and write to internal DSP and boot ROM memory, tables containing readout parameters and timing waveforms, and array readout code. Modifications to the code can be done either by re-programming the ROM or by modifying the DSP contents over the fiber optic link from the host computer. Thirty two kilowords of external memory are provided on the board

for no wait state access by the DSP to supplement its internal memory. A fast fiber optic data link processes commands, generates replies and writes image data to and from the host computer, operating at 4 MHz for receiving incoming commands and 50 MHz for transmitting replies and image data, providing a maximum image data rate of 2.5 megapixels per second, or 400 nanosec per pixel. This will support five readouts at the nominal processing time of two microsec per pixel.

Timing Board (parallel cable)

The parallel cable version of the timing board is similar to the fiber optic version, but instead has support for a 16-bit parallel image data link that transmits over commercially available SCSI-3 cable to a host computer interface card for PCI buses designed by Spectral Instruments of Tucson, AZ. The cable will support very high data rates and is presently implemented at 6 Megapixels per second. Command and reply communication is implemented over the DSPs asynchronous serial interface with RS-422 drivers operating over the same parallel data cable.

CCD Video Processing Board

A DC coupled preamplifier with an input offset adjustment is followed by a stage with four switchable gains. A polarity reversing set of amplifiers drives a resettable integrator to implement a dual slope integrator. A fast sample/hold operates at x2 gain to drive the A/D converter and provide a second stage of offset adjustment. Two complete video processors are provided on each board.

Potentiometers are not used anywhere in the controller, as all adjustable voltages are set digitally by the DSP. The analog board is implemented on a six-layer printed circuit card with careful isolation between digital grounds, the noisy analog and digital ground surrounding the clock drivers and logic circuitry, and the quiet analog grounds in the video processor. Ground planes are placed liberally throughout the circuit, and a careful physical placement of components isolates these circuits as well.

Infrared Video Processor Board

A preamplifier operates at x5 gain and contains an input offset circuit to remove the bias of the incoming array signal. A unity gain inverting stage is needed to present the correct polarity to the A/D converter,
followed by a sample/hold switch and a x2 gain stage to allow the S/H switch to operate over the range of
0 to +5 volts and the A/D over the range of 0 to +10 volts.

Clock Driver Board

The clock driver board supplies a total of 24 clocks for driving CCD or IR arrays over a range of +10 to -10 volts. The clock voltages are set by 12-bit DACs with a resolution of about 10 millivolts. Two DAC output voltages are used by each clock driver circuit, with a fast analog switch selecting one of the two DAC voltages for amplification by a fast op amp. Low noise (less than 10 nanovolts per root Hertz) and fast (40 nanosec switching times for a 20 volts swing) circuit techniques are used. Protection against overvoltages that could damage sensor arrays are provided by zener diodes on the voltage reference circuit, by user-configurable blocks of zener diodes on each clock driver output circuit and by analog switches placed at the output of each clock driver circuit that is controlled by the

power monitor of the power control board and by software control from the timing board.

Utility Board

The utility board provides a miscellany of support functions that are not directly involved with readout of the arrays. These include, but are not limited to, exposure timing, array temperature control, and system voltage and temperature monitoring. Based around a DSP56001, it is programmed to support these functions, and can be programmed by the user to support other functions (such as an additional temperature controller, dewar level and ID, shutter status, LED driving for status, switch monitoring for direct system control without a host computer) by programming the use of a number of uncommitted I/O pins. Communication with the timing board can be either through the asynchronous serial port of the timing board's DSP, through a 9-pin RS-232 connector on the utility board, or through two asynchronous serial lines on the backplane.

Power Control Board

The power control board conditions the DC power to protect the array from overvoltage transients. The board passes three analog voltages (high voltage, nominally +32V, and low voltages, nominally +/- 15V) from the power supplies to the backplane in a controlled manner so that short high voltage spikes are not passed on to the analog board. The board plugs into the back of the backplane, is parallel to it, and is six slots wide. It allows the utility board to turn on switches only after the digital supply has stabilized, all DSPs have had their software loaded and the DACs on the analog boards have all been set to their proper values. On command from the utility board the power control board slowly turns on the +/-15V supplies to the system backplane following a linear ramp of about 40 millisecs duration, after which the high voltage is switched on after the utility board signal. A bank of comparators examines the three analog supplies and the ave. digital supply to prevent any of the analog supplies from being switched on to the system backplane if any of them are out of range, and turning off all analog supplies in the event of a power supply failure after the power has been turned on. A power-on reset circuit examines the digital supply and resets the utility board if is is not within range.

VME Interface Board

The VME interface board provides a communication path between the fiber optic link on the timing board and the host computer. It sends commands from the host computer to the timing board following the 24-bit protocol of the serial link, and accepts image data from the timing board and writes them to VME memory using an on-board DMA (Direct Memory Access) controller. Image size is only limited by the 32-bit addressing range of the VMEbus, as entire images can be written to VMEbus memory without intervention from the host processor. This allows non real-time operating system such as UNIX to be used in the host computer, and permits concurrent operation of the host computer even during image readout. Exposures are initiated by the host computer, timed by the utility board, then placed into memory by the interface board, after which the interface board signals to the host processor that the image is available in memory so it can be processed, displayed and stored by the host computer.

The interface board utilizes a DSP56001 processor for housekeeping and DMA address generation. A local buffer memory (32k x 24 bits) stores incoming image data to avoid lost data if the VMEbus is unavailable for short periods. Interrupts can be generated by the interface board, and VMEbus memory can be written to or read from under control of the on-board DSP. The host computer communicates

with the interface board by writing to a single memory mapped address, and is denied direct access to the on-board buffer memory.

SBus Interface Board

The Sbus interface board that communicates over the fiber optic data link between the timing board and a host computer containing SBus slots, which are commonly found on workstations manufactured by Sun Microsystems. The board serves the same function as the VMEbus interface described in earlier, but has the advantage of plugging directly into Sun workstations. This may be of interest to users of Sun workstations since an intermediate VMEbus chassis, memory and communications link are no longer necessary. The interface board contains a DMA (direct memory access) controller with 24-bit word and address counters that writes image and reply data directly to Sun system memory without processor intervention, enabling large images to be read out without burdening the host processor. Lacking a DSP, it does not perform any processing such as de-interlacing or two's complement calculation on the incoming images.

Parallel cable interface board

Spectral Instruments, Inc. of Tucson, AZ.

Backplane and Power Supply

The backplane is simply implemented as a VMEbus J1/P1 backplane whose pins and timing have been completely redefined for this application. 96-pin DIN connectors provide a plentiful number of reliable pins, while the multilayer backplane provides good power distribution and noise suppression. DC power is distributed to the boards through the backplane, using the +5 connection for +5 volts, whereas the +/- 12 volt connection is powered with +/- 15 volt supply that is then down-regulated to +/- 12 volts on each analog board. The high voltage supply, nominally +36 volts, that is required for operating the drain of the CCD on-chip amplifier is brought onto the analog boards separately, to insure low noise operation, and is heavily filtered as well. The boards are all of the standard VME 3U width, that is, roughly four inches wide, but longer than the VME standard by about 50%. The number of VMEbus boards used in a particular installation is determined by the number of analog readout boards that are required; up to 21 connector VME backplanes are available, allowing 19 readouts if a timing and utility board are installed. It is expected in typical installations that the backplane and controller boards will be mounted as close as practical to the array, which is typically on the side of the cryogenic dewar containing the arrays. Robust grounding of the analog boards at the array connector end is required for low noise operation in multiple readout configurations.

The backplane supports full 24-bit data words on both reading and writing. While the analog readout board reads 16 of these bits, it writes 16 bits containing image data and an 8-bit identification tag that is equal to the jumpering of the address selection jumper block. our address lines, A00-A03, are carried on the backplane in order to address the A/D converter when transferring pixel image data to the DSP. This makes the backplane a D24:A04 system. It is not a bus in the normal sense since only the timing board can be a master, and no bus arbitration circuitry is needed. A complement of 21 timing signals generated by the timing board are also carried over the backplane, while only seven of these are currently used by the analog board. These additional signals could be used to operate such devices as a programmable array temperature controller, a shutter, diagnostic hardware, filter wheels and so on. Two interrupt input lines to the DSP are also available on the backplane, which can be used

to implement a hardware timing circuit for overall exposure timing that would be independent of the host computer.

Controller housing

The controller boards are housed in a rugged box that is attached to the side of a cryogenic dewar. It is mounted to the dewar on four standoff spacers, and contains a hole in the baseplate for passing through a 61-pin hermetically sealed circular connector attached to the dewar. Short wires run from this connector to the analog and utility boards, and are totally enclosed by the housing for electrical isolation from potential external sources of interference. The housing contains a six slot VME backplane that accommodates a timing board, a utility board, a clock driver board and and three video processor boards for implementing six readouts. It also has a power control board, and internally mounted fans. Built of aluminum, it has a skeleton to which removable panels are attached with screws for easy access to the controller boards for diagnostic probing. Six panels, all except the bottom plate that attaches to the dewar, can be removed while the controller is operational. The box is sealed from the outside so cooling occurs by circulating air inside the box through the boards, relying on heat conduction to the box. This is done to minimize dust and dirt contamination of the controller boards and to allow the boards keep their internally generated heat when operated in cold climates. The outside housing dimensions are (inches) 13.25 L x 6.75 H x 5.50 W, or (cm) 33.30 L x 16.20 H x 14.0 W.

Cryogenic dewar

The standard dewar implemented by SDSU is a model ND-5 nitrogen dewar purchased from Infrared Labs with additions for mounting the CCD, wiring to it and controlling its temperature. Dewars for infrared arrays should be obtained directly from Infrared Labs. Liquid nitrogen tank capacities are available from 1.5 to 3 liters, with the smaller capacity chosen for operating smaller CCD for less than 24 hour hold times, and the larger capacity chosen for greater than 24 hour hold times with 2048 square CCDs. The dewar has an 8-inch diameter front plate containing an AR-coated quartz window in front of a working volume that is six inches in diameter and three inches deep where the CCD is placed. The CCD is placed in a socket that is attached to a glass epoxy support structure that attaches to a clamp ring on the inside of the dewar wall, allowing focal distance, tilt and rotation adjustments with the aid of an alignment jig. Cooling is transferred from the nitrogen cold plate to the CCD with a cold strap that is trimmed to bring the CCD close to the desired temperature and then a small resistive heater actively brings it to the desired temperature under control by the utility board with a small forward biased diode acting as a temperature sensor. A calibrated temperature sensor gives absolute calibration of the CCD temperature to one degree Celsius.

Host computer and control program

A user interface program is available that executes in the Solaris operating system developed by Sun Microsystems. It operates with either the VMEbus or SBus interface board. In VMEbus systems the CPU chip set is either resident on a VMEbus board that resides in the same backplane as the interface board, or resides in a workstation that connects to a VMEbus backplane over a host adapter or other communications link. The program, named generically "ccdtool", executes on the Sun to acquire images and manage the controller. It is a windowing program written in C with the Xview graphical tools conforming to the OpenLook graphical user interface. It sets up the three controller DSPs with either download or on-board application programs, sets user parameters, issues exposure sequence

commands, allows individual manual commands to be issued and writes images to disk in the FITS format. IRAF is used for image display and analysis, reading the images from disk.

PERFORMANCE

A list of salient performance parameters is presented below to give the user some orientation. The meaning of some of the terms may not be apparent, but hopefully some of this will get cleared up in the remaining sections of this manual.

Form Factors	Timing, clock driver, video processor and utility boards: 3.96 x 9 inches		
	VME interface board	9.2 x 6.30 inches (6U VME size)	
	Power control:	5.5 x 4.75 inches.	
	SBus interface board	5.75 x 3.25 inches.	
Power Dissipation	Timing board: ??? +5 V only		
	Analog board: ??? watts total		
	+5V	??? A	watts
	+15V	A	watts
	-15V	A	watts
	+36V	mA	watts
	Utility board: 2.65 watts total		
	+5V	0.3 A	1.5 watts
	+15V	0.05 A	0.45 watts
	-15V	0.05 A	0.75 watts
	Power control board: 1.65 watts for two video processors and one clock driver		
	+5V	0.08 A	
	+15V	0.04 + 0.004 A per analog board	
	-15V	0.03 + negligible per analog board	

Data path, fiber optic	A fiber optic data cable connects the timing board and VMEbus or SBus interface board. AT&T ST type connectors, 62.5/125 micron multimode Ge-doped silica core fiber cable. The command and reply data words are 32 bits long, plus one start bit, with the most significant bits first, NRZ scrambled. Twenty-four of these bits contain useful data, and eight more are header bits. The image data words are 16 bits long plus one start bit. The host computer interface board transmits at 4 Mbits/sec and receives at 50 Mbits/sec.
Data path, parallel data	A SCSI-3 cable connects the timing board and parallel cable interface board. Image data is sent in parallel form over the cable at a rate 8 Megapixels/sec to a PCI host computer interface board manufactured by Spectral Instruments, Inc. of Tucson, AZ. Command and reply data is sent over an asynchronous serial link over the same cable.
DSP operation	A Motorola DSP56002 Digital Signal Processor is used as the heart of the timing board. It has an instruction time of 40 nanosec, operating from a 50 MHz clock, and the following address spaces:
	512 x 24-bit words program space internal, 8k external

	256 x 24-bit words X: data space internal, 8k external
	256 x 24-bit words Y: data space internal, 16k external

Approx. 80% of the program space, and 60 locations of Y: space, are used up by the current program to control a dual readout array. Approx. 18-20 locations of X: or Y: space are needed for each additional readout.

Clock drivers Twenty four clock drivers are provided on each clock driver board. They each drive over the range of +10 to -10 volts, and provide 40 nanosec rise and fall times, 10% to 90%, 20 volts transition. They can drive high capacitive loads at approx. 60 milliamps typical drive current.

DC bias supplies Twelve programmable DC bias supplies on the CCD video processing board provide the following voltage ranges:

Eight at 5 to +30 volts, intended for the Drain of CCDs.

Four at -10 to +10 volts, intended for driving gates or wells.

They are controlled by 12-bit DACs, and can be set to within about 10 millivolts. Their long term voltage stability is about 5 millivolts, and their noise is less than one microvolt rms if connected to the input of the video processor board.

Six programmable DC bias supplies on the infrared video processing board provide the following voltage ranges:

Six at either 0 to +5 V, 0 to -5V or -5V to +5V, jumper selectable

They can be used for controlling NICMOS arrays (positive voltages) or InSb arrays (negative voltages). They are controlled by 12-bit DACs, and can be set to within about 3 millivolts. Their long term voltage stability is about 2 millivolts, and their noise is less than one microvolt rms if connected to the input of the video processor board.

A/D converter Datel ADS937 analog-to-digital converters are provided that convert to 16 bits straight binary in one microsec. They have a fast (300 microsec) internal sample/hold.

Utility board A DSP56001 provides a miscellany of support functions for the system, including integration timing, array temperature control, shutter control, system power supply and temperature monitoring at a time resolution of one millisec. It also provides uncommitted analog and digital inputs and outputs whose functions can be programmed by the user.

VME interface A DMA (Direct Memory Access) interface communicates between the host computer and the timing board over the fiber optic data link. Once initialized by the host computer it writes entire multi-megabyte images directly to VMEbus memory, relieving the host processor of this real-time responsibility. It has 32k x 24 bits of internal buffer memory, VMEbus interrupt capability and 32-bit data transfer capability, and contains a DSP56001 processor. Its transfer over the VMEbus has been measured to be 7 Mbytes/sec.