MicroSys

User's Manual

CPU87 Rev. 4

2nd edition

Declaration of Conformity

We, Manufacturer
MicroSys Electronics GmbH
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Germany

declare that the product

CPU87

is in conformity with:

EN 50081-1 Generic emission standard
EN 50082-1 Generic immunity standard

in accordance with **89/336 EEC-EMC** Directive.

We also declare the conformity of the above mentioned product with the actual required safety standards in accordance with Low Voltage Directive **73/23 EEC**.

Date:

Signature:

Position: General Manager

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1. Introduction

1.1 Short Description

The **Double Euro** sized board **CPU87** is based on the Motorola PowerPC **MPC8270**.

It features a **64 bit** wide data bus for the **32 (64/128) Mbytes SDRAM** area and the **8 Mbytes Flash** memory bank. Additionally, it offers two **8 bit** wide **32 pin JEDEC** sockets for a boot **ROM** and a **DiskOnChip®** device. An additional **16 bit** wide **SRAM** area with battery backup is shareable with any other VMEbus master.

The I^2C-Interface of the MPC8270 controls a **2KBytes EEPROM,** a **RTC** with battery backup and a **System Monitor** for supply voltage supervision.

The **CPM Module** of the MPC8270 handles **two 10/100Mbit Ethernet** ports, **three RS232** communication ports and **two** special **RS422** and **RS485** interfaces .

The **local bus** of the MPC8270 is accessible via a 64 pin extension connector. A PMC slot is connected to the PCI interface, replacing the local bus lines.

The **VMEbus interface** contains a single level arbiter, a requester with a four level ROR option and a **7 level interrupt handler**. The short I/O decoded **mailbox** with interrupt capability allow for process synchronization.

For background debug purposes the **JTAG/COP** interface of the MPC8270 is accessible via a 16 pin standard wrap connector.

The complete board is implemented in **CMOS technology**, which allows for a power consumption as low as: **5V / 9W @ 450 MHz** CPU speed.

The 5 volt board supply voltage is protected by a transient suppresser diode against over voltage or wrong polarity.

The CPU87 conforms to the VMEbus specification ANSI/IEEE STD1014-1987, IEC 821 & 297.

1.2 Specifications

The power requirements for the CPU87 board are shown in the following table.

Power Requirements:

+5V, +5%/-2.5%,	(t.b.d.) (typ. @450 MHz)
+12V, +5%/-2.5%	for PMC slot only
-12V, +5%/-2.5%	for PMC slot only

Environmental Requirements:

Operating Temperature	0 ° C to +70 ° C -40°C to +85°C optional
Relative Humidity	0 to 95 % (non-condensing)
Storage Temperature	-40 ° C to + 85 ° C

1.3 Related Documentation

The following manuals are applicable to the CPU87:

- MPC8270 Power QUICC-II Microprocessor User's Manual
- HY57V651620B-TC7 4x1Mx16 SDRAM Data Sheet
  (Note: DRAM may actually vary, depending on the specific version and availability)
- I28F160C3B Intel Boot Block Flash Memory Data Sheet
  (Note: Flash may actually vary, depending on the specific version and availability)
- LM81 System Hardware Monitor Data Sheet
- PCF8563 Real-Time-Clock User's Manual
- X24C164 EEPROM Data Sheet
- DiskOnChip® 2000 User's Manual
- VMEbus Specification Manual ANSI/IEEE STD1014-1987

2. Delivery

2.1 Items shipped with this unit

- User's Manual CPU87 Hardware
- MicroSys shipping carton

ATTENTION: STATIC DISCHARGE CAN DESTROY UNIT

2.2 Hints for unpacking, handling and storing

- Avoid touching areas of integrated circuitry.
- Unit should only be placed on a static-free conductive surface
- Unit must only be transported using anti-static bags or MicroSys shipping carton
- Packing should be saved if unit needs to be reshipped or returned
- When the unit needs to be stored, it should be placed in a moist free, dust free environment. The storage temperatures and humidity specifications are shown in chapter 1

3. Installation

3.1 Items required for CPU87 installation

For installation of the CPU87, the following items are required.

- Card cage or housing
- VMEbus motherboard
- Adequate rated power supply

3.2 Points to be observed

Before the unit is inserted into the card cage, the following points should be observed.

- Unit requires +5V (+ 5 %, - 2,5 %).
- Unit requires +12V (+ 5 %, - 2,5 %) for PMC extension.
- Unit requires -12V (+ 5 %, - 2,5 %) for PMC extension.
- Be sure voltage is of correct polarity.
- Check default jumper or switch setting.

The card cage must be well ventilated.

The operating temperature must never exceed its specified range.

GUARANTEE IS VOID IF UNIT IS OPERATED

OUT OF IT'S SPECIFICATIONS!

4. Board Overview

4.1 Features CPU87

Board Format:	double euro card format
Main Processor:	MPC8270 with PowerPC 603e Core 64 Bit 603e-bus 32 Bit local bus 16 Kbytes instruction cache 16 Kbytes data cache up to 450 MHz CPU core clock rate CPM interface with four SCCs & one SMC
Dynamic RAM:	four SDRAM devices 32 Mbytes capacity (optional 64MB or 128MB) 64 bit data bus width
Flash Memory:	8 Mbytes capacity 64 bit data bus width single 3.3 volt programmable devices
Boot ROM Area:	one 32 pin socket according to JEDEC standard max. 1 Mbytes capacity (512Kbytes for FLASH types) device type selection by soldering links 8 bit data bus width 5 volt supply ROM, PROM, EPROM, EEPROM, FLASH support
Static DPRAM:	64 Kbytes (max. 1 Mbytes) SRAM capacity 16 bit data bus width data backup with onboard supply accessible by other VMEbus masters
EEPROM:	I^2C serial access device 2KBytes capacity
DiskOnChip®:	MD-2800-D08 5V device (optional) 32 pin socket with standard JEDEC pin out
FD-Interface:	FDC37C78 Floppy Disk Controller (optional)
Real Time Clock:	I^2C serial access device PCF8563 with time & date function backup function with onboard supply
Serial Interfaces:	2 SMCs with RS232 interface 2 SCCs with configurable buffers via I/O modules
System Control:	I^2C serial access device LM81 hardware monitor for temperature and voltage control
Data Backup:	short time backup via service free gold cap extended backup via 260mAh lithium cell (CR2430) external backup via VMEbus standby line

features CPU87 continued:

Network Capabilities:	two IEEE compliant Fast Ethernet PHY Transceivers full-duplex operation for 100BASE-TX and 10BASE-T
Front Panel LEDs:	four network status LEDs four user programmable LEDs
Front Panel Keys:	ABORT key with level 1 interrupt capability RESET key for complete hardware reset
Watchdog:	hardware watchdog timer with system reset programmable time out rate via external parts
Debug Features:	16 pin JTAG/COP Interface
Interrupt Handler:	7 level onboard interrupt handler 7 level VMEbus interrupt handler software programmable interrupt mask
System Controller:	full VMEbus slot 1 functions, single level arbiter single jumper function enable
VMEbus Interface:	according to ANSI/IEEE STD1014-1987
VMEbus Master:	DTB A16/A24/A32 -D8/D16/D32 VMEbus address modifier support standard, extended and short I/O addressing dynamic bus sizing feature
VMEbus Slave:	DTB A24/A32 -D8/D16 programmable VMEbus access base address programmable VMEbus access window size DTB A16 -D8/D16 programmable VMEbus access base address
VMEbus Mailbox:	short I/O decoded with interrupt capability
VMEbus Arbiter:	single level arbiter on level 3
VMEbus Requester:	single level 2:1 pass requester release when done or 4 level release on request modes
Mezzanine Slot:	PMC form factor Local Bus Interface for MPC8260 Processor type 3.3V PCI Interface for MPC8250 and MPC8270 Processor type

5. Address Map CPU87

5.1 The 603e-Bus Address Map

Type	Base	End	Select	Bus	Size	
SDRAM Bank	$0000 0000	$01FF FFFF	CS2	603	64Bit	
Dual Ported SRAM Area	$4000 0000	$4001 FFFF	CS3	603	16Bit	
DiskOnChip® Socket	$F400 0000		CS4	603	8Bit	
FDC37C78 Controller Std.Access	$F100 0000	$F100 007F	CS5	603	8Bit	
FDC37C78 Controller DMA Access	$F100 0080	$F100 00FF	CS5	603	8Bit	
VMEbus Ext.Address Compare Register	$F200 0000	$F200 0000	CS6	603	8Bit	
VMEbus Std.Address Compare Register	$F200 0001	$F200 0001	CS6	603	8Bit	
VMEbus Mb.Address Compare Register	$F200 0002	$F200 0002	CS6	603	8Bit	
Board Control Register	$F200 0003	$F200 0003	CS6	603	8Bit	
Board Status Register	$F200 0004	$F200 0004	CS6	603	8Bit	
Watchdog Retrigger Port	$F200 0005	$F200 0005	CS6	603	8Bit	
Clear Mailbox IRQ Port	$F200 0006	$F200 0006	CS6	603	8Bit	
Revision Register	$F200 0007	$F200 0007	CS6	603	8Bit	
VMEbus IRQ Mask Register	$F200 0080	$F200 0080	CS6	603	8Bit	
VMEbus IRQ Status Register	$F200 0081	$F200 0081	CS6	603	8Bit	
Local IRQ Mask Register	$F200 0082	$F200 0082	CS6	603	8Bit	
Local IRQ Status Register	$F200 0083	$F200 0083	CS6	603	8Bit	
PMC IRQ Status Register	$F200 0084	$F200 0084	CS6	603	8Bit	
Power QUICC-II Internal Memory	$F000 0000		---	603	32Bit	
VMEbus Extended Access Range I	$8000 0000	$80FF FFFF	CS7	603	32Bit	
VMEbus Extended Access Range II	not initialized	not initialized	CS11	603	32Bit	
VMEbus Standard Access Range	$FE00 0000	$FEFF FFFF	CS8	603	16Bit	
VMEbus Short I/O Access Range	$FD00 0000	$FD07 FFFF	CS9	603	16Bit	
VMEbus Int.Ackn. Access Range	$FD08 0000	$FD0F FFFF	CS9	603	16Bit	
Flash Memory Bank	$FF00 0000	$FF7F FFFF	CS1	603	64Bit	[1]
Boot ROM Socket	$FFF0 0000	$FFFF FFFF	CS0	603	8Bit	[1]

Boot ROM Socket	$FF00 0000	$FF0F FFFF	CS1	603	8Bit	[2]
Flash Memory Bank	$FF80 0000	$FFFF FFFF	CS0	603	64Bit	[2]

[1]) BTMD Jumpers set to 1-2 and 3-4

[2]) BTMD Jumpers set to 1-3 and 2-4

Note!
The address map shown above reflects the standard MicroSys initialization. Due to the flexibility of the MPC8270 memory controller, nearly any customized address map may be defined.

5.2 The I²C-Bus Address Map

Type	write	read	
24C164 EEPROM	$B0..$BE	$B1..$BF	I²C-Bus
LM81 System Hardware Monitor	$58	$59	I²C-Bus
PCF8563 Real Time Clock	$A2	$A3	I²C-Bus

6. Functional Description

6.1 The PowerQUICC II Processor

The CPU87 uses the MPC8270 Power QUICC-II RISC microprocessor from Motorola. It can be configured for different CPU core and bus speed versions. The MPC8270 contains a 603e compatible core with 16 Kbytes data cache and 16 Kbytes instruction cache. It uses a 3,3 volt bus supply and a 1,8 volts core supply voltage. The processor works with CPU clock rates up to 450 MHz and the according system clock rate varies from 50 to 100 MHz. The desired clock configuration can be adjusted via the soldering link area MDCK according to the following table.

MDCK			**MPC8270 - 100/300/450 MHz**		
1-2	**3-4**	**5-6**	**System-Clock**	**CPM-Clock**	**CPU-Clock**
X	X	X	33MHz	99MHz	132MHz
X	X	---	33MHz	99MHz	165MHz
X	---	X	33MHz	132MHz	132MHz
X	**---**	**---**	**33MHz**	**132MHz**	**165MHz**
---	**X**	**X**	**100MHz**	**128MHz**	**450 MHz [1])**
---	*X*	---	*66MHz*	*132MHz*	*198MHz*
---	---	*X*	*66MHz*	*165MHz*	*165MHz*
---	---	---	*66MHz*	*165MHz*	*198MHz*

[1]) Resulting clock rates with 50 MHz Oscillator (OSC1)

(x = link installed / --- link not installed)

The MPC8270 of the CPU87 is configured for the **MPC8270-stand-alone-mode**, i.e. **not** for the 603e bus mode. If the link **RCFG** is not installed, the power up configuration is set to the internal default mode. Otherwise the reset configuration word is taken out of the memory device connected to the **CS0** line of the MPC8270. The 64 bit flash area or the 8 bit ROM socket can be configured as boot memory by jumper BTMD.

BTMD	**Function**	**RCFG**
Pin 1-2	CS0 connected to 8 bit socket	closed
Pin 3-4	CS1 connected to 64 bit Flash	---
Pin 1-3	CS0 connected to 64 bit Flash	open or closed
Pin 2-4	CS1 connected to 8 bit socket	---

Because of a special BCTL0/BCTL1 buffer control, the configuration word **must** be always read from the boot device. Only during the use of the BDM port, the internal configuration word can be used.

6.1.1 The Debug Port

The **JTAG/COP** interface of the CPU87 can be used via the 16 pin standard wrap connector JTAG according to following table.

JTAG	Signal		Signal	JTAG
Pin 1	TDO		GND	Pin 2
Pin 3	TDI		TRST#	Pin 4
Pin 5	QREQ#		2K2 pullup	Pin 6
Pin 7	TCK		n.c.	Pin 8
Pin 9	TMS		n.c.	Pin 10
Pin 11	SRST#		GND	Pin 12
Pin 13	HRST#		n.c.	Pin 14
Pin 15	CKSTPO#		GND	Pin 16

6.1.2 The Processor Pin Configuration

The MPC8270 offers a wide variety of pin functional swapping. The CPU87 uses the multi functional processor pins according to following table.

Functions	BGA	Signal	Status	Description
DP0/RSRV/EXT_BR2	B22	EXTBR2#	not used	pullup
DP1/**IRQ1**/EXT_BG2	A22	ABOIR#	interrupt	
DP2/**IRQ2**/TLBISYNC/EXT_DBG2	E21	SCMIR#	interrupt	
DP3/ IRQ3/CHKSTP_OUT/EXT_BR3	D21	CKSTPO#	not used	pullup
DP4/ **IRQ4**/CORE_SRST/EXT_BG3	C21	RTCIR#	interrupt	
DP5/ **IRQ5**/TBEN/EXT_DBG3	B21	CNAIR#	interrupt	
DP6/ **IRQ6**/CSE0	A21	CNBIR#	interrupt	
DP7/ **IRQ7**/CSE1	E20	CNCIR#	interrupt	
IRQ0/NMI_OUT	T1	NMIO#	interrupt	pullup
IRQ1/GBL	W1	GBL#	not used	pullup
IRQ2/BADDR29/CI	U2	BADDR29	not used	pullup
IRQ3/BADDR30/WT	U3	ATMIR#	interrupt	
IRQ4/L2_HIT	Y4	L2HIT#	not used	pullup
IRQ5/BADDR31/CPU_BG	U4	BADDR31	not used	pullup
IRQ7/INT_OUT/APE	D1	INTO#	not used	pullup
IRQ2/ABB	E2	ABB#	not used	pullup
IRQ3/DBB	V2	DBB#	not used	pullup
DBG_DIS/BCTL1/CS10	F29	BCTL1#	not used	ispLSI
AP0/**CS11**	G28	CS11#	select	extension module
PBS0/**PSDDQM0**/**PWE0**	C25	PSDQM0#	control	SDRAM/FLASH
PBS1/**PSDDQM1**/**PWE1**	E24	PSDQM1#	control	SDRAM/FLASH
PBS2/**PSDDQM2**/**PWE2**	D24	PSDQM2#	control	SDRAM/FLASH
PBS3/**PSDDQM3**/**PWE3**	C24	PSDQM3#	control	SDRAM/FLASH
PBS4/**PSDDQM4**/**PWE4**	B26	PSDQM4#	control	SDRAM/FLASH
PBS5/**PSDDQM5**/**PWE5**	A26	PSDQM5#	control	SDRAM/FLASH
PBS6/**PSDDQM6**/**PWE6**	B25	PSDQM6#	control	SDRAM/FLASH
PBS7/**PSDDQM7**/**PWE7**	A25	PSDQM7#	control	SDRAM/FLASH
PGLP0/**PSDA10**	E23	PGPL0	control	SDRAM/FLASH
PGLP1/**PSDWE**	B24	PGPL1	control	SDRAM/FLASH
PGLP2/**PSDRAS**/POE	A24	PGPL2	control	SDRAM/FLASH
PGLP3/**PSDCAS**	B23	PGPL3	control	SDRAM/FLASH
PGLP4/PPBS/PUPWAIT/**PGTA**	A23	PGPL4	control	ispLSI
PGLP5/PSDAMUX	D22	---	not used	not connected
MODCK1/AP1/TC0/BNKSL0	W2	MDCK1	config./ctl.	clock
MODCK2/AP2/TC0/**BNKSL1**	W3	MDCK2	config./ctl.	clock & SDRAM
MODCK3/AP3/TC0/**BNKSL2**	W4	MDCK3	config./ctl.	clock & SDRAM

(used functionality is shown in bold characters)

Functions	BGA	Signal	Status	Description
LD(0:31)/**AD(0:31)**	.....	LD(0.31)	used	local bus/PMC/PCI
LDP0/C0/CBE0	L28	---	used	local bus/PMC/PCI
LDP1/C1/CBE1	N28	---	used	local bus/PMC/PCI
LDP2/C2/CBE2	T28	---	used	local bus/PMC/PCI
LDP3/C3/CBE3	W28	---	used	local bus/PMC/PCI
PAR/LA14	N27	---	used	local bus/PMC/PCI
xxx/**LA(15:31)**	.....	LA(15:31)	used	local bus/PMC/PCI
LGPL0/**LSDA10**	D27	LGPL0	control	local bus
LGPL1/**LSDWE**	C28	LGPL1	control	local bus
LGPL2/**LSDRAS**	E26	LGPL2	control	local bus
LGPL3/**LSDCAS**	D25	LGPL3	control	local bus
LGPL4/LPBS/LUPWAIT/**LGTA**	C26	LGPL4	control	local bus
LBS0/**LSDQM0**/LWE0	H28	LSDQM0	control	local bus
LBS1/**LSDQM1**/LWE1	H27	LSDQM1	control	local bus
LBS2/**LSDQM2**/LWE2	H26	LSDQM2	control	local bus
LBS3/**LSDQM3**/LWE3	G29	LSDQM3	control	local bus

(used functionality is shown in bold characters)

Functions	BGA	Signal	Status	Description
PA0/.../...	AC29	MII1_MDINT	input	LAN Channel 1
PA1/.../...	AC25	MII2_MDINT	input	LAN Channel 2
PA3/.../...	AG29	MII1_PWRDN	output	LAN Channel 1
PA4/.../...	AF23	MII2_PWRDN	output	LAN Channel 2
PA5/.../...	AH23	MII1_PAUSE	output	LAN Channel 1
PA6/.../...	AE24	MII2_PAUSE	output	LAN Channel 2
PA8/.../**SMRXD2**	AF23	SMC2_RXD	input	RS232 on ST4
PA9/.../**SMTXD2**	AH23	SMC2_TXD	output	RS232 on ST4
PA10/.../...	AE22	MII1_TXSL0	output	LAN Channel 1
PA11/.../...	AH22	MII1_TXSL1	output	LAN Channel 1
PA12/.../...	AJ21	MII2_TXSL0	output	LAN Channel 2
PA13/.../...	AH20	MII2_TXSL1	output	LAN Channel 2
PA14/.../**FCC1_RXD3**	AG19	MII1_RXD3	input	LAN Channel 1
PA15/.../**FCC1_RXD2**	AF18	MII1_RXD2	input	LAN Channel 1
PA16/.../**FCC1_RXD1**	AF17	MII1_RXD1	input	LAN Channel 1
PA17/.../**FCC1_RXD0**	AE16	MII1_RXD0	input	LAN Channel 1
PA18/.../**FCC1_TXD0**	AJ16	MII1_TXD0	output	LAN Channel 1
PA19/.../**FCC1_TXD1**	AG15	MII1_TXD1	output	LAN Channel 1
PA20/.../**FCC1_TXD2**	AJ13	MII1_TXD2	output	LAN Channel 1
PA21/.../**FCC1_TXD3**	AE13	MII1_TXD3	output	LAN Channel 1
PA22/.../...	AF12	MII1_MDC	output	LAN Channel 1
PA23/.../...	AG11	MII1_MDIO	output	LAN Channel 1
PA24/.../...	AH9	MII2_MDC	output	LAN Channel 2
PA25/.../...	AJ8	MII2_MDIO	output	LAN Channel 2
PA26/.../**FCC1_RXER**	AH7	MII1_RXER	input	LAN Channel 1
PA27/.../**FCC1_RXDV**	AF7	MII1_RXDV	input	LAN Channel 1
PA28/.../**FCC1_TXEN**	AD5	MII1_TXEN	output	LAN Channel 1
PA29/.../**FCC1_TXER**	AF1	MII1_TXER	output	LAN Channel 1
PA30/.../**FCC1_CRS**	AD3	MII1_CRS	input	LAN Channel 1
PA31/.../**FCC1_COL**	AB5	MII1_COL	input	LAN Channel 1

Functions	BGA	Signal	Status	Description
PB18/.../**FCC2_RXD3**	AE14	MII2_RXD3	input	LAN Channel 2
PB19/.../**FCC2_RXD2**	AF13	MII2_RXD2	input	LAN Channel 2
PB20/.../**FCC2_RXD1**	AG12	MII2_RXD1	input	LAN Channel 2
PB21/.../**FCC2_RXD0**	AH11	MII2_RXD0	input	LAN Channel 2
PB22/.../**FCC2_TXD0**	AH16	MII2_TXD0	output	LAN Channel 2
PB23/.../**FCC2_TXD1**	AE15	MII2_TXD1	output	LAN Channel 2
PB24/.../**FCC2_TXD2**	AJ9	MII2_TXD2	output	LAN Channel 2
PB25/.../**FCC2_TXD3**	AE9	MII2_TXD3	output	LAN Channel 2
PB26/.../**FCC2_CRS**	AJ7	MII2_CRS	input	LAN Channel 2
PB27/.../**FCC2_COL**	AH6	MII2_COL	input	LAN Channel 2
PB28/.../**FCC2_RXER**	AE3	MII2_RXER	input	LAN Channel 2
PB29/.../**FCC2_TXEN**	AE2	MII2_TXEN	output	LAN Channel 2
PB30/.../**FCC2_RXDV**	AC5	MII2_RXDV	input	LAN Channel 2
PB31/.../**FCC2_TXER**	AC4	MII2_TXER	output	LAN Channel 2

(used functionality is shown in bold characters)

Functions	BGA	Signal	Status	Description
PC0/.../**DREQ1**/...	AB26	DRQFD#	input	FDC37C78
PC10/.../**CD3**/..	AF20	SCC3_DCD#	input	SCC3
PC11/.../**CTS3**/..	AE19	SCC3_CTS#	input	SCC3
PC17/.../**CLK15/BRGO8**/...	AJ15	EXBRG	input	ext.baud rate
PC18/.../**CLK14** /...	AH14	MII2_TXCLK	input	LAN Channel 2
PC19/.../**CLK13/BRGO7**/...	AG13	MII2_RXCLK	input	LAN Channel 2
PC20/.../**CLK12** /...	AH12	MII1_TXCLK	input	LAN Channel 1
PC21/.../**CLK11/BRGO6**/...	AJ11	MII1_RXCLK	input	LAN Channel 1
PC22/.../**DONE1** /...	AG10	DNFD#	output	FDC37C78
PC23/.../**DACK1**/...	AE10	DACFD#	output	FDC37C78
PC24/.../**CLK8**/..	AF9	SCC3_RXC	input	SCC3
PC25/.../**CLK7**/..	AE8	SCC3_TXC	input	SCC3
PC26/.../**CLK6**/..	AJ6	SCC4_RXC	input	SCC4
PC27/.../**CLK5**/..	AG2	SCC4_TXC	input	SCC4
PC28/.../**CTS2**/..	AF3	SCC2_CTS#	input	RS232 on ST3-C
PC29/.../**CTS1**/..	AF2	SCC1_CTS#	input	RS232 on ST3-D

(used functionality is shown in bold characters)

Functions	BGA	Signal	Status	Description
PD8/.../**SMRXD1**/...	AG25	SMC1_RXD	input	RS232 on ST4
PD9/.../**SMTXD1**/...	AH26	SMC1_TXD	output	RS232 on ST4
PD14/.../**I2CSCL**/..	AE20	SCL	I/O	I^2C-Bus
PD15/.../**I2CSDA**/..	AJ20	SDA	I/O	I^2C-Bus
PD16/.../**SPIMISO**/..	AG18	SPI_MISO	input	SPI-Bus
PD17/.../**SPIMOSI**/..	AG17	SPI_MOSI	output	SPI-Bus
PD18/.../**SPICLK**/..	AF16	SPI_CLK	output	SPI-Bus
PD19/.../**SPISEL**/..	AH15	SPI_SEL#	output	SPI-Bus
PD20/.../**RTS4**/..	AJ14	SCC4_RTS#	output	SCC4
PD21/.../**TXD4**/..	AH13	SCC4_TXD	output	SCC4
PD22/.../**RXD4**/..	AJ12	SCC4_RXD	input	SCC4
PD23/.../**RTS3**/..	AE12	SCC3_RTS#	output	SCC3
PD24/.../**TXD3**/..	AF10	SCC3_TXD	output	SCC3
PD25/.../**RXD3**/..	AG9	SCC3_RXD	input	SCC3
PD26/.../**RTS2**/..	AH8	SCC2_RTS#	output	RS232 on ST3-C
PD27/.../**TXD2**/..	AG7	SCC2_TXD	output	RS232 on ST3-C
PD28/.../**RXD2**/..	AE4	SCC2_RXD	input	RS232 on ST3-C
PD29/.../**RTS1**/..	AG1	SCC1_RTS#	output	RS232 on ST3-D
PD30/.../**TXD1**/...	AD4	SCC1_TXD	output	RS232 on ST3-D
PD31/.../**RXD1**/..	AD2	SCC1_RXD	input	RS232 on ST3-D

(used functionality is shown in bold characters)

6.2 Memory

6.2.1 The SDRAM Area

The CPU87 is fitted out with four synchronous dynamic ram devices which allows for a total capacity of 32 MBytes, 64 MBytes or 128 MBytes depending on the used chip sizes. The RAM bank is directly controlled by the **CS2** select line of the MPC8270. The DRAM data port is **64 bits** wide and no parity check is performed. The SDRAM contains 4 banks and supports auto refresh and self refresh with **4096** cycles during **64ms**. The pins of the SDRAM device are controlled by the MPC8270 according to following table.

SDRAM	MPC8270	Description
A0-A9	A28-A19	603bus address
A10/AP	PGPL0	address/auto precharge
A11	A18	603bus address
n.c./A12	A17	603bus address
BA0	BNKSL2	bank address 0
BA1	BNKSL1	bank address 1
CLK	CLKIN	system clock
CLKE	n.c.	clock enable set to high
UDQM	PSDQMx	upper data I/O mask
LDQM	PSDQMy	lower data I/O mask
RAS	PGPL2	row address strobe
CAS	PGPL3	column address strobe
CS	CS2	chip select
WE	PGPL1	write enable

For detailed information about the SDRAM chip specification, please refer to the according SDRAM data sheet.

6.2.2 The Boot Socket

The boot socket of the CPU87 is able to handle a 32 pin, JEDEC compatible, 600mil, standard **5V** 8 bit wide **ROM**, **PROM**, **EPROM** or **Flash** device. The device type selection is made by the 3 soldering links BA, BB and BC. The socket can be controlled via the **CS0** or the **CS1** line on the 603 bus of the MPC8270. The selection between both CS-lines is performed via jumper BTMD. If the links are set to BTMD(1-2) and BTMD(3-4), the **8 bit** socket is connected to the CS0 line, while the 64 bit wide flash memory is controlled via the CS1 line of the MPC8270. The data lanes are swapped according to the necessary endian conversion. The pins of the socket are controlled by the MPC8270 according to following table.

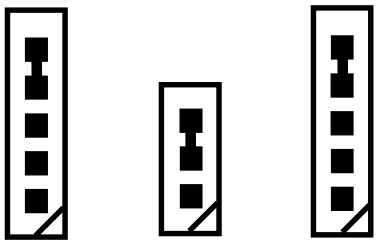
Boot Socket	MPC8270	Description
PA0-PA16	A31-A15	603bus address
PA17/VCC	A14/VCC	via link BB
PA18/WE	A13/PSDQM0	via link BC
PA19/VPP	A12/A13/VDD	via link BA
CE	CS0/CS1	via link BTMD
OE	PGPL2	603bus control line
PD7-PD0	D7-D0	endian swapped data lanes

6.2.2.1 Type Selection for Boot-ROM Socket

controlled pin:		**pin:1**	**pin:30**	**pin:31**
by link:		**BA**	**BB**	**BC**
ROM:	512Kbit	---	1-2	---
	1Mbit	1-2	---	1-2
	2Mbit	1-2	2-3	1-2
	4Mbit	1-2	2-3	2-3
	8Mbit	2-3	2-3	2-3
EEPROM:	1Mbit	---	---	4-5
Flash:	1Mbit	---	---	4-5
	4Mbit	**4-5**	**2-3**	**4-5**

(--- = don't care)

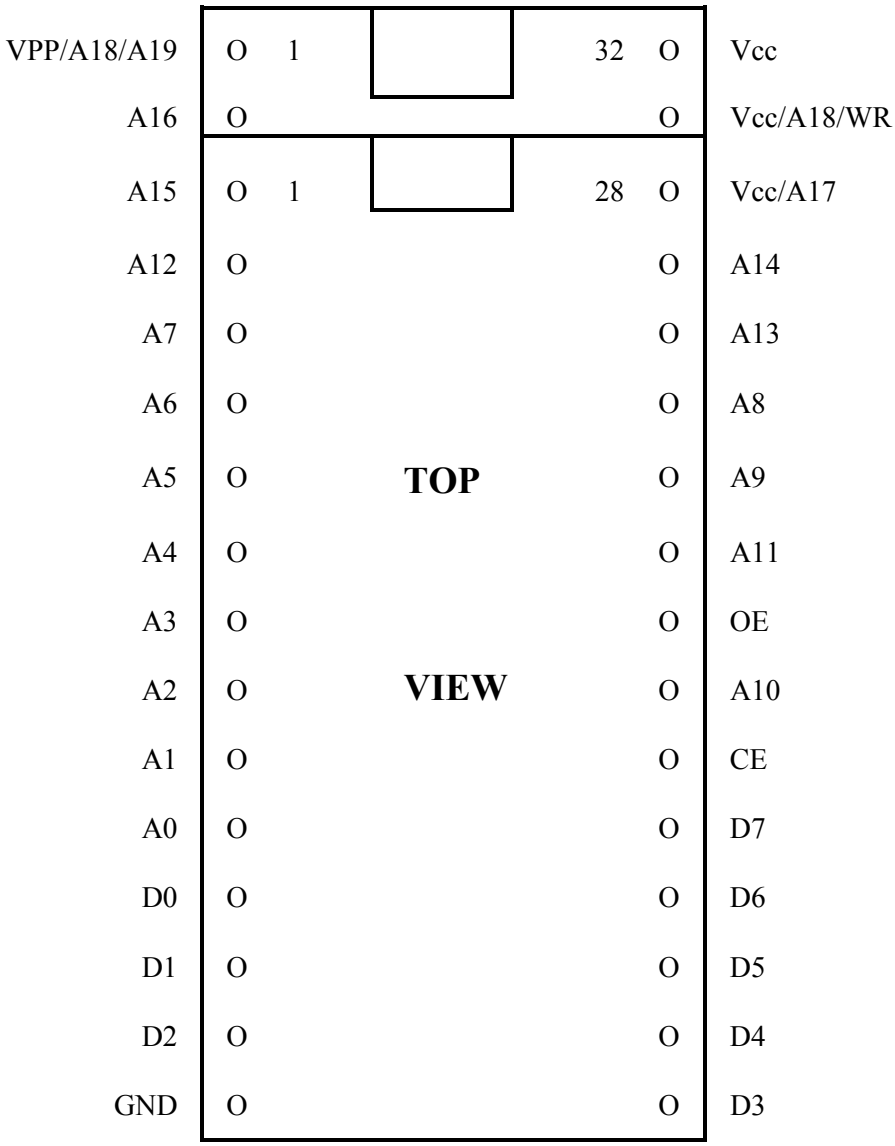
Default soldering links setting for 4Mbit Flash types:



BA **BB** **BC**

6.2.2.2 Socket Pin out:

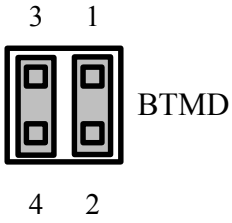
Please check for correct pin compatibility before mounting any device. 28 pin and 32 pin packages must be inserted into socket as shown below **only during power down**. Any insertion of other types or not as directed may cause permanent damage to the device and/or the board.



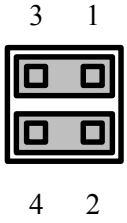
6.2.2.3 Boot Options

The CPU87 can be configured to boot either from the 8 bit ROM socket or from the 64 bit Flash Rom bank after Reset. The selection is done by jumper BTMD. When set to 1-2 and 3-4, the factory default setting, the MPC8270 boots from the 8 bit device, when BTMD is set to 1-3 and 2-4, the MPC8270 boots from 64 bit Flash.
The jumper RCFG defines if the MPC8270 „Hard Reset Configuration Word“ is read external from Flash Rom address $00, $08, $10 and $18, or if a processor internal configuration is used. Only with external configuration, some settings like various clock rates can be used by reprogramming the Flash.

Note! Internal configuration (RCFG removed) must only be set when the BDM port is used and no external hard reset configuration word is available.



Boot from 8 bit socket.
Jumper RCFG **must** be installed
and Hard Reset Config Word
must exist at address $00.



Boot from 64 bit Flash.
Jumper RCFG **must** be installed
and Hard Reset Config Word
must exist at address $00.

If the **8 bit** socket is used as boot memory, it must contain the 4 bytes of the hard reset configuration word for the MPC8270 at its base address locations $00, $08, $10 and $18.

Bit	Name	State
0	EARB	0
1	EXMC	0
2	CDIS	0
3	EBM	0
4	BPS	0
5	BPS	1
6	CIP	0
7	ISPS	0

Bit	Name	State
8	L2CPC	0
9	L2CPC	0
10	DPPC	0
11	DPPC	0
12	---	0
13	ISB	0
14	ISB	0
15	ISB	0

Bit	Name	State
16	BMS	0
17	BBD	1
18	MMR	0
19	MMR	0
20	LBPC	0
21	LBPC	0
22	APPC	1
23	APPC	0

Bit	Name	State
24	CS10PC	0
25	CS10PC	1
26	---	0
27	---	0
28	MODCK	0
29	MODCK	0
30	MODCK	0
31	MODCK	0

For detailed information about the Hard Reset Configuration Word, please refer to the MPC8270 User’s Manual.

6.2.3 The Flash Memory

The flash memory area of the CPU87 consists of four devices with a total capacity of 8MBytes as standard. The **64 bit** wide flash bank can be controlled via the **CS0** or the **CS1** line on the 603 bus of the MPC8270 and no parity check is performed. The selection between both CS-lines is performed via jumper BTMD. If the links are set to BTMD(1-3) and BTMD(2-4), the main flash memory is connected to the CS0 line, while the boot flash memory is controlled via the CS1 line of the MPC8270. The data lanes of all devices are swapped according to the necessary endian conversion. The WAIT pin is not connected and left floating. The flash memory works in normal mode if the soldering link FA is set to position 2-3. The ADV pin is connected to ground by factory and must not be changed. The pins of the Flash devices are controlled by the MPC8270 according to following table.

Main Flash Bank	MPC8270	Description
A0-A19	A28-A9	603bus address
n.c./A20	A8	603bus address
n.c./A21	A7	603bus address
CLK	CLKIN	system clock
CE	CS1	chip select
OE	---	output enable via ispLSI
ADV	CS1 or GND	address valid
WE	---	write enable via ispLSI
RST	PORST	power on reset
WP	---	write protect via ispLSI
D0-D15	D15-D0	endian swapped data lanes

If the **64 bit** wide main flash memory is used as boot memory, it must contain the 4 bytes of the hard reset configuration word for the MPC8270 at its base address locations $00, $08, $10 and $18.

Bit	Name	State
0	EARB	0
1	EXMC	0
2	CDIS	0
3	EBM	0
4	BPS	0
5	BPS	0
6	CIP	0
7	ISPS	0

Bit	Name	State
8	L2CPC	0
9	L2CPC	0
10	DPPC	0
11	DPPC	0
12	---	0
13	ISB	0
14	ISB	0
15	ISB	0

Bit	Name	State
16	BMS	0
17	BBD	1
18	MMR	0
19	MMR	0
20	LBPC	0
21	LBPC	0
22	APPC	1
23	APPC	0

Bit	Name	State
24	CS10PC	0
25	CS10PC	1
26	---	0
27	---	0
28	MODCK	0
29	MODCK	0
30	MODCK	0
31	MODCK	0

6.2.3.1 The FLASH Memory Write Protection

The (B)oard (C)ontrol (R)e(g)ister at location **CS6** offset **$03** allows for a complete protection against all write accesses to the flash devices. The BCRG contains two protection bits, one for the device write line (WE) and one for the write protect pin (WP) of the 64bit flash bank. The BCRG can be read back for verification. After a reset, these bits are set to low and the write protect mode is activated.

Bit map of the (B)oard (C)ontrol (R)e(g)ister:

BCRG @ CS6+$03	D0	D1	D2	D3	D4	D5	**D6**	**D7**
read/write	ULED3	---	ULED2	ULED1	AM2	AM0/1	**FWRE**	**FWPT**
reset	0	0	0	0	0	0	0	0
flash write protect pin = 0	x	x	x	x	x	x	x	**0**
flash write protect pin = 1	x	x	x	x	x	x	x	**1**
flash write disable	x	x	x	x	x	x	**0**	x
flash write enable	x	x	x	x	x	x	**1**	x

In addition, the flash area can be hardware protected against unintended write cycles by jumper FWRE. If jumper FWRE is installed, the flash devices are protected independent of the contents of the BCR.

For detailed chip information see Technical manual of Intel 28F160C3B

6.2.3.2 Flash Address Map for 64 Bit Boot Option

64 Bit Flash Jumper BTMD 1-3 and 2-4			
Sector	**Size**	**Address**	**Comment**
0	32 KBytes	FF80 0000 - FF80 7FFF	Hard Reset Configuration Word address 0x0000 0000 = 0x00 address 0x0000 0008 = 0x00 address 0x0000 0010 = 0x00 address 0x0000 0018 = 0x40
1	32 KBytes	FF80 8000 - FF80 FFFF	
2	32 KBytes	FF81 0000 - FF81 7FFF	
3	32 KBytes	FF81 8000 - FF81 FFFF	
4	32 KBytes	FF82 0000 - FF82 7FFF	
5	32 KBytes	FF82 8000 - FF82 FFFF	
6	32 KBytes	FF83 0000 - FF83 7FFF	
7	32 KBytes	FF83 8000 - FF83 FFFF	
8	256 KBytes	FF84 0000 - FF87 FFFF	
9	256 KBytes	FF88 0000 - FF8B FFFF	
10	256 KBytes	FF8C 0000 - FF8F FFFF	
11	256 KBytes	FF90 0000 - FF93 FFFF	
12	256 KBytes	FF94 0000 - FF97 FFFF	
13	256 KBytes	FF98 0000 - FF9B FFFF	
14	256 KBytes	FF9C 0000 - FF9F FFFF	
15	256 Kbytes	FFA0 0000 - FFA3 FFFF	
16	256 Kbytes	FFA4 0000 - FFA7 FFFF	
17	256 Kbytes	FFA8 0000 - FFAB FFFF	
18	256 KBytes	FFAC 0000 - FFAF FFFF	
19	256 Kbytes	FFB0 0000 - FFB3 FFFF	
20	256 Kbytes	FFB4 0000 - FFB7 FFFF	
21	256 Kbytes	FFB8 0000 - FFBB FFFF	
22	256 Kbytes	FFBC 0000 - FFBF FFFF	
23	256 KBytes	FFC0 0000 - FFC3 FFFF	
24	256 KBytes	FFC4 0000 - FFC7 FFFF	
25	256 KBytes	FFC8 0000 - FFCB FFFF	
26	256 KBytes	FFCC 0000 - FFCF FFFF	
27	256 KBytes	FFD0 0000 - FFD3 FFFF	
28	256 KBytes	FFD4 0000 - FFD7 FFFF	
29	256 KBytes	FFD8 0000 - FFDB FFFF	
30	256 KBytes	FFDC 0000 - FFDF FFFF	
31	256 Kbytes	FFE0 0000 - FFE3 FFFF	
32	256 Kbytes	FFE4 0000 - FFE7 FFFF	
33	256 Kbytes	FFE8 0000 - FFEB FFFF	
34	256 KBytes	FFEC 0000 - FFEF FFFF	
35	256 KBytes	FFF0 0000 - FFF3 FFFF	
36	256 KBytes	FFF4 0000 - FFF7 FFFF	
37	256 KBytes	FFF8 0000 - FFFB FFFF	
38	256 KBytes	FFFC 0000 - FFFF FFFF	Boot Code with Reset Vector at address 0xFFF0 0100

Sector 0 - 7: 32KBytes organized 4K x 64Bit = 4 Flash Devices
Sector 8 - 38: 256KBytes organized 32K x 64Bit = 4 Flash Devices

6.2.4 The DiskOnChip® Socket

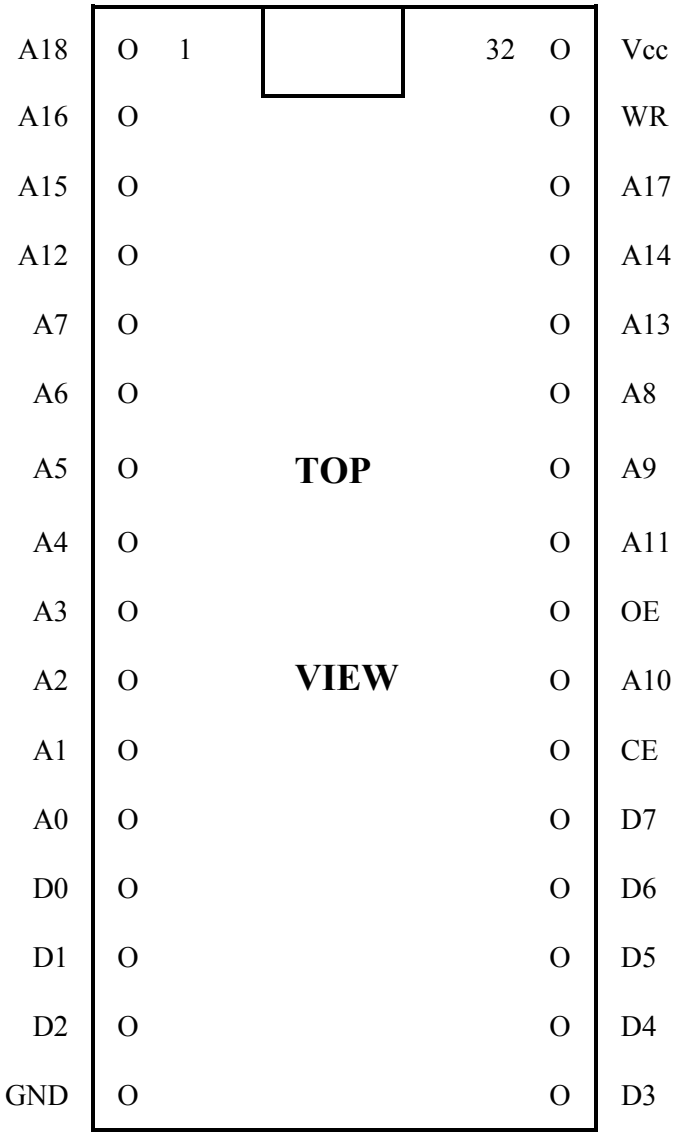
The CPU87 offers a 32 pin JEDEC socket for mounting a **5 volt** DiskOnChip® device. The selection of this device is handled via the **CS4** line on the 603 bus side of the MPC8270. Its control, data and address lines are connected according to the following table.

connected to:	DiskOnChip® Device		connected to:
(A13)	1	32	VCC
(A15)	2	31	PWE0#
(A16)	3	30	*(A14)*
A19	4	29	*(A17)*
A24	5	28	*(A18)*
A25	6	27	A23
A26	7	26	A22
A27	8	25	A20
A28	9	24	POE#
A29	10	23	A21
A30	11	22	CS11#
A31	12	21	D0
D7	13	20	D1
D6	14	19	D2
D5	15	18	D3
GND	16	17	D4

The signals within brackets are not used by the DiskOnChip® device, but the socket might also be used for other pin compatible devices with a larger address range, e. g. FLASH memory.

6.2.4.1 Socket Pin out:

Please check for correct pin compatibility before mounting any device. All 32 pin packages must be inserted into socket as shown below **only during power down**. Any insertion of other types or not as directed may cause permanent damage **to the device and/or the board.**



6.2.5 The Static RAM Area

The CPU87 contains a static ram area consisting of two SRAM devices with 512Kx8 capacity, which allows for a total capacity of 1MBytes at a **16 bit** wide data bus. The SRAM is accessed on the 603 bus side of the MPC8270 by the **CS3** select line and no parity check is performed.

The SRAM bank can be shared with other VMEbus masters but any access from an alternate VMEbus master to this area cannot be snooped, because no CPU bus arbitration is performed, i.e. this area must not be configured as cacheable.

The contents of the SRAM area is protected against data loss by a backup circuitry. The backup power is supplied by a service free gold capacitor or a lithium cell. An extended backup time can be reached, if the VMEbus standby line on ST1B pin 31 is used to supply the necessary backup power. In any case, the backup time mainly depends on the used SRAM devices and their standby power consumption. The backup feature of the CPU87 cannot be disabled. The backup power is supplied to the SRAM area as well as to the onboard real time clock.

6.2.5.1 Low-Battery Monitor

The MAX791 backup-battery controller features a monitor function to detect a low battery voltage. The low backup supply (GoldCap and Lithium cell) is monitored only during the reset period. If the voltage is below 2.0V ±0.15V, the second chip select pulse to the SRAM devices is inhibited. If the voltage is above 2.0V, all CS pulses are allowed. To use this feature you may write 0x00 to a SRAM location and 0xFF to the same location directly after Reset. The contents of the SRAM then indicates a good battery if 0xFF can be read. If you read 0x00, the battery is below 2.0V.

Note ! This feature cannot be disabled. With a low battery voltage and no check routine implemented, the second access to the SRAM fails after Reset.

6.2.5.2 The DPRAM Shared Address Decoding

The 16bit SRAM area onboard the CPU87 can be accessed by other VMEbus masters. The necessary access address from the VMEbus side is decoded and enabled by two internal registers of the VME-ispLSI. Any shared ram access from the VMEbus side must be performed with the proper address modifier combination for a standard or extended access and the state of the according compare bit must match with the state of the desired VMEbus address line. The address decoding for the extended or standard access range is automatically activated by the according address modifier combination. The enable bits for standard and extended access allow the SRAM area to be shareable or not within one or both address ranges. After reset, both registers are cleared and the shared access is disabled at all.

Bit map of the (V)ME (E)xtended (A)ddress (C)ompare Register:

VEAC @ CS6+$00	D0	D1	D2	D3	D4	D5	D6	D7
read/write	EXCR7	EXCR6	EXCR5	EXCR4	EXCR3	EXCR2	EXCR1	EXCR0
reset	0	0	0	0	0	0	0	0
compared with VME-	**A31**	**A30**	**A29**	**A28**	**A27**	**A26**	**A25**	**A24**

Bit map of the (V)ME (S)tandard (A)ddress (C)ompare Register:

VSAC @ CS6+$01	D0	D1	D2	D3	D4	D5	D6	D7
read/write	RWDN	VSHTE	VEXTE	VSTDE	STCR3	STCR2	STCR1	STCR0
reset	0	0	0	0	0	0	0	0
std.shared access disabled	x	x	x	**0**	x	x	x	x
std.shared access enabled	x	x	x	**1**	0/1	0/1	0/1	0/1
ext.shared access disabled	x	x	**0**	x	0/1	0/1	0/1	0/1
ext.shared access enabled	x	x	**1**	x	0/1	0/1	0/1	0/1
compared with VME-	x	x	x	**1**	**A23**	**A22**	**A21**	**A20**

The following AM-Codes are necessary for the shared SRAM access:

AM5	AM4	AM3	AM2	AM1	AM0	Access for:	
H	H	H	H	L	H	Standard Supervisory Data	(3D)
H	H	H	L	L	H	Standard User Data	(39)
L	L	H	H	L	H	Extended Supervisory Data	(0D)
L	L	H	L	L	H	Extended User Data	(09)

L = logical low H = logical high

6.3 The I²C Bus

The I²C bus onboard the CPU87 is controlled via the SDA (port D15) and SCL (port D14) pins of the MPC8270 and contains a real-time clock, an EEPROM and a system hardware monitor device.

6.3.1 The EEPROM

The CPU87 offers a **16KBit** serial EEPROM for storing system or board parameters. The X24C164 device is internally organized to 2048 x 8 bit and allows for at least 100000 write cycles with a typical cycle time of 5ms.

The 24C164 device responds on the I²C bus at the odd addresses from $B1 to $BF for read and on the even addresses from $B0 to $BE for write accesses.

For detailed programming information and chip description, please refer to X24C164 Data Sheet !

6.3.2 The Real Time Clock

The PCF8563 RTC features a clock function with a calendar and an universal timer with alarm and interrupt function. The RTC is protected against data loss by a backup circuitry. The backup feature supplied from a service free gold capacitor cannot be disabled. For long time applications the VMEbus standby line on ST1B pin 31 can be used to supply the necessary backup power. The low active RTC interrupt signal is connected on the MPC8270 IRQ line 5.

The RTC device responds on the I²C bus at address $A3 for read and $A2 for write accesses.

For detailed programming information and chip description, please refer to Philips PCF8563 Data Sheet !

6.3.2.1 The PCF8563T Address Map

Address	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
$00	Control/Satus 1	TEST1	0	STOP	0	TESTC	0	0	0
$01	Control/Status 2	0	0	0	TI/TP	AF	TF	AIE	TIE
$0D	CLKOUT frequency	FE	--	--	--	--	--	FD1	FD0
$0E	Timer control	TE	--	--	--	--	--	TD1	TD0
$0F	Timer countdown value	<timer countdown value>							
Address	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
		BCD format tens nibble				BCD format units nibble			
$02	Seconds	VL	<seconds 00 to 59 coded in BCD>						
$03	Minutes	--	<minutes 00 to 59 coded in BCD>						
$04	Hours	--	--	<hours 00 to 23 coded in BCD>					
$05	Days	--	--	<days 01 to 31 coded in BCD>					
$06	Weekdays	--	--	--	--	--	<weekday 0 to 6>		
$07	Monts/Century	C	--	--	<month 01 to 12 coded in BCD>				
$08	Years	<years 00 to 99 coded in BCD>							
$09	Minute alarm	AE	<minute alarm 00 to 59 coded in BCD>						
$0A	Hour alarm	AE	--	<hour alarm 00 to 23 coded in BCD>					
$0B	Day alarm	AE	--	<day alarm 01 to 31 coded in BCD>					
$0C	Weekday alarm	AE	--	--	--	--	<weekday alarm 0 to 6>		

6.3.3 The System Hardware Monitor

The board ambient and supply conditions of the CPU87 can be sensed by the microprocessor system hardware monitor LM81. It offers the monitoring of the board ambient temperature, all board supply voltages and the voltage range of an external battery. The VID0-4 inputs can be used for a user configurable 5 bit identification. A maskable interrupt can be generated on the MPC8270 **IRQ level 2** if the according enable bit within the (L)ocal (I)nterrupt (M)ask (R)egister at location **CS6+$82** is set to high. The LIMR contents is cleared after reset and can be read back for verification. The current status of the LM81 interrupt line can be detected within the LISR register at location **CS6+$83**.

The LM81 device responds on the I^2C bus at address $59 for read and $58 for write accesses.

The pins of the LM81 are connected according to following table.

connected to:	LM81		connected to:
pulldown to ground	A0/NTO	VID0	via R59 to GND, or pulled up
pulldown to ground	A1	VID1	via R60 to GND, or pulled up
CPU-SDA	SMBdata	VID2	via R61 to GND, or pulled up
CPU-SCL	SMBclock	VID3	via R62 to GND, or pulled up
not used and left open	FAN1	VID4	via R63 to GND, or pulled up
not used and left open	FAN2	Vccp1	-12V VMEbus supply
not used and left open	CI	+2.5Vin	VEE = CPU Core (2.5V or 1.8V)
not used and left open	OVTA	+3.3Vin	VDD = 3.3V for CPU & Logic
3.3V supply	V+	+5.0Vin	+5V VMEbus supply
CPU-IRQ	INT	+12Vin	+12V VMEbus supply
not used and left open	DACO/NTI	Vccp2	VMEbus 5V standby line
CPU-Reset	RESET	GND	ground

The voltage detection of the -12V VMEbus supply is handled by a resistor divider against the +5V VMEbus supply. The used division factor formats the -12V to +1.25V according to the formula:

R1 = 141K R2 = 40K Vcc = 5V V_{-12} = -12V

$$Vccp1 = Vcc \times \left(1 - \frac{R2}{R1+R2}\right) + V_{-12} \times \frac{R2}{R1+R2}$$

Vccp1 = 3.895V + (-12V) x 0.221

For detailed programming information and chip description, please refer to National LM81 Data Sheet !

6.4 Miscellaneous

6.4.1 The Backup Feature

The backup feature of the CPU87 is used to protect the **RTC** as well as the **SRAM** area. Both devices are connected to the MAX-791A, which controls the backup supply and the power up and down sequences to avoid unintended write pulses. The backup power is supplied by a **service free gold capacitor** as well as by a **260mAh lithium cell (CR2430)**. In case the cell must be replaced, the goldcap will avoid data loss of the connected devices. The RTC as well as the SRAM area cannot be disconnected from the backup power.

The gold capacitor allows for a service free short time backup without any battery or other time or temperature degrading parts. If the backup time should be extended the backup power can be supplied via the onboard lithium cell or via the VMEbus standby line on connector ST1A, pin 31. The external supply voltage should not exceed 5.25 volts and not fall below 2.5 volts to ensure correct data retention.

The power consumption table of all backup connected devices:

device:	**max.current:**	**total:**
MAX791A	5µA	5µA
PCF8563	0.5µA @ 5volts	0.5µA
KM684000ALG-5L	50µA @ 3volts	100µA

6.4.2 The Board Reset Function

During power up or power down sequences, the board supervisory circuit MAX-791A activates the board reset line and holds the CPU87 in a defined state. The reset line will be low for at least 200ms if the supply voltage reaches 4.65 volts. Below that voltage, the reset line will be continuously low.

6.4.3 Hardware Watchdog Timer

The CPU87 features a fixed rate hardware timer for watchdog purposes, which can be enabled by software. The time out rate is set to 1.6 seconds by default. Within that time at least one write access must be performed to the (W)atchdog (R)etrigger (P)ort, located at CS6+$05, to retrigger the timer. Once retriggered, i.e. enabled, it only can be disabled by a hardware reset. The time out sequence can be modified by an additional hardware component on the SMD-1206 location C35 according to following equation:

Watchdog Time-out Period in ms = 2.1 x (capacitor C35 value in nF)
(allowed values are 4,7nF to 100nF)

The modified time out sequence will only be activated, if the 0-R SMD-Resistor R42 is removed ! If R42 is installed, the time out rate is set to 1.6 seconds, independent of the value of C35.

The watchdog timer must be reset within the given time-out period by a write access to the (W)atch(D)og (R)etrigger (P)ort located at CS6+$05.

WDRP @ CS6+$05	D0	D1	D2	D3	D4	D5	D6	D7
write	---	---	---	---	---	---	---	---

6.4.4 Board Control Register

The board control register, located at CS6+$03, handles the user programmable leds, the VMEbus address modifier lines and the Flash write protect switches. A logical high enables the according function. After reset, the register is cleared, all leds are switched off and the 64 bit Flash memory area is write protected.

Bit map of the (B)oard (C)ontrol (R)e(g)ister:

BCRG @ CS6+$03	**D0**	**D1**	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**
read/write	**ULED3**	**---**	**ULED2**	**ULED1**	**AM2**	**AM0/1**	**FWRE**	**FWPT**
reset	0	0	0	0	0	0	0	0
flash write protect pin = 0	x	x	x	x	x	x	x	**0**
flash write protect pin = 1	x	x	x	x	x	x	x	**1**
flash write disable	x	x	x	x	x	x	**0**	x
flash write enable	x	x	x	x	x	x	**1**	x
VME-AM0 = 1, AM1 = 0	x	x	x	x	x	**0**	x	x
VME-AM0 = 0, AM1 = 1	x	x	x	x	x	**1**	x	x
VME-AM2 = 0	x	x	x	x	**0**	x	x	x
VME-AM2 = 1	x	x	x	x	**1**	x	x	x
user led 1 switch off	x	x	x	**0**	x	x	x	x
user led 1 switch on	x	x	x	**1**	x	x	x	x
user led 2 switch off	x	x	**0**	x	x	x	x	x
user led 2 switch on	x	x	**1**	x	x	x	x	x
user led 4 switch off	**0**	x	x	x	x	x	x	x
user led 4 switch on	**1**	x	x	x	x	x	x	x

6.4.5 Board Revision Register

For identification purposes and user defined demands, the CPU87 features an 8 bit read only register at location CS6+$07.

Bit map of the (B)oard (R)evision (R)e(g)ister:

BRRG @ CS6+$07	D0	D1	D2	D3	D4	D5	D6	D7
Revsison 4	0	0	0	0	0	1	0	0

6.5 The CPU87 Interfaces

6.5.1 The Serial I/Os

Four RS232 serial interfaces are accessible via three RJ45 connectors on the front panel of the CPU87. The SCC1 and SCC2 ports use a standard pin out with two handshake lines on their connectors while both SMC ports share a single RJ45 connector according to the following table. The SMC2 port uses the standard RTS/CTS lines and can be disconnected by removing the 0R links R101 and R102.

Frontpanel Connector ST4		
RJ45	**Port**	**RS232**
1		---
2	SMC2	TxD
3		GND
4	SMC1	TxD
5	SMC1	RxD
6		---
7	SMC2	RxD
8		---

Frontpanel Connector ST3-D		
RJ45	**Port**	**RS232**
1		---
2	SCC1	RTS
3		GND
4	SCC1	TxD
5	SCC1	RxD
6		---
7	SCC1	CTS
8		---

Frontpanel Connector ST3-C		
RJ45	**Port**	**RS232**
1		---
2	SCC2	RTS
3		GND
4	SCC2	TxD
5	SCC2	RxD
6		---
7	SCC2	CTS
8		---

6.5.2 The Fast Ethernet Ports

The CPU87 offers two 100/10Mbit Ethernet channels with twisted pair interface. Both ports are accessible via two 8 pin RJ45 connectors on the front panel. Each channel is handled by an LXT971 controller with MII-Interface connected to the FCC1 and FCC2 ports of the MPC8270. The device address for the channel A controller is set by hardware to $1. The controller for channel B uses the device address $2.

Channel-A = FCC1			Channel-B = FCC2		
LXT971	**Signal**	**MPC8270**	**MPC8270**	**Signal**	**LXT971**
MDINT	A_MDINT	P_A0	P_A1	B_MDINT	MDINT
MDC	MII1_MDC	P_A22	P_A24	MII2_MDC	MDC
MDIO	MII1_MDIO	P_A23	P_A25	MII2_MDIO	MDIO
PWRDN	MII1_PWRDN	P_A3	P_A4	MII2_PWRDN	PWRDN
PAUSE	MII1_PAUSE	P_A5	P_A6	MII2_PAUSE	PAUSE
TXSLEW0	MII1_TXSL0	P_A10	P_A12	MII2_TXSL0	TXSLEW0
TXSLEW1	MII1_TXSL1	P_A11	P_A13	MII2_TXSL1	TXSLEW1
TXD3	MII1_TXD3	P_A21	P_B25	MII2_TXD3	TXD3
TXD2	MII1_TXD2	P_A20	P_B24	MII2_TXD2	TXD2
TXD1	MII1_TXD1	P_A19	P_B23	MII2_TXD1	TXD1
TXD0	MII1_TXD0	P_A18	P_B22	MII2_TXD0	TXD0
TXEN	MII1_TXEN	P_A28	P_B29	MII2_TXEN	TXEN
TXER	MII1_TXER	P_A29	P_B31	MII2_TXER	TXER
TXCLK	MII1_TXCLK	P_C20	P_C18	MII2_TXCLK	TXCLK
RXD3	MII1_RXD3	P_A14	P_B18	MII2_ RXD3	RXD3
RXD2	MII1_RXD2	P_A15	P_B19	MII2_ RXD2	RXD2
RXD1	MII1_ RXD1	P_A16	P_B20	MII2_ RXD1	RXD1
RXD0	MII1_ RXD0	P_A17	P_B21	MII2_ RXD0	RXD0
RXDV	MII1_ RXDV	P_A27	P_B30	MII2_ RXDV	RXDV
RXER	MII1_RXER	P_A26	P_B28	MII2_RXER	RXER
RXCLK	MII1_RXCLK	P_C21	P_C19	MII2_RXCLK	RXCLK
COL	MII1_COL	P_A31	P_B27	MII2_COL	COL
CRS	MII1_CRS	P_A30	P_B26	MII2_CRS	CRS

6.5.2.1 The 10/100Mbps LAN Interface Connector ST3-A

Pin:	Signal:	Description:	Port FCC1
1	TxD+	10/100Mbps TP+ transmit line	
2	TxD-	10/100Mbps TP- transmit line	
3	RxD+	10/100Mbps TP+ receive line	
4	center	75R terminated	
5	center	75R terminated	
6	RxD-	10/100Mbps TP- receive line	
7	center	75R terminated	
8	center	75R terminated	

6.5.2.2 The 10/100Mbps LAN Interface Connector ST3-B

Pin:	Signal:	Description:	Port FCC2
1	TxD+	10/100Mbps TP+ transmit line	
2	TxD-	10/100Mbps TP- transmit line	
3	RxD+	10/100Mbps TP+ receive line	
4	center	75R terminated	
5	center	75R terminated	
6	RxD-	10/100Mbps TP- receive line	
7	center	75R terminated	
8	center	75R terminated	

6.5.2.3 The Network Status Leds

There are two network front panel status LEDs for each channel, which can be programmed via the management data port within the LED configuration register of each LXT971 according to following table.

LED config. register @ $14	Led 1				Led 2			
data bit:	15	14	13	12	11	10	9	8
speed status)[1]	0	0	0	0	**0**	**0**	**0**	**0**
transmit status	0	0	0	1	0	0	0	1
receive status	0	0	1	0	0	0	1	0
collision status	0	0	1	1	0	0	1	1
link status	0	1	0	0	0	1	0	0
duplex status	0	1	0	1	0	1	0	1
unused	0	1	1	0	0	1	1	0
receive or transmit activity	0	1	1	1	0	1	1	1
test mode led on	1	0	0	0	1	0	0	0
test mode led off	1	0	0	1	1	0	0	1
test mode led flash fast	1	0	1	0	1	0	1	0
test mode led flash slow	1	0	1	1	1	0	1	1
link and receive status	1	1	0	0	1	1	0	0
link and activity status)[2]	**1**	**1**	**0**	**1**	1	1	0	1
duplex and collision status	1	1	1	0	1	1	1	0
unused	1	1	1	1	1	1	1	1

)[1] Default setting in VxWorks BSP for LED 2

)[2] Default setting in VxWorks BSP for LED 1

6.6 The Floppy Disk Controller (Option)

The CPU87 provides the **FDC37C78** floppy disk controller interface from **SMSC®**. It uses the **CS5** select line of the MPC8270 as an **8 bit** device. The DMA function works in memory to memory mode with external request and no address increment on the FDC access address **CS5+$80**. This feature allows the DMA read/write timing parameters to be equivalent to the normal read/write operation.

FDC-Signal:		Description:	MPC8270-Signal:
RESET	input	high active reset	HRST via ispLSI
D0-D7	I/O	byte lane big/little endian swapped	D7-D0
A0-A2	input	byte sized register offset	A31-A29
CS	input	low active select line	CS5 via ispLSI
IOR	input	low active read line	POE via ispLSI
IOW	input	low active write line	PWE0 via ispLSI
IRQ	output	high active interrupt line	IRQ6 via ispLSI
DRQ	output	high active DMA request	DREQ1 via ispLSI
DACK	input	low active DMA acknowledge	CS5 +$80 via ispLSI
TC	input	high active terminal count	tied to low via ispLSI

all signals, fed through the ispLSI, are changed, if necessary, to their respective logical active state

6.6.1.1 The Floppy Interface Connector ST2

The FDC interface signals are linked to the VMEbus connector ST2 on its row C as show in the following table.

Pin	Row z	Row a	Row b	Row c	Row d
1	Opt I/O		+5V		Opt I/O
2	Opt I/O		GND		Opt I/O
3	Opt I/O				Opt I/O
4	Opt I/O		A24	**Index**	Opt I/O
5	Opt I/O		A25	**Motor On 2**	Opt I/O
6	Opt I/O		A26	**Drive Select 1**	Opt I/O
7	Opt I/O		A27	**Drive Select 2**	Opt I/O
8	Opt I/O		A28	**Motor On 1**	Opt I/O
9	Opt I/O		A29	**Direction In**	Opt I/O
10	Opt I/O	**GND**	A30	**Step**	Opt I/O
11	Opt I/O	**GND**	A31	**Write Data**	Opt I/O
12	Opt I/O	**GND**	GND	**Write Gate**	Opt I/O
13	Opt I/O		+5V	**Track 0**	Opt I/O
14	Opt I/O	**GND**	D16	**Write Protect**	Opt I/O
15	Opt I/O	**GND**	D17	**Read Data**	Opt I/O
16	Opt I/O		D18	**Side Select**	Opt I/O
17	Opt I/O	**GND**	D19	**Ready**	Opt I/O
18	Opt I/O		D20		Opt I/O
19	Opt I/O		D21		Opt I/O
20	Opt I/O		D22		Opt I/O
21	Opt I/O		D23		Opt I/O
22	Opt I/O		GND		Opt I/O
23	Opt I/O		D24		Opt I/O
24	Opt I/O		D25		Opt I/O
25	Opt I/O		D26		Opt I/O
26	Opt I/O		D27		Opt I/O
27	Opt I/O	Dout_SM+	D28	Dout_SM-	Opt I/O
28	Opt I/O	Din_SM+	D29	Din_SM-	Opt I/O
29	Opt I/O	Clk_SM+	D30	Clk_SM-	Opt I/O
30	Opt I/O	Ld_SM+	D31	Ld_SM-	Opt I/O
31	Opt I/O	DataHP+	GND	DataHP-	Opt I/O
32	Opt I/O	ClkHP+	+5V	ClkHP-	Opt I/O

6.7 Interrupt Structure

6.7.1 The Interrupt Handler

The CPU87 offers a bit maskable 7 level VMEbus and a 7 level onboard interrupt handler. The 7 VMEbus interrupt levels work in vector controlled mode only. The interrupt priority structure of the VMEbus must be realized by software, i.e. by the use of mask and status register bits for each VMEbus interrupt level. The interrupt priorisation of all local interrupt sources can be freely handled according to the users' demands.

6.7.2 The VMEbus Interrupt Handler

Each VMEbus interrupt level can be enabled or disabled by software via the VMEbus interrupt mask register at location **CS6+$80**. After a hardware reset all bits of this register are set to zero and all VMEbus interrupt levels are disabled. **To enable** a VMEbus interrupt level the according bit must be **set to high**. The register contents can be read back for verification. All VMEbus interrupt lines share the MPC8270 interrupt line **IRQ3.**

Bit map of the (V)MEbus (I)nterrupt (M)ask (R)egister:

VIMR @ CS6+$80	D0	D1	D2	D3	D4	D5	D6	D7
read/write	**VIM7**	**VIM6**	**VIM5**	**VIM4**	**VIM3**	**VIM2**	**VIM1**	BYMD
reset	0	0	0	0	0	0	0	0
VME-IRQ1 enable	x	x	x	x	x	x	**1**	x
VME-IRQ1 disable	x	x	x	x	x	x	**0**	x
VME-IRQ2 enable	x	x	x	x	x	**1**	x	x
VME-IRQ2 disable	x	x	x	x	x	**0**	x	x
VME-IRQ3 enable	x	x	x	x	**1**	x	x	x
VME-IRQ3 disable	x	x	x	x	**0**	x	x	x
VME-IRQ4 enable	x	x	x	**1**	x	x	x	x
VME-IRQ4 disable	x	x	x	**0**	x	x	x	x
VME-IRQ5 enable	x	x	**1**	x	x	x	x	x
VME-IRQ5 disable	x	x	**0**	x	x	x	x	x
VME-IRQ6 enable	x	**1**	x	x	x	x	x	x
VME-IRQ6 disable	x	**0**	x	x	x	x	x	x
VME-IRQ7 enable	**1**	x	x	x	x	x	x	x
VME-IRQ7 disable	**0**	x	x	x	x	x	x	x

The current state of each VMEbus interrupt line can be checked within the VMEbus interrupt status register at location CS6+$81. The low active status of each interrupt line is valid at any time, no matter if the according interrupt line is enabled or not.

Bit map of the (V)MEbus (I)nterrupt (S)tatus (R)egister:

VISR @ CS6+$81	**D0**	**D1**	**D2**	**D3**	**D4**	**D5**	**D6**	D7
read only	**VIRQ7**	**VIRQ6**	**VIRQ5**	**VIRQ4**	**VIRQ3**	**VIRQ2**	**VIRQ1**	---
VME-IRQ1 inactive	x	x	x	x	x	x	**0**	0
VME-IRQ1 active	x	x	x	x	x	x	**1**	0
VME-IRQ2 inactive	x	x	x	x	x	**0**	x	0
VME-IRQ2 active	x	x	x	x	x	**1**	x	0
VME-IRQ3 inactive	x	x	x	x	**0**	x	x	0
VME-IRQ3 active	x	x	x	x	**1**	x	x	0
VME-IRQ4 inactive	x	x	x	**0**	x	x	x	0
VME-IRQ4 active	x	x	x	**1**	x	x	x	0
VME-IRQ5 inactive	x	x	**0**	x	x	x	x	0
VME-IRQ5 active	x	x	**1**	x	x	x	x	0
VME-IRQ6 inactive	x	**0**	x	x	x	x	x	0
VME-IRQ6 active	x	**1**	x	x	x	x	x	0
VME-IRQ7 inactive	**0**	x	x	x	x	x	x	0
VME-IRQ7 active	**1**	x	x	x	x	x	x	0

6.7.2.1 The VMEbus Interrupt Acknowledge

The necessary VMEbus acknowledge procedure must be performed by a **read** access within the address range from $xxx80000 to $xxx8FFFF of **CS9** decoded area. This range works as a 16 bit device with an **external** acknowledge. The data byte transferred on the data line D7 to D0 during the acknowledge cycle can be used to distinguish between different interrupt sources on the same VMEbus interrupt level. The upper byte from D15 to D8 does not contain valid data during the **byte sized** acknowledge read cycle on odd VMEbus addresses. In order to meet the VMEbus specifications, the necessary acknowledge cycles must be performed according to following table.

VMEbus Interrupt Acknowledge Access Address Overview:

IACK for level	VA3	VA2	VA1	Access Address	Command
VME-IRQ1	0	0	1	$xxx8 0003	Byte Read
VME-IRQ2	0	1	0	$xxx8 0005	Byte Read
VME-IRQ3	0	1	1	$xxx8 0007	Byte Read
VME-IRQ4	1	0	0	$xxx8 0009	Byte Read
VME-IRQ5	1	0	1	$xxx8 000B	Byte Read
VME-IRQ6	1	1	0	$xxx8 000D	Byte Read
VME-IRQ7	1	1	1	$xxx8 000F	Byte Read

6.7.3 The Onboard Interrupt Handler

There are seven low active interrupt sources onboard the CPU87. Each source can be enabled or disabled individually by software and its current status can be checked within a status register. After a hardware reset all bits of the enable register are set to zero and all local interrupt sources are disabled. **To enable** an interrupt source the according bit must be **set to high**. The register contents can be read back for verification. The sources are distributed to the seven interrupt input lines of the MPC8270 according to following table.

Level	MPC8270	External Source
0	**IRQ0/NMI_OUT/APE**	not used
1	**IRQ1/EXT_BG2**	**VME-ACF, Abort-Key**
2	**IRQ2/EXT_DBG2**	**System-Monitor**
3	**IRQ3/WT/BADDR30**	**VME-IRQ1-7**
4	**IRQ4/EXT_BG3**	**PMC-IRQA,B,C,D**
5	**IRQ5/EXT_DBG3**	**Real Time Clock**
6	**IRQ6/CSE0**	**Floppy Disc Controller**
7	**IRQ7/CSE1**	**VME-SYSF, VMEbus-Mailbox**

Bit map of the (L)ocal (I)nterrupt (M)ask (R)egister:

LIMR @ CS6+$82	D0	D1	D2	D3	D4	D5	D6	D7
read/write	VACF	PMC	VSYF	ISCM	IRTC	IFDC	IMBX	IABO
reset	0	0	0	0	0	0	0	0
ABORT key IRQ disable	x	x	x	x	x	x	x	**0**
ABORT key IRQ enable	x	x	x	x	x	x	x	**1**
Mailbox IRQ disable	x	x	x	x	x	x	**0**	x
Mailbox IRQ enable	x	x	x	x	x	x	**1**	x
FDC IRQ disable	x	x	x	x	x	**0**	x	x
FDC IRQ enable	x	x	x	x	x	**1**	x	x
RTC IRQ disable	x	x	x	x	**0**	x	x	x
RTC IRQ enable	x	x	x	x	**1**	x	x	x
LM81 IRQ disable	x	x	x	**0**	x	x	x	x
LM81 IRQ enable	x	x	x	**1**	x	x	x	x
VME-SYS-Fail disable	x	x	**0**	x	x	x	x	x
VME-SYS-Fail enable	x	x	**1**	x	x	x	x	x
PMC IRQ disable	x	**0**	x	x	x	x	x	x
PMC IRQ enable	x	**1**	x	x	x	x	x	x
VME-AC-Fail disable	**0**	x	x	x	x	x	x	x
VME-AC-Fail enable	**1**	x	x	x	x	x	x	x

The current state of each local interrupt source can be checked within the local interrupt status register at location CS6+$83. The high active status of each interrupt line is valid at any time, no matter if the according interrupt line is enabled or not.

Bit map of the (L)ocal (I)nterrupt (S)tatus (R)egister:

LISR @ CS6+$83	**D0**	D1	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**
read only	**VACF**	**---**	**VSYF**	**ISCM**	**IRTC**	**IFDC**	**IMBX**	**IABO**
Abort Key inactive	x	0	x	x	x	x	x	**0**
Abort Key active	x	0	x	x	x	x	x	**1**
Mailbox IRQ inactive	x	0	x	x	x	x	**0**	x
Mailbox IRQ active	x	0	x	x	x	x	**1**	x
FDC IRQ inactive	x	0	x	x	x	**0**	x	x
FDC IRQ active	x	0	x	x	x	**1**	x	x
RTC IRQ inactive	x	0	x	x	**0**	x	x	x
RTC IRQ active	x	0	x	x	**1**	x	x	x
LM81 IRQ inactive	x	0	x	**0**	x	x	x	x
LM81 IRQ active	x	0	x	**1**	x	x	x	x
VME-Sys-Fail inactive	x	0	**0**	x	x	x	x	x
VME-Sys-Fail active	x	0	**1**	x	x	x	x	x
VME-AC-Fail inactive	**0**	0	x	x	x	x	x	x
VME-AC-Fail active	**1**	0	x	x	x	x	x	x

6.8 The VMEbus Interface

The VMEbus interface of the CPU87 is designed according to the VMEbus specification ANSI/IEEE STD1014-1987, IEC 821 & 297. The VMEbus connector ST1 rows A, B and C and ST2 row B contain all standard VMEbus lines, necessary for A16/A24/A32, D8/D16/D32 master/slave boards. All unused daisy chain lines are linked through, i.e. no external bypass links are necessary. The address modifier signals AM0 to AM5 are a part of the VMEbus specification and serve to differentiate between certain memory areas. All address modifier lines are necessary for the mailbox and the shared access decoding logic. The CPU87 accepts only slave data accesses within the VMEbus short I/O range, the VMEbus standard access area and the VMEbus extended access range.

The following AM-Codes are accepted by the CPU87:

AM5	AM4	AM3	AM2	AM1	AM0	Access for:	
H	H	H	H	L	H	Standard Supervisory Data	(3D)
H	H	H	L	L	H	Standard User Data	(39)
H	L	H	H	L	H	Short I/O Supervisory Data	(2D)
H	L	H	L	L	H	Short I/O User Data	(29)
L	L	H	H	L	H	Extended Supervisory Data	(0D)
L	L	H	L	L	H	Extended User Data	(09)

L = logical low H = logical high

The CPU87 is able to generate user or supervisor, data or program access cycles on the VMEbus. The according address modifier combination is handled by different address ranges and the board control register.

Bit map of the (B)oard (C)ontrol (R)e(g)ister:

BCRG @ CS6+$03	D0	D1	D2	D3	**D4**	**D5**	D6	D7
read/write	ULED3	---	ULED2	ULED1	**AM2**	**AM0/1**	FWRE	FWPT
reset	0	0	0	0	0	0	0	0
data access	x	x	x	x	x	**0**	x	x
program access	x	x	x	x	x	**1**	x	x
user access	x	x	x	x	**0**	x	x	x
supervisor access	x	x	x	x	**1**	x	x	x

The address modifier lines AM5 and AM4 are address decoded according to the following table. The data size represents the maximum allowed data width, i.e. the longword signal is only driven active within the A32/D32 address range, never within the other address ranges. Any longword access within the non-D32 ranges is automatically split into several byte or word sized cycles.

Function	AM5	AM4	start	end	size
VMEbus Extended Access Range	L	L	$8000 0000	$80FF FFFF	A32/D32
VMEbus Standard Access Range	H	H	$FE00 0000	$FEFF FFFF	A24/D16
VMEbus Short I/O Access Range	H	L	$FD00 0000	$FD07 FFFF	A24/D16
VMEbus Int.Ackn. Access Range	X	X	$FD08 0000	$FD0F FFFF	A24/D16

L = logical low H = logical high X = don't care

The following AM-Codes are generated by the CPU87:

AM5	**AM4**	**AM3**	**AM2**	**AM1**	**AM0**	**Access for:**	
H	H	H	H	H	L	Standard Supervisory Prog.	(3E)
H	H	H	H	L	H	Standard Supervisory Data	(3D)
H	H	H	L	H	L	Standard User Prog.	(3A)
H	H	H	L	L	H	Standard User Data	(39)
H	L	H	H	L	H	Short I/O Supervisory Data	(2D)
H	L	H	L	L	H	Short I/O User Data	(29)
L	L	H	H	H	L	Extended Supervisory Prog.	(0E)
L	L	H	H	L	H	Extended Supervisory Data	(0D)
L	L	H	L	H	L	Extended User Prog.	(0A)
L	L	H	L	L	H	Extended User Data	(09)

L = logical low H = logical high

The CPU87 generates the following VMEbus cycles within the standard, extended and interrupt acknowledge address ranges.

CPU		VIMR	VMEbus		
cycle	**A0**	**BYMD**	**UDS**	**LDS**	**LWRD**
read byte	x	0	0	0	1
read word	x	0	0	0	1
read lword	x	0	0	0	0
write byte	0	x	0	1	1
write byte	1	x	1	0	1
write word	x	x	0	0	1
write lword	x	x	0	0	0
read byte	0	1	0	1	1
read byte	1	1	1	0	1
read word	0	1	0	1	1
read word	1	1	1	0	1
read lword	0	1	0	1	0
read lword	1	1	1	0	0

The BYMD function is contained within the VMEbus interrupt mask register. It is used to generate byte sized read cycles on the VMEbus, because all normal read cycles from the VMEbus are by default word or longword sized. The shadowed area can be used, but care must be taken because of invalid data paths or unallowed VMEbus cycle combinations. Any write cycle to the VMEbus is always performed with the CPU requested size.

Bit map of the (V)MEbus (I)nterrupt (M)ask (R)egister:

VIMR @ CS6+$80	D0	D1	D2	D3	D4	D5	D6	**D7**
read/write	VIM7	VIM6	VIM5	VIM4	VIM3	VIM2	VIM1	**BYMD**
reset	0	0	0	0	0	0	0	**0**
VMEbus Byte Mode Enable	x	x	x	x	x	x	x	**1**
VMEbus Byte Mode Disable	x	x	x	x	x	x	x	**0**

Pin Assignment of the VMEbus Connector ST1

Pin	Row A	Row B	Row C
1	D00	BBSY*	D08
2	D01	(BCLR*)	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	UDS*	BR0*	SYSRESET*
13	LDS*	BR1*	LWORD*
14	RW*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*		A17
22	IACKOUT*		A16
23	AM4	GND	A15
24	A01	IRQ7*	A14
25	A02	IRQ6*	A13
26	A03	IRQ5*	A12
27	A04	IRQ4*	A11
28	A05	IRQ3*	A10
29	A06	IRQ2*	A09
30	A07	IRQ1*	A08
31	-12V	5VSTB	+12V
32	+5V	+5V	+5V

(signals enclosed in brackets are not used and left open)

6.8.1 Pin Assignment of the VMEbus Connector ST2

Pin	Row z	Row a	Row b	Row c	Row d
1	Opt I/O		+5V		Opt I/O
2	Opt I/O		GND		Opt I/O
3	Opt I/O				Opt I/O
4	Opt I/O		A24	Index	Opt I/O
5	Opt I/O		A25	Motor On 1	Opt I/O
6	Opt I/O		A26	Drive Select 2	Opt I/O
7	Opt I/O		A27	Drive Select 1	Opt I/O
8	Opt I/O		A28	Motor On 2	Opt I/O
9	Opt I/O		A29	Direction In	Opt I/O
10	Opt I/O	GND	A30	Step	Opt I/O
11	Opt I/O	GND	A31	Write Data	Opt I/O
12	Opt I/O	GND	GND	Write Gate	Opt I/O
13	Opt I/O		+5V	Track 0	Opt I/O
14	Opt I/O	GND	D16	Write Protect	Opt I/O
15	Opt I/O	GND	D17	Read Data	Opt I/O
16	Opt I/O		D18	Side Select	Opt I/O
17	Opt I/O	GND	D19	Ready	Opt I/O
18	Opt I/O		D20		Opt I/O
19	Opt I/O		D21		Opt I/O
20	Opt I/O		D22		Opt I/O
21	Opt I/O		D23		Opt I/O
22	Opt I/O		GND		Opt I/O
23	Opt I/O		D24		Opt I/O
24	Opt I/O		D25		Opt I/O
25	Opt I/O		D26		Opt I/O
26	Opt I/O		D27		Opt I/O
27	Opt I/O	Dout_SM+	D28	Dout_SM-	Opt I/O
28	Opt I/O	Din_SM+	D29	Din_SM-	Opt I/O
29	Opt I/O	Clk_SM+	D30	Clk_SM-	Opt I/O
30	Opt I/O	Ld_SM+	D31	Ld_SM-	Opt I/O
31	Opt I/O	DataHP+	GND	DataHP-	Opt I/O
32	Opt I/O	ClkHP+	+5V	ClkHP-	Opt I/O

6.8.2 The VMEbus Mailbox

The mailbox feature of the CPU87 is realized by a programmable location monitor function within the VMEbus short I/O range. The programmable base address decodes the VMEbus address lines from A15 down to A8 and all VMEbus address modifier lines. The mailbox issues an interrupt on **level 7** if a byte or word sized write cycle is performed within the programmed address range. The mailbox decoding function must be enabled within the VSAC at location CS6+$01. If the VSHTE bit is set to high, the mailbox decoding is enabled and, in case the according interrupt mask bit within LIMR is set, a mailbox interrupt can be generated. The interrupt will be held active until a mailbox clear command by a single write access to location CS6+$06 is performed. The actual state of the mailbox interrupt can be detected within the local IRQ status register at location CS6+$83. After a reset the according mask and enable bits are set to zero and the mailbox decoding and interrupt are disabled.

Bit map of the (V)ME (M)ailbox (A)ddress (C)ompare Register:

VMAC @ CS6+$02	**D0**	**D1**	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**
read/write	**SHCR7**	**SHCR6**	**SHCR5**	**SHCR4**	**SHCR3**	**SHCR2**	**SHCR1**	**SHCR0**
reset	0	0	0	0	0	0	0	0
compared with VME-	**A15**	**A14**	**A13**	**A12**	**A11**	**A10**	**A9**	**A8**

Bit map of the (V)ME (S)tandard (A)ddress (C)ompare Register:

VSAC @ CS6+$01	D0	**D1**	D2	D3	D4	D5	D6	D7
read/write	RWDN	**VSHTE**	VEXTE	VSTDE	STCR3	STCR2	STCR1	STCR0
reset	0	0	0	0	0	0	0	0
short I/O access disabled	x	**0**	x	x	x	x	x	x
short I/O access enabled	x	**1**	x	x	x	x	x	x

The following AM-Codes are necessary for the mailbox access:

AM5	**AM4**	**AM3**	**AM2**	**AM1**	**AM0**	**Access for:**	
H	L	H	H	L	H	Short I/O Supervisory Data	(2D)
H	L	H	L	L	H	Short I/O User Data	(29)

L = logical low H = logical high

Bit map of the (L)ocal (I)nterrupt (M)ask (R)egister:

LIMR @ CS6+$82	D0	D1	D2	D3	D4	D5	**D6**	D7
read/write	VACF	PMC	VSYF	ISCM	IRTC	IFDC	**IMBX**	IABO
reset	0	0	0	0	0	0	0	0
Mailbox IRQ disable	x	x	x	x	x	x	**0**	x
Mailbox IRQ enable	x	x	x	x	x	x	**1**	x

Bit map of the (L)ocal (I)nterrupt (S)tatus (R)egister:

LISR @ CS6+$83	D0	D1	D2	D3	D4	D5	**D6**	D7
read only	VACF	---	VSYF	ISCM	IRTC	IFDC	**IMBX**	IABO
Mailbox IRQ inactive	x	0	x	x	x	x	**0**	x
Mailbox IRQ active	x	0	x	x	x	x	**1**	x

Bit map of the (C)lear (M)ailbox (I)nterrupt (P)ort:

CMIP @ CS6+$06	D0	D1	D2	D3	D4	D5	D6	D7
write	clear mailbox IRQ							

6.8.3 The VMEbus Requester

The CPU87 contains a single level 2:1 pass requester with (**R)**elease (**W)**hen (**D)**one or a four level (**R)**elease (**O)**n (**R)**equest mode. The RWD requester releases the VMEbus mastership after the completion of each bus cycle and it has to request for it for every following VMEbus cycle. The ROR method releases the VMEbus only, if the current VMEbus cycles have been completed and any other device in the VMEbus system requests for the bus mastership. If there are no other requests, the ROR requester remains being bus master even if it does not access the VMEbus.

The **RWDN** method is enabled within the VME standard access compare at location CS6+$01. If this bit is set to low, the release when done mode is active, otherwise the requester works in release on request mode.

Bit map of the (V)ME (S)tandard (A)ddress (C)ompare Register:

VSAC @ CS6+$01	**D0**	D1	D2	D3	D4	D5	D6	D7
read/write	**RWDN**	VSHTE	VEXTE	VSTDE	STCR3	STCR2	STCR1	STCR0
reset	0	0	0	0	0	0	0	0
Requester RWDN mode	**0**	x	x	x	x	x	x	x
Requester ROR mode	**1**	x	x	x	x	x	x	x

6.8.4 The VMEbus Arbiter

The CPU87 is equipped with a single level VMEbus arbiter on request level 3. This allows the board to work as VMEbus controller as well as a bus slave in any combination.

The VMEbus arbiter function can be enabled, if jumper ARBE is installed. This link enables also all other system controller functions according to following table.

VMEbus Signal	**Slot 1 Function**	**Driver Type**	**not Slot 1 Function**
System Clock	Output	Totem Pole	Tristate
System Reset	Input/Output	Open Drain	Input
Bus Error	Input/Output	Open Drain	Input
Bus Grant In 3	Input/Output	Totem Pole	Input

Please make sure, that only **one** system controller is enabled within a VMEbus system at a time, usually located in the leftmost slot. The use of more than one system controller will lead to improper operation and may cause permanent damage.

6.8.5 The VMEbus Timer

The CPU87 offers a bus monitor to supervise all VMEbus accesses. This time out counter terminates any cycle with the bus error signal, if the access exceeds a certain time, because a non existing device has been addressed or a defect device does not respond. The VMEbus **BTO** feature offers a **time out** sequence of **27µs** starting at the falling edge of one or both VMEbus data strobes. It will be automatically activated, if the system controller function is enabled by jumper **ARBE**. If the board is not system controller, the bus monitor function of the VMEbus side is **not** disabled but the time out sequence is set to about **60µs.**

6.8.6 Preparations for VMEbus Multiprocessing

In case a VMEbus system should be configured for more than one VMEbus master, the user must verify, that only **one** system controller is enabled in the whole system. The system controller is usually located in the leftmost slot and drives the bus grant in lines of slot 1. It supplies the system with the system clock, the system reset, and optionally the bus error and the bus clear information. All these lines, with the exception of the system reset and the bus error signal, are totem pole outputs and **must** be controlled **only** by the system controller within the VMEbus system. The system reset and the bus error lines are driven by open collector circuits and might be driven by more than one board.

7. Register Overview

Bit map of the (V)ME (E)xtended (A)ddress (C)ompare Register:

VEAC @ CS6+$00	D0	D1	D2	D3	D4	D5	D6	D7
read/write	EXCR7	EXCR6	EXCR5	EXCR4	EXCR3	EXCR2	EXCR1	EXCR0
reset	0	0	0	0	0	0	0	0
compared with VME-	A31	A30	A29	A28	A27	A26	A25	A24

Bit map of the (V)ME (S)tandard (A)ddress (C)ompare Register:

VSAC @ CS6+$01	D0	D1	D2	D3	D4	D5	D6	D7
read/write	RWDN	VSHTE	VEXTE	VSTDE	STCR3	STCR2	STCR1	STCR0
reset	0	0	0	0	0	0	0	0
std.shared access disabled	x	x	x	0	x	x	x	x
std.shared access enabled	x	x	x	1	0/1	0/1	0/1	0/1
ext.shared access disabled	x	x	0	x	0/1	0/1	0/1	0/1
ext.shared access enabled	x	x	1	x	0/1	0/1	0/1	0/1
compared with VME-	x	x	x	1	A23	A22	A21	A20
short I/O access disabled	x	0	x	x	x	x	x	x
short I/O access enabled	x	1	x	x	x	x	x	x
Requester RWDN mode	0	x	x	x	x	x	x	x
Requester ROR mode	1	x	x	x	x	x	x	x

Bit map of the (V)ME (M)ailbox (A)ddress (C)ompare Register:

VMAC @ CS6+$02	D0	D1	D2	D3	D4	D5	D6	D7
read/write	SHCR7	SHCR6	SHCR5	SHCR4	SHCR3	SHCR2	SHCR1	SHCR0
reset	0	0	0	0	0	0	0	0
compared with VME-	A15	A14	A13	A12	A11	A10	A9	A8

Bit map of the (B)oard (C)ontrol (R)e(g)ister:

BCRG @ CS6+$03	D0	D1	D2	D3	D4	D5	D6	D7
read/write	ULED3	---	ULED2	ULED1	AM2	AM0/1	FWRE	FWPT
reset	0	0	0	0	0	0	0	0
flash write protect pin = 0	x	x	x	x	x	x	x	0
flash write protect pin = 1	x	x	x	x	x	x	x	1
flash write disable	x	x	x	x	x	x	0	x
flash write enable	x	x	x	x	x	x	1	x
VME-AM0 = 1, AM1 = 0	x	x	x	x	x	0	x	x
VME-AM0 = 0, AM1 = 1	x	x	x	x	x	1	x	x
VME-AM2 = 0	x	x	x	x	0	x	x	x
VME-AM2 = 1	x	x	x	x	1	x	x	x
user led 1 switch off	x	x	x	0	x	x	x	x
user led 1 switch on	x	x	x	1	x	x	x	x
user led 2 switch off	x	x	0	x	x	x	x	x
user led 2 switch on	x	x	1	x	x	x	x	x
user led 4 switch off	0	x	x	x	x	x	x	x
user led 4 switch on	1	x	x	x	x	x	x	x

Bit map of the (B)oard (S)tatus (R)e(g)ister:

BSRG @ CS6+$04	D0	D1	D2	D3	D4	D5	D6	D7
read only	SW3	SW2	SW1	IRMB	0	0	ARBE	0
System Controller	x	x	x	x	x	x	0	x
not System Controller	x	x	x	x	x	x	1	x
no mailbox write access occurred	x	x	x	0	x	x	x	x
mailbox write access occurred	x	x	x	1	x	x	x	x
MDCK link 1-2 installed	x	x	0	x	x	x	x	x
MDCK link 1-2 removed	x	x	1	x	x	x	x	x
MDCK link 3-4 installed	x	0	x	x	x	x	x	x
MDCK link 3-4 removed	x	1	x	x	x	x	x	x
MDCK link 5-6 installed	0	x	x	x	x	x	x	x
MDCK link 5-6 removed	1	x	x	x	x	x	x	x

Bit map of the (W)atch(D)og (R)etrigger (P)ort:

WDRP @ CS6+$05	D0	D1	D2	D3	D4	D5	D6	D7
write	retrigger watchdog timer							

Bit map of the (C)lear (M)ailbox (I)nterrupt (P)ort:

CMIP @ CS6+$06	D0	D1	D2	D3	D4	D5	D6	D7
write	clear mailbox IRQ							

Bit map of the (B)oard (R)evision (R)e(g)ister:

BRRG @ CS6+$07	D0	D1	D2	D3	D4	D5	D6	D7
Revsison 4	0	0	0	0	0	1	0	0

Bit map of the (V)MEbus (I)nterrupt (M)ask (R)egister:

VIMR @ CS6+$80	D0	D1	D2	D3	D4	D5	D6	D7
read/write	VIM7	VIM6	VIM5	VIM4	VIM3	VIM2	VIM1	BYMD
reset	0	0	0	0	0	0	0	0
VMEbus Byte Mode Enable	x	x	x	x	x	x	x	1
VMEbus Byte Mode Disable	x	x	x	x	x	x	x	0
VME-IRQ1 enable	x	x	x	x	x	x	1	x
VME-IRQ1 disable	x	x	x	x	x	x	0	x
VME-IRQ2 enable	x	x	x	x	x	1	x	x
VME-IRQ2 disable	x	x	x	x	x	0	x	x
VME-IRQ3 enable	x	x	x	x	1	x	x	x
VME-IRQ3 disable	x	x	x	x	0	x	x	x
VME-IRQ4 enable	x	x	x	1	x	x	x	x
VME-IRQ4 disable	x	x	x	0	x	x	x	x
VME-IRQ5 enable	x	x	1	x	x	x	x	x
VME-IRQ5 disable	x	x	0	x	x	x	x	x
VME-IRQ6 enable	x	1	x	x	x	x	x	x
VME-IRQ6 disable	x	0	x	x	x	x	x	x
VME-IRQ7 enable	1	x	x	x	x	x	x	x
VME-IRQ7 disable	0	x	x	x	x	x	x	x

Bit map of the (V)MEbus (I)nterrupt (S)tatus (R)egister:

VISR @ CS6+$81	D0	D1	D2	D3	D4	D5	D6	D7
read only	VIRQ7	VIRQ6	VIRQ5	VIRQ4	VIRQ3	VIRQ2	VIRQ1	---
VME-IRQ1 inactive	x	x	x	x	x	x	0	0
VME-IRQ1 active	x	x	x	x	x	x	1	0
VME-IRQ2 inactive	x	x	x	x	x	0	x	0
VME-IRQ2 active	x	x	x	x	x	1	x	0
VME-IRQ3 inactive	x	x	x	x	0	x	x	0
VME-IRQ3 active	x	x	x	x	1	x	x	0
VME-IRQ4 inactive	x	x	x	0	x	x	x	0
VME-IRQ4 active	x	x	x	1	x	x	x	0
VME-IRQ5 inactive	x	x	0	x	x	x	x	0
VME-IRQ5 active	x	x	1	x	x	x	x	0
VME-IRQ6 inactive	x	0	x	x	x	x	x	0
VME-IRQ6 active	x	1	x	x	x	x	x	0
VME-IRQ7 inactive	0	x	x	x	x	x	x	0
VME-IRQ7 active	1	x	x	x	x	x	x	0

Bit map of the (L)ocal (I)nterrupt (M)ask (R)egister:

LIMR @ CS6+$82	D0	D1	D2	D3	D4	D5	D6	D7
read/write	VACF	PMC	VSYF	ISCM	IRTC	IFDC	IMBX	IABO
reset	0	0	0	0	0	0	0	0
ABORT key IRQ disable	x	x	x	x	x	x	x	0
ABORT key IRQ enable	x	x	x	x	x	x	x	1
Mailbox IRQ disable	x	x	x	x	x	x	0	x
Mailbox IRQ enable	x	x	x	x	x	x	1	x
FDC IRQ disable	x	x	x	x	x	0	x	x
FDC IRQ enable	x	x	x	x	x	1	x	x
RTC IRQ disable	x	x	x	x	0	x	x	x
RTC IRQ enable	x	x	x	x	1	x	x	x
LM81 IRQ disable	x	x	x	0	x	x	x	x
LM81 IRQ enable	x	x	x	1	x	x	x	x
VME-SYS-Fail disable	x	x	0	x	x	x	x	x
VME-SYS-Fail enable	x	x	1	x	x	x	x	x
PMC IRQ disable	x	0	x	x	x	x	x	x
PMC IRQ enable	x	1	x	x	x	x	x	x
VME-AC-Fail disable	0	x	x	x	x	x	x	x
VME-AC-Fail enable	1	x	x	x	x	x	x	x

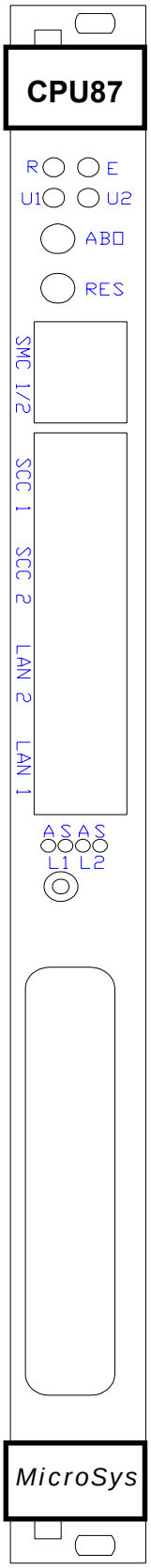
Bit map of the (L)ocal (I)nterrupt (S)tatus (R)egister:

LISR @ CS6+$83	D0	D1	D2	D3	D4	D5	D6	D7
read only	VACF	---	VSYF	ISCM	IRTC	IFDC	IMBX	IABO
Abort Key inactive	x	0	x	x	x	x	x	0
Abort Key active	x	0	x	x	x	x	x	1
Mailbox IRQ inactive	x	0	x	x	x	x	0	x
Mailbox IRQ active	x	0	x	x	x	x	1	x
FDC IRQ inactive	x	0	x	x	x	0	x	x
FDC IRQ active	x	0	x	x	x	1	x	x
RTC IRQ inactive	x	0	x	x	0	x	x	x
RTC IRQ active	x	0	x	x	1	x	x	x
LM81 IRQ inactive	x	0	x	0	x	x	x	x
LM81 IRQ active	x	0	x	1	x	x	x	x
VME-Sys-Fail inactive	x	0	0	x	x	x	x	x
VME-Sys-Fail active	x	0	1	x	x	x	x	x
VME-AC-Fail inactive	0	0	x	x	x	x	x	x
VME-AC-Fail active	1	0	x	x	x	x	x	x

Bit map of the (P)MC (I)nterrupt (S)tatus (R)egister:

PISR @ CS6+$84	D0	D1	D2	D3	D4	D5	D6	D7
read only	INTD	INTC	INTB	INTA	0	0	0	0
PMC IRQ-A inactive	x	x	x	0	x	x	x	x
PMC IRQ-A active	x	x	x	1	x	x	x	x
PMC IRQ-B inactive	x	x	0	x	x	x	x	x
PMC IRQ-B active	x	x	1	x	x	x	x	x
PMC IRQ-C inactive	x	0	x	x	x	x	x	x
PMC IRQ-C active	x	1	x	x	x	x	x	x
PMC IRQ-D inactive	0	x	x	x	x	x	x	x
PMC IRQ-D active	1	x	x	x	x	x	x	x

8. Front Panel Description



8.1 Front Leds

There are three user programmable leds, a processor RUN indicating led and four LAN status leds located on the front panel of the CPU87.

8.1.1.1 The User Programmable Leds

These leds can be controlled via the (B)oard (C)ontrol (R)e(g)ister at location **CS6** offset **$03**. The BCR contains three high active bits for the led control, two VME address modifier control bits and two protection bits, used for the 64bit flash bank. The BCRG can be read back for verification. After a reset, all bits are set to low and all leds are deactivated.

Bit map of the (B)oard (C)ontrol (R)e(g)ister:

BCRG @ CS6+$03	**D0**	**D1**	**D2**	**D3**	D4	D5	D6	D7
read/write	**ULED3**	**---**	**ULED2**	**ULED1**	AM2	AM0/1	FWRE	FWPT
reset	0	0	0	0	0	0	0	0
user led 1 switch off	x	x	x	**0**	x	x	x	x
user led 1 switch on	x	x	x	**1**	x	x	x	x
user led 2 switch off	x	x	**0**	x	x	x	x	x
user led 2 switch on	x	x	**1**	x	x	x	x	x
user led 4 switch off	**0**	x	x	x	x	x	x	x
user led 4 switch on	**1**	x	x	x	x	x	x	x

8.1.1.2 The Network Status Leds

There are two network front panel status LEDs for each channel, which can be programmed via the management data port within the LED configuration register of each LXT971.

8.1.2 Front Switches

The **RESET** switch performs a hardware reset to the CPU87.

The **ABORT** switch generates a low active interrupt to the MPC8270 on the **IRQ1** line.

9. The Mezzanine Slot

The CPU87 supports an extension slot for mezzanine boards with PMC form factor. The interface to this extension depends on the type of processor mounted on the CPU87. With the standard **MPC8260** CPU **only** the **Local Bus** signals are available. To use the **PCI** interface for PMC modules a **MPC8250 CPU** type is necessary.

9.1 The Local Bus Module Slot

The Local Bus module slot uses the connectors ST9 and ST10. The bus signals and power pins are available on ST10. The mezzanine I/O lines are connected via ST9 to the rows D & E of the VG160 connector ST2.

9.2 The Local Bus Connector Pin out

ST10			
+12V	**1**	**2**	**GND**
GND	**3**	**4**	**-12V**
+5V	**5**	**6**	**GND**
GND	**7**	**8**	**+3.3V**
REQ1#	**9**	**10**	**GND**
GNT0#	**11**	**12**	**PBXCLK**
GNT1#	**13**	**14**	**LGPL0**
GNT2#	**15**	**16**	**LGPL1**
PRST#	**17**	**18**	**LGPL2**
INTA	**19**	**20**	**LGPL3**
REQ2#	**21**	**22**	**LGPL4**
LA31	**23**	**24**	**LGPL5**
GND	**25**	**26**	**IRDY#**
AD0	**27**	**28**	**STOP#**
AD1	**29**	**30**	**DVSL#**
AD2	**31**	**32**	**IDSL**
AD3	**33**	**34**	**PERR#**
AD4	**35**	**36**	**SERR#**
AD5	**37**	**38**	**REQ0#**
AD6	**39**	**40**	**CS11#**
AD7	**41**	**42**	**LSDQM0#**
GND	**43**	**44**	**LSDQM1#**
AD8	**45**	**46**	**LSDQM2#**
AD9	**47**	**48**	**LSDQM3#**
AD10	**49**	**50**	**LWR#**
AD11	**51**	**52**	**CBE0#**
AD12	**53**	**54**	**CBE1#**
AD13	**55**	**56**	**CBE2#**
AD14	**57**	**58**	**CBE3#**
AD15	**59**	**60**	**GND**
GND	**61**	**62**	**+3.3V**
+5V	**63**	**64**	**GND**

9.3 The Local Bus and PMC I/O Connector Pin out

ST2	ST9		ST2
d1	1	2	e1
d2	3	4	e2
d3	5	6	e3
d4	7	8	e4
d5	9	10	e5
d6	11	12	e6
d7	13	14	e7
d8	15	16	e8
d9	17	18	e9
d10	19	20	e10
d11	21	22	e11
d12	23	24	e12
d13	25	26	e13
d14	27	28	e14
d15	29	30	e15
d16	31	32	e16
d17	33	34	e17
d18	35	36	e18
d19	37	38	e19
d20	39	40	e20
d21	41	42	e21
d22	43	44	e22
d23	45	46	e23
d24	47	48	e24
d25	49	50	e25
d26	51	52	e26
d27	53	54	e27
d28	55	56	e28
d29	57	58	e29
d30	59	60	e30
d31	61	62	e31
d32	63	64	e32

9.4 The PMC Module Slot

The PMC module slot uses the connectors ST7, ST8 and ST9. The PCI configuration space is decoded by AD13 for this slot. The PMC I/O lines are connected via ST9 to the rows D & E of the VG160 connector ST2.

Attention !

Standard PMC modules work ONLY with processors offering PCI bus, i.e. MPC8250, MPC8265, MPC8266, MPC8270 and MPC8280. The MPC8260, however, does not support standard PMC/PCI support! Using PMC cards on a system with MPC8260 may cause permanent damage to the board and/or the whole system !

9.5 The PMC PCI Connector Pin out

ST7			
TCK	1	2	-12V
GND	3	4	INTA#
INTB#	5	6	INTC#
---	7	8	VCC
INTD#	9	10	---
GND	11	12	---
CLKB	13	14	GND
GND	15	16	GNT1#
REQ1#	17	18	VCC
VCC	19	20	AD31
AD28	21	22	AD27
AD25	23	24	GND
GND	25	26	CBE3#
AD22	27	28	AD21
AD19	29	30	VCC
VCC	31	32	AD17
FRAME#	33	34	GND
GND	35	36	IRDY#
DEVSEL#	37	38	VCC
GND	39	40	LOCK#
SDONE	41	42	SBO#
PAR	43	44	GND
VCC	45	46	AD15
AD12	47	48	AD11
AD9	49	50	VCC
GND	51	52	CBE0#
AD6	53	54	AD5
AD4	55	56	GND
VCC	57	58	AD3
AD2	59	60	AD1
AD0	61	62	VCC
GND	63	64	REQ64#

ST8			
+12V	1	2	TRST#
---	3	4	---
---	5	6	GND
GND	7	8	---
---	9	10	---
---	11	12	VDD
RESET#	13	14	---
VDD	15	16	---
---	17	18	GND
AD30	19	20	AD29
GND	21	22	AD26
AD24	23	24	VDD
IDSEL	25	26	AD23
VDD	27	28	AD20
AD18	29	30	GND
AD16	31	32	CBE2#
GND	33	34	---
TRDY#	35	36	VDD
GND	37	38	STOP#
PERR#	39	40	GND
VDD	41	42	SERR#
CBE1#	43	44	GND
AD14	45	46	AD13
GND	47	48	AD10
AD8	49	50	VDD
AD7	51	52	---
VDD	53	54	---
---	55	56	GND
---	57	58	---
GND	59	60	---
---	61	62	VDD
GND	63	64	---

(„---“ marked pins are not connected)

10. The ispLSI Programming Port

The programmable logic onboard the CPU87 can be modified or updated via a PC controlled programming interface. The ISP programming port contains the necessary lines for serial a programming of all ispLSI devices. Besides the programming option, also a JTAG mode is available for the ispLSI devices in hardware or emulation mode.

The pin assignment of the ISP port is shown in the following table:

Connector ISP		
Pin:	**Signal:**	**Description:**
1	VDD	3,3 Volts
2	SDO/TDO	serial data out
3	SDI/TDI	serial data in
4	ispEN	program enable
5	no pin	keyed
6	MODE/TMS	mode control in
7	GND	Ground
8	SCLK/TCLK	serial clock in

Attention !

Please contact MicroSys before attaching this interface!

11. Summary of Jumpers

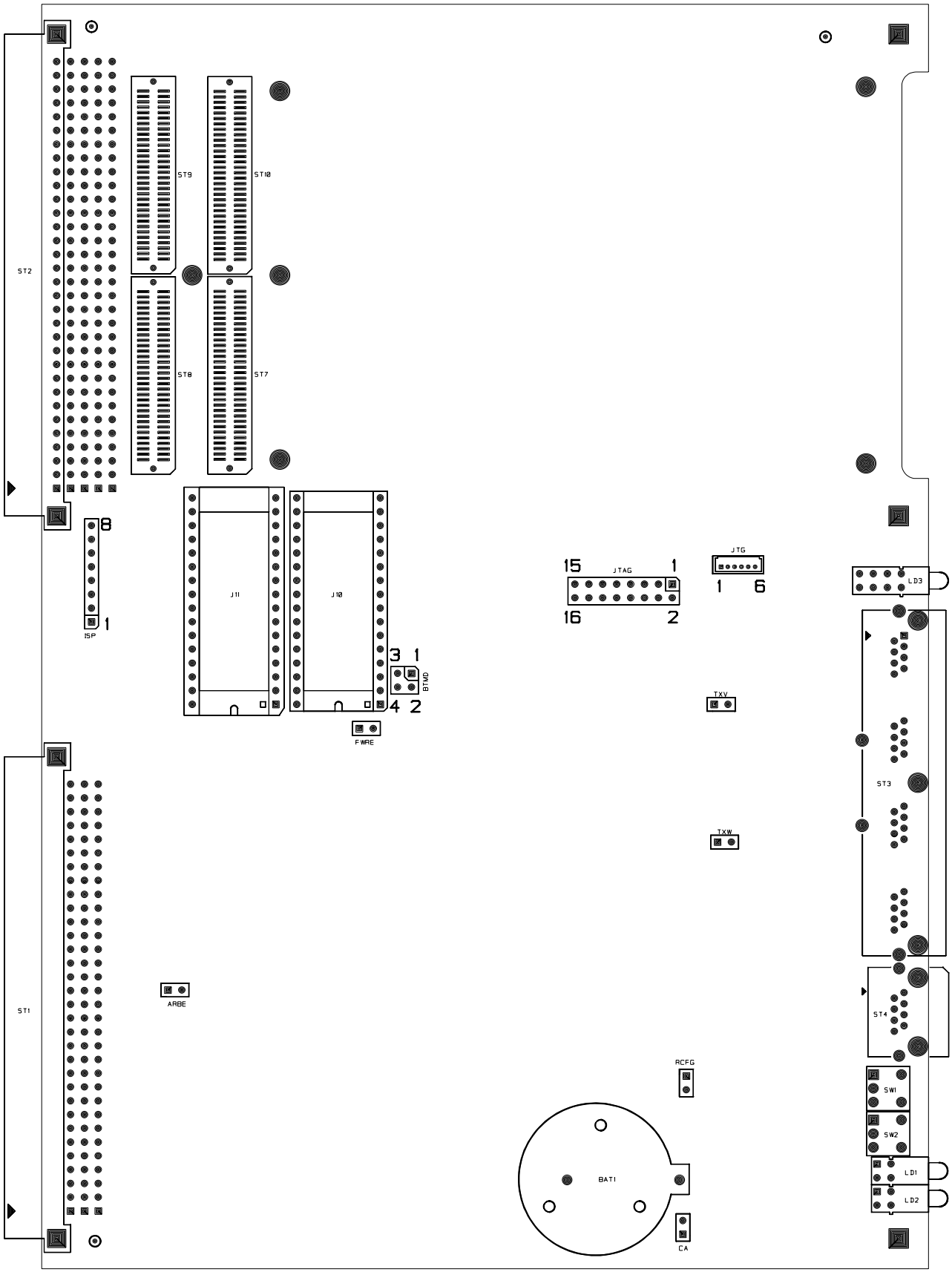
Described function is valid, when jumper is set or link is intact !

Size:	Name:	Default:	Position:	Function:
1x2	ARBE	#	1-2	System Controller Function Enable
			---	System Controller Function Disable
1x5	BA		1-2	Boot ROM Pin 1 to Vcc
			2-3	Boot ROM Pin 1 to A19
		#	4-5	Boot ROM Pin 1 to A18
1x3	BB		1-2	Boot ROM Pin 30 to Vcc
		#	2-3	Boot ROM Pin 30 to A17
1x5	BC		1-2	Boot ROM Pin 31 to Vcc
			2-3	Boot ROM Pin 31 to A18
		#	4-5	Boot ROM Pin 31 to RW
1x2	CA		1-2	Lithium battery connected
		#	---	Lithium battery disconnected
1x3	FA		1-2	flash bank: ADV connected to CS [1])
		#	2-3	flash bank: ADV connected to GND [1])
1x2	JTE	#	1-2	LXT971-TRST# connected to GND
				LXT971-TRST# open
3x2	MDCK		1-2	MPC8270-MODCK1 = high
		#	3-4	MPC8270-MODCK2 = low
		#	5-6	MPC8270-MODCK3 = low
1x2	PLL		1-2	Source Clock PLL link through
		#	---	Source Clock PLL enable
1x2	RCFG	#	1-2	external configuration MPC8270
			---	internal default configuration MPC8270 **(usable only when booting from 64Bit Flash !)**
1x2	TXV	#	1-2	10/100BaseT Channel-A TX CT voltage set

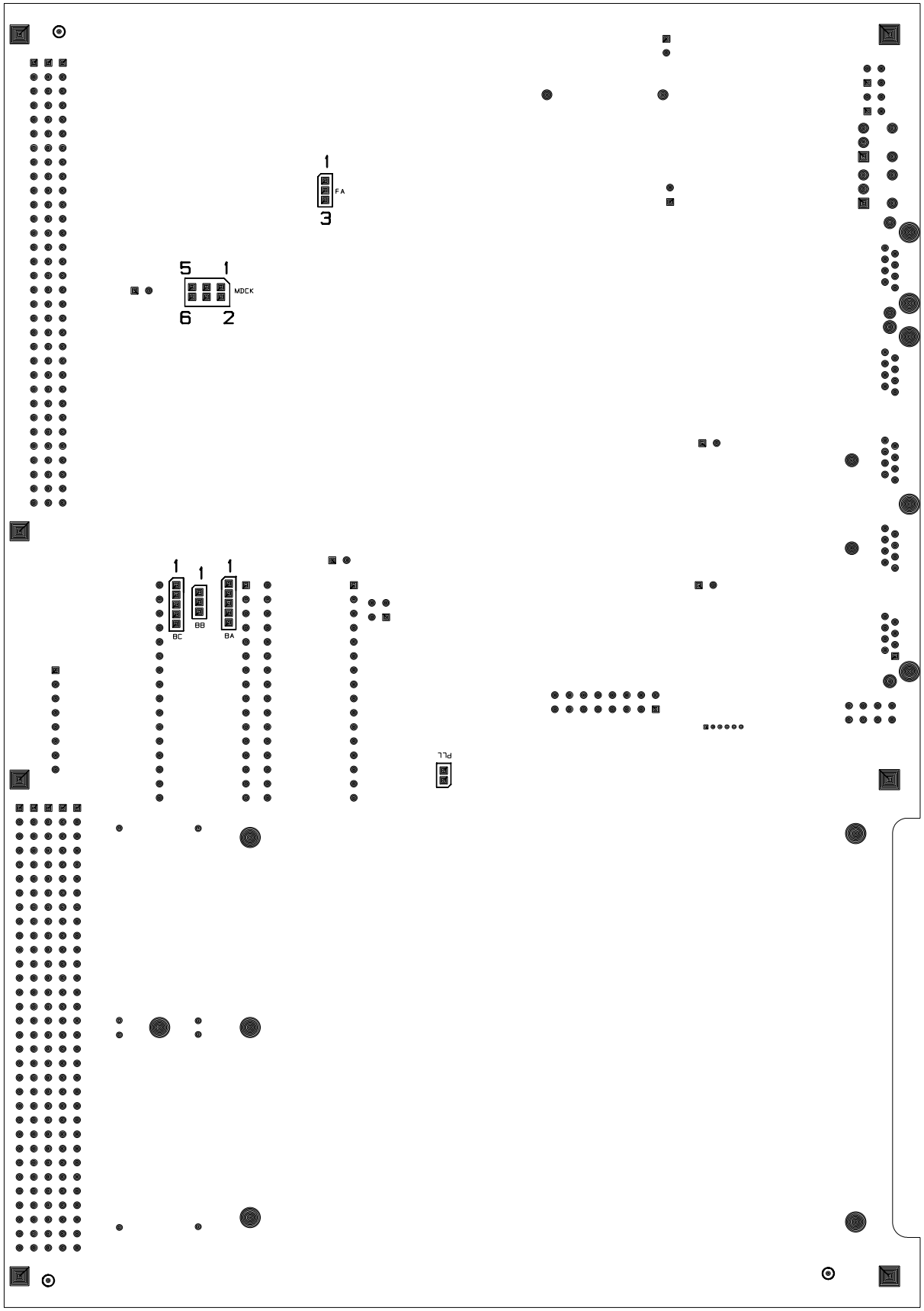
1x2	TXW	#	1-2	10/100BaseT Channel-B TX CT voltage set
			---	

[1]) Factory setting dependent on Flash types mounted. Must not be changed!

11.1 Jumpers Component Side

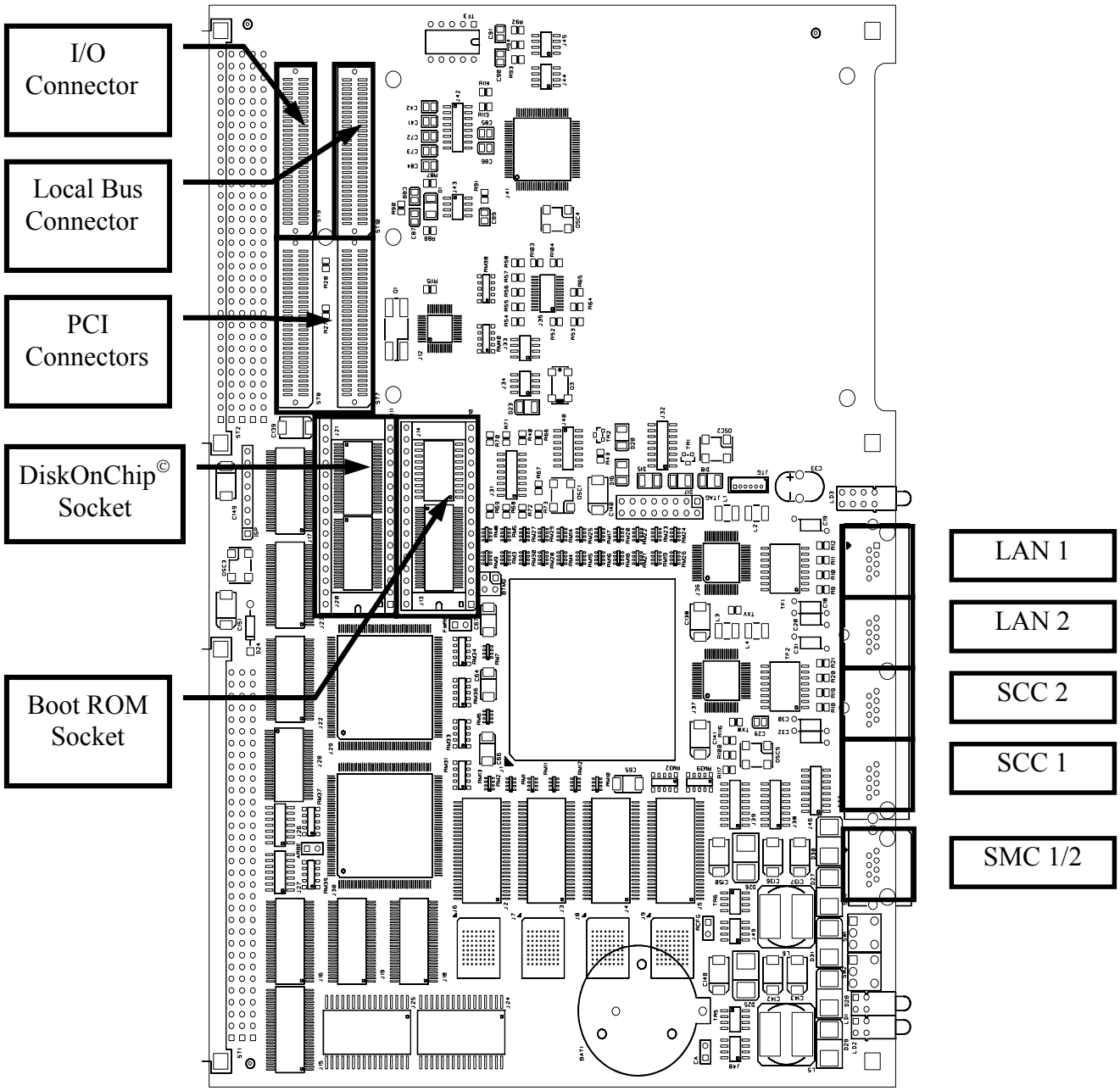


11.2 Jumpers Solder Side

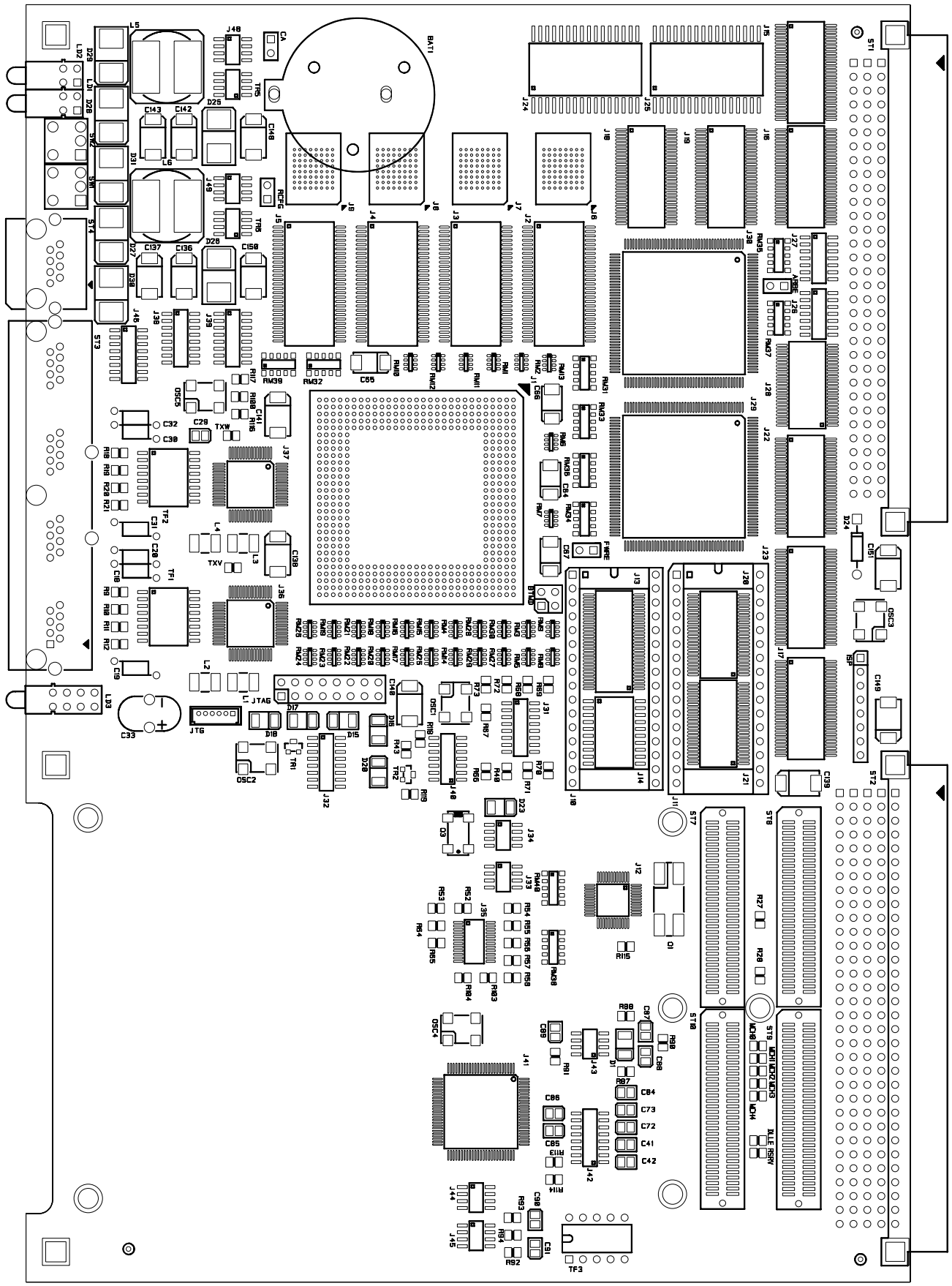


Appendices

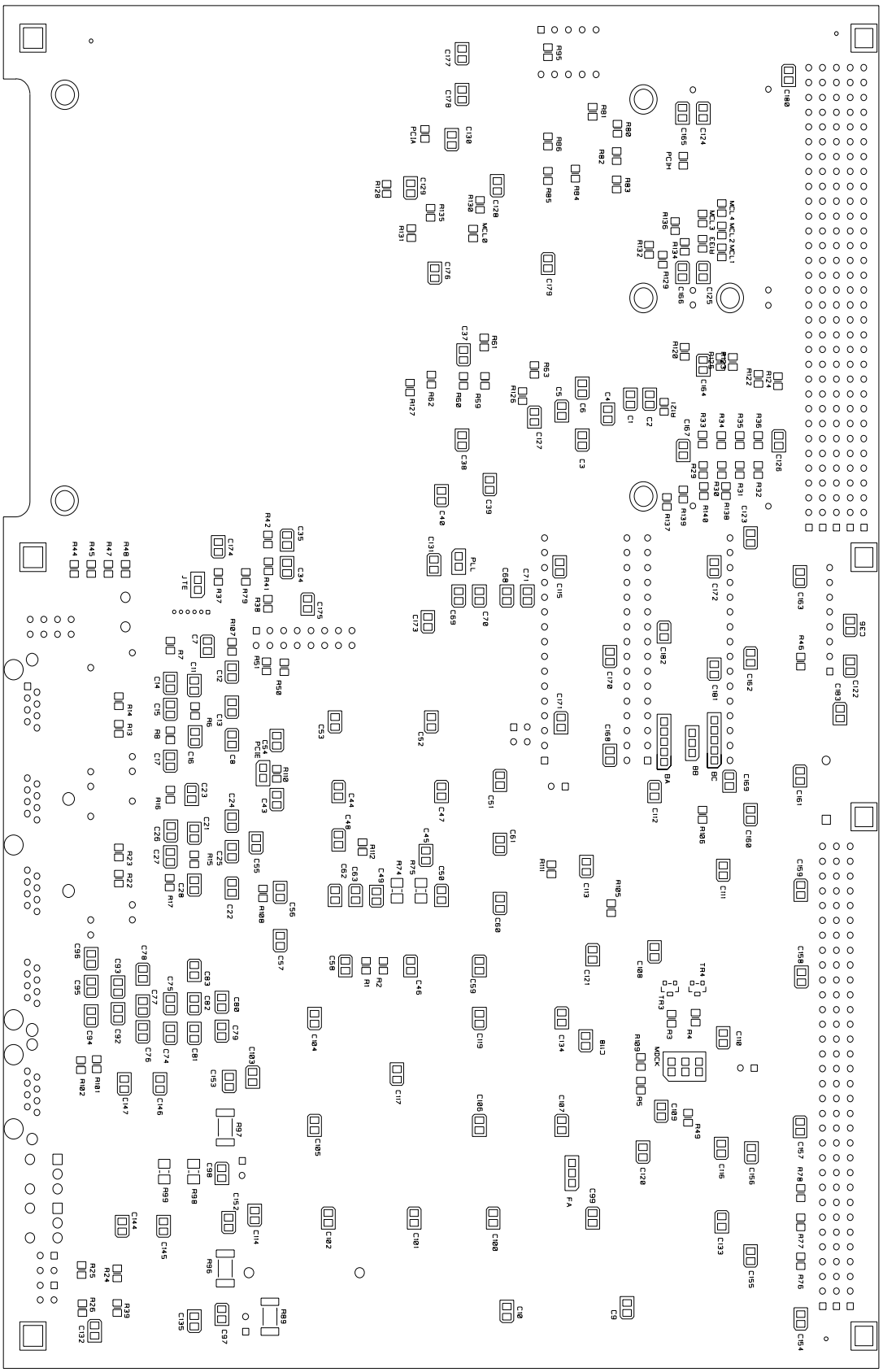
Appendix A: I/O Connector Overview



Appendix B: Layout Component Side



Appendix C: Layout Solder Side



Appendix D: Schematics CPU87 (on request)