TQMLS102xA
Preliminary User's Manual

TQMLS102xA UM 0002
26.05.2015

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TABLE DIRECTORY

ILLUSTRATION DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMLS102xA and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the used modules:**
  These documents describe the service, functionality and special characteristics of the used module (incl. BIOS).
- **Specifications of the used components:**
  The manufacturer's specifications of the used components, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- Circuit diagram MBLS102xA
- Documentation of boot loader U-Boot (http://www.denx.de/wiki/U-Boot/Documentation)
- Documentation of PTXdist (http://www.ptxdist.de)

2. BRIEF DESCRIPTION

This Preliminary User's Manual describes the TQMLS102xA, and refers to some software settings.
A certain derivative of the TQMLS102xA does not necessarily provide all features described in this User's Manual.
This Preliminary User's Manual does also not replace the Freescale Reference Manuals of the CPU.
The TQMLS102xA is a universal Minimodule based on the Freescale ARM CPU Dual Cortex A7 with QorIQ technology (Layerscape). The Cortex A7 cores of this CPU are clocked with up to 1 GHz.
The TQMLS102xA extends the TQC product range and offers an outstanding computing performance.
A suitable CPU derivative (LS1020, LS1021, and LS1022) can be selected for each requirement.

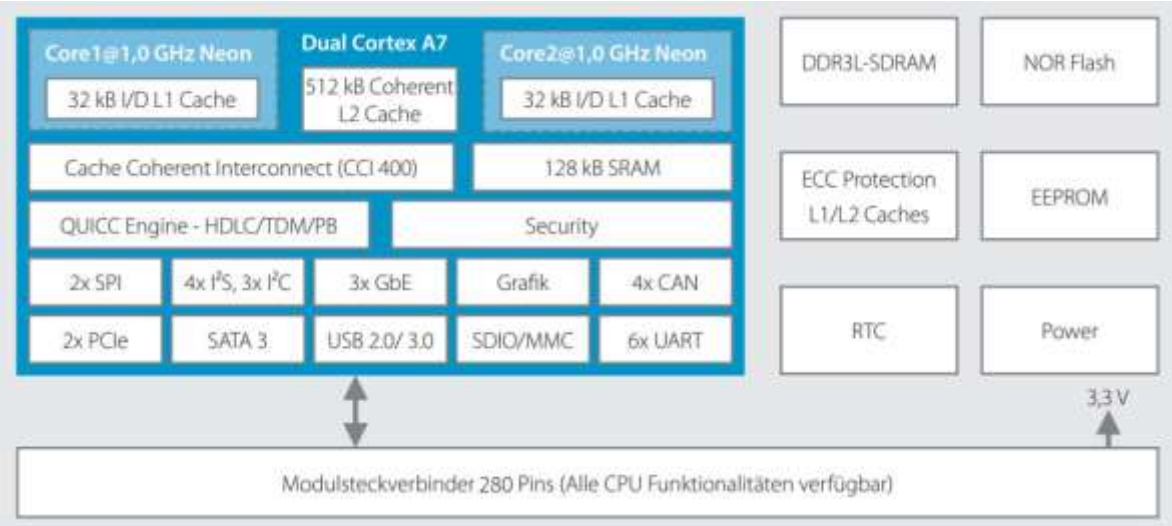


Illustration 1: Block diagram TQMLS102xA (simplified)

Attention: Malfunction	
	The SERDES lines are multiplexed and can therefore not be used simultaneously.

2.1 Key functions and characteristics

The TQMLS102xA provides the following key functions and characteristics:

- Graphics
- SD card interface
- On-Board flash (NOR, eMMC, NAND)
- DDR3L SDRAM
- USB 2.0 Hi-Speed interface with PHY
- USB 3.0 Hi-Speed interface with PHY
- Ethernet 10/100/1000
- CAN
- SATA
- PCIe
- I²C, I²S, SPI, UART
- RTC (optional)
- Software support possible for:
  - Linux
  - VxWorks
  - QNX
  - PikeOS

All essential CPU pins are routed to the connectors.
There are therefore no restrictions for customers using the TQMLS102xA with respect to an integrated customised design.

2.2 Available versions

The default versions offer the following basic features:

- CPUs: LS1020, LS1021, LS1022
- DDR3/4L-RAM: 1 Gbyte + ECC
- QSPI NOR flash: 512 Mbyte
- EEPROM: 64 kbit

All versions of the TQMLS102xA are fully pin-compatible and therefore interchangeable.
The functionality of the different TQMLS102xA is mainly determined by the features provided by the respective CPU.

3. ELECTRONICS SPECIFICATION

The information in this User's Manual is only valid in connection with the boot loader adapted for the TQMLS102xA, which is preinstalled on every TQMLS102xA (see also section 6) and the BSP provided by TQ-Systems GmbH.

3.1 System overview

3.1.1 System architecture / block diagram

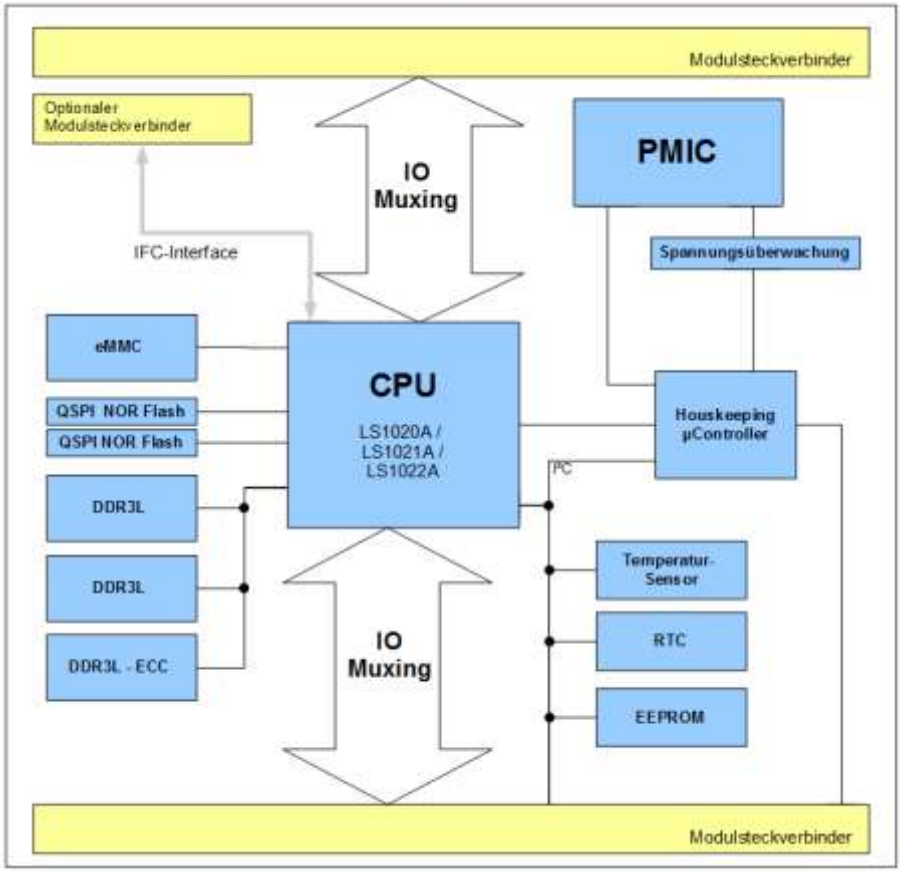


Illustration 2: Block diagram TQMLS102xA

3.1.2 System components

- CPU: LS1020A / LS1021A / LS1022A
- DDR3L SDRAM
- On-board flash (NOR and eMMC)
- Power supply
- Voltage supervision
- Power management or Housekeeping Microcontroller (PMC)
- RTC
- Temperature sensor
- EEPROM

All CPU pins with useful functionality are routed to the connectors.

3.2 CPU LS102xA

3.2.1 CPU versions

The following CPUs from the LS102x family are used for the TQMLS102xA:

- LS1020A
- LS1021A
- LS1022A

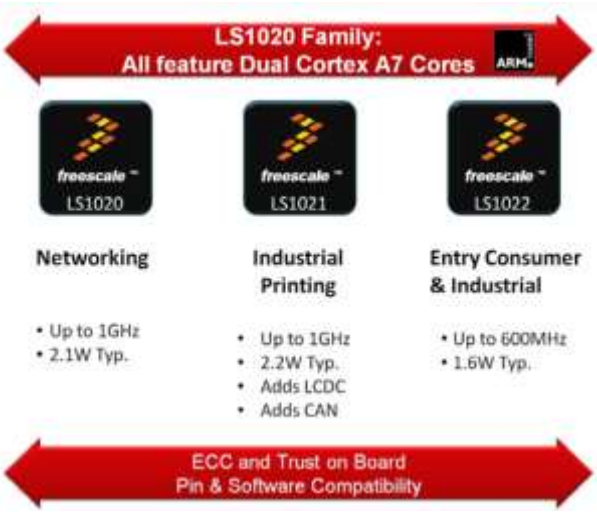


Illustration 3: TQMLS102xA product family

In the following tables more details of the different features is shown.

Table 2: Functional differences of the LS102x family CPUs

Function			LS1021A	LS1020A	LS1022A
DDR	Type	DDR3L	Yes	Yes	Yes
		DDR4	Yes	Yes	No
	Data Bus I/F	8-bit	Yes	Yes	Yes
		16-bit	Yes	Yes	Yes
		32-bit	Yes	Yes	No
		ECC	Yes	Yes	Yes
IFC	Controller	NAND	Yes	Yes	Yes
		NOR	Yes	Yes	Yes
		QSPI	2	2	2
		GPCM	Yes	Yes	Yes
		GASIC	Yes	Yes	Yes
	Data Bus I/F	16-bit	Yes	Yes	Yes
SERDES	Lanes		4	4	1
PCIe		PCIe	2	2	1
SATA		SATA	1	1	0
Ethernet	Controller	EC1	Yes	Yes	Yes
		EC2	Yes	Yes	Yes
		EC3	Yes	Yes	No
	Interface	SGMII	2	2	0
		RGMII	3	3	2
		MII	2	2	2
		IEEE 1588	1	1	1
SD		eSDHC	Yes	Yes	Yes
USB 3.0	[PHY]	USB 3.0	Yes	Yes	No
	[PHY]	USB 2.0	Yes	Yes	No
USB 2.0	No PHY	USB 2.0	Yes	Yes	Yes
Low Power UART	4-wire	LPUART1	Yes	Yes	Yes
	4-wire	LPUART2	Yes	Yes	Yes
	4-wire	LPUART3	Yes	Yes	Yes
	2-Wire	LPUART4	Yes	Yes	Yes
	2-Wire	LPUART5	Yes	Yes	Yes
	2-Wire	LPUART6	Yes	Yes	Yes
UART	4-wire	UART1	Yes	Yes	Yes
	4-wire	UART2	Yes	Yes	Yes
	2-Wire	UART3	Yes	Yes	Yes
	2-Wire	UART4	Yes	Yes	Yes
IIC		IIC1	Yes	Yes	Yes
		IIC2	Yes	Yes	Yes
		IIC3	Yes	Yes	Yes
SPI		SPI1	Yes	Yes	Yes
		SPI2	Yes	Yes	Yes
CAN		CAN1	Yes	Yes	Yes
		CAN2	Yes	Yes	Yes
		CAN3	Yes	Yes	Yes
		CAN4	Yes	Yes	Yes
LCD		LCD	Yes	No	No

Table 2: Functional differences of the LS102x family CPUs (continued)

Flex Timer	FTM1	Channel[0:7]	Yes	Yes	Yes
		Clock in	Yes	Yes	Yes
		Fault	Yes	Yes	Yes
		QD Phase A + B	Yes	Yes	Yes
	FTM2	Channel[0:7]	Yes	Yes	Yes
		Clock in	Yes	Yes	Yes
		Fault	Yes	Yes	Yes
		QD Phase A + B	Yes	Yes	Yes
	FTM3	Channel[0:7]	Yes	Yes	Yes
		Clock in	Yes	Yes	Yes
		Fault	Yes	Yes	Yes
		QD Phase A + B	Yes	Yes	Yes
	FTM4	Channel[0:7]	Yes	Yes	Yes
		Clock in	Yes	Yes	Yes
		Fault	Yes	Yes	Yes
		QD Phase A + B	Yes	Yes	Yes
	FTM5	Channel[0:1]	Yes	Yes	Yes
	FTM6	Channel[0:1]	Yes	Yes	Yes
	FTM7	Channel[0:1]	Yes	Yes	Yes
	FTM8	Channel[0:1]	Yes	Yes	Yes
Audio	I2S	SAI1	Yes	Yes	Yes
		SAI2	Yes	Yes	Yes
		SAI3	Yes	Yes	Yes
		SAI4	Yes	Yes	Yes
		SPDIF	Yes	Yes	Yes
uQE	output	BRGO[1:4]	Yes	Yes	No
	Input	CLK[9:12]	Yes	Yes	No
	TDM/HDLC	TDMA	Yes	Yes	No
		TDMB	Yes	Yes	No
		UCC1	Yes	Yes	No
		UCC3	Yes	Yes	No

The LS1022A CPU contains some function blocks like both other CPUs, but a lower number of the corresponding blocks, see following table:

Table 3: LS102x function blocks

Function		LS1021A	LS1020A	LS1022A
DDR		32-bit 3L/4	32-bit 3L/4	16-bit 3L
LCD		1	0	0
SERDES	Lanes	4	4	1
	PCIe	2	2	1
	SGMII	2	2	0
	SATA	1	1	0
Ethernet	EC	[1:3]	[1:3]	[1:2]
	RGMII	3	3	2
	MII	2	2	2
	IEE 1588	1	1	1
USB	USB3.0	1	1	0
	USB2.0	1	1	1
CAN		4	4	4
LPUART	2/4-wire	3 / 3	3 / 3	3 / 3
UART	2/4-wire	2 / 2	2 / 2	2 / 2
IIC		3	3	3
SPI		2	2	2
FTM		[1:8]	[1:8]	[1:8]
Audio	SAI (I2S)	[1:4]	[1:4]	[1:4]
	SPDIF	1	1	1
SD	eSDHC	1	1	1
IFC	NAND	1	1	1
	NOR	1	1	1
	QSPI	2	2	2
	GPSM	1	1	1
	GASIC	1	1	1
uQE		Yes	Yes	No
	TRUST	Yes		
	IRQ			
	EVENTS			
	RTC			

In this User's Manual the TQMLS102xA is referred to, since it offers the greatest expansion stage.

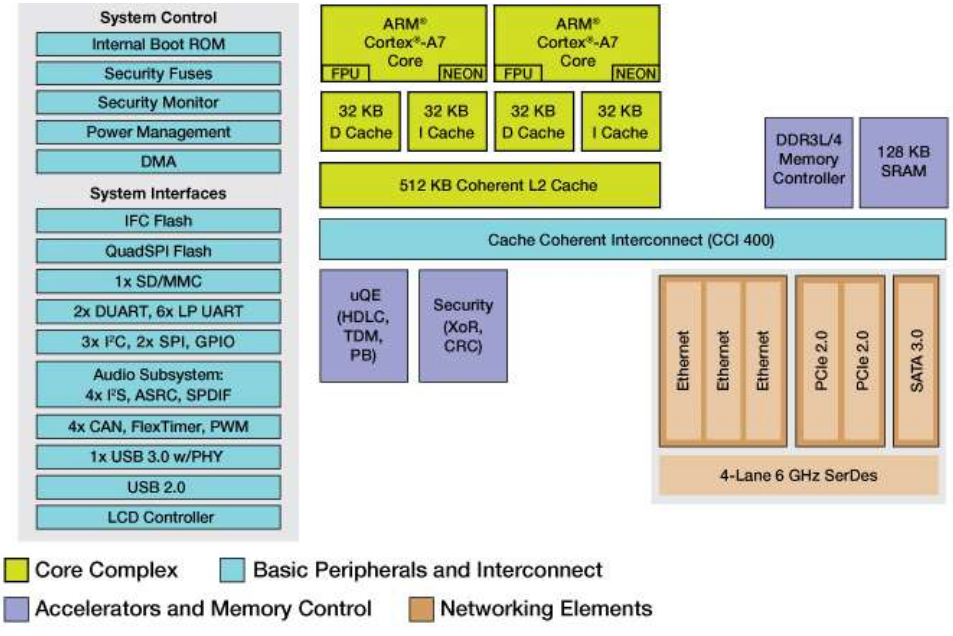


Illustration 4: LS1021A CPU Block diagram

3.2.2 Boot options

The LS102x provides the following boot options:

- Parallel NOR flash
- NAND flash
- QSPI
- SD/MMC (eSDHC)

The SDHC interface is part of the pin-multiplexing and routed to the connectors.

The boot options Parallel NOR, NAND and QSPI are connected via the configurable IFC interface.
The serial NOR flash on the TQMLS102xA is connected via QSPI (see 3.4).
The whole IFC interface is routed to a connector to use the CPU to its full extent.
The IFC interface also offers the option to run a parallel bus (NOR / NAND / GPCM / GASIC).

The multiplexing is configured to boot the TQMLS102xA from the On-Board SPI flash.

Table 4: Configuration of the boot source

Signal		Parallel NOR 8 bit	Parallel NOR 16 bit	QSPI	SDHC
IFC_AD08	cfg_rcw_src0	0	0	0	0
IFC_AD09	cfg_rcw_src1	0	0	0	0
IFC_AD10	cfg_rcw_src2	0	0	1	1
IFC_AD11	cfg_rcw_src3	0	1	0	0
IFC_AD12	cfg_rcw_src4	1	0	0	0
IFC_AD13	cfg_rcw_src5	X	X	0	0
IFC_AD14	cfg_rcw_src6	X	X	1	0
IFC_AD15	cfg_rcw_src7	X	X	0	0
IFC_CLE	cfg_rcw_src8	X	X	X	0

The QSPI interfaces 1 and 2 are routed to the connector as well. Depending on how the QSPI interface is used, SPI1 and I²C_3 are available by suitable multiplexing. These signals are also routed to the connector.

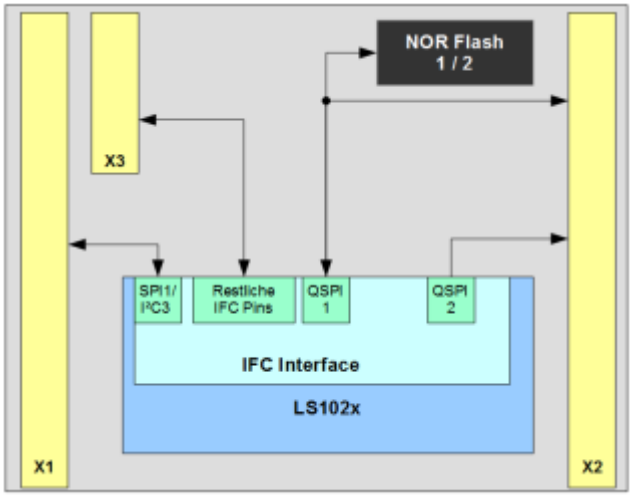


Illustration 5: IFC interface at the connector

If the IFC interface is not used, because the TQMLS102xA only boots from NOR flash, some pins of this interface can be configured as GPIOs by suitable pin multiplexing. These are available at the connectors.

The POR pin strapping-pins according to Table 4 define the source for the RCW (Reset Configuration Word).

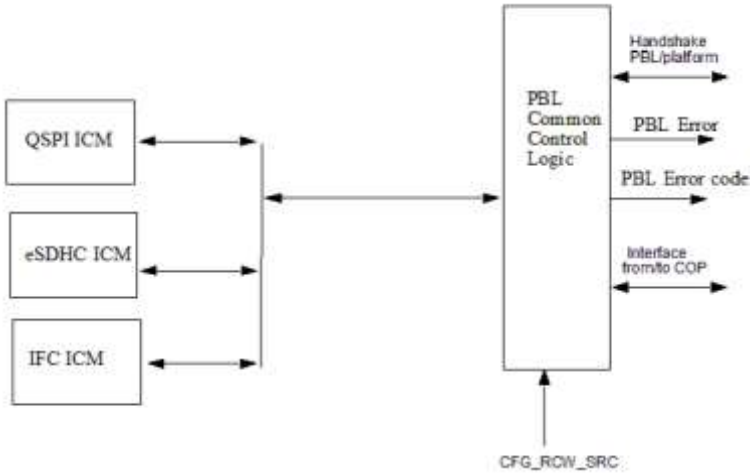


Illustration 6: Block diagram PBL

The following configuration pins are used as follows:

Table 5: Further configuration pins with optional wiring

Configuration	Signal	Implementation
cfg_ifc_te	IFC_TE	Required for IFC Boot Sets the polarity Signal at optional X3, but with active pin strapping on the TQMLS102xA
cfg_dram_type	IFC_A21	Defines the type of DDR Active pin strapping on the TQMLS102xA, fix configured to DDR3L
cfg_gpinput[0:7]	IFC_AD[0:7]	Available at X3 No PU/PD option on the TQMLS102xA planned Default value „1111 1111“

3.2.3 Multiplexing

Freescale provides a pin multiplexing table in Excel format for registered users:

Table 6: Pin multiplexing options

Ball	Power Rail	EC1	RCW[EC1] = 36'000 RGMII 1		RCW[EC1] = 36'001 GPIO3[2:14]		RCW[EC1] = 36'010 CAN[1:2]		RCW[EC1] = 36'011 MII 1		RCW[EC1] = 36'100 SAI[1:2]		RCW[EC1] = 36'101 FTM1
W5	LVDD	EC1_TXD3		GPIO3_02		CAN2_TX		EC1_TXD3		SAI1_TX_DATA		FTM1_CH5	
AA5	LVDD	EC1_TXD2		GPIO3_03		CAN1_TX		EC1_TXD2		SAI2_TX_DATA		FTM1_CH7	
Y6	LVDD	EC1_TXD1		GPIO3_04		-		EC1_TXD1		SAI1_TX_SYNC		FTM1_CH3	
AA6	LVDD	EC1_TXD0		GPIO3_05		-		EC1_TXD0		SAI2_TX_SYNC		FTM1_CH2	
W6	LVDD	EC1_TX_EN		GPIO3_06		-		EC1_TX_EN		SAI1_TX_BCLK		FTM1_FAULT	
Y7	LVDD	EC1_GTX_CLK	OR	GPIO3_07	OR	-	OR	EC1_TX_CLK	OR	SAI2_TX_BCLK	OR	FTM1_EXTCLK	
AA4	LVDD	EC1_GTX_CLK125		GPIO3_08		-		EC1_RX_ER		EXT_AUDIO_MCLK2		-	
AB4	LVDD	EC1_RXD3		GPIO3_09		CAN2_RX		EC1_RXD3		SAI1_RX_DATA		FTM1_CH4	
AC4	LVDD	EC1_RXD2		GPIO3_10		CAN1_RX		EC1_RXD2		SAI2_RX_DATA		FTM1_CH6	
AC5	LVDD	EC1_RXD1		GPIO3_11		-		EC1_RXD1		SAI1_RX_SYNC		FTM1_CH1	
AB6	LVDD	EC1_RXD0		GPIO3_12		-		EC1_RXD0		SAI2_RX_SYNC		FTM1_CH0	
AC3	LVDD	EC1_RX_CLK		GPIO3_13		-		EC1_RX_CLK		SAI1_RX_BCLK		FTM1_QD_PHA	
AC6	LVDD	EC1_RX_DV		GPIO3_14		-		EC1_RX_DV		SAI2_RX_BCLK		FTM1_QD_PHB	
		EC2	RCW[EC2] = 36'000 RGMII 2		RCW[EC2] = 36'001 GPIO3[15:27]		RCW[EC2] = 36'010 CAN[3:4]		RCW[EC2] = 36'011 MII 1		RCW[EC2] = 36'100 USB2 (USB 2.0)		RCW[EC2] = 36'101 FTM2
R4	LVDD	EC2_TXD3		GPIO3_15		CAN4_TX		EC2_TXD3		USB2_D7		FTM2_CH5	
R3	LVDD	EC2_TXD2		GPIO3_16		CAN3_TX		EC2_TXD2		USB2_D6		FTM2_CH7	
T4	LVDD	EC2_TXD1		GPIO3_17		-		EC2_TXD1		USB2_D5		FTM2_CH3	
T3	LVDD	EC2_TXD0		GPIO3_18		-		EC2_TXD0		USB2_D4		FTM2_CH2	
T5	LVDD	EC2_TX_EN		GPIO3_19		-		EC2_TX_EN		USB2_STP		FTM2_FAULT	
U3	LVDD	EC2_GTX_CLK	OR	GPIO3_20	OR	-	OR	EC2_TX_CLK	OR	USB2_CLK	OR	FTM2_EXTCLK	
U5	LVDD	EC2_GTX_CLK125		GPIO3_21		-		EC2_RX_ER		USB2_PWRFAULT		-	
R2	LVDD	EC2_RXD3		GPIO3_22		CAN4_RX		EC2_RXD3		USB2_D3		FTM2_CH4	
T1	LVDD	EC2_RXD2		GPIO3_23		CAN3_RX		EC2_RXD2		USB2_D2		FTM2_CH6	
U1	LVDD	EC2_RXD1		GPIO3_24		-		EC2_RXD1		USB2_D1		FTM2_CH1	
U2	LVDD	EC2_RXD0		GPIO3_25		-		EC2_RXD0		USB2_D0		FTM2_CH0	
R1	LVDD	EC2_RX_CLK		GPIO3_26		-		EC2_RX_CLK		USB2_DIR		FTM2_QD_PHA	
V1	LVDD	EC2_RX_DV		GPIO3_27		-		EC2_RX_DV		USB2_NXT		FTM2_QD_PHB	

The respective power rail of a certain block has to be taken into account.

3.2.4 Pinout connectors

The following pinout is a preliminary appraisal.

Table 7: Pinout appraisal connector X1

X1							
Bemerkung	Signal	Ball	Pin	Pin	Ball	Signal	Bemerkung
	VCC3V3		1	2		VCC3V3	
	VCC3V3		3	4		VCC3V3	
	VCC3V3		5	6		VCC3V3	
	VCC3V3		7	8		VCC3V3	
	VBAT		9	10		BVDD	
	O1VDD		11	12		LVDD	
	LDO1_OUT		13	14		GND	
	LDO2_OUT		15	16	N6	IIC1_SCL	I²C EXT / I²C_BASE
	L1VDD		17	18	P6	IIC1_SDA	I²C EXT / I²C_BASE
	GND		19	20	K1	SDHC_CD_E	I²C EXT / I²C_BASE
Main Reset	RESIN#		21	22	L1	SDHC_WP	I²C EXT / I²C_BASE
Reset Request	RESET_REQ		23	24	R5	IRQ3	IRQ_EXT
HRSET	HRESET		25	26	L2	IRQ4	IRQ_EXT
	RTC_CLKOUT		27	28		GND	
	RTC_INT#		29	30	K3	GPIO4_14	QE / TDMB
	STBY		31	32	L3	GPIO4_15	QE / TDMB
	RTC - Reset		33	34	M3	GPIO4_16	QE / TDMB
	PMIC EN		35	36	M4	GPIO4_17	QE / TDMB
	GND		37	38	K4	GPIO4_18	QE / TDMB
	OTP SDA		39	40		GND	
	OTP SCL		41	42	M5	[CLK11]	QE / TDMB
	EVDD		43	44	N5	[CLK12]	QE / TDMB
DDR RST Control	DR_RST_CTRL		45	46		GND	
Reset Ausgang	RST_OUT		47	48		CLK9	SCFG_QUEI
	GND		49	50		CLK10	SCFG_QUEI
DDR Clock nach auße	DDR_CLK		51	52		GND	
	GND		49	54		CLK11	SCFG_QUEI
SYSCLK nach außen	SYSCLK		55	56		CLK12	SCFG_QUEI
	GND		57	58		GND	
SDHC	SDHC_DAT4	H2	59	60	E2	SDHC_CMD	SDHC_EXT
SDHC	SDHC_DAT5	H1	61	62	E1	SDHC_DAT0	SDHC_EXT
SDHC	SDHC_DAT6	J2	63	64	F2	SDHC_DAT1	SDHC_EXT
SDHC	SDHC_DAT7	J1	65	66	F1	SDHC_DAT2	SDHC_EXT
	GND		67	68	G1	SDHC_DAT3	SDHC_EXT
	USB1_D_M		69	70	D1	SDHC_CLK	SDHC_EXT
	USB1_D_P		71	72		GND	
	GND		73	74		USB1_ID	
	USB1_RX_M		75	76		USB1_RESREF	
	USB1_RX_P		77	78		USB1_VBUS	
	GND		79	80	M2	IRQ5	IRQ_EXT
	USB1_TX_M		81	82		GND	
	USB1_TX_P		83	84		IFC - QSPI	
	GND		85	86		IFC - QSPI	
	IFC - SPI1		87	88		IFC - QSPI	
	IFC - SPI1		89	90		GND	
	IFC - SPI1		91	92		IFC - QSPI	
	IFC - SPI1		93	94		IFC - QSPI	
	IFC - SPI1		95	96		IFC - QSPI	
	IFC - SPI1		97	98		IFC - QSPI	
	GND		99	100		IFC - QSPI	
	IFC - SPI1		101	102		IFC - QSPI	
	IFC - SPI1		103	104		GND	
	IFC - SPI1 / I²C		105	106		IFC - QSPI	
	IFC QSPI- I²C		107	108		IFC - QSPI	
SYSCLK/DDRCLK dis	CLK_OE		109	110		IFC - QSPI	
RTC Control Extern	Control Extern		111	112		IFC - QSPI	
OTP Spannung für PM	VDD_OTP		113	114		IFC - QSPI	
	GND		115	116		IFC - QSPI	
Temperatursensor Wa	ALERT#		117	118		IRQ-3	
Temperatursensor Wa	T_CRIT#		119	120		GND	

Table 8: Pinout appraisal connector X2

X2							
Bemerkung	Signal	Ball	Pin		Ball	Signal	Bemerkung
	IRQ-1		1	2		GND	
	GND		3	4		Lane_A_TX_P	
	GND		5	6		Lane_A_TX_N	
	Lane_B_TX_P		7	8		GND	
	Lane_B_TX_N		9	10		GND	
	GND		11	12		Lane_A_RX_P	
	GND		13	14		Lane_A_RX_N	
	Lane_B_RX_P		15	16		GND	
	Lane_B_RX_N		17	18		GND	
	GND		19	20		Lane_C_TX_P	
	GND		21	22		Lane_C_TX_N	
	Lane_D_TX_P		23	24		GND	
	Lane_D_TX_N		25	26		GND	
	GND		27	28		Lane_C_RX_P	
	GND		29	30		Lane_C_RX_N	
	Lane_D_RX_P		31	32		GND	
	Lane_D_RX_N		33	34		GND	
	GND		35	36		SD_REFCLK_1+	
	GND		37	38		SD_REFCLK_1-	
	SD_REFCLK_2+		39	40		GND	
	SD_REFCLK_2-		41	42	W5	GPIO3_02	EC1
	GND		43	44	AA!	GPIO3_03	EC1
EC1	GPIO3_09	AB	45	46	Y6	GPIO3_04	EC1
EC1	GPIO3_10	AC	47	48	AA	GPIO3_05	EC1
EC1	GPIO3_11	AC	49	50	W6	GPIO3_06	EC1
EC1	GPIO3_12	AB	51	52	Y7	GPIO3_07	EC1
EC1	GPIO3_13	AC	53	54		GND	
EC1	GPIO3_14	AC	55	56	R4	GPIO3_15	EC2
EC1	GPIO3_08	AA	57	58	R3	GPIO3_16	EC2
	GND		59	60	T4	GPIO3_17	EC2
EC2	GPIO3_21	U5	61	62	T3	GPIO3_18	EC2
EC2	GPIO3_22	R2	63	64	T5	GPIO3_19	EC2
EC2	GPIO3_23	T1	65	66	U3	GPIO3_20	EC2
EC2	GPIO3_24	U1	67	68		GND	
EC2	GPIO3_25	U2	69	70	V3	GPIO3_28	EC3
EC2	GPIO3_26	R1	71	72	V4	GPIO3_29	EC3
EC2	GPIO3_27	V1	73	74	W3	GPIO3_30	EC3
	GND		75	76	W4	GPIO3_31	EC3
EC3	GPIO4_02	Y4	77	78	Y3	GPIO4_00	EC3
EC3	GPIO4_03	W1	79	80	V5	GPIO4_01	EC3
EC3	GPIO4_04	Y1	81	82		GND	
EC3	GPIO4_05	Y2	83	84	AB;	GPIO3_00	MDC / MDIO
EC3	GPIO4_06	AA	85	86	AB:	GPIO3_01	MDC / MDIO
EC3	GPIO4_07	V2	87	88		GND	
EC3	GPIO4_08	AA	89	90	E10	RTC	
	GND		91	92	E6	ASLEEP	
UART_EXT/ BASE	GPIO1_16	P1	93	94	D7	EVT9_B	
UART_EXT/ BASE	GPIO1_17	M1	95	96	G6	IRQ0	
UART_EXT/ BASE	GPIO1_18	P2	97	98	W7	IRQ2	
UART_EXT/ BASE	GPIO1_19	N3	99	100	N1	GPIO1_15	UART_EXT/ BASE
UART_EXT/ BASE	GPIO1_20	P3	101	102		GND	
UART_EXT/ BASE	GPIO1_21	N4	103	104	H3	GPIO4_09	QE / TDMA
UART_EXT/ BASE	GPIO1_22	P5	105	106	J3	GPIO4_10	QE / TDMA
	GND		107	108	J4	GPIO4_11	QE / TDMA
	JTAG		109	110	J5	GPIO4_12	QE / TDMA
	JTAG		111	112	H5	GPIO4_13	QE / TDMA
	JTAG		113	114		GND	
	JTAG		115	116	K5	[CLK9]	QE / TDMA
	JTAG		117	118	L5	[CLK10]	QE / TDMA
	GND		119	120		GND	

Table 9: Pinout appraisal connector X3

X3 - Optional						
Bemerkung	Signal	Ball	Pin	Ball	Signal	Bemerkung
	GND		1 2		GND	
	IFC_AD00		3 4		IFC_WE0_B	
	IFC_AD01		5 6		IFC_CLE	
	IFC_AD02		7 8		IFC_WP0_B	
	IFC_AD03		9 10		GND	
	IFC_AD04		11 12		IFC_CLK0	
	GND		13 14		GND	
	IFC_AD05		15 16		IFC_CLK1	
	IFC_AD06		17 18		GND	
	IFC_AD07		19 20		IFC_NDDDR_CLK	
	IFC_AD14		21 22		GND	
	IFC_AD15		23 24		IFCNDDQS	
	GND		25 26		frei	
	IFC_AVD		27 28		frei	
	IFC_BCTL		29 30		frei	
	IFC_TE		31 32		GND	
	IFC_CS0_B		33 34		frei	
	IFC_OE_B		35 36		frei	
	IFC_RB0_B		37 38		frei	
	GND		39 40		GND	

3.2.5 JTAG interface

The JTAG interface is routed to the connector.

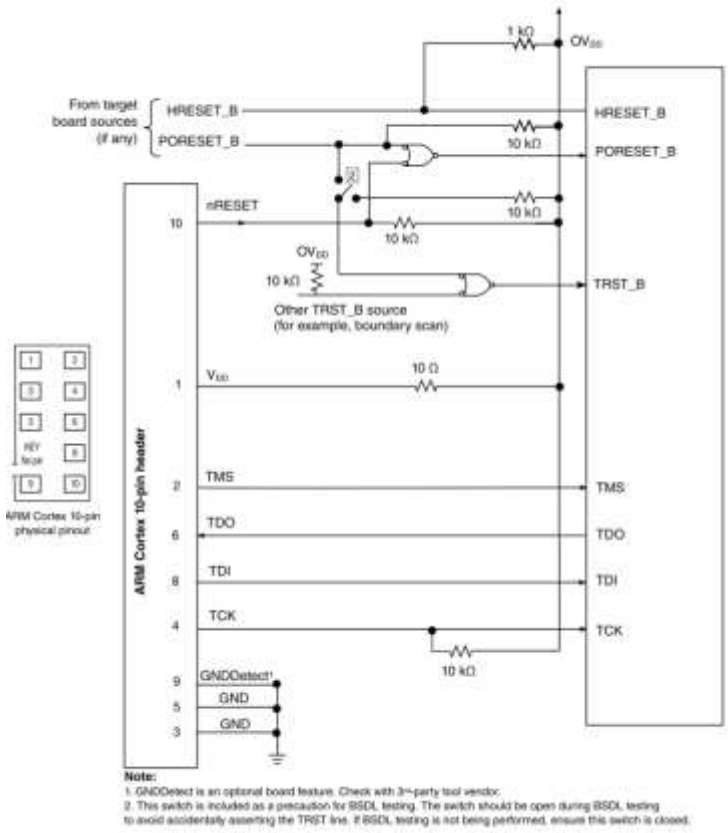


Illustration 7: JTAG interface

Attention: Power rail OVDD	
	The power rail OVDD (1.8 V) is used for the JTAG interface. An external level conversion is necessary, if applicable.

3.2.6 Deep Sleep

Deep Sleep is an especially efficient energy-saving mode (LPM35), a variation of the LPM20, with which parts of the Core Supply are switched off.

The transition into Deep Sleep is a complicated multistage process, which is partly controlled by software, and partly by a CPU-internal State Machine, which also has to be configured by software.

Note: Supply PROG_SFP	
	The supply PROG_SFP is exclusively required to program the Security Fuses. In case it is used, a suitable switchable supply must be provided on the carrier board for this special use case.

3.3 DDR3L SDRAM

The maximum memory size is 2 Gbyte, plus ECC. 1 Gbyte is assembled by default, plus ECC.

The LS102x CPU provides the following DDR features:

- DDR3L memory interface
- Data bus width 32-/36 Bit incl. ECC (LS1022 16Bit + ECC)

There are the following options:

- 2 × 8 Gbit = 2 Gbyte + ECC
- 2 × 4 Gbit = 1 Gbyte + ECC
- 2 × 2 Gbit = 512 Mbyte + ECC

3.4 On-board flash

The following flash expansion is possible:

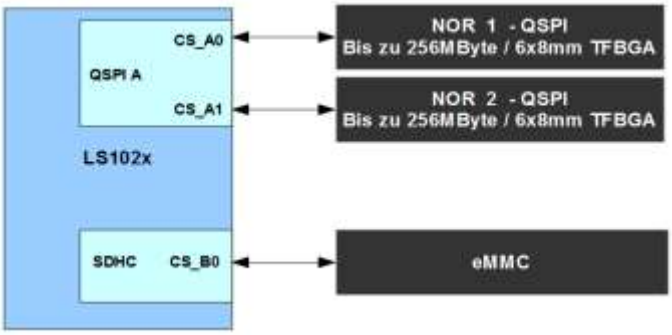


Illustration 8: On-board flash maximum expansion

QSPI is used as an interface. NOR flashes are connected at QSPI_A.
QSPI_A, chip select A0, is used as a boot source. The flashes support the 4-bit QSPI interface.
The following illustration shows how the eMMC is connected:

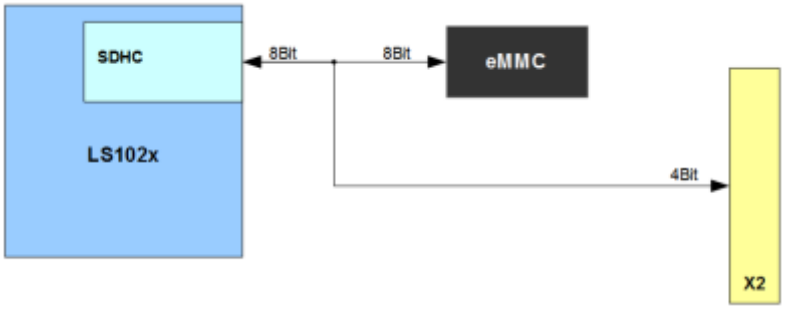


Illustration 9: Connection of the eMMC at the SDHC interface

The SDHC interface is connected with 8 bit to the eMMC and is also routed with 4 bit to the connector to connect an SD card.

Attention: eMMC and SD card	
	eMMC and SD card cannot operate simultaneously!

eMMC memory

Manufacturer:	Micron
Series:	MTFC2GMDEA…
Size:	2, 4, 8, 16, or 32 Gbyte
Functions:	ECC, bad block management, wear levelling

Optionally the reset signal is connected to PORESET.

3.5 Reset structure

A LED indicates the RESET condition. A suitable driver is provided.
The system RESET is routed to the connector via a buffer.
HRESET# of the CPU is directly routed to the connector. A 1 kΩ pull-up to OVDD (1.8 V) is required.
A 1 kΩ pull-up to OVDD is provided at RESET_REQ# of the CPU.

3.6 Housekeeping

3.6.1 Overview

The following components are present on the TQMLS102xA:

- RTC (optional)
- Temperature sensor (local and remote in the CPU)
- EEPROM

The components are connected via the I²C_1 interface.

The following illustration shows the implementation:

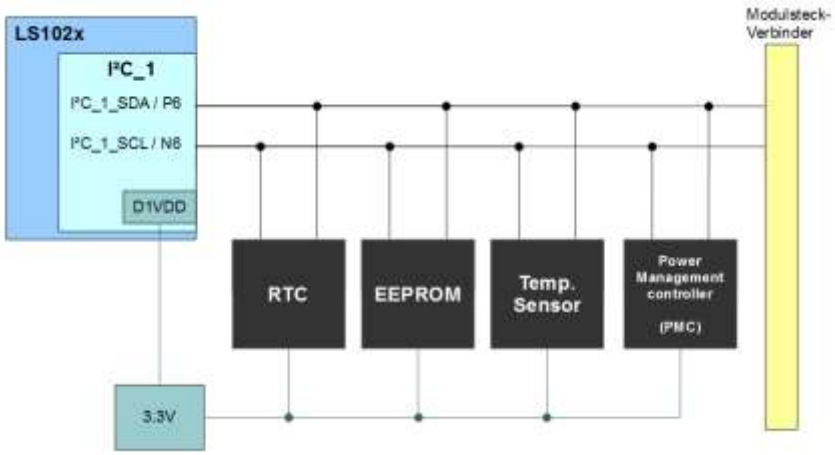


Illustration 10: I²C bus components on the TQMLS102xA

I²C_1 is supplied via voltage block D1VDD. D1VDD is supplied with 3.3 V, therefore, the I²C bus subscribers also have to be supplied with 3.3 V.

The addresses of the respective I²C-bus subscribers are configurable using address pins, or already hardwired by the manufacturer.

The following addresses are used:

Table 10: I²C bus addresses

Function block	Device	Address	Remark
RTC	PCF85063	1010 001b	
EEPROM	M24C64	1010 000b 1011 000b	E0 / E1 / E2 connected to GND
Temperature sensor	SA56004EDP,118	1001 100b	Address is defined by order code
PMC	Kinetis µController	freely programmable	

3.6.2 RTC

An RTC is optionally available. The NXP PCF85063TP is used as an RTC.
It has the following characteristics:

- Real-Time clock / calendar
- 1.8 V … 5.5 V power supply
- I²C interface (up to 400 kHz)
- Current consumption max. 50 µA in operation / <0.6 µA in standby
- Programmable register offset to increase precision

The following functions of the RTC are available:

- RTC function block, INT at the connector
  The RTC on the TQMLS102xA is a separate function block. It can be configured using the CPU (I²C). The interrupt signal is routed to the connector, so every reaction / wakeup sequence must be carried out external.
- RTC function with power management µController
  The RTC is also an independent function block. It can be configured during runtime using the CPU. In Standby mode the RTC can wake the PMC with a wakeup event, which then wakes the CPU.

Since the RTC is optionally, the CLKOUT signal is routed to the connector and is not used on the TQMLS102xA.
A simple implementation of the RTC function block is shown in the following block diagram:

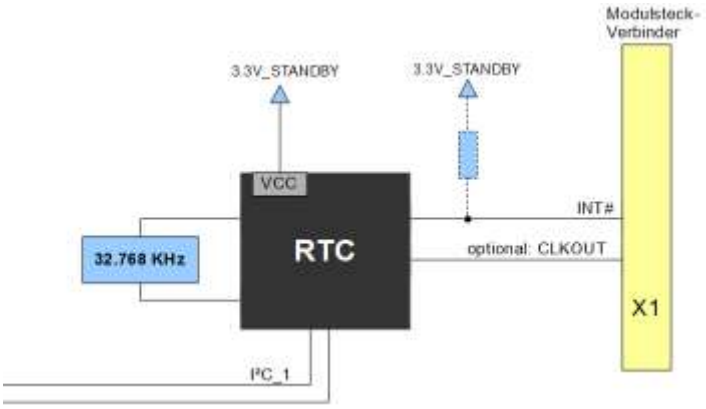


Illustration 11: RTC function block (1)

When the RTC is supplied with the standby voltage, it can be configured or read by the CPU via I²C during runtime. In standby mode all further operations can be initiated using the low-active interrupt, which is available at the connector.
The logic to wake the TQMLS102xA must therefore be provided externally.
An alternative with independent RTC wakeup function is described in the following block diagram:

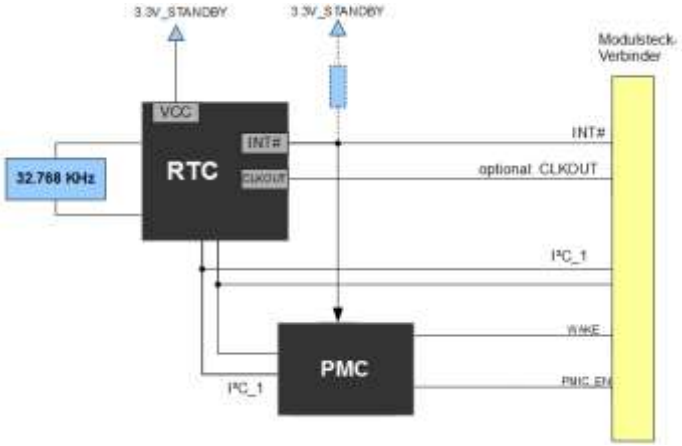


Illustration 12: RTC function block (2)

The RTC interrupt can be used to wake the TQMLS102xA from standby.
The PMC reacts to the RTC interrupt and starts the Power-Sequencing.
The current consumption is approximately 0.8 µA, in addition to power mode VLLS1
The µController is specified with a maximum of 5.5 µA at +85 °C in power mode VLLS1.

3.6.3 Temperature supervision

The NXP SA56004X is used.

The parameters are:

- Local and remote temperature sensor
- Accuracy: ±1 °C remote / ±2 °C local
- 11 bit resolution / 0.125 °C
- I²C bus
- 3.3 V supply
- Programmable ALERT# and T_CRIT# outputs

Table 11: SA56004X slave addresses

Table 4. Slave addresses

Type number	Device slave address[1]
SA56004AD	1001 000
SA56004ADP	
SA56004ATK	
SA56004BD	1001 001
SA56004BDP	
SA56004CD	1001 010
SA56004CDP	
SA56004DD	1001 011
SA56004DDP	
SA56004ED[2]	1001 100
SA56004EDP[2]	
SA56004ETK[2]	
SA56004FD	1001 101
SA56004FDP	
SA56004GD	1001 110
SA56004GDP	
SA56004HD	1001 111
SA56004HDP	

The communication is done via the I²C bus. The slave address of the device is "factory programmed".

Programmable warning signals:

ALERT#:

The trigger level of the open-drain signal is freely programmable and can be used as a warning. The signal is routed to the connector.
No pull-up is provided on the TQMLS102xA to remain variable. If this is implemented on the carrier board, any voltage can be switched.

T_CRIT#:

The trigger level of the open-drain signal is freely programmable. Depending on the programming this value can also signal the most critical value. This signal provides the option to trigger RESET# independently, or to send the signal to the power management µController (placement option). The signal is routed to the connector without pull-up.

The following Illustration shows the connection of the temperature sensor:

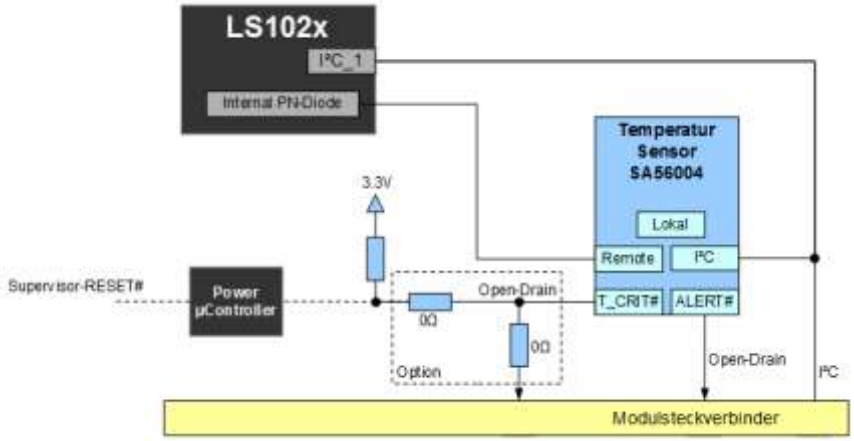


Illustration 13: Wiring of temperature sensor

For the remote temperature measurement a 2.2 nF capacitor is recommended between D + and D– (noise suppression).
The CPU-internal PN junction for temperature measurement is connected here:

Table 12: Pin assignment CPU-internal PN junction

TD1_ANODE	Reserved	J6	IO	-	19
TD1_CATHODE	Reserved	K6	IO	-	19

3.6.4 EEPROM

An EEPROM with 64 kBit is assembled on the TQMLS102xA. The ST M24C64 series is used.

- 64 Kbit
- I²C interface (100 kHz, 400 kHz, 1 MHz)
- 1.8 V … 5.5 V
- –40 °C … +85 °C

The EEPROM is supplied with 3.3 V.
According to the I²C bus addresses (see section 3.6.1) E0/E1/E2 are connected to GND.

3.7 Power supply

3.7.1 Power estimation

The single values are estimated and assume an average load.

Table 13: Power estimation

Component	Power consumption
CPU	1.5 W
DDR3L SDRAM	1.0 W
NOR flash	0.2 W
Other	0.5 W
Total	**3.2 W**

3.8 External interfaces

3.8.1 SERDES

All three SERDES interfaces require 100 nF AC-coupled capacitors.
The coupling capacitors are not assembled on the TQMLS102xA to enable the usage of the interface for other purposes.

3.8.2 USB3.0

According to the specification the AC-transmit lines are AC-coupled. Recommendation: 100 nF. (Permitted: 75 nF … 200 nF.

4. MECHANICS

4.1 Connectors

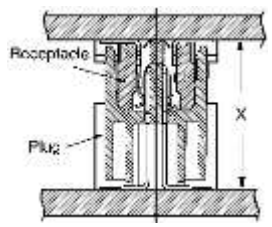
The TQMLS102xA is connected to the carrier board with 280 pins on three connectors.
The following table shows details of the plug connector used.

Table 14: Plug connectors on the TQMLS102xA

Manufacturer	Part number	Remark
TE connectivity	120-pin: 5177985-5	• 0.8 mm pitch • Plating: Gold 0.2 µm • –40 °C to 125 °C
TE connectivity	40-pin: 5177985-1	• 0.8 mm pitch • Plating: Gold 0.2 µm • –40 °C to 125 °C

The TQMLS102xA is held in the plug connectors with a considerable retention force.
To avoid damaging the plug connectors of the TQMLS102xA as well as the carrier board plug connectors while removing the TQMLS102xA the use of an extraction tool is strongly recommended. See section 4.7 for further information.
The following table shows some suitable mating plug connectors for the carrier board.

Table 15: Suitable carrier board mating plug connectors

Manufacturer	Part number	Stack height (X)	
TE connectivity	40-pin: 5177986-1 120-pin: 5177986-5	5 mm	
TE connectivity	40-pin: 1-5177986-1 120-pin: 1-5177986-5	6 mm	
TE connectivity	40-pin: 2-5177986-1 120-pin: 2-5177986-5	7 mm	
TE connectivity	40-pin: 3-5177986-1 120-pin: 3-5177986-5	8 mm	

4.2 TQMLS102xA image

Illustration 14: TQMLS102xA

4.3 Adaptation to the environment

The overall dimensions (length × width) of the TQMLS102xA are 55 × 44 mm².
The maximum height of the TQMLS102xA above the carrier board is approximately 8.5 mm.

4.4 Protection against external effects

As an embedded module the TQMLS102xA is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

4.5 Thermal management

To cool the TQMLS102xA, approximately 3 W have to be dissipated.
The power dissipation originates primarily in the CPU, the DDR3L-SDRAM and the PMIC.
The power dissipation also depends on the software used and can vary according to the application.
See Freescale Application Note (3) for further information.

Attention: Destruction or malfunction	
	The CPU belongs to a performance category in which a cooling system may be essential in certain applications. It is the responsibility of the customer to define a suitable cooling method depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software).

4.6 Structural requirements

The TQMLS102xA is held in the mating plug connectors by the retention force of the pins (a total of 280). For high requirements with respect to vibration and shock firmness an additional holder has to be provided in the final product to hold the TQMLS102xA in its position. For this purpose TQ-Systems GmbH can provide a suitable solution. As no heavy and big components are used, no further requirements are given.

4.7 Notes of treatment

To avoid damage caused by mechanical stress, the TQMLS102xA may only be extracted from the carrier board by using the extraction tool MOZI8XXL that can also be obtained separately.

Attention: Note with respect to the component placement of the carrier board	
	2.5 mm should be kept free on the carrier board, along the longitudinal edges on both sides of the TQMLS102xA for the extraction tool.

5. TECHNICAL DATA

5.1 Vibration load

Table 16: Vibration test

Parameter	Details
Oscillation, sinusoidal	According to DIN EN 60068-2-6
Frequency ranges	2 – 9 Hz, 9 – 200 Hz, 200 – 500 Hz
Wobble rate	1.0 octaves / min
Excitation axes	X-Y-Z axis
Number of frequency cycles	20 frequency cycles
Amplitude	2 Hz … 9 Hz: 3.5 ms^{-2} 9 Hz … 200 Hz: 10 ms^{-2} 200 Hz … 500 Hz: 15 ms^{-2}

5.2 Shock load

Table 17: Shock test

Parameter	Details
Shocks	According to DIN EN 60068-2-27
Shock form	Half sine
Acceleration	30 g
Residence time	18 ms
Number of shocks	3 shocks per direction
Excitation axes	6X, 6Y, 6Z

The values shown are based on the guidelines of the standard DIN ETS 300019 (Environmental tests for telecommunications equipment).

6. SOFTWARE

The TQMLS102xA is delivered with a preinstalled boot loader and a BSP which is configured for the Starterkit STK-MBLS102xA.
The boot loader provides module-specific as well as board-specific settings, e.g.:

- CPU configuration
- PMIC configuration
- RAM configuration and timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

More information can be found in the Support Wiki for the TQMLS102xA.

7. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

7.1 EMC

The TQMLS102xA was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

The TQMLS102xA it designed to pass the following tests:

- EMC-Interference radiation:
  Measurement of the electrically radiated emission for standard, residential, commercial and light industrial environments in the range of 30 MHz to 1 GHz according to
  DIN EN 61000-6-3 or DIN EN 55022
- EMC-Interference radiation:
  Measurement of the electrically radiated emission for industrial environments in the range of 30 MHz to 1 GHz according to DIN EN 61000-6-4 or DIN EN 55011
- EMC-Immunity according to EN 61000-4-2[1)]:
  Electrostatic discharge immunity (ESD)
- EMC-Immunity according to EN 61000-4-3[1)]:
  Radiated radio frequency, electromagnetic field immunity
- EMC-Immunity to fast transients according to EN 61000-4-4[1)]:
  Electrical fast transient (BURST)
- EMC-Immunity to surge according to EN 61000-4-5[1)]:
  Surge immunity test (SURGE).
  In DC networks an inlet length of less than 10 m is assumed.
  For the audit a reference power supply has to be defined / supplied.
  Signal and I/O lines >30 m must be checked for SURGE.
- EMC-Immunity according to EN 61000-4-6[1)]:
  Immunity to conducted disturbances, induced by radio-frequency fields
- EMC-Immunity according to EN 61000-4-11[1)]:
  Immunity to voltage dips, voltage variation and short interruptions in the mains supply (VOLTAGE DIPS)
- EMC-Immunity according to EN 61000-4-29[2)]:
  Immunity to voltage dips and short interruptions on the DC input power supply

[1)]: The test level and test criteria are taken from the generic standards: the EN 61000-6-1 generic standard; immunity for standard, residential, commercial and light industrial environments, and the EN 61000-6-2 generic standard for industrial environments.

[2)]: The test criteria are not fixed here yet, because there are still no generic standards or product standards on, which to base this standard. When required the test criteria have to be defined with the customer.

The following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanent clocked lines (e.g., clock) should be kept short;
  avoid interference of other signals by distance and / or shielding besides,
  take note of not only the frequency, but also the signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)

Because the TQMLS102xA is used on an application-specific carrier board, EMC or ESD tests only make sense for the whole device.

7.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMLS102xA.

Following measures are recommended for a carrier board:

- Generally applicable: Shielding of the inputs
  (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signal lines: RC filtering / Zener diode(s)
- Fast signal lines: Integrated protective devices (e.g., suppressor diode arrays)

7.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety haven't been carried out.

7.4 Climatic and operational conditions

The possible temperature range strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the whole assembly.

In general, a reliable operation is given when following conditions are met:

Table 18: Climate and operational conditions

Parameter	Range	Remark
Permitted Environment temperature	–40 … +85 °C	–
Permitted storage temperature	–40 … +100 °C	–
Relative humidity (operating / storage)	10 … 90 %	Not condensing

Detailed information concerning the thermal characteristics of the CPU is to be taken from Freescale's Product Brief and Fact Sheet (1) and (2).

7.5 Reliability and service life

No detailed MTBF calculation has been done for the TQMLS102xA.

The TQMLS102xA is designed to be insensitive to vibration and impact.

Middle grade connectors, which guarantee at least 100 mating cycles, were used for the TQMLS102xA.

7.6 Environment protection

7.6.1 RoHS

The TQMLS102xA is manufactured RoHS compliant.

- All used components and assemblies are RoHS compliant
- RoHS compliant soldering processes are used

7.6.2 WEEE

The company placing the product on the market is responsible for the observance of the WEEE regulation.

To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.

7.6.3 REACH

The EU-chemical regulation 1907/2006 (REACH regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as TQ-Systems GmbH is informed by suppliers accordingly.

7.6.4 EuP

The guideline 2005/32/EC (EuP) is the next step after WEEE and RoHS for an environmentally friendly production of electric and electronic products. The consideration of environmental requirements with the product design "creation appropriate for the environment" ("ecological design") with the aim to improve the environmental compatibility of the product during its whole life cycle should be taken into consideration.

The guideline appropriate for the product (embedded PC) is applied.

7.7 Battery

No batteries are used on the TQMLS102xA.

7.8 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.

The energy consumption of this subassembly is minimised by suitable measures.

Printed PC-boards are delivered in reusable packaging.

Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material.

Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (source of information: BGBl I 1996, 1382, (1997, 2860)
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 19: Acronyms

Acronym	Meaning
ARM®	Advanced RISC Machine
ATA	Advanced Technology Attachment
BIOS	Basic Input/Output System
BSP	Board Support Package
CPU	Central Processing Unit
DC	Direct Current
DDR3L	Double Data Rate 3 Low voltage
DIN	German industry standard (Deutsche Industrienorm)
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded MultiMedia Card (Flash)
EN	European Standard (Europäische Norm)
ESD	Electrostatic Discharge
eSDHC	enhanced Secure Digital High Capacity
ETS	European Telecommunications Standards
EuP	Energy using Products
FR4	Flame Retardant-4
GPCM	General Purpose Programmable Machines
GPIO	General Purpose Input/Output
IFC	Integrated Flash-Controller
IP00	Ingress Protection 00
I²C	Inter-Integrated Circuit
I²S	Integrated Interchip Sound
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LPM	Low Power Mode
MOZI	Module extractor (Modulzieher)
MTBF	Mean operating Time Between Failures
NAND	Not-And
NOR	Not-Or
PBL	Pre-Boot Loader
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PCMCIA	People Can't Memorize Computer Industries Acronyms
PHY	Physical (layer of the OSI model)
PMC	Power Management Controller
PMIC	Power Management IC
QSPI	Queued Serial Peripheral Interface
RAM	Random Access Memory
RC	Resistor-Capacitor
RCW	Reset Configuration Word
REACH	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RoHS	Restriction of (the use of certain) Hazardous Substances
RTC	Real-Time Clock
SATA	Serial ATA
SD card	Secure Digital Card
SD/MMC	Secure Digital Multimedia Card
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SERDES	Serializer/Deserializer
SPI	Serial Peripheral Interface
SVHC	Substances of Very High Concern
UART	Universal Asynchronous Receiver/Transmitter
UM	User's Manual
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment

8.2 References

Table 20: Further applicable documents

No.:	Name	Rev. / Date	Company
(1)	QorIQ LS1021A Family Communications Processor Product Brief LS1021APB	9/10/2014	Freescale
(2)	QorIQ LS1021A - Fact Sheet LS1021AFS	2/4/2015	Freescale
(3)	Thermal Solutions AN4871	2/7/2014	Freescale

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