XVME-202
3U PAMUX Module

USER'S MANUAL

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Chapter 1

INTRODUCTION

1.1 OVERVIEW

The XVME-202 PAMUX Interface Module is a single high, VMEbus compatible board which allows a VMEbus master to communicate with a PAMUX I/O subsystem. The specific features of the XVME-202 Interface Module are listed below:

- Directly compatible with PAMUX I/O system.
- 16 PAMUX units can be addressed from one module providing up to 5 12 I/O points.
- Termination resistors provided on board.
- Connection is made via a 50 conductor ribbon cable.
- Cable length can be up to 500 feet.

The XVME-202 occupies a 1K block of the VMEbus short I/O Address Space. The module address decode logic allows the user to select (via 6 jumpers) any one of 64 of the 1K boundaries in the short I/O Address Space to be used as the module base address. The module's Internal Registers are accessible at specific addresses offset from the selected module base address.

1.2 MANUAL STRUCTURE

This manual consists of three chapters which divide the various aspects of module specification and operation into three distinct areas. The three chapters develop these aspects in the following progression:

Chapter One - A general description of the XVME-202 PAMUX Interface Module, including complete functional and environmental specifications, VME bus compliance information, and a block diagram.

Chapter Two - Module installation information covering module specific system requirements, jumpers, and connector pinouts.

Chapter Three - Details covering functional addressing, and programming considerations.

The Appendices are designed to provide additional information in terms of the backplane signal/pin descriptions, a block diagram and assembly drawing, and module schematics.

1.3 MODULE OPERATIONAL DESCRIPTION

Figure 1-1 shows an operational block diagram of the XVME-202 PAMUX Interface Module.

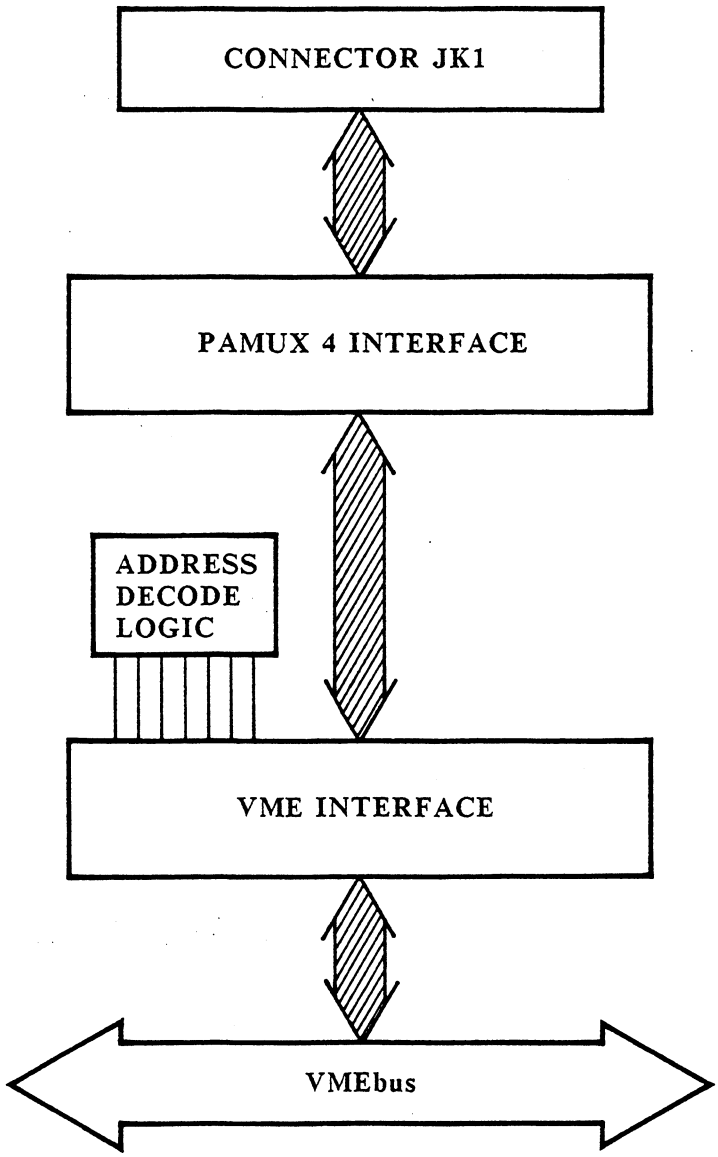


Figure 1-1. XVME-202 Module Operational Block Diagram

1.4 MODULE SPECIFICATIONS

The following is a list of the operational and environmental specifications for the XVME-202 PAMUX Interface Module.

Power Requirements .	+5V, 1.6A typ., 1.8 A max
Board Dimensions	150 x 116.7 mm
Temperature	
Operating . .	0 to 65 degrees C 32 to 149 degrees F
Non-Operating	-40 to 85 degrees C -40 to 158 degrees F
Humidity . . .	5 to 95% RH non-condensing (Extremely low humidity may require protection against static discharge.)
Altitude	
Operating . .	Sea-level to 10,000 ft. (3048m)
Non-Operating .	Sea-level to 50,000 ft. (15240m)
Vibration	
Operating . .	5 to 2000 Hz 0.0 15" peak-to-peak displacement 2.5 g peak acceleration
Non-Operating .	5 to 2000 Hz 0.030" peak-to-peak displacement 5.0 g peak acceleration
Shock	
Operating . .	30 g peak acceleration' 11 msec duration
Non-operating .	50 g peak acceleration 11 msec duration
VMEbus Compliance .	Complies with VMEbus Standard Revision C. 1 A16:D08(0) DTB Slave Form Factor - SINGLE Base address jumper-selectable on 1K boundaries within the VMEbus short I/O address space

Compatibility	Compatible with OPT0 2 2 PAMUX 4 *(or PAMUX 2 if the PAMUX unit is configured for 8-bit use)

VMEbus Access Time.	Typical	Maximum
DSO ASSERTED TO DTACK ASSERTED (READ)	2500nS	2700nS
DSO ASSERTED TO DTACK ASSERTED (WRITE)	500nS	600nS
DSO NEGATED TO DTACK NEGATED . .	65nS	IOOnS

Chapter 2

INSTALLATION

2.1 INTRODUCTION

This chapter explains how to configure the XVME-202 PAMUX Interface Module prior to installation in a VMEbus backplane. Included in this chapter is information on module base address selection jumpers, address modifier jumper, connector pinouts, and a brief outline of the physical installation procedure.

2.2 SYSTEM REQUIREMENTS

The XVME-202 PAMUX Interface Module is a single high VMEbus compatible module. To operate, it must be properly installed in a VMEbus backplane.

The minimum system requirements for the operation of an XVME-202 PAMUX Interface Module are one of the following:

A) - A host processor properly installed on the same backplane.

- A properly installed system controller module which provides the following functions:

  -- Data Transfer Bus Arbiter
  -- System Clock driver
  -- System Reset driver
  -- Bus time-out module

An example of such a controller subsystem is the XYCOM XVME-010 System Resource Module (SRM).

-- OR --

B) l A host processor which incorporates the system controller functions on-board.

An example of such a processor is the XVME-600 or the XVME-601.

Prior to installing the XVME-202 PAMUX Interface Module, it will be necessary to configure three jumper options. These options are:

1) Module base address within the short I/O address space.

2) Address Modifier codes to which the Module will respond.

3) Select SYSCLOCK or on-board Oscillator.

2.3 XVME-202 PAMUX INTERFACE MODULE JUMPER/CONNECTOR LOCATIONS

The jumpers and connectors relevant to the installation of the XVME-202 are shown in Figure 2-1.

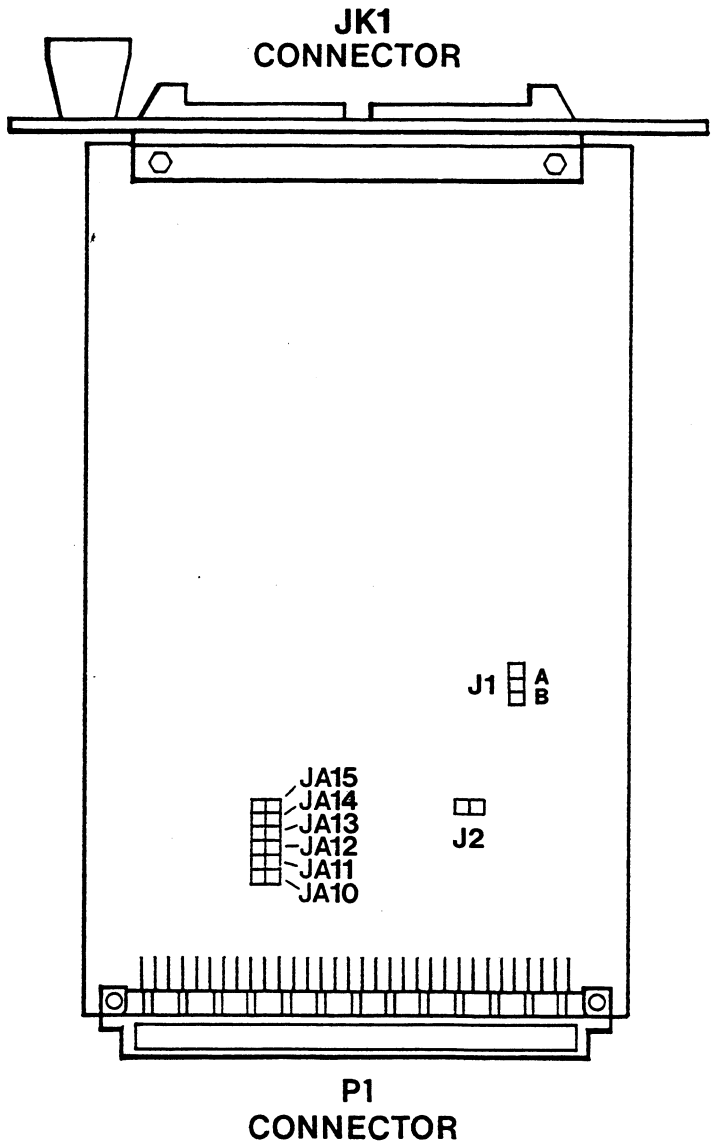


Figure 2-1. Jumper/Connector Locations on the XVME-202

2.4 XVME-202 MODULE JUMPER LIST

Table 2-1. Module Jumper List

JUMPER	USE
JlA	Selects optional on-board oscillator.
JlB	Selects SYSCLK from VMEbus.
J2	Determines whether the module will respond to supervisory or non-privileged short I/O VMEbus cycles (refer to section 2.4.2 of this manual).
JAl0-JAI5	Select module base address on any one of the 64 1K boundaries within the short I/O address space (refer to Section 2.4.1 of this manual).

2.4.1 Base Address Jumpers

The XVME-202 can be configured to be addressed at any one of the 64 1K boundaries within the VME Short I/O Address space by using jumpers JAl0 through JA15 (see Figure 2-1 for the location of the jumpers on the board) as shown in Table 2-2.

Table 2-2. Base Address Jumper Options

JA15	JA14	JA13	JA12	JAll	JAI0	Base Address
IN	IN	IN	IN	IN	IN	OOOOH
IN	IN	IN	IN	IN	OUT	0400H
IN	IN	IN	IN	OUT	IN	OSOOH
IN	IN	IN	IN	OUT	OUT	OCOOH
IN	IN	IN	OUT	IN	IN	1 OOOH
IN	IN.	IN	OUT	IN	OUT	1400H
IN	IN	IN	OUT	OUT	IN	1800H
IN	IN	IN	OUT	OUT	OUT	ICOOH
IN	IN	OUT	IN	IN	IN	2000H
IN	IN	OUT	IN	IN	OUT	2400H
IN	IN	OUT	IN	OUT	IN	2800H
IN	IN	OUT	IN	OUT	OUT	2COOH
IN	IN	OUT	OUT	IN	IN	3000H
IN	IN	OUT	OUT	IN	OUT	3400H
IN	IN	OUT	OUT	OUT	IN	3800H
IN	IN	OUT	OUT	OUT	OUT	3COOH
IN	OUT	IN	IN	IN	IN	4000H
IN	OUT	IN	IN	IN	OUT	4400H
IN	OUT	IN	IN	OUT	IN	4800H
IN	OUT	IN	IN	OUT	OUT	4COOH
IN	OUT	IN	OUT	IN	IN	5000H
IN	OUT	IN	OUT	IN	OUT	5400H
IN	OUT	IN	OUT	OUT	IN	5800H
IN	OUT	IN	OUT	OUT	OUT	5COOH
IN	OUT	OUT	IN	IN	IN	6000H
IN	OUT	OUT	IN	IN	OUT	6400H
IN	OUT	OUT	IN	OUT	IN	6800H
IN	OUT	OUT	IN	OUT	OUT	6COOH
IN	OUT	OUT	OUT	IN	IN	7000H
IN	OUT	OUT	OUT	IN	OUT	7400H
IN	OUT	OUT	OUT	OUT	IN	7800H
IN	OUT	OUT	OUT	OUT	OUT	7COOH
OUT	IN	IN	IN	IN	IN	8000H
OUT	IN	IN	IN	IN	OUT	8400H
OUT	IN	IN	IN	OUT	IN	8800H
OUT	IN	IN	IN	OUT	OUT	8COOH
OUT	IN	IN	OUT	IN	IN	9000H
OUT	IN	IN	OUT	IN	OUT	9400H
OUT	IN	IN	OUT	OUT	IN	9800H
OUT	IN	IN	OUT	OUT	OUT	9COOH
OUT	IN	OUT	IN	IN	IN	AOOOH
OUT	IN	OUT	IN	IN	OUT	A400H
OUT	IN	OUT	IN	OUT	IN	A800H
OUT	IN	OUT	IN	OUT	OUT	ACOOH
OUT	IN	OUT	OUT	IN	IN	BOOOH

Table 2-2. Base Address Jumper Options (Cont'd)

OUT	IN	OUT	OUT	IN	OUT	B400H
OUT	IN	OUT	OUT	OUT	IN	B800H
OUT	IN	OUT	OUT	OUT	OUT	BC00H
OUT	OUT	IN	IN	IN	IN	C000H
OUT	OUT	IN	IN	IN	OUT	C400H
OUT	OUT	IN	IN	OUT	IN	C800H
OUT	OUT	IN	IN	OUT	OUT	CC00H
OUT	OUT	IN	OUT	IN	IN	D000H
OUT	OUT	IN	OUT	IN	OUT	D400H
OUT	OUT	IN	OUT	OUT	IN	D800H
OUT	OUT	IN	OUT	OUT	OUT	DC00H
OUT	OUT	OUT	IN	IN	IN	E000H
OUT	OUT	OUT	IN	IN	OUT	E400H
OUT	OUT	OUT	IN	OUT	IN	E800H
OUT	OUT	OUT	IN	OUT	OUT	EC00H
OUT	OUT	OUT	OUT	IN	IN	F000H
OUT	OUT	OUT	OUT	IN	OUT	F400H
OUT	OUT	OUT	OUT	OUT	IN	F800H
OUT	OUT	OUT	OUT	OUT	OUT	FC00H

2.4.2 Address Modifier Jumper

The XVME-202 has one jumper that determines which Address Modifier Codes it will respond to. This jumper is labeled as J2 (see Figure 2-1 for the jumper location). Jumper J2 determines whether the module will respond to supervisory or to non-privileged short I/O VMEbus cycles. When jumper J2 is in, the module will respond to supervisory short I/O bus cycles only. When jumper J2 is out, the module will respond to both non-privileged and supervisory short I/O bus cycles. Table 2-3 shows the relationship between jumper J2 and the Address Modifiers.

Table 2-3. Addressing Options

Jumper J2	Address Modifier that the XVME-202 Module will respond to
In	(2DH) Supervisory Only
Out	(2DH) Supervisory or (29H) Non-privileged

2.5 JKl Pin Assignments

The XVME-202 interconnects to the PAMUX bus via JKl on the front panel. The PAMUX bus has 8 data lines, 6 address lines, a read strobe line, a write strobe line, and a reset line. Table 2-4 shows the standard PAMUX pin out.

NOTE

The JKI connector is directly compatible with the PAMUX I/O systems, flat cables can be connected directly from the XVME-202 to the PAMUX system without the need for a transition interface.

Table 2-4. PAMUX **P**'in out

JKl Pin	Signal	JKl Pin	Signal
1	A0	33	D7
3	Al	35	D6
5	A2	37	D5
7	A3	39	D4
9	A4	41	D3
11	A5	43	D2
13	WRITE STROBE	45	Dl
15	READ STROBE	47	D0
49	RESET		

NOTE: All even numbered pins on connector JKl are tied to logic ground.

2.6 MODULE INSTALLATION

XYCOM VME modules are designed to comply with all physical and electrical VMEbus backplane specifications. The XVME-202 PAMUX Interface Module is a single-high, single-wide VMEbus module, and as such, only requires the Pl backplane.

CAUTION

Never attempt to install or remove any boards before turning off the power to the bus, and all related external power supplies.

Prior to installing a module, you should determine and verify all relevant jumper configurations, and all connections to external devices or power supplies. (Please check the jumper configuration against the diagrams and lists in this manual.)

To install a board in the cardcage, perform the following steps:

1) Make certain that the particular cardcage slot which you are going to use is clear and accessible.

2) Center the board on the plastic guides in the slot so that the handle on the front panel is towards the bottom of the cardcage.

3) Push the card slowly toward the rear of the chassis until the connectors engage (the card should slide freely in the plastic guides).

4) Apply straight-f orward pressure to the handle located on the front panel of the module until the connector is fully engaged and properly seated.

NOTE

It should not be necessary to use excessive pressure or force to engage the connectors. If the board does not properly connect with the backplane, remove the module and inspect all connectors and guide slots for possible damage or obstructions.

5) Once the board is properly seated, it should be secured to the chassis by tightening the two machine screws at the extreme top and bottom of the board.

2.7 CONNECTING THE PAMUX UNIT

On the PAMUX connector there is a notch indicating where pin 1 is located (refer to Figure 2-2). On XYCOM's XVME-202 PAMUX Interface Adapter the ribbon connector has a similar notch indicating the position of pin 1.

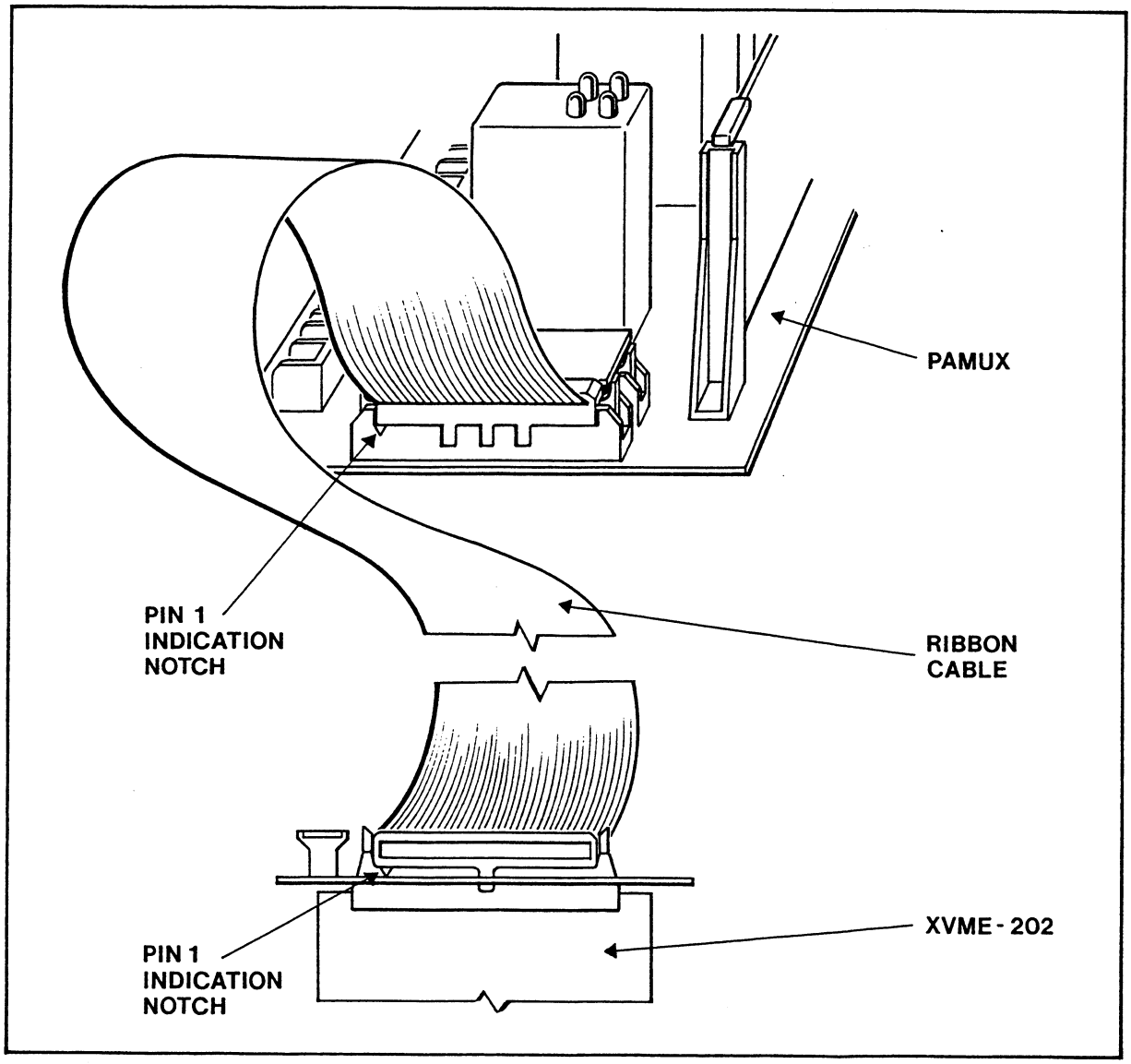


Figure 2-2. Pin 1 Notch on XYCOM Adapter and PAMUX Units

To connect a PAMUX (or a string of PAMUXs), plug one end of a flat ribbon cable into the XVME-202 JKl connector so Pin 1 on the XVME-202 JKl is connected to Pin 1 of the PAMUX connector (refer to Figure 2-2).

It is possible to connect 16 PAMUX Units in a daisy chain to the XVME-202 (see Figure 2-3) as long as the total length of the ribbon does not exceed 500 feet.

2.8 OPTIONAL ON-BOARD OSCILLATOR

Jumper Jl is used to select between the VMEbus signal SYSCLK or an optional 16 MHz oscillator. Position JIB selects the VMEbus SYSCLK and is factory shipped in this position. For systems where SYSCLK is not provided on the VMEbus backplane, A 16 MHz oscillator, Ul9, can be installed and selecting JlA, the module will operate with its own clock.

Oscillator type: CTS Knights MXO-55GA-2C-16.0MHz or equivalent

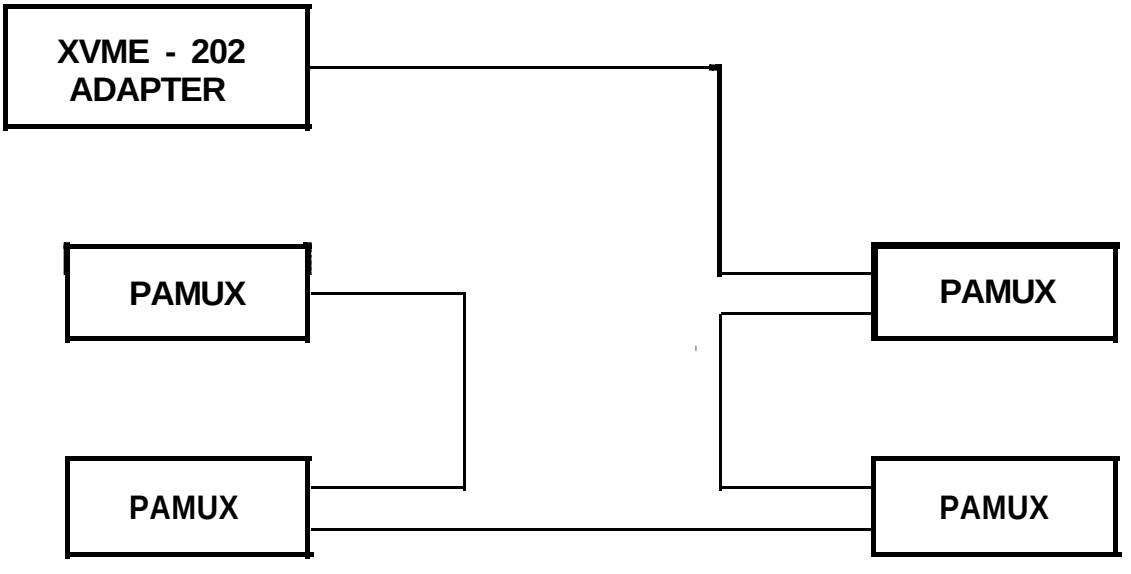


Figure 2-3. PAMUX Daisy Chain

2.9 INSTALLING A 6U FRONT PANEL KIT (optional)

XYCOM Model Number XVME-943 is an optional 6U front panel kit designed to replace the existing 3U front panel on the XVME-600. The 6U front panel facilitates the secure installation of single-high modules in those chassis which are designed to accommodate double-high modules. The following is a step-by-step procedure for installing the 6U front panel on an XVME-600 Module (refer to figure 2-4 for a graphic depiction of the installation procedure).

1. Disconnect the module from the bus.

2. Remove the screw and plastic collar assemblies (labeled #6 and #7) from the extreme top and bottom of the existing 3U front panel (#11), and install the screw assemblies in their corresponding locations on the 6U front panel.

3. Slide the module identification plate (labeled #13) from the handle (#9) on the 3U front panel. By removing the screw/nut found inside the handle, the entire handle assembly will separate from the 3U front panel. Remove the counter-sunk screw (#8) to separate the 3U front panel from the printed circuit board (#12).

4. Line-up the plastic support brackets on the printed circuit board with the corresponding holes in the 6U front panel (i.e. the holes at the top and top-center of the panel). Install the counter-sunk screw (#8) in the hole near the top center of the 6U panel, securing it to the lower support bracket on the printed circuit board.

5. Install the handle assembly (which was taken from the 3U panel) at the top of the 6U panel, using the screw and nut previously attached inside the handle. After securing the top handle, slide the module identification plate in place.

6. Finally, install the bottom handle (i.e. the handle that accompanies the kit - labeled #2) using the screw and nut (#3 & #5) provided. Slide the XYCOM VMEbus I.D. plate (#4) in place on the bottom handle. The module is now ready to be re-installed in the backplane.

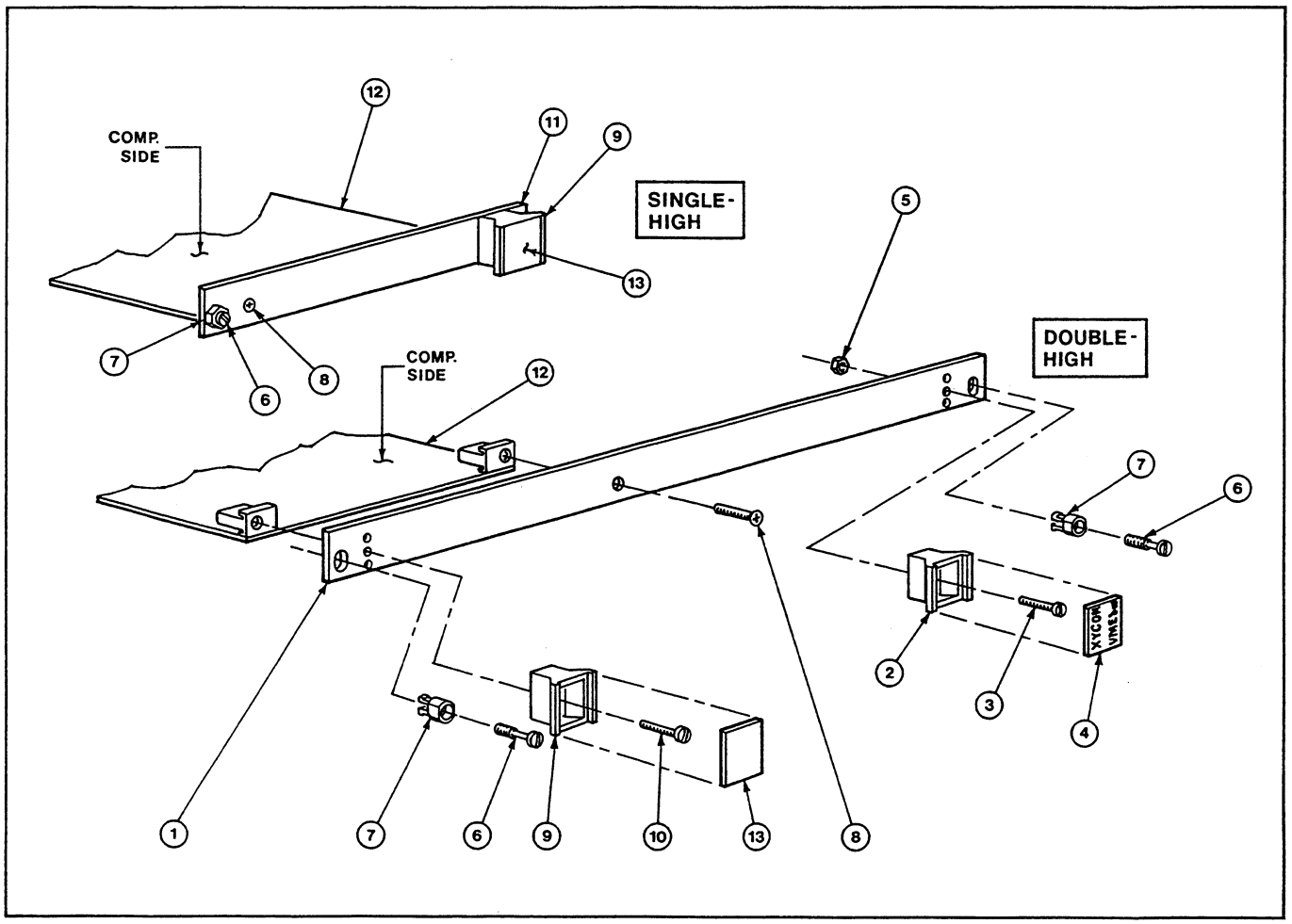


Figure 2-4. Installation of an XVME-943 6U Front Panel

Chapter 3

MODULE PROGRAMMING

3.1 INTRODUCTION

This chapter will briefly examine the addressing, and initialization procedures and constraints required when programming the XVME-202 PAMUX Interface Adapter.

3.2 MODULE ADDRESSING

The XVME-202 is an odd byte only slave, and as such, the module will not respond to even, single-byte accesses. However, word accesses may be used, with the understanding that only the odd byte of the word is used to exchange PAMUX data.

The PAMUX data bus is only 8-bits wide, while the PAMUX unit contains 32 points of I/O. To be able to access all 32 points, the PAMUX is composed of 4 consecutive banks of 8 I/O channels (refer to Figure 3-l). Refer to the OPTO 22, PAMUX 4 32 Channel Data Acquisition/Control System manual for information about how to assign each PAMUX unit a base address. With 16 PAMUX units connected to the XVME-202, there will be a block of 64 consecutive banks that could be accessed.

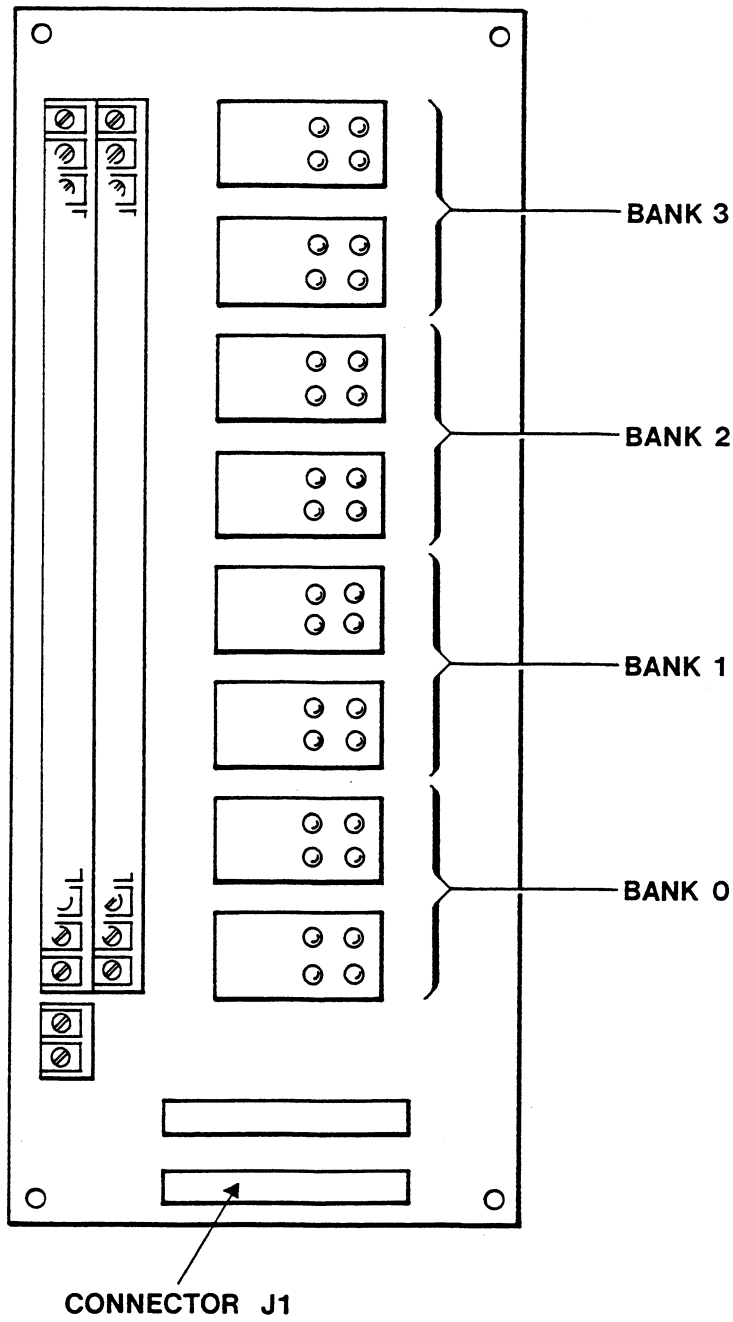


Figure 3-1. PAMUX Banks

3.3 MEMORY MAP

Figure 3-2 shows a simple memory map of the 1K block of the short I/O address space which is occupied by the XVME-202 Module. The block occupied is defined by jumper JA10-JA15 (see Chapter 2).

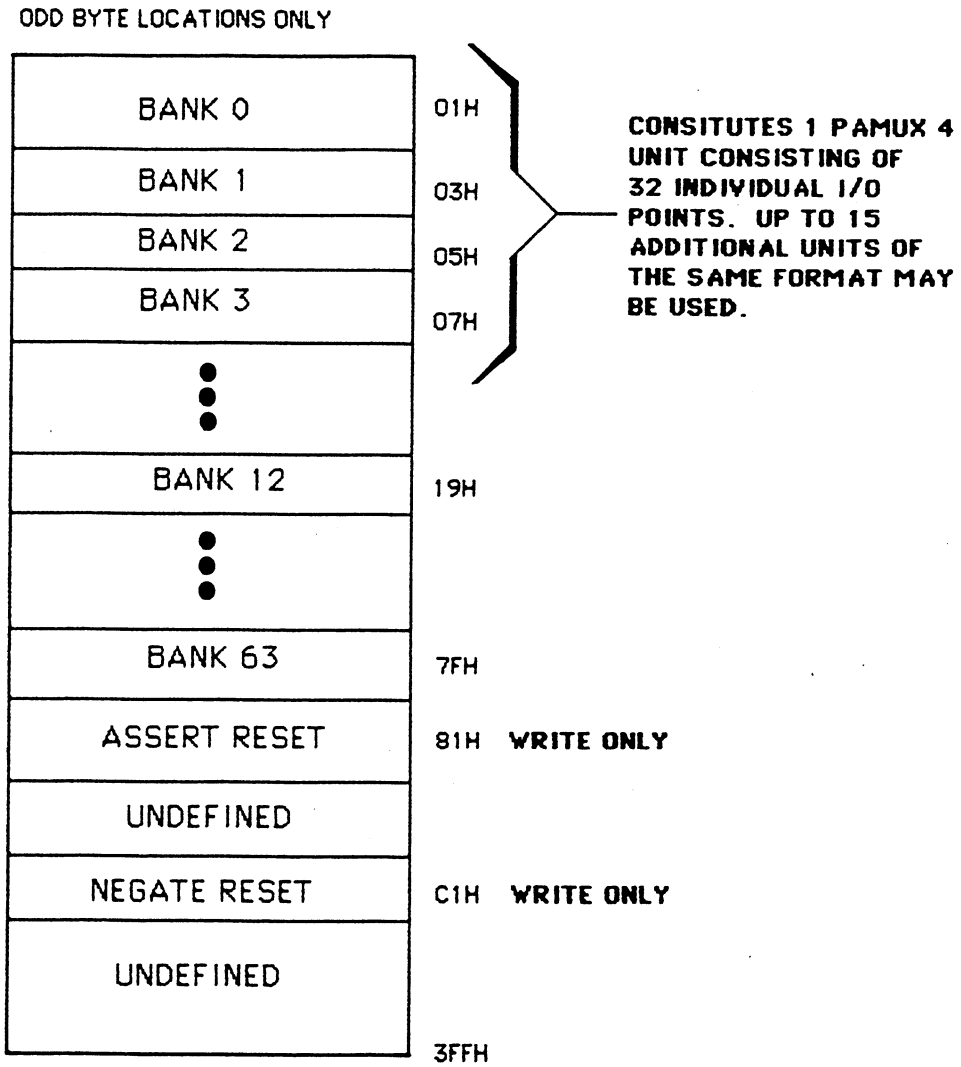


Figure 3-2. Memory Map

3.4 RESET

The PAMUX unit has a Reset line that is used for turning off the relays on all PAMUX units on the bus. On power-up and in response to SYSRESET, the Reset is asserted on the XVME-202 which causes the attached PAMUX units to be reset. The user must deactivate the Reset line by performing a write operation to Base address + C1H. To activate RESET, perform a write operation to Base Address + 81H.

The XVME-202 uses a active low Reset line. Refer to the PAMUX manual for information on how to select the correct Reset polarity on the PAMUX unit.

3.5 READ/WRITE

To read a bank it is necessary to indicate the base address (for example, 1000H plus the bank address. Using the Memory Map (Figure 3-2), if the user needed to read bank 12, they would simply perform a read operation from location 1019H. This is also true if the user wished to write to bank 12.

When the user is writing to a relay bank that has input and output modules, the user MUST make sure that zeros are written to the input module positions. If the user write's a 1 to an input module by mistake, the module will read back as being active even if it is inactive.

3.6 VMEbus ACCESS TIME

The PAMUX unit requires a read/write strobe pulse width of 2 uSec. It then requires another 2 uSec before another read/write strobe can be generated. Therefore, on a read cycle, DTACK will be asserted 2.5 uSec. after the start of the cycle, but the XVME-202 cannot be accessed for another 1.5 uSec. after DTACK. During a write cycle, the data is latched on the module and DTACK will be generated within 500 nSec. If an attempt is made to access the XVME-202 during this time, DTACK will be delayed further. Table 3-1 shows the DTACK access time.

Table 3-1. DTACK Access Time

Description	Typical	Maximum
DSO ASSERTED TO DTACK ASSERTED (READ)	2500nS	2700nS
DSO ASSERTED TO DTACK ASSERTED (WRITE)	500nS	600nS
DSO NEGATED TO DTACK NEGATED	65nS	100nS

Appendix A

VMEbus CONNECTOR/PIN DESCRIPTION

Table A-l. Pl - VMEbus Signal Identification

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
ACFAIL*	lB:3	AC FAILURE: Open-collectors driven signal which indicates that the AC input to the power supply is no longer being provided, or that the required input voltage levels are not being met.
IACKIN*	lA:21	INTERRUPT ACKNOWLEDGE IN: Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKIN* signal indicates to the VME board that an acknowledge cycle is in progress.
IACKOUT*	1A:22	INTERRUPT ACKNOWLEDGE OUT: Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKOUT* signal indicates to the next board that an acknowledge cycle is in progress.
AM0-AM5	1A:23 lB:16,17, 18,19 lC:14	ADDRESS MODIFIER (bits 0-5): Three-state driven lines that provide additional information about the address bus, such as: size, cycle type, and/or DTB master identification.
AS*	lA:l8	ADDRESS STROBE: Three-state driven signal that indicates a valid address is on the address bus.

Table A-1. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
A0l-A23	1A:24-30 lC:15-30	ADDRESS BUS (bits l-23): Three-state driven address lines that specify a memory address.
A24-A31	2B:4-11	ADDRESS BUS (bits 24-31): Three-state driven bus expansion address lines.
BBSY*	1B:l	BUS BUSY: Open-collector driven signal generated by the current DTB master to indicate that it is using the bus.
BCLR*	lB:2	BUS CLEAR: Totem-pole driven signal generated by the bus arbitrator to request release by the DTB master if a higher level is requesting the bus.
BERR*	1C:ll	BUS ERROR: Open-collector driven signal generated by a slave. It indicates that an unrecoverable error has occurred and the bus cycle must be aborted.
BG0IN*- BG3IN*	1B:4,6, 8,l0	BUS GRANT (0-3) IN: Totem-pole driven signals generated by the Arbiter or Requesters. Bus Grant In and Out signals form a daisy-chained bus grant. The Bus Grant In signal indicates to this board that it may become the next bus master.
BG0OUT*- BG3OUT*	1B:5,7, 9,ll	BUS GRANT (0-3) OUT: Totem-pole driven signals generated by Requesters. These signals indicate that a DTB master in the daisy-chain requires access to the bus.

Table A-1. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
BR0*-BR3*	lB:12-15	BUS REQUEST (0-3): Open-collector driven signals generated by Requesters. These signals indicate that a DTB 'master in the daisy-chain requires access to the bus.
DS0*	lA:13	DATA STROBE 0: Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data buss lines (D00-D07).
DSl*	lA:12	DATA STROBE 1: Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines (D08-D15).
DTACK*	lA:16	DATA TRANSFER ACKNOWLEDGE: Open-collector driven signal generated by a DTB slave. The falling edge of this signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
D00-D15	lA:l-8 lC:l-8	DATA BUS (bits 0-15): Three-state driven, bi-directional data lines that provide a data path between the DTB master and slave.
GND	lA:9,11, 15,17,19, 1B:20,23, lC:9 2B:2,12, 22,31	GROUND

Table A-l. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
IACK*	1 A:20	INTERRUPT ACKNOWLEDGE: Open-collector or three-state driven signal from any master processing an interrupt request. It is routed via the backplane to slot 1, where it is looped-back to become slot 1 IACKIN* in order to start the interrupt acknowledge daisy-chain.
IRQl*-IRQ7*	1B:24-30	INTERRUPT REQUEST (1-7): Open-collector driven signals, generated by an interrupter, which carry prioritized interrupt requests. Level seven is the highest priority.
LWORD*	lC:13	LONGWORD: Three-state driven signal indicates that the current transfer is a 32-bit transfer.
(RESERV-ED)	2B:3	RESERVED: Signal line reserved for future VMEbus enhancements. This line must not be used.
SERCLK	lB:21	A reserved signal which will be used as the clock for a serial communication bus protocol which is still being finalized.
SERDAT	1B:22	A reseved signal which will be used as the transmission line for serial communication bus messages.
SYSCLK	lA:10	SYSTEM CLOCK: A constant 16-MHz clock signal that is independent of processor speed or timing. It is used for general system timing use.

Table A-l. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
SYSFAIL*	1C:l0	SYSTEM FAIL: Open-collector driven signal that indicates that a failure has occurred in the system. It may be generated by any module on the VMEbus.
SYSRESET*	lC:12	SYSTEM RESET: Open-collector driven signal which, when low, will cause the system to be reset.
WRITE*	lA:14	WRITE: Three-state driven signal that specifies the data transfer cycle in progress to be either read or written. A high level indicates a read operation, a low level indicates a write operation.
+5V STDBY	lB:31	+5 VDC STANDBY: This line supplies +5 VDC to devices requiring battery backup.
+5v	lA:32 lB:32 1C:32 2B:1,13,32	+5 VDC POWER: Used by system logic circuits.
+12v	lC:31	+12 VDC POWER: Used by system logic circuits.
-12v	lA:31	-12 VDC POWER: Used by system logic circuits.

BACKPLANE CONNECTOR Pl

The following table lists the Pl pin assignments by pin number order. (The connector consists of three rows of pins labeled rows **A,** B, and C.)

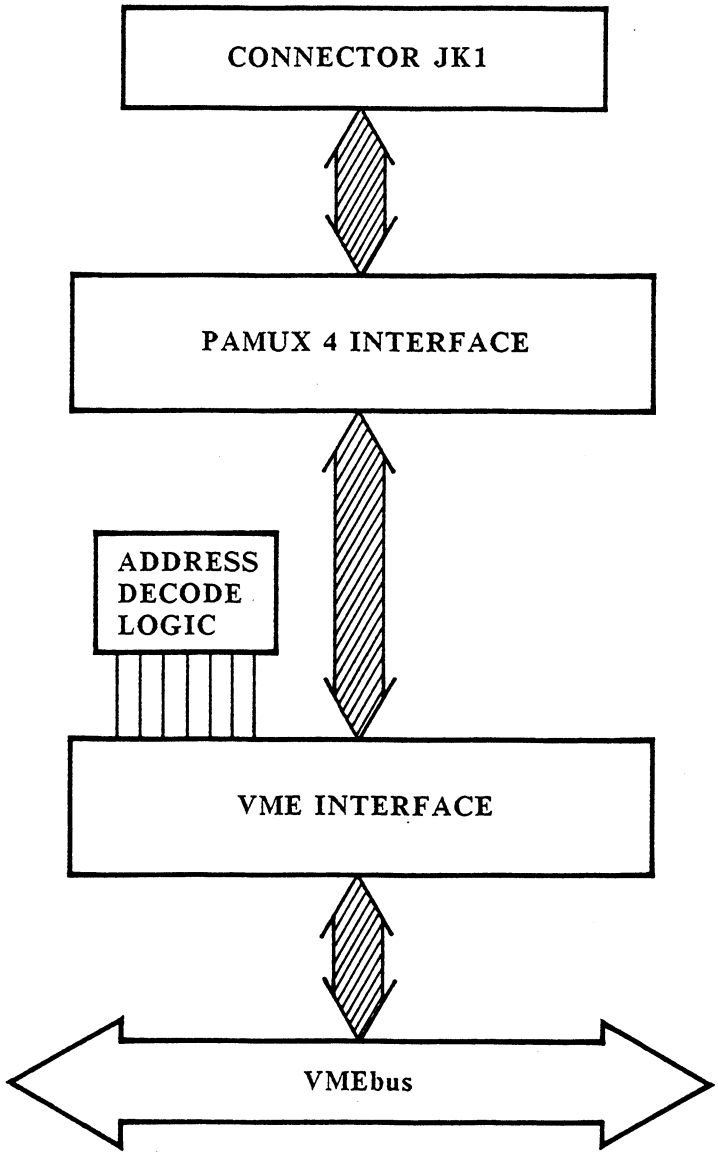
Table A-2. Pl Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D00	BBSY *	**DO8**
2	D01	BCLR*	**DO9**
3	DO2	ACFAIL*	Dl0
4	DO3	BGOIN*	Dll
5	DO4	BGOOUT*	D12
6	**DO5**	BGlIN*	D13
7	DO6	BGlOUT*	D14
8	DO7	BG2IN*	D15
9	GND	BG20UT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DSl*	BRO*	SYSRESET*
13	DSO*	BRl*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS *	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	Al8
21	IACKIN*	SERCLK(1)	A17
22	IACKOUT*	SERDAT(1)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	All
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQl*	A08
31	-12v	+5v STDBY	+12v
32	+5v	+5v	+5v

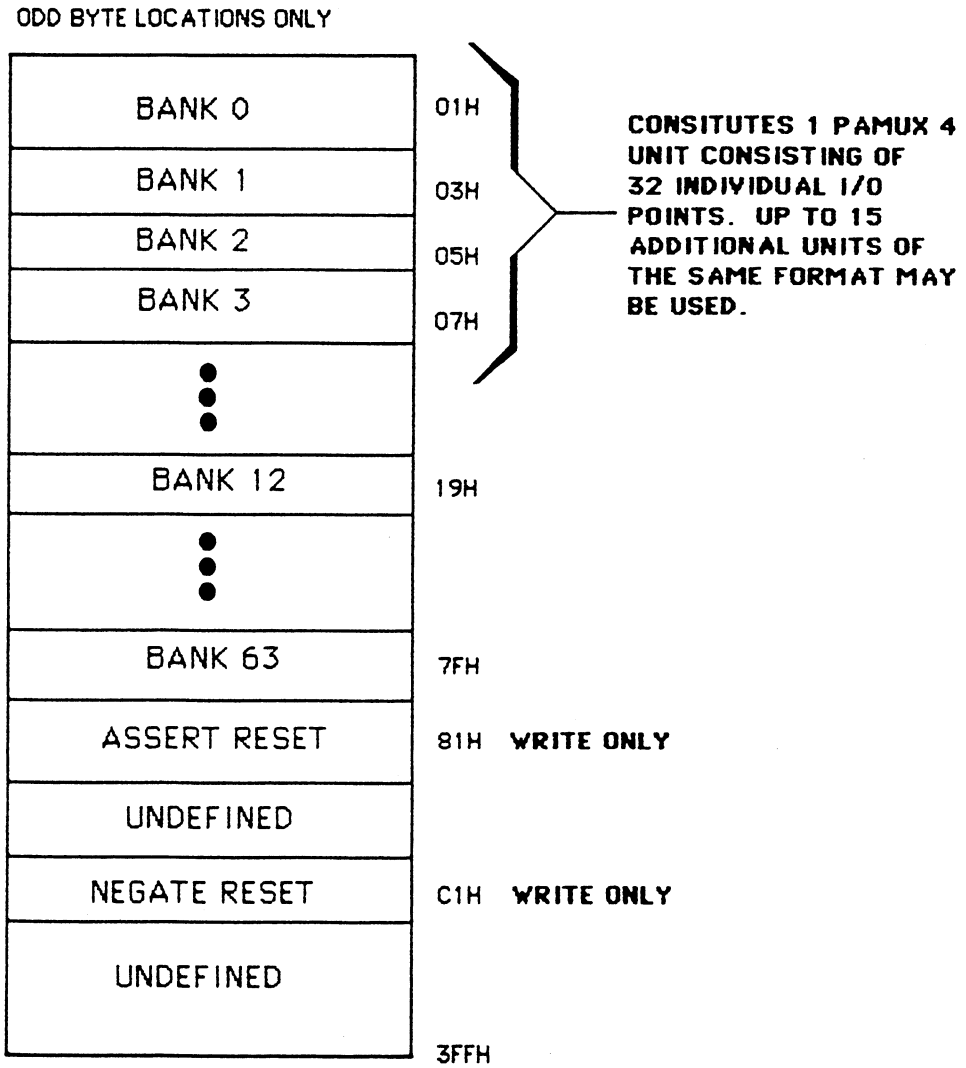
Appendix B

BLOCK DIAGRAM, MEMORY MAP, ASSEMBLY DRAWING, & SCHEMATICS

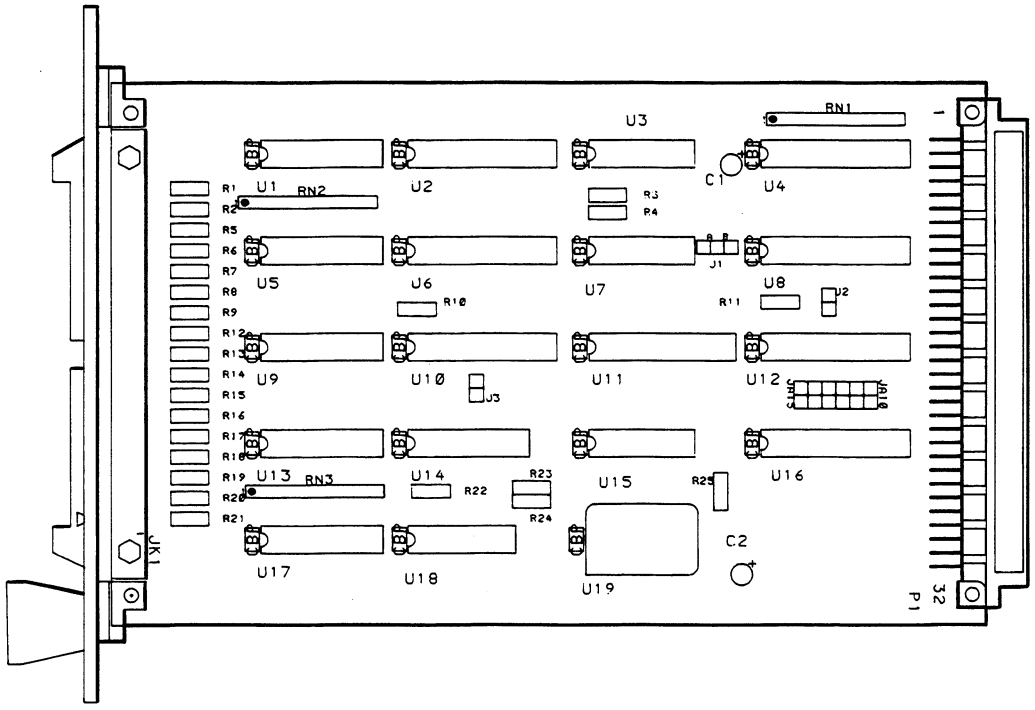
Block Diagram



Memory Map


ODD BYTE LOCATIONS ONLY
BANK 0
BANK 1
BANK 2
BANK 3
BANK 12
BANK 63
ASSERT RESET
UNDEFINED
NEGATE RESET
UNDEFINED
01H
03H
05H
07H
19H
7FH
81H
C1H
3FFH
WRITE ONLY
WRITE ONLY
CONSITUTES 1 PAMUX 4 UNIT CONSISTING OF 32 INDIVIDUAL I/O POINTS. UP TO 15 ADDITIONAL UNITS OF THE SAME FORMAT MAY BE USED.

Assembly Drawing



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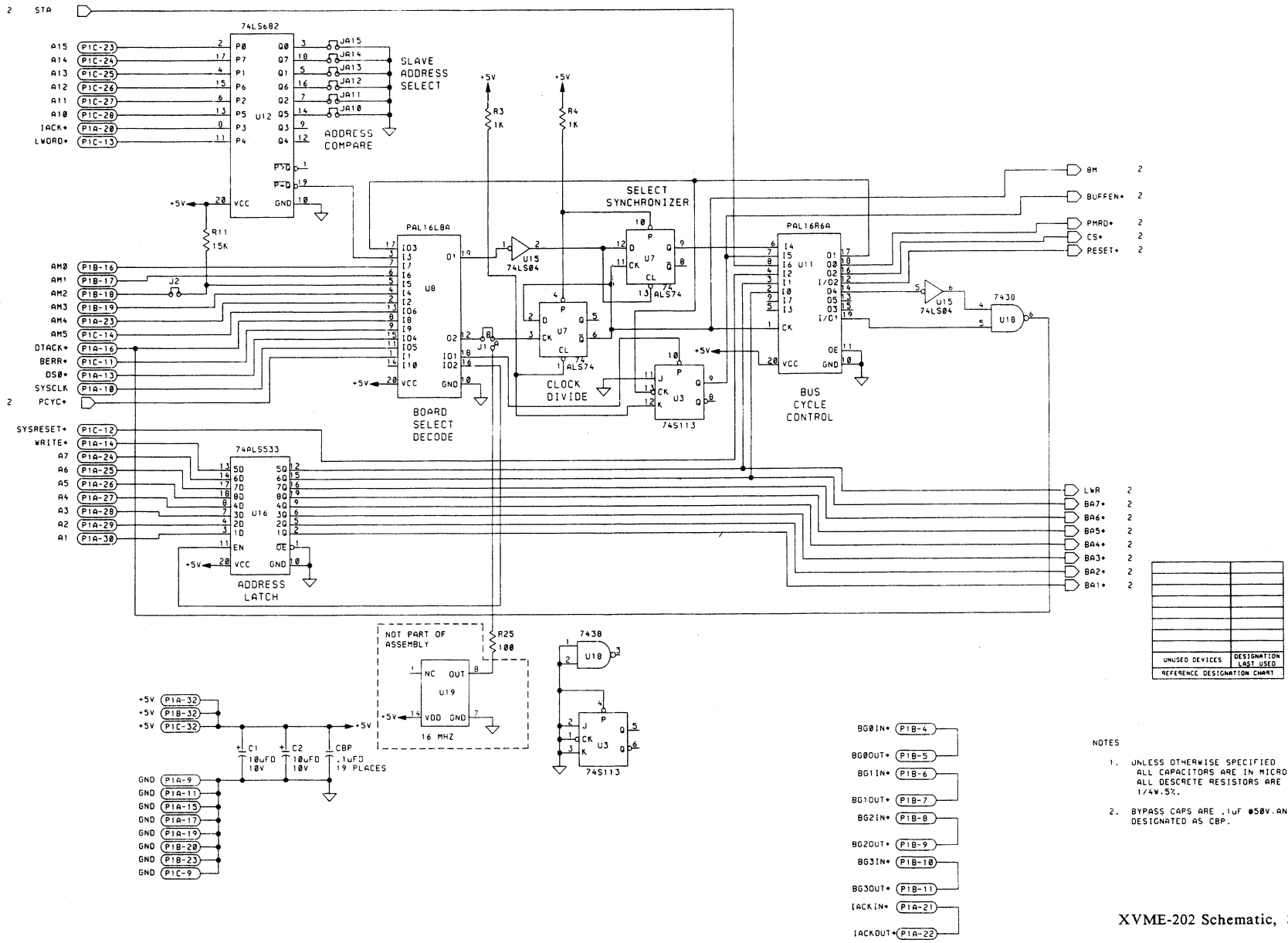
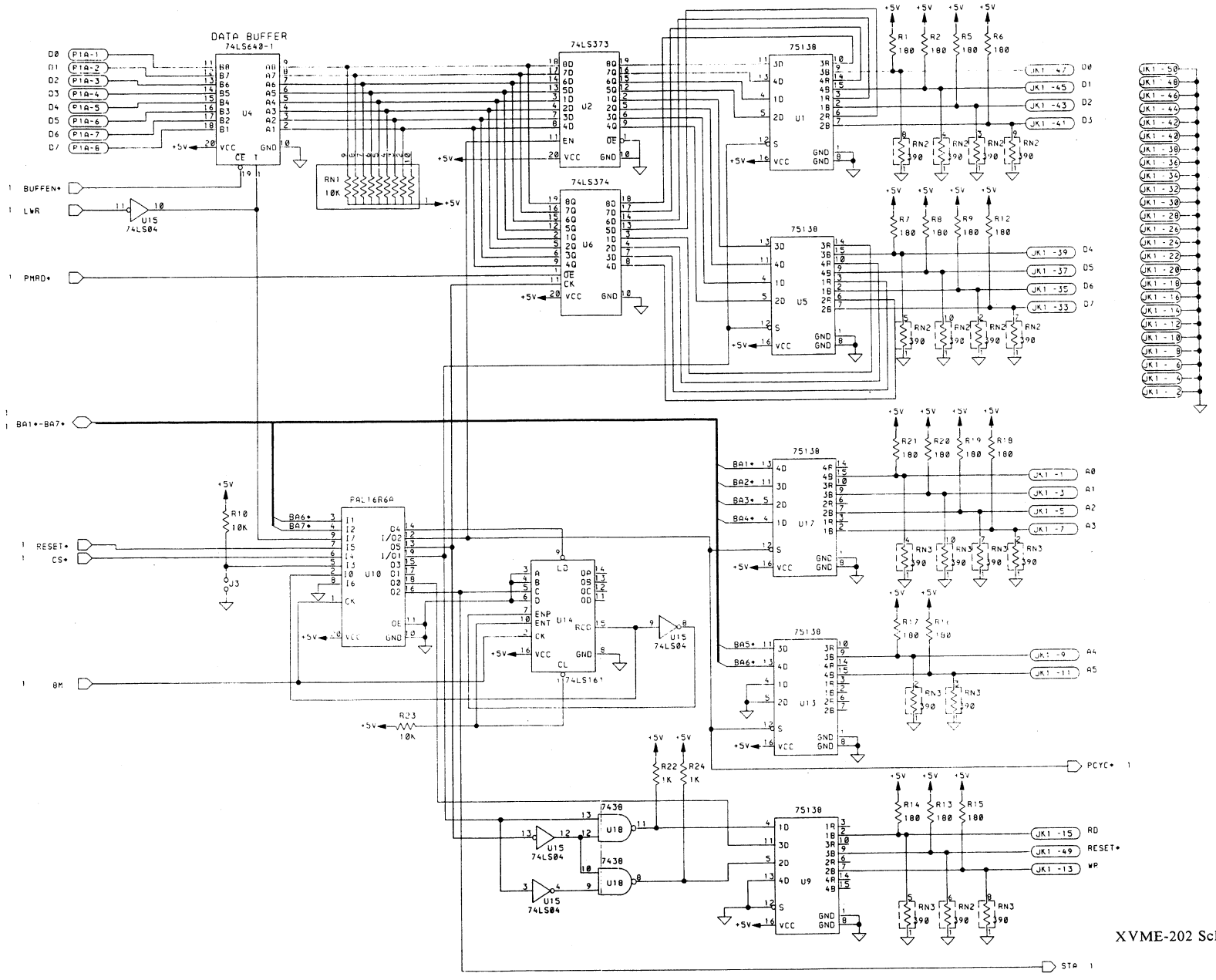


XVME-202 Schematic, Sheet 1 of 2


DATA BUFFER
74LS640-1
74LS373
74LS374
75138
PAL16R6A
74LS161
74LS04
7438
BUFFEN*
LWR
PMRD*
BA1*-BA7*
RESET*
CS*
BM
PCYC*
STA
D0
D1
D2
D3
D4
D5
D6
D7
A0
A1
A2
A3
A4
A5
RD
RESET*
WR

Appendix C

QUICK REFERENCE GUIDE

XVME-202 MODULE JUMPER LIST

JUMPER	USE
J1A	Selects optional on-board oscillator.
J1B	Selects SYSCLK from VMEbus.
J2	Determines whether the module will respond to supervisory or non-privileged short I/O VMEbus cycles (refer to section 2.4.2 of this manual).
JA10-JA15	Select module base address on any one of the 64 1K boundaries within the short I/O address space (refer to Section 2.4.1 of this manual).

Base Address Jumpers

JA15	JA14	JA13	JA12	JA11	JA10	Base Address
IN	IN	IN	IN	IN	IN	0000H
IN	IN	IN	IN	IN	OUT	0400H
IN	IN	IN	IN	OUT	IN	0800H
IN	IN	IN	IN	OUT	OUT	0C00H
IN	IN	IN	OUT	IN	IN	1000H
IN	IN	IN	OUT	IN	OUT	1400H
IN	IN	IN	OUT	OUT	IN	1800H
IN	IN	IN	OUT	OUT	OUT	1C00H
IN	IN	OUT	IN	IN	IN	2000H
IN	IN	OUT	IN	IN	OUT	2400H
IN	IN	OUT	IN	OUT	IN	2800H
IN	IN	OUT	IN	OUT	OUT	2C00H
IN	IN	OUT	OUT	IN	IN	3000H
IN	IN	OUT	OUT	IN	OUT	3400H
IN	IN	OUT	OUT	OUT	IN	3800H
IN	IN	OUT	OUT	OUT	OUT	3C00H
IN	OUT	IN	IN	IN	IN	4000H
IN	OUT	IN	IN	IN	OUT	4400H
IN	OUT	IN	IN	OUT	IN	4800H
IN	OUT	IN	IN	OUT	OUT	4C00H
IN	OUT	IN	OUT	IN	IN	5000H
IN	OUT	IN	OUT	IN	OUT	5400H
IN	OUT	IN	OUT	OUT	IN	5800H
IN	OUT	IN	OUT	OUT	OUT	5C00H
IN	OUT	OUT	IN	IN	IN	6000H
IN	OUT	OUT	IN	IN	OUT	6400H
IN	OUT	OUT	IN	OUT	IN	6800H
IN	OUT	OUT	IN	OUT	OUT	6C00H
IN	OUT	OUT	OUT	IN	IN	7000H
IN	OUT	OUT	OUT	IN	OUT	7400H
IN	OUT	OUT	OUT	OUT	IN	7800H
IN	OUT	OUT	OUT	OUT	OUT	7C00H
OUT	IN	IN	IN	IN	IN	8000H
OUT	IN	IN	IN	IN	OUT	8400H
OUT	IN	IN	IN	OUT	IN	8800H
OUT	IN	IN	IN	OUT	OUT	8C00H
OUT	IN	IN	OUT	IN	IN	9000H
OUT	IN	IN	OUT	IN	OUT	9400H
OUT	IN	IN	OUT	OUT	IN	9800H
OUT	IN	IN	OUT	OUT	OUT	9C00H
OUT	IN	OUT	IN	IN	IN	A000H
OUT	IN	OUT	IN	IN	OUT	A400H
OUT	IN	OUT	IN	OUT	IN	A800H
OUT	IN	OUT	IN	OUT	OUT	AC00H
OUT	IN	OUT	OUT	IN	IN	B000H
OUT	IN	OUT	OUT	IN	OUT	B400H
OUT	IN	OUT	OUT	OUT	IN	B800H

Base Address Jumper Options (Cont'd)

OUT	IN	OUT	OUT	OUT	OUT	BC00H
OUT	OUT	IN	IN	IN	IN	C000H
OUT	OUT	IN	IN	IN	OUT	C400H
OUT	OUT	IN	IN	OUT	IN	C800H
OUT	OUT	IN	IN	OUT	OUT	CC00H
OUT	OUT	IN	OUT	IN	IN	D000H
OUT	OUT	IN	OUT	IN	OUT	D400H
OUT	OUT	IN	OUT	OUT	IN	D800H
OUT	OUT	IN	OUT	OUT	OUT	DC00H
OUT	OUT	OUT	IN	IN	IN	E000H
OUT	OUT	OUT	IN	IN	OUT	E400H
OUT	OUT	OUT	IN	OUT	IN	E800H
OUT	OUT	OUT	IN	OUT	OUT	EC00H
OUT	OUT	OUT	OUT	IN	IN	F000H
OUT	OUT	OUT	OUT	IN	OUT	F400H
OUT	OUT	OUT	OUT	OUT	IN	F800H
OUT	OUT	OUT	OUT	OUT	OUT	FC00H

Addressing Options

Jumper J2	Address Modifier that the Module will respond to
In	(2DH) Supervisory Only
Out	(2DH) Supervisory or (29H) Non-privileged

PAMUX Pin Out

JK1 Pin	Signal	JK1 Pin	Signal
1	A0	33	D7
3	A1	35	D6
5	A2	37	D5
7	A3	39	D4
9	A4	41	D3
11	A5	43	D2
13	WRITE STROBE	45	D1
15	READ STROBE	47	D0
49	RESET		

NOTE: All even numbered pins on connector JK1 are tied to logic ground.