AdvancedMC®

EP8641A 1.1 (DES0222)
User Manual

Developing Embedded Applications and Products
Utilizing Freescale™ MPC86xx Integrated Host Processors

P5010000087RA00

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Introduction

Chapter 1

The EP8641A board is a single-width, full-height advanced mezzanine card (AMC) based on the Freescale MPC8641D Integrated Host Processor. The EP8641A board can operate as an AdvancedMC module within an AdvancedTCA® system when plugged into an ATCA® carrier or MicroTCA® chassis. The board can also operate as a stand-alone module for rapid application development outside of the integrated ATCA or MicroTCA environment.

Functions

The functions included on the EP board are listed in Table 1-1.

Table 1-1. Hardware Features

Entity	Function
Form factor	Single-width, full-height AMC.0 compliant
Processor	MPC8641D (up to 1.5 GHz)
SDRAM	512 MBytes, x64 DDR2: - 256 MBytes, DDR controller 1 - 256 MBytes, DDR controller 2
FLASH	Up to 128 MBytes, x32
Ethernet	2 10/100/1000, front panel RJ-45
	2 10/100/1000, AMC connector port 0 and port 1
Serial port	2-wire RS-232, front panel RJ-45
Serial RIO	AMC.4 compliant x1/x4 data, AMC connector port 4, 5, 6, 7 1.25, 2.5, or 3.125 Gbaud; 8b/10b encoding
Debug	JTAG/COP port access for software debug and programming
Power requirements	12 VDC @ 5A maximum from barrel connector (stand-alone) or via AMC backplane connector 3.3 VDC @ 100 mA maximum via AMC backplane connector
Operating temperature[1]	0° C to 70° C (32° C to 158° F)

NOTES:
1. Contact Embedded Planet for information about an industrial temperature version board.
2. The means of disconnection from the mains power supply is the plug.
3. No serviceable parts.

First Steps

While it may be tempting to jump right into application development, it is recommended that you take a few minutes to review the Getting Started material, paying special attention to the following recommended first steps.

1. Register your EP board; go to Support at www.embeddedplanet.com.

2. Complete the steps in Chapter 3 when ready to connect and powerup the EP board for development.

Reminder

You must register your EP board to become eligible for customer assistance or more detailed technical support from Embedded Planet. Refer to ***Customer Support*** in this chapter.

How to Use This Manual

1. Refer to Chapter 2 for a description of the board features and functions.

2. Refer to Chapter 3 for quick start information: connection, configuration, and powerup.

3. Refer to Chapter 4 for setup information including switch and jumper settings.

4. Refer to Chapter 5 for a description of the connectors and headers available on the board.

5. Refer to Chapter 6 for information about the operation of the EP board.

6. Refer to Chapter 7 for memory map and interrupt information.

About Embedded Planet

Embedded Planet is a leading single board computer and embedded systems solution provider. Our capabilities range from standard off the shelf single board computer products and embedded operating systems to full custom design and intellectual property solutions.

In 1997, Embedded Planet pioneered the Design, Develop, Deploy process for embedded systems engineering. This process allows our customers to take advantage of production tested, reusable product designs in all phases of system development to reduce time to market, project risk, and development costs.

Design

Embedded Planet products help remove risk and shorten the design cycle through production tested, integrated hardware and software designs. CPU module design is becoming more complicated with advanced memory interfaces and highly integrated communications processors. Our production proven modules help OEMs eliminate the risky and time intensive design and verification of the CPU module and focus on their value added application.

Develop

Embedded Planet products provide early access to production modules for all members of the engineering team to allow for a parallel development path. Software developers get access to turnkey platforms with the operating system of their choice ready to run out of the box. Hardware developers gain access to pro-

duction designs and prototyping systems to test advanced system functionality. Fully integrated software and hardware platforms simplify and shorten the development cycle.

Deploy

Embedded Planet products are ready to go to market today. Our designs are production proven and ready to be manufactured in quantity. We offer full lifecycle management to simplify the deployment of your embedded solution.

Customer Support

Embedded Planet provides complete support for our product line. Embedded Planet technical support includes product assistance for EP firmware and hardware. Technical support can assist with setup, installation, configuration, documentation, product related questions, and expansion guidelines. Second level software support for SDP's is handled through our partners. We also provide development tools for all of our PowerPC boards.

Using our online support system our technical support engineers can assist you with questions regarding Embedded Planet products. Via a browser our support team can access your system directly and quickly answer your technical questions. Please contact us today to learn more; refer to ***Contact Embedded Planet*** in this chapter.

Contact Embedded Planet

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Document Conventions

This document uses standard text conventions to represent keys, display items, and user data inputs:

Display Item

Italic - Identifies an item that displays on the screen such as a menu option or message (e.g., *File* > *Open*).

User Data Input

Bold - Identifies any part of a command or user entry that is not optional or variable and must be entered exactly as shown.

Italic - Identifies any part of a command or user entry that is a variable parameter.

[ ] - Identifies any part of a command or user entry that is an optional parameter; text within the brackets follows the previously described conventions.

KEY - Identifies a specific key that is not alphabetic, numeric, or punctuation:

Press **ENTER**
Press **ESC V M** (press and release each key in sequence)
Press **CTRL-ALT-DEL** (press all keys in sequence simultaneously).

File Names

`Name` - Indicates a file or directory name. Example:

```
file.h
/bin
```

Reference Documents

- MPC8641D Integrated Host Processor Reference Manual
- AMC.0 R1.0, Advanced Mezzanine Card, Base Specification
- AMC.4 Rx.x, Advanced Mezzanine Card, Serial RapidIO

Description

Chapter 2

This chapter provides some description of the EP8641A board features including the PowerPC processor, external interfaces, and u-boot firmware. Figure 2-1 is a simplified block diagram of the EP board. Figures 2-2 and 2-3 show the top and bottom views of the board layout. These figures show the headers unpopulated (i.e., without pins or connectors).

NOTE: JP1 shown in Figure 2-2 is intended for development purposes only and should **not** be populated during normal operating conditions.

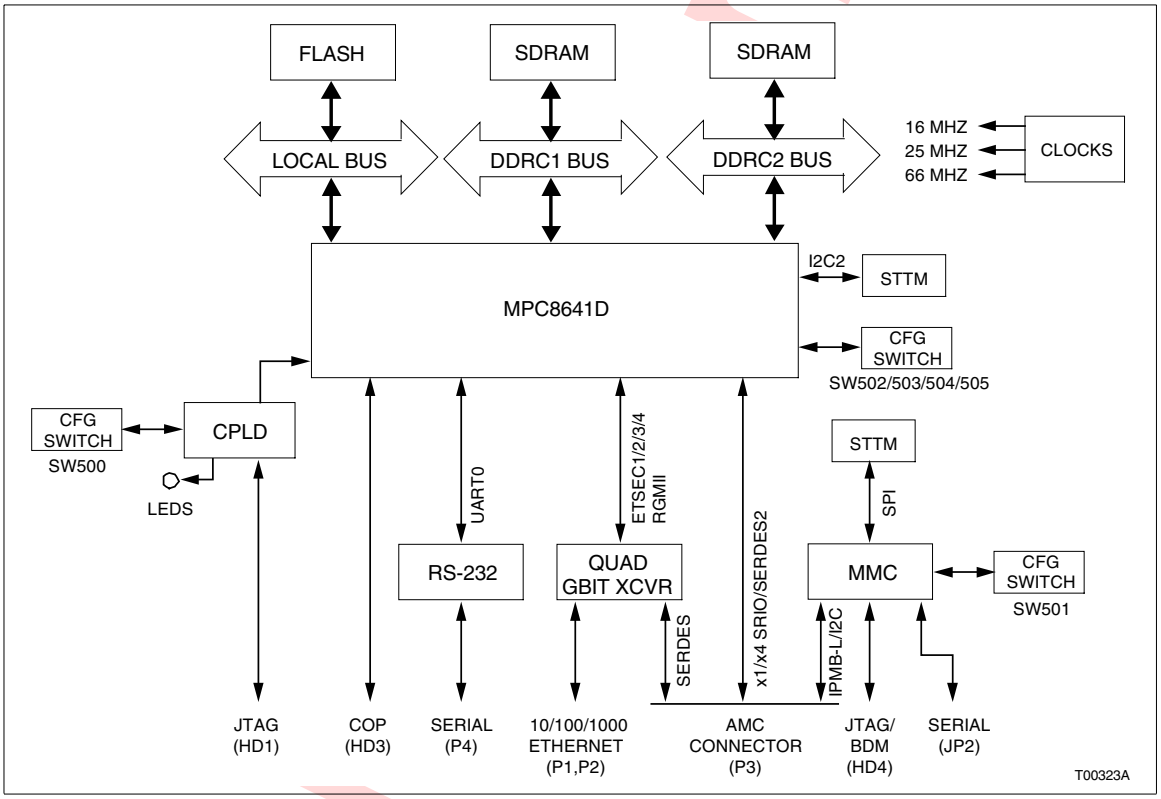

Figure 2-1. Simplified Block Diagram

MPC8641D — Refer to ***PowerPC Processor*** in this chapter.

Clocks — All of the clocks used on the EP board are generated locally. There are three distinct clocking environments on the board:

- System and real-time clocks.
- Ethernet clock.
- SERDES clock.

An onboard 66 MHz clock oscillator (ECS-3953C or equivalent) generates the system clock (SYSCLK) input to the MPC8641D processor. This is the primary clock

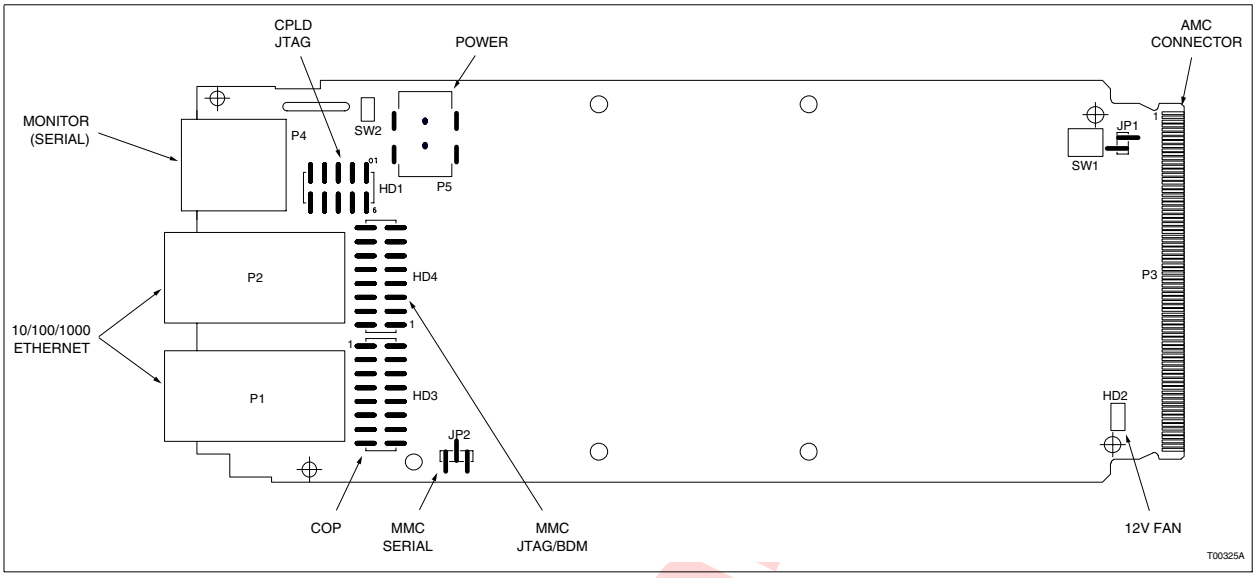

Figure 2-2. EP Board - Top View

input to the device. An onboard 16 MHz clock oscillator (ECS-3953C or equivalent) generates the real-time clock (RTC) input to the processor. This clock input can be used to clock the global timers in the programmable interrupt controller (PIC) of the processor. A second onboard 66 MHz clock oscillator provides a clock input to the CPLD for timing.

An onboard 25 MHz crystal oscillator (FX532 or equivalent) provides the clock input needed by the Ethernet transceiver. The Ethernet controller (eTSEC) of the processor requires a 125 MHz external clock input. The Ethernet transceiver generates the 125 MHz clock to the processor (EC1_GTX_CLK125, EC2_GTX_CLK125) from its 25 MHz clock input.

The high-speed SERDES interface of the processor requires either a 100 MHz or 125 MHz LVDS clock reference to operate SRIO at either 1.25, 2.5, or 3.125 Gbaud. A frequency synthesizer device (ICS840001-34) generates the 100 MHz or 125 MHz clock from an onboard 25 MHz crystal oscillator (FX532 or equivalent) input. An LVDS clock fan-out buffer (ICS8545) selects either the 100 MHz or 125 MHz single-ended input and distributes it to the processor as an LVDS reference clock (SD2_REF_CLK, $\overline{\text{SD2\_REF\_CLK}}$).

NOTE: An option to clock the SERDES interface from CLK3 of the AMC connector is provided. Additionally an option to source CLK3 to the AMC connector is provided. These options are controlled from a BCSR register; refer to Table 4-10.

Memory

The board has DDR2 SDRAM memory and FLASH memory (Table 1-1).

The processor supports two DDR controller interfaces: DDRC1 and DDRC2. The board is typically configured as shown in Table 1-1 with both DDRC1 memory and DDRC2 memory populated. Each bank has a 64-bit bus width; refer to ***SDRAM Organization*** in this chapter for additional information. There is no ECC option.

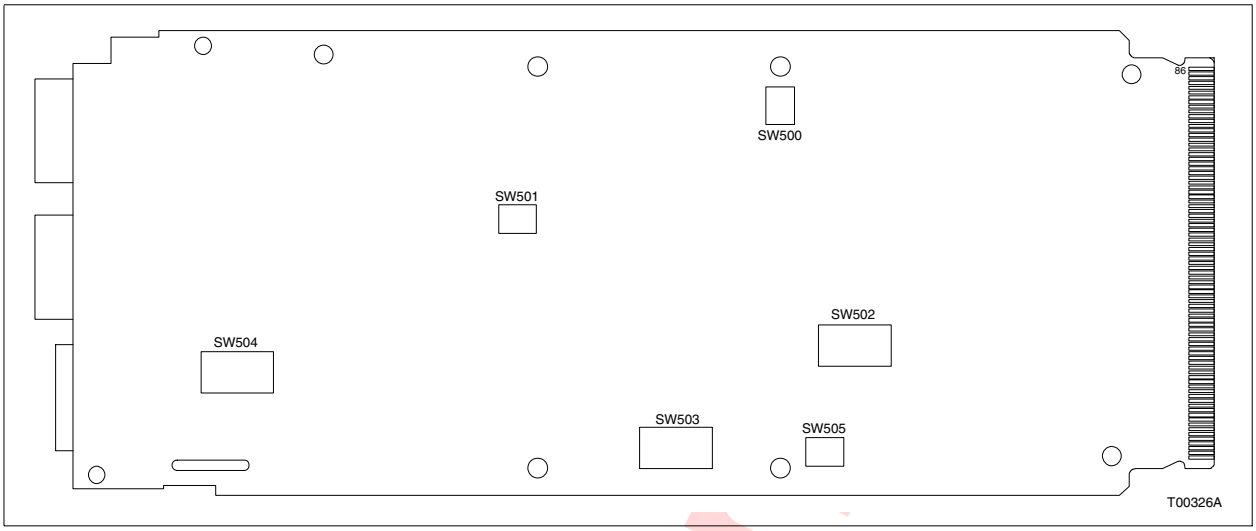

Figure 2-3. EP Board - Bottom View

The FLASH memory is Spansion™ MirrorBit. The memory bus is 32-bit bus width; refer to ***FLASH Organization*** in this chapter for additional information.

NOTE: The local bus address and data lines are multiplexed. An external demultiplexer, controlled by the LBC address latch enable (LALE) and LBC data buffer control (LBCTL) signals, is used to separate the address and data bus.The local bus is buffered using two bus transceiver (SN74ALVCH32973 or equivalent).

RS-232

There is one RS-232 serial port available at the front panel (P4). The port communicates via UART0 of the processor. The serial port uses an Intersil ICL3225E RS-232 transceiver or equivalent.

Ethernet

There are two 10/100/1000 Ethernet ports available at the front panel (P1, P2). Two additional 10/100/1000 Ethernet ports are available at the AMC connector.

The Ethernet ports communicate via eTSEC1, eTSEC2, eTSEC3, and eTSEC4 of the processor and use a Marvell® 88E1145 quad transceiver device. The interface to the processor is RGMII.

Port 3 of the transceiver device routes to AMC port 0 and port 4 of the transceiver device routes to AMC port 1 in the common options region of the AMC port mappings. The interface to the AMC connector is SERDES using SGMII protocol. An external PHY or SERDES device is required to complete the interface to the media.

The MII management connection (MDC/MDIO) to the processor is for configuration and monitoring of the transceiver device. The default Ethernet PHY addresses are 0b00000, 0b00001, 0b00010, and 0b00011 respectively.

STTM

There is one serial temperature and thermal monitor (STTM) device on the local I2C bus. The STTM part is a 2-wire, digital temperature sensor. Its functionality is equivalent to the Microchip TCN75 part. The minimum resolution provided by this part is a 9-bit temperature conversion. The STTM address is hard-wired to 0x90 (0b1001000x).

COP/JTAG

The HD3 header provides access to the COP port of the processor for debug access. The HD1 header provides access to the CPLD JTAG port for programming.

MMC

The module management controller (MMC) funtionality required for AMC.0 compliance is implemented in an MCF5213 Coldfire processor. The MMC communicates with the ATCA carrier or microTCA carrier hub over the IPMB-L bus using I2C protocol. The carrier and MMC communicate through a limited set of IPMI commands.

Two serial temperature sensors and internal FLASH memory implement the temperature sensor and FRU information storage device requirements for AMC.0 compliance. The temperature devices are accessed via the SPI bus of the Coldfire processor. Additionally access to the RS-232 serial port and JTAG/BDM port of the Coldfire processor are provided for development purposes.

Refer to Chapter 5 for more information and pinouts for the connectors.

PowerPC Processor

The EP board incorporates an MPC8641D dual-core, integrated host processor. This 32-bit processor includes an integrated PowerPC core and peripheral interfaces that can be used in a variety of embedded networking, telecom, military, storage, and pervasive computing applications. The MPC8641D processor incorporates:

- e600 core scaling up to 1.5 GHz.
- Dual DDR memory controllers operating at up to 667 MHz data rate.
- Local bus controller operating at up to 166 MHz.
- Dual UART (DUART).
- Dual I2C interfaces (master or slave mode).
- Serial RapidIO interface unit.
- PCI Express interface unit (not accessible on EP board).
- Four enhanced three-speed Ethernet controllers (eTSEC).
- Programmable interrupt controller (PIC).
- Four-channel DMA controller.
- Device performance monitor.

SDRAM Organization

Memory Clock

The DDR SDRAM clock speed is generated internal to the CPU and is 1/2 the platform clock (i.e., MPX bus clock). The maximum is 600 MHz data rate (300 MHz clock) for the MPC8641D processor with a 66 MHz SYSCLK.

256 MByte

512 Mbit (32M × 16 bit) devices
4 Micron MT47H32M16 or equivalent
16 MBytes × 4 banks × 4 devices = 256 MBytes total
2 bit bank address (BA0-BA1)
13 bit row address (A0-A12)
10 bit column address (A0-A9)

FLASH Organization

The FLASH memory on the EP board is accessed using the general purpose chip select machine (GPCM) of the processor. Figure 2-4 shows the address and data line connections. An offset is needed when issuing commands to the FLASH devices due to the address line connections.

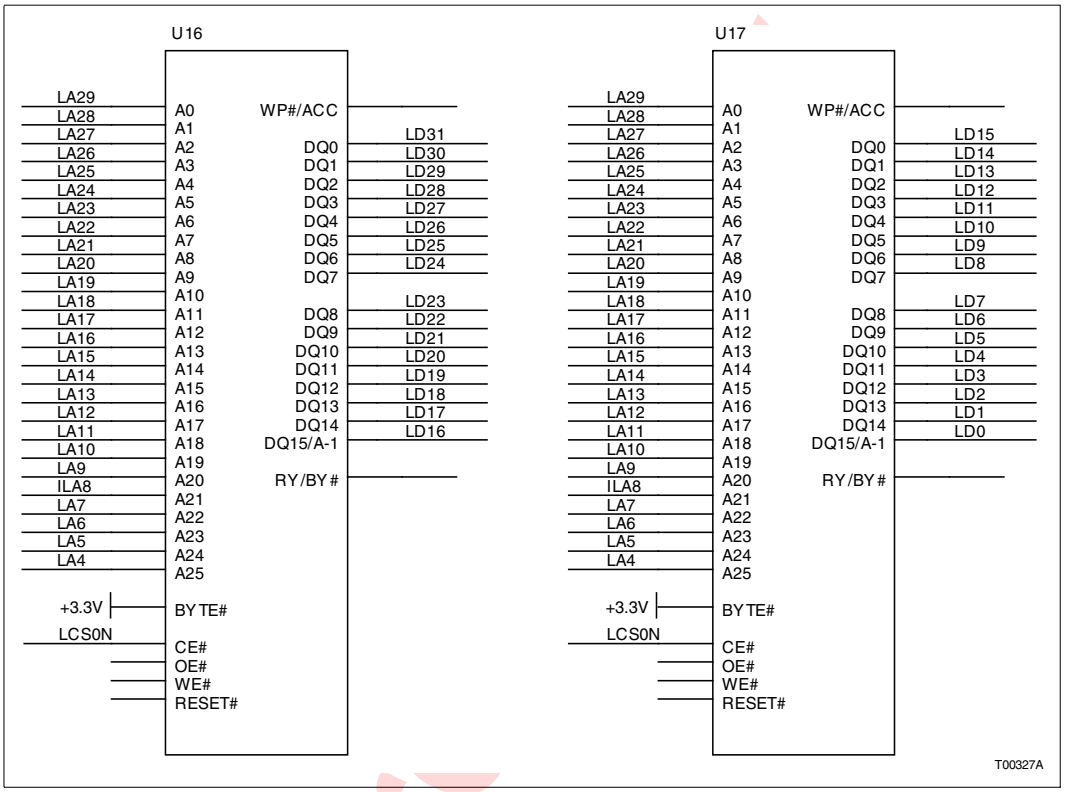

Figure 2-4. FLASH Address and Data Lines

Table 2-1 lists the FLASH memory devices and their device IDs that are currently supported on the board. Refer to the Spansion datasheets for detailed information about the FLASH memory devices. Command codes for all Spansion devices are the same. Device ID varies among the different devices. Sector addresses also vary among the different devices.

Table 2-1. FLASH Devices

Device	MFG ID	Device ID
S29GL128	0001	0x2101
S29GL256		0x2201
S29GL512		0x2301

The following guidelines apply to x32 ported FLASH memory:

- FLASH devices configured in 16-bit mode.
- Sector and chip erases should be performed only on a long word (32-bit) basis.
- Programming should be done on a long word (32-bit) basis if possible.

Processor I/O Interface Signals

Table 2-2 lists the processor I/O interface signals used on the EP board.

Table 2-2. I/O Signals

Interface	Signal
Serial	UART_SOUT0
	UART_SIN0
	UART_SOUT1
	UART_SIN2
Ethernet	EC_MDC
	EC_MDIO
	EC1_GTX_CLK125
	EC2_GTX_CLK125
	TSEC1_TXD[3:0]
	TSEC1_TX_EN
	TSEC1_GTX_CLK
	TSEC1_RXD[3:0]
	TSEC1_RX_DV
	TSEC1_RX_CLK
	TSEC2_TXD[3:0]
	TSEC2_TX_EN
	TSEC2_GTX_CLK
	TSEC2_RXD[3:0]
	TSEC2_RX_DV
	TSEC2_RX_CLK
	TSEC3_TXD[3:0]
	TSEC3_TX_EN
	TSEC3_GTX_CLK
	TSEC3_RXD[3:0]
	TSEC3_RX_DV
	TSEC3_RX_CLK
	TSEC4_TXD[3:0]
	TSEC4_TX_EN
	TSEC4_GTX_CLK
	TSEC4_RXD[3:0]
	TSEC4_RX_DV
	TSEC4_RX_CLK

Table 2-2. I/O Signals *(continued)*

Interface	Signal
I2C	IIC1_SDA
	IIC1_SCL
	IIC2_SDA
	IIC2_SCL
SRIO	SD2_TX[4:7]
	$\overline{\text{SD2\_TX[4:7]}}$
	SD2_RX[4:7]
	$\overline{\text{SD2\_RX[4:7]}}$
	SD2_REF_CLK
	$\overline{\text{SD2\_REF\_CLK}}$

Operating Modes

The EP board can operate in two different modes:

- Stand-alone mode.
- AdvancedMC mode.

Stand-alone mode is primarily intended for development; AMC mode provides the ability to use the same development board in a carrier card or chassis environment. SW500 determines stand-alone or AMC mode operation; refer to Table 4-10.

Thermal

The MPC8641D processor is fitted with a heat sink. The choice of size and type of heat sink is dependant on the environment in which the board is operating. Factors such as processor speed, ambient temperature, and air flow all dictate the specific characteristics of the heat sink required. Additionally, the choice of heat sink is dependant on the space available which is ultimately determined by the mechanical constraints of the system in which the EP board will operate. The heat sink used when the card is situated in a chassis environment with forced air flow will differ from that used when the card operates stand-alone. Refer to the ***MPC8641D Reference Manual*** for the processor thermal characteristics.

Firmware

U-boot is open source firmware for the embedded PowerPC architecture. It can be installed in a boot ROM and used to initialize and test hardware or to download and run application code.

The EP8641A board is shipped with the u-boot firmware residing in FLASH memory. U-boot loads at the address 0xFFF00000. U-boot utilities provide the ability to initialize the board and auto execute an operating system or application. Refer to online u-boot documentation for complete information about u-boot and its utilities.

Restoring MAC Addresses

The EP board has four media access control (MAC) address assigned to it. The MAC address is the physical address of a device connected to a network, expressed as a 48-bit hexadecimal number. The EP boards are assigned MAC addresses during manufacture using the following convention:

Enet controller 1 MAC = 0x0010ECxxxxxx ORed with 0x000000000000
Enet controller 2 MAC = 0x0010ECxxxxxx ORed with 0x000000800000
Enet controller 3 MAC = 0x0010ECxxxxxx ORed with 0x000000400000
Enet controller 4 MAC = 0x0010ECxxxxxx ORed with 0x000000C00000

where

xxxxxx	EP board serial number. The serial number can be found in decimal form on a label affixed to the Ethernet port on the board (e.g., 007573).

For example, a board with a serial number of 007573 decimal (001D95 hexadecimal) has a MAC address of:

00:10:EC:00:1D:95 for Enet controller 1
00:10:EC:80:1D:95 for Enet controller 2

If it becomes necessary to restore a missing or corrupted MAC address, use the above procedure to determine the EP board's MAC addresses and issue the following commands in u-boot:

setenv ethaddr *<MAC ADDRESS1>* **ENTER**

setenv eth1addr *<MAC ADDRESS2>* **ENTER**

setenv eth2addr *<MAC ADDRESS3>* **ENTER**

setenv eth3addr *<MAC ADDRESS4>* **ENTER**

saveenv ENTER

Getting Started

Chapter 3

This chapter describes how to get the EP board up and running in stand-alone mode including initial configuration, connection, and powerup. The board comes preprogrammed with u-boot firmware. An RS-232 serial monitor connection is required to access u-boot utilities. A network connection is required to transfer files to the EP board using TFTP.

To start up and begin communicating with the EP board:

1. Verify the switches are configured properly for stand-alone operation; refer to Chapter 3.

2. Establish a serial connection; refer to ***Serial Monitor Connection*** in this chapter.

3. Establish a network connection, if required; refer to ***Network Connection*** in this chapter.

4. Apply power; refer to ***Power Up*** in this chapter.

Serial Monitor Connection

A terminal emulator program on the host machine (e.g., minicom, Tera Term, or HyperTerminal) or a dumb terminal is required to interact with the EP board. To establish a serial monitor connection with the host system:

1. Connect the RJ-45 patch cable to the RJ-45 monitor port (Fig. 2-2).

2. Connect the opposite end of the RJ-45 cable to the RJ-45 to DB-9 adapter.

3. Connect the DB-9 adapter to a serial port on the host machine (or dumb terminal).

The default settings for the monitor port are:

- 115200 baud.
- 8 data bits.
- 1 stop bit.
- No parity.
- No flow control.

Network Connection

A network connection between the development target (i.e., EP board) and host system is needed if planning to use TFTP services to transfer files to the EP board. A TFTP server must be running on the host machine to use the network connection for file transfer. Connect to the EP board in one of two ways: directly or through a network hub or switch.

Direct

To directly connect to the host machine, use a Ethernet crossover cable connected between the RJ-45 Ethernet port on the EP board (Fig. 2-2) and the Ethernet port on the host machine.

Hub or Switch

To connect to the host machine via a hub or switch, use a standard Ethernet patch cable connected between the RJ-45 Ethernet port on the EP board (Fig. 2-2) and a free port on the hub.

NOTE: Most new Ethernet cards, hubs, and switches have auto-crossover capabilities which means the same cable may be able to be used for either direct, hub, or switch connection.

Power Up

NOTE: Start the terminal emulation program (e.g., minicom, Tera Term, or HyperTerminal) or make sure the dumb terminal is connected before powering up the EP board.

When operating stand-alone, an external cooling fan is required. Optionally, a 12 VDC fan can be powered from the fan header (HD2) of the EP board; refer to Table 5-7. The fan should be placed next to the board and in a position so as to maximize airflow over the processor.

After all connections have been properly made, connect the 12 VDC power supply to the barrel connector P5 (Fig. 2-2). The EP board will boot up into u-boot automatically. Refer to online u-boot documentation for complete information about u-boot and its utilities.

Setup

Chapter 4

This chapter describes the various configuration switches that setup the EP8641A board for operation.

NOTE: JP1 shown in Figure 2-2 is intended for development purposes only and should **not** be populated during normal operating conditions.

Processor Clock Configuration

Switches SW503 and SW504 configure the processor clock options. Tables 4-1 through 4-3 describe the configuration options. Refer to Figure 2-3 for the location of the switch.

Table 4-1. MPX Clock PLL Ratio Configuration (SW503[1:4])

Option 1 2 3 4 5 6 7 8	MPC:SYSCLK
0 0 0 0 x x x x	16:1
0 0 1 0 x x x x	2:1
0 0 1 1 x x x x	3:1
0 1 0 0 x x x x	4:1
0 1 0 1 x x x x	5:1
0 1 1 0 x x x x	6:1
1 0 0 0 x x x x	8:1
1 0 0 1 x x x x	9:1

NOTES:
1. on = closed position = logic 0; off = open position = logic 1.
2. Refer to the ***MPC8641D Reference Manual*** for additional information.

Table 4-2. e600 Core Clock PLL Ratio Configuration (SW504[1:5])

Option 1 2 3 4 5 6 7 8	e600:MPX
0 1 0 0 0 x x x	2:1
0 1 1 0 0 x x x	2.5:1
1 0 0 0 0 x x x	3:1
1 1 1 0 0 x x x	3.5:1
1 0 1 0 0 x x x	4:1
0 1 1 1 0 x x x	4.5:1

NOTES:
1. on = closed position = logic 0; off = open position = logic 1.
2. Refer to the ***MPC8641D Reference Manual*** for additional information.

Table 4-3. Platform Frequency Configuration (SW504[6])

Option 1 2 3 4 5 6 7 8	Description[1]
x x x x x 0 x x	Platform frequency (MPX clock) 400 MHz or less
x x x x x 1 x x	Platform frequency (MPX clock) 500 MHz or greater

NOTES:
1. Must be set consistent with MPX clock PLL ratio; refer to Table 4-1.
2. on = closed position = logic 0; off = open position = logic 1.
3. Refer to the ***MPC8641D Reference Manual*** for additional information.

Processor Boot Configuration

Switches SW503 and SW505 configure the processor boot options. Tables 4-4 and 4-5 describe the configuration options. Refer to Figure 2-3 for the location of the switch.

Table 4-4. Boot ROM Location Configuration (SW503[5:8])

Option 1 2 3 4 5 6 7 8	Description
x x x x 0 0 1 0	SRIO
x x x x 0 1 0 0	DDRC1
x x x x 0 1 0 1	DDRC2
x x x x 1 1 1 1	Local bus GPCM, 32-bit; normal operation

NOTES:
1. on = closed position = logic 0; off = open position = logic 1.
2. Refer to the ***MPC8641D Reference Manual*** for additional information.

Table 4-5. CPU Boot Configuration (SW505[3:4])

Option 1 2 3 4	Description
x x 1 x	Boot vector fetched from default boot ROM location 0xFFF00100
x x x 0	Enable CPU boot hold off mode; e600 core 0 is prevented from booting until configured by an external master.
x x x 1	Disable CPU boot hold off mode; normal operation.

NOTES:
1. on = closed position = logic 0; off = open position = logic 1.
2. Refer to the ***MPC8641D Reference Manual*** for additional information.

e600 Core 1 Configuration

Switch SW504 configures the e600 core 1 options. Table 4-6 describes the configuration options. Refer to Figure 2-3 for the location of the switch.

Table 4-6. e600 Core 1 Configuration (SW504[7:8])

Option 1 2 3 4 5 6 7 8	Description
x x x x x x 0 x	Core 1 disabled
x x x x x x 1 x	Core 1 enabled
x x x x x x x 0	Enable low memory offset for e600 core 1; real address A in range 0 to 256 MByte translated to address A + 256 MByte.
x x x x x x x 1	Disable low memory offset for e600 core 1; system address = real address.

NOTES:
1. on = closed position = logic 0; off = open position = logic 1.
2. Refer to the ***MPC8641D Reference Manual*** for additional information.

SRIO Configuration

Switches SW502 and SW505 configure SRIO options. Table 4-7 through 4-9 describe the configuration options. Refer to Figure 2-3 for the location of the switch.

Table 4-7. SERDES Port Configuration (SW502[1:4])

Option 1 2 3 4 5 6 7 8	Description
1 0 0 1 x x x x	SERDES1: disabled SERDES2: x4 SRIO, 3.125 Gbaud interface; 125 MHz reference clock
1 0 1 0 x x x x	SERDES1: disabled SERDES2: x4 SRIO, 2.5 Gbaud interface; 100 MHz reference clock
1 0 1 1 x x x x	SERDES1: disabled SERDES2: x4 SRIO, 1.25 Gbaud interface; 100 MHz reference clock

NOTES:
1. on = closed position = logic 0; off = open position = logic 1.
2. Refer to the ***MPC8641D Reference Manual*** for additional information.

Table 4-8. SRIO Device ID and System Size Configuration (SW502[5:8])

Position	Description
5	cfg_device_id[5]
6	cfg_device_id[6]
7	cfg_device_id[7]
8	0 = large system size; up to 65,536 devices 1 = small system size; up to 256 devices

NOTES:
1. If SRIO host, device ID is cfg_device_id[5:7]. If SRIO agent, device ID is 0xFF ANDed with cfg_device_id[5:7].
2. on = closed position = logic 0; off = open position = logic 1.

Table 4-9. SRIO Host/Agent Configuration (SW505[1:2])

Option 1 2 3 4	Description
0 0 x x	SERDES2: agent
0 1 x x	SERDES2: host
1 0 x x	SERDES2: agent
1 1 x x	SERDES2: host

NOTES:
1. on = closed position = logic 0; off = open position = logic 1.
2. Refer to the ***MPC8641D Reference Manual*** for additional information.

User Options

Switch SW500 provides some additional user options. Table 4-10 describes the options. Refer to Figure 2-3 for the location of the switch.

Table 4-10. User Options (SW500[1:4])

Position	Description
1	Selects operating mode: 0 = stand-alone mode 1 = AMC mode
2	Select SERDES clock source: 0 = SERDES interface clocked from external clock (AMC CLK3) 1 = SERDES interface clocked from local clock
3	Enables or disables inversion of memory interface address bit 8 (LA8) from the CPU to the FLASH memory: 0 = normal FLASH memory bank; LA8 to FLASH is not inverted 1 = alternate FLASH memory bank; LA8 to FLASH is inverted
4	Controls power up of the board in stand-alone mode. If SW500[1] = 1 to select AMC mode, then this bit has no effect: 0 = power enabled 1 = power disabled

NOTE:
on = closed position = logic 0; off = open position = logic 1

MMC Configuration

Switch SW501 configures the MMC processor options. Table 4-11 describes the configuration options. Refer to Figure 2-3 for the location of the switch.

NOTE: This switch is primarily for development purposes. It is factory set and should **not** be changed.

Table 4-11. MMC Configuration (SW501[1:4])

Position	Description
1	RCON; selects serial FLASH programming mode: 0 = enable serial FLASH programming mode 1 = disable serial FLASH programming mode
2	JTAG_EN; selects between debug and JTAG mode: 0 = debug mode 1 = JTAG mode
3	CLKMOD[1:0]; determines the clock mode: 00 = PLL disabled 10 = PLL in normal mode
4	

NOTES:
1. on = closed position = logic 0; off = open position = logic 1
2. Refer to the ***MCF5213 Reference Manual*** for additional information.

Connectors and Headers

Chapter 5

The EP8641A board has the following connectors for I/O functions and expandability:

- One connector for power (used for stand-alone only).
- One RJ-45 connector for processor RS-232 monitor port.
- Two RJ-45 connectors for the 10/100/1000 Ethernet ports.
- One 2 × 8 header for COP access.
- One 2 × 5 header for JTAG access.
- One 1 × 3 header for MMC RS-232 serial port.
- One 2 × 8 header for MMC debug port.
- One 1 × 2 header for external 12 VDC fan.
- AMC bus connector.

This chapter describes these connectors and headers. Refer to Figure 2-2 for the locations of these connectors and headers.

Power

Refer to Table 1-1 for input power requirements.

Stand-Alone

When operating in stand-alone mode the EP board is powered from +12 VDC supplied through the barrel connector (P5). An onboard regulator generates +3.3 VDC to power the MMC. The specifications for the mating connector are:

Inner diameter = 2.1 mm (0.083 inches)
Outer diameter = 5.5 mm (0.217 inches)
Outer shell is GND
Inner shell is 12 VDC

AMC

When operating in AMC mode the EP board is powered from the AMC connector of the carrier card or from the chassis backplane. Both +12 VDC to power the board and +3.3 VDC to power the MMC are required.

Processor Monitor Port

The RS-232 monitor port is connector P4. It is an RJ-45 connector. Table 5-1 shows the port pinout. The monitor port is from UART0.

Table 5-1. Monitor Port Pinout (P4)

Pin	Function	Pin	Function
1	—	5	RXD
2	—	6	TXD
3	+3.3V	7	—
4	GND	8	+3.3V

NOTE:
1. Pin numbering is from right (1) to left (8) when looking into the RJ-45 jack with the locking tab on top.

Ethernet Port

The 10/100/1000 Ethernet ports are connectors P1 and P2. The connectors are shielded RJ-45 jacks. Table 5-2 shows the RJ-45 jack pinout.

Table 5-2. Ethernet Port Pinout (P1, P2)

Pin	Function	Pin	Function
1	TXD+	5	—
2	TXD-	6	RXD-
3	RXD+	7	—
4	—	8	—

NOTE:
1. Pin numbering is from right (1) to left (8) when looking into the RJ-45 jack with the locking tab on top.

CPLD JTAG Port

The CPLD JTAG port is HD1. It is a 2 × 5 (0.1 × 0.1) header. Table 5-4 shows the JTAG header pinout.

Table 5-3. CPLD JTAG Port Pinout (HD1)

Pin	Function	Pin	Function
1	TCK	2	GND
3	TDO	4	+3.3V
5	TMS	6	—
7	—	8	—
9	TDI	10	GND

COP Port

The COP port is HD3. It is a 2 × 8 (0.1 × 0.1) header. Table 5-4 shows the COP header pinout.

Table 5-4. COP Port Pinout (HD3)

Pin	Function	Pin	Function
1	TDO	2	—
3	TDI	4	$\overline{\text{TRST}}$
5	+3.3V	6	+3.3V
7	TCK	8	$\overline{\text{CHKSTOP\_IN}}$
9	TMS	10	—
11	$\overline{\text{SRESET}}$	12	—
13	$\overline{\text{HRESET}}$	14	—
15	$\overline{\text{CHKSTOP\_OUT}}$	16	GND

MMC Serial Port

The MMC serial port is connector JP2. It is a 1 × 3 (0.1 × 0.1) header. Table 5-5 shows the pinout.

Table 5-5. MMC Serial Port Pinout (JP2)

Pin	Function
1	TXD
2	GND
3	RXD

MMC Debug Port

The MMC debug port is HD4. It is a 2 × 8 (0.1 × 0.1) header. Table 5-6 shows the utility header pinout.

Table 5-6. MMC Debug Port Pinout (HD4)

Pin	Function	Pin	Function
1	—	2	TMS
3	GND	4	$\overline{\text{TRST}}$
5	GND	6	TCK
7	$\overline{\text{RST\_IN}}$	8	TDI
9	IPMCV	10	TDO
11	GND	12	ALLPST
13	ALLPST	14	ALLPST
15	ALLPST	16	—

12 VDC Fan Header

The 12 VDC fan header is connector HD2. It is a 1 × 2 (0.1 × 0.1) header. Table 5-5 shows the pinout.

Table 5-7. 12 VDC Fan Header Pinout (HD2)

Pin	Function
1	+12V
2	GND

AMC Connector

Table 5-8 lists the pin assignments for the AMC connector (P3). The AMC connector signal assignments follow the AMC standard.

Table 5-8. AMC Connector (P3)

Pin	Signal	Pin	Signal
1	GND	170	GND
2	+12V	169	TDI
3	$\overline{PS1}$	168	TDO
4	+3.3V IPMCV	167	$\overline{TRST}$
5	GA0	166	TMS
6	—	165	TCLK
7	GND	164	GND
8	—	163	—
9	+12V	162	—
10	GND	161	GND
11	TX0+	160	—
12	TX0-	159	—
13	GND	158	GND
14	RX0+	157	—
15	RX0-	156	—
16	GND	155	GND
17	GA1	154	—
18	+12V	153	—
19	GND	152	GND
20	TX1+	151	—
21	TX1-	150	—
22	GND	149	GND
23	RX1+	148	—
24	RX1-	147	—
25	GND	146	GND
26	GA2	145	—
27	+12V	144	—
28	GND	143	GND
29	—	142	—
30	—	141	—
31	GND	140	GND

Table 5-8. AMC Connector (P3) *(continued)*

Pin	Signal	Pin	Signal
32	—	139	—
33	—	138	—
34	GND	137	GND
35	—	136	—
36	—	135	—
37	GND	134	GND
38	—	133	—
39	—	132	—
40	GND	131	GND
41	$\overline{\text{ENABLE}}$	130	—
42	+12V	129	—
43	GND	128	GND
44	TX4+	127	—
45	TX4-	126	—
46	GND	125	GND
47	RX4+	124	—
48	RX4-	123	—
49	GND	122	GND
50	TX5+	121	—
51	TX5-	120	—
52	GND	119	GND
53	RX5+	118	—
54	RX5-	117	—
55	GND	116	GND
56	SCL_L	115	—
57	+12V	114	—
58	GND	113	GND
59	TX6+	112	—
60	TX6-	111	—
61	GND	110	GND
62	RX6+	109	—
63	RX6-	108	—
64	GND	107	GND
65	TX7+	106	—
66	TX7-	105	—
67	GND	104	GND
68	RX7+	103	—
69	RX7-	102	—
70	GND	101	GND
71	SDA_L	100	—
72	+12V	99	—

Table 5-8. AMC Connector (P3) *(continued)*

Pin	Signal	Pin	Signal
73	GND	98	GND
74	—	97	—
75	—	96	—
76	GND	95	GND
77	—	94	—
78	—	93	—
79	GND	92	GND
80	CLK3+	91	—
81	CLK3-	90	—
82	GND	89	GND
83	$\overline{PS0}$	88	—
84	+12V	87	—
85	GND	86	GND

Operation

Chapter 6

This chapter describes the reset switch and board LED indications for the EP8641A board. It also provides some firmware description and communication information.

System Reset Pushbutton

The system reset pushbutton (SW1) can be used to reset the board. This pushbutton activates a power-on-reset (POR) to the board. Refer to Figure 2-2 for the location of the pushbutton.

Board LEDs

Table 6-1 describes the indications for the EP board LEDs

Table 6-1. Board LEDs

LED	Definition (On)	Color
LD500	AMC hot swap indicator	Blue
LD3	AMC LED1	Red
LD2	AMC LED2	Green
LD1	AMC LED3	Amber
LD501	+12 VDC power OK	Yellow
LD502	+5V power OK	Yellow
LD503	+3.3V power OK	Yellow
LD504	+1.1V e600 power OK	Yellow
LD505	+2.5V PHY power OK	Yellow
LD506	+1.8V DDR power OK	Yellow
LD507	“Heart Beat”	Yellow
LD508	“Morse” Version#	Green
LD509	Ethernet port 3 RXD	Green
LD510	Ethernet port 3 TXD	Green
LD511	Ethernet port 4 RXD	Green
LD512	Ethernet port 4 TXD	Green

NOTE: AMC LEDs are under MMC control.

Ethernet Port LEDs

Table 6-2 describes the indications given by the Ethernet port LEDs (P1, P2). Refer to Figure 2-2 for the location of the Ethernet port.

Table 6-2. Ethernet Port (P1, P2) LEDs

State	Indication	
	LED1 (Yellow)	LED2 (Green/Amber)
Off	No RXD/TXD activity	10 Mbps
On	RXD/TXD activity	100 Mbps (amber) 1000 Mbps (green)

User Applications

The u-boot firmware assumes the board is connected to a dumb terminal or a PC-based terminal emulator, and requires user intervention for the utilities. The dumb terminal or PC serial port should be set as follows:

- 115200 baud (default).
- 8 data bits.
- 1 stop bit.
- No parity.
- No hardware handshake.

Proper interfacing to the serial port via the correct RS-232 connections must be insured as described in ***RS-232 Connection*** in this chapter.

RS-232 Connection

A DB-9 (or DB-25) to RJ-45 connection is required for RS-232 communication. Table 5-1 provides the pinouts for the RJ-45 connector. The EP board has its serial ports wired as DTE. A null modem type of connection is required when interfacing to a DTE port.

For DTE:

DB9-3 = TXD	DB25-2 = TXD
DB9-2 = RXD	DB25-3 = RXD
DB9-8 = CTS	DB25-5 = CTS
DB9-7 = RTS	DB25-4 = RTS
DB9-5 = GND	DB25-7 = GND

Memory and Interrupts

Chapter 7

This chapter contains memory map and interrupt information for the EP8641A board.

Memory Map

Table 7-1 describes the default memory map for the EP board.

NOTE: The address map is recommended for the EP board and is as defined in u-boot. Other mappings can be utilized for any given application.

Table 7-1. Memory Map

Chip Select	Function	Address	Size	Description
$\overline{\text{LCS0}}$	FLASH	0xF8000000	128 MB	32-bit, GPCM
$\overline{\text{LCS1}}$	—	—	—	Unused
$\overline{\text{LCS2}}$	—	—	—	Unused
$\overline{\text{LCS3}}$	—	—	—	Unused
$\overline{\text{LCS4}}$	—	—	—	Unused
$\overline{\text{LCS5}}$	—	—	—	Unused
$\overline{\text{LCS6}}$	—	—	—	Unused
$\overline{\text{LCS7}}$	—	—	—	Unused
$\overline{\text{D1\_MCS0}}$	DDR SDRAM	0x00000000	256 MB	64-bit, DDRC1 controller
$\overline{\text{D1\_MCS1}}$		—	—	Unused
$\overline{\text{D1\_MCS2}}$		—	—	Unused
$\overline{\text{D1\_MCS3}}$		—	—	Unused
$\overline{\text{D2\_MCS0}}$	DDR SDRAM	0x10000000	256 MB	64-bit, DDRC2 controller
$\overline{\text{D2\_MCS1}}$		—	—	Unused
$\overline{\text{D2\_MCS2}}$		—	—	Unused
$\overline{\text{D2\_MCS3}}$		—	—	Unused
—	CCSRBAR	0xE0000000	1 MB	Memory mapped processor registers

External Interrupts

All onboard, external interrupts are active low signals. Each IRQ line has a 10 Kohm pull-up resister. All used IRQ lines should be programmed for level sense. Table 7-2 identifies the IRQ lines used by the EP board.

Table 7-2. External Interrupts

IRQ	Interrupt Source
IRQ0	Unused
IRQ1	Unused
IRQ2	Unused
IRQ3	Unused
IRQ4	Ethernet port 1
IRQ5	Ethernet port 2
IRQ6	Ethernet port 3
IRQ7	Ethernet port 4
IRQ8	STTM
IRQ9	Unused
IRQ10	Unused
IRQ11	Unused

Mechanical Dimensions

Appendix A

This appendix contains mechanical dimension drawings for the EP8641A board. The board is designed as a single-width, full-height AMC module. Figure A-1 shows the dimensions for the EP board.

NOTE: The dimensions in this document are believed correct, but if this unit is to be placed into a housing that has cut outs, an actual unit must be procured to verify all required connector cut outs. In addition, the vendor datasheets for the connectors should be referenced to determine the tolerances of the connectors.

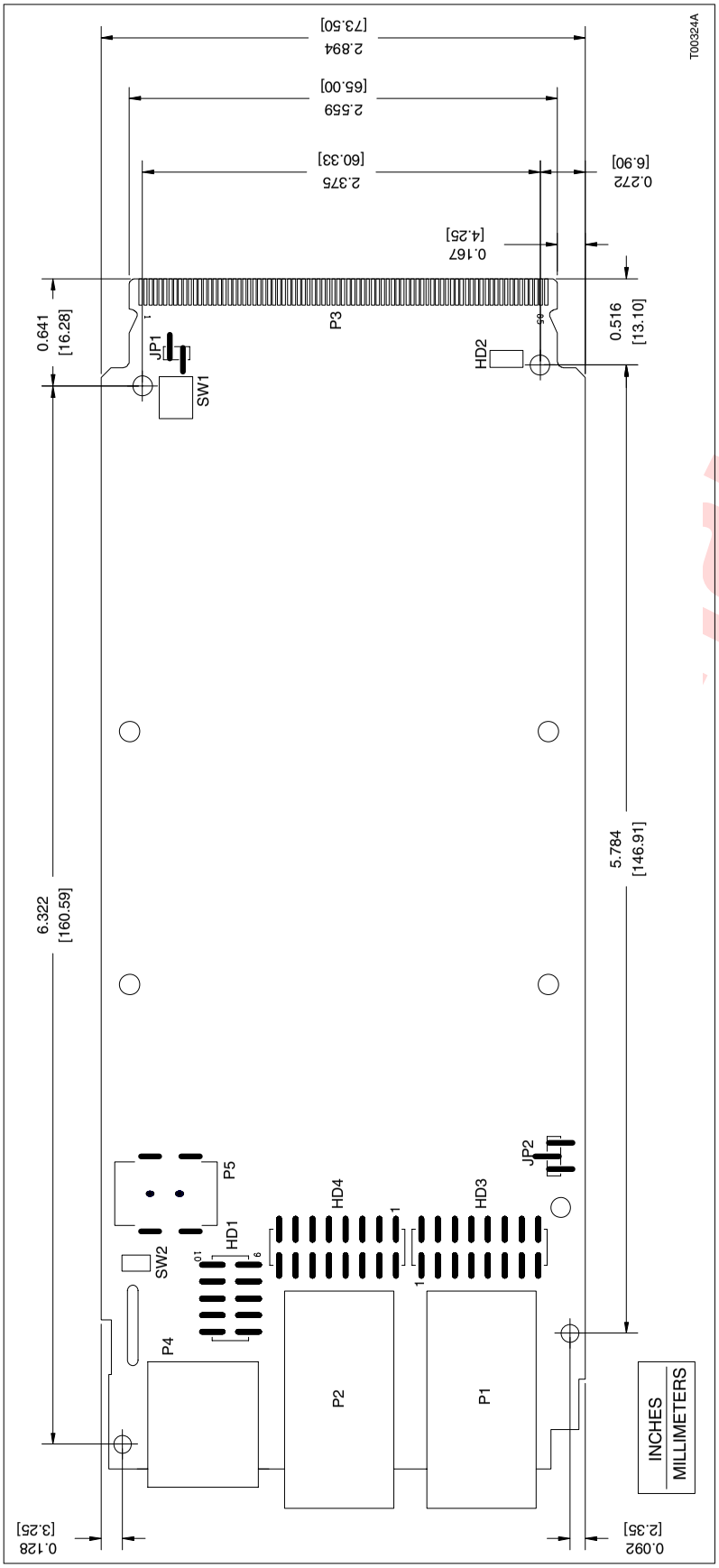

Figure A-1. Mechanical Dimensions

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