MCF5307

Product Brief

MCF5307 Integrated ColdFire® Microprocessor

Overview

Introduction

The MCF5307 integrated microprocessor combines a ColdFire® processor core with the following components:

- 8K unified cache
- Multiply-Accumulate (MAC) unit and Divide unit
- DRAM controller
- DMA controller
- Timers
- M-Bus (I^2C)[1]
- Parallel and serial interface
- System integration unit

Designed for embedded control applications, the ColdFire core delivers enhanced performance (70 MIPS) while maintaining low system costs.

Performance boosts are supplied to the clock-doubled core through the on-chip, 8 Kbyte unified cache and 4K SRAM, which provide pipelined, single-cycle access to critical code and data.

The integrated Multiply-Accumulate (MAC) module enhances the device's functionality through support of high-speed, complex arithmetic operations. The MAC supports instruction issue rates of 1 multiply-accumulate per cycle for 16x16 operations, and also performs 32x32 operations, all producing a 32-bit result.

The MCF5307 processor greatly reduces the time required for system design and implementation by packaging common system functions on chip and providing glueless interfaces to 8-, 16-, and 32-bit DRAM, EDO DRAM, SDRAM, SRAM, ROM, FLASH, and I/O devices.

---

[1] I^2C is a proprietary Philips bus.

SEMICONDUCTOR PRODUCT INFORMATION

Overview, Continued

ColdFire Architecture Provides New Price/ Performance Levels

The revolutionary ColdFire microprocessor architecture gives cost-sensitive, high-volume markets new levels of price and performance. Based on the concept of variable-length RISC technology, ColdFire combines the architectural simplicity of conventional 32-bit RISC with a memory-saving, variable-length instruction set. In defining the ColdFire architecture for embedded processing applications, Motorola incorporated RISC architecture for peak performance and a simplified version of the variable-length instruction set found in the M68000 Family for code density.

Clock-Doubled Version 3 Core Boosts Performance

The MCF5307 is the first of the ColdFire Family to contain the Version 3, clock-doubled ColdFire microprocessor core. Increasing the internal speed of the core allows higher performance while providing the system designer with an easy-to-use external system interface.

ColdFire VL RISC Offers Many Advantages

By using a variable-length instruction set architecture, embedded system designers using ColdFire RISC processors will enjoy significant advantages over conventional fixed-length RISC architectures. The denser binary code for ColdFire processors consumes less valuable memory than any fixed-length instruction set RISC processor available. This improved code density means more efficient system memory use for a given application, and requires slower, less costly memory to help achieve a target performance level.

The MCF5307 Integrates a Rich Set of Modules with the ColdFire V3 Core

The integrated peripheral functions provide high performance and flexibility. The DRAM controller can interface with up to 256 Mbytes of DRAM and supports bursting, page-mode, EDO and synchronous DRAMs.

Serial communication channels are provided by two programmable full-duplex UARTs and an M-Bus (I^2C interface-compatible) module. Four channels of DMA allow for fast data transfer using a programmable burst mode independent of processor execution. The two 16-bit general-purpose multimode timers provide separate input and output signals. For system protection, the processor includes a programmable 16-bit software watchdog timer. In addition, common system functions such as chip-selects, interrupt control, bus arbitration, and an IEEE 1149.1 JTAG module are included.

A sophisticated debug interface supports background-debug mode and real-time trace, with on-chip breakpoint registers accessible from an emulator or the processor itself. This interface is present in all ColdFire-based processors and allows common emulator support across the entire ColdFire Family.

MCF5307 Product Brief MOTOROLA

MCF5307 Features

ColdFire Processor Core
- Variable-length RISC, clock-doubled Version 3 microprocessor core
- Independent 4-stage instruction and 2-stage operand pipelines
- 8-instruction FIFO buffer to provide decoupling between the pipelines
- Branch acceleration unit for increased performance
- 32-bit internal address bus with up to 4 Gbytes of linear address space
- 32-bit data bus
- 16 user-accessible, 32-bit-wide, general-purpose registers
- Supervisor / User modes for system protection
- Vector base register to relocate exception-vector table
- Optimized for high-level language constructs
- Hardware Integer Divide Unit

Multiply and Accumulate Unit
- Provides high-speed, complex arithmetic processing for DSP applications
- 1 clock issue rate with 3-stage execute pipeline
- Supports 16x16 and 32x32 multiplies, all with 32-bit accumulate

8 Kbyte Unified Cache
- Four-way set associative organization with writethrough and copyback modes
- Operates at microprocessor core speed
- Provides single-cycle access to critical code and data

4 Kbyte SRAM
- Programmable location within 4 Gbyte linear address space
- Provides pipeline single cycle access to critical code and data
- Information stored in SRAM not affected by RESET instruction

DMA Controller
- Four fully programmable channels
- Supports dual-address and single-address transfers with 32-bit data capability
- Two address pointers per channel that can increment or remain constant
- 16-bit transfer counter per channel
- Operand packing and unpacking supported
- Auto-alignment transfers supported for efficient block movement
- Supports bursting and cycle steal
- Provides two clock-cycle internal access

DRAM Controller
- Supports up to 512 Mbytes of DRAM
- Programmable refresh timer provides CAS-before-RAS refresh
- Support for two separate memory banks
- Support for EDO DRAMs and synchronous DRAMs
- Support for external masters

MCF5307 Features, Continued

---

2 UARTs

- Full duplex operation
- Flexible baud-rate generator
- Modem control signals available ($\overline{\text{CTS}}$, $\overline{\text{RTS}}$)
- Processor-interrupt capability

Dual 16-Bit General-Purpose Multimode Timers

- 8-bit prescaler
- Timer input and output pins
- Processor-interrupt capability
- 22 ns resolution at 45 MHz

Motorola Bus (M-Bus) Module

- Interchip bus interface for EEPROMs, LCD controllers, A/D converters, keypads
- Fully compatible with industry-standard I^2C Bus
- Master or slave modes support multiple masters
- Automatic interrupt generation with programmable level

System Interface

- Glueless bus interface with chip selects and DRAM controller support for interface to 8-, 16-, and 32-bit DRAM, SRAM, ROM, FLASH, and I/O devices
- 8 chip-select signals; 2 that are fully programmable with base address registers, 6 at a fixed offset off the chip-select base address register
- Programmable wait states and port sizes
- User-defined bus speed @ 1/2, 1/3, or 1/4 of processor clock
- Programmable interrupt controller
- Low interrupt latency
- 4 external interrupt request inputs
- Programmable autovector generator
- 16-Bit general-purpose I/O interface
- IEEE 1149.1 test (JTAG) module

System Debug Support

- Real-time trace for determining dynamic execution path
- Background debug mode (BDM) for debug features while halted
- Real-time debug support, including three user-visible hardware breakpoint registers

---

MCF5307 Features, Continued

On-Chip PLL
- Accepts input frequencies ranging from 16.67 to 45 MHz
- Generates 2X core clock and a bus clock of either 1/2, 1/3, or 1/4 the core clock based on user configuration at reset
- Supports low-power mode

Product Offerings
- 75 MIPS at 45 MHz (90 MHz clock-doubled internally)
- Offered at 90 MHz core clock with external bus capability of 45, 30, and 22.5 MHz (operating temperature: 0° to +70° C)
- Offered at 66.7 MHz core clock with external bus capability of 33.3, 22.2, and 16.7 MHz (operating temperature: 0° to +70° C and -40° to +85° C)
- Fully static 3.3-volt operation with 5V tolerant I/O pads
- 208 QFP package

MCF5307 Block Diagram

Overview of MCF5307 Components

Figure 1 is a block diagram of the MCF5307 processor. The paragraphs that follow provide an overview of the integrated processor components.

Figure 1: MCF5307 Block Diagram
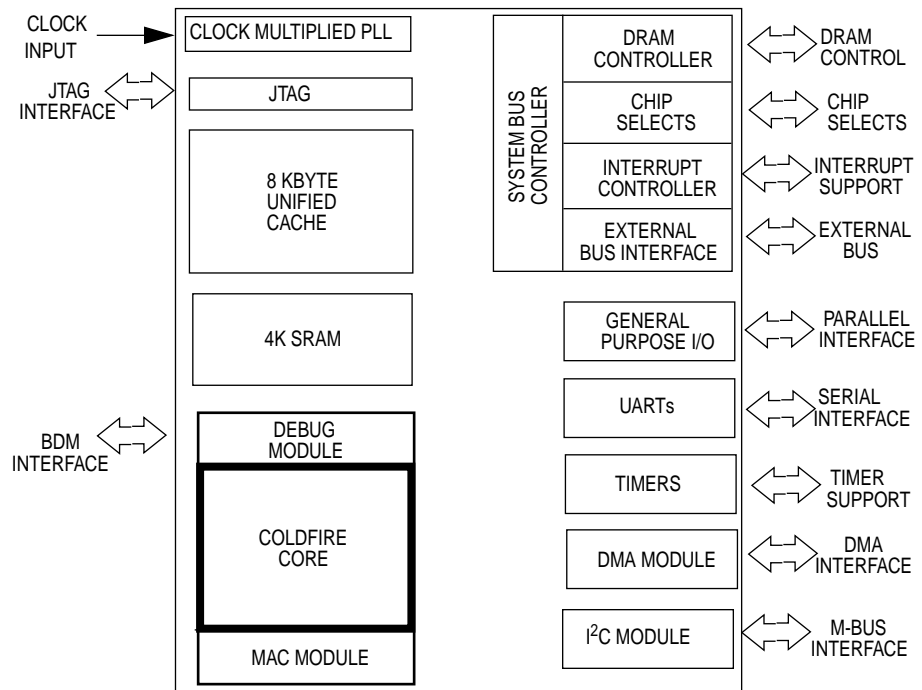
ColdFire Processor Core

Overview

The ColdFire processor Version 3 core consists of two independent, decoupled pipelines to maximize performance while minimizing core size: the instruction fetch pipeline (IFP) and the operand execution pipeline (OEP).

Instruction Fetch Pipeline

The four-stage instruction fetch pipeline is for prefetching instructions. The IFP contains a branch acceleration unit that analyzes the prefetched instruction stream and takes a predicted branch to allow this pipeline to begin fetching the target path before the instruction is executed. This technique can improve the execution time of these change-of-flow instructions considerably. In addition, illegal instructions are decoded and an illegal instruction exception will be taken.

Operand Execution Pipeline

The prefetched instruction stream is gated into the two-stage operand execution pipeline, which decodes the instruction, fetches the required operands and executes the required function. Because the IFP and OEP are decoupled by an instruction buffer that serves as a FIFO queue, the IFP can prefetch instructions in advance of their actual use by the OEP, thereby minimizing time stalled waiting for instructions. The OEP is implemented in a two-stage pipeline featuring a traditional RISC datapath with a two-read/one-write port register file connected to these four execution units:

1. Arithmetic/logic unit
2. Barrel shifter
3. Integer divide
4. MAC

MAC Module

The MAC unit provides high-performance DSP capabilities for the MCF5307. Integrated as an execution unit in the processor's operand execution pipeline, the MAC unit implements a 3-stage arithmetic pipeline with a sustained instruction issue rate of 1 multiply-accumulate per cycle for 16 x 16 operations (while also supporting 32 x 32 operations). The MAC opcodes provide a full-featured set of extensions to the standard ColdFire instruction set for signed and unsigned operands. In addition to executing the MAC-specific instructions, this unit also performs all integer multiply opcodes, providing higher performance for this class of operations.

8 Kbyte Unified Cache

The cache improves system performance by providing pipelined, single-cycle access to the processor core on references that hit in this memory. This decouples processor performance from system memory performance and increases bus availability for alternate bus masters, whether internal (the 4-channel DMA) or external.

The nonblocking design of the MCF5307 cache includes 16-byte line-fill buffers that allows processor-initiated requests that are mapped into this memory to be serviced while cache line-fill transfers are in progress. You can configure various memory address regions to operate as copyback or write-through cacheable regions, or as noncacheable spaces.

In addition to the 16 bytes of data, each cache line contains an address tag, and control bits. Support for a bursting interface quickly performs line-sized transfers in response to cache misses. A 4-entry, 32-bit-wide store buffer can decouple processor writes from the slower system bus interface to improve performance. The cache design, coupled with the processor microarchitecture, allows the MCF5307 to achieve 70 MIPS performance using a 90/45 MHz operating frequency.

Internal 4Kbyte SRAM

The 4 Kbyte on-chip SRAM is connected directly to the ColdFire core and provides pipelined single-cycle access to the address space mapped into this memory. Typically, this memory serves as the system stack. Additionally, you can map heavily referenced code segments or data variables into the SRAM to maximize performance. Users define the location of this memory within the 4 Gbyte linear address space of the processor.

DRAM Controller

The MCF5307 DRAM controller provides a glueless interface for as many as 2 banks of DRAM, each of which can be as large as 128 Kbytes up to 256 Mbytes. The controller supports 8-, 16-, or 32-bit memory widths. A unique addressing scheme allows for increases in system memory size without rerouting address lines and rewiring boards. The controller operates in normal mode or in page mode, and supports extended-data-out (EDO) DRAMs and synchronous DRAMs. At a 45 MHz external bus speed, the DRAM controller supports DRAMs with access times as fast as 22 ns.

DMA Controller

MCF5307 provides four fully programmable DMA channels for quick data transfer. Single- and dual-address mode is provided with the ability to program bursting and cycle steal. Data transfers are 32 bits in length with packing and unpacking supported along with an auto-alignment option for efficient block transfers.

UART Modules

Each UART on the MCF5307 contains an on-chip baud-rate generator, which provides both standard and nonstandard baud rates. Data formats can be 5, 6, 7, or 8 bits with even, odd, or no parity, and up to 2 stop bits in 1/16 increments. Four-byte receive buffers and two-byte transmit buffers minimize CPU service calls. The UART modules also provide several error-detection and maskable-interrupt capabilities. Modem support includes request-to-send ($\overline{\text{RTS}}$) and clear-to-send ($\overline{\text{CTS}}$) lines.

The system clock provides the clocking function via a programmable prescaler. Full duplex, auto-echo loopback, local loopback, and remote loopback modes let you test UART connections. The programmable UARTs can interrupt the CPU on various normal or error-condition events.

Timer Module

The timer module includes two general-purpose timers, each of which contains a free-running 16-bit timer for use in any of three modes. One mode captures the timer value with an external event. Another mode triggers an external signal or interrupts the CPU when the timer reaches a set value, while a third mode counts external events.

The timer unit has an 8-bit prescaler that allows programming of the clock input frequency, which is derived from the system clock or an external clock input pin (TIN). The programmable timer-output pin generates either an active-low pulse or toggles the output.

Motorola Bus (M-Bus) Module

The M-Bus interface is a two-wire, bidirectional serial bus that exchanges data between devices and is compliant with the I^2C Bus standard. The M-Bus minimizes the interconnection between devices in the end system and is best suited for applications that need occasional bursts of rapid communication over short distances among several devices.

System Interface

Overview

The MCF5307 processor provides a glueless interface to 8-, 16-, and 32-bit port size FLASH, SRAM, ROM, and peripheral devices with independent programmable control of the assertion and negation of chip-selects and write-enables. The MCF5307 also supports bursting ROMs. The MCF5307 has a clock-multiplied core that operates at 2x, 3x, or 4x the external bus frequency. You select the multiplier for the bus frequency at reset of the microprocessor.

External Bus Interface

The bus interface controller transfers information between the ColdFire core or DMA and memory, peripherals, or other devices on the external bus. The external bus interface provides 32 bits of address bus space, a 32-bit data bus, and all associated control signals. This interface implements an extended synchronous protocol that supports bursting operations.

Simple two-wire request/acknowledge bus arbitration between the MCF5307 processor and another bus master, such as an external DMA device, is glueless with arbitration logic internal to the MCF5307 processor. Multiple-master arbitration is also available with some external arbitration logic.

Chip-Selects

Eight chip-select outputs (2 that are programmable with base address registers, 6 at fixed offsets from the chip-select bus address register) provide signals that enable external memory and peripheral circuits with automatic wait-state insertion. These signals interface to 8-, 16-, or 32-bit ports. The base address, access permissions, and internal bus transfer terminations are programmable with configuration registers.

16-Bit Parallel Port Interface

A 16-bit general-purpose programmable parallel port serves as either an input or an output on a bit-by-bit basis.

System Interface, Continued

Interrupt Controller   The interrupt controller provides user-programmable control of 10 internal peripheral interrupts and implements 4 external fixed interrupt-request pins. You can program each internal interrupt to any one of 7 interrupt levels and 4 priority levels within each of these levels and can program the external interrupt request pins to level 1, 3, 5, and 7 or levels 2, 4, 6, and 7. Autovector capability is available for internal and external interrupts.

JTAG   To help with system diagnostics and manufacturing testing, the MCF5307 processor includes dedicated user-accessible test logic that complies with the IEEE 1149.1a standard for boundary-scan testability, often referred to as Joint Test Action Group, or JTAG. For more information, refer to the IEEE 1149.1a standard.

System Debug Interface

The ColdFire processor core debug interface supports real-time trace and debug, along with background debug mode (BDM). The BDM interface is implemented using a serial communication channel with an emulator. The BDM is compatible with the BDM interface provided on Motorola's 683XX Family of parts.

To support real-time trace, four output bits (PST) provide status information on processor activity on a cycle-by-cycle basis. Additionally, a 4-bit output data bus (DDATA) can be configured to display operand data and certain change-of-flow target addresses for determining the dynamic execution path through the application.

Finally, the Debug module provides a number of on-chip breakpoint registers that can be configured by an emulator, or by the processor itself to generate special debug interrupts or processor halts. The breakpoint resources include two 32-bit address registers, a 32-bit PC and 32-bit PC mask registers, and a 32-bit data register and 32-bit data mask register. These breakpoint registers can be configured in single- or double-level triggers where you define the trigger response.

PLL Module

Overview
The MCF5307 PLL module has three modes of operation:

1. Normal mode
2. Reduced power mode
3. Reset mode

Normal Mode Input Frequency
In normal mode, an input frequency to the MCF5307 can range from 16.67 MHz to 45 MHz. This input frequency is programmed at reset and clock-doubled to provide the processor clock and then is divided down to provide the bus clock output. The bus clock is programmed to 1/2, 1/3, or 1/4 of the core clock.

Reduced Power Mode
In reduced power mode, the PLL core clock is shut off by a combination of executing the STOP instruction and programming a control bit in the System Configuration register. This low-power mode allows the core to be turned off while retaining the core register contents.

Reset Mode
When the MCF5307 $\overline{\text{RESET}}$ pin is asserted, the PLL enters reset mode. At reset, the PLL asserts $\overline{\text{RESETO}}$ to the rest of the processor and as an external pin from the MCF5307. The system input frequency range, MCF5307 bus clock frequency (along with other MCF5307 configuration information) are all sampled during reset mode.

Programming Model, Instruction Set, and Addressing Mode

Overview

The ColdFire programming model is separated into two privilege modes: supervisor and user. The S-bit in the status register (SR) indicates the current privilege mode. The processor identifies a logical address by accessing either the supervisor or user address space, which differentiates between supervisor and user modes.

Supervisor Mode

Supervisor mode protects system resources from uncontrolled access by users. In supervisor mode, you can access all registers and execute all ColdFire instructions. Operating system functions (including I/O control) are performed while in supervisor mode. During exception processing, the processor enters supervisor mode regardless of the operating mode at the time of the exception.

Typically, system programmers use the supervisor programming model to implement operating system functions and provide I/O control. The supervisor programming model provides access to the same registers as the user model, plus seven additional registers. These added resources include the upper byte of the Status Register (SR), the Vector Base Register (VBR), plus five registers defining the configuration and attributes of the address space connected to the MCF5307.

User Mode

While in user mode, access to only a subset of the supervisor registers is allowed, and execution of privileged instructions is not permitted. Typically, most application processing occurs while in user mode. Entry into user mode is usually accomplished by executing a "return from exception" (RTE) or MOVE, SR instruction.

User Programming Model

The registers depicted in the programming model (see Figure 2) provide high-speed storage for data and addresses for the ColdFire processor core. The user programming model consists of sixteen general-purpose 32-bit registers {D0-D7, A0-A7} plus two additional registers: the program counter (PC) and the condition code register (CCR).

The program counter is a 32-bit register containing the address of the instruction currently being executed by the MCF5307 processor. The 8-bit CCR contains indicator flags that reflect the result of a previous operation and are used for conditional instruction execution.

MCF5307 Product Brief MOTOROLA

Programming Model, Instruction Set, and Addressing Mode,
Continued

Status Register (SR)   The upper byte of the Status Register provides interrupt information in addition to a variety of mode indicators signaling the operating state of the ColdFire processor.

Vector Base Register (VBR)   The VBR defines the upper 12 bits of the base address of the exception vector table used during exception processing. The low-order 20 bits are forced to zero, placing the vector table on a 0-modulo-1Mbyte address boundaries, which is set by the upper 12 bits of the address.

Cache Control Register (CCR)   The Cache Control Register (CACR) defines the configuration of the unified cache and provides a set of default address attributes.
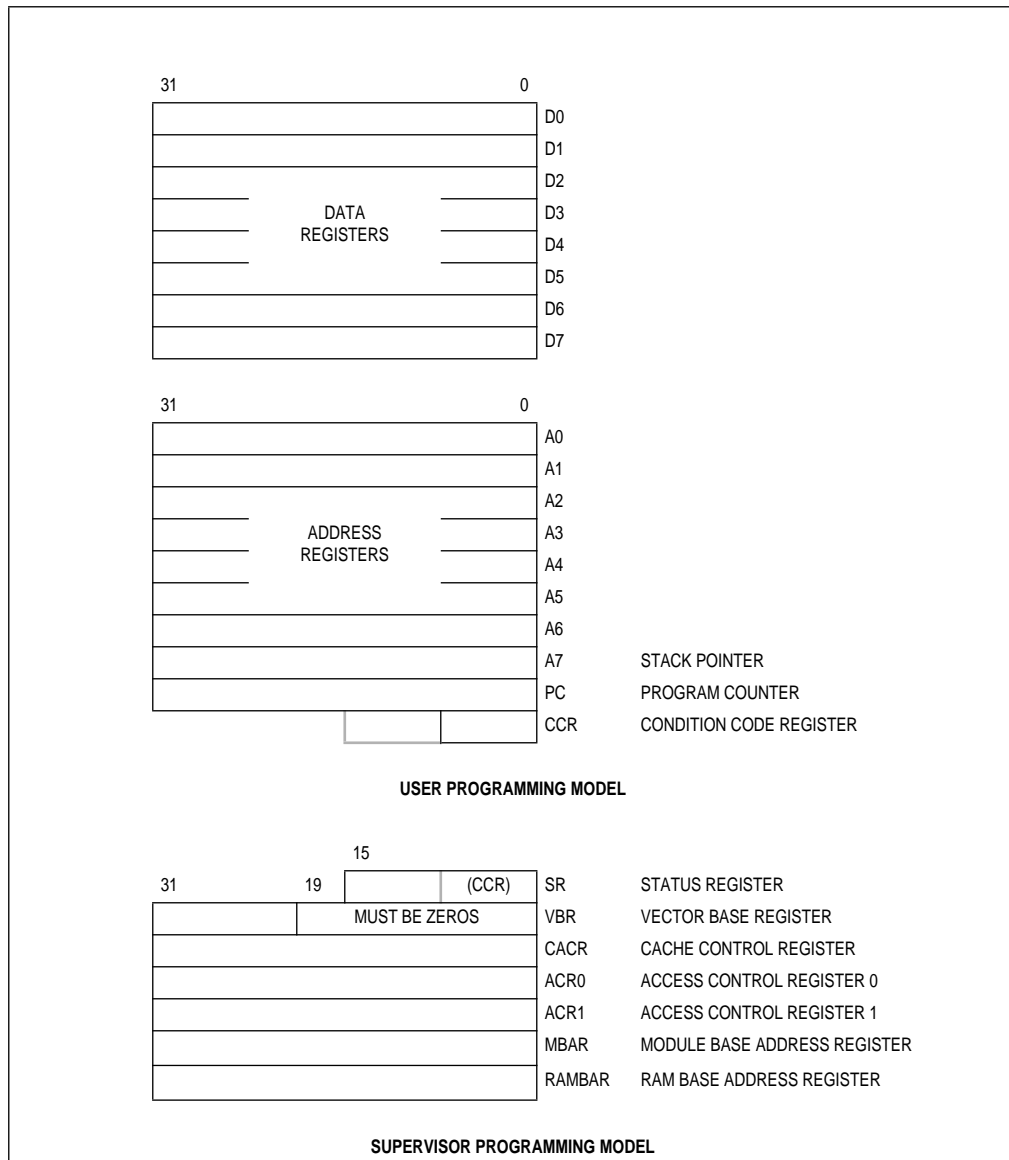

Access Control Registers (ACRs)   There are two Access Control Registers (ACR0, ACR1), which each define a set of address attributes for a specific memory space. For example, a memory space can be defined as copyback, writethrough, or noncacheable using the ACR registers.

RAM Base Address Register (RAMBAR)   The RAM Base Address Register (RAMBAR) provides the logical base address for the processor's 4 Kbyte SRAM module as well as definition of those access types that are allowed to access that SRAM.

Module Base Address Register (MBAR)   The Module Base Address Register (MBAR) defines the logical base address for the memory-mapped space containing the control registers for the on-chip peripherals.

Programming Model, Instruction Set, and Addressing Mode,
Continued

**Figure 2. ColdFire
Programming Model**

```
         31                          0
        ┌──────────────────────────┐ D0
        ├──────────────────────────┤ D1
        ├──────────────────────────┤ D2
        │         DATA             │ D3
        │       REGISTERS          │ D4
        │                          │ D5
        ├──────────────────────────┤ D6
        └──────────────────────────┘ D7

         31                          0
        ┌──────────────────────────┐ A0
        ├──────────────────────────┤ A1
        ├──────────────────────────┤ A2
        │        ADDRESS           │ A3
        │       REGISTERS          │ A4
        │                          │ A5
        ├──────────────────────────┤ A6
        ├──────────────────────────┤ A7      STACK POINTER
        ├──────────────────────────┤ PC      PROGRAM COUNTER
        └──────────────────────────┘ CCR     CONDITION CODE REGISTER
```

USER PROGRAMMING MODEL

```
                      15
         31      19   ┌────────┐ SR       STATUS REGISTER
        ┌────────┬────┴────────┤ VBR      VECTOR BASE REGISTER
        │     MUST BE ZEROS    │ CACR     CACHE CONTROL REGISTER
        ├─────────────────────┤ ACR0     ACCESS CONTROL REGISTER 0
        ├─────────────────────┤ ACR1     ACCESS CONTROL REGISTER 1
        ├─────────────────────┤ MBAR     MODULE BASE ADDRESS REGISTER
        └─────────────────────┘ RAMBAR   RAM BASE ADDRESS REGISTER
```

SUPERVISOR PROGRAMMING MODEL

Programming Model, Instruction Set, and Addressing Mode,
Continued

Data Format Summary

Operands can be signed or unsigned and are contained in registers, memory, or the instructions themselves. The operand specifiers and size for each operation are either explicitly encoded in the instruction or implicitly defined by the instruction's definition. Table 1 summarizes the MCF5307 data formats.

Table 1: MCF5307 Data Formats

OPERAND DATA FORMAT	SIZE
Bit	1 Bit
Byte	8 Bits
Word	16 Bits
Longword	32 Bits

Notational Conventions

The following tables list the commonly used ColdFire notational conventions.

REGISTER SPECIFICATION	
An	Any Address Register n (example: A3 is address register 3)
Ay, Ax	Source and destination address registers, respectively.
Dn	Any Data Register n (example: D5 is data register 5)
Dy, Dx	Source and destination data registers, respectively.
Rc	Control Register (example: VBR, CACR)
Rn	Any Address or Data Register n
Ry, Rx	Any source and destination registers, respectively.
Rw	Destination Register w (used on certain MAC instructions only)
Xi	Index Register i (Can be an address or data register: A, Di)

REGISTER NAMES	
CCR	Condition Code Register (lower byte of status register)
MACSR	MAC Status Register
PC	Program Counter
Racc	MAC Accumulator Register
Rmask	MAC Mask Register
SR	Status Register
DATA SIZE AND TYPE	
<size>	Operand Data Size: Byte (B), Word (W), Longword (L).
B, W, L	Specifies a signed integer data type of 8-bit byte, 16-bit word, or 32-bit longword.

SUBFIELDS AND QUALIFIERS	
#<data>	Immediate data following the 16-bit instruction word of the instruction
#<list>	List of registers for MOVEM instruction (example: D3-D0 = D3, D2, D1, D0)
#<vector>	Identifies a 4-bit vector number for TRAP instructions
()	Identifies an indirect operand address referencing memory
(xxx)	Identifies an absolute address referencing memory
<ea>	Effective address
<ea>y	Source effective address
<ea>x	Destination effective address
<label>	Assembly language program label
d_n	Signed displacement Value, n Bits Wide (example: d_{16} is a 16-bit displacement).
+	Postincrement indicator
-	Predecrement indicator
SF	Scale factor (x1, x2, or x4 for indexed addressing modes, <<1 or >>1 for MAC ops)

Addressing Capability Summary

The MCF5307 processor supports seven addressing modes (refer to Table 2a). The register indirect addressing modes support postincrement, predecrement, offset, and indexing, which are particularly useful for handling data structures common to sophisticated embedded applications and high-level languages. The program counter indirect mode also has indexing and offset capabilities. This addressing mode is typically required to support position-independent software. As part of the indexed addressing mode, ColdFire supports an optional scale factor which can be applied to the index register to easily access byte, word or longword entries within an array (x1, x2, x4).

Addressing Capability Summary, Continued

Effective Addressing Modes

An instruction's effective addressing mode can specify the operand in one of three ways:

1. It can specify the data value directly as an immediate operand
2. It can specify the register containing the operand
3. It can specify the addressing calculation needed to reference the memory location containing the operand

Each addressing mode has a unique assembler syntax. In addition to the generalized format where the addressing mode is specified directly in the instruction, there are some opcodes where the effective address is implicitly defined by the operation itself. Table 2a summarizes the effective addressing modes of ColdFire processors; Table 2b shows specific effective addressing modes for the MOVE instruction; and Table 2c presents addressing variants used by certain instructions.

Table 2a: ColdFire Effective Addressing Modes

ADDRESSING MODES	SYNTAX
Register Direct Data Address	 Dn An
Register Indirect Address Address with Postincrement Address with Predecrement Address with Displacement	 (An) (An)+ –(An) (d16,An)
Address Register Indirect with Scaled Index 8-Bit Displacement	(d$_8$,An,Xi*SF)
Program Counter Indirect with Displacement	(d$_{16}$,PC)
Program Counter Indirect with Scaled Index 8-Bit Displacement	(d$_8$,PC,Xi*SF)
Absolute Data Addressing Short Long	 (xxx).W (xxx).L
Immediate	#<data>

Table 2b: Specific Effective Addressing Modes for MOVE Instructions

SOURCE <EA>	DESTINATION <EA>
Dy	All
Ay	All
(Ay)	All
(Ay)+	All

Table 2b: Specific Effective Addressing Modes for MOVE Instructions (Continued)

SOURCE <EA>	DESTINATION <EA>
-(Ay)	All
(d$_{16}$,Ay) (d$_{16}$,PC)	Dx Ax (Ax) (Ax)+ -(Ax) (d$_{16}$,Ax)
(d$_8$,Ay,Xi*SF) (d$_8$,PC,Xi*SF)	Dx Ax (Ax) (Ax)+ -(Ax)
(xxx).W (xxx).L	Dx Ax (Ax) (Ax)+ -(Ax)
#<data>	Dx Ax (Ax) (Ax)+ -(Ax)

Table 2c: Addressing Variants Used By Certain Instructions

ADDRESSING VARIANT	ALLOWABLE MODES
<ea-1>	Dn (An) (An)+ -(An) (d$_{16}$,An)
<ea-2>	(An) (d$_{16}$,An)
<ea-3>	(An) (d$_{16}$,An) (d$_8$,An,Xi*SF) (xxx).W (xxx).L (d$_{16}$,PC) (d$_8$,PC,Xi*SF)

Instruction Set

Overview

The ColdFire instruction set supports high-level languages and is optimized for those instructions most commonly generated by compilers in embedded applications. Tables 3a and 3b provide an alphabetized listing of the ColdFire instruction set opcode, supported operation sizes, and assembler syntax. For two-operand instructions, the first operand in the syntax is generally the source operand, and the second operand is the destination.

Table 3a: Supervisor Mode Instruction Summary

OPCODE	SUPPORTED OPERAND SIZES	ADDRESSING MODES
CPUSHL	Unsized	(An)
HALT*	Unsized	
MOVE from SR	.W	SR,Dx
MOVE to SR	.W	Dy,SR #<data>,SR
MOVEC	.L	Ry,Rc
RTE	Unsized	
STOP	.W	#<data>
WDEBUG	.L	<ea-2>

*The HALT instruction can be configured to allow user mode execution by setting the UHE bit in the debug module's Configuration/Status Register (CSR).

Table 3b: User Mode Instruction Summary

OPCODE	SUPPORTED OPERAND SIZES	ADDRESSING MODES
ADD	.L	<ea>y,Dx Dy,<ea>x
ADDA	.L	<ea>y,Ax
ADDI	.L	#<data>,Dx
ADDQ	.L	#<data>,<ea>x
ADDX	.L	Dy,Dx
AND	.L	<ea>y,Dx Dy,<ea>x
ANDI	.L	#<data>,Dx
ASL	.L	Dy,Dx #<data>,Dx
ASR	.L	Dy,Dx #<data>,Dx
Bcc	.B,.W	<label>
BCHG	.B,.L	Dy,<ea>x #<data>,<ea-1>x
BCLR	.B,.L	Dy,<ea>x #<data>,<ea-1>x
BRA	.B,.W	<label>

**Table 3b: User Mode
Instruction Summary**
(Continued)

OPCODE	SUPPORTED OPERAND SIZES	ADDRESSING MODES
BSET	.B,.L	Dy,<ea>x #<data>,<ea-1>x
BSR	.B,.W	
BTST	.B,.L	Dy,<ea>x #<data>,<ea-1>x
CLR	.B,.W,.L	<ea>x
CMP	.L	<ea>y,Dx
CMPA	.L	<ea>y,Ax
CMPI	.L	#<data>,Dx
DIVS	.W	<ea>y, Dx
DIVS	.L	<ea-1>y, Dx
DIVU	.W	<ea>y, Dx
DIVU	.L	<ea-1>y, Dx
EOR	.L	Dy,<ea>x
EORI	.L	#<data>,Dx
EXT	.W,.L	Dx
EXTB	.L	Dx
JMP	Unsized	<ea-3>y
JSR	Unsized	<ea-3>y
LEA	.L	<ea>y,Ax
LINK	.W	Ax,#<d16>
LSL	.L	Dy,Dx #<data>,Dx
LSR	.L	Dy,Dx #<data>,Dx
MAC	.W,.L	Ry, RxSF
MAC	.W,.L	Rx, RySF,<ea-1>y, Rw
MOVE	.B,.W,.L	see MOVE Table
MOV	.L	Ry,MACSR #<data>,MACSR Ry,Racc #<data>,Racc Ry,Rmask #,data>,Rmask MACSR,CCR MACSR,Rx Racc,Rx Rmask,Rx
MOVE from CCR	.W	CCR,Dx
MOVE to CCR	.W	Dy,CCR #<data>,CCR
MOVEM	.L	<ea-2>y,#<list> #<list>,<ea-2>x
MOVEQ	.L	#<data>,Dx
MSAC	.W,.L	Ry, RxSF
MSAC	.W,.L	Rx, RxSF,<ea-1>y, Rw
MULS	.W	<ea>y,Dx
MULS	.L	<ea-1>y,Dx
MULU	.W	<ea>,Dx
MULU	.L	<ea-1>y,Dx

Table 3b: User Mode Instruction Summary (Continued)

OPCODE	SUPPORTED OPERAND SIZES	ADDRESSING MODES
NEG	.L	Dx
NEGX	.L	Dx
NOP	Unsized	
NOT	.L	Dx
OR	.L	<ea>y,Dx Dy,<ea>x
ORI	.L	#<data>,Dx
PEA	.L	<ea-3>y
PULSE	Unsized	
REMS	.L	<ea-1>, Dx
REMU	.L	<ea-1>, Dx
RTS	Unsized	
Scc	.B	Dx
SUB	.L	<ea>y,Dx Dy,<ea>x
SUBA	.L	<ea>y,Ax
SUBI	.L	#<data>,Dx
SUBQ	.L	#<data>,<ea>x
SUBX	.L	Dy,Dx
SWAP	.W	Dx
TRAP	Unsized	#<vector>
TRAPF	Unsized	
TRAPF	.W,.L	#<data>
TST	.B,.W,.L	<ea>y
UNLK	Unsized	Ax
WDDATA	.B,.W,.L	<ea>y

General Device Information

Table 4: MCF5307 Package/Frequency Availability

PACKAGE	OPERATING TEMP.	FREQUENCY
208 QFP	0 to 70 C, -40 to +85 C	66.7 MHz core w/16.7, 22.2, & 33.3 MHz bus capability
208 QFP	0 to 70 C	90 MHz core w/ 22.5, 30, & 45MHz bus capability

Documentation

Additional and detailed information is available from Motorola literature distribution centers. To find out more about Motorola's ColdFire products and development tool offerings, please visit our website at http://www.mot.com/coldfire.

DOCUMENT NUMBER	DOCUMENT TITLE
MCF5307 Specification	*MCF5307 Spec. Rev. 0.0*(Available through secure website. Contact your local salesperson for access)
MCF5307UM/AD	*MCF5307 User's Manual* (Est. Stocking 1Q98)
5200PRM/AD Rev1	*MCF5200 ColdFire Family Programmer's Reference Manual*

MCF5307 Product Brief

Literature Distribution Centers:
USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912, Arizona 85036.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong.