



Hexagon Application Kit

For XMC4000 Family

CPU_45A-V2

CPU Board XMC4500 General Purpose

Board User's Manual

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Microcontroller

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Revision History

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Introduction

This document describes the features and hardware details of the CPU Board XMC4500 General Purpose (CPU_45A-V2) designed to work with Infineon's XMC4500 Microcontroller. This board is part of Infineon's Hexagon Application Kits.

1 Overview

The CPU_45A-V2 board houses the XMC4500 Microcontroller and three satellite connectors (HMI, COM, ACT) for application expansion. The board along with satellite cards (e.g. HMI_OLED-V1, COM_ETH-V1, AUT_ISO-V1 boards) demonstrates the capabilities of XMC4500. The main use case for this board is to demonstrate the generic features of XMC4500 device including toolchain. The focus is safe operation under evaluation conditions. The board is not cost optimized and cannot be seen as reference design.

1.1 Key Features

The CPU_45A-V2 board is equipped with following features

- XMC4500 (ARM® Cortex™-M4) Microcontroller, LQFP-144
- Connection to XMC4500 satellite cards via satellite connectors COM, HMI and ACT
- USB OTG Host/Device support via micro USB connector
- Debug options
 - Cortex Debug connector 10-pin (0.05")
 - Cortex Debug+ETM connector 20-pin (0.05")
 - DriveMonitor2 Stick connector
- Reset push button
- 32MBit quad SPI flash memory
- Boot from Embedded Flash, UART or CAN
- Ready for power consumption analysis
- 5 LED's
 - 3 Power indicating LED's
 - 1 GPIO (P3.9) LED
 - 1 RESET LED
- Potentiometer, connected to analog input P14.1
- Power supply
 - Via micro USB connector in USB device mode
 - Via satellite connector pins (COM/ACT satellites cards can supply power to CPU board)
 - RTC backup battery

1.2 Block Diagram

Figure 1 shows the block diagram of the CPU_45A-V2 board. There are following building blocks:

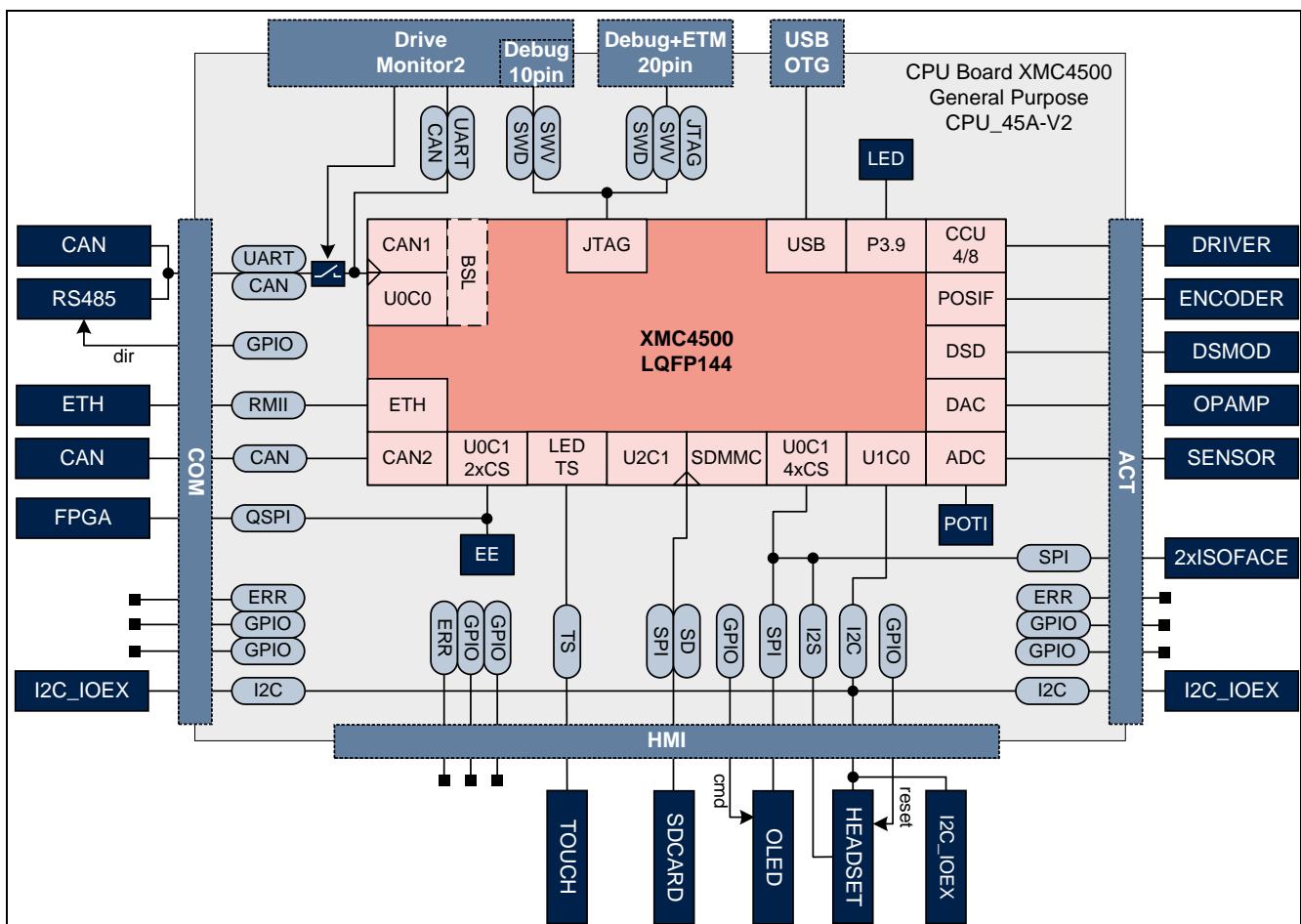


Figure 1 CPU_45A-V2 Board Block Diagram

2 Hardware Description

The following sections give a detailed description of the hardware and how it can be used.

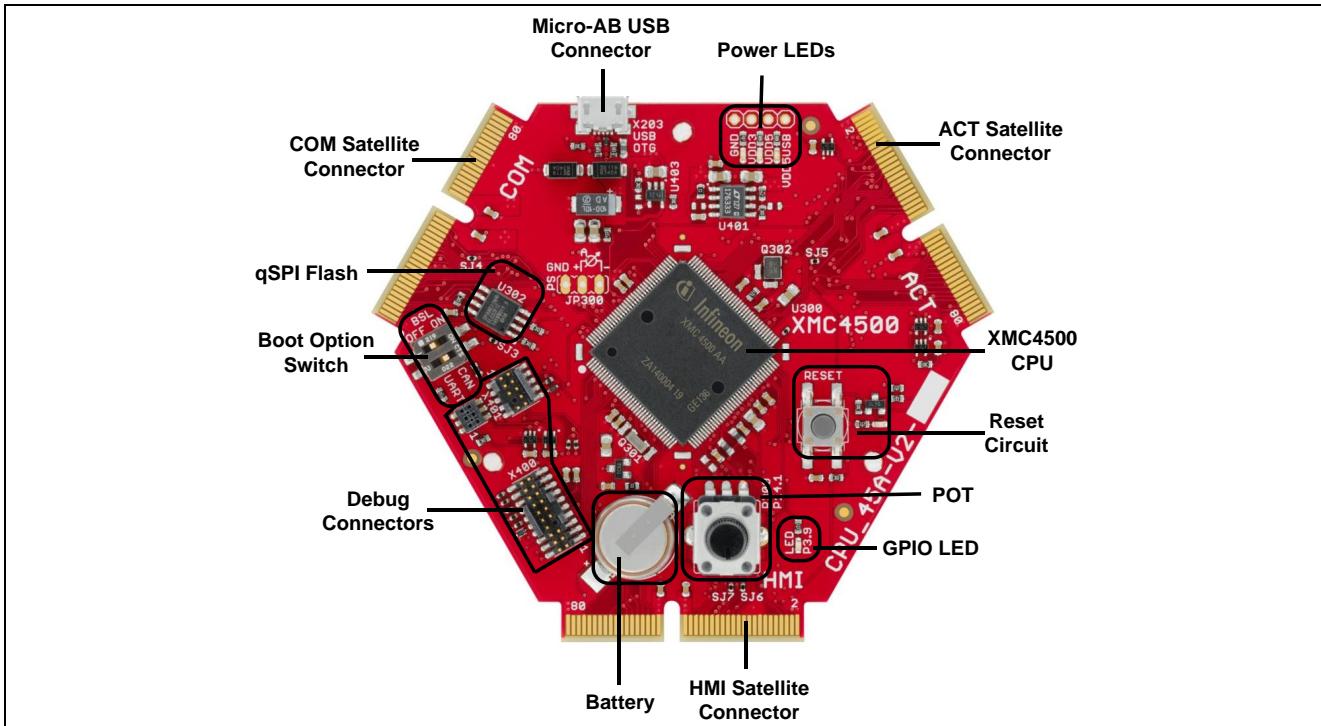


Figure 2 CPU Board XMC4500 General Purpose (CPU_45A-V2)

2.1 Power Supply

The CPU_45A-V2 board can be powered from USB (5 V); however, there is a current limit that can be drawn from the host PC through USB. If the CPU_45A-V2 board is used to drive other satellite cards (e.g. AUT_ISO-V1) and the total current required exceeds 500 mA, then the board needs to be powered by either an external USB power supply or a satellite card.

For powering the board through USB interface, connect the USB cable provided with the kit to the Micro AB USB connector on board.

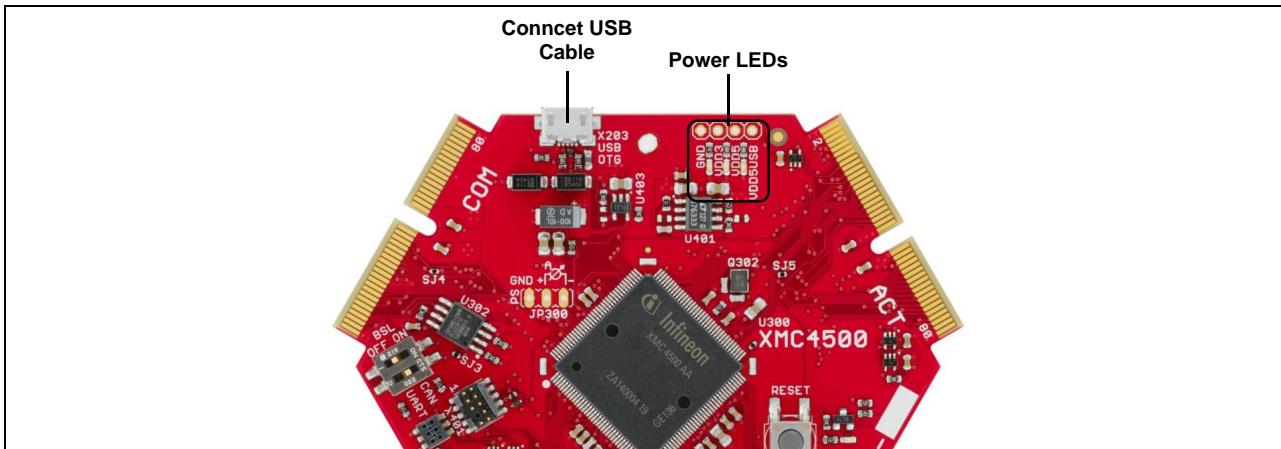


Figure 3 Powering option through USB interface (5 V)

Hardware Description

To indicate the power status of CPU_45A-V2 board three LED's are provided on board (See Figure 3). The LED will be "ON" when the corresponding rail is powered.

Table 1 Power status LED's

LED Reference	Power Rail	Voltage	Note
V401	VDD5	5 V	Must always be "ON"
V402	VDD5USB	5 V	"ON" if powered by USB plug
V403	VDD3.3	3.3 V	Must always be "ON"

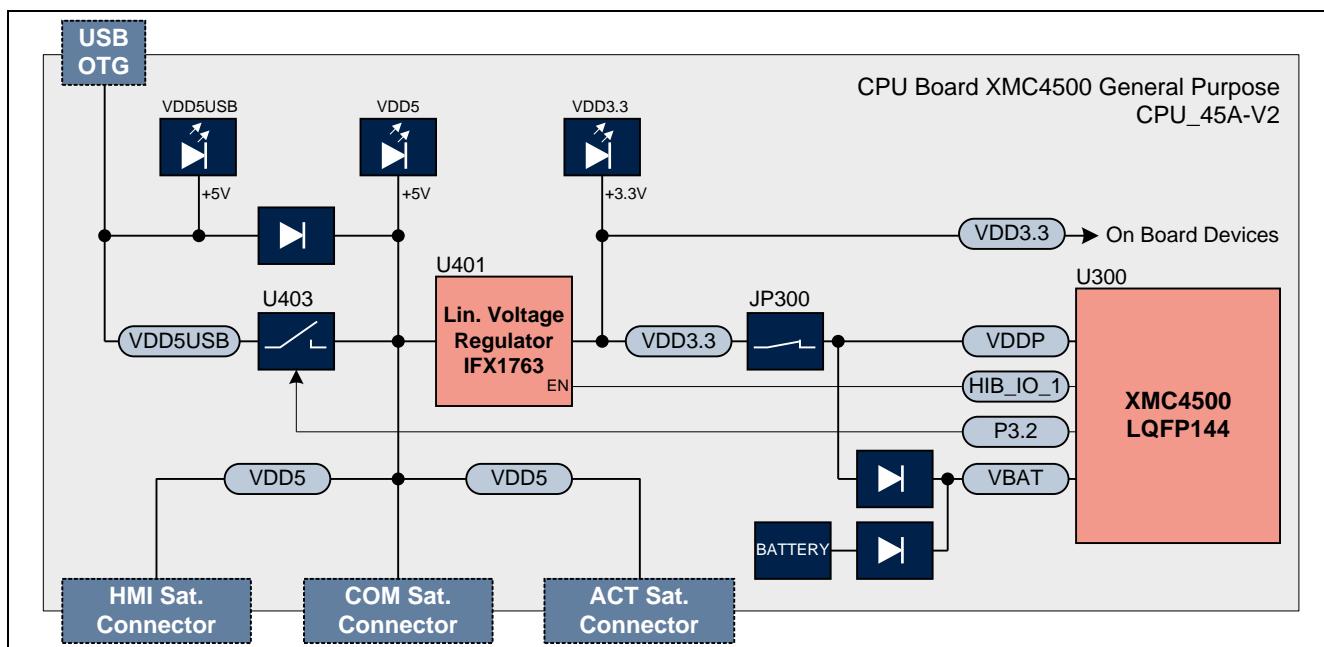


Figure 4 CPU_45A-V2 Board Power

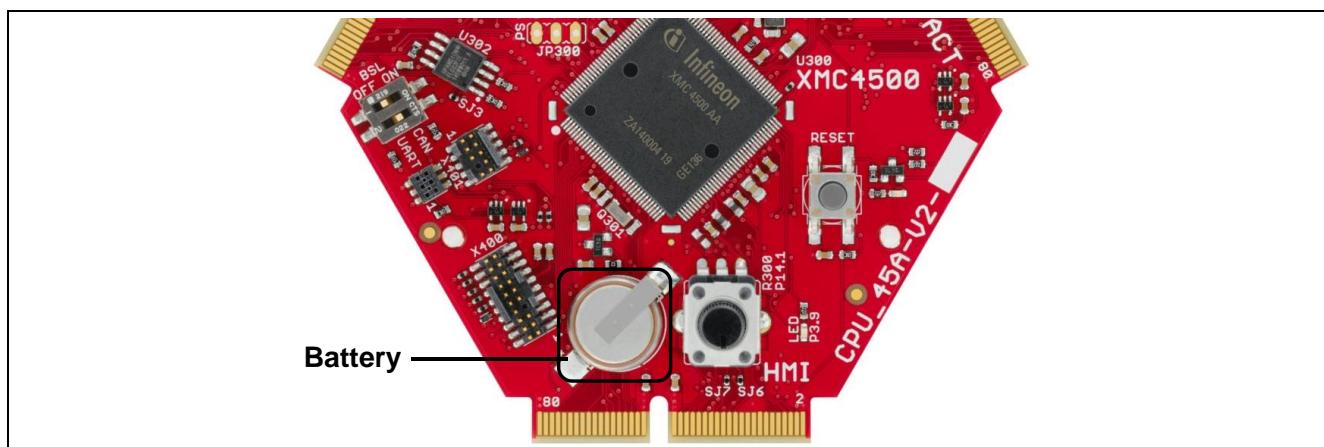


Figure 5 Battery (VBAT Supply)

Hitex PowerScale probe is provided on the CPU_45A-V2 board to measure the power consumption.

Table 2 Power Measurement

Jumper	Function	Description
JP300	PowerScale	A Hitex PowerScale probe can be connected for current sensing the VDD3.3 (CPU power source). Default: pos. 1-2 (closed) <i>Note: On the PCB there is a shorting trace between pin 1-2. This trace has to be cut first, before using PowerScale. Pin 3 is GND.</i>

The maximum current drawn by board in stand alone mode is 150 mA.

2.2 Reset

A simple RC circuit on board ensures the Power-on-Reset. Additionally an on board pushbutton switch (SW400, RESET) supports a hard reset of the CPU. This signal is routed to all the satellite connectors. The reset circuit includes a green LED (V407) to indicate the status. LED (V407) will be “ON” during reset state and will be “OFF” during normal working conditions.

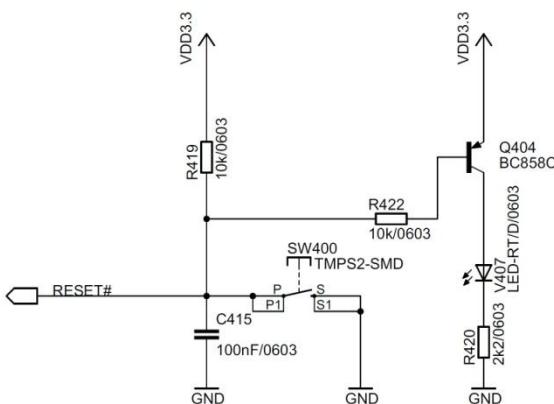


Figure 6 Reset



Figure 7 Reset LED and Reset Switch

2.3 Clock Generation

An external 12 MHz crystal provides clock signal to XMC4500 microcontroller. For RTC clock, a separate external 32.768 KHz crystal is used on board.

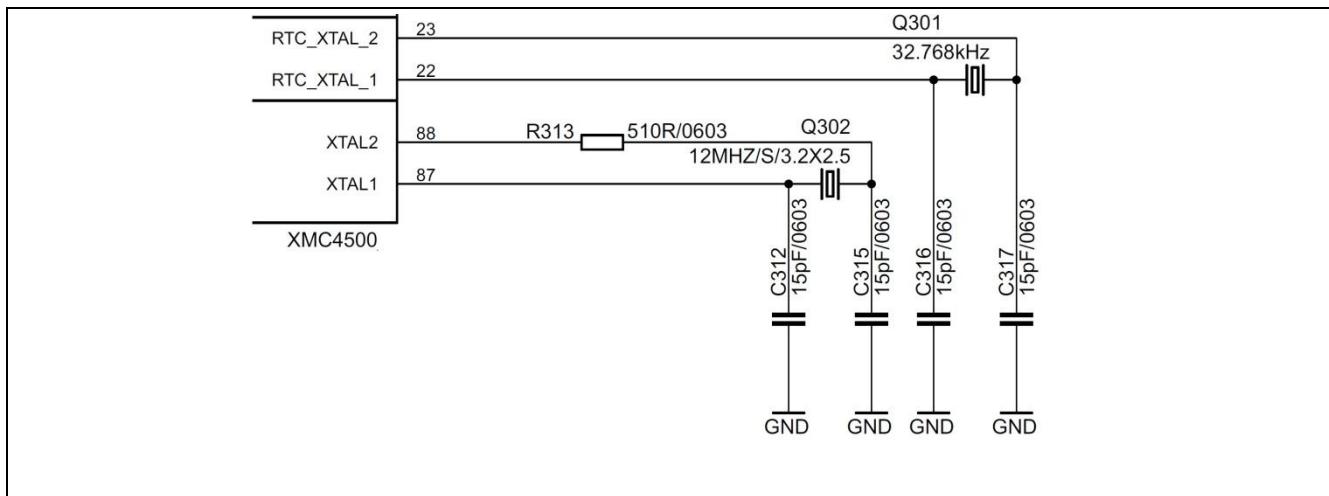


Figure 8 Clock Generation

2.4 Boot Option

During Power on Reset the XMC4500 latches SW300 settings via TCK & TMS pins. Based on the values latched different boot options are possible.

Table 3 Boot Options Settings

BSL (TMS)	CAN/UART (TCK)	Boot Option
OFF (1)	UART (0)	Normal Mode (Boot from flash)
ON (0)	UART (0)	ASC BSL Enabled (Boot from UART)
OFF (1)	CAN (1)	BMI Customized Boot Enabled
ON (0)	CAN (1)	CAN BSL Enabled (Boot from CAN)



Figure 9 Boot Options Switch

Hardware Description

The board supports boot/debug from Infineon's DriveMonitor2 Stick or COM satellite card (via UART or CAN). If a DriveMonitor2 Stick is attached to CPU_45A-V2 board via a DriveMonitor2 adapter the DM2PRES# signal will be set to low. The switches U301 and U306 will be disabled in this case. The communication to and from a COM satellite card via UART/CAN will be disconnected. This means P1.4 of XMC4500 will be disconnected from BSL_RXD signal of COM satellite card and connected to DriveMonitor Connector. Similarly pP1.5 of XMC4500 is disconnected from BSL_TXD signal of the COM satellite card and connected to DriveMonitor Connector.

If the DriveMonitor2 Stick is not present the switch U301 and U306 will be enabled. Communication to and from a COM satellite card via UART/CAN will be active. This means P1.4 of XMC4500 will be connected to BSL_RXD signal of COM satellite card and P1.5 of XMC4500 is conneted to BSL_TXD signal of the COM satellite card.

This implementation automatically takes care of switching between DriveMonitor2 Stick and COM satellite card for boot/debug and XMC4500 is not able to detect whether COM satellite card or DriveMonitor2 Stick is communicating.

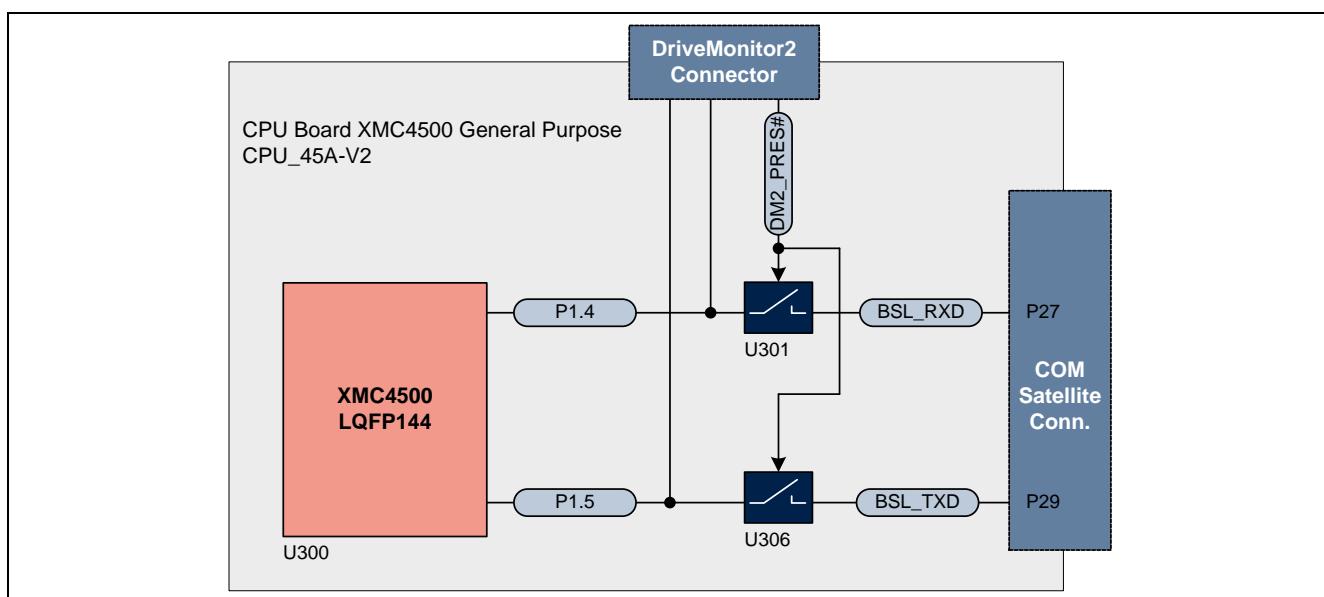


Figure 10 Boot Strap Signal Switching

2.5 Debug Interface

The CPU_45A-V2 board supports JTAG debug via 3 different connectors.

- Cortex Debug Connector (10-pin)
- Cortex Debug+ETM Connector (20-pin)
- DriveMonitor2 Connector

2.5.1 Cortex Debug Connector (10-pin)

The CPU_45A-V2 board supports JTAG debug, Serial Wire debug and Serial Wire viewer (via SWO connection when Serial Wire debug mode is used) operation through extended Cortex Debug 10-pin connector.

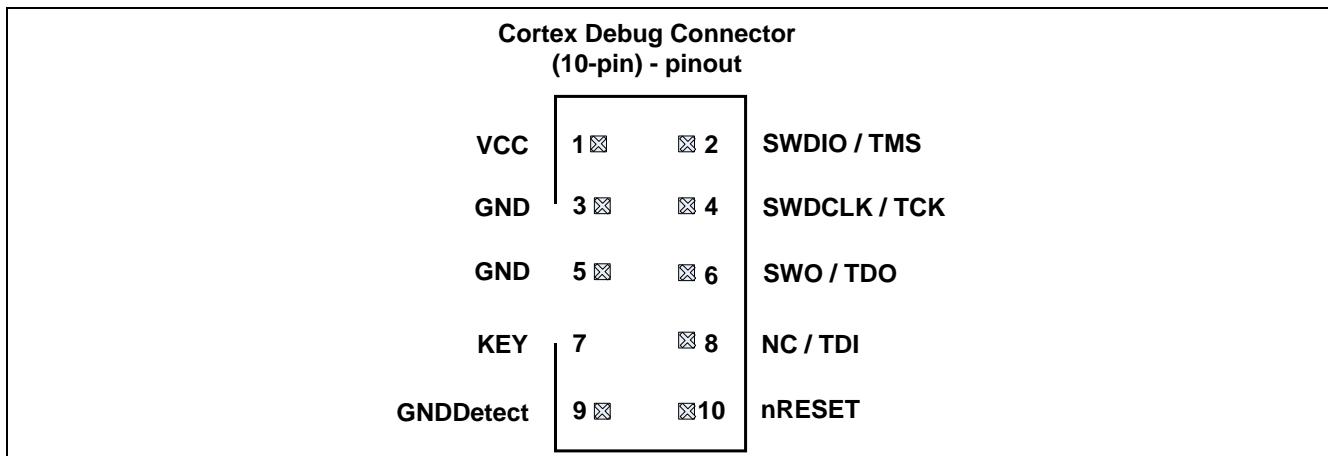


Figure 11 Cortex Debug Connector (10-pin)

Table 4 Cortex Debug Connector (10 Pin)

Pin No.	Signal Name	Serial Wire Debug	JTAG Debug
1	VCC	+3.3 V	+3.3 V
2	SWDIO / TMS	Serial Wire Data I/O	Test Mode Select
3	GND	Ground	Ground
4	SWDCLK / TCK	Serial Wire Clock	Test Clock
5	GND	Ground	Ground
6	SWO / TDO	Trace Data OUT	Test Data OUT
7	KEY	KEY	KEY
8	NC / TDI	Not connected	Test Data IN
9	GNDDetect	Ground Detect	Ground Detect
10	nRESET	Reset (Active Low)	Reset (Active Low)

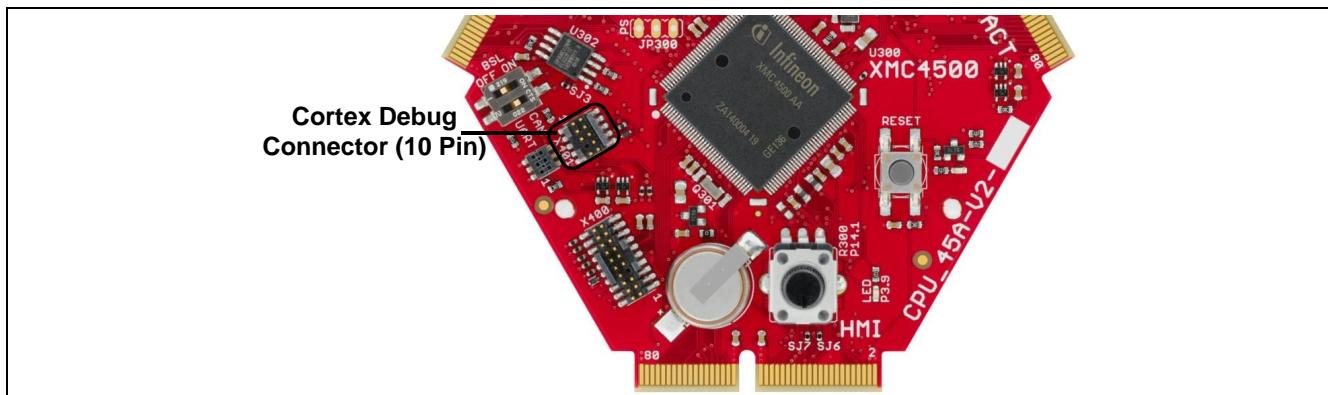


Figure 12 Cortex Debug Connector (10-pin) Layout

2.5.2 Cortex Debug+ETM Connector (20-pin)

The CPU_45A-V2 board supports JTAG debug, Serial Wire debug, Serial Wire viewer (via SWO connection when Serial Wire debug mode is used) and Instruction Trace operation through a standard 20-pin connector.

Cortex Debug+ETM Connector (20-pin) - pinout				
VCC	1	2	SWDIO / TMS	
GND	3	4	SWDCLK / TCK	
GND	5	6	SWO / TDO / EXTa / TRACECTL	
KEY	7	8	NC/EXTb/TDI	
GND/Detect	9	10	nRESET	
GND/TgtPwr+Cap	11	12	TRACECLK	
GND/TgtPwr+Cap	13	14	TRACEDATA[0]	
GND	15	16	TRACEDATC[1]	
GND	17	18	TRACEDATA[2]	
GND	19	20	TRACEDATA[3]	

Figure 13 Cortex Debug+ETM Connector (20-pin)

Table 5 Cortex Debug+ETM Connector (20 Pin)

Pin No.	Signal Name	Serial Wire Debug	JTAG Debug
1	VCC	+3.3 V	+3.3 V
2	SWDIO / TMS	Serial Wire Data I/O	Test Mode Select
3	GND	Ground	Ground
4	SWDCLK / TCK	Serial Wire Clock	Test Clock
5	GND	Ground	Ground
6	SWO / TDO	Trace Data OUT	Test Data OUT
7	KEY	KEY	KEY
8	NC / TDI	Not connected	Test Data IN
9	GND/Detect	Ground Detect	Ground Detect
10	nRESET	Reset (Active Low)	Reset (Active Low)
11	GND/TgtPwr+Cap	Ground	Ground
12	TRACECLK	Trace Clock	Trace Clock
13	GND/TgtPwr+Cap	Ground	Ground
14	TRACEDATA[0]	Trace Data 0	Trace Data 0
15	GND	Ground	Ground
16	TRACEDATA[1]	Trace Data 1	Trace Data 1
17	GND	Ground	Ground

Table 5 Cortex Debug+ETM Connector (20 Pin)

Pin No.	Signal Name	Serial Wire Debug	JTAG Debug
18	TRACEDATA[2]	Trace Data 2	Trace Data 2
19	GND	Ground	Ground
20	TRACEDATA[3]	Trace Data 3	Trace Data 3

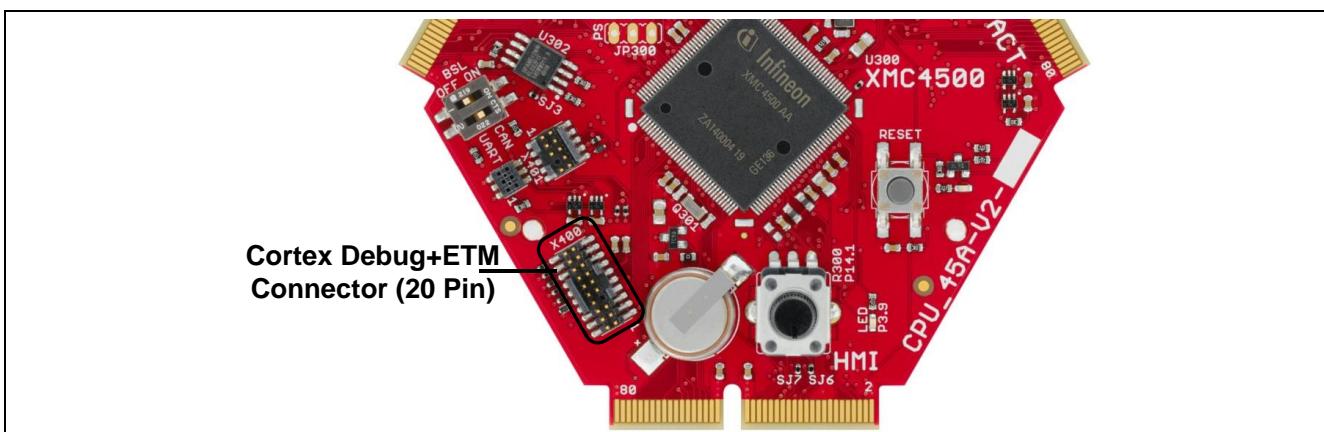


Figure 14 Cortex Debug+ETM Connector (20-pin) Layout

2.5.3 DriveMonitor2 Connector

The Coretex debug connector explained in section 2.5.1 and a small 6-pin connector on board together works as DriveMonitor2 connector. DriveMonitor2 adapter card interfaces DriveMonitor2 Stick to these connectors.

Note: Do not use Cortex debug+ETM connector (20-pin) and DriveMonitor2 connector at the same time.

6 Pin Connector - pinout

VCC	1	2	UART_TX
GND	3	4	UART_RX
GND	5	6	nRESET

Figure 15 6-Pin Connector

Table 6 6-pin Connector

Pin No.	Signal Name	Description
1	VCC	3.3 V
2	UART_TX	Transmit Data
3	GND	Ground
4	UART_RX	Receive Data
5	GND	Ground

Table 6 6-pin Connector

Pin No.	Signal Name	Description
6	nRESET	Reset (Active low)



Figure 16 DriveMonitor2 Connector

2.6 Serial Flash Memory

The CPU_45A-V2 board has 32Mbit serial flash memory interfaced to XMC4500 through a SPI interface. The SPI interface can be configured as single, dual or quad SPI.

Table 7 Quad SPI Signals

Pin No.	Pin Description	Signal Name	Signal Description
P0.13	U1C1_SCLKOUT	CLK	Clock
P3.3	U1C1_SELO1	CS#	Active Low Chip Select
P3.15	U1C1_DOUT0	DI	Data Input
P3.14	U1C1_DX0B	DO	Data Output
P0.14	U1C1_HWIN3	Data I/O	Data Input/Output
P0.15	U1C1_HWIN2	Data I/O	Data Input/Output

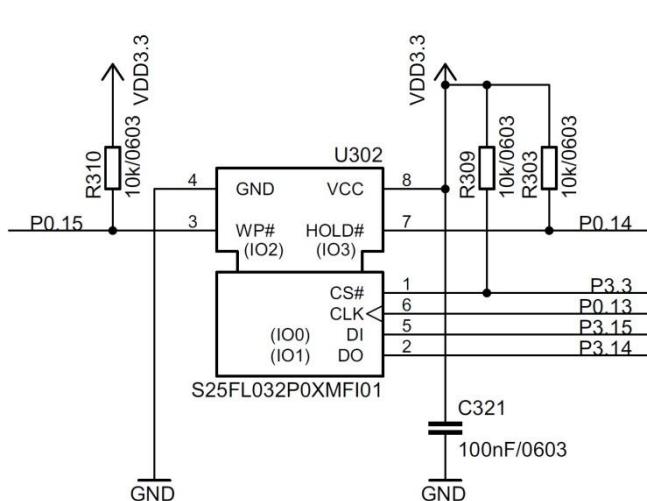


Figure 17 Quad SPI Flash Interface

2.7 USB

The XMC4500 supports USB interface in the host only mode, the device only mode or as an OTG Dual Role Device (DRD). In USB device mode, power is expected through VBUS (pin 1) from an external host (e.g. PC). When the current is more than 500 mA power from an external source through satellite cards shall be used.

Note: Some PCs, notebooks or hubs have a weak USB supply which is not sufficient for proper supply. In this case use the external 24V supply or a powered USB hub.

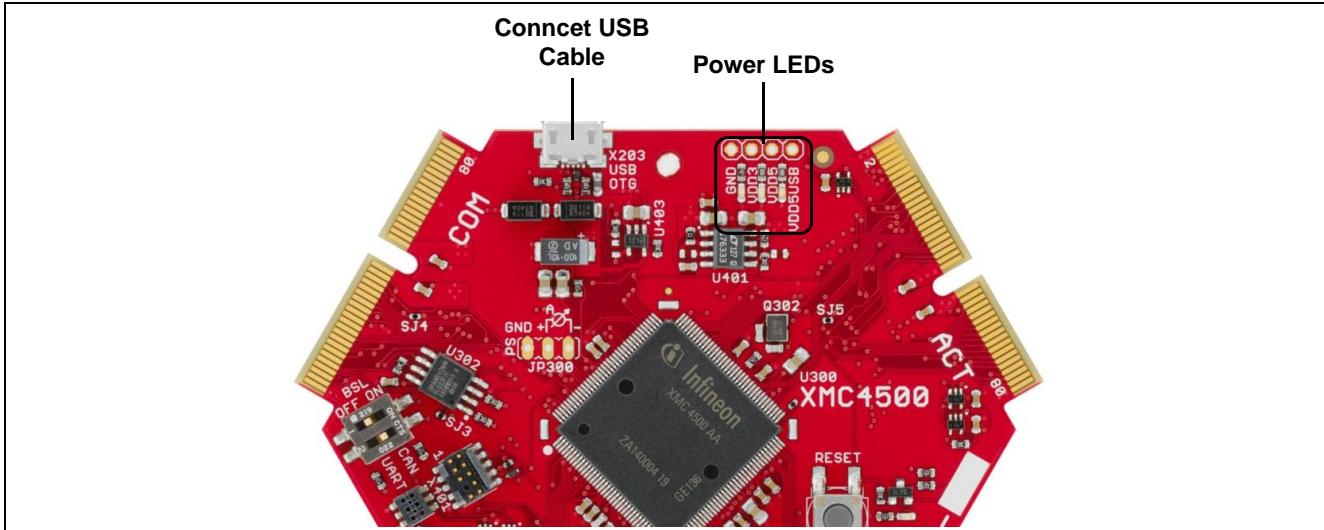


Figure 18 USB Connector

Port P0.9 of XMC4500 is connected to the ID pin (pin 4). An OTG device will detect whether a USB 3.0 Micro-A or Micro-B plug is inserted by checking the ID pin. When the ID = FALSE, Micro-A connector is plugged and when ID = TRUE a micro-B connector is interface. When ID is true the XMC4500 acts as USB host else as USB device.

Table 8 USB micro AB connector Pinout

Pin No.	Pin Name	Pin Description
1	VBUS	5 V
2	D-	Data Minus
3	D+	Data Plus
4	ID	Identification
5	GND	Ground

In the host only mode and OTG mode the CPU_45A-V2 board is capable of supplying power to the connected device (e.g. USB mouse). The board has a power-switch which is controlled by the XMC4500. Port P3.2 (active high) is used for this purpose. In the Host/OTG mode, if the external device draws more than 500mA, a low is indicated to XMC4500 via HIB_IO_0 signal. HIB_IO_0 signal is used as general purpose input pin for this implementation.

Diode V400 will allow powering the board through USB.

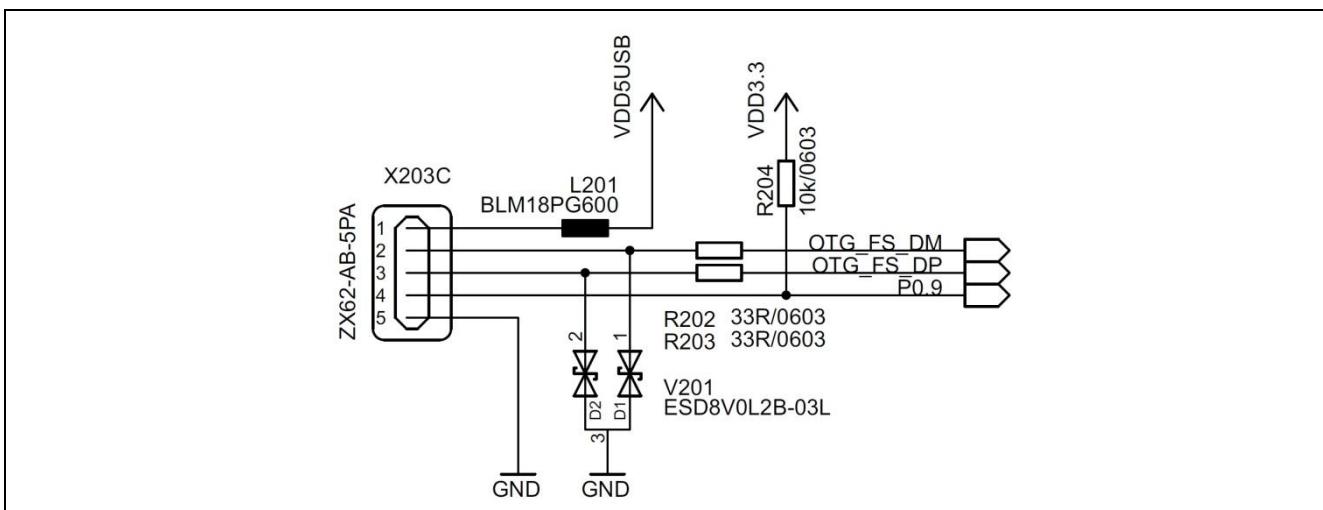


Figure 19 USB power generation - Host/OTG mode

2.8 RTC

The XMC4500 CPU has two power domains, core power domain and hibernate domain. The core power domain (VDDP pins) is connected to VDD3.3 rail. An on board LDO generates VDD3.3 (3.3 V) from VDD5 (5 V). The hibernate domain is powered via the auxiliary supply VBAT. A 3 V lithium coin cell on board or 3.3 V (VDD3.3) provides power to the auxiliary supply pin VBAT.

The RTC is located in the hibernate domain. The XMC4500 uses HIB_IO_1 signal (Active low) to shutdown the LDO which generates VDD3.3 (core domain). Even if the Core Domain is not powered the Hibernate Domain will operate if VBAT is available. RTC keeps running as long as the hibernate domain is powered via the auxiliary supply VBAT. The RTC is capable to wake-up the whole system from Hibernate domain by setting HIB_IO_1 to high.

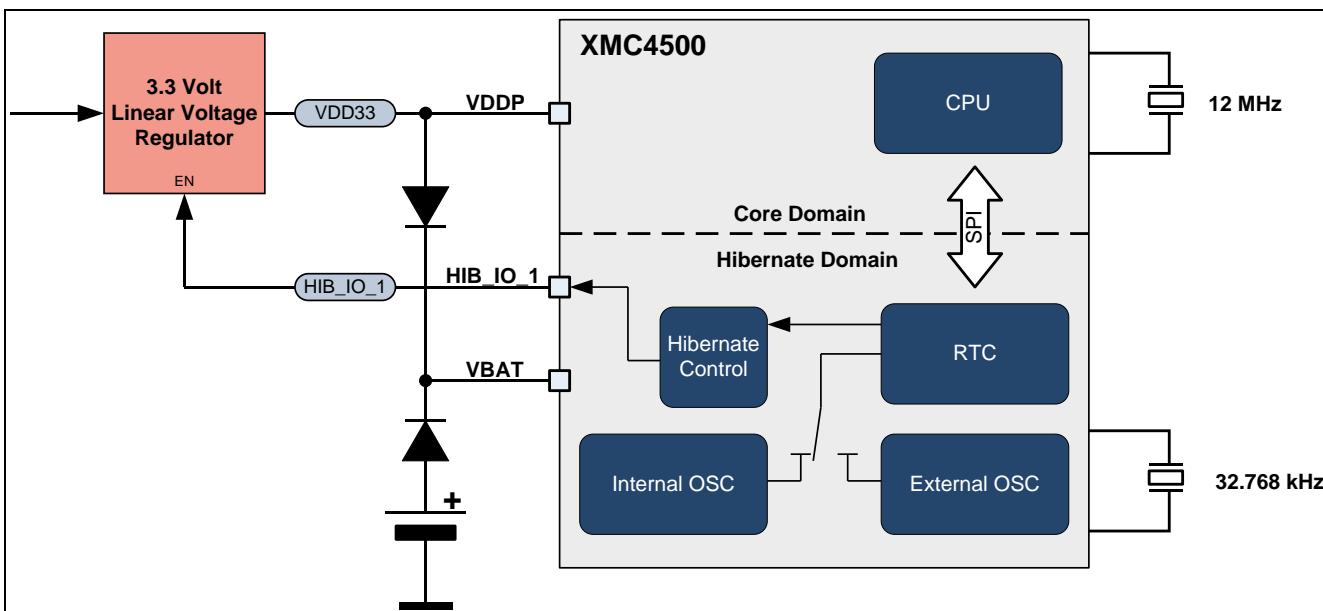


Figure 20 RTC

2.9 LED

The port pin P3.9 of XMC4500 on the CPU_45A-V2 board is connected to LED V300. More user LED's are available through I2C GPIO expander on most of the satellite cards.

Table 9 GPIO LED

LED	Connected to Port Pin
V300	P3.9

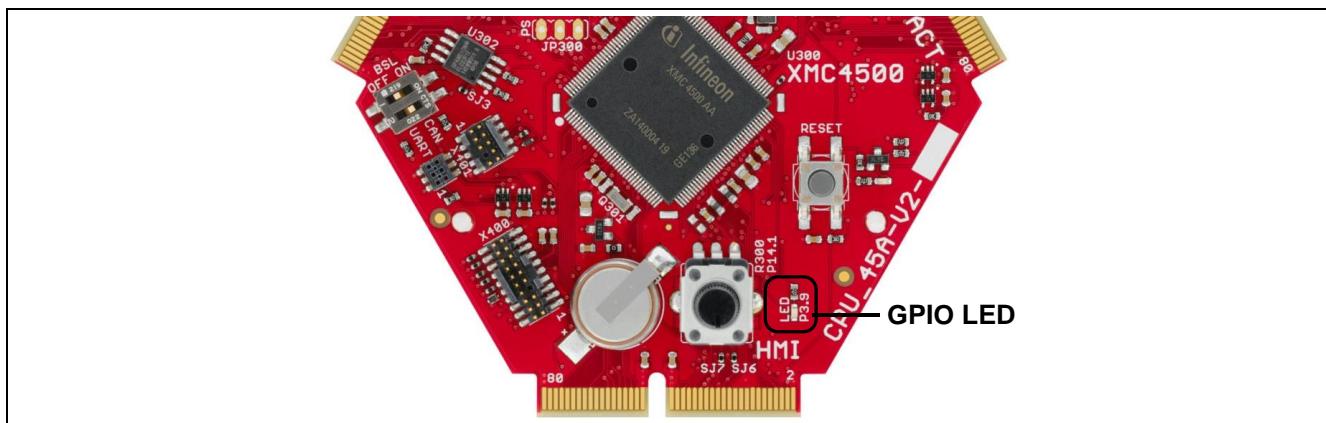


Figure 21 GPIO LED

2.10 Potentiometer

The CPU_45A-V2 board provides a potentiometer POT1 for ease of use and testing of the on-chip analog to digital converter. The potentiometer is connected to the analog input G0_CH1 (P14.1). The analog output of the potentiometer ranges from 0 V to 3.3 V.

2.11 Satellite Connectors

The CPU_45A-V2 board has three satellite connector types

- COM satellite connector (Communication)
- HMI satellite connector (Human Machine Interface)
- ACT satellite connector (Actuator)

The satellite connector interfaces the satellite cards to the CPU board.

Note: Only respective application satellite cards shall be connected to the respective satellite connectors.

(For e.g. COM satellite cards shall be connected only to COM satellite connector only)

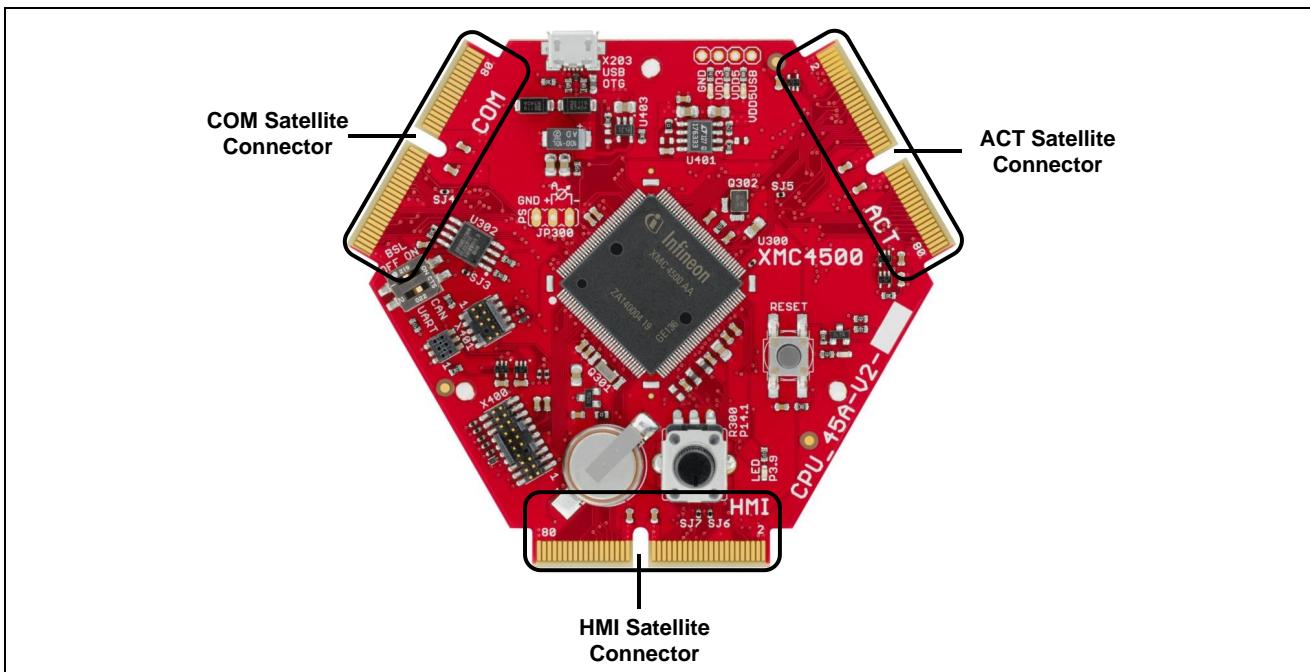


Figure 22 Satellite Connectors

2.11.1 COM Connector

The COM satellite connector on the CPU_45A-V2 board allows interface expansion through COM satellite cards (e.g. COM_ETH-V1)

CPU_45A V2 function >>		COM		GND		GND			
CPU_45A V2 pins >>		2	4	6	P3.15	U1C1_DOUT0	P3.14	U1C1_DOUT1	
CONpins >>		1	3	5	qSPI_SCLK	qSPI_CS	qSPI_D1	qSPI_D2	P0.15 U1C1_DOUT2
CONpins >>		7	9	10	qSPI_D3	RSVD	RSVD	RSVD	P0.14 U1C1_DOUT3
CPU_45A V2 pins >>		nc	nc	nc	RSVD	RSVD	RSVD	RSVD	nc
CONpins >>		ETH_RXD1A	P2.3	ETH_RXD1A	P2.2	ETH_RXD1A	P2.0	ETH_RXD1A	P2.9 ETH_RXD1
CPU_45A V2 pins >>		ETH_RXD0A	P2.2	ETH_RXD0A	P2.0	ETH_RXD0A	P2.7	ETH_RXD0A	P2.8 ETH_RXD0
CONpins >>		ETH_MDO	P2.0	ETH_MDO	P2.7	ETH_MDO	P5.9	ETH_MDO	P15.9 ETH_RXDVC
CPU_45A V2 pins >>		ETH_RXD0B	P2.7	ETH_RXD0B	P5.9	ETH_RXD0B	P15.9	ETH_RXD0B	P5.3 ETH_RXERD
CONpins >>		ETH_TX_EN	P5.9	ETH_TX_EN	nc	ETH_TX_EN	nc	ETH_TX_EN	P15.8 ETH_CLK_RMIC
CPU_45A V2 pins >>		U0C1_SEL00	nc	U0C1_SEL00	P3.10	U0C1_SEL00	P3.10	U0C1_SEL00	GND
CONpins >>		U0C0_DOUT11	P1.4	U0C0_DOUT11	P1.5	U0C0_DOUT11	P1.4	U0C0_DOUT11	P1.9 MOAN_N2_TxD
CPU_45A V2 pins >>		U0C0_RX0A	P1.5	U0C0_RX0A	P5.5	U0C0_RX0A	P1.5	U0C0_RX0A	P1.8 MOAN_N2_RXDA
CONpins >>		CCU81_OUT12	P5.5	CCU81_OUT12	P2.14	CCU81_OUT12	P2.14	CCU81_OUT12	P3.13 U0C1_DOUT0
CPU_45A V2 pins >>		I2C_SDA	P2.14	I2C_SDA	P14.13	I2C_SDA	P14.13	I2C_SDA	P2.5 U0C1_RXOB
CONpins >>		COMERR	P14.13	COMERR	P3.7	COMERR	P3.7	COMERR	P0.6 P0.6
CPU_45A V2 pins >>		XC822_tbd	P14.13	XC822_tbd	P3.7	XC822_tbd	P3.7	XC822_tbd	RESET PORST# PORST
CONpins >>		V _{S_MAIN}	5V	V _{S_MAIN}	5V	V _{S_MAIN}	5V	V _{S_MAIN}	5V
CPU_45A V2 pins >>		RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
CONpins >>		EBU_A	EBU_A	EBU_A	EBU_A	EBU_A	EBU_A	EBU_A	EBU_A
CPU_45A V2 pins >>		EBU_B	EBU_B	EBU_B	EBU_B	EBU_B	EBU_B	EBU_B	EBU_B
CONpins >>		EBU_CS	EBU_CS	EBU_CS	EBU_CS	EBU_CS	EBU_CS	EBU_CS	EBU_CS
CPU_45A V2 pins >>		GND	GND	GND	GND	GND	GND	GND	GND

Figure 23 Satellite Connector Type COM

2.11.2 HMI Connector

The HMI satellite connector on the CPU_45A-V2 board allows interface expansion through HMI satellite cards (e.g. HMI_OLED-V1)

CPU_45A V2 function >>		HMI													
CPU_45A V2 pins >>		CONpins >>							CONpins >>						
CPU_45A V2 pins >>		CPU_45A V2 function >>							CPU_45A V2 function >>						
GND	GND	GND	GND	GND	P3.6	MMC_CLK	GND	GND	P0.11	MMC_NRST	P4.0	MMC_DATA0	P1.7	MMC_DATA0	MMC_IRQ1
nc	nc	PFI1IN0	P1.3	PIFOIN1	P1.6	MMC_DATA1	1	4	6	MMC_DATA0	P4.0	MMC_DATA0	P1.7	MMC_DATA0	MMC_IRQ1
nc	nc	PFI1IN1	P1.2	PIFOIN2	P1.5	MMC_DATA3	3	5	7	8	MMC_DATA2	P1.7	MMC_DATA2	nc	nc
nc	nc	PFI1IN2	P1.1	PIFOIN3	P1.4	MMC_DATA5	nc	9	10	12	MMC_DATA4	nc	MMC_DATA4	nc	nc
nc	nc	DSD_PWMN	P1.0	DSDIN0	P0.8	DSD_DIN0A	9	10	11	12	MMC_DATA7	nc	MMC_DATA6	nc	nc
DSD_PWMMP	P5.1	PWMMP	P2.6	DSDIN1	P2.6	DSD_DIN1B	11	12	13	14	MMC_BUSPOW	P3.5	MMC_GND	P3.5	MMC_GND
DSD_MCLK2A	P1.7	DSDCLK0	P1.6	DSDIN2	P6.5	DSD_DIN2A	13	14	15	16	MMC_CMD	P5.11	MMC_GND	P5.11	MMC_GND
DSD_MCLK3B	P3.4	DSDCLK1	P6.5	DSDIN3	nc	DSD_DIN3A	15	16	17	18	MMC_LED	nc	MMC_SDWC	nc	nc
nc	nc	RSVD	nc	RSVD	nc	RSVD	17	18	19	20	RSVD	nc	RSVD	nc	nc
CCU43_INSA	P4.3	CC_IN3	P4.6	CC_IN0	P4.6	CCU43_INDA	19	20	21	22	I2S_WA	P5.11	OLED_CMD	P5.11	P5.11
CCU81_IN1B	P5.2	CC_IN4	P4.5	CC_IN1	P4.5	CCU43_INIA	21	22	23	24	I2S_WA	P3.13	UOC1_DOUT0	P3.13	UOC1_DOUT0
CCU81_INSB	P5.4	CC_IN5	P4.4	CC_IN2	P4.4	CCU43_INZA	23	24	25	26	I2S_MCLK	P2.5	UOC1_DXOB	P2.5	UOC1_DXOB
CCU80_INDA	P0.7	TRAP_A	P2.13	ENA_A	P2.13	CCU43_IN2C	25	26	27	28	I2S_SYNCCLK	P3.0	I2S_SCLK	P3.0	I2S_SCLK
CCU81_INDA	P5.0	TRAP_B	P2.12	ENA_B	P2.12	CCU43_IN3C	27	28	29	30	SPI_CS0	P3.12	SPI_MTSR	P3.13	UOC1_DOUT0
CCU43_INDC	P4.7	TRAP_X	P6.4	ENA_X	P6.4	CCU43_OUT1	29	30	31	32	SPI_CS1	P3.1	SPI_MTSR	P2.5	UOC1_DXOB
UOC1_SEL01	P3.11	SPI_CSA0	P3.13	SPI_MTSR	P3.13	UOC1_DOUT0	31	32	33	34	SPI_CS2	P3.0	I2S_SCLK	P3.0	I2S_SCLK
UOC1_SEL03	P3.8	SPI_CSA1	P2.5	SPI_MRST	P2.5	UOC1_DXOB	33	34	35	36	I2C_SDA	P5.8	I2C_SCL	P5.8	I2C_SCL
UOC1_DXOCDOUT	P2.14	I2C_SDA	P5.8	I2C_SCL	P3.0	UOC1_SCLKOUT	35	36	37	38	I2C_SDA	P15.5	HMI_ERR	P0.6	P0.6
XG822.fbd	P15.4	ACTERR	P0.6	GPIO	P0.6	P0.6	40	41	42	43	HMI_GPIO	P5.6	RESET#	P0.6	P0.6
P4.2	P4.2	ACT_GPIO	41	RESET	42	PORST#	43	44	45	46	5V	5V	5V	5V	5V
5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	VAGND	AGND	AREF	VAREF	VAREF
5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	VAGND	AGND	AREF	VAREF	VAREF
VADC_GICH1	P14.9	DAC0/ADC1	P14.8	DAC1/ADC0	P14.9	DAC0/ADC0	49	50	51	52	DAC0/ADC1	P14.8	DAC0/ADC0	P14.8	VADC_GICH4
VADC_GICH6	P14.6	ADC3/ORC0	P14.4	ADC2/DACREF	P14.4	VADC_GUCH4	51	52	53	54	ADC15	P14.12	VADC_GUCH4	P14.12	VADC_GUCH3
VADC_GICH7	P14.7	ADC5/ORC2	P14.14	ADC4/ORC1	P14.14	VADC_GICH6	53	54	55	56	ADC16	P15.13	VADC_GUCH3	P15.13	VADC_GUCH3
VADC_GCH0	P14.0	ADC7	P14.15	ADC6/ORC3	P14.15	VADC_GICH7	55	56	57	58	ADC17	P15.12	VADC_GCH2	P15.2	VADC_GCH2
VADC_GCH5	P14.5	ADC9	P14.2	VADC_G00H2	P14.2	VADC_G00H2	57	58	59	60	RSVD	nc	RSVD	nc	nc
VADC_G3CH6	P15.14	ADC11	P15.6	VADC_G2CH6	P15.6	VADC_G2CH6	59	60	61	62	RSVD	nc	RSVD	nc	nc
VADC_G3CH7	P15.15	ADC13	P15.7	VADC_G2CH7	P15.7	VADC_G2CH7	61	62	63	64	TP7	P5.10	LEDTS_TSIN7/A	P5.10	LEDTS_TSIN7/A
CCU81_OUT00	P1.15	PWMBO_H	P0.5	CCU80_OUT00	P0.5	CCU80_OUT00	63	64	65	66	TPx1	TP6	nc	nc	nc
CCU81_OUT01	P1.12	PWMBO_L	P0.2	CCU80_OUT01	P0.2	CCU80_OUT01	65	66	67	68	TPx0	TP5	nc	nc	nc
CCU81_OUT10	P1.14	PWMBO_H	P0.4	CCU80_OUT10	P0.4	CCU80_OUT10	67	68	69	70	COL3	TP4	nc	nc	nc
CCU81_OUT11	P1.11	PWMBO_L	P0.1	CCU80_OUT11	P0.1	CCU80_OUT11	69	70	71	72	COL2	TP3	nc	nc	nc
CCU81_OUT20	P1.13	PWMBO_H	P0.3	CCU80_OUT20	P0.3	CCU80_OUT20	71	72	73	74	COL1	TP2	P2.4	P2.4	LEDTS_TSIN2/A
CCU81_OUT21	P1.10	PWMBO_L	P0.0	CCU80_OUT21	P0.0	CCU80_OUT21	73	74	75	76	COL0	TP1	nc	nc	nc
CCU81_OUT31	P6.0	PWMX0	P6.3	CCU80_OUT32	P6.3	CCU80_OUT32	75	76	77	78	COLA	TP0	nc	nc	nc
CCU81_OUT30	P6.1	PWMX3	P6.2	CCU80_OUT33	P6.2	CCU80_OUT33	77	78	79	80	GND	GND	GND	GND	GND

Figure 24 Satellite Connector Type HMI

2.11.3 ACT Satellite Connector

The ACT satellite connector on the CPU_45A-V2 board allows interface expansion through ACT satellite cards (e.g. AUT_ISO-V1)

CPU_45A V2 function >>		ACT													
CPU_45A V2 pins >>		CONpins >>							CONpins >>						
CPU_45A V2 pins >>		CPU_45A V2 function >>							CPU_45A V2 function >>						
GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
nc	nc	PFI1IN0	P1.3	PIFOIN1	P1.4	MMC_CLK	P3.6	MMC_CLK	P3.6	MMC_CLK	P3.6	MMC_CLK	P3.6	MMC_CLK	P3.6
nc	nc	PFI1IN1	P1.2	PIFOIN2	P1.5	MMC_DATA1	P1.6	MMC_DATA1	P1.6	MMC_DATA1	P1.6	MMC_DATA1	P1.6	MMC_DATA1	P1.6
nc	nc	PFI1IN2	P1.1	PIFOIN3	P1.4	MMC_DATA3	P4.1	MMC_DATA3	P4.1	MMC_DATA3	P4.1	MMC_DATA3	P4.1	MMC_DATA3	P4.1
nc	nc	DSD_PWMN	P1.0	DSDIN0	P0.8	DSD_DIN0A	P0.8	DSD_DIN0B	P0.8	DSD_DIN0B	P0.8	DSD_DIN0B	P0.8	DSD_DIN0B	P0.8
DSD_PWMMP	P5.1	PWMMP	P2.6	DSDIN1	P2.6	DSD_DIN1B	P2.6	DSDIN2	P1.6	DSD_DIN2A	P1.6	DSD_DIN2A	P1.6	DSD_DIN2A	P1.6
DSD_MCLK2A	P1.7	DSDCLK0	P1.6	DSDIN2	P6.5	DSD_DIN2A	P6.5	DSDIN3	P6.5	DSD_DIN3A	P6.5	DSD_DIN3A	P6.5	DSD_DIN3A	P6.5
DSD_MCLK3B	P3.4	DSDCLK1	P6.5	DSDIN3	nc	DSD_DIN3A	nc	RSVD	nc	RSVD	nc	RSVD	nc	RSVD	nc
nc	nc	RSVD	nc	RSVD	nc	RSVD	nc	RSVD	nc	RSVD	nc	RSVD	nc	RSVD	nc
CCU43_INSA	P4.3	CC_IN3	P4.6	CC_IN0	P4.6	CCU43_INDA	P4.6	CCU43_IN1B	P4.5	CCU43_IN1A	P4.5	CCU43_IN1C	P4.5	CCU43_IN1D	P4.5
CCU81_IN1B	P5.2	CC_IN4	P4.5	CC_IN1	P4.5	CCU43_INIA	P4.5	CCU81_INSB	P4.4	CCU43_IN2A	P4.4	CCU43_IN2B	P4.4	CCU43_IN2C	P4.4
CCU81_INSB	P5.4	CC_IN5	P4.4	CC_IN2	P4.4	CCU43_INZA	P4.4	CCU80_INDA	P4.3	CCU43_IN1B	P4.3	CCU43_IN1C	P4.3	CCU43_IN1D	P4.3
CCU80_INDA	P0.7	TRAP_A	P2.13	ENA_A	P2.13	CCU43_IN2C	P2.13	CCU81_IN1B	P2.12	CCU43_IN1A	P2.12	CCU43_IN1C	P2.12	CCU43_IN1D	P2.12
CCU81_INDA	P5.0	TRAP_B	P2.12	ENA_B	P2.12	CCU43_IN3C	P2.12	CCU81_INSB	P2.11	CCU43_OUT1	P2.11	CCU43_OUT2	P2.11	CCU43_OUT3	P2.11
CCU43_INDC	P4.7	TRAP_X	P6.4	ENA_X	P6.4	CCU43_OUT1	P6.4	CCU81_INDC	P3.13	CCU43_OUT2	P3.13	CCU43_OUT3	P3.13	CCU43_OUT4	P3.13
P3.11	P3.11	SPI_CSA0	P3.13	SPI_MTSR	P3.13	SPI_CS0	P3.13	P3.11	P3.11	SPI_CS1	P3.1	SPI_CS2	P3.1	SPI_CS3	P3.1
P3.8	P3.8	SPI_CSA1	P2.5	SPI_MRST	P2.5	SPI_CS1	P2.5	P3.8	P3.8	SPI_CS2	P3.8	SPI_CS3	P3.8	SPI_CS4	P3.8
nc	nc	SPI_CS2A2	P3.0	SPI_CS2A2	P3.0	SPI_CS2	P3.0	P3.0	P3.0	SPI_CS3	P3.0	SPI_CS4	P3.0	SPI_CS5	P3.0
P2.14	P2.14	I2C_SDA	P5.8	I2C_SDA	P5.8	I2C_SCL	P5.8	P5.8	P5.8	I2C_SCL	P5.8	I2C_SCL	P5.8	I2C_SCL	P5.8
P15.4	P15.4	ACTERR	P0.6	GPIO	P0.6	P0.6	P0.6	P0.6	P0.6	GPIO	P0.6	P0.6	P0.6	P0.6	P0.6
P4.2	P4.2	ACT_GPIO	41	RESET	42	PORST#	43	44	45	46	47	48	49	49	49
5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V
5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V
VADC_GICH1	P14.9	DAC0/ADC1	P14.8	DAC1/ADC0	P14.8	VADC_GICH0	P14.9	VADC_GICH6	P14.6	VADC_GUCH4	P14.12	VADC_GUCH4	P14.12	VADC_GUCH3	P14.12
VADC_GUCH6	P14.6	ADC3/ORC0	P14.4	ADC2/DACREF	P14.4	VADC_GUCH4	P14.6	VADC_GICH7	P14.7	ADC4/ORC1	P14.14	VADC_GICH6	P15.13	VADC_GUCH3	P15.13
VADC_GICH7	P14.7	ADC5/ORC2	P14.14	ADC4/ORC1	P14.14	VADC_GICH6	P14.7	VADC_GCH0	P14.0	ADC6/ORC3	P14.15	VADC_GICH7	P15.12	VADC_GCH2	P15.12
VADC_GCH0	P14.0	ADC7	P14.15	ADC6/ORC3	P14.15	VADC_GICH7	P14.0	VADC_GCH5	P14.5	ADC9	P14.2	VADC_G00H2	P14.2	VADC_G00H2	P14.2
VADC_GCH5	P14.5	ADC9	P14.2	VADC_G00H2	P14.2	VADC_G00H2	P14.2	VADC_G3CH6	P15.14	ADC11	P15.6	VADC_G2CH6	P15.6	VADC_G2CH6	P15.6
VADC_G3CH6	P15.14	ADC11	P15.6	VADC_G2CH6	P15.6	VADC_G2CH6	P15.6	VADC_G3CH7	P15.15	ADC13	P15.7	VADC_G2CH7	P15.7	VADC_G2CH7	P15.7
VADC_G3CH7	P15.15	ADC13	P15.7	VADC_G2CH7	P15.7	VADC_G2CH7	P15.7								

3 Production Data

3.1 Schematics

This chapter contains the schematics for the CPU board:

- Satellite Connectors, USB-OTG
- XMC4500
- Power, Debug

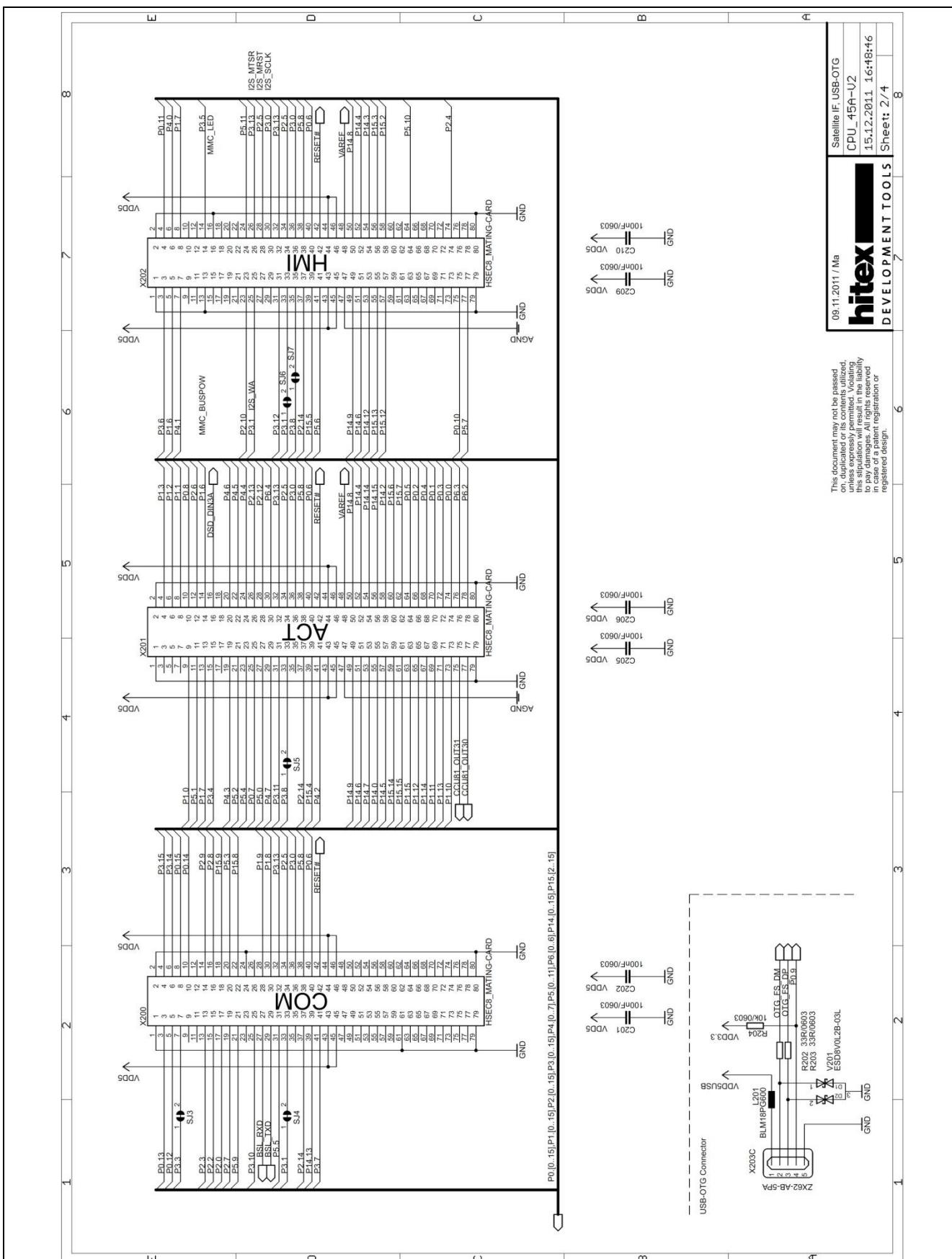
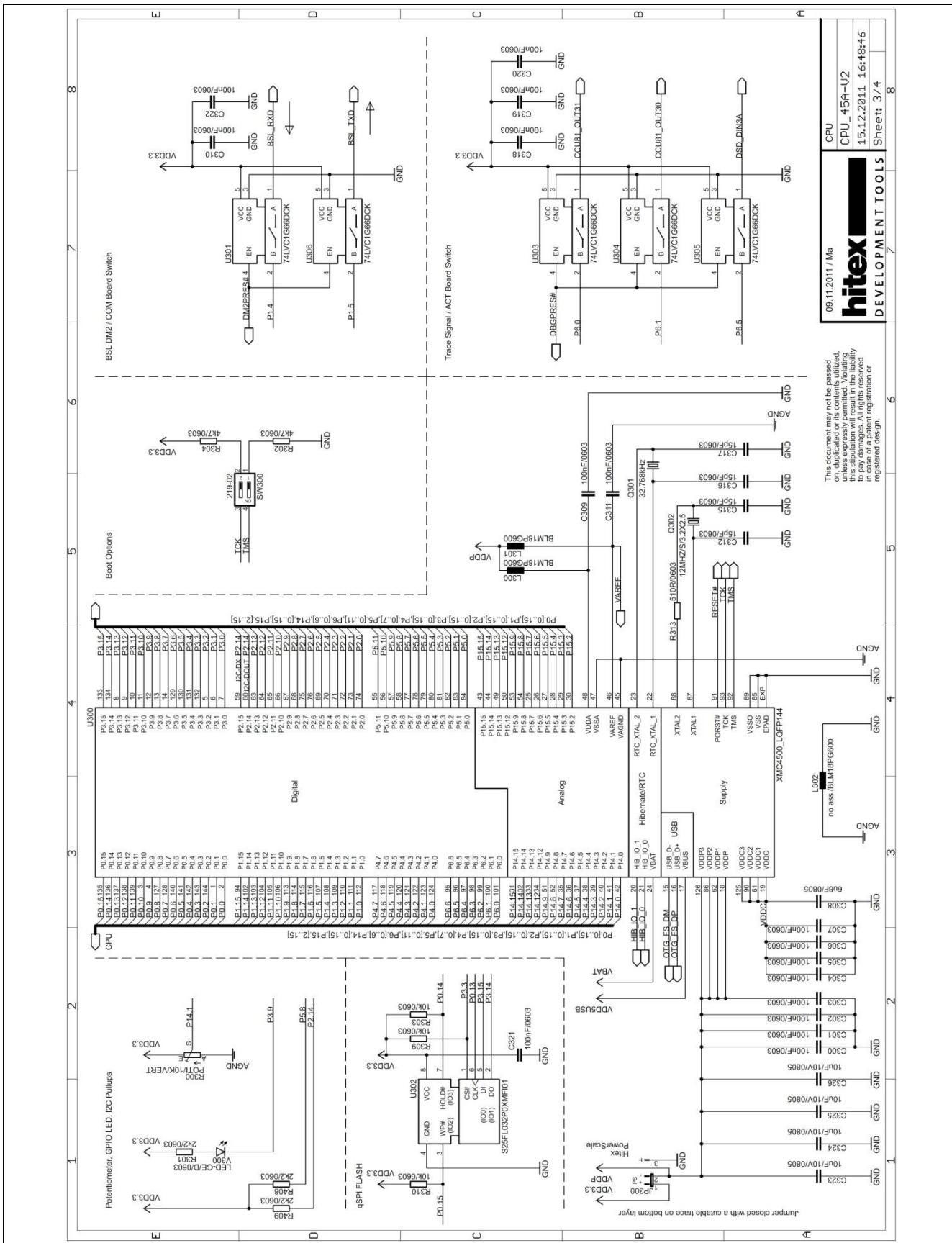


Figure 26 Satellite Connectors, USB-OTG

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DEVELOPMENT TOOLS

Satellite IF, USB-OTG
CPU_45A-U2
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Figure 27 XMC4500

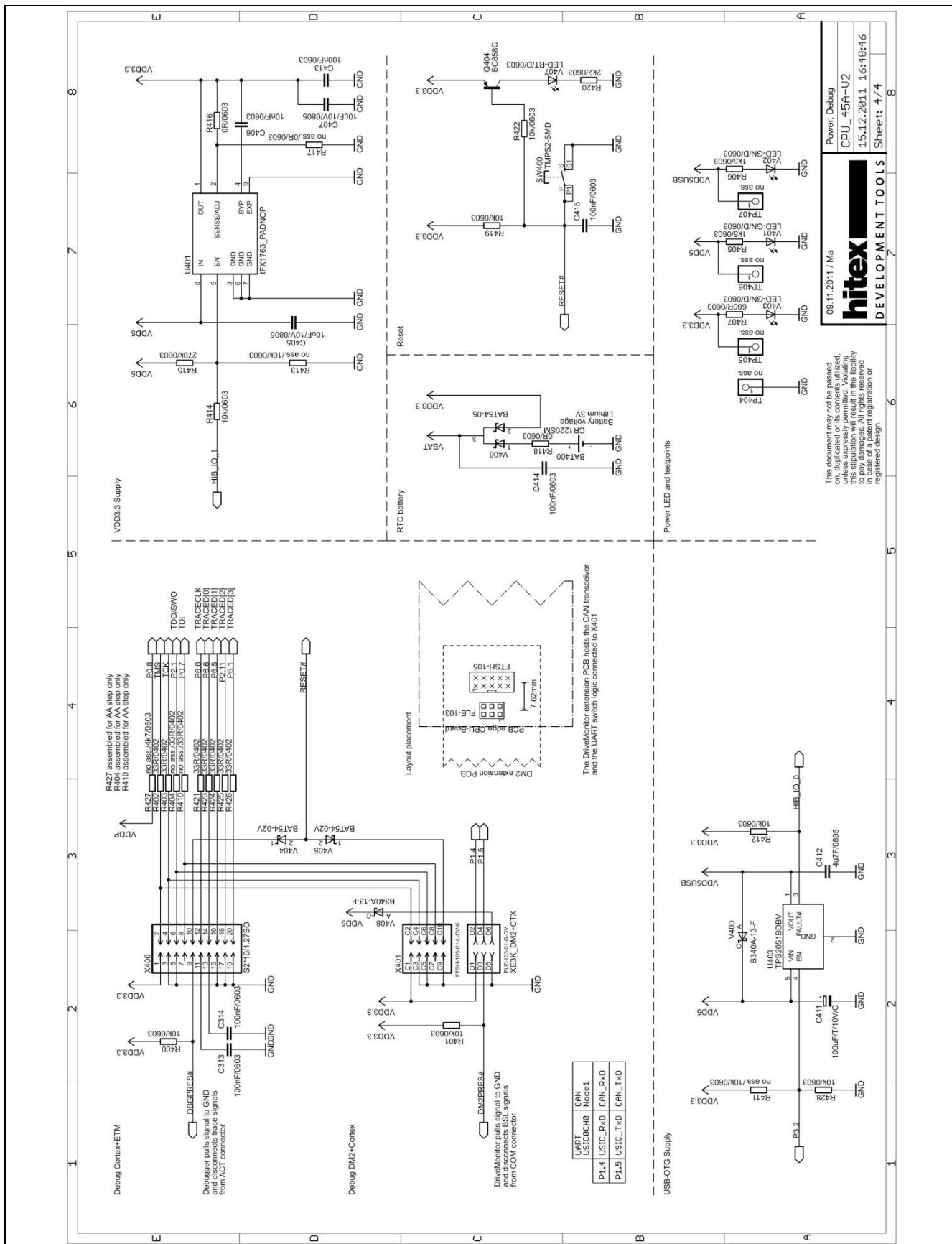


Figure 28 Power, Debug

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3.2 Layout and Geometry

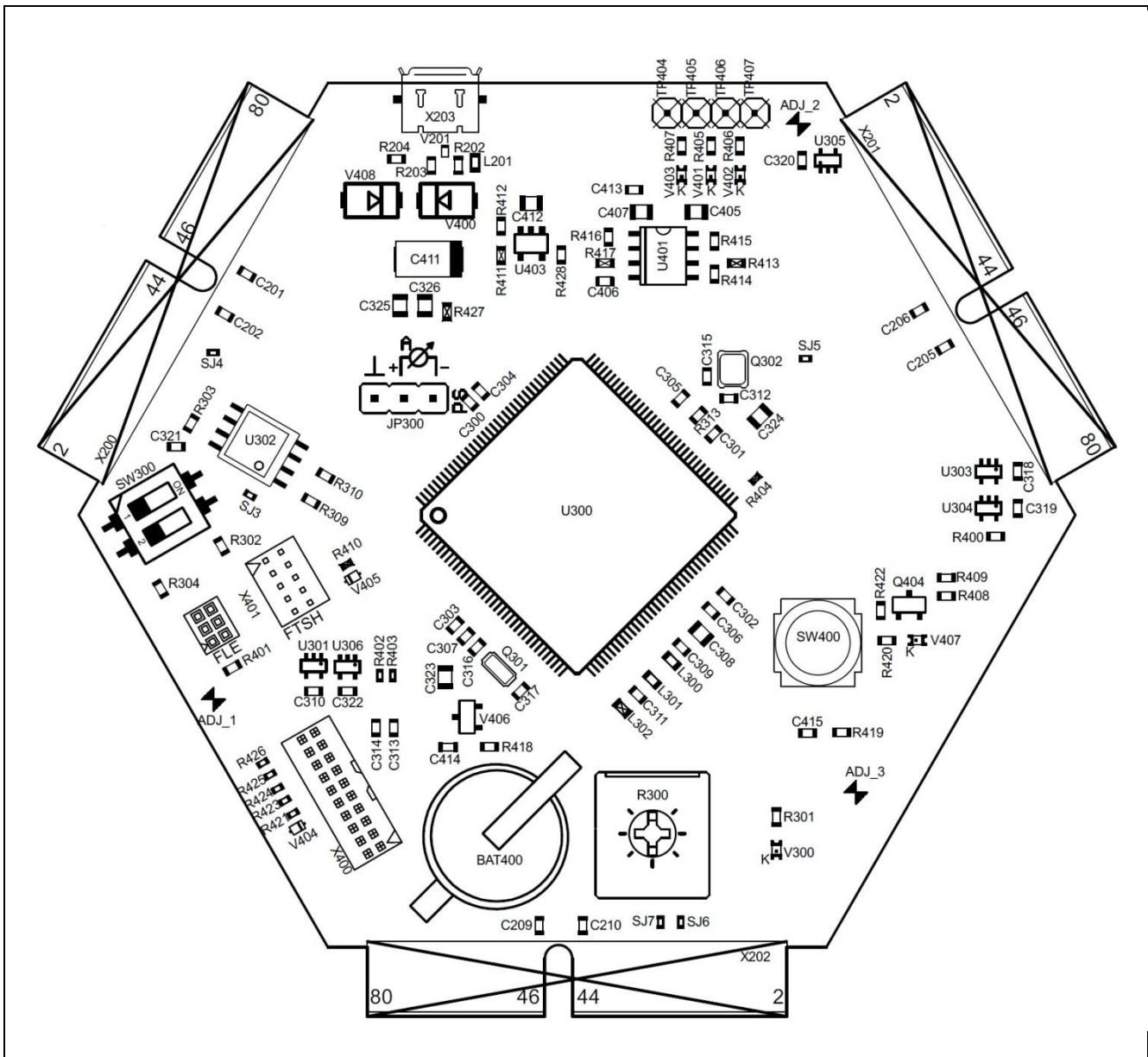


Figure 29 CPU_45A-V2 Board Layout

3.3 Bill of Material

Table 10 CPU_45A-V2 Board BOM

Pos. No.	Quantity	Value	Device	Reference Des.
1	5	0 R/0402	Resistor	SJ3, SJ4, SJ5, SJ6, SJ7
2	2	0 R/0603	Resistor	R416, R418
3	2	1 k5/0603	Resistor	R405, R406
4	4	2 k2/0603	Resistor	R301, R408, R409, R420
5	2	4 k7/0603	Resistor	R302, R304
6	1	4 u7F/0805	Capacitor	C412
7	1	6 u8F/0805	Capacitor	C308
				R204, R303, R309, R310, R400, R401, R412, R414, R419, R422, R428
8	11	10 k/0603	Resistor	
9	1	10 nF/0603	Capacitor	C406
10	6	10 uF/10 V/0805	Capacitor	C323, C324, C325, C326, C405, C407
11	1	12 MHZ/S/3.2X2.5	Crystal, 12 MHz, 3.2x2.5 mm	Q302
12	4	15 pF/0603	Capacitor	C312, C315, C316, C317
13	1	32.768 kHz	Crystal, 32.768 KHz, 3.2x1.5 mm	Q301
14	8	33 R/0402	Resistor	R402, R403, R404, R421, R423, R424, R425, R426
15	2	33 R/0603	Resistor	R202, R203
16	5	74LVC1G66DCK	IC, Texas Instruments, SN74LVC1G66DCK	U301, U303, U304, U305, U306
17	27	100 nF/0603	Capacitor	C201, C202, C205, C206, C209, C210, C300, C301, C302, C303, C304, C305, C306, C307, C309, C310, C311, C313, C314, C318, C319, C320, C321, C322, C413, C414, C415
18	1	100 uF/T/10 V/C	Capacitor	C411
19	1	219-02	Dual DIP-Switch, 0.1"pitch	SW300
20	1	270 k/0603	Resistor	R415
21	1	510 R/0603	Resistor	R313
22	1	680 R/0603	Resistor	R407
23	2	B340A-13-F	Diode, B340A-13-F Diodes Inc.	V400, V408
24	2	BAT54-02V	Diode, BAT54-02V SC79, Infineon Technologies	V404, V405
25	1	BAT54-05	Diode, BAT54-05 SOT23-3, Infineon technologies	V406
26	1	BC858C	Transistor, BC858C PNP SOT23-3	Q404
27	3	BLM18PG600	Ferrite Bead, Murata	L201, L300, L301

Table 10 CPU_45A-V2 Board BOM

Pos. No.	Quantity	Value	Device	Reference Des.
28	1	CR1220SM	Battery, 3 V Li-Ion coin cell	BAT400
29	1	ESD8V0L2B-03L	ESD8V0L2B-03L Infineon Technologies	V201
30	1	IFX1763_PADNOP	LDO, IFX1763SJV33 Infineon Technologies	U401
31	1	LED-GE/D/0603	LED	V300
32	3	LED-GN/D/0603	LED Green	V401, V402, V403
33	1	LED-RT/D/0603	LED	V407
34	1	POTI/10 K/VERT	Potentiometer, ALPS RK09K1130A8G	R300
35	1	S2*10/1.27SO	Connector, FTSFH-110-01-L-DV-K-P Samtec, without pin 7	X400
36	1	S25FL032P0XMF101	IC, Flash memory, Spansion	U302
37	1	TMPS2-SMD	FSM2JSMATR TEconn.	SW400
38	1	TPS2051BDBV	IC, TPS2051BDBV, Texas Instruments	U403
39	1	XE3K_DM2+CTX	Connector, FTSFH-105-01-LM-DV-K Samtec, without pin 7 FLE-103-01-G-DV Samtec	X401
40	1	XMC4500_LQFP144	IC, XMC4500, Infineon Technologies	U300
41	1	ZX62-AB-5PA	Connector, ZX62-AB-5PA Hirose	X203
42	4	no ass.	Pinheader, 0.1" TH	TP404, TP405, TP406, TP407
43	1	no ass./0 R/0603	Resistor	R417
44	1	no ass./4 k7/0603	Resistor	R427
45	2	no ass./10 k/0603	Resistor	R411, R413
46	1	no ass./33 R/0402	Resistor	R410
47	1	no ass./BLM18PG600	Ferrite Bead, Murata	L302
48	1	no ass.	Pinheader, 0.1" TH, Hitex PowerScale	JP300
49	3	no ass.	Edgecard connector	X200, X201, X202

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