REV	DESCRIPTION	DATE	APPROVED
A	ECO# 2095482 - Initial Release	01/08/2009	Jason Thompson

Pico-Projector Development Kit Programmer's Guide

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NHA	USED ON	QA Faisal Khan	DATE 01/08/2009	SIZE **A**	DRAWING NO 2510280	REV A
APPLICATION		APVD Jason Thompson	DATE 01/08/2009	SCALE NONE	SHEET 1 OF 16	

Revision History

Rev	Date	Section	Summery of Changes

1 Description:

This document specifies the command and control interface to the Pico-Projector development module. It defines all applicable commands, default settings, and control register bit definitions to communicate with the Pico-Projector development module.

1.1 Input Format

DVI-D interface to the Beagle board
Pixel clock: 27MHz
Pixel format: RGB888

2 Trademarks

DLP® is a trademark of Texas Instruments.

3 Reference:

For use with the Beagle Board: http://beagleboard.org/

I2C-bus specification and user manual, Rev. 03 - June 2007

4 Interface Standard

The interface used for communication with the Pico-projector is the I2C interface. The configuration registers can be accessed over the I2C interface. The respective addresses are listed in the register definition section.

4.1 I2C Interface

The I2C protocol used in communicating information to the Pico-Projector shall consist of a serial data bus conforming to the Philips I^2C specification, up to 400 KHz. The I^2C interface timing waveforms are shown in the diagram in Figure 1 and Figure 2:

4.1.1 Projector Control I2C commands

The I2C Addresses for projector control are 8 bits, followed by an 8 bit sub-address. The address and/or sub-address are followed by either writing or reading 32 bits of data. The protocols for I2C projector control read and write are listed below.

Write Command:

Address (8-bit)	Sub-Address (8-bit)	Data (32-bit)	
0x36	0xAA	DDDDDDDDh	(AAh = Register Address, DDDDDDDDh = write data)

Read Command:

(8-bit)	(8-bit)	(8-bit)	
0x36	0x15	xxh (address of reg.)	Read Part 1 (Write address of requested register)
(8-bit)		(32-bit)	
0x37		XXXXXXXXh	Read Part 2 (Read data of requested register)

4.1.2 Slave Receive Mode (Write)

With the Pico-Projector is operating in the slave-receiver configuration, the first byte following the start condition is the Pico-Projector device write address (ex. 36h). The interface consists of a number of sub-address registers each capable of accepting multiple bytes of data. Each command/sub-address expects a certain number of data bytes, typically 4. The number of data bytes for each command/sub-address is described in Section 4.1.5.

Writing to registers is performed with a single series of bus transactions, preceded by exactly one start condition (S) and terminated by exactly one stop condition (P). All register write transactions shall include one byte for the sub-address and 4 bytes for data. The following string of characters represents each byte or condition on the bus which makes up a register write transaction:

An example of register writing to device address 0x36, sub-address 0x04 with data 0x00000000 would be as follows:
S 36 04 00 00 00 00 P

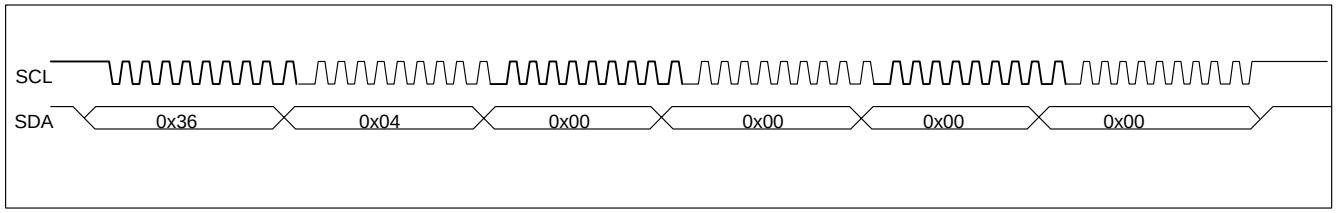


Figure 1 - I2C Interface Write Register

4.1.3 Slave Transmit Mode (Read)

With the Pico-Projector operating in the slave-transmitter mode, the first byte following the start condition is Pico-Projector device read address (37h). The selected register to read must be specified with a write previously.

Reading from registers is accomplished with a two step process of writing to a specific sub-address, then reading 4 bytes on a subsequent transaction. This sub-address is 0x15. A full two step read transaction would follow this format:

For the specific example of reading from register 0x04 that has data 0x00000000, the bus data would be:

S 36 15 04 P
S 37 00 00 00 00 P

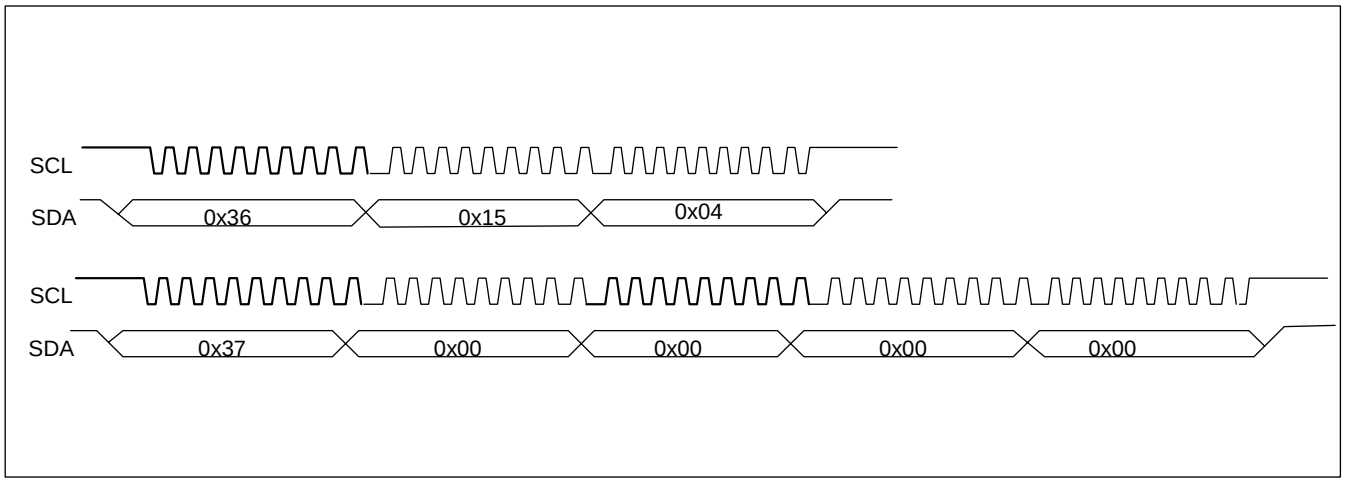


Figure 2 - I2C Interface Read Register

4.1.4 Reserved Areas

When writing to valid registers, all unused/reserved bits should be set to zero unless specified otherwise. Reserved registers should never be written to. When reading valid registers, all unused/reserved bits should be ignored.

4.1.5 I2C Projector Control Commands

The following shows the support Configuration Registers and the Control Commands. In the Type column 'wr' type is writeable. Data can also be read back through the I2C interface for 'wr' type bits. 'r' type is read-only. Writes to these fields will have no effect. 's' type is a latched status bit. Reading a '1' in this field means that the signal has gone high since the last clear. Writing a '1' to this field clears the status bit.

The "Reset" column in all of the following command tables is the default value in the command register immediately after power-up. These values may be overwritten soon after power-up. When writing to valid registers, all unused/RESERVED bits should be set to zero unless specified otherwise. RESERVED registers should never be written to.

4.1.5.1 Input Source and Interface Mode: (I2C: 0x04, CPU Command code: 0x8004)

When a command 0x04 is received by the projector, the 32 bits of data define the projector input image mode.

Bit(s)	Description	Reset	Type
2:0	Select the input source and interface mode: 0 - Parallel RGB I/F 1 - Internal Test Patterns 2 - Splash screen - *Note* (**1**) 3 - CPU I/F - *Note*(**1**) 4 – BT.656 - *Note* (**1**) 5+ - RESERVED	d0	wr
15: 3	Spare	x0000	
31:16	Unused		

Note

(1) Not supported at the Kit level

Further clarification on the above 2 options:

0: Parallel interface is in RGB mode

1: Internal test patterns uses command 0x0B to define the test pattern internal source

I2C Command Format Example:

I2C Address	I2C Sub-Address code	Data (32-bits)
0x36	0x04	DDDDDDDDh

4.1.5.2 Pixel Format: (I2C: 0x06, CPU Command code: 0x8006)

Bit(s)	Description	Reset	Type
2:0	Select the pixel format: 0 - RGB565 - *Note* (**2**) 1 - RGB666 - *Note* (**2**) 2 - RGB888 - *Note* (**1**) 3+ - RESERVED	d2	wr
15: 3	Spare	x0000	
31:16	Unused		

Note

(1) RGB888 is for the Parallel interface only

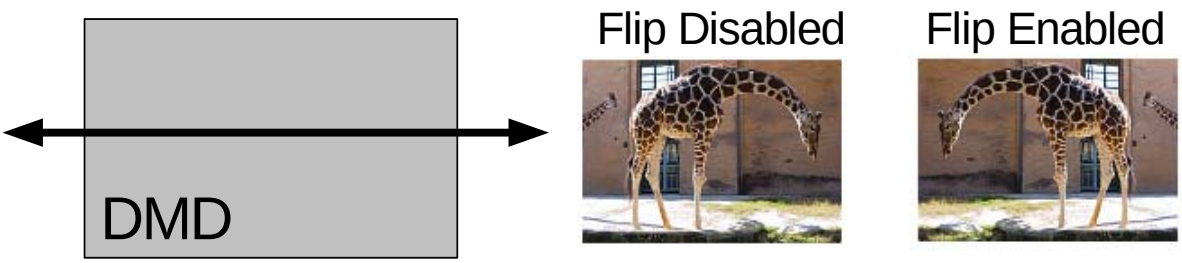
(2) Not supported at the Kit level

4.1.5.3 Image Flip Long Axis: (I2C: 0x08, CPU Command code: 0x8008)

When this command is received by the projector, the data defines if the input image is flipped across the long axis of the DMD.

Bit(s)	Description	Reset	Type
0	Flips image along long Axis on DMD: 0 - Disable flip 1 - Enable flip	d1	wr
15: 1	Spare	x0000	
31:16	Unused		

Long axis flip means this:

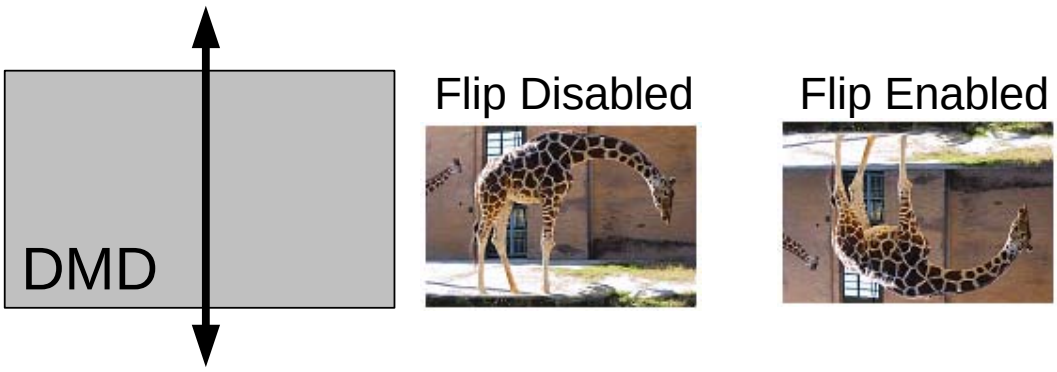


4.1.5.4 Image Flip Short Axis: (I2C: 0x09, CPU Command code: 0x8009)

When this command is received by the projector, the data defines if the input image is flipped across the short axis of the DMD.

Bit(s)	Description	Reset	Type
0	Flips image along short Axis on DMD: 0 - Disable flip 1 - Enable flip	d1	wr
15: 1	Spare	x0000	
31:16	Unused		

Short axis flip means this:



4.1.5.5 Internal Test Patterns: (I2C: 0x0B, CPU Command code: 0x800B)

Bit(s)	Description	Reset	Type
3:0	Test pattern select: 0x0 - Checkerboard 0x1 - Solid black 0x2 - Solid white 0x3 - Solid red 0x4 - Solid blue 0x5 - Solid green 0x6 - Vertical lines - 1-white, 7-black 0x7 - Horizontal lines - 1-white, 7-black 0x8 - Vertical lines - 1-white, 1-black 0x9 - Horizontal lines - 1-white, 1-black 0xA - Diagonal lines 0xB - Vertical Gray Ramps 0xC - Horizontal Gray Ramps 0xD - 8x8 grid w/ border (1 pixel wide) 0xE - 16x16 grid w/ border (1 pixel wide) 0xF - 32x32 grid w/ border (1 pixel wide)	d0	wr
15: 4	Spare	x000	
31:16	Unused		

For typical test pattern usage, these command settings should be used:

Input Source and Interface Mode: (I2C: 0x04, CPU Command code: 0x8004)

- **0x1 - Internal Test Patterns**

Pixel Format: (I2C: 0x06, CPU Command code: 0x8006)

- **0x2 - RGB888**

4.1.5.6 Parallel Interface Clock Edge: (I2C: 0x0C, CPU Command code: 0x800C)

Bit(s)	Description	Reset	Type
0	Defines the clock edge (for PCLK) on which pixel data is sampled: 0 - Sample on falling edge 1 - Sample on rising edge	d1	wr
15: 1	Spare	x0000	
31:16	Unused		

4.1.5.7 Parallel Interface Sync Polarity: (I2C: 0x0D, CPU Command code: 0x800D)

Bit(s)	Description	Reset	Type
0	Defines the polarity of the incoming VSYNC signal: 0 – Active low pulse 1 – Active high pulse	d0	wr
1	Defines the polarity of the incoming HSYNC signal: 0 – Active low pulse 1 – Active high pulse	d0	wr
2	Defines the polarity of the incoming DATEN signal: 0 – Active low pulse 1 – Active high pulse	d1	wr
15: 3	Spare	x0000	
31:16	Unused		

4.1.5.8 Red LED Driver Current: (I2C: 0x0E, CPU Command code: 0x800E)

Bit(s)	Description	Reset	Type
9:0	PWM duty cycle Valid range is 0x000 (0% duty cycle) to 0x3ff (100% duty cycle)	d236	wr
15:10	Spare	x00	
31:16	Unused		

Red current is applied according to: ILED(mA) = 70 + 0.74 * (1023 - PWM)

The recommended current range supported by the LED Driver is 100mA to 650mA.

When this command is received by the projector, the data defines a PWM value that controls the red LED Driver current. The resolution is 10 bits and corresponds to a percentage of the driver current. The current value can be set from 23% to 100% in 1/1024 steps. For the LED Driver a max value of 0x3ff gives the minimum current setting.

4.1.5.9 Green LED Driver Current: (I2C: 0x0F, CPU Command code: 0x800F)

Bit(s)	Description	Reset	Type
9:0	PWM duty cycle Valid range is 0x000 (0% duty cycle) to 0x3ff (100% duty cycle)	d236	wr
15:10	Spare	x00	
31:16	Unused		

Green current is applied according to: ILED(mA) = 70 + 0.74 * (1023 - PWM)

The recommended current range supported by the LED Driver is 100mA to 650mA.

4.1.5.10 Blue LED Driver Current: (I2C: 0x10, CPU Command code: 0x8010)

Bit(s)	Description	Reset	Type
9:0	PWM duty cycle Valid range is 0x000 (0% duty cycle) to 0x3ff (100% duty cycle)	d236	wr
15:10	Spare	x00	
31:16	Unused		

Blue current is applied according to: ILED(mA) = 70 + 0.74 * (1023 - PWM)

The recommended current range supported by the LED Driver is 100mA to 650mA.

4.1.5.11 Enable Red LED: (I2C: 0x11, CPU Command code: 0x8011)

When this command is received by the projector, the data defines if the Red LED is enabled.

Bit(s)	Description	Reset	Type	Notes
0	Enable Red LED: 0 - disable LED 1 - enable LED	d1	wr	
15: 1	Spare	x0000		
31:16	Unused			

4.1.5.12 Enable Green LED: (I2C: 0x12, CPU Command code: 0x8012)

Bit(s)	Description	Reset	Type	Notes
0	Enable Green LED: 0 - disable LED 1 - enable LED	d1	wr	
15: 1	Spare	x0000		
31:16	Unused			

4.1.5.13 Enable Blue LED: (I2C: 0x13, CPU Command code: 0x8013)

Bit(s)	Description	Reset	Type	Notes
0	Enable Blue LED: 0 - disable LED 1 - enable LED	d1	wr	
15: 1	Spare	x0000		
31:16	Unused			

4.1.5.14 Degamma Curve Select: (I2C: 0x1E, CPU Command code: 0x801E)

When this command is received by the projector, the data defines the degamma curve selected. If the degamma curve select command is not issued, then the projector uses the default curve.

Bit(s)	Description	Reset	Type	Notes
3:0	Degamma curve select: 0x0 - Degamma curve #1 0x1 - Degamma curve #2 0x2 - Degamma curve #3 0x3 - Degamma curve #4 0x4 to 0xF - RESERVED	d0	wr	
15: 4	Spare	x000		
31:16	Unused			

TI provides four pre-programmed degamma curves in Flash as selected by bits 3:0:

0x0 – Enhanced Graphics (TI default, an s-curve) – recommended

0x1 – Power Law 2.2 (NTSC and also almost identical to sRGB except for very dark shades of colors)

0x2 – Power Law 2.5 (NTSC-like but tends to look better on projectors than Power Law 2.2)

0x3 – Linear (for lab test use only)

4.1.5.15 Mode Select: (I2C: 0x1F, CPU Command code: 0x801F)

When this command is received by the projector, the data defines the mode selected.

Bit(s)	Description	Reset	Type	Notes
3:0	Mode select: 0x0 – 60Hz Mode 0x1 – RESERVED 0x2 – RESERVED 0x3 – RESERVED 0x4 – RESERVED 0x5 – RESERVED 0x6 – RESERVED 0x7 – 50Hz Mode – *Note* (**1**) 0x8 to 0xF - RESERVED	d0	wr	
15: 4	Spare	x000		
31:16	Unused			

Note

(1) 50Hz Mode for PAL/SECAM support.

4.1.5.16 Sync Mode: (I2C: 0x24, CPU Command code: 0x8024)

When this command is received by the projector, the synchronization method is selected.

Bit(s)	Description	Reset	Type	Notes
0	Sync Mode 0 - Lock to internally generated sync 1 - Lock to incoming sync (frequency of the input source is 60Hz or 50Hz)	d0	wr	
3: 1	Spare	b000		
31:4	Unused			

The only valid image inputs for using "Lock to incoming sync" mode are:

1. Parallel I/F for frame rates of 50-60Hz and input frames are periodic
2. NTSC inputs from the TVP5150 video decoder (periodic at 60Hz)
3. PAL/SECAM inputs from the TVP5150 video decoder (periodic at 50Hz)
4. Internal Test Patterns when an external VSYNC is being input that is periodic and within 50-60Hz

If selecting lock to incoming sync mode, but the source is not a valid image input, the LEDs may turn off due to a watchdog timer inside used to protect the LEDs. Also, image artifacts may occur if the LEDs do not turn off.

"Lock to internally generated sync" mode must be selected in these cases:

1. Parallel I/F for frame rates <50Hz
2. Parallel I/F for frame rates that are not periodic
3. Internal Test Patterns (unless an external VSYNC is being input that is periodic and within 50-60Hz)

4.1.5.17 Temporal Enhance Enable: (I2C: 0x26, CPU Command code: 0x8026)

When this command is received by the projector, temporal Enhance is turned on or off. Temporal Enhance should be disabled for any non-periodic source or any periodic source with a frame rate slower than 50Hz. Otherwise temporal Enhance should be enabled to improve image quality.

Bit(s)	Description	Reset	Type	Notes
0	Temporal Enhance Enable – *Note* (**1**) 0 – Disabled 1 – Enabled	d0	wr	
3: 1	Spare	b000		
31:4	Unused			

Note

(1) Temporal Enhance Enable should be used in video mode to improve image quality.

4.1.5.18 Firmware Revision: (I2C: 0x40, CPU Command code: N/A)

Bit(s)	Description	Reset	Type	Notes
11:0	DDP1501 firmware revision (Read-only)	d536	r	
31:12	Unused			

5 Command Quick Reference

The following table provides a quick reference summary of all available projector commands.

I2C Addr	Register	Size	Type	Default Value	Default Action (Video mode)
x04	Input Source and Interface Mode	16	WR	0x0	0 - Parallel RGB I/F
x05	* RESERVED				
x06	Pixel Format	16	WR	0x2	RGB888
x07	* RESERVED				
x08	Image Flip Long Axis	16	WR	0x1	Enabled
x09	Image Flip Short Axis	16	WR	0x1	Enabled
x0B	Internal Test Patterns	16	WR	0x0	Checkerboard
x0C	Parallel Interface Clock Edge	16	WR	0x1	Rising edge
x0D	Parallel Interface Sync Polarity	16	WR	0x4	VSYNC-low, HSYNC-low, DATEN-high
x0E	Red LED Driver Current	16	WR	0x0EC	Max current
x0F	Green LED Driver Current	16	WR	0x0EC	Max current
x10	Red LED Driver Current	16	WR	0x0EC	Max current
x11	Enable Red LED	16	WR	0x1	Enabled
x12	Enable Green LED	16	WR	0x1	Enabled
x13	Enable Blue LED	16	WR	0x1	Enabled
x14-x1D	* RESERVED				
x1E	Degamma Curve Select	16	WR	0x0	Enhanced Gr.
x1F	Mode Select	16	WR	0x0	60Hz Mode
x21-x23	* RESERVED				
x24	Sync Mode	4	WR	0x0	Lock to internally generated sync
X25	* RESERVED				
x26	Temporal Enhance Enable	4	WR	0x0	Disabled
x27	* RESERVED				
x28-x3F	* RESERVED				
x40	Firmware Revision	12	R	536	n/a
x41-xFF	* RESERVED				

Note

* RESERVED registers should never be written to.
'WR' type is writeable and data is also readable.
'R' type is read-only. Writes to these fields will have no effect.

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