PEB-2739I Series

Embedded System Board

User's Manual

Version 1.0

Table of Contents

How to Use This Manual

How to Use This Manual

The manual describes how to configure your PEB-2739I to meet various operating requirements.   It is divided into five chapters, with each chapter addressing a basic concept and operation of Single Board Computer.

Chapter 1 : System Overview. Presents what you have in the box and give you an overview of the product specifications and basic computer architecture.

Chapter 2 : Hardware Configuration. Shows the definitions and locations of Jumpers and Connectors that you can easily configure your embedded board.

Chapter 3 : System Installation.   Describes how to properly mount the CPU, main memory and Compact Flash to get a safe installation and provides a programming guide of Watch Dog Timer function.

Chapter 4 : BIOS Setup Information. Specifies the meaning of each setup parameters, how to get advanced BIOS performance and update new BIOS. In addition, POST checkpoint list will give users some guidelines of trouble-shooting.

Chapter 5 : Troubleshooting. Provides various useful tips to quickly get PEB-2739I running with success. As basic hardware installation has been addressed in Chapter 3, this chapter will basically focus on system integration issues, in terms of backplane setup, BIOS setting, and OS diagnostics.

The content of this manual is subject to change without prior notice.   These changes will be incorporated in new editions of the document. **Portwell** may make supplement or change in the products described in this document at any time.

Updates to this manual, technical clarification, and answers to frequently asked questions will be shown on the following web site: http://www.portwell.com.tw/.

Chapter 1
System Overview

1.1 Introduction

Portwell Inc., a world-leading innovator in the Industrial PC (IPC) market and a member of the Intel® Embedded and Communications Alliance (Intel ECA), announced today the Portwell PEB-2739I utilizing the Intel® ECX form factor based on the Intel® Atom™ processor Z500PT series and the Intel® System Controller Hub US15WPT. The new micro-architecture of the Intel® platform will provide a range of low power, wide temperature and fanless devices such as Panel PC, Kiosk, DS, Medical, Military, Government and Industrial automation and control applications.

PEB-2739I is specifically designed to operate at a very low power consumption of less than 10 watts at full loading. It supports dual independent display by LVDS and SDVO daughter card (DVI/VGA/LVDS, by request).

Based on the Intel® Atom™ processor Z500PT series platform, the PEB-2739I takes advantage of the processor's very low power consumption, Ground-breaking power management techniques and wide temperature so it can be a truly industrial temperature and fanless configuration. In addition, the PEB-2739I supports DC 12V input, one SO-DIMM memory slot for DDR2 SDRAM up to 2GB, and comes with one SATA, one CompactFlash® socket, one SDVO connector (with one PCIE x1 and USB signal), one gigabit Ethernet, two RS232, six USB2.0 and one SDIO connector.

PEB-2739I features:

- Intel® Atom™ processor Z500PT series and System Controller Hub US15WPT

- One 200-pin SO-DIMM support DDR2 SDRAM up to 2GB

- Dual independent display: SDVO(by VGA/DVI/LVDS daughter card) and 24bit LVDS

- One Gigabit Ethernet

- TPM (Trusted Platform Module) could be added on board (optional)

- Customization (Extension card): BTB connector with SDVO/USB/PCI-E x1 signal and SDIO pin header

- Storage: One SATA / One CompactFlash / One USB Flash / One SDIO

- 12V DC input

1.2 Check List

The PEB-2739I package should include the following items:

- One PEB-2739I embedded system board
- One 2-in-1 Heatsink
- One SATA Cable
- One Installation Resources CD Title

If any of these items is damaged or missing, please contact your vendor and keep all packing materials for future replacement and maintain.

1.3 Product Specification

- **CPU**
  On board Intel® Atom™ Z510PT (1.1GHz) / Z520PT (1.33GHz) processor
  CPU clock bus: Z520PT: 533MHz / Z510PT:400MHz
- **Chipset**
  Intel® System Controller Hub US15WPT
- **System BIOS**
  AMI BIOS
- **Main Memory**
  One 200-pin DDR2 SODIMM socket supports up to 2GB dual channel 400/533MHz memory
- **Serial Port**
  Support one RS-232 and one RS-232/422/485 selectable
- **USB Interface**
  Support six USB (Universal Serial Bus) ports, four on rear I/O and two on board header for internal devices. USB port6, 7 can support USB 2.0 only base on Intel specification.
- **Client USB**
  Support one Client USB on board edge
- **Audio Interface**
  Connector for Mic-In and Line-Out
- **Keyboard and PS/2 Mouse interface**
  Support one PS/2 header for keyboard and mouse
- **Watch Dog Timer**
  Support WDT function through software programming for enable/disable and interval setting
  General system reset
- **On Board VGA**
  Intel® System Controller Hub US15WPT integrated GMA 500 Graphic device
- **On-board Ethernet**
  One Gigabit Ethernet (10/100/1000 Mbits/sec) LAN ports using Intel PCI-Expressx1interface GbE Ethernet Controller **(82574IT)**

- On Board I/O
  - Rear I/O
    ・Line-Out
    ・MIC-In
    ・Four USB ports
    ・One DB-9 support RS-232/422/485
    ・Fast Ethernet port (RJ45)
    ・12V DC Jack
  - Internal I/O
    ・One SATA connector(with Power)
    ・One Type II CompactFlash socket
    ・One LVDS port
    ・One SDVO port (BTB connector with SDVO/USB/PCI-E x1 signal)
    ・One SDIO port (2x8-pin, 2mm-pitch box header)
    ・One RS-232 port (2x5-pin, 2mm-pitch box header)
    ・Two USB 2.0 ports (2x5-pin, 2mm-pitch header)
    ・One Client USB connector
    ・One 3-pin power connector for system fan
    ・One power output port
    ・Power on/off LED, Hard drive activity LED and system Reset switch headers
    ・On-board programmable 8-bit Digital I/O interface
- **System Monitoring Feature**
  Monitor system temperature and major power sources.
- **Outline Dimension (L X W):**
  146mm X 105mm

● **Power requirements**

System Configuration	
CPU Type	Intel® Atom™ CPU Z510PT@1.10GHz FSB:400MHz L2:512K
SBC BIOS	Portwell,Inc.PEB-2739I BIOS Rev.:R1.00.E2(09232009)
Memory	Transcend DDR2-533 1GB(SamSung K4T51083QE)
VGA Card	Onboard Intel Corporation US15WPT Embedded Graphics Chipset Function
VGA Driver	Intel Corporation US15WPT Embedded Graphics Chipset Ver:10.1.0.1390
LAN Card	Onboard Intel 82574IT Gigabit Chipset
LAN Driver	Intel® 82574IT Gigabit Network Connection Ver:10.6.15.0
Audio Card	Onboard Realtek ALC662 Audio Chipset
Audio Driver	Realtek High Definition Audio Ver:6.0.1.5680
Chip Driver	Intel® Chipset Device Software Ver:8.8.0.1011
USB 2.0 Driver	Intel® SCH Family USB2 Enhanced Host Controller Ver:8.8.0.1001
IDE HDD	WD WD1200BEVE 120GB 2.5″
Compact Flash	Transcend Ultra DMA 1GB(TS1GCF45IF-A5)
USB-CDROM	ASUS CB-52164 DVD-ROM
Power Supply	Seasonic SSA-0651-1

Programs for loading both CPU & VGA: Run Burning Test V5.3
RUN time: 10 / 30 Minutes.

Item	Power ON	Full Loading 10Min	Full Loading 30Min
DC 12V	0.6A	0.88A	0.89A
USB Loading Test	4.73 V/ 510 mA		

● Operating Temperature:
  -40°C ~ 80°C
● Storage Temperature:
  -40°C ~ 80°C
● Relative Humidity:
  5% ~ 90%, non-condensing

1.3.1   Mechanical Drawing
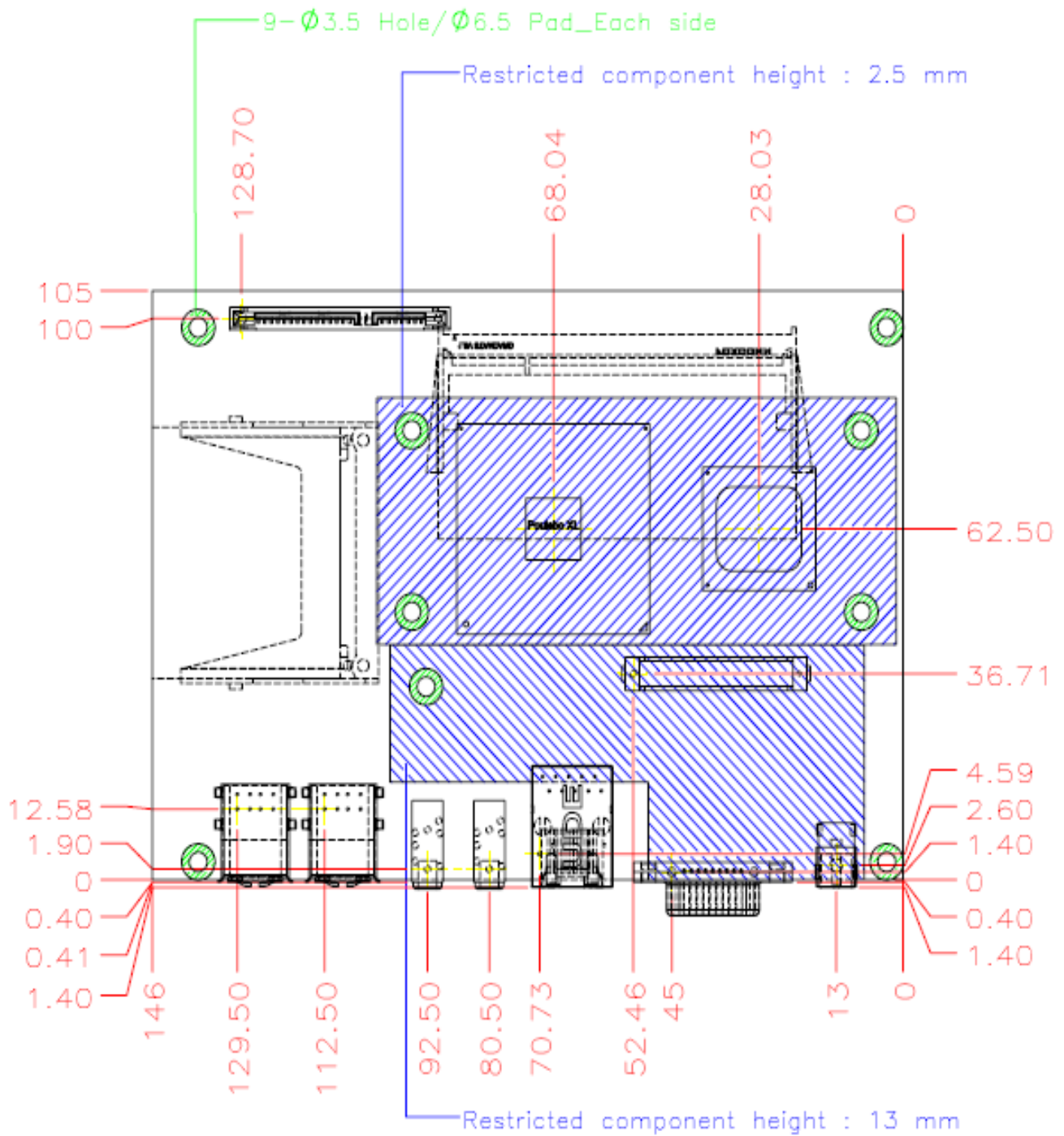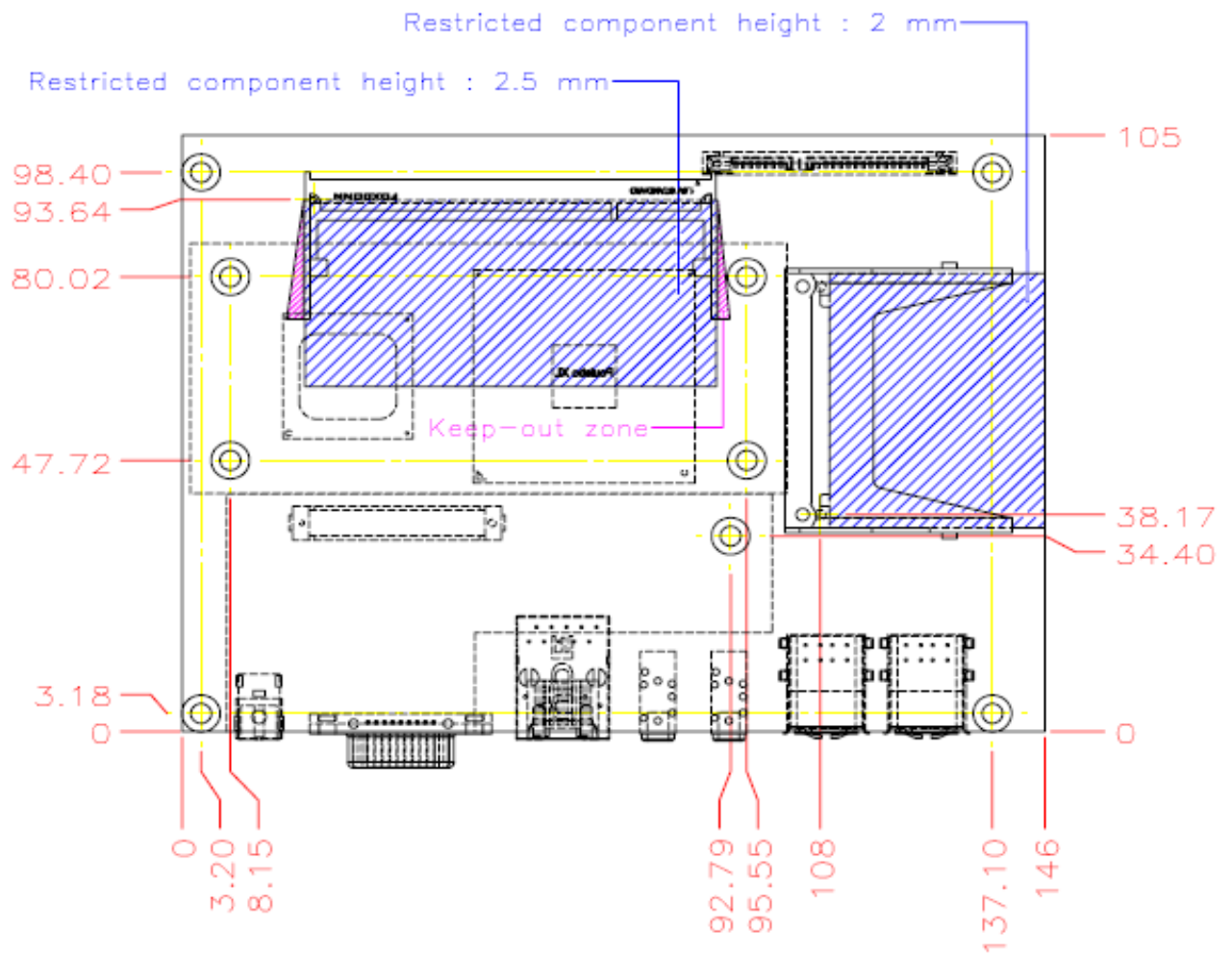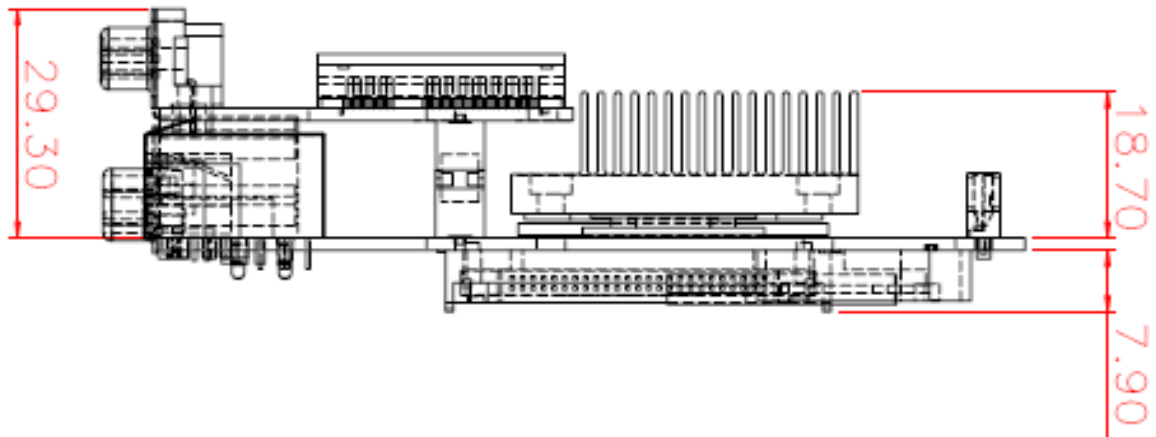
1.4   System Architecture

All of details operating relations are shown in PEB-2739I System Block Diagram.

Block Diagram
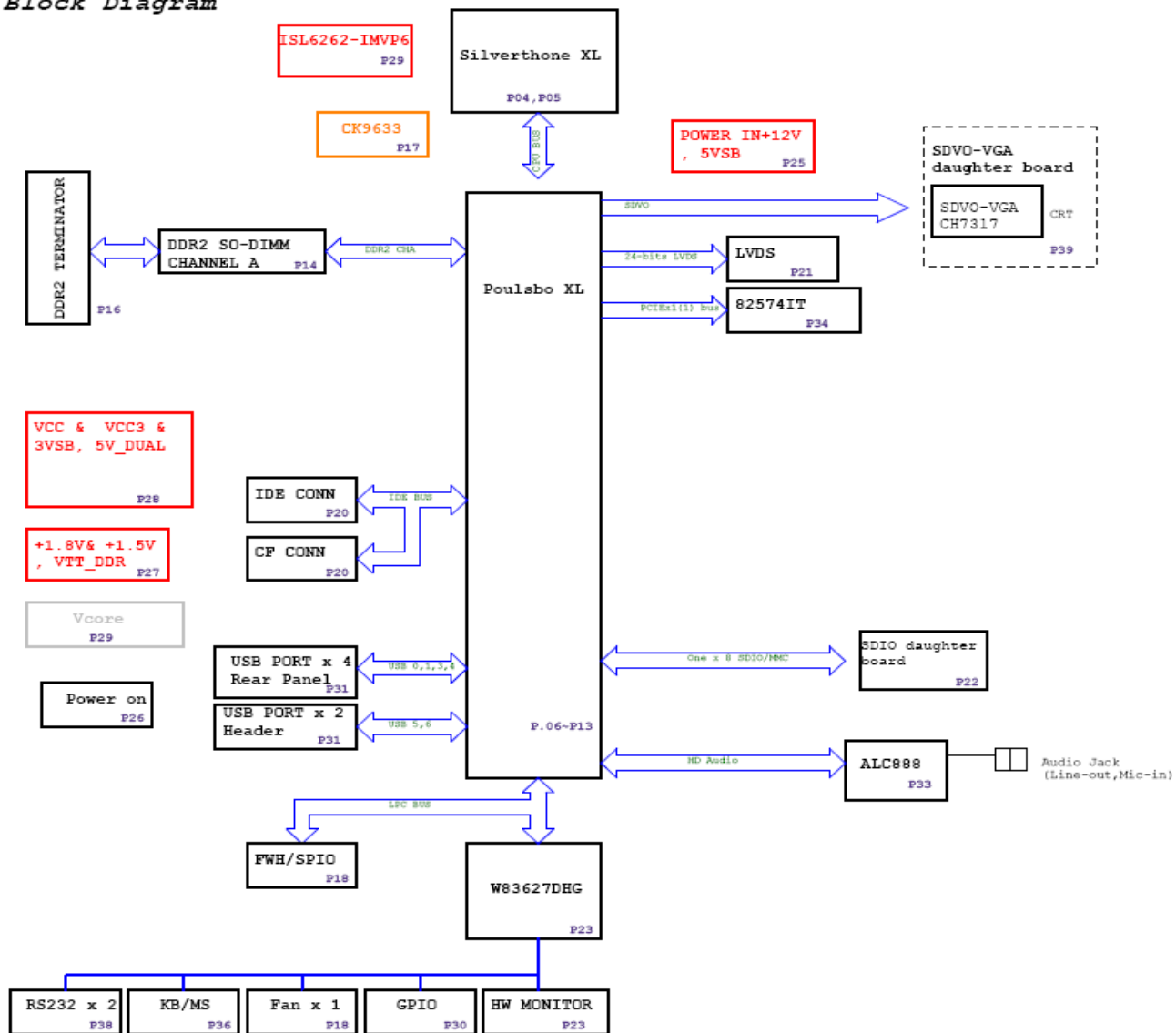
PEB-2739I Block Diagram

Chapter 2
Hardware Configuration

This chapter gives the definitions and shows the positions of jumpers, headers and connector. All of the configuration jumpers on PEB-2739I are in the proper position. The default settings are indicated with a star sign (★).

2.1   Jumper Setting

For users to customize PEB-2739I's features. In the following sections, **Short** means covering a jumper cap over jumper pins; **Open** or **N/C** (Not Connected) means removing a jumper cap from jumper pins. Users can refer to Figure 2-1 for the Jumper and Connector locations.
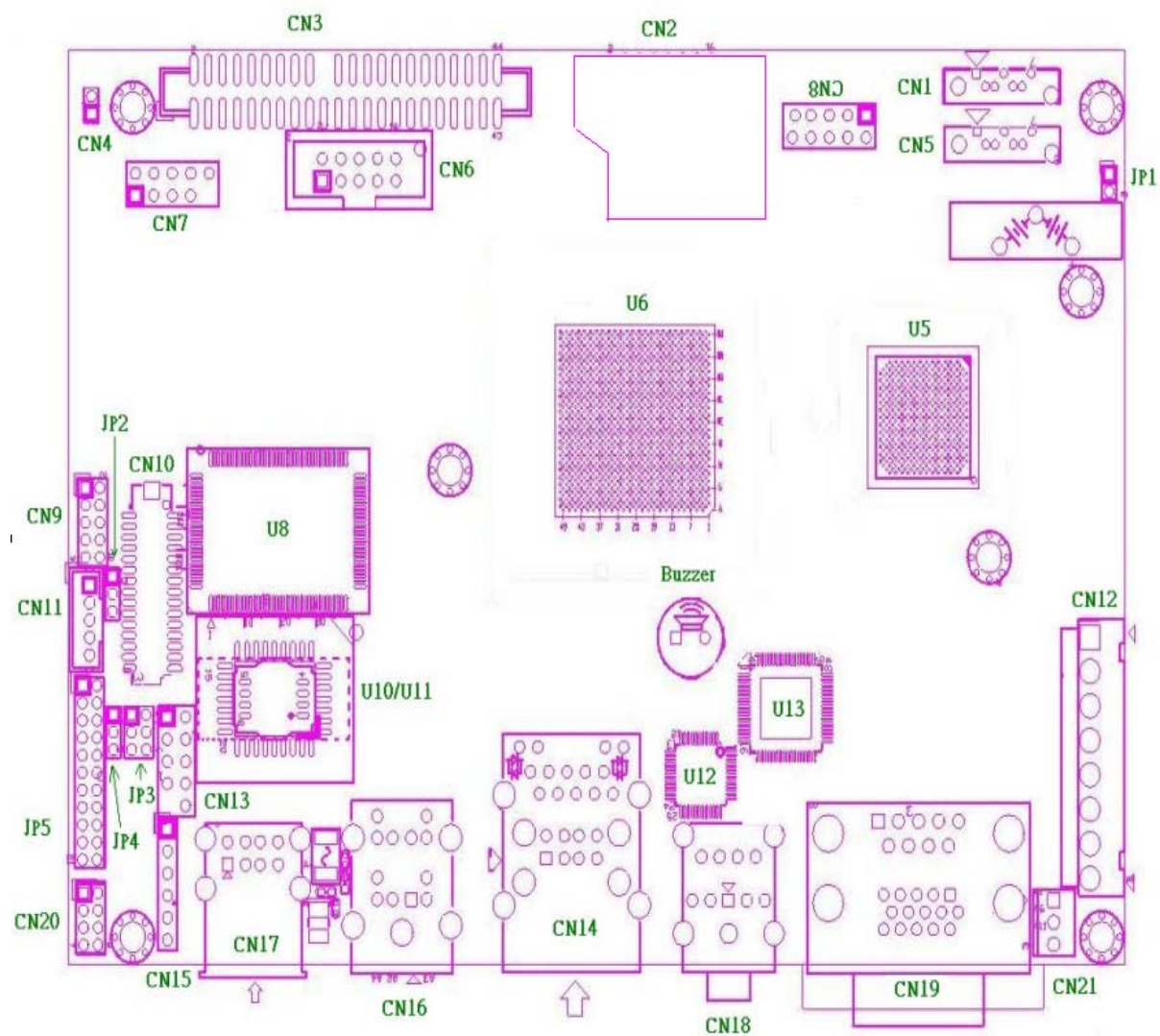
PEB-2739I   Jumper and Connector Locations (Top)

JP1 : Clear CMOS

JP1	Function
Open	Normal operation ★
Short	Clear CMOS

JP2 : 5V / 3.3V Panel power selection

JP2	Function
1-2 Short	3.3V
2-3 Short	5V ★

JP3 : Microcontroller programming

JP3	Function
1-2, 3-4, 5-6 Short	Normal operation ★
1-2, 3-4, 5-6 Open	Programming microcontroller

JP4 : 5V / 3.3V backlight enable pin power level selection

JP4	Function
1-2 Short	3.3V
2-3 Short	5V ★

JP5 : Serial port 2 function selection

JP5	Function
5-6, 9-11, 10-12, 15-17, 16-18 Short	RS-232 ★
3-4, 7-9, 8-10, 13-15, 14-16, 21-22 Short	RS-422
1-2, 7-9, 8-10, 19-20 Short	RS-485

2.2   Connector Allocation

I/O peripheral devices are connected to the interface connectors.

Connector Function List

Connector	Function	Remark
CN1	SATA port 1	
CN2	SDIO Port **(Support SD 1.1 and MMC 4.0 only)**	
CN3	PATA 44-Pin (IDE)	
CN4	Temperature Sense	
CN5	SATA port 2	
CN6	Serial port 2	
CN7	USB port 6,7	
CN8	USB port 0,2	
CN9	8 bit GPIO	
CN10	Single channel LVDS panel interface	
CN11	Panel backlight inverter's power	

CN12	ATX power source	
CN13	LPC Debug Port	
CN14	Giga Ethernet with USB port 1,3	
CN15	Microcontroller programmer	
CN16	PS/2 Keyboard & Mouse	
CN17	USB port 4,5	
CN18	Audio port (Stereo line output, microphone input)	
CN19	CRT with serial port 1	
CN20	Front Panel	
CN21	FAN	
CN22	DDR2 SO-DIMM 200Pin	
CN23	Compact flash	

Pin Assignments of Connectors

CN1 : SATA Port 1

Pin No.	Signal Description
1	GND
2	SATATX+
3	SATATX-
4	GND
5	SATARX+
6	SATARX-
7	GND

CN2 : SDIO Connector

Pin No.	Signal Description	Pin No.	Signal Description
1	SDIO_DATA0	2	+3.3V
3	SDIO_DATA1	4	SDIO_CLK
5	SDIO_DATA2	6	SDIO_CMD
7	SDIO_DATA3	8	+3.3V
9	SDIO_DATA4	10	GND
11	SDIO_DATA5	12	SDIO_CD#
13	SDIO_DATA6	14	SDIO_WP
15	SDIO_DATA7	16	GND

CN3 : Hard Disk 44-pin Connector

Pin No.	Signal Description	Pin No.	Signal Description
1	R_PLT_RST#	2	GND
3	PDD7	4	PDD8
5	PDD6	6	PDD9
7	PDD5	8	PDD10
9	PDD4	10	PDD11

11	PDD3	12	PDD12
13	PDD2	14	PDD13
15	PDD1	16	PDD14
17	PDD0	18	PDD15
19	GND	20	N/C
21	PDDREQ	22	GND
23	PDIOW#	24	GND
25	PDIOR#	26	GND
27	PDIORDY	28	GND
29	PDDACK#	30	GND
31	IRQ14#	32	N/C
33	PDA1	34	GND
35	PDA0	36	PDA2
37	PDCS1#	38	PDCS3#
39	IDEACT#	40	GND
41	+5V	42	+5V
43	GND	44	N/C

CN4 : Temperature Sense

Pin No.	Signal Description
1	Thermal resister 10K+
2	Analog ground

CN5 : SATA Port 2

Pin No.	Signal Description
1	GND
2	SATATX+
3	SATATX-
4	GND
5	SATARX+
6	SATARX-
7	GND

CN6 : Serial port 2 Connector

Pin No.	Signal Description	Pin No.	Signal Description
1	DCD1#	2	RXD1#
3	TXD1#	4	DTR1#
5	GND	6	DSR1#
7	RTS1#	8	CTS1#
9	RI1#	10	N/C

CN7 : USB Port6&Port7 Header

Pin No.	Signal Description	Pin No.	Signal Description
1	+5V	2	+5V
3	USBD6-	4	USBD7-
5	USBD6+	6	USBD7+
7	GND	8	GND
9	N/C		

CN8 : USB Port0&Port2 Header

Pin No.	Signal Description	Pin No.	Signal Description
1	+5V	2	+5V
3	USBD0-	4	USBD2-
5	USBD0+	6	USBD2+
7	GND	8	GND
9	N/C		

CN9 : 8 bit GPIO Header

Pin No.	Signal Description	Pin No.	Signal Description
1	LPC_GP10	2	LPC_GP14
3	LPC_GP11	4	LPC_GP15
5	LPC_GP12	6	LPC_GP16
7	LPC_GP13	8	LPC_GP17
9	GND	10	+5V

CN10 : LVDS Panel Interface Connector

Pin No.	Signal Description	Pin No.	Signal Description
1	LVDSA_DATA0+	2	LVDSA_DATA0-
3	LVDSA_DATA1+	4	LVDSA_DATA1-
5	LVDSA_DATA2+	6	LVDSA_DATA2-
7	LVDSA_DATA3+	8	LVDSA_DATA3-
9	LVDSA_CLK+	10	LVDSA_CLK-
11	N/C	12	N/C
13	N/C	14	N/C
15	N/C	16	N/C
17	N/C	18	N/C
19	N/C	20	N/C
21	LVDS_I2C_DATA	22	LVDS_I2C_CLK
23	GND	24	BACKLIGHT_CTL
25	GND	26	GND
27	VDD_LVDS	28	VDD_LVDS
29	N/C	30	VDD_LVDS

CN11 : LVDS Panel Back Light Inverter Power Connector

Pin No.	Signal Description
1	+5V
2	GND
3	+12V
4	GND
5	BACKLIGH_ENABLE

CN12 : Power Connector

Pin No.	Signal Description
1	+5V
2	+5V
3	+5V Standby
4	+12V
5	PS_ON#
6	GND
7	GND
8	GND

CN13 : LPC Debug Port Header

Pin No.	Signal Description	Pin No.	Signal Description
1	LAD0	2	+3.3V
3	LAD1	4	PLT_RST#
5	LAD2	6	LFRAME#
7	LAD3	8	LPC_PCID
9	N/C	10	GND

CN14 : Giga Ethernet RJ45 with 2 port USB Jack

Pin No.	Signal Description	Pin No.	Signal Description
1	LAN 0+	2	LAN 0-
3	LAN 1+	4	LAN 2+
5	LAN 2-	6	LAN 1-
7	LAN 3+	8	LAN 3-
9	+5V	10	+5V
11	USBD1-	12	USBD3-
13	USBD1+	14	USBD3+
15	GND	16	GND

CN15 : Microcontroller programmer Header

Pin No.	Signal Description
1	Vpp
2	+3.3V
3	GND
4	I2C_DATA
5	I2C_CLK
6	N/C

CN16 : PS/2 Keyboard/Mouse

Pin No.	Signal Description	Pin No.	Signal Description
B1	KB_DATA	T1	MS_DATA
B2	N/C	T2	N/C
B3	GND	T3	GND
B4	+5V	T4	+5V
B5	KB_CLK	T5	MS_CLK
B6	N/C	T6	N/C

CN17 : USB Port4&Port5 Jack

Pin No.	Signal Description	Pin No.	Signal Description
T1	+5V	B1	+5V
T2	USBD5-	B2	USBD4-
T3	USBD5+	B3	USBD4+
T4	GND	B4	GND

CN18 : Audio Jack

Pin No.	Signal Description
Top	Stereo line out
Bottom	Microphone input

CN19 : CRT with Serial port 1 Connector (DB15+DB9)

Pin No.	Signal Description	Pin No.	Signal Description
B1	RED	B2	GREEN
B3	BLUE	B4	MON2PU
B5	GND	B6	GND
B7	GND	B8	GND
B9	N/C	B10	GND
B11	MONOPU	B12	5VDDCDA
B13	HSYNC	B14	VSYNC
B15	RED		
T1	DCD2#	T2	RXD2#
T3	TXD2#	T4	DTR2#
T5	GND	T6	DSR2#
T7	RTS2#	T8	CTS2#
T9	RI2#		

CN20 : Front Panel Header

Pin No.	Signal Description	Pin No.	Signal Description
1	SUS_LED	2	5V_Dual
3	HDD_LED	4	+3.3V
5	GND	6	RESET
7	PWR_ON_SW#	8	GND

CN21 : Fan Connector

Pin No.	Signal Description
1	GND
2	+12V
3	RPM

CN22 : DDR2 SO-DIMM 200Pin Connector

CN23 : Compact Flash connector

Pin No.	Signal Description	Pin No.	Signal Description
1	Ground	26	N/C
2	Data 3	27	Data 11
3	Data 4	28	Data 12
4	Data 5	29	Data 13
5	Data 6	30	Data 14
6	Data 7	31	Data 15
7	HDC CS0#	32	HDC CS1#
8	Ground	33	N/C
9	Ground	34	IOR#

10	Ground	35	IOW#
11	Ground	36	Write Enable(pull-high 4.7k to 5V)
12	Ground	37	IRQ
13	+5V	38	+5V
14	Ground	39	CSEL (pull-low 470 to Gnd)
15	Ground	40	N/C
16	Ground	41	RESET#
17	Ground	42	IORDY
18	HDC SDA2	43	DREQ#
19	HDC SDA1	44	DACK#
20	HDC SDA0	45	HDC ACT#
21	Data 0	46	PDIAG# (Pull-Low 150 ohms)
22	Data 1	47	Data 8
23	Data 2	48	Data 9
24	N/C	49	Data 10
25	N/C	50	Ground

Chapter 3
System Installation

This chapter provides you with instructions to set up your system. The additional information is enclosed to help you set up onboard PCI device and handle Watch Dog Timer (WDT) and operation of GPIO in software programming.

3.1   System Architecture

- Intel® Atom™ Processor Z510PT (512K Cache, 1.10 GHz, 400 MHz FSB)
- Intel® Atom™ Processor Z520PT (512K Cache, 1.33 GHz, 533 MHz FSB)

3.2   System Architecture

PEB-2739I provide 1 x 200pin SO-DIMM sockets which supports 400/533 DDR2-SODIMM as main memory, Non-ECC (Error Checking and Correcting), non-register functions. The maximum memory can be up to 2GB. Memory clock and related settings can be detected by BIOS via SPD interface.

For system compatibility and stability, do not use memory module without brand. Memory configuration can be set to either one double-sided DIMM in one DIMM socket.

Beware of the connection and lock integrity from memory module to socket. Inserting improperly it will affect the system reliability.
Before locking, make sure that all modules have been fully inserted into the card slots.

Note:
To insure the system stability, please do not change any of DRAM parameters in BIOS setup to modify system the performance without acquired technical information.

3.3 System Architecture

To install your PEB-2739I into standard chassis or proprietary environment, please perform the following:

Step 1 : Check all jumpers setting on proper position

Step 2 : Install and configure CPU and memory module on right position
Step 3 : Place PEB-2739I into the dedicated position in the system
Step 4 : Attach cables to existing peripheral devices and secure it

WARNING
Please ensure that SBC is properly inserted and fixed by mechanism.

Note:
Please refer to section 3.3.1 to 3.3.7 to install INF/VGA/LAN/Audio drivers.

3.3.1 Mechanical Drawing

PEB-2739I uses state-of-art Intel® Z510 CPU. It's a new chipset that some old operating systems might not be able to recognize. To overcome this compatibility issue, for Windows Operating Systems such as Windows XP/Vista/Win7, please install its INF before any of other Drivers are installed. You can find very easily this chipset component driver in PEB-2739I CD-title.

3.3.2 Intel Integrated Graphics GMCH Chip

PEB-2739I uses Intel GMA500 integrated graphic chipset to gain an outstanding graphic performance. Shared 8 accompany it to 128MB system DDR2-SODIMM with Total Graphics Memory. PEB-2739I supports VGA, LVDS dual display. This combination makes PEB-2739I an excellent piece of multimedia hardware.

With no additional video adaptor, this onboard video will usually be the system display output. By adjusting the BIOS setting to disable on-board VGA, an add-on PCI-Express by 1 VGA card can take over the system display.

Drivers Support
Please find all the drivers in the PEB-2739I CD-title. Drivers support , Windows XP/Vista/Win7.

3.3.3 Intel Gigabit Ethernet Controller

Drivers Support

Please find INTEL 82574IT LAN driver in /Ethernet directory of PEB-2739I CD-title. The drivers support Windows XP/Vista/Win7.

3.3.4 Audio Controller

Please find Intel® High Definition Audio driver form PEB-2739I CD-title. The drivers support Windows XP/Vista/Win7.

3.4 Clear CMOS Operation

The following table indicates how to enable/disable Clear CMOS Function hardware circuit by putting jumpers at proper position.

(JP7)RTC Reset

JP7	Function	JP7
1-2 Short	Normal operation *	1-2 Short
1-2 Open	Clear CMOS	1-2 Open

3.5 WDT Function

The algorithm of the WDT function can be simply described as a timer counting process with an output event. The Time-Out period (Twd) can be set by software commands or hardware jumpers that depend on the board circuit design and may be different among the boards. This timer can be used to monitor a software hang.

PEB-2739I allows users to control WDT by issuing dynamic software commands.The WDT starts counting when it is activated. It will cause a system reset once it expires. Before WDT expires, a refreshing command with a Twd can be issued to re-count WDT and continue the status monitoring. If the system encounters a software or application hang, WDT will generate a system reset after its timeout.

The related Control Registers of WDT are included in the following programming guide that is written in C language. User can write a non-zero value (defined as Twd) into the Time-out Value Register (CR_Twd) to enable WDT. Users can write 0x00 and then Twd to CR_Twd to refresh WDT. To refresh WDT, the time tolerance of refreshing interval must be considered. The smaller of Twd, the more deviation of WDT and you need to include more tolerance. "Let Twd be longer than 2 seconds" is the recommendation due to the limitation of Winbond W83627DHG WDT. You can call Portwell support center for reference. The value read back from CR_Twd indicates the counting down value instead of the original Twd. System will be reset after the Time-out Value to be counted down to zero. Users can directly fill a zero value into CR_Twd to disable WDT immediately. To ensure a successful access to the desired Control Register, the following programming guide should be followed.

Programming guide :

3.6   GPIO

The PEB-2739I provides 8 programmable input or output ports that can be individually configured to perform a simple basic I/O function. Users can configure each individual port to become an input or output port by programming register bit of I/O Selection. To invert port value, the setting of Inversion Register has to be made. Port values can be set to read or write through Data Register.

The GPIO ports are located on J9 shown as follows.
Notes : **Do not short-circuit Pin 9 and 10 of J9 !**

3.7   WDT/GPIO Assembly Code

```
#include <stdio.h>
#include <stdlib.h>
#include <conio.h>
void WDT_Enable(int time,int mode);
void WDT_Disable();
void GPIO_Set_Mode(int bit,int mode);
void GPIO_Write(int bit,int data);
int GPIO_Read(int bit);

void main(){
        outp (0x2e,0x87);//Input SIO entry key
        outp (0x2e,0x87);

        //WDT sample code
        WDT_Enable(20,0);
        //WDT_Disable();

        //GPIO sampe code
        GPIO_Set_Mode(0,0);//set GPIO 30 for output
        GPIO_Set_Mode(1,1);//set GPIO 31 for input
        GPIO_Set_Mode(2,1);//Set GPIO 32 for input
        GPIO_Write(0,1);//Set GPIO 30 for high

        outp (0x2e,0xAA);//Input SIO Exit key

        return;
}
// time<255    , mode 0 =sec, 1 =min
void WDT_Enable(int time,int mode){

        outp (0x2e,0x2d);
```

```
        outp (0x2f,inp(0x2f)&0xfe);//Enable WDT function

        outp (0x2e,0x07);
        outp (0x2f,0x08); //entry device 8

        outp (0x2e,0xF5);
        outp (0x2f,inp(0x2f)|(mode*0x08)); //bit3 0:second,1 Minute

        outp (0x2e,0xf6);
        outp (0x2f,time);// Set time (sec/min)

        outp (0x2e,0xf7);
        outp (0x2f,inp(0x2f)|0xc0);//enable reset time by mouse/keyboard
interrupt

}
void WDT_Disable(){

        outp (0x2e,0x2d);
        outp (0x2f,inp(0x2f)|0x01);//Disable WDT function
}
//bit 0~7=GPIO 30~37, mode 0=output 1=input
void GPIO_Set_Mode(int bit,int mode){
        int tmp=1<<bit;
        outp (0x2e,0x07);
        outp (0x2f,0x09);// entry device 9
        outp (0x2e,0xf0);
        outp (0x2f,(inp(0x2f)&~tmp)|(tmp*mode));//0 for output,1 for intput
}

//data 0 for low, 1 for high
void GPIO_Write(int bit,int data){
        int tmp=1<<bit;
        outp (0x2e,0x07);
        outp (0x2f,0x09);// entry device 9

        outp (0x2e,0xf1);
        outp (0x2f,(inp(0x2f)&~tmp)|(tmp*data));//0 for low,1 for high

}
//high return 1, low return 0
int GPIO_Read(int bit){
        int tmp=1<<bit;
        int data;
        outp (0x2e,0x07);
```

```
outp (0x2f,0x09);// entry device 9

outp (0x2e,0xf1);
data=inp(0x2f)&~tmp;//read bit

if (data==0)
          return 0;
else
          return 1;
```

Chapter 4
BIOS Setup Information

PEB-2739I is equipped with the AMI BIOS stored in Flash ROM. These BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power-off periods. When system is turned on, PEB-2739I communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start up.
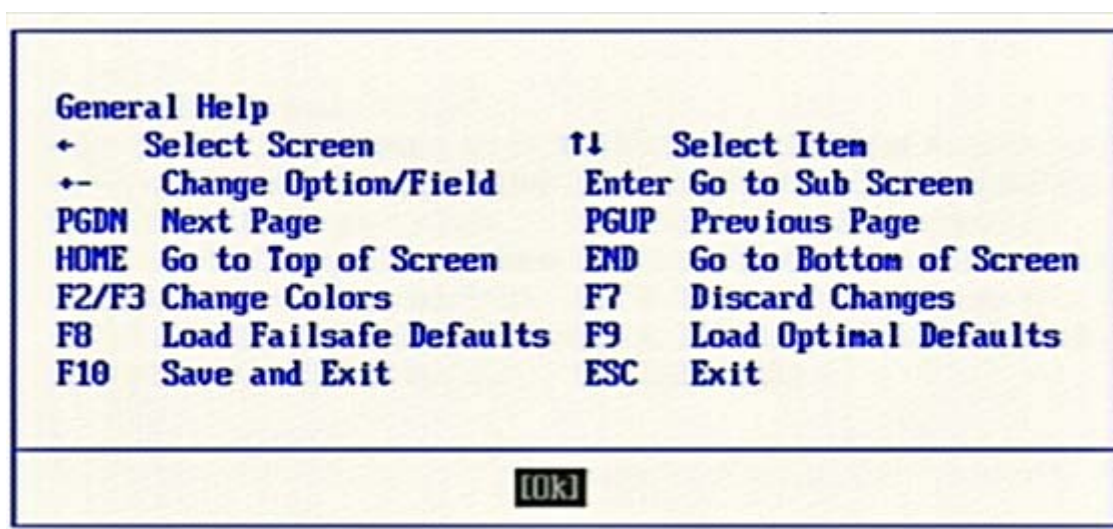
4.1 Entering Setup -- Launch System Setup

Power on the computer and the system will start POST (Power On Self Test) process. When the message below appears on the screen, press <Del> key to enter Setup.
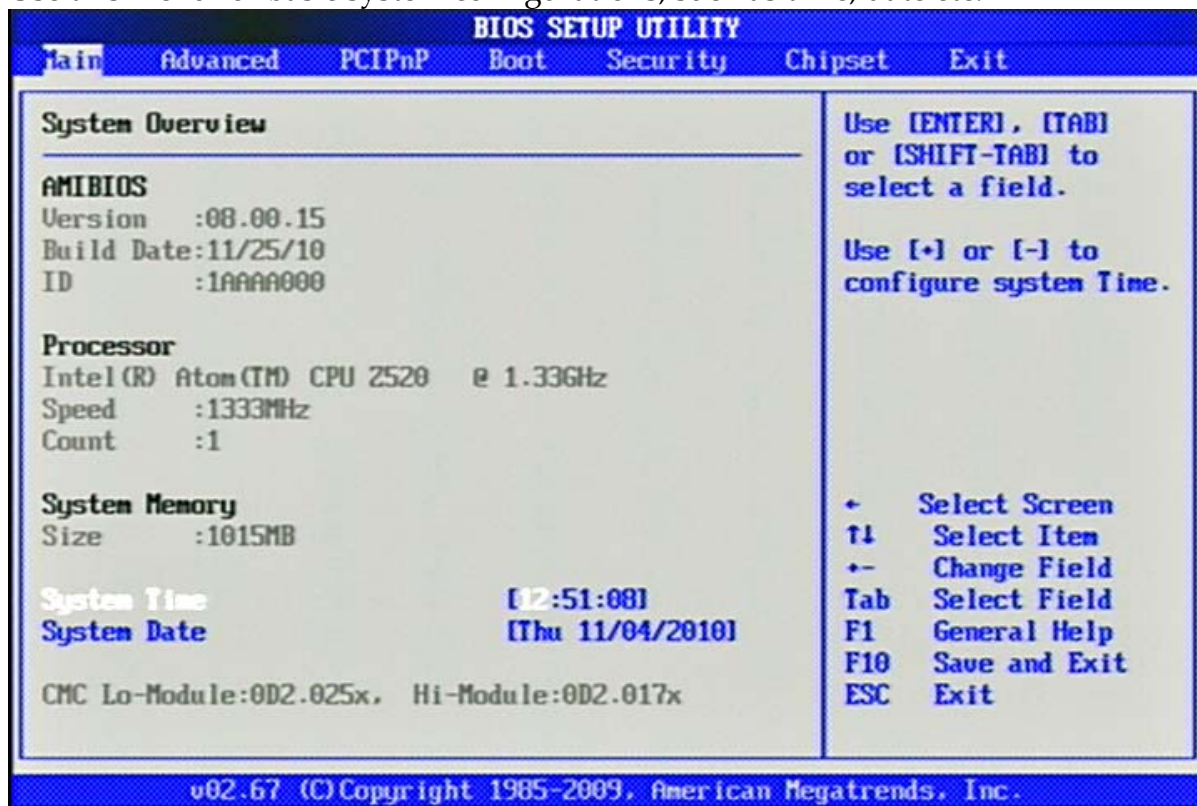Press <Del> to enter SETUP
If the message disappears before you respond and you still wish to enter Setup, restart the system by turning it OFF and On or pressing the RESET button. You may also restart the system by simultaneously pressing <Ctrl>, <Alt>, and <Delete> keys.
Press <F1> to Run SETUP or Resume
The BIOS setup program provides a General Help screen. You can call up this screen from any menu by simply pressing <F1>. The Help screen lists the appropriate keys to use and the possible selections for the highlighted item. Press <Esc> to exit the Help screen.

```
General Help
  ←      Select Screen        ↑↓      Select Item
  ←-     Change Option/Field   Enter Go to Sub Screen
 PGDN  Next Page              PGUP  Previous Page
 HOME  Go to Top of Screen    END   Go to Bottom of Screen
 F2/F3 Change Colors          F7    Discard Changes
 F8    Load Failsafe Defaults F9    Load Optimal Defaults
 F10   Save and Exit          ESC   Exit

                       [Ok]
```

4.2 Main

Use this menu for basic system configurations, such as time, date etc.

AMI BIOS, Processor, System Memory
These items show the firmware and hardware specifications of your system. Read only.
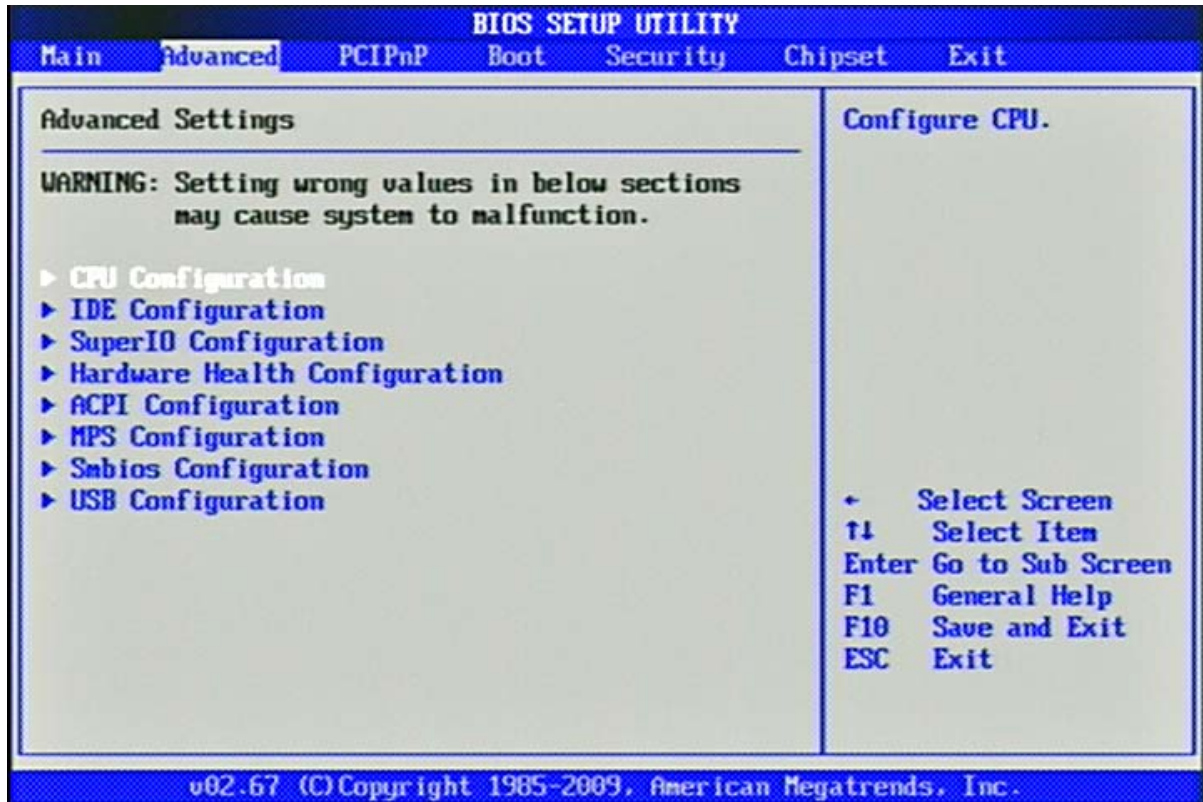
System Time
The time format is <Hour> <Minute> <Second>. Use [+] or [−] to configure system Time.

System Date
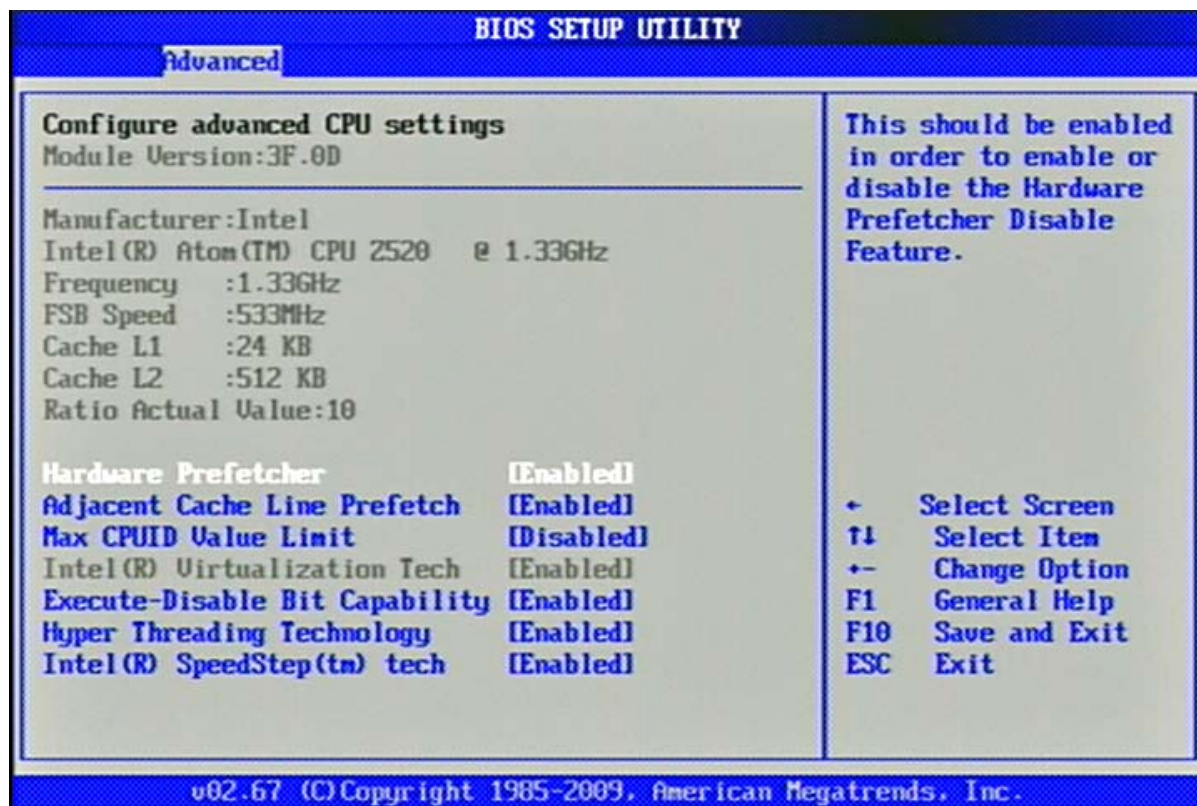The date format is <Day>, <Month> <Date> <Year>. Use [+] or [−] to configure system Date.

4.3   Advanced

Use this menu to set up the items of special enhanced features.

CPU Configuration

These items show the advanced specifications of your CPU. Read only.

```
                    BIOS SETUP UTILITY
  Advanced

 Configure advanced CPU settings              This should be enabled
 Module Version:3F.0D                         in order to enable or
 ─────────────────────────────────────        disable the Hardware
 Manufacturer:Intel                           Prefetcher Disable
 Intel(R) Atom(TM) CPU Z520   @ 1.33GHz        Feature.
 Frequency    :1.33GHz
 FSB Speed    :533MHz
 Cache L1     :24 KB
 Cache L2     :512 KB
 Ratio Actual Value:10

 Hardware Prefetcher          [Enabled]
 Adjacent Cache Line Prefetch [Enabled]        ←     Select Screen
 Max CPUID Value Limit        [Disabled]       ↑↓    Select Item
 Intel(R) Virtualization Tech [Enabled]        ←─    Change Option
 Execute-Disable Bit Capability [Enabled]      F1    General Help
 Hyper Threading Technology   [Enabled]        F10   Save and Exit
 Intel(R) SpeedStep(tm) tech  [Enabled]        ESC   Exit


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```

Hardware Prefetcher

The choice: Disabled, Enabled.

Adjacent Cache Line Prefetch

The choice: Disabled, Enabled.

Max CPUID Value Limit
Disabled for Windows XP

The choice: Disabled, Enabled.

Execute-Disable Bit capability
When disabled, force the XD feature flag to always return 0

The choice: Disabled, Enabled.

Hyper Threading Technology

"Enabled" for Windows XP and Linux 2.4.X (OS optimized for Hyper-Threading Technology and "Disabled" for other OS (OS not optimized for Hyper-Threading Technology).
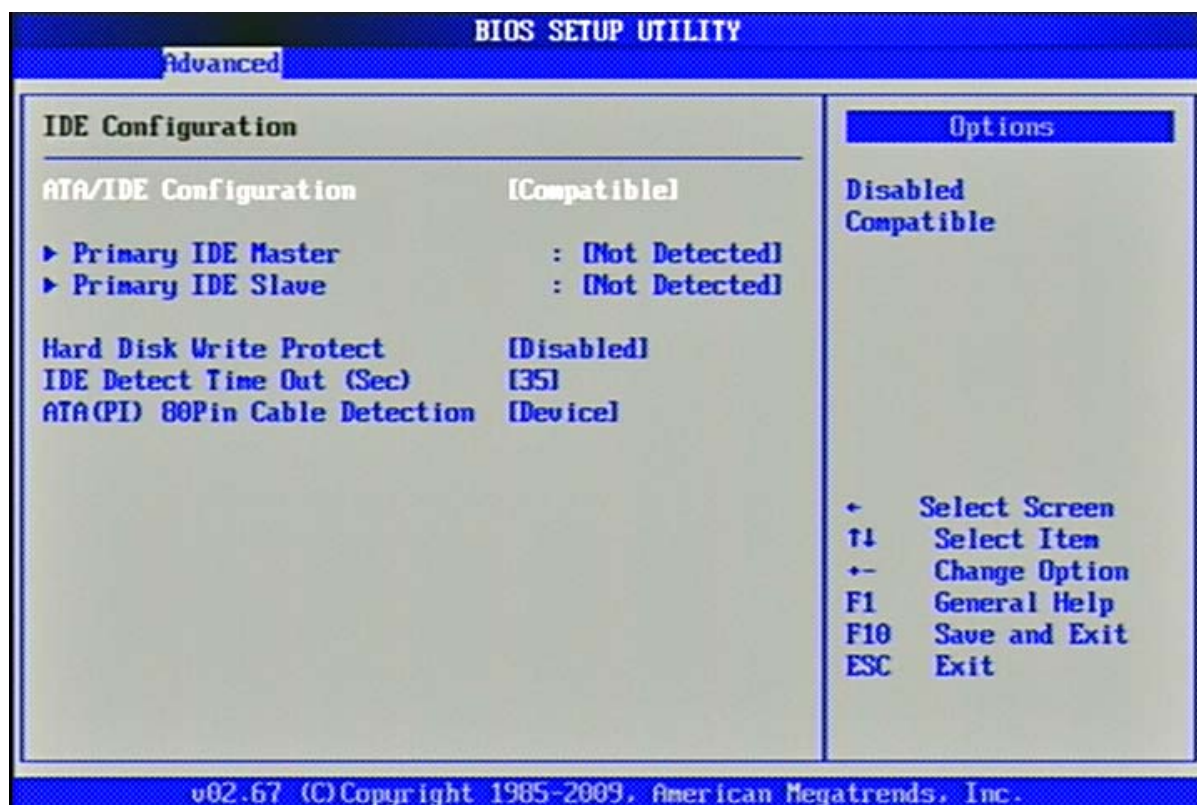
The choice: Enabled, Disabled.

Intel(R) Speed Step (tm) Tech

Disable: Disable GV3.
Enable: Enable GV3.

IDE Configuration

The IDE Configuration the IDE devices, such as hard disk drive or CD-ROM drive. It uses a separate sub menu to configure each hard disk drive (Master and Slave).
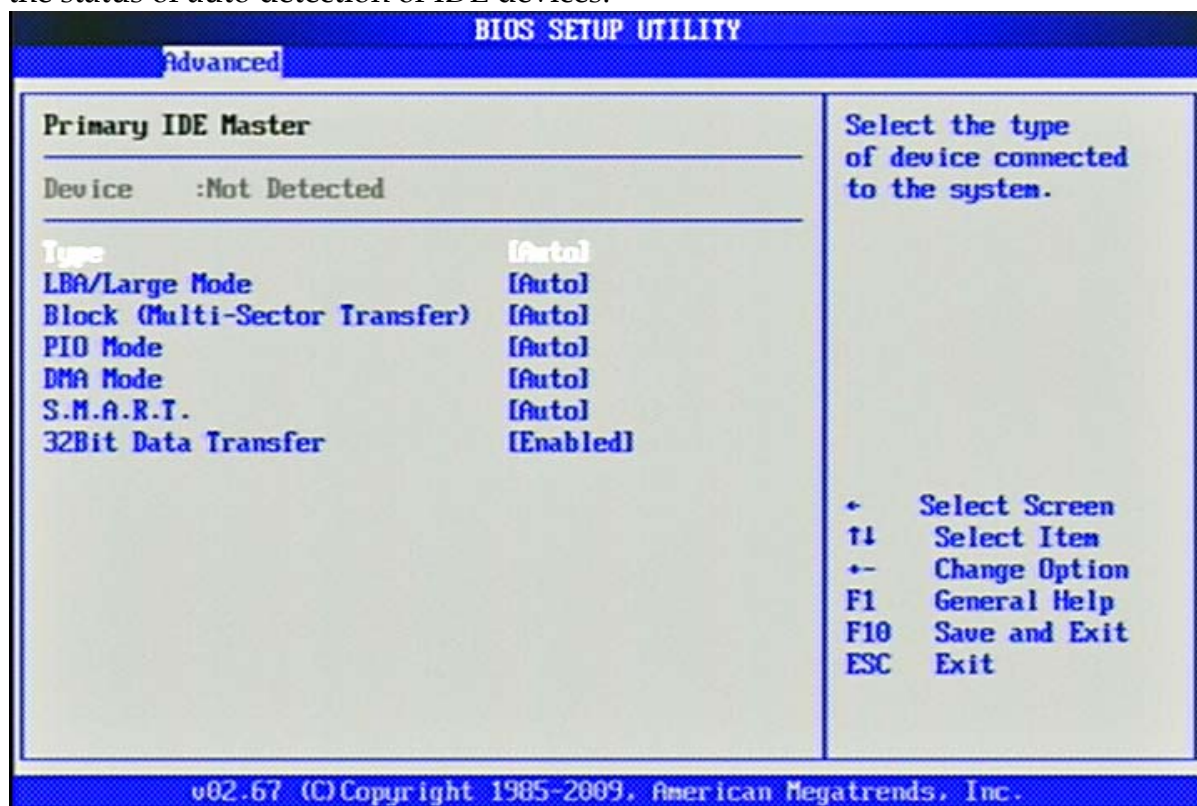

ATA/IDE Configuration

The choice: Disabled, Compatible, Enabled.

Primary IDE Master / Slave

While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of auto detection of IDE devices.

```
                    BIOS SETUP UTILITY
 Advanced

 Primary IDE Master                          Select the type
 ─────────────────────────                   of device connected
 Device    :Not Detected                     to the system.

 Type                        [Auto]
 LBA/Large Mode              [Auto]
 Block (Multi-Sector Transfer)  [Auto]
 PIO Mode                    [Auto]
 DMA Mode                    [Auto]
 S.M.A.R.T.                  [Auto]
 32Bit Data Transfer         [Enabled]

                                             ←    Select Screen
                                             ↑↓   Select Item
                                             +-   Change Option
                                             F1   General Help
                                             F10  Save and Exit
                                             ESC  Exit


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```

[Type] Press PgUp/<+> or PgDn/<−> to select [Manual], [None] or [Auto] type. You can use [Manual] to define your own drive type manually.

[LBA/Large Mode] Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads and Sectors.

[Block (Multi-Sector Transfer)] Any selection except Disabled determines the number of sectors transferred per block.

[PIO Mode] Indicates the type of PIO (Programmed Input/Output)

[DMA Mode] Indicates the type of Ultra DMA

[S.M.A.R.T.] This allows you to activate the S.M.A.R.T. (Self-Monitoring Analysis & Reporting Technology) capability for the hard disks. S. M.A.R.T is a utility that monitors your disk status to predict hard disk failure. This gives you an opportunity to move data from a hard disk that is going to fail to a safe place before the hard disk becomes offline.

[32 Bit Data Transfer] Enable/Disable 32-bit Data Transfer.

Hard Disk Write Protect

Disabled/Enabled device write protection, this will be effective only if device is accessed through BIOS.

The choice: Disabled, Enabled.

IDE Detect Time Out (Sec)

Select the time out value for detecting ATA/ATAPI device (s).
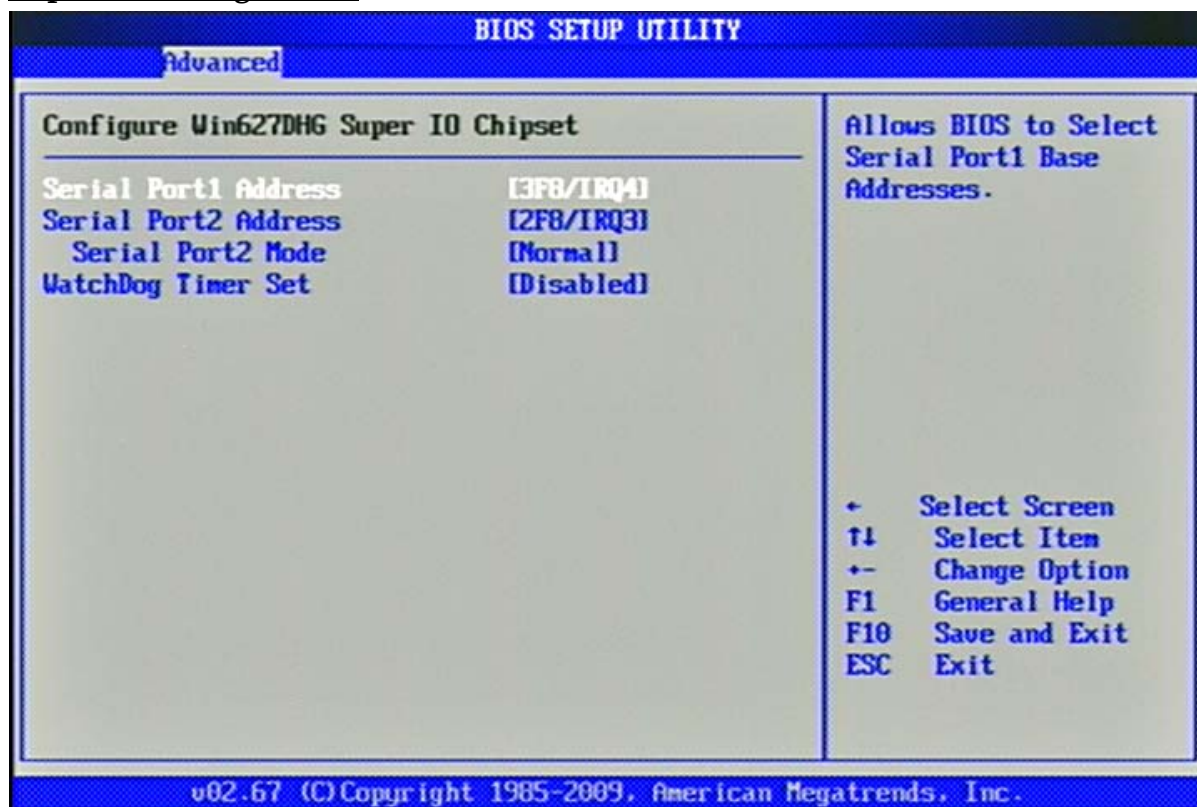
The choice: 0, 5, 10, 15, 20, 25, 30, 35.

ATA(PI) 80Pin Cable Detection

Select the mechanism for detecting 80Pin ATA (PI) cable.

The choice: Host & Device, Host, Device.

Super IO Configuration

Serial Port 1 Address/IRQ

Allows BIOS Select Serial Port1 Base Addresses.

The choice: Address: Disabled, 3F8, 3E8, 2E8,
                          IRQ: 3, 4, 10, 11.

Serial Port 2 Address/IRQ

Allows BIOS Select Serial Port2 Base Addresses.

The choice: Address: Disabled, 2F8, 3E8, 2E8,
IRQ: 3, 4, 10, 11.

Serial Port 2 Mode

The choice: Normal, IrDA, ASK IR,

Watch Dog Timer Set

This BIOS testing option is able to reset the system according to the selected table.

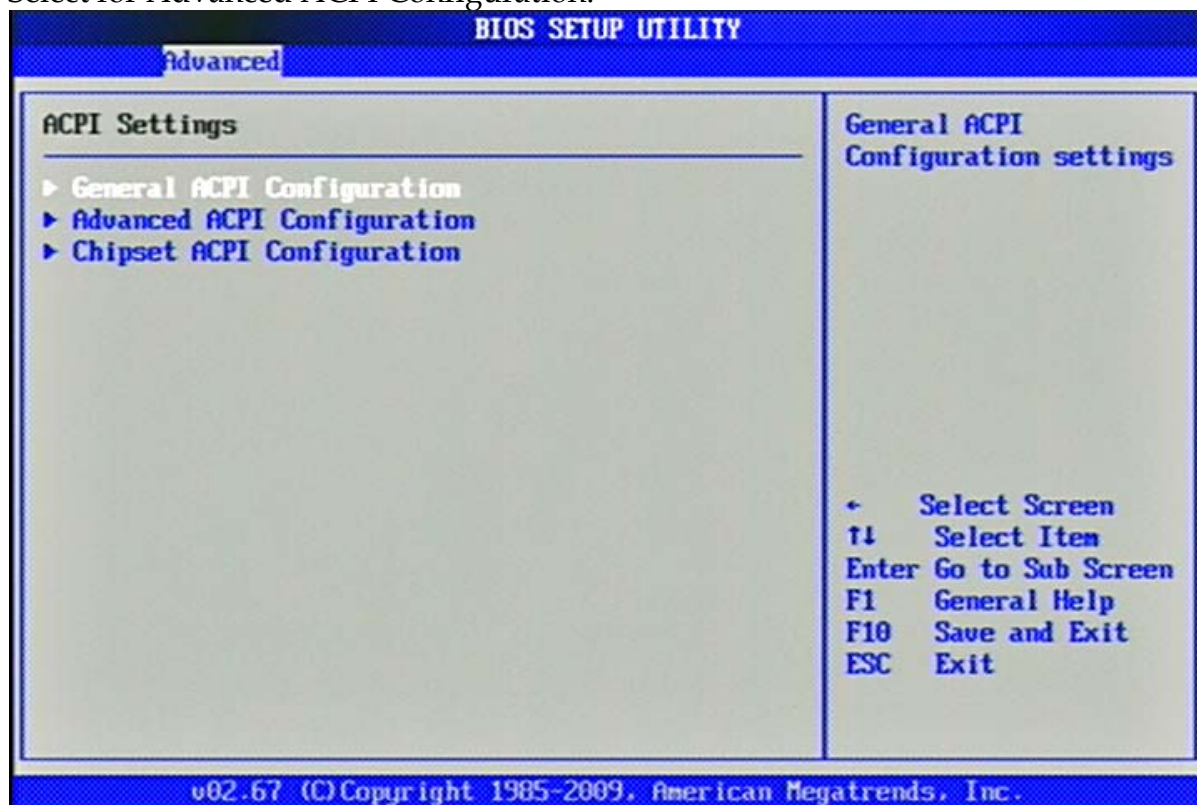The Choice: Disabled, 10, 20, 30, 40 sec. 1, 2, 4 min.

Hardware Health Configuration
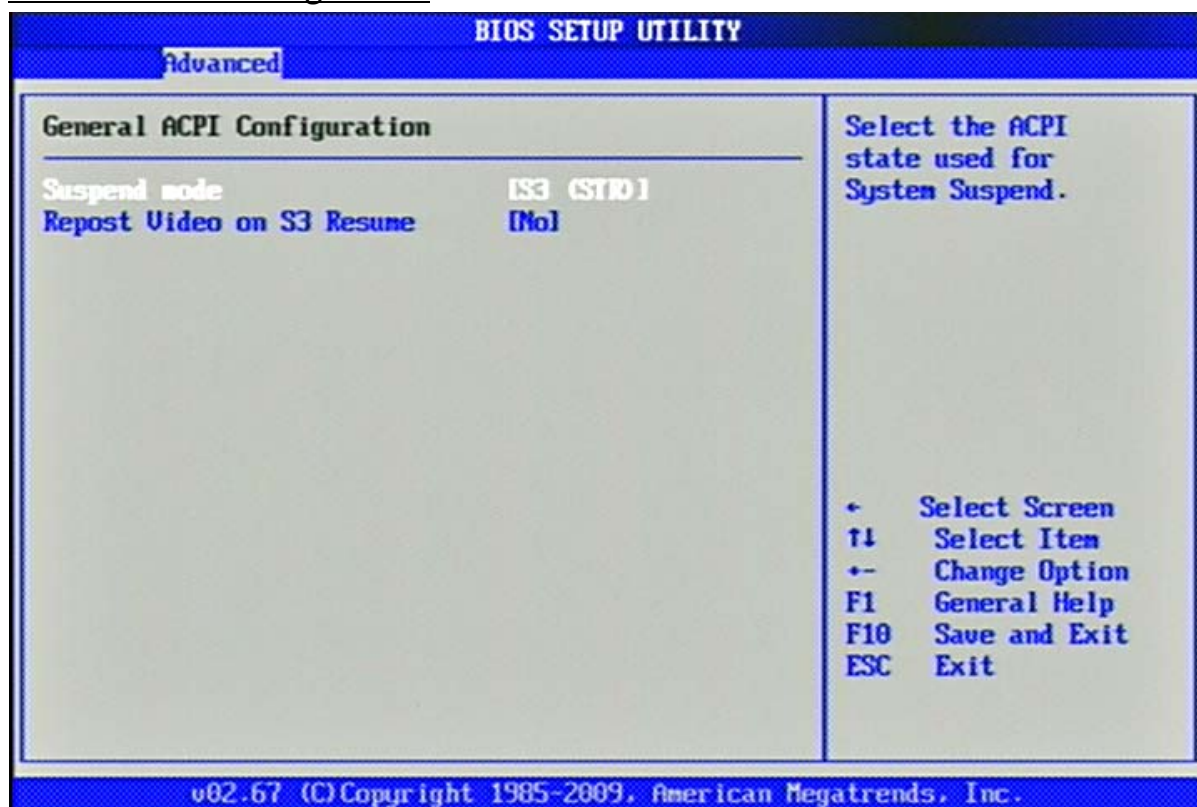
Configuration / monitor the Hardware Health.
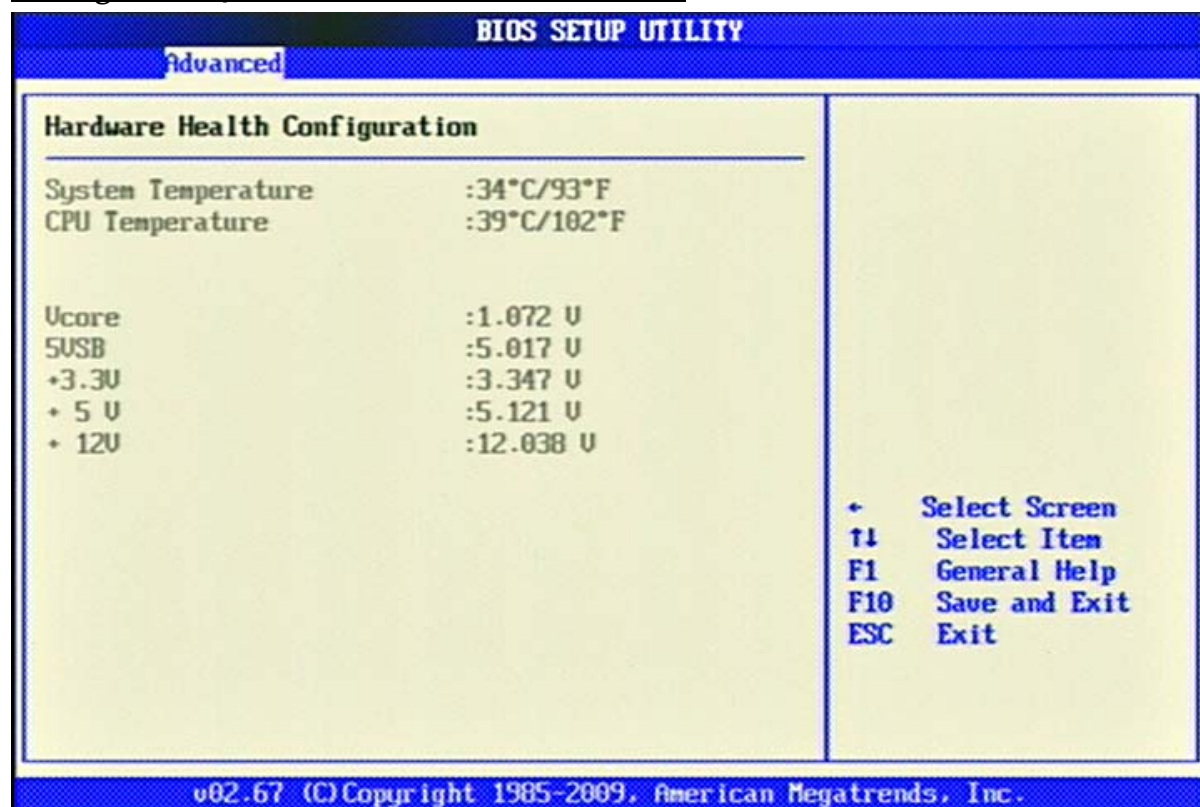
ACPI Settings

Select for Advanced ACPI Configuration.

```
                        BIOS SETUP UTILITY
   Advanced

 ACPI Settings                                 General ACPI
                                               Configuration settings
 ▶ General ACPI Configuration
 ▶ Advanced ACPI Configuration
 ▶ Chipset ACPI Configuration




                                               ←      Select Screen
                                               ↑↓     Select Item
                                               Enter  Go to Sub Screen
                                               F1     General Help
                                               F10    Save and Exit
                                               ESC    Exit


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```

General ACPI Configuration

```
                        BIOS SETUP UTILITY
   Advanced

 General ACPI Configuration                    Select the ACPI
                                               state used for
 Suspend mode            [S3 (STR)]            System Suspend.
 Repost Video on S3 Resume  [No]





                                               ←      Select Screen
                                               ↑↓     Select Item
                                               +-     Change Option
                                               F1     General Help
                                               F10    Save and Exit
                                               ESC    Exit


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```

Suspend mode

This item specifies the power saving modes for ACPI function. If your operating system supports ACPI, you can choose to enter the Standby mode in S1 (POS) or S3 (STR) fashion through the setting of this field. Options are:

  [S1 (POS)] The S1 sleep mode is a low power state. In this state, no system context is lost (CPU or chipset) and hardware maintains all system contexts.

[S3 (STR)] The S3 sleep mode is a lower power state where the information of system configuration and open applications/ files is saved to main memory that remains powered while most other hardware components turn off to save energy. The information stored in memory will be used to restore the system when a "wake up" event occurs.

Advanced ACPI Configuration

Advanced ACPI Configuration settings, Use this section to configure additional ACPI options.
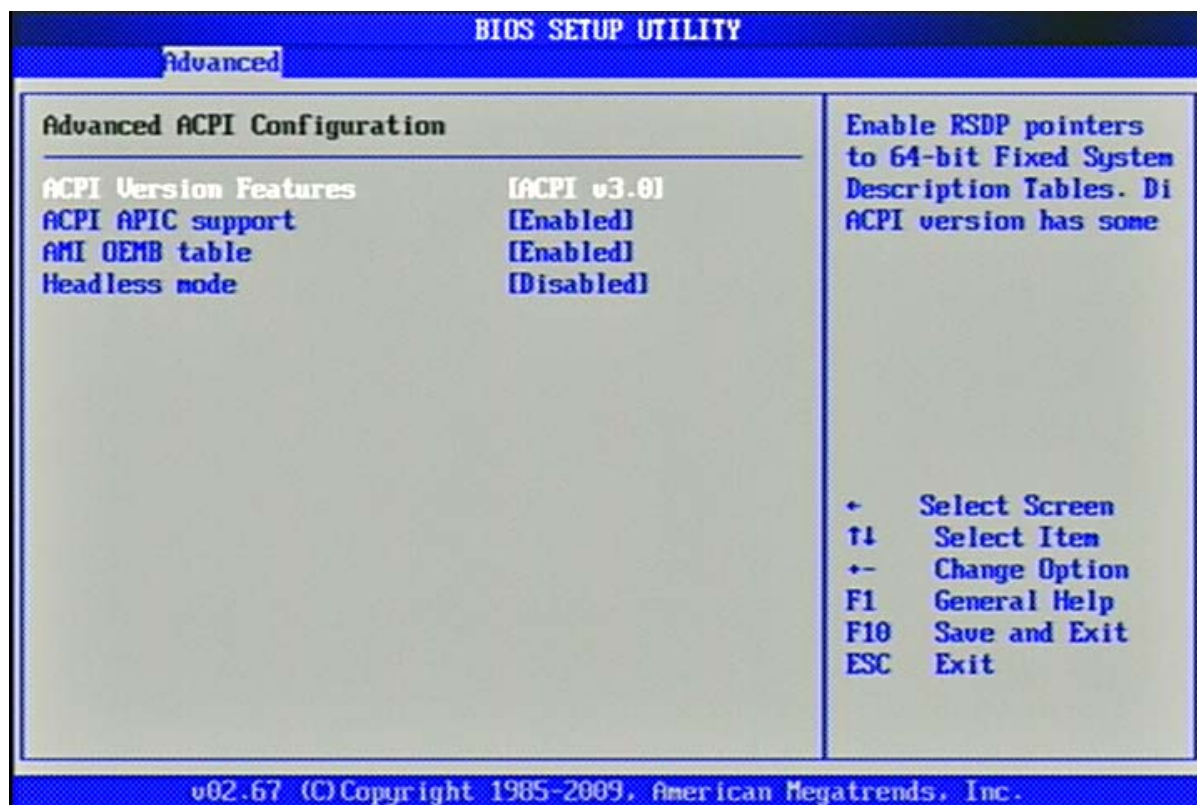
ACPI Version Features

Enable RSDP pointers to 64-bit Fixed System Description Tables.

The choice: ACPI v1.0 / ACPI v2.0 / ACPI v3.0.

ACPI APIC support
Include ACPI APIC table pointer to RSDT pointer list.

The choice: Disabled, Enabled.

AMI OEMB table
Include OEMB table pointer to R(X) SDT pointer list.

The choice: Disabled, Enabled.

Headless mode
Enable / Disable Headless operation mode through ACPI.

The choice: Disabled, Enabled.

South Bridge ACPI Configuration
The South Bridge ACPI related Configuration settings, Use this section to configure additional ACPI options.
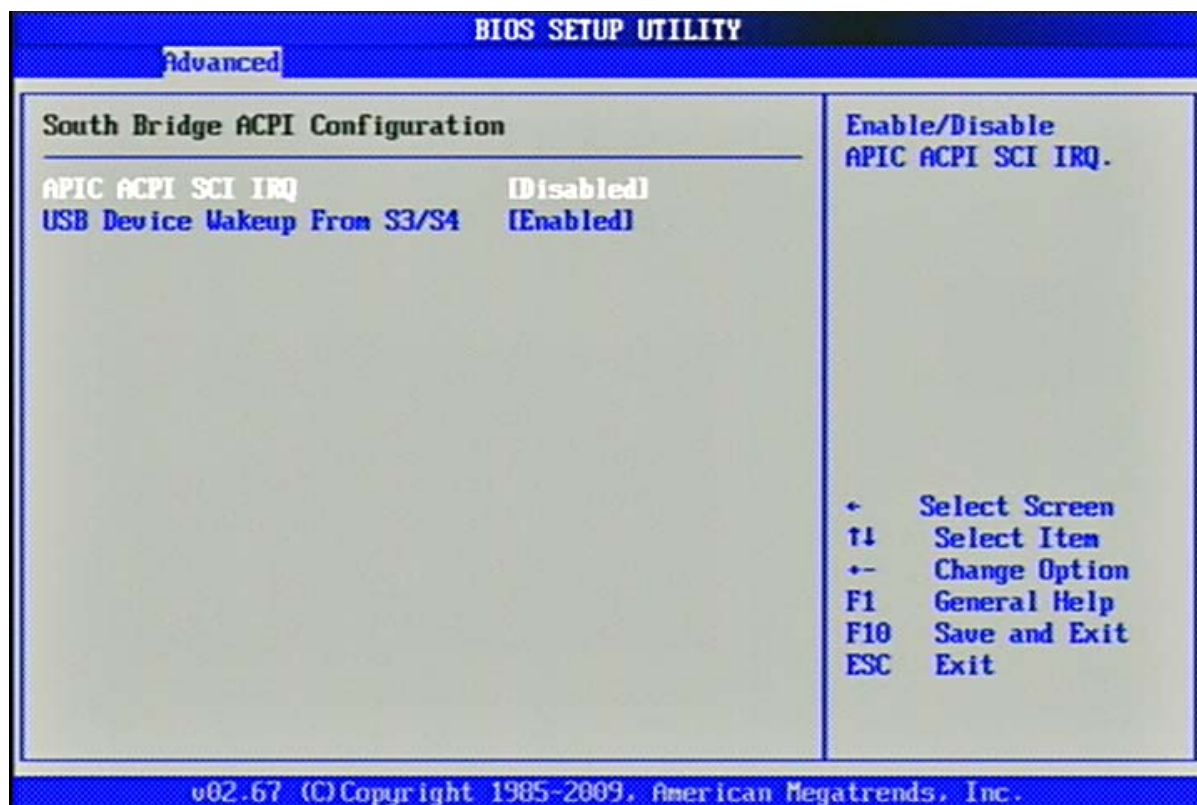
APIC ACPI SCI IRQ

Enable / Disable APIC ACPI SCI IRQ.

The choice: Disabled, Enabled.

USB Device Wakeup From S3/S4

Enable / Disable USB device Wake from S3/S4 mode.

The choice: Disabled, Enabled.

MPS Configuration

Configure the Multi-Processor Table.
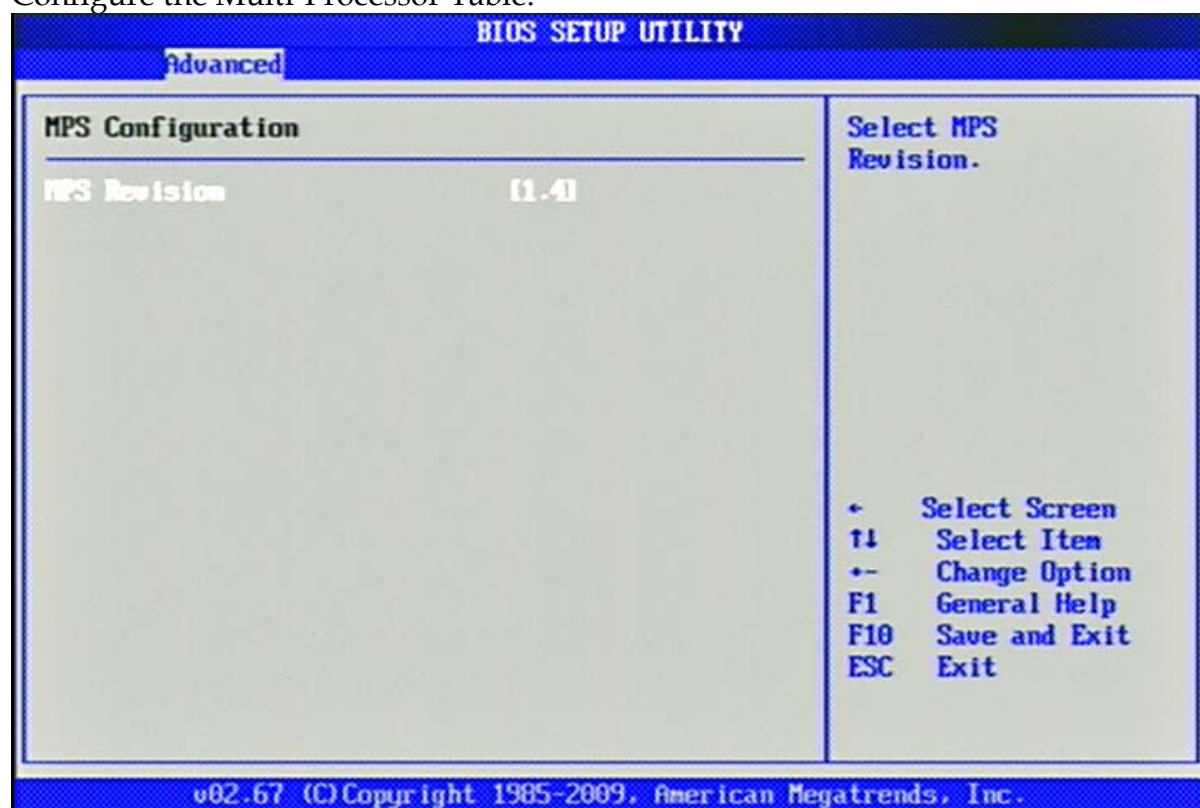
MPS Revision

This field allows you to select which MPS (Multi-Processor Specification) version to be used for the operating system. You need to select the MPS version supported by your operating system. To find out which version to use, consult the vendor of your operating system.

The choice: 1.1, 1.4.

Smbios Configuration

SMBIOS Configuration Menu
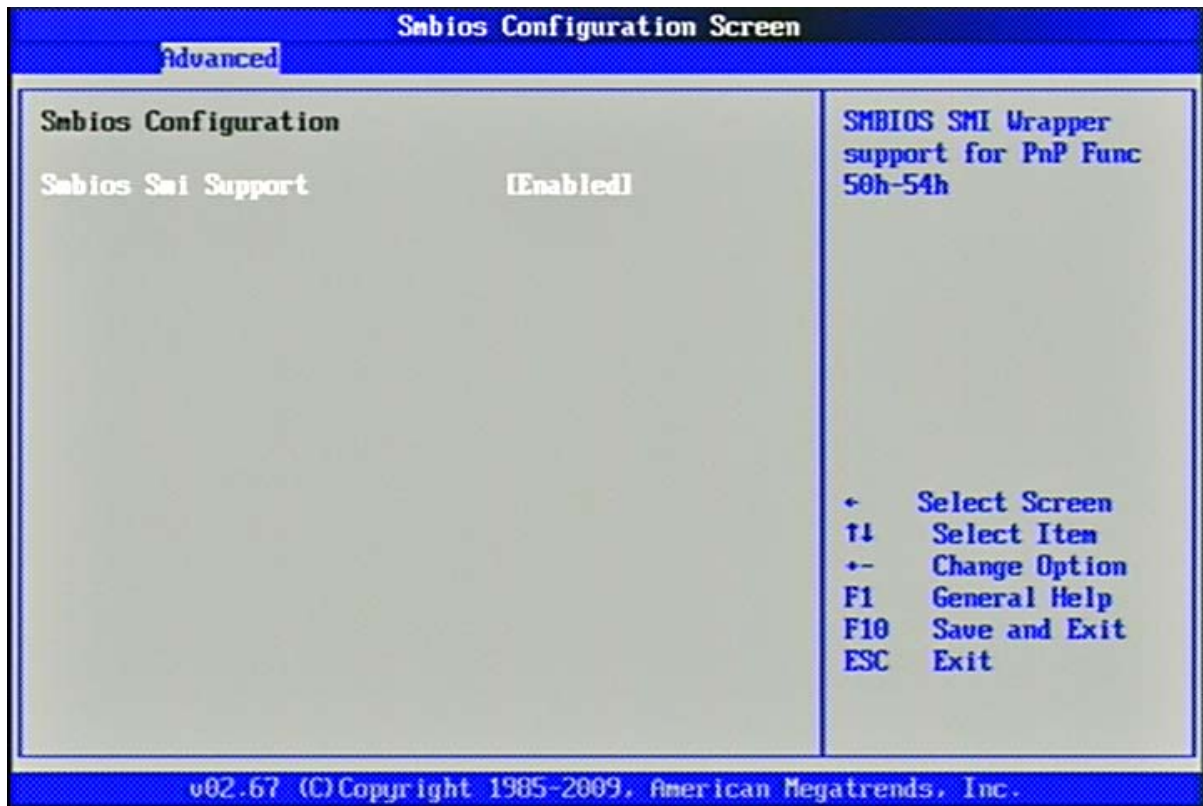
Smbios Smi Support

SMBIOS SMI Wrapper support for PnP Function 50h-54h

The choice: Disabled, Enabled.

USB Configuration
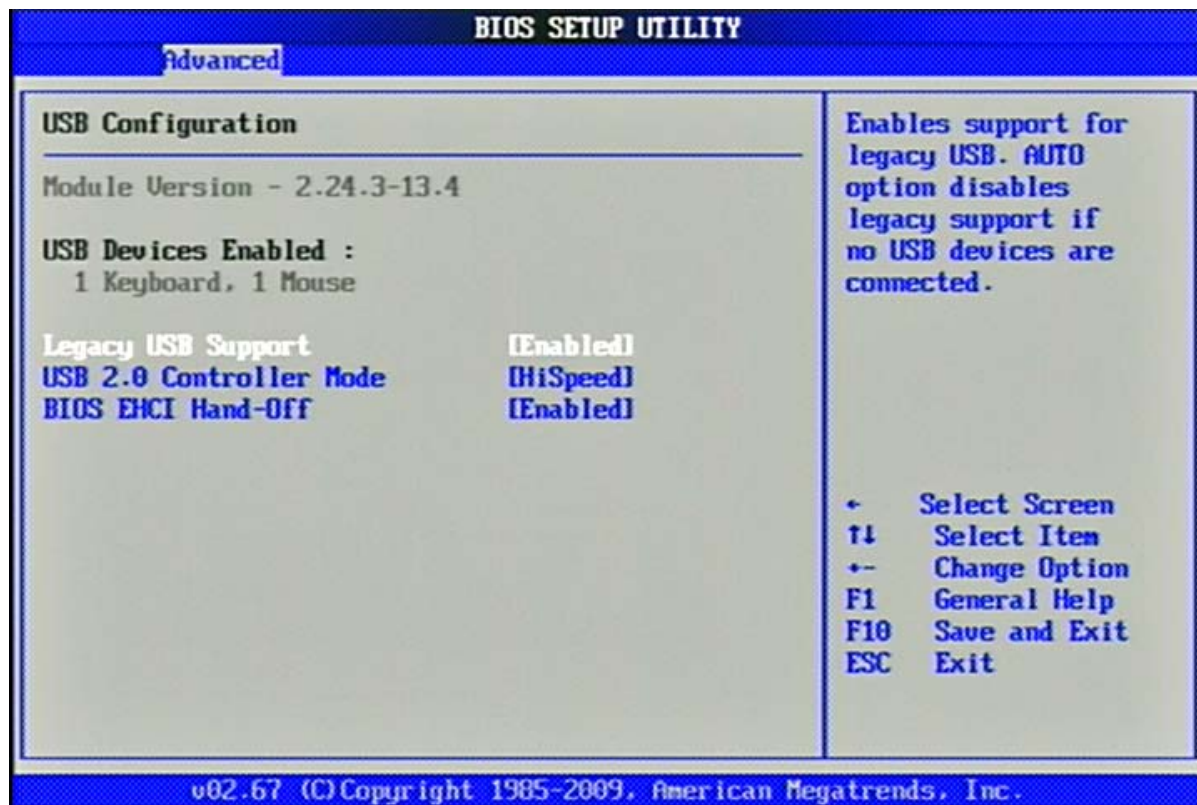
Legacy USB Support

Set to [Enabled] if you need to use any USB 1.1/2.0 device in the operating system that does not support or have any USB 1.1/2.0 driver installed, such as DOS and SCO Unix.

The choice: Disabled, Enabled, Auto.

USB 2.0 Controller Mode

This setting specifies the operation mode of the onboard USB 2.0 controller.

The choice: FullSpeed, HiSpeed.

BIOS EHCI Hand-Off

This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should claim by EHCI driver.

The choice: Disabled, Enabled.

4.4   PCIPnP

Advanced PCI/PnP setting wrong values in below sections may cause system to malfunction.
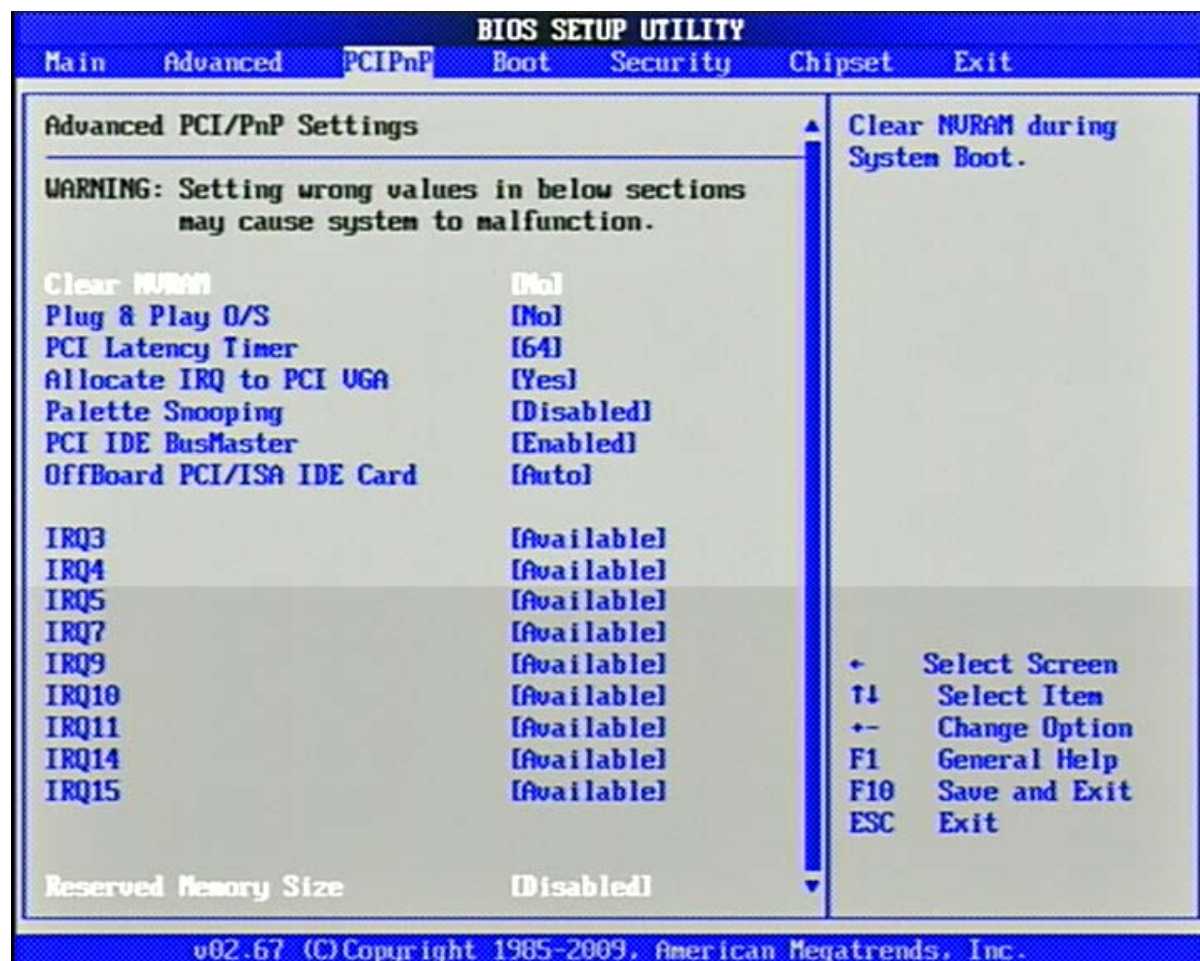
Clear NVRAM
Clear NVRAM during System Boot.
The choice: No, Yes.

Plug & Play O/S
No: lets the BIOS configure all the devices in the system.
Yes: lets the operating system configure Plug and Play (PnP) devices not required for boot if your system has a Plug and Play operating system.

The choice: No, Yes.

PCI Latency Timer
Select value in units of PCI clocks for PCI device latency timer register.
The choice: 32, 64, 96, 128, 160, 192, 224, 248.

Allocate IRQ to PCI VGA

Yes: Assigns IRQ to PCI VGA card if card requests an IRQ.
No: Does not assign IRQ to PCI VGA card even if card requests an IRQ.

The choice: No, Yes.

Palette Snooping

Enabled: informs the PCI devices that an ISA graphics device is installed in the system so the card will function correctly.

The choice: Disabled, Enabled.

PCI IDE BusMaster

Enabled: Uses PCI bus mastering for reading / writing to IDE drives.

The choice: Disabled, Enabled.

OffBoard PCI/ISA IDE Card

Some PCI IDE cards may require this to be set to the PCI slot number that is holding the card. AUTO: Works for most PCI IDE cards

The choice: Auto, PCI Slot1, PCI Slot2, PCI Slot3, PCI Slot4, PCI Slot5, PCI Slot6.

IRQ 3 / IRQ 4 / IRQ5 / IRQ7 / IRQ 9 / IRQ 10 / IRQ 11 / IRQ 14 / IRQ 15

Available: Specified IRQ is available to be used by PCI/PnP devices.
Reserved: Specified IRQ is reserved for used by Legacy ISA devices.
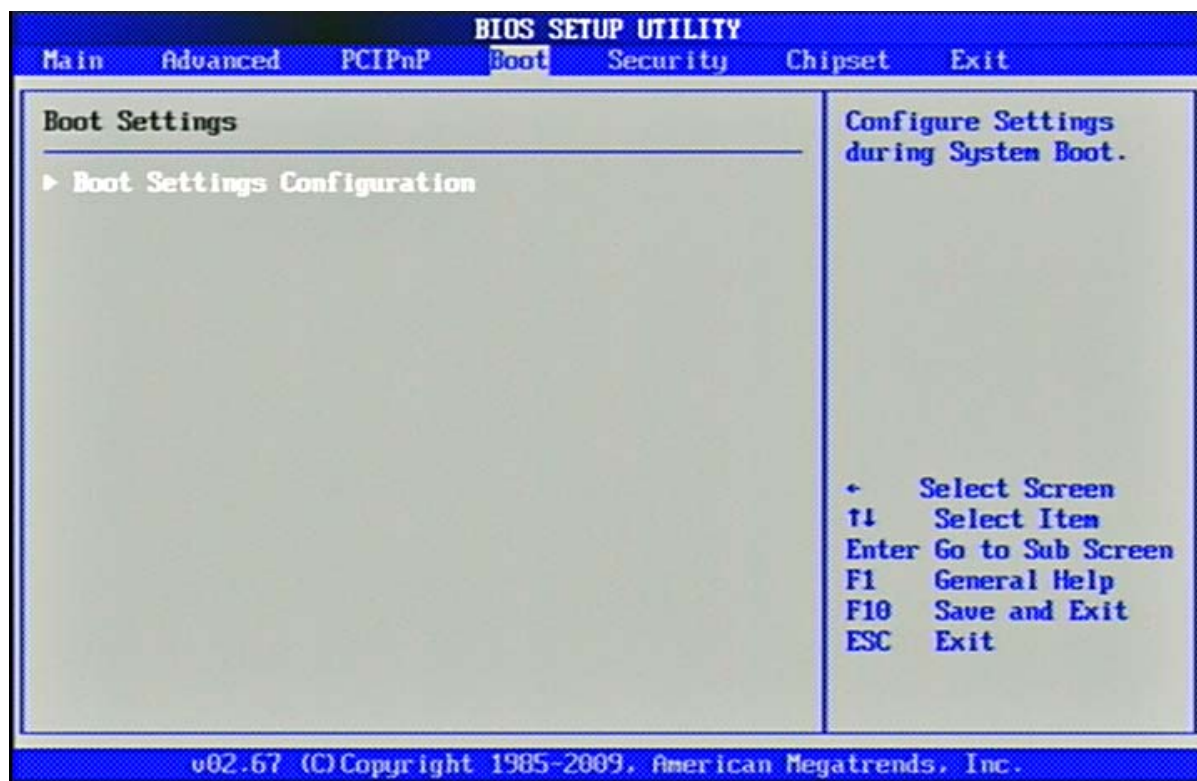
The choice: Available, Reserved.

Reserved Memory Size

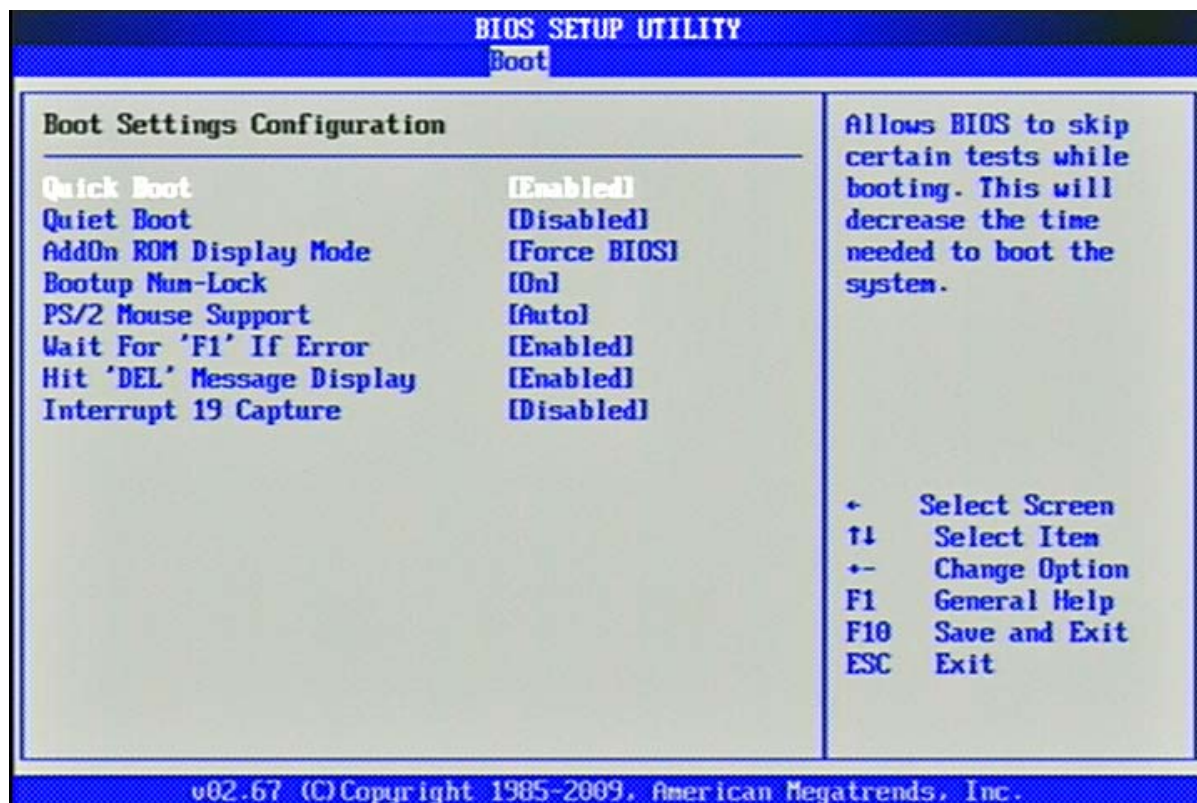Select Size of memory block to reserve for legacy ISA devices.

The choice: Disabled, 16K, 32K, 64K.

4.5 Boot

Use this menu to specify the priority of boot devices.

Boot Settings Configuration

Quick Boot

Enabling this setting will cause the BIOS power-on self test routine to skip some of its tests during boot up for faster system boot.

The choice: Disabled, Enabled.

Quiet Boot

This BIOS feature determines if the BIOS should hide the normal POST messages with the motherboard or system manufacturer's full-screen logo. When it is enabled, the BIOS will display the full-screen logo during the boot-up sequence, hiding normal POST messages.
When it is disabled, the BIOS will display the normal POST messages, instead of the full-screen logo.

Please note that enabling this BIOS feature often adds 2-3 seconds of delay to the booting sequence. This delay ensures that the logo is displayed for a sufficient amount of time. Therefore, it is recommended that you disable this BIOS feature for a faster boot-up time.

The choice: Disabled, Enabled.

AddOn ROM Display Mode

This item is used to determine the display mode when an optional ROM is initialized during POST. When set to [Force BIOS], the display mode used by AMI BIOS is used. Select [Keep Current] if you want to use the display mode of optional ROM.

The choice: Force BIOS, Keep Current.

Bootup Num-Lock

This setting is to set the Num Lock status when the system is powered on.
Setting to [On] will turn on the Num Lock key when the system is powered on.
Setting to [Off] will allow users to use the arrow keys on the numeric keypad.

The choice: Off, On.

PS/2 Mouse support

Select [Enabled] if you need to use a PS/2-interfaced mouse in the operating system.

The choice: Disabled, Enabled, Auto.

Wait For 'F1' If Error

When this setting is set to [Enabled] and the boot sequence encounters an error, it asks you to press F1. If disabled, the system continues to boot without waiting for you to press any keys.

The choice: Disabled, Enabled.

Hit 'DEL' Message Display

Set this option to [Disabled] to prevent the message as follows:

Hit Del if you want to run setup
It will prevent the message from appearing on the first BIOS screen when the computer boots. Set it to [Enabled] when you want to run the BIOS Setup Utility.

The choice: Disabled, Enabled.

Interrupt 19 Capture

Interrupt 19 is the software interrupt that handles the boot disk function. When enabled, this BIOS feature allows the ROM BIOS of these host adaptors to "capture" Interrupt 19 during the boot process so that drives attached to these adaptors can function as bootable disks. In addition, it allows you to gain access to the host adaptor's ROM setup utility, if one is available.

When disabled, the ROM BIOS of these host adaptors will not be able to "cap ture" Interrupt 19. Therefore, you will not be able to boot operating systems from any bootable disks attached to these host adaptors. Nor will you be able to gain access to their ROM setup utilities.

The choice: Disabled, Enabled.
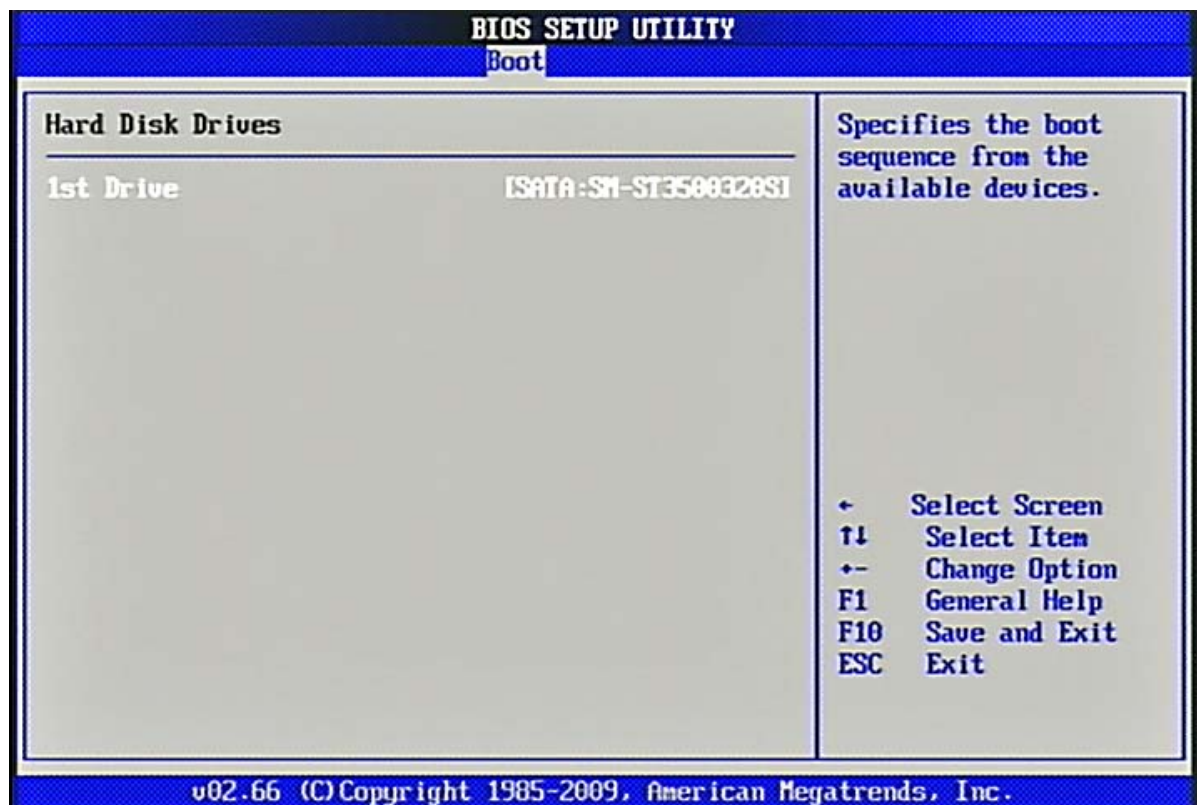
Boot Device Priority
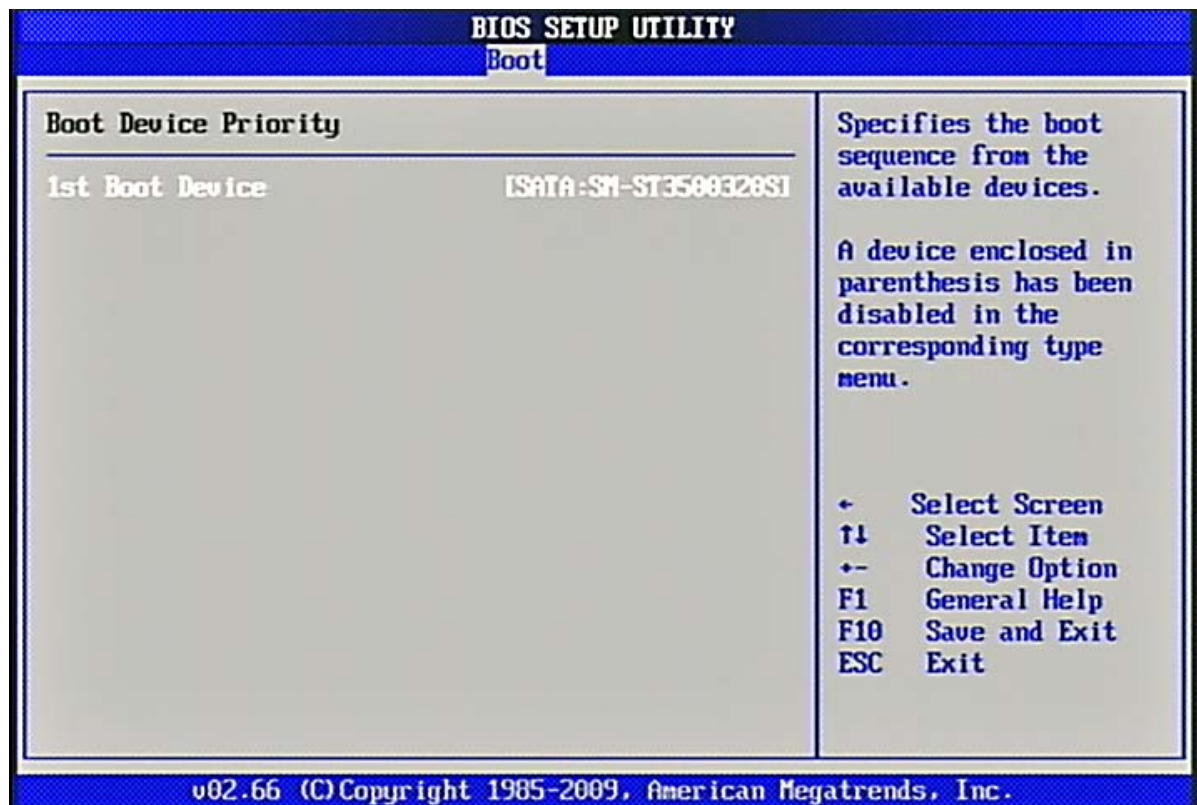
1st Boot Device

The items allow you to set the sequence of boot devices where BIOS attempts to load the disk operating system. First press <Enter> to enter the sub-menu. Then you may use the arrow keys (↑ ↓) to select the desired device, then press <+>, <−> or <PageUp>, <PageDown> key to move it up/down in the priority list.

The choice: (Network: IBA GE Slot 00C8 v1324), Disabled.

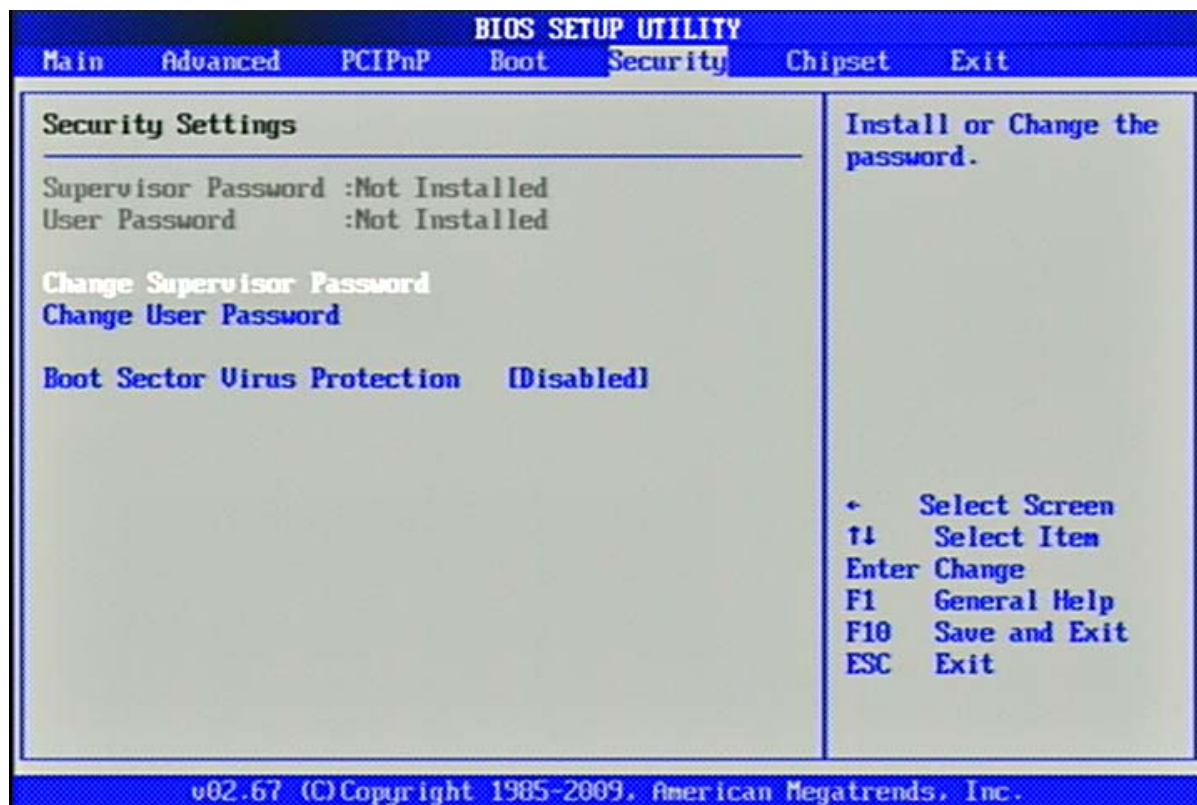## Hard Disk Drives

1st Drive

This setting allows users to set the priority of the removable devices. First press <Enter> to enter the sub-menu. Then you may use the arrow keys (↑ ↓) to select the desired device, then press <+>, <−> or <PageUp>, <PageDown> key to move it up/down in the priority list.

4.6 Security

Use this menu to set supervisor and user passwords.

```
                    BIOS SETUP UTILITY
 Main    Advanced    PCIPnP    Boot    Security    Chipset    Exit

 Security Settings                           Install or Change the
                                             password.
 Supervisor Password :Not Installed
 User Password        :Not Installed

 Change Supervisor Password
 Change User Password

 Boot Sector Virus Protection    [Disabled]


                                             +     Select Screen
                                             ↑↓    Select Item
                                             Enter Change
                                             F1    General Help
                                             F10   Save and Exit
                                             ESC   Exit


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```

Supervisor Password / Change Supervisor Password
Supervisor Password controls access to the BIOS Setup utility. These settings allow you to set or change the supervisor password.

User Password / Change User Password
User Password controls access to the system at boot. These settings allow you to set or change the user password.
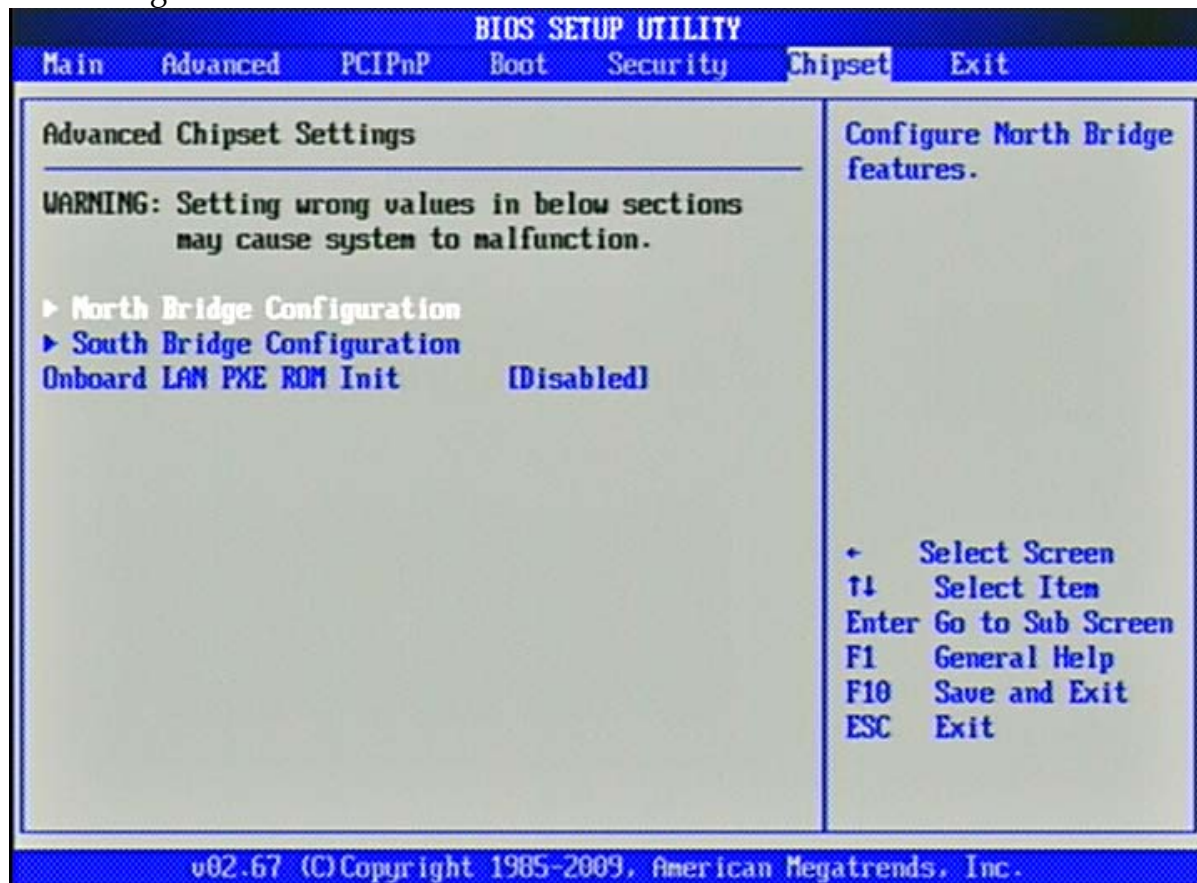
Boot Sector Virus Protection
Boot Sector Virus Protection.

The choice: Disabled, Enabled.

4.7   Chipset

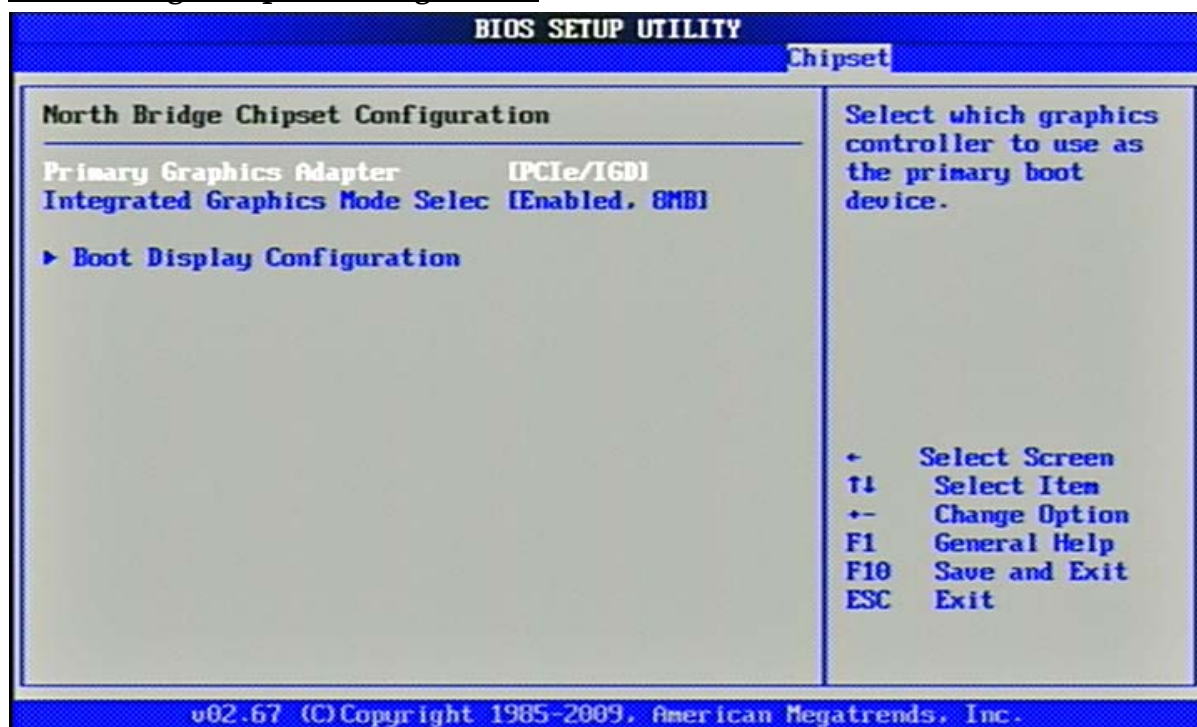This menu controls the advanced features of the onboard Northbridge and Southbridge.

Onboard LAN PXE ROM Init

The choice: Disabled, Enabled.

North Bridge Chipset Configuration

```
                    BIOS SETUP UTILITY
                                          Chipset

North Bridge Chipset Configuration            Select which graphics
                                              controller to use as
Primary Graphics Adapter        [PCIe/IGD]    the primary boot
Integrated Graphics Mode Selec  [Enabled, 8MB] device.

▶ Boot Display Configuration




                                              ←     Select Screen
                                              ↑↓    Select Item
                                              +-    Change Option
                                              F1    General Help
                                              F10   Save and Exit
                                              ESC   Exit


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```

Primary Graphic Adapter

Select which graphics controller to use as the primary boot device.
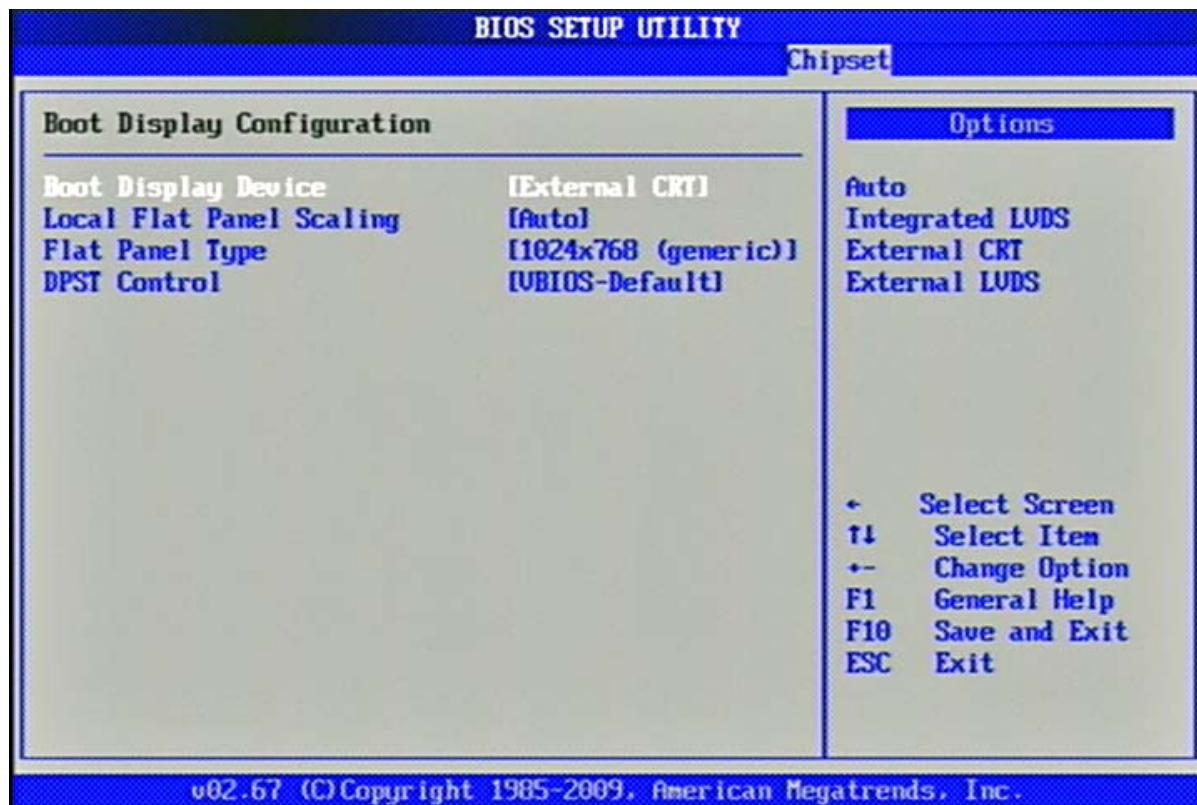
The choice: IGD, PCIe/IGD.

Internal Graphics Mode Select

Select the amount of system memory used by the internal graphics device.

The choice: Disable, Enabled, 1MB, Enabled, 4MB, Enabled, 8MB.

Video Function Configuration

Boot Display Device

The choice: Auto, Integrated LVDS, External CRT, External LVDS.

Local Flat Panel Scaling

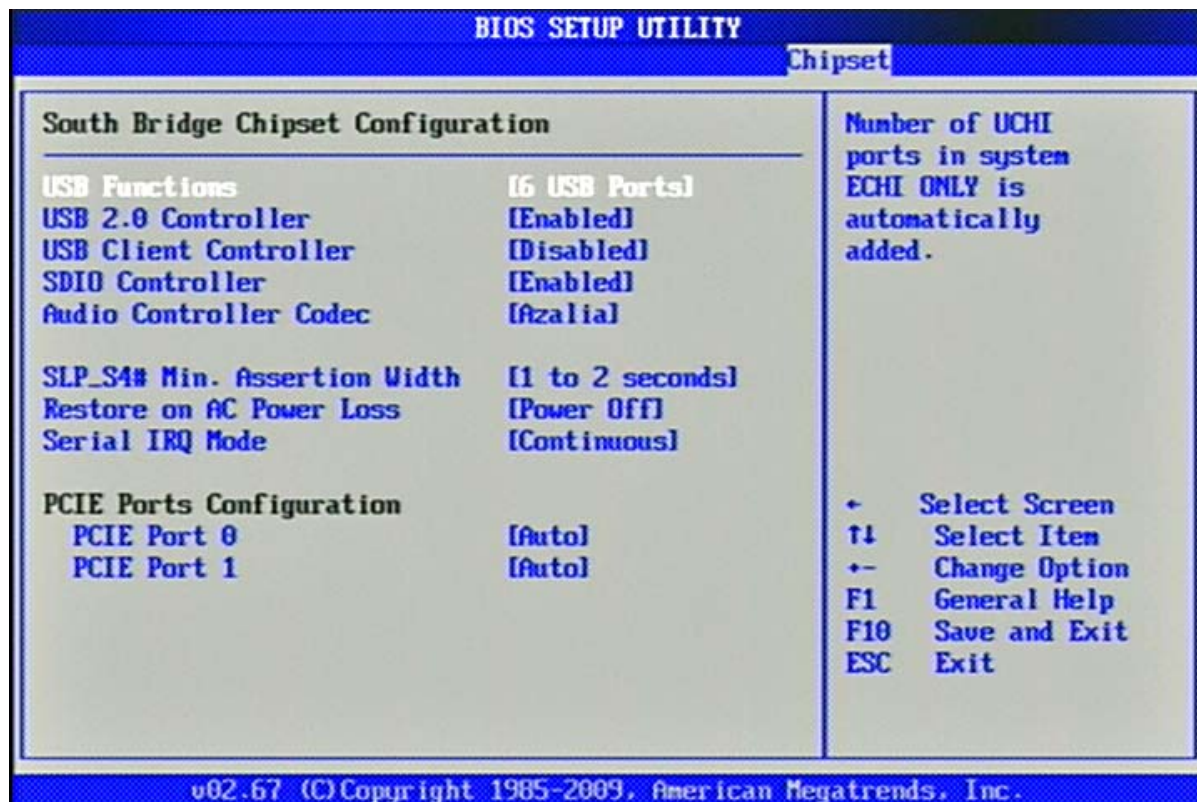The choice: Auto, Forced Scaling, Disabled.

Flat Panel Type

The choice: 640x480 (generic), 800x600 (generic), 1024x768 (generic), 1200x1024.

DPST Control

The choice: VBIOS Default, DPST Disabled, DPST Enabled at Level 1, DPST Enabled at Level 2, DPST Enabled at Level 3, DPST Enabled at Level 4, DPST Enabled at Level 5.

South Bridge Configuration

USB Functions

This setting specifies the function of the onboard USB controller.

The choice: Disabled, 2 USB Ports, 4 USB Ports, 6 USB Ports.

USB 2.0 Controller

Set to [Enabled] if you need to use any USB 2.0 device in the operating system that does not support or have any USB 2.0 driver installed, such as DOS and SCO Unix.

The choice: Enabled, Disabled.

USB Client Controller

The choice: Enabled, Disabled.

SDIOController

The choice: Enabled, Disabled.

Audio Controller Codec

The choice: Auto, Azalia, Disabled.

SLP_S4# Min. Assertion Width

The choice: 4 to 5 seconds, 3 to 4 seconds, 2 to 3 seconds, 1 to 2 seconds.

Restore on AC Power Loss

This item allows user to configure the power status of using ATX power supply after a serious power loss occurs.

The choice: Power Off, Power On, Last State.
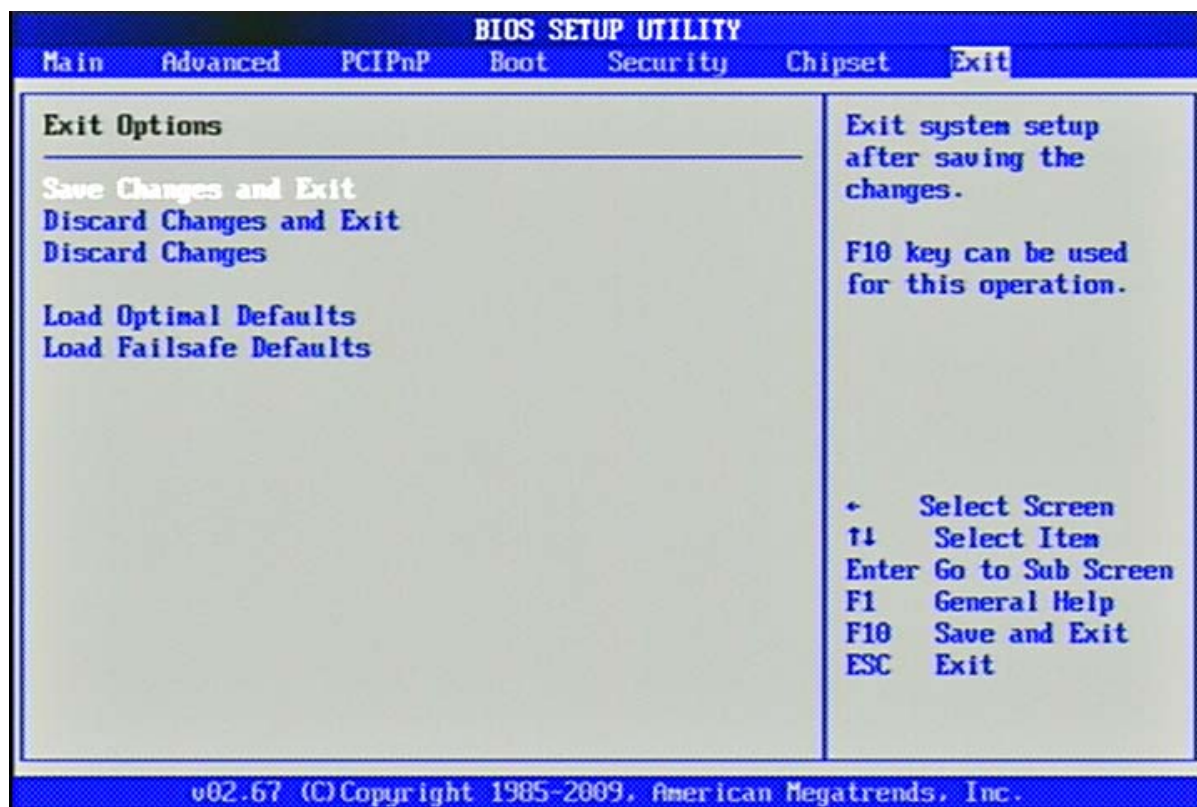
Serial IRQ Mode

The choice: Continuous, Quiet.

PICE Port 0/1

The choice: Auto, Enabled, Disabled.

4.8 Exit

This menu allows you to load the BIOS default values or factory default settings into the BIOS and exit the BIOS setup utility with or without changes.

Exit Saving Changes

Exit System Setup and save your changes to CMOS. Pressing <Enter> on this item asks for confirmation: Save changes to CMOS and exit the Setup Utility.

Discard Changes and Exit

Abandon all changes and exit the Setup Utility.

Discard Changes

Abandon all changes and continue with the Setup Utility.

Load Optimal Defaults

Use this menu to load the default values set by the SBC manufacturer specifically for optimal performance of the SBC.

Load Failsafe Defaults

Use this menu to load the default values set by the BIOS vendor for stable system performance.

Chapter 5
Troubleshooting

This chapter provides a few useful tips to quickly get PEB-2739I running with success. As basic hardware installation has been addressed in Chapter 2, this chapter will primarily focus on system integration issues, in terms of BIOS setting, and OS diagnostics.

5.1 Hardware Quick Installation

DC 12V Power Input
PEB-2739I supports DC12V input only(J21).
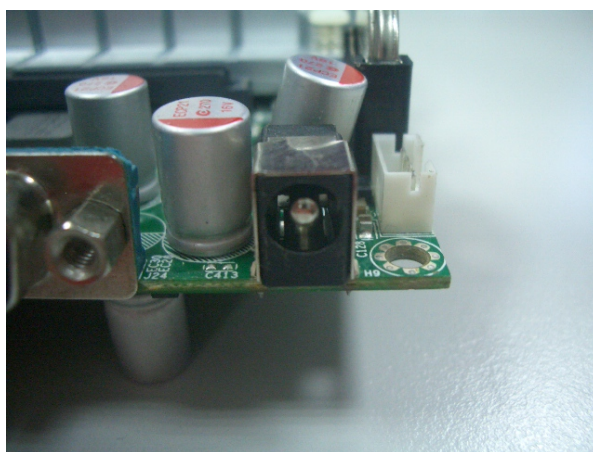
5.2 BIOS Setting

It is assumed that users have correctly adopted modules and connected all the device
cables required before turning on ATX power. 200-pin DDR2 SO-DIMM, keyboard, mouse, SATA hard disk, CF connector, VGA connector, device power cables, ATX accessories are
good examples that deserve attention. With no assurance of properly and correctly accommodating these modules and devices, it is very possible to encounter system failures that result in malfunction of any device.

To make sure that you have a successful start with PEB-2739I, it is recommended, when going with the boot-up sequence, to hit "DEL" key and enter the BIOS setup menu to tune up a stable BIOS configuration so that you can wake up your system far well.

Loading the default optimal setting

When prompted with the main setup menu, please scroll down to "**Restore Defaults**", press "Enter" and "Y" to load in default optimal BIOS setup. This will force your BIOS setting back to the initial factory configuration. It is recommended to do this so you can be sure the system is running with the BIOS setting that Portwell has highly endorsed. As a matter of fact, users can load the default BIOS setting any time when system appears to be unstable in boot up sequence.

Auto Detect Hard Disks

In the BIOS => Standard CMOS setup menu, pick up any one from Primary/Secondary Master/Slave IDE ports, and press "Enter". Setup the selected IDE port and its access mode to "Auto". This will force system to automatically pick up the IDE devices that are being connected each time system boots up.

Improper disable operation

There are too many occasions where users disable a certain device/feature in one application through BIOS setting. These variables may not be set back to the original values when needed. These devices/features will certainly fail to be detected.

It is also very common that users would like to disable a certain device/port to release IRQ resource. A few good examples are

A quick review of the basic IRQ mapping is given below for your reference.

IRQ#	Description
IRQ #0	System Timer
IRQ #1	Keyboard Event
IRQ #2	Usable IRQ
IRQ #3	COM2
IRQ #4	COM1
IRQ #5	Usable IRQ
IRQ #6	Diskette Event
IRQ #7	Usable IRQ
IRQ #8	Real-Time Clock
IRQ #9	Usable IRQ
IRQ #10	Usable IRQ
IRQ #11	Usable IRQ
IRQ #12	IBM Mouse Event
IRQ #13	Coprocessor Error
IRQ #14	Hard Disk Event
IRQ #15	Usable IRQ

It is then very easy to find out which IRQ resource is ready for additional peripherals. If IRQ resource is not enough, please disable some devices listed above to release further IRQ numbers.

System Memory Address Map

Each On-board device in the system is assigned a set of memory addresses, which also can be identical of the device. The following table lists the system memory address used for your reference.

Memory Area	Size	Description
0000 – 0XXX	XXK	XXX
0000-003F	1K	Interrupt Area
0040-004F	0.3K	BIOS Data Area
0050-006F	0.5K	System Data
0070-0E2E	54K	DOS
0E2F-0F6B	5K	Program Area
0F6C-9FBF	577K	【Available】
First Meg	**-- Conventional memory end at 639K --**	
A000-AXXX	XX K	XXX
9FC0-9FFF	1K	Extended BIOS Area
A000-AFFF	64K	VGA Graphics
B000-B7FF	32K	Unused
B800-BFFF	32K	VGA Text
C000-CE5F	57K	Video ROM
CE60-EFFF	134K	Unused
F000-FFFF	64K	System ROM

Interrupt Request Lines (IRQ)

Peripheral devices can use interrupt request lines to notify CPU for the service required.　The following table shows the IRQ used by the devices on board.

IRQ#	Current Use	Default Use
IRQ 0	System ROM	System Timer
IRQ 1	System ROM	Keyboard Event
IRQ 2	【Unassigned】	Usable IRQ
IRQ 3	System ROM	COM2
IRQ 4	System ROM	COM1
IRQ 5	【Unassigned】	Usable IRQ
IRQ 6	System ROM	Diskette Event
IRQ 7	Unused	Usable IRQ
IRQ 8	System ROM	Real-Time Clock
IRQ 9	【Unassigned】	Usable IRQ
IRQ 10	【Unassigned】	Usable IRQ
IRQ 11	【Unassigned】	Usable IRQ
IRQ 12	System ROM	IBM Mouse Event
IRQ 13	System ROM	Coprocessor Error
IRQ 14	System ROM	Hard Disk Event
IRQ 15	【Unassigned】	Usable IRQ