APV25 Power Consumption

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1. Introduction

In this note I draw together the APV25 power consumption information in one place, with links to documents where it has been discussed previously, to answer questions that sometimes arise as to what the power consumption actually is, and how it can change depending on external conditions.

The APV power consumption depends on the I2C bias parameters programmed and the recommended values have been specified for some time, for room temperature operation and at lower temperatures. Values in this note result mainly from single chip measurements, but have been found consistent with measurements made on a few detector modules for the cold operation studies.

summary of main information

Based on information in the user manual [1], adjusted to take into account changes resulting from the decision to power the inverter stage from the V250 rail using a 50 ohm resistor (explained in [2] and discussed further later) the currents drawn from the V250 and V125 rails are:

I250: 116 ± 12 mA and **I125: 52 ± 5 mA**

These numbers assume ISHA=30 and VPSP is set to position the analogue baseline at 25% of the digital header range. The tolerances reflect ± 10% chip-to-chip variations [2]. The effects of various conditions on the supply currents are summarised in the table below and then discussed in more detail in section 2.

condition	I250 effect	I125 effect	comment
temperature	no change	no change	assumes bias parameters are adjusted appropriately for operating temperature
radiation	~ no change	no change	small increases in I250 at the per cent level to compensate for slight gm reduction affecting pulse shape
VPSP baseline adjustment	-11% baseline -> min. +7%, baseline -> 50% + 28%, baseline -> max.	no change	taking nominal position to be 25% of digital header range
pulse shape tuning	-7% -> +7%	no change	tuning ISHA in the range 0 – 100 about mid value 50
trigger rate	no change	no change	power consumption drops slowly if chip not triggered at all
power supply	+7% at V250=2.7 V	no change	analogue currents are insensitive to supply voltages, but not digital

power supply contingency

The baseline adjustment has the most significance when considering power supply operating margins. If it is necessary to scan the baseline through its full range then large fluctuations in I250 will result. One way to avoid this is to perform such a scan one chip per hybrid, or even one chip

per power group, at a time. Alternatively, power increases in channels that are scanned can be offset by disabling chips or groups of chips on the same power bus (the bias on/off bit in the APV mode register reduces power by switching off the analogue circuitry).

If a more permanent adjustment to the baseline is required for operational reasons then sufficient contingency will be needed in the power supplies. For example to adjust the baseline for all chips from 25% to 50% of the digital range a contingency of 7% would be required.

Pulse shape tuning will be required occasionally, but the need to provide any significant contingency in the power supplies can be avoided, in the same way as the baseline scan operation, by either limiting the numbers of chips being tuned at any one time, or by switching off groups of chips while others on the same power bus are tuned.

Power supply effects are included in the table, since there will be power droops along conductors feeding many modules, but extra digital current consumed by modules seeing higher voltages closest to the power supplies will be offset by those seeing lower voltages further away, so it is not clear that any contingency is required here.

From the APV perspective alone at least 10% contingency in the I125 and I250 power supply currents should be allowed for chip-to-chip variations, since groups of chips sharing the same power bus may all originate from the same wafer and hence may all have larger than nominal consumption. A further 10% should be sufficient to allow adjustment or optimisation of operating conditions, such as a baseline adjustment. If larger margins are possible, without significant penalties, then all the better.

2. More detailed discussion of power consumption effects

previous information

A brief account of the nominal APV25 power consumption, with links to some explanatory information, has been available for some time [1]. The nominal current consumption is quoted in the user manual [2], table 12, for an external reference current tuned to 128 μA. In [1] it is explained that the power consumption changed because of subsequent decisions to power the inverter stage via a 50 ohm resistor from V250. In the user manual the original currents are I250 = 90 mA and I125 = 65 mA, but supplying the inverter stage via a 100 ohm resistor to cure the hybrid stability problem transfers 13 mA from I125 to I250, and reducing the 100 ohms to 50 to help with the HIPs behaviour doubles this transferred current to 26 mA. Consequently the nominal “user manual” current consumption/rail becomes I250 = 116 mA and I125 = 52 mA. The GND rail therefore sinks 168 mA, the sum of I250 and I125.

Note that these numbers are not explicitly stated in [1], where only the power is discussed.

The above numbers assume values for variable parameters ISHA and VPSP. ISHA is one of the parameters used to tune the pulse shape and is taken to be the room temperature value of 30. VPSP sets the analogue baseline position which has to be tuned on a chip-to-chip basis. The baseline position for the above currents is not explicitly stated in the user manual, but the numbers are consistent with what I have measured for individual chips where the baseline is positioned at 25% of the digital header range.

There will be some chip-to-chip variation, assuming that the I2C bias parameters are not tuned for individual chips in the system. In [2] it is explained that a reasonable figure for the tolerances on the supply currents is ± 10%. So I250 = 116 ± 12 mA and I125 = 52 ± 5 mA as stated earlier.

temperature effects

The temperature at which the chip is operated has an effect on the power consumption because the on-chip master reference current has a temperature dependence. This has been studied in some detail for TIB, TOB and TEC modules and the results can be found in [3-5]. The bottom line here is that the bias settings must be chosen to suit the operating temperature, and if the temperature is reduced the settings must be adjusted to maintain the same power consumption. To avoid unnecessary excess power consumption as the system cools down, the bias parameters can be programmed to the values appropriate for the target temperature before cooling commences.

radiation effects

Many chips have now been sampled from the production wafers and irradiated to 10 Mrad levels with X-rays. Figure 1 shows some results from production lots 9 – 16 where very little difference in the current consumption before and after irradiation and annealing can be seen. Actual current levels can be seen to be consistent with expectations.

effect of baseline change (VPSP)

The analogue baseline position can be adjusted using the VPSP bias setting, and this has a significant effect on the power consumption, so has to be set with care. Figure 2 shows a measurement on a 4 APV TIB module from [3]. The red curve shows the average baseline level dependence on VPSP setting, where VPSP is scanned in a range that positions the baseline between the minimum (where the baseline is at the digital header '0' level) to a level beyond the digital header '1' level. The blue curve shows the effect on I250 for the whole module. Changing the baseline from 25% to 50% of the digital header range, gives a change in I250 from 470 mA to 500 mA. This corresponds to an increase of ~ 7%.

Using the data from figure 2, if VPSP were scanned over its full possible range then the change in I250 would be from ~ 420 mA to ~600 mA, a percentage change from the 25% nominal position of - 11% to + 28%. Note that not all APVs per module (or per power grouping) have to be scanned simultaneously

power variation during pulse shape tuning

If all APVs in the system were to be loaded with identical I2C parameters, including the pulse shape tuning parameters ISHA and VFS, the uniformity of pulse shapes that would result is actually quite good [6]. Nevertheless to obtain the best possible performance tuning will be required. How often it will be considered necessary to perform this operation can be debated, but what is clear is that power variations during tuning can be minimised by not tuning all APVs at once (e.g. one APV at a time on an individual hybrid, or even one at a time on an individual power grouping, could be considered), but this does implications for how long it will take to tune the whole tracker.

ISHA is the parameter that will affect the current consumption during pulse shape tuning. The bigger the value, the larger the current consumption. During measurements of module operation in the cold [3 - 5] it was found that values of 50 (decimal) or less were appropriate for operation at CMS temperatures of around -10 degrees for the TIB, TOB and TEC modules studied. Figure 3 shows a measurement on an individual chip of the I250 current dependence on ISHA setting. The current varies with ISHA by ~ 0.16 mA / ISHA unit. If the tuning range is constrained to values ± 50 around a mid-point value of 50 (so in the range 0 – 100) then the I250 current will vary by ± 8 mA.

This is not quite the whole story since varying ISHA also affects the DC level at the shaper output, which in turn affects the analogue baseline position, and hence the power consumption due to this

effect. To avoid this the baseline position should be monitored and adjusted to maintain it at the same level during the pulse shape tuning exercise. The data in figure 3 were measured after performing this correction.

trigger rate

There is no significant change in power consumption depending on trigger rate, up to rates in excess of 100 kHz. There will be more digital activity on the chip when the pipeline is being read out through the APSP but the readout speed is slow here. One might have expected an increase due to the digital activity in the output mux, but this has been designed so that only the last 4:1 stage of the mux runs at the full 20 MHz rate.

It has been noted that if the chip is not triggered at all then over a relatively long period of time (values from several seconds – several minutes have been observed) the power consumption drifts down to a minimum. This minimum actually corresponds to the same power consumption that you get if you set the analogue baseline to the minimum value (VPSP large). When the chip is untriggered the sample/hold switch transistor at the mux input remains permanently open (also the APSP core amplifier, which has only capacitive feedback, never gets reset), and the mux input storage capacitor can then drift due to DC leakage. It is probably a good thing that the power consumption drifts down, rather than up, but one consequence is that as soon as a trigger is applied there will be a sudden increase in power when the sample/hold switch operates. This will occur for all chips in the system at the same time. This can be avoided by ensuring that the trigger rate never drops to zero.

power supply voltage effects

The internally generated on-chip master reference current is provided by a circuit which, although temperature sensitive, is supply voltage independent. This means that the analogue current consumption will be supply independent but the digital consumption will not. Increasing the V125 and V250 from their nominal 1.25/2.50 levels to 1.35/2.70 (2.7 is the maximum voltage recommended for the process), I250 increases by 7%, I125 remaining unchanged.

module measurements

For comparison with the expected supply currents based on individual chip measurements it is worth including here some measurements made on detector modules. In the table below are average values (the average of measurements at all temperatures) of I250 and I125 measured on individual TIB, TOB and TEC modules during the cold operation studies [3 - 5]. Each module had 4 APVs. When measuring the currents on modules it is not possible to separate out the APV supply currents from the other chips on the modules (APVMUX, PLL and DCU), which also draw current from the V250 rail. So I250 currents are higher than would be predicted for the APVs alone, and this is evident in the table. The TIB module has a noticeably lower consumption, but ~ 4 mA of the higher I250 currents drawn by the TOB and TEC modules can be attributed to the higher values of ISHA required for these modules which had larger, higher capacitance, sensors. The I125 values are quite consistent with expectation, although slightly high for the TEC module.

	TIB module	TOB module	TEC module
I250 / APV	120 mA	132 mA	135 mA
I125 / APV	55 mA	52 mA	58 mA

3. References

[1] APV user guide 2.2:

http://www.te.rl.ac.uk/med/projects/High_Energy_Physics/CMS/APV25-S1/pdf/User_Guide_2.2.pdf

[2] APV power consumption note:

http://www.hep.ph.ic.ac.uk/~dmray/pdffiles/APV25%20Power%20Consumption.pdf

[3] TIB module cooling note:

http://www.hep.ph.ic.ac.uk/~dmray/pdffiles/cold_APV_params.pdf

[4] TOB module cooling note:

http://www.hep.ph.ic.ac.uk/~dmray/pdffiles/TOB_cold_APV_params.pdf

[5] TEC module cooling note:

http://www.hep.ph.ic.ac.uk/~dmray/pdffiles/TEC_cold_APV_params.pdf

[6] Final Results from the APV25 Production Wafer Testing
M.Raymond, R.Bainbridge, M.French, G.Hall, P.Barrillon
Proceedings of 11th Workshop on Electronics for LHC Experiments, Heidelberg (Germany), CERN/LHCC/2005-038 (2005) 453-457.

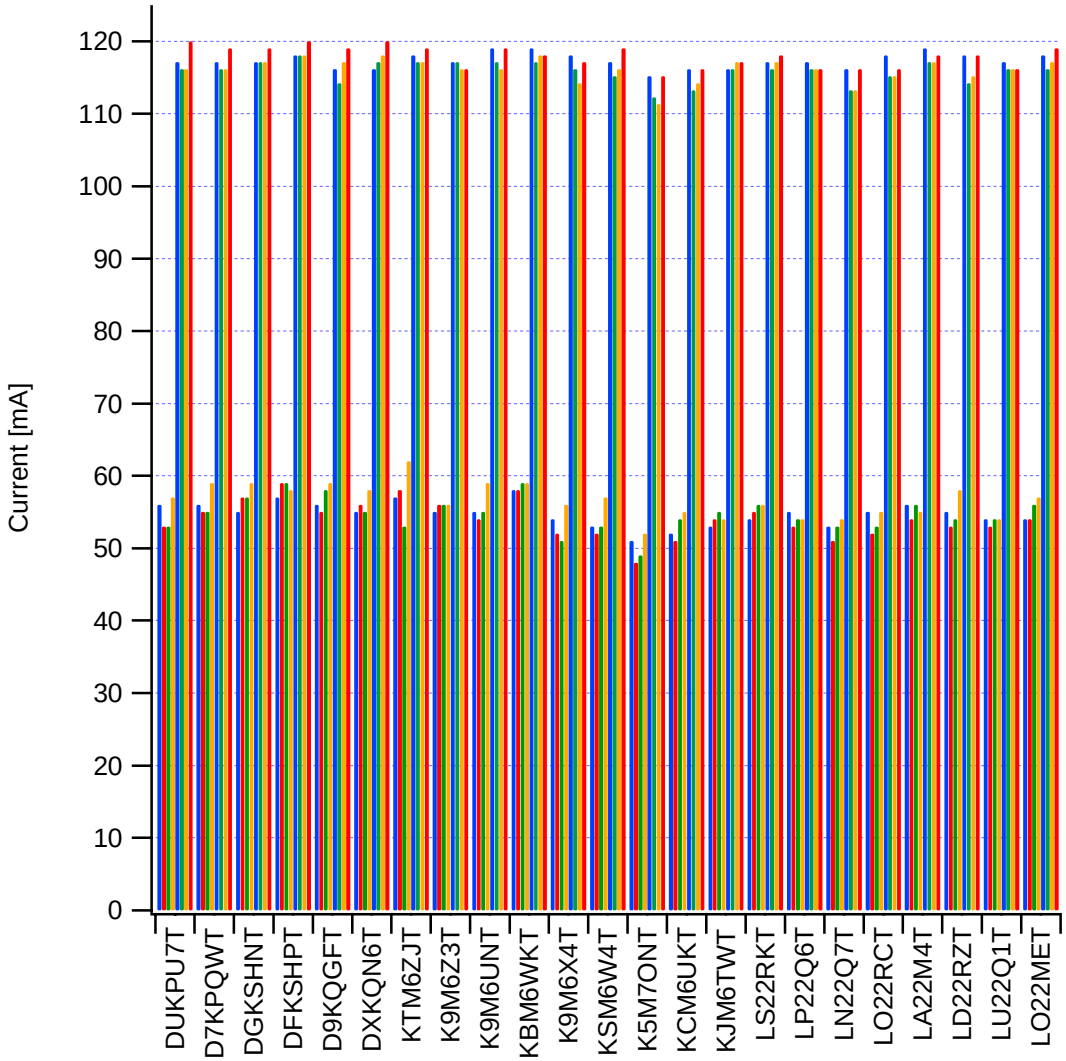

Figure 1. I250 and I125 current consumption of 23 APV25 chips sampled from production wafer lots 9 - 16. Blue, red, green and orange colours refer respectively to measurements before and after irradiation to 10 Mrads and before and after annealing. Higher bars correspond to I250, lower to I125.

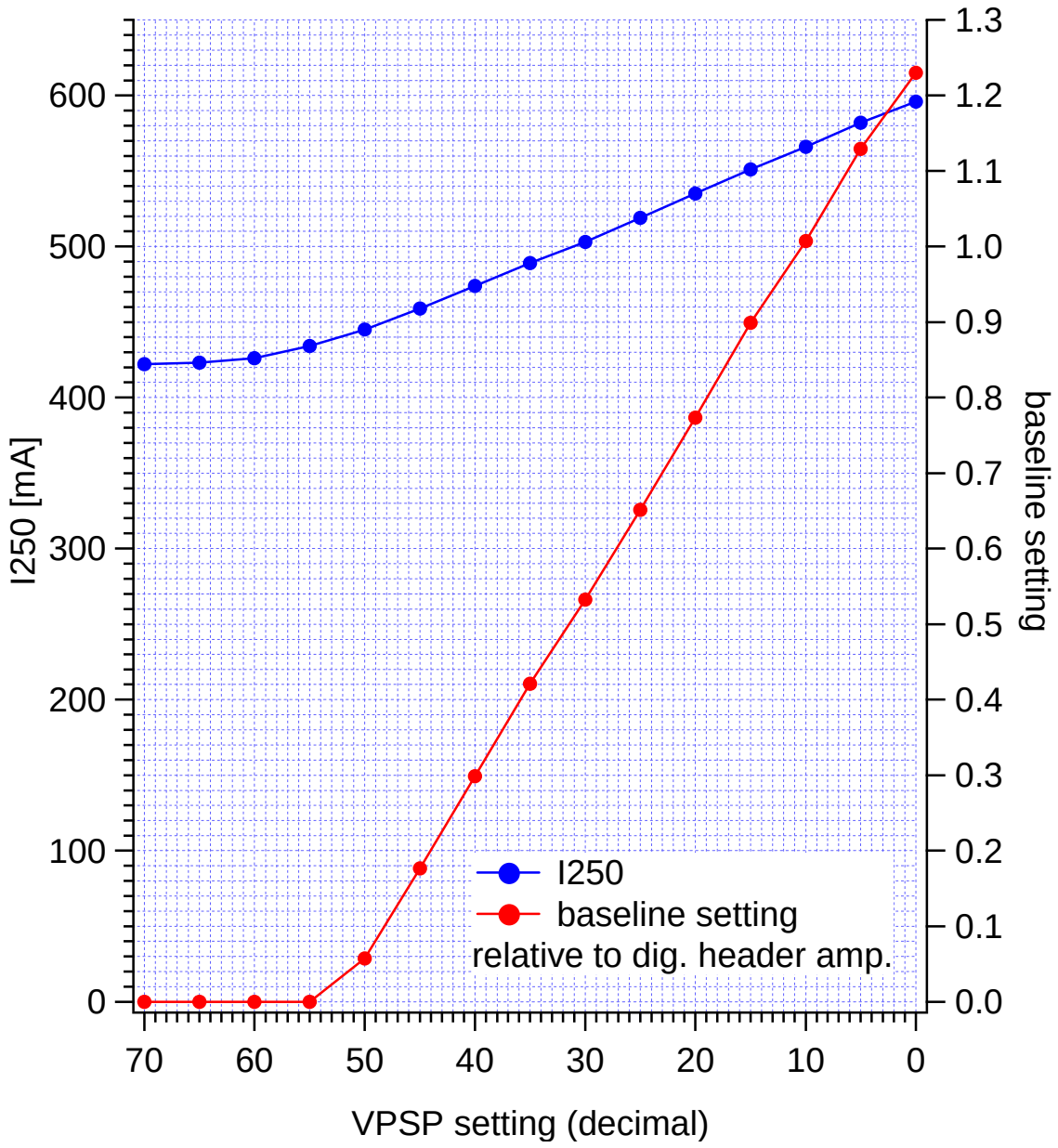

Figure 2. VPSP dependence of total I250 current and analogue baseline position measured at +30 degrees, measured on a 4 APV TIB module. The analogue baseline position is normalised to the digital header amplitude (e.g. value of 0 means average channel pedestals at digital '0' level, value of '1' means average channel pedestals level with maximum digital header amplitude). Note that I250 includes contributions from DCU, APVMUX and PLL chips which cannot be measured separately.

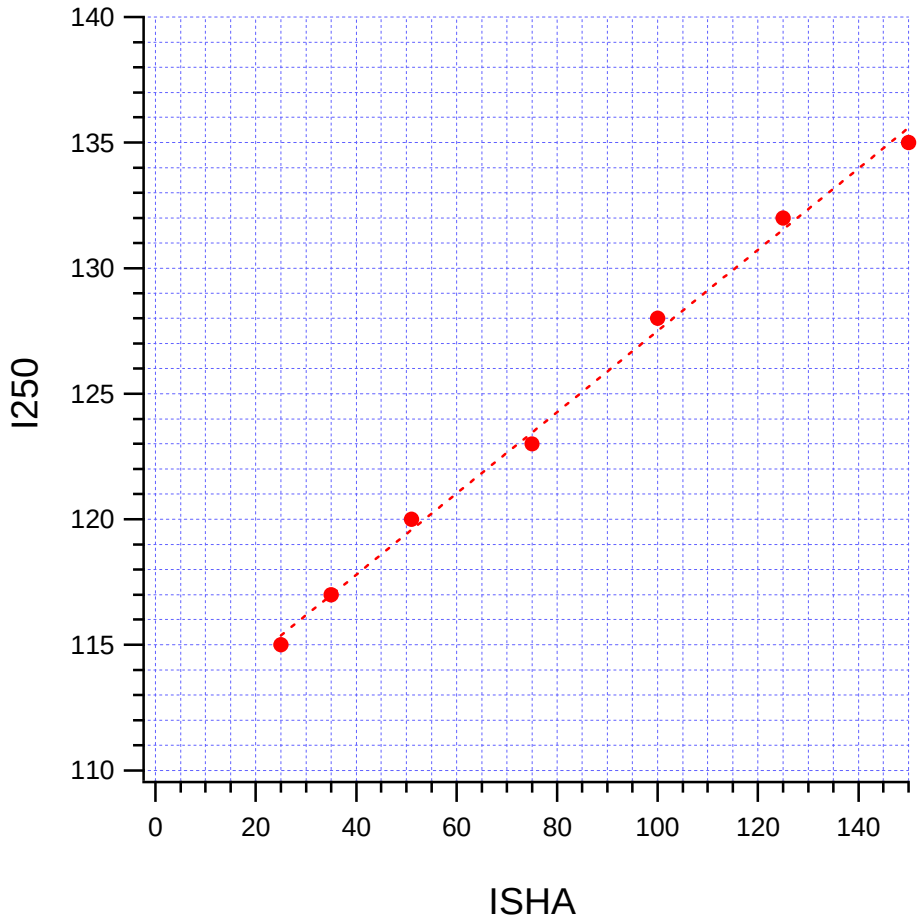

Figure 3. single chip measurement of I250 dependence on ISHA setting. The analogue baseline does change as ISHA is adjusted, so VPSP was altered at each measurment point to maintain the baseline position at approximately the same level.