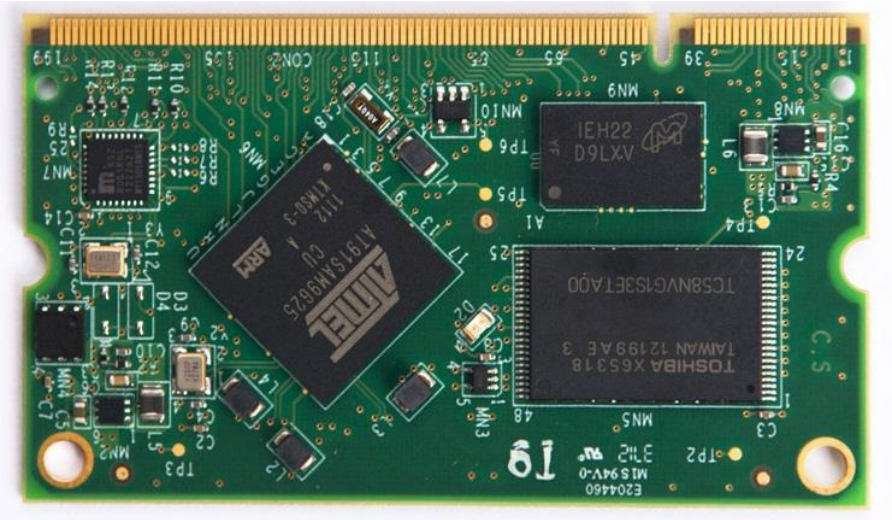
AT-901

ARM9 System on Module



Hardware user manual

Revision 1.0

SHIRATECH

Contents

1. Introduction

The AT- 901 is an industrial embedded System-On-Module using the latest ARM and Linux technology. It is designed to serve as the controller and processing building block for embedded devices in applications such as medical devices, communications and industrial automation. The module can be provided with several levels of software integration starting from an 'out of the box' Debian Linux and up to a full software solution.

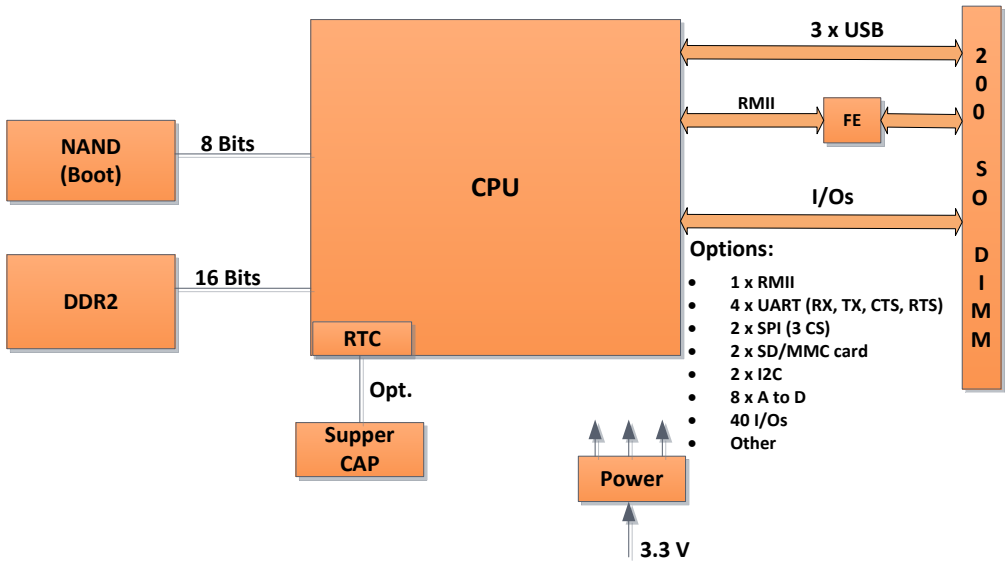
Features:

- Using the SAM9Gx@400Mhz from Atmel offering a unique combination of an ARM9 processor combined with DDR2 for both enhanced performance and low cost solution. The card offers two processor types :
  - AT91SAM9G25
  - AT91SAM9X35 – for touch screen and CAN interface support
- RAM - 128 MB DDR2
- Flash - 256 MB NAND Flash
- A large variety of internal interfaces over a 200 pin SO-DIMM.

2. AT-901 internal hardware description

2.1. Block Diagram

The following figure describes the AT-901 block diagram



AT-901 Block Diagram

The AT-901 block diagram includes:

- AT-901 system.
- AT-901 FE interface.
- AT-901 power & Reset.
- AT-901 extension connector.

The following paragraphs describe each part of the system in details.

2.2. AT-901 System

2.2.1. ARM-926EJ-S Processor

The AT-901 uses Atmel's SAM-9 ARM9 based series. The SAM-9 is a family of processors which uses an enhanced version of the ARM-926EJ-S processor.
The SAM-9 support different flavors e.g. Single/dual Ethernet, enhanced graphic accelerator, LCD and more. All those flavors are footprint compatible and can be supported by the AT-901 module.
The SAM-9 main features are:

- 400 MHZ core frequency (400 MIPS)
- 16 Kbytes data and instruction cache
- System running at 133 MHz
- Integrated RTC, POR and WDT
- Low power mode
- Multiplex peripherals bus
- 217 pins BGA package

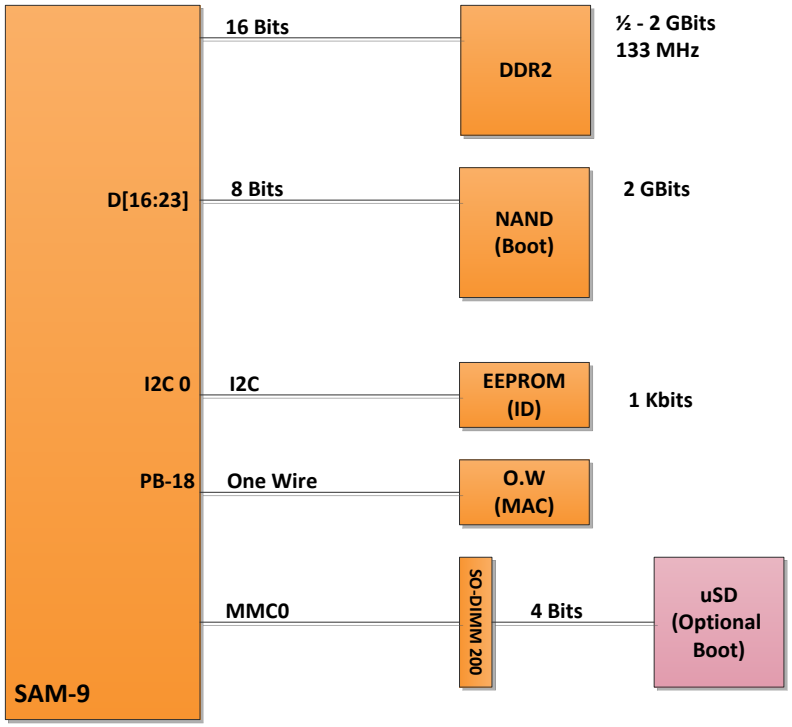
For full data sheet, use the following links:

http://www.atmel.com/devices/SAM9G25.aspx?tab=documents

http://www.atmel.com/devices/SAM9X35.aspx?tab=documents

2.2.2. Memories

The AT-901 includes several types of memory for supporting booting, program execution and ID. The following figure describes the memories available on the AT-901.



AT-901 Memory configuration

2.2.2.1. DDR2

The AT-901 a incorporate a 16 bits wide DDR2 for its program execution. The following are the DDR2 main features:

- Up to 2GBits.
- 16 bits data bus
- Support for 8 banks
- Up to 133 MHz clock
- Uses CS1
- ODT not supported
- OCD not supported
- The default configuration includes 128M bytes, it can be enlarge to 256M bytes (ordering option).

2.2.2.2. NAND flash

The AT-901 incorporates 8 bits wide NAND flash. The NAND is an SLC raw data NAND. It stores the AT-901 second level boot in a secured sector and 2 last versions of the application SW.
It uses data signals D [16-23]. The main features of the NAND flash:

- 8 bits data bus.
- Up to 2Gbits memory volume

- CS3
- Uses data bits D[16-23]
- 3.3V interfaces.
- The default configuration is 256M bytes

Note – The SOM's NAND flash is from Toshiba. Any assembled flash need to be either from Toshiba or to support the ONFI (JEDEC) standard.

2.2.2.3. Micro SD

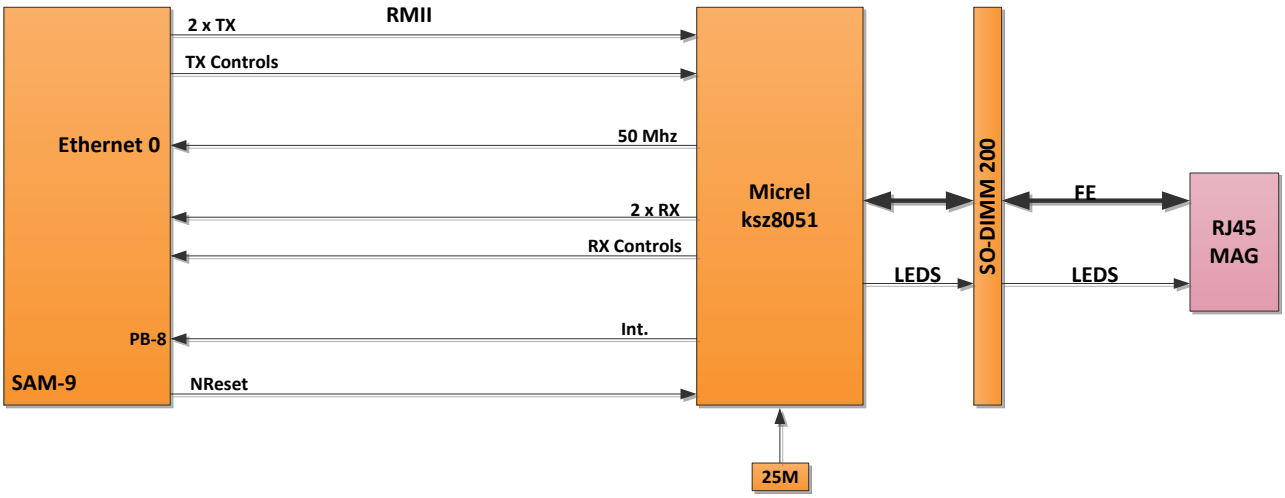
The AT-901 has an option to run the software from a Micro SD. It uses MC0 of the PROCESSOR with up to 4 data lines. The Micro SD is connected through the SO-DIMM 200 connector.

2.2.2.4. Other memory devices

- A one wire device which holds a build in unique ID , along with board information.
- The AT-901 has an EEPROM option - Currently not available.

2.3. Build in Ethernet interface

The AT-901 supports a build in Fast Ethernet interface, including a build in physical layer transceiver (PHY). The transceiver uses an RMII interface to interconnect with the processor's Ethernet port 0. The following figure describes the Fast Ethernet interface.



Fast Ethernet RMII Interface

The RMII interface is running at 50 MHz. The 50 MHz clock is generated by the Fast Ethernet PHY. PB-8 of the PROCESSOR uses as an interrupt input for the Fast Ethernet PHY.

The Fast Ethernet PHY analog signals (TX+/-, RX+/-) are connected the SO-DIMM edge connector. Two led signal from the FE PHY are also connected to the SOM edge connector.

Notes:

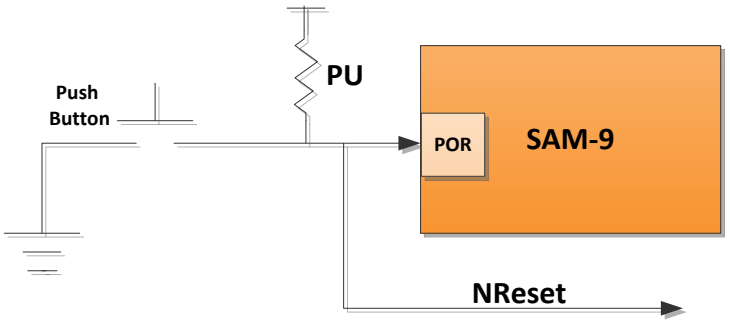
- The FE interface has a separate power plane that is separated from the common digital plane. It sources from the edge connector (VDDANA).
- An additional Ethernet interface is available using the X25 version of the processor. The interface available on the edge connector for the second Ethernet port will be RMII.

2.4. Power & Reset

2.4.1. Reset

The AT-901 integrates an internal Power-On-Reset (POR) controller. It monitors the power and drive the internal and external reset.
The NRST I/O can be used as an input for resetting the processor. In that case the external reset should be an open drain solution asserted only when a reset action is required (see the figure below).
The NRST can be used also as a programmable length reset for the carrier board (between 60 µs and 2 seconds).

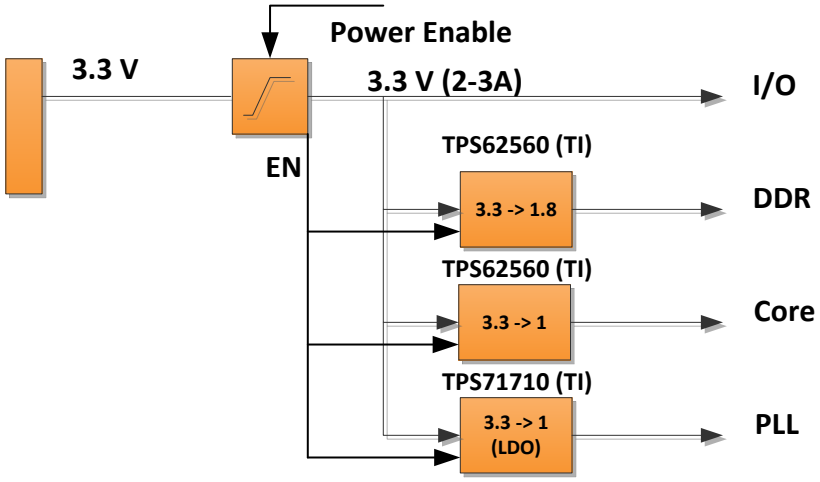
Note: A pull up resistor for the NRST is assembled on the carrier board.



Reset mechanism

2.4.2. Power

The power to the AT-901 module is coming from SO-DIMM 200 edge connector. The main power is a 3.3V +/- 5% which generates all other powers.



AT-901 Power Hierarchy

The available power levels used are as follows:

- The 1V is used to power the processor internal core and the
- 1.8V is used for to power the DDR2 interfaces.
- All I/O signals are fed from the 3.3V power supply.

2.4.2.1. Power signals on the SO-DIMM connector

- The power signals VDDIOP0 and VDDNF should be connected directly to the 3.3V power plane.
- VDDANA, power for Analog interfaces, should be connected to the 3.3V plane using a filter.
- The VBAT pin on the SO-DIMM connector should be either connected to an external battery located on the carrier board or shortens to 3.3V power source.
- ADREF is the A/D reference voltage, if not used connect directly to 3.3V

2.4.2.2. Backup battery

The AT-901 has an option for build in backup power source for the Real-Time-Clock connected to the VDDBU pin of the processor. The backup power device monitors the main power level and when it drops below a configurable threshold it switch to its internal power source. On normal operation the device charges the internal power source using the main power input.
When installed, the battery supports an approximately 1 hour work of the RTC and backup section of the processor when the main power fails. (Contact sales@shiratech.com for more information).

Note: When using the option of a SoM with a build in battery the VBAT pin on the SO-DIMM connector should be left un-connected.

The following figure describes the AT-901 backup power:

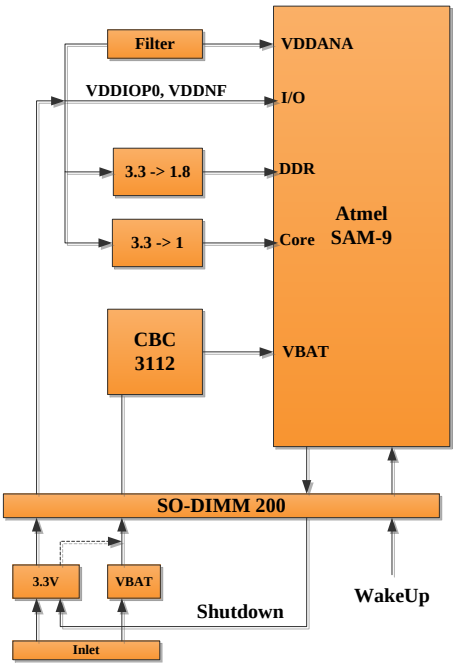


Figure 1 - AT-901 Backup Power

2.5. Extension connector

The AT-901 support varieties of interfaces through the SO-DIMM 200 edge connector. Some of the interfaces are multiplexed with other interfaces on the PROCESSOR processor and thus not all options are available at the same time
The options are preconfigured by the software. The main supported interfaces are:

- Up to 3 USART supporting TX, RX, CTS and RTS
- Up to 3 UART supporting TX, RX only(one of them is a debug port as well)

- Up to 2 Fast Ethernet port(an additional Ethernet port is available only with the X25 version – different ordering option)
  - Port 0 – TX+/-, RX+/-
  - Port 1 - RMII
- Up to 2 SPI interfaces with 2 Chip Select each.
- Up to two I2C interfaces
- Up to 2 SDIO/MMC ports supporting 4 data bits each
- Up to 6 A to D convertors with 10 bits resolution and 100 KHz sampling rate
- Other optional interfaces are:
  - LCD monitor(X35 only)
  - Touch screen(X35 only)
  - Audio.
  - CAN interface (X35 only)
  - Others
- GPIOs – any un used pin can be configured as a GPIO for various control and monitor functions

3. Hardware Software interface

3.1. Hardware Configuration

During power up some I/O bits status is latch to configure the CPU. The following table describes the bits and their functionality.

Signal	Description	Default
BMS (SOM)	0 – Booting from CS0 using parallel NOR 1 – Booting from internal ROM	The AT-901 is always boot from the internal ROM.
JTAG Select (Carrier)	0 – Normal JTAG chain 1 – ICE mode	According to the pin connected to the connector
ETH0 Address	The access address to the Ethernet 0 PHY	0001
EEPROM I2C	The access address to the I2C EEPROM	1010001

Table 1 – HW Configured After Reset

3.2. Interrupt & I/O Table

The following table describes the AT-901 dedicated I/O configuration. Some of the configurations are valid only when the relevant interfaces are assembled e.g. Ethernet and USB. When not assembled these pins can be used as I/Os.

Signal	I/O	Description	Remarks
E0 INTR	PB-8	Ethernet 0 interrupt	Active Low
E1 INTR	PC-26	Ethernet 1 interrupt	Active Low
MCI0 CD	PD-15	uSD card detect	0 – Card in 1 – No card
MCI1 CD	PD-14	SD card detect	0 – Card in 1 – No card
VBUS Sense	PB-16	USB port A power sense	0 – No power sensed 1 – Power sensed
OverCur USB	PB-17	USB port A or Port B over current	Open Drain
EN5V HDA#	PD-18	USB port A power drive enable	0 – Enable 1 – Disable (Default)
EN5V HDB#	PD-19	USB port B power drive enable	0 – Enable 1 – Disable (Default)
EN5V HDC#	PD-20	USB port C power drive enable	0 – Enable 1 – Disable (Default)

Table 2 – Configured I/O and Interrupts

NOTE – More interrupts are available through the PROCESSOR I/O pins and can be configured according to the user application.

3.3. Booting Sequence

The AT-901 has 3 boot phases:

- First level boot loader running from internal ROM.
- Device configuration running from internal RAM.
- SW downloads from NVRAM (NAND or SD Card) to DDR2 and execution.

After POR the processor runs the "First Level Boot loader" program stored in its internal ROM. The program configures the SAM-9 clocks and looks for executable program in one of the non-volatile memories (See SAM-9 datasheet for a "valid" code for each of the optional memories).
The optional memories are:

- NAND (Default).
- Micro SD card (Carrier).
- Serial NOR (Carrier).

The following figure describes the optional boot memories and its priorities.

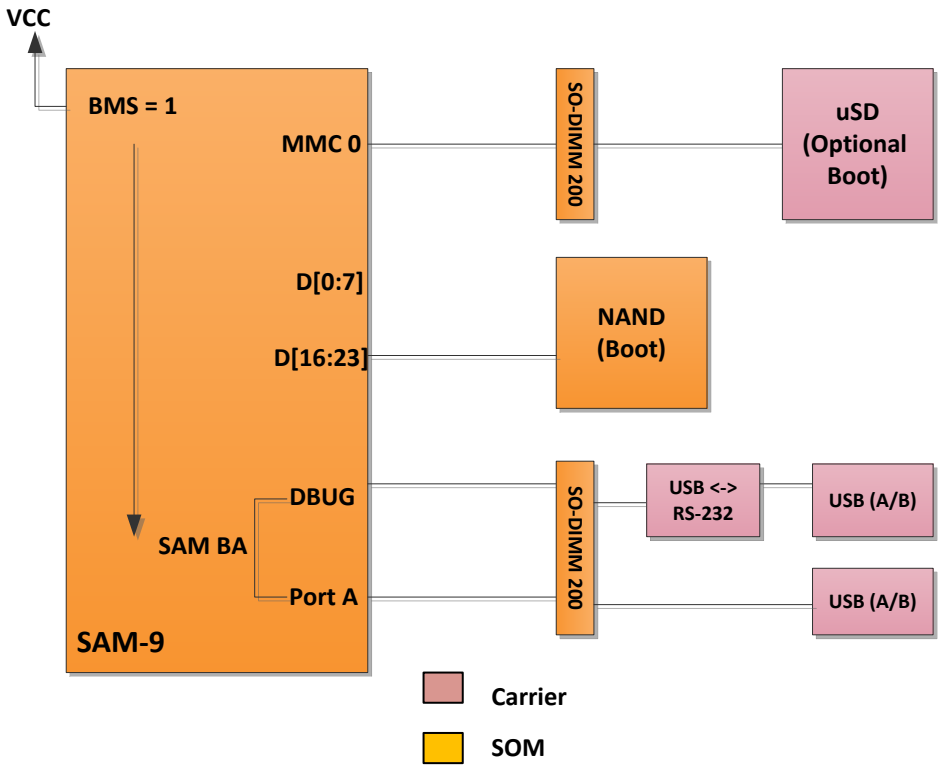


Figure 2 - Boot Sequancing Priority

If the "First Level Boot-Loader" doesn't find an executable program in one of the non-volatile memories, it configures the Debug port (RS-232) and the USB port (Port 0 as device) to wait for external program download from the PC.

For more information see the Atmel's boot sequencing chapter in the SAM-9 datasheet

3.4. Debug Options

The SOM has two options for debug:

- JTAG Connector
- Debug interface (PA-9, PA-10)

Both debug options are available on the SO-DIMM 200 edge connector.

3.4.1. JTAG Interface

A standard interface which can be used for the following options:

- Debug using off-the-shelf Atmel's ICE (Default).
- Standard JTAG emulation.

Choosing between the options is done by asserting the JTAGSEL signal available on the SO-DIMM edge connector.

3.4.2. Debug Interface

The SAM-9 integrates an internal debug controller with UART interface (TX and RX signals only).

3.5. Interfaces

3.5.1. Ethernet

The SAM9-G25/X35 support a single/dual Fast Ethernet interfaces. Each interface has its own MDC/MDIO controller.
The default PHY address is 0001 for both interfaces.
The MDC frequency is derived from the system clock and should not exceed 2.5MHz.

3.5.2. I2C

There are up to three I2C interfaces dependent on PIO utilization
The I2C main features are:

- One, Two or Three Bytes for Slave Address
- Sequential Read-write Operations
- Master, Multi-master and Slave Mode Operation
- Bit Rate: Up to 400 Kbits
- General Call Supported in Slave mode
- SMBUS Quick Command Supported in Master Mode
- Connection to DMA Controller (DMA) Channel Capabilities optimizes Data Transfers in Master Mode Only

Standard Compliances

I2C Standard	Atmel TWI
Standard Mode Speed (100 KHz)	Supported
Fast Mode Speed (400 KHz)	Supported
7 or 10 bits Slave Addressing	Supported
START BYTE(1)	Not Supported
Repeated Start (Sr) Condition	Supported
ACK and NACK Management	Supported
Slope control and input filtering (Fast mode)	Not Supported
Clock stretching	Supported
Multi Master Capability	Supported

Note: 1. START + b000000001 + Ack + Sr

3.5.3. USB

The AT-901 supports three 2.0 USB interfaces. Port A can be used as a Host or a Device interface and port B as a Host interface both support high speed operation and port C which support only full speed operation only (12Mbps).
The 5V power supply for the USB ports is SW Controlled and should be enable according to the application. When Port-A is used as a device (Configurable), the USB interface can sense if the Host device drives the USB power bus.
The following figure describes the USB interfaces.

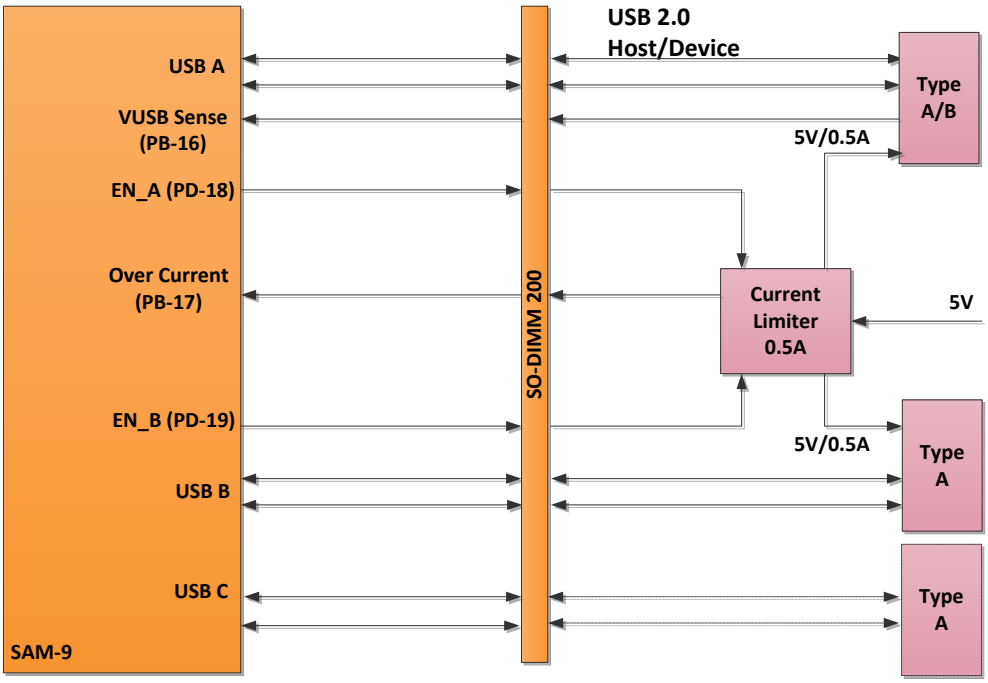


Figure 3 - USB interfaces

3.5.4. SPI

The Serial Peripheral Interface (SPI) circuit is a synchronous serial data link that provides communication with external devices in Master or Slave Mode. It also enables communication between processors if an external processor is connected to the system.
There are up to two SPI interfaces depending on configuration. Both interfaces are available on the SO-DIMM 200 connector.

3.5.5. USART

The Universal Synchronous Asynchronous Receiver Transceiver (USART) provides one full duplex universal synchronous asynchronous serial link. Data frame format is widely programmable (data length, parity, number of stop bits) to support a maximum of standards. The receiver implements parity error, framing error and overrun error detection. The receiver time-out enables handling variable-length frames and the

transmitter time guard facilitates communications with slow remote devices. Multidrop communications are also supported through address bit handling in reception and transmission.

3.5.6. UART

The Universal Asynchronous Receiver Transmitter features a two-pin UART that can be used for communication and trace purposes. Moreover, the association with two DMA controller channels permits packet handling for these tasks with processor time reduced to a minimum.

3.5.7. HSMCI

The High Speed Multi Media Card Interface (HSMCI) supports the Multi Media Card (MMC) Specification V4.3, the SD Memory Card Specification V2.0, the SDIO V2.0 specification and CE-ATA V1.1.

3.6. GPIO Ports Allocation

The processor has several flavors each with a different set of optional interfaces. The following tables describe the interfaces available in each option. In bold are the "FIXED" options that can't be changed.

3.6.1. Ports Allocation (SAM9-G25)

Signal	Alternate	Option A	Option B	Option C	SO-DIMM	Power	REMARK
PA0		USART0 TX	SPI1 NPCS1		89	3.3V	
PA1		USART0 RX	SPI0 NPCS2		90	3.3V	
PA2		USART0 RTS	MCI1 D1	ETX0	91	3.3V	
PA3		USART0 CTS	MCI1 D2	ETX1	92	3.3V	
PA4		USART0 CLK	MCI1 D3	ETXER	93	3.3V	
PA5		USART1 TX			115	3.3V	
PA6		USART1 RX			116	3.3V	
PA7		USART2 TX	SPI0 NPCS1		100	3.3V	
PA8		USART2 RX	SPI1 NPCS0		101	3.3V	
PA9		DGB RX			118	3.3V	
PA10		DBG TX			119	3.3V	
PA11		SPI0 MISO	MCI1 D0		95	3.3V	
PA12		SPI0 MOSI	MCI1 CDA		96	3.3V	
PA13		SPI0 SPCK	MCI1 CK		97	3.3V	
PA14		SPI0 NPCS0			98	3.3V	
PA15		MCI0 D0			108	3.3V	uSD Card
PA16		MCI0 CDA			109	3.3V	uSD Card
PA17		MCI0 CK			110	3.3V	uSD Card
PA18		MCI0 D1			111	3.3V	uSD Card
PA19		MCI0 D2			112	3.3V	uSD Card
PA20		MCI0 D3			113	3.3V	uSD Card
PA21		TIOA0	SPI1 MISO		102	3.3V	
PA22		TIOA1	SPI1 MOSI		103	3.3V	
PA23		TIOA2	SPI1 SPK		104	3.3V	
PA24		TCLK0	TK		120	3.3V	
PA25		TCLK1	TF		121	3.3V	
PA26		TCLK2	TD		122	3.3V	
PA27		TIOB0	RD		123	3.3V	
PA28		TIOB1	RK		124	3.3V	
PA29		TIOB2	RF		125	3.3V	
PA30		I2C0 D	SPI1 NPCS3	EMDC	106	3.3V	
PA31		I2C0 CK	SPI1 NPCS2	ETXEN	105	3.3V	

Table 3 – PIO A signal Options

Signal	Alternate	Option A	Option B	Option C	SO-DIMM	Power	REMARK
PB0		ETH0 RX0	USART2 RTS		NA	VDDANA	ETH0 RMII
PB1		ETH0 RX1	USART2 CTS		NA	VDDANA	ETH0RMII
PB2		ETH0 RXER	USART2 CK		NA	VDDANA	ETH0RMII
PB3		ETH0 RXDV	SPI0 NPCS3		NA	VDDANA	ETH0RMII
PB4		ETH0 TXCK	I2C2 D		NA	VDDANA	ETH0RMII
PB5		ETH0 MDIO	I2C2 CLK		174	VDDANA	ETH0RMII
PB6	AD7	ETH0 MDC			175	VDDANA	ETH0RMII
PB7	AD8	ETH0 TXEN			NA	VDDANA	ETH0RMII
PB8	AD9	ETH0 TXER			NA	VDDANA	ETH0 Int.
PB9	AD10	ETH0 TX0	PCK1		NA	VDDANA	ETH0RMII
PB10	AD11	ETH0 TX1	PCK0		NA	VDDANA	ETH0RMII
PB11	AD0	ETH0 TX2	PMW0		181	VDDANA	
PB12	AD1	ETH0 TX3	PMW1		182	VDDANA	
PB13	AD2	ETH0 RX2	PMW2		183	VDDANA	
PB14	AD3	ETH0 RX3	PMW3		184	VDDANA	
PB15	AD4	ETH0 RXCK			185	VDDANA	
PB16	AD5	ETH0 CRS			186	VDDANA	VBUS Sense
PB17	AD6	ETH0 COL			187	VDDANA	Over Current
PB18		IRQ	ADTRG		189	VDDANA	

Table 1 - PIO B Signal Options

Signal	Alternate	Option A	Option B	Option C	SO-DIMM	Power	REMARK
PC0			ISI D0	I2C1 D	129	3.3V	
PC1			ISI D1	I2C1 CK	130	3.3V	
PC2			ISI D2	TIOA3	131	3.3V	
PC3			ISI D3	TIOB3	132	3.3V	
PC4			ISI D4	TCLK3	133	3.3V	
PC5			ISI D5	TIOA4	134	3.3V	
PC6			ISI D6	TIOB4	136	3.3V	
PC7			ISI D7	TCLK4	137	3.3V	
PC8			ISI D8	UART0 TX	138	3.3V	
PC9			ISI D9	UART0 RX	139	3.3V	
PC10			ISI D10	PMW0	140	3.3V	
PC11			ISI D11	PMW1	141	3.3V	
PC12			ISI PCK	TIOA5	143	3.3V	
PC13			ISI VSYNC	TIOB5	144	3.3V	
PC14			ISI HSYNC	TCLK5	145	3.3V	
PC15			ISI MCK	PCK0	146	3.3V	
PC16				UART1 TX	148	3.3V	
PC17				UART1 RX	149	3.3V	
PC18				PMW0	150	3.3V	
PC19				PMW1	151	3.3V	
PC20				PMW2	152	3.3V	
PC21				PMW3	153	3.3V	
PC22			USART3 TX		155	3.3V	
PC23			USART3 RX		156	3.3V	
PC24			USART3 RTS		157	3.3V	
PC25			USART3 CTS		158	3.3V	
PC26			USART3 SCK		159	3.3V	
PC27				USART1 RTS	160	3.3V	
PC28				USART1 CTS	162	3.3V	
PC29				USART1 SCK	163	3.3V	
PC30					164	3.3V	
PC31		FIQ		PCK1	165	3.3V	

Table 2 - PIO C Signal Options

Signal	Alternate	Option A	Option B	Option C	SO-DIMM	Power	REMARK
PD0		NANDOE			NA	3.3V	NAND
PD1		NANDWE			NA	3.3V	NAND
PD2		NANDALE			NA	3.3V	NAND
PD3		NANDCLE			NA	3.3V	NAND
PD4		NCS3			NA	3.3V	NAND
PD5		NWAIT			NA	3.3V	NAND
PD6		D16			NA	3.3V	NAND
PD7		D17			NA	3.3V	NAND
PD8		D18			NA	3.3V	NAND
PD9		D19			NA	3.3V	NAND
PD10		D20			NA	3.3V	NAND
PD11		D21			NA	3.3V	NAND
PD12		D22			NA	3.3V	NAND
PD13		D23			NA	3.3V	NAND
PD14		D24			79	3.3V	MCI1 CD
PD15		D25	A20		80	3.3V	MCI0 CD
PD16		D26	A23		81	3.3V	
PD17		D27	A24		82	3.3V	
PD18		D28	A25		83	3.3V	EN5V A
PD19		D29	NCS2		84	3.3V	EN5V B
PD20		D30	NCS4		85	3.3V	EN5V C
PD21		D31	NCS5		NA	3.3V	

Table 3 - PIO D Signal Options

3.6.2. Ports Allocation (SAM9-X35)

Signal	Alternate	Option A	Option B	Option C	SO-DIMM	Power	REMARK
PA0		USART0 TX	SPI1 NPCS1		89	3.3V	
PA1		USART0 RX	SPI0 NPCS2		90	3.3V	
PA2		USART0 RTS	MCI1 D1	ETX0	91	3.3V	
PA3		USART0 CTS	MCI1 D2	ETX1	92	3.3V	
PA4		USART0 CLK	MCI1 D3	ETXER	93	3.3V	
PA5		USART1 TX	CAN1 TX		115	3.3V	
PA6		USART1 RX	CAN1 RX		116	3.3V	
PA7		USART2 TX	SPI0 NPCS1		100	3.3V	
PA8		USART2 RX	SPI1 NPCS0		101	3.3V	
PA9		DGB RX	CAN0RX		118	3.3V	
PA10		DBG TX	CAN0 TX		119	3.3V	
PA11		SPI0 MISO	MCI1 D0		95	3.3V	
PA12		SPI0 MOSI	MCI1 CDA		96	3.3V	
PA13		SPI0 SPCK	MCI1 CK		97	3.3V	
PA14		SPI0 NPCS0			98	3.3V	
PA15		MCI0 D0			108	3.3V	
PA16		MCI0 CDA			109	3.3V	
PA17		MCI0 CK			110	3.3V	
PA18		MCI0 D1			111	3.3V	
PA19		MCI0 D2			112	3.3V	
PA20		MCI0 D3			113	3.3V	
PA21		TIOA0	SPI1 MISO		102	3.3V	
PA22		TIOA1	SPI1 MOSI		103	3.3V	
PA23		TIOA2	SPI1 SPK		104	3.3V	
PA24		TCLK0	TK		120	3.3V	
PA25		TCLK1	TF		121	3.3V	
PA26		TCLK2	TD		122	3.3V	
PA27		TIOB0	RD		123	3.3V	
PA28		TIOB1	RK		124	3.3V	
PA29		TIOB2	RF		125	3.3V	
PA30		I2C0 D	SPI1 NPCS3	EMDC	106	3.3V	
PA31		I2C0 CK	SPI1 NPCS2	ETXEN	105	3.3V	

Table 4 - PIO A Signal Options

Signal	Alternate	Option A	Option B	Option C	SO-DIMM	Power	REMARK
PB0		**ETH0 RX0**	USART2 RTS		NA	VDDANA	
PB1		**ETH0 RX1**	USART2 CTS		NA	VDDANA	
PB2		**ETH0 RXER**	USART2 CK		NA	VDDANA	
PB3		**ETH0 RXDV**	SPI0 NPCS3		NA	VDDANA	
PB4		**ETH0 TXCK**	I2C2 D		NA	VDDANA	
PB5		**ETH0 MDIO**	I2C2 CLK		174	VDDANA	
PB6	AD7	**ETH0 MDC**			175	VDDANA	
PB7	AD8	**ETH0 TXEN**			NA	VDDANA	
PB8	AD9	**ETH0 TXER**			NA	VDDANA	
PB9	AD10	**ETH0 TX0**	PCK1		NA	VDDANA	
PB10	AD11	**ETH0 TX1**	PCK0		NA	VDDANA	
PB11	AD0	ETH0 TX2	PMW0		181	VDDANA	
PB12	AD1	ETH0 TX3	PMW1		182	VDDANA	
PB13	AD2	ETH0 RX2	PMW2		183	VDDANA	
PB14	AD3	ETH0 RX3	PMW3		184	VDDANA	
PB15	AD4	ETH0 RXCK			185	VDDANA	
PB16	AD5	ETH0 CRS			186	VDDANA	
PB17	AD6	ETH0 COL			187	VDDANA	
PB18		IRQ	ADTRG		189	VDDANA	

Table 5 - PIO B Signal Options

Signal	Alternate	Option A	Option B	Option C	SO-DIMM	Power	REMARK
PC0		LCDAT0		I2C1 D	129	3.3V	
PC1		LCDAT1		I2C1 CK	130	3.3V	
PC2		LCDAT2		TIOA3	131	3.3V	
PC3		LCDAT3		TIOB3	132	3.3V	
PC4		LCDAT4		TCLK3	133	3.3V	
PC5		LCDAT5		TIOA4	134	3.3V	
PC6		LCDAT6		TIOB4	136	3.3V	
PC7		LCDAT7		TCLK4	137	3.3V	
PC8		LCDAT8		UART0 TX	138	3.3V	
PC9		LCDAT9		UART0 RX	139	3.3V	
PC10		LCDAT10		PMW0	140	3.3V	
PC11		LCDAT11		PMW1	141	3.3V	
PC12		LCDAT12		TIOA5	143	3.3V	
PC13		LCDAT13		TIOB5	144	3.3V	
PC14		LCDAT14		TCLK5	145	3.3V	
PC15		LCDAT15		PCK0	146	3.3V	
PC16		LCDAT16		UART1 TX	148	3.3V	
PC17		LCDAT17		UART1 RX	149	3.3V	
PC18		LCDAT18		PMW0	150	3.3V	
PC19		LCDAT19		PMW1	151	3.3V	
PC20		LCDAT20		PMW2	152	3.3V	
PC21		LCDAT21		PMW3	153	3.3V	
PC22		LCDAT22			155	3.3V	
PC23		LCDAT23			156	3.3V	
PC24		LCDDISP			157	3.3V	
PC25					158	3.3V	
PC26		LCDPWM			159	3.3V	
PC27		LCDVSYNC		USART1 RTS	160	3.3V	
PC28		LCDHSYNC		USART1 CTS	162	3.3V	
PC29		LCDDEN		USART1 SCK	163	3.3V	
PC30		LCDPCK			164	3.3V	
PC31		FIQ		PCK1	165	3.3V	

Table 6 - PIO C Signal Options

Signal	Alternate	Option A	Option B	Option C	SO-DIMM	Power	REMARK
PD0		**NANDOE**			NA	3.3V	
PD1		**NANDWE**			NA	3.3V	
PD2		**NANDALE**			NA	3.3V	
PD3		**NANDCLE**			NA	3.3V	
PD4		**NCS3**			NA	3.3V	
PD5		**NWAIT**			NA	3.3V	
PD6		**D16**			NA	3.3V	
PD7		**D17**			NA	3.3V	
PD8		**D18**			NA	3.3V	
PD9		**D19**			NA	3.3V	
PD10		**D20**			NA	3.3V	
PD11		**D21**			NA	3.3V	
PD12		**D22**			NA	3.3V	
PD13		**D23**			NA	3.3V	
PD14		D24			79	3.3V	
PD15		D25	A20		80	3.3V	
PD16		D26	A23		81	3.3V	
PD17		D27	A24		82	3.3V	
PD18		D28	A25		83	3.3V	
PD19		D29	NCS2		84	3.3V	
PD20		D30	NCS4		85	3.3V	
PD21		D31	NCS5		NA	3.3V	

Table 7 - PIO D Signal Options

3.7. Identification

The SOM ID and version is programmed in the 1 Wire EEPROM.