

6 *Using Basic Instructions*

This chapter contains general information about the basic instructions and explains how they function in your application program. Each of the basic instructions includes information on:

- what the instruction symbol looks like
- typical execution time for the instruction
- how to use the instruction

In addition, the last section contains an application example for a paper drilling machine that shows the basic instructions in use.

Bit Instructions

Instruction		Purpose	Page
Mnemonic	Name		
XIC	Examine if Closed	Examines a bit for an On condition.	6-4
XIO	Examine if Open	Examines a bit for an Off condition.	6-4
OTE	Output Energize	Turns a bit On or Off.	6-5
OTL and OTU	Output Latch and Output Unlatch	OTL turns a bit on when the rung is executed, and this bit retains its state when the rung is not executed or a power cycle occurs. OTU turns a bit off when the rung is executed, and this bit retains its state when the rung is not executed or when power cycle occurs.	6-5
OSR	One-Shot Rising	Triggers a one time event.	6-7

Timer/Counter Instructions

Instruction		Purpose	Page
Mnemonic	Name		
TON	Timer On-Delay	Counts timebase intervals when the instruction is true.	6-11
TOF	Timer Off-Delay	Counts timebase intervals when the instruction is false.	6-12
RTO	Retentive Timer	Counts timebase intervals when the instruction is true and retains the accumulated value when the instruction goes false or when power cycle occurs.	6-14
CTU	Count Up	Increments the accumulated value at each false-to-true transition and retains the accumulated value when the instruction goes false or when power cycle occurs.	6-18
CTD	Count Down	Decrements the accumulate value at each false-to-true transition and retains the accumulated value when the instruction goes false or when power cycle occurs.	6-19
RES	Reset	Resets the accumulated value and status bits of a timer or counter. Do not use with TOF timers.	6-20

About the Basic Instructions

These instructions, when used in ladder programs represent hardwired logic circuits used for the control of a machine or equipment.

The basic instructions are separated into three groups: bit, timer, and counter. Before you learn about the instructions in each of these groups, we suggest that you read the overview that precedes the group:

- Bit Instructions Overview
- Timer Instructions Overview
- Counter Instructions Overview

Bit Instructions Overview

These instructions operate on a single bit of data. During operation, the controller may set or reset the bit, based on the logical continuity of ladder rungs. You can address a bit as many times as your program requires.

Note

Using the same address with multiple output instructions is not recommended.

Bit instructions are used with the following data files:

- Output and input data files. These represent external outputs and inputs.
- The status data file (file 2).
- The bit data file (B3:). These are the internal coils used in your program.
- Timer, counter, and control data files (T4:, C5:, and R6:). These instructions use various control bits.
- The integer data file (N7:). Use these addresses (at the bit level) as your program requires.

Examine if Closed (XIC)



Execution Times
(μsec) when:

True	False
1.54	1.72

Use the XIC instruction in your ladder program to determine if a bit is On. When the instruction is executed, if the bit addressed is on (1), then the instruction is evaluated as true. When the instruction is executed, if the bit addressed is off (0), then the instruction is evaluated as false.

Bit Address State	XIC Instruction
0	False
1	True

Examples of devices that turn on or off include:

- a push button wired to an input (addressed as I1:0/4)
- an output wired to a pilot light (addressed as O0:0/2)
- a timer controlling a light (addressed as T4:3/DN)

Examine if Open (XIO)



Execution Times
(μsec) when:

True	False
1.54	1.72

Use an XIO instruction in your ladder program to determine if a bit is Off. When the instruction is executed, if the bit addressed is off (0), then the instruction is evaluated as true. When the instruction is executed, if the bit addressed is on (1), then the instruction is evaluated as false.

Bit Address State	XIO Instruction
0	True
1	False

Examples of devices that turn on or off include:

- motor overload normally closed (N.C.) wired to an input (I1:0/10)
- an output wired to a pilot light (addressed as O0:0/4)
- a timer controlling a light (addressed as T4:3/DN)

Output Energize (OTE)

—()—

Use an OTE instruction in your ladder program to turn On a bit when rung conditions are evaluated as true.

Execution Times
(μsec) when:

True	False
4.43	4.43

An example of a device that turns on or off is an output wired to a pilot light (addressed as O0:0/4).

OTE instructions are reset when:

- You enter or return to the REM Run or REM Test mode or power is restored.
- The OTE is programmed within an inactive or false Master Control Reset (MCR) zone.

Note

A bit that is set within a subroutine using an OTE instruction remains set until the subroutine is scanned again.

Output Latch (OTL) and Output Unlatch (OTU)

—(L)—

OTL and OTU are retentive output instructions. OTL can only turn on a bit, while OTU can only turn off a bit. These instructions are usually used in pairs, with both instructions addressing the same bit.

—(U)—

Your program can examine a bit controlled by OTL and OTU instructions as often as necessary.

Execution Times
(μsec) when:

	True	False
OTL	4.97	3.16
OTU	4.97	3.16



Under fatal error conditions, physical outputs are turned off. Once the error conditions are cleared, the controller resumes operation using the data table value of the operand.

Using OTL

When you assign an address to the OTL instruction that corresponds to the address of a physical output, the output device wired to this screw terminal is energized when the bit is set (turned on or enabled).

When rung conditions become false (after being true), the bit remains set and the corresponding output device remains energized.

When enabled, the latch instruction tells the controller to turn on the addressed bit. Thereafter, the bit remains on, regardless of the rung condition, until the bit is turned off (typically by a OTU instruction in another rung).

Using OTU

When you assign an address to the OTU instruction that corresponds to the address of a physical output, the output device wired to this screw terminal is de-energized when the bit is cleared (turned off or disabled).

The unlatch instruction tells the controller to turn off the addressed bit. Thereafter, the bit remains off, regardless of the rung condition, until it is turned on (typically by a OTL instruction in another rung).

One-Shot Rising (OSR)

—[OSR]—

Execution Times
(μsec) when:

True	False
13.02	11.48

The OSR instruction is a retentive input instruction that triggers an event to occur one time. Use the OSR instruction when an event must start based on the change of state of the rung from false to true.

When the rung conditions preceding the OSR instruction go from false to true, the OSR instruction will be true for one scan. After one scan is complete, the OSR instruction becomes false, even if the rung conditions preceding it remain true. The OSR instruction will only become true again if the rung conditions preceding it transition from false to true.

The controller allows you to use one OSR instruction per output in a rung.

Entering Parameters

The address assigned to the OSR instruction is *not* the one-shot address referenced by your program, nor does it indicate the state of the OSR instruction. This address allows the OSR instruction to *remember* its previous rung state.

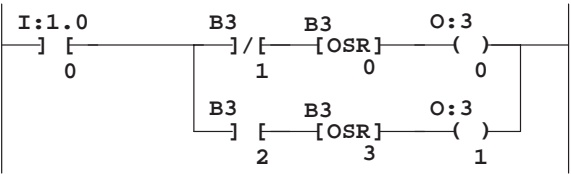
Use a bit address from either the bit or integer data file. The addressed bit is set (1) for one scan when rung conditions preceding the OSR instruction are true (even if the OSR instruction becomes false); the bit is reset (0) when rung conditions preceding the OSR instruction are false.

Note

The bit address you use for this instruction must be unique. Do not use it elsewhere in the program.

Do not use an input or output address to program the address parameter of the OSR instruction.

Example Rung



Timer Instructions Overview

Each timer address is made of a 3-word element. Word 0 is the control word, word 1 stores the preset value, and word 2 stores the accumulated value.

	15 14 13									
Word 0	<table><tr><td>EN TT DN</td><td> </td><td>Internal Use</td></tr><tr><td colspan="3">Preset Value</td></tr><tr><td colspan="3">Accumulator Value</td></tr></table>	EN TT DN		Internal Use	Preset Value			Accumulator Value		
EN TT DN		Internal Use								
Preset Value										
Accumulator Value										
Word 1										
Word 2										

EN = Timer Enable Bit
TT = Timer Timing Bit
DN = Timer Done Bit

Entering Parameters

Accumulator Value (ACC)

This is the time elapsed since the timer was last reset. When enabled, the timer updates this continually.

Preset Value (PRE)

Specifies the value which the timer must reach before the controller sets the done bit. When the accumulated value becomes equal to or greater than the preset value, the done bit is set. You can use this bit to control an output device.

Preset and accumulated values for timers range from 0 to +32,767. If a timer preset or accumulated value is a negative number, a runtime error occurs.

Timebase

The timebase determines the duration of each timebase interval. The timebase is selectable as 0.01 (10 ms) second or 1.0 second.

Timer Accuracy

Timer accuracy refers to the length of time between the moment a timer instruction is enabled and the moment the timed interval is complete.

Timing accuracy is –0.01 to +0 seconds, with a program scan of up to 2.5 seconds. The 1-second timer maintains accuracy with a program scan of up to 1.5 seconds. If your programs can exceed 1.5 or 2.5 seconds, repeat the timer instruction rung so that the rung is scanned within these limits.

Note

Timing could be inaccurate if Jump (JMP), Label (LBL), Jump to Subroutine (JSR), or Subroutine (SBR) instructions skip over the rung containing a timer instruction while the timer is timing. If the skip duration is within 2.5 seconds, no time will be lost; if the skip duration exceeds 2.5 seconds, an undetectable timing error occurs. When using subroutines, a timer must be executed at least every 2.5 seconds to prevent a timing error.

Addressing Structure

Address bits and words using the format **Tf:e.s/b**

Format		Explanation	
Tf:e	T	Timer file	
	f	File number. The only valid file number is 4.	
	:	Element delimiter	
	e	Element number	Ranges from 0 – 39. These are 3-word elements. See figure on page 6–8.
	.	Word element	
	s	subelement	
	/	Delimiter	
	b	bit	

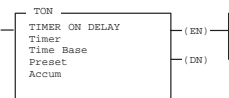
Addressing Examples

- **T4:0/15** or **T4:0/EN** Enable bit
- **T4:0/14** or **T4:0/TT** Timer timing bit
- **T4:0/13** or **T4:0/DN** Done bit

- **T4:0.1** or **T4:0.PRE** Preset value of the timer
- **T4:0.2** or **T4:0.ACC** Accumulator value of the timer

- **T4:0.1/0** or **T4:0.PRE/0** Bit 0 of the preset value
- **T4:0.2/0** or **T4:0.ACC/0** Bit 0 of the accumulated value

Timer On-Delay (TON)



Execution Times
(μsec) when:

True	False
38.34	30.38

Use the TON instruction to delay the turning on or off of an output. The TON instruction begins to count timebase intervals when rung conditions become true. As long as rung conditions remain true, the timer increments its accumulated value (ACC) each scan until it reaches the preset value (PRE). The accumulated value is reset when rung conditions go false, regardless of whether the timer has timed out.

Using Status Bits

This Bit	Is Set When	And Remains Set Until One of the Following
Timer Done Bit DN (bit 13)	accumulated value is equal to or greater than the preset value	rung conditions go false
Timer Enable Bit EN (bit 14)	rung conditions are true	rung conditions go false
Timer Timing Bit TT (bit 15)	rung conditions are true and the accumulated value is less than the preset value	rung conditions go false or when the done bit is set

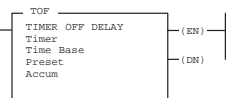
When the controller changes from the REM Run or REM Test mode to the REM Program mode or user power is lost while the instruction is timing but has not reached its preset value, the following occurs:

- Timer Enable (EN) bit remains set.
- Timer Timing (TT) bit remains set.
- Accumulated value (ACC) remains the same.

On returning to the REM Run or REM Test mode, the following can happen:

Condition	Result
If the rung is true:	EN bit remains set. TT bit remains set. ACC value is reset.
If the rung is false:	EN bit is reset. TT bit is reset. ACC value is reset.

Timer Off-Delay (TOF)



Execution Times
(μsec) when:

True	False
39.42	31.65

Use the TOF instruction to delay turning on or off an output. The TOF instruction begins to count timebase intervals when the rung makes a true-to-false transition. As long as rung conditions remain false, the timer increments its accumulated value (ACC) each scan until it reaches the preset value (PRE). The controller resets the accumulated value when rung conditions go true regardless of whether the timer has timed out.

Using Status Bits

This Bit	Is Set When	And Remains Set Until One of the Following
Timer Done Bit DN (bit 13)	rung conditions are true	rung conditions go false and the accumulated value is greater than or equal to the preset value
Timer Timing Bit TT (bit 14)	rung conditions are false and the accumulated value is less than the preset value	rung conditions go true or when the done bit is reset
Timer Enable Bit EN (bit 15)	rung conditions are true	rung conditions go false

When the controller changes from the REM Run or REM Test mode to the REM Program mode, or user power is lost while a timer off-delay instruction is timing but has not reached its preset value, the following occurs:

- Timer Enable (EN) bit remains set.
- Timer Timing (TT) bit remains set.
- Timer Done (DN) bit remains set.
- Accumulated value (ACC) remains the same.

On returning to the REM Run or REM Test mode, the following can happen:

Condition	Result
If the rung is true:	TT bit is reset. DN bit remains set. EN bit is set. ACC value is reset.
If the rung is false:	TT bit is reset. DN bit is reset. EN bit is reset. ACC value is set equal to the preset value.

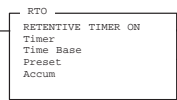


The Reset (RES) instruction cannot be used with the TOF instruction because RES always clears the status bits as well as the accumulated value. (See page 6–20.)

Note

The TOF times inside an inactive MCR Pair.

Retentive Timer (RTO)



Use the RTO instruction to turn an output on or off after its timer has been on for a preset time interval. The RTO instruction is a retentive instruction that lets the timer stop and start without resetting the accumulated value (ACC).

Execution Times
(µsec) when:

True	False
38.34	27.49

The RTO instruction retains its accumulated value when any of the following occurs:

- Rung conditions become false.
- You change controller operation from the REM Run or REM Test mode to the REM Program mode.
- The controller loses power.
- A fault occurs.

Using Status Bits

This Bit	Is Set When	And Remains Set Until One of the Following
Timer Done Bit DN (bit 13)	accumulated value is equal to or greater than the preset value	the appropriate RES instruction is enabled
Timer Timing Bit TT (bit 14)	rung conditions are true and the accumulated value is less than the preset value	rung conditions go false or when the done bit is set
Timer Enable Bit EN (bit 15)	rung conditions are true	rung conditions go false

Note

To reset the retentive timer’s accumulated value and status bits after the RTO rung goes false, you must program a reset (RES) instruction with the same address in another rung.

When the controller changes from the REM Run or REM Test mode to the REM Program or REM Fault mode, or user power is lost while the timer is timing but not yet at the preset value, the following occurs:

- Timer Enable (EN) bit remains set.
- Timer Timing (TT) bit remains set.
- Accumulated value (ACC) remains the same.

On returning to the REM Run or REM Test mode or when power is restored, the following can happen:

Condition	Result
If the rung is true:	TT bit remains set. EN bit remains set. ACC value remains the same and resumes incrementing.
If the rung is false:	TT bit is reset. DN bit remains in its last state. EN bit is reset. ACC value remains in its last state.

Counter Instructions Overview

Each Counter address is made of a 3-word data file element. Word 0 is the control word, containing the status bits of the instruction. Word 1 is the preset value. Word 2 is the accumulated value.

The control word for counter instructions includes six status bits, as indicated below.

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word 0	CU	CD	DN	OV	UN	UA										
Word 1	Preset Value															
Word 2	Accumulator Value															

CU = Counter up enable bit

CD = Counter down enable bit

DN = Done bit

OV = Overflow bit

UN = Underflow bit

UA = Update accumulator (HSC only)

For high-speed counter instruction information, see chapter 12.

Entering Parameters

Accumulator Value (ACC)

This is the number of false-to-true transitions that have occurred since the counter was last reset.

Preset Value (PRE)

Specifies the value which the counter must reach before the controller sets the done bit. When the accumulator value becomes equal to or greater than the preset value, the done status bit is set. You can use this bit to control an output device.

Preset and accumulated values for counters range from –32,768 to +32,767, and are stored as signed integers. Negative values are stored in two’s complement form.

Addressing Structure

Address bits and words using the format **Cf:e.s/b**

Format	Explanation		
Cf:e	C	Counter file	
	f	File number. The only valid file number is 5.	
	:	Element delimiter	
	e	Element number	Ranges from 0 – 39. These are 3-word elements. See figure on page 6–15.
	.	Word element	
	s	subelement	
	/	Delimiter	
	b	bit	

Note *If assigned to a high-speed counter instruction, C5:0 is not available as an address for any other counter instructions. For more information on high-speed counter instructions, see chapter 12.*

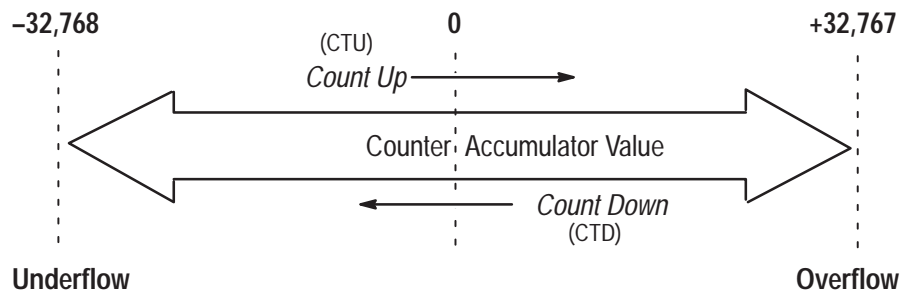
Addressing Examples

- **C5:0/15** or **C5:0/CU** Count up enable bit
- **C5:0/14** or **C5:0/CD** Count down enable bit
- **C5:0/13** or **C5:0/DN** Done bit
- **C5:0/12** or **C5:0/OV** Overflow bit
- **C5:0/11** or **C5:0/UN** Underflow bit
- **C5:0/10** or **C5:0/UA** Update accumulator bit
- **C5:0.1** or **C5:0.PRE** Preset value of the counter
- **C5:0.2** or **C5:0.ACC** Accumulator value of the counter
- **C5:0.1/0** or **C5:0.PRE/0** Bit 0 of the preset value
- **C5:0.2/0** or **C5:0.ACC/0** Bit 0 of the accumulated value

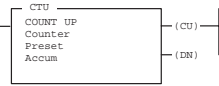
How Counters Work

The figure below demonstrates how a counter works. The count value must remain in the range of $-32,768$ to $+32,767$. If the count value goes above $+32,767$ or below $-32,768$, a counter status overflow (OV) or underflow (UN) bit is set.

A counter can be reset to zero using the reset (RES) instruction. (See page 6–20.)



Count Up (CTU)



Execution Times
(μsec) when:

True	False
29.84	26.67

The CTU is an instruction that counts false-to-true rung transitions. Rung transitions can be caused by events occurring in the program (from internal logic or by external field devices) such as parts traveling past a detector or actuating a limit switch.

When rung conditions for a CTU instruction have made a false-to-true transition, the accumulated value is incremented by one count, provided that the rung containing the CTU instruction is evaluated between these transitions. The ability of the counter to detect false-to-true transitions depends on the speed (frequency) of the incoming signal.

Note *The on and off duration of an incoming signal must not be faster than the scan time 2x (assuming a 50% duty cycle).*

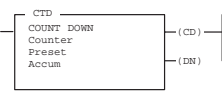
The accumulated value is retained when the rung conditions again become false. The accumulated count is retained until cleared by a reset (RES) instruction that has the same address as the counter reset.

Using Status Bits

This Bit	Is Set When	And Remains Set Until One of the Following
Count Up Overflow Bit OV (bit 12)	accumulated value wraps around to -32,768 (from +32,767) and continues counting up from there	a RES instruction having the same address as the CTU instruction is executed OR the count is decremented less than or equal to +32,767 with a CTD instruction
Done Bit DN (bit 13)	accumulated value is equal to or greater than the preset value	the accumulated value becomes less than the preset
Count Up Enable Bit CU (bit 15)	rung conditions are true	rung conditions go false OR a RES instruction having the same address as the CTU instruction is enabled

The accumulated value is retained after the CTU instruction goes false, or when power is removed from and then restored to the controller. Also, the on or off status of counter done, overflow, and underflow bits is retentive. The accumulated value and control bits are reset when the appropriate RES instruction is enabled. The CU bits are always set prior to entering the REM Run or REM Test modes.

Count Down (CTD)



The CTD is a retentive output instruction that counts false-to-true rung transitions. Rung transitions can be caused by events occurring in the program such as parts traveling past a detector or actuating a limit switch.

Execution Times
(µsec) when:

True	False
32.19	27.22

When rung conditions for a CTD instruction have made a false-to-true transition, the accumulated value is decremented by one count, provided that the rung containing the CTD instruction is evaluated between these transitions.

The accumulated counts are retained when the rung conditions again become false. The accumulated count is retained until cleared by a reset (RES) instruction that has the same address as the counter reset.

Using Status Bits

This Bit	Is Set When	And Remains Set Until One of the Following
Count Down Underflow Bit UN (bit 11)	accumulated value wraps around to +32,768 (from -32,767) and continues counting down from there	a RES instruction having the same address as the CTD instruction is enabled. OR the count is incremented greater than or equal to +32,767 with a CTU instruction
Done Bit DN (bit 13)	accumulated value is equal to or greater than the preset value	the accumulated value becomes less than the preset
Count Down Enable Bit CD (bit 14)	rung conditions are true	rung conditions go false OR a RES instruction having the same address as the CTD instruction is enabled

The accumulated value is retained after the CTD instruction goes false, or when power is removed from and then restored to the controller. Also, the on or off status of counter done, overflow, and underflow bits is retentive. The accumulated value and control bits are reset when the appropriate RES instruction is executed. The CD bits are always set prior to entering the REM Run or REM Test modes.

Reset (RES)

—(RES)—

Execution Times
(μsec) when:

True	False
15.19	4.25

Use a RES instruction to reset a timer or counter. When the RES instruction is executed, it resets the data having the same address as the RES instruction.

Using a RES instruction for a:	The controller resets the:
Timer (Do not use a RES instruction with a TOF.)	ACC value to 0 DN bit TT bit EN bit
Counter	ACC value to 0 OV bit UN bit DN bit CU bit CD bit
Control	POS value to 0 EN bit EU bit DN bit EM bit ER bit UL bit IN and FD go to last state

Note

If using this instruction to reset the HSC accumulator, see page 12–21.

When resetting a counter, if the RES instruction is enabled and the counter rung is enabled, the CU or CD bit is reset.

If the counter preset value is negative, the RES instruction sets the accumulated value to zero. This in turn causes the done bit to be set by a count down or count up instruction.



Because the RES instruction resets the accumulated value, and the done, timing, and enabled bits, do *not* use the RES instruction to reset a timer address used in a TOF instruction. Otherwise, unpredictable machine operation or injury to personnel may occur.

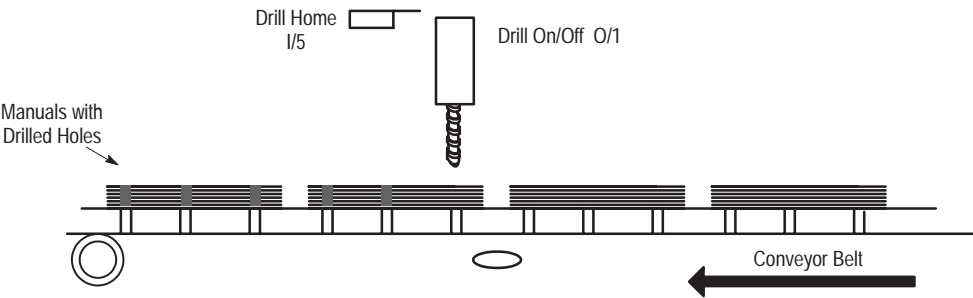
Basic Instructions in the Paper Drilling Machine Application Example

This section provides ladder rungs to demonstrate the use of basic instructions. The rungs are part of the paper drilling machine application example described in appendix E. You will be adding the main program in file 2 and adding a subroutine to file 6.

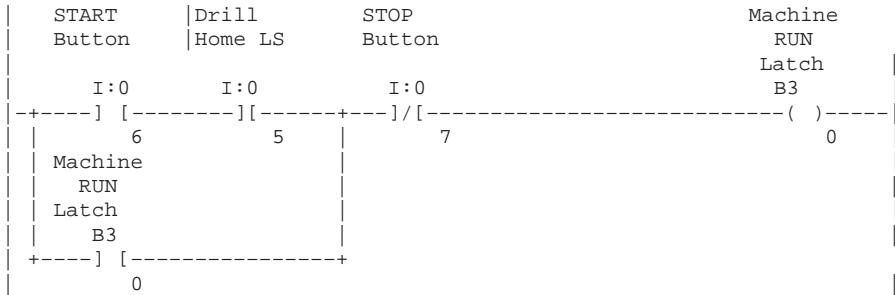
Adding File 2

The rungs shown on the following page are referred to as the program’s “start-up” logic. They determine the conditions necessary to start the machine in motion by monitoring the start and stop push buttons. When the start push button is pressed, it enables the conveyor to move and starts spinning the drill bit. When the stop push button is pressed, it disables the conveyor motion and turns off the drill motor.

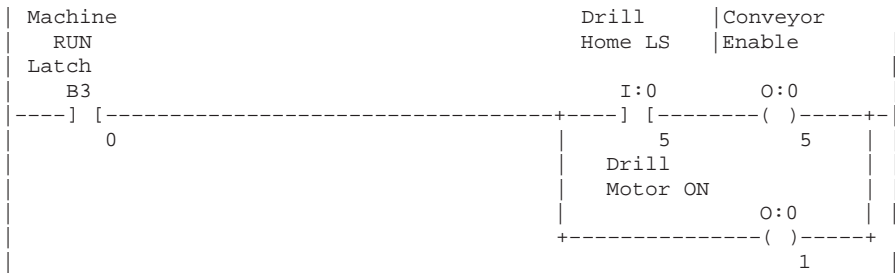
The start-up logic also checks to make sure that the drill is fully retracted (in the home position) before allowing the conveyor to move.



Rung 2:3^①
Starts the conveyor in motion when the start button is pressed. However, another condition must also be met before we start the conveyor: the drill must be in its fully retracted position (home). This rung also stops the conveyor when the stop button is pressed.

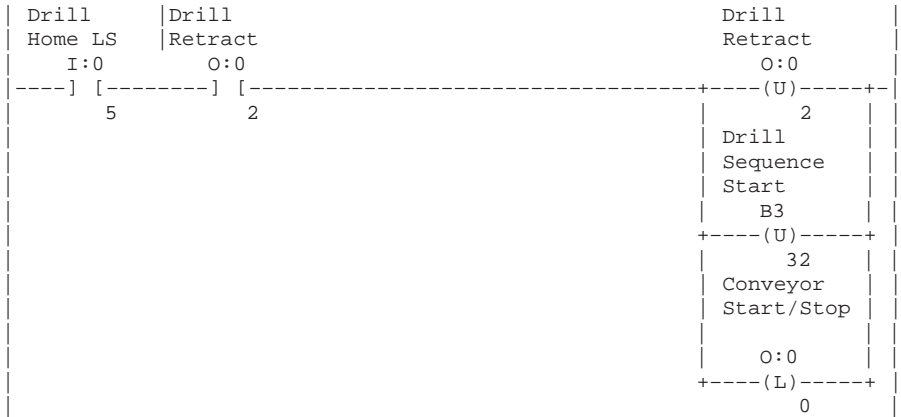


Rung 2:4
Applies the above start logic to the conveyor and drill motor.



^① Rungs 2:0 through 2:2 will be added in chapter 12.

Rung 6:2
When the drill is retracting (after drilling a hole), the body of the drill actuates the DRILL HOME limit switch. When this happens the DRILL RETRACT signal is turned off, the DRILL SEQUENCE START bit is turned off to indicate the drilling process is complete, and the conveyor is restarted.



Rung 6.3

