PowerDNA DIO-40x User Manual

24-channel Digital I/O layer
for the PowerDNA Cube

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Introduction

This document outlines the feature-set and use of the DIO-401, DIO-402, and DIO-404/5 digital input layers for the PowerDNA I/O Cube.

Organization of this manual

This PowerDNA DIO-401/2/5 User Manual is organized as follows:

Introduction
This chapter provides an overview of PowerDNA Digital Input Series board features, the various models available and what you need to get started.

The DIO-401/2/5 layer
This chapter provides an overview of the device architecture, connectivity, and logic of the DIO-401/2/5 series layer.

Programming using the UeiDaq Framework High-Level API
This chapter provides an overview of the how to create a session, configure the session for digital data acquisition/output, and format relevant output.

Programming using the Low-Level API
Low-level API commands for configuring and using the DIO-401/2/5 series layer.

Appendix A - Accessories
This appendix outlines accessories available for DIO-401/2/5 series layer.

Appendix B - Layer Verification
This appendix outlines how to verify calibration for the DIO-401/2/5 series layer.

Conventions

To help you get the most out of this manual and our products, please note that we use the following conventions:

TIP Tips are designed to highlight quick ways to get the job done, or reveal good ideas you might not discover on your own.

Note Notes alert you to important information.

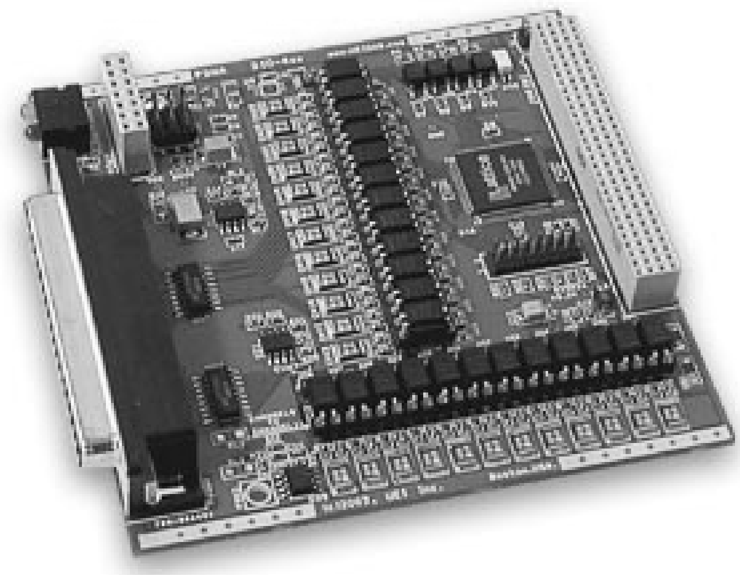
CAUTION! *Caution advises you of precautions to take to avoid injury, data loss, and damage to your boards or a system crash.*

Text formatted in **bold** typeface generally represents text that should be entered verbatim. For instance, it can represent a command, as in the following example: "You can instruct users how to run setup using a command such as **setup.exe**."

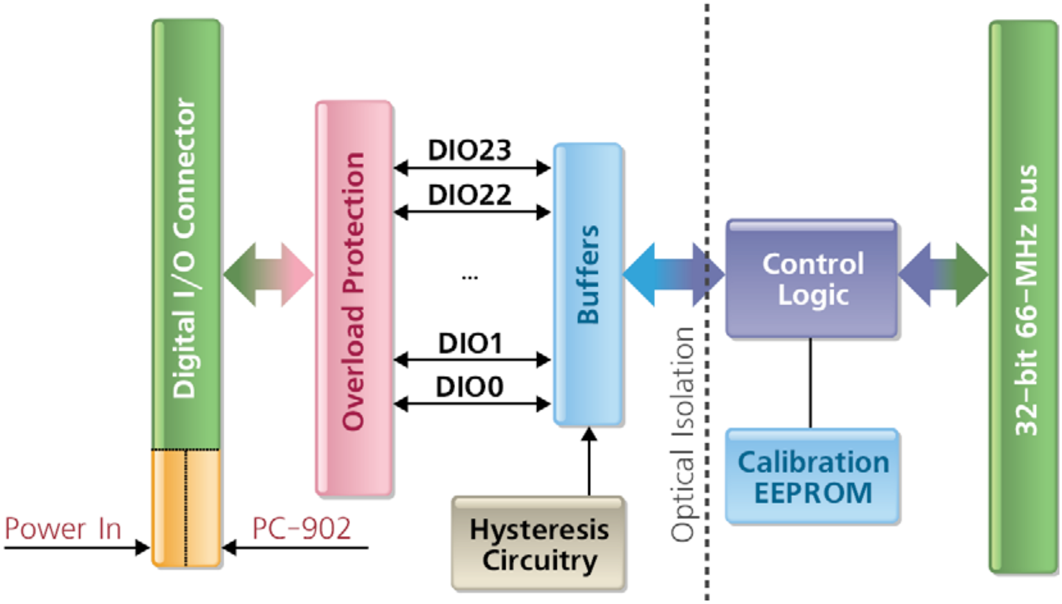
1 The DIO-40x Layer

The DIO-40x layers have the following functions:

- DIO-401/2/5 are digital I/O layers.
- DIO-401 has 24 digital inputs.
- DIO-402 has 24 digital outputs.
- DIO-405 has 12 digital inputs and 12 digital outputs.
- Lines handle levels to 36V (max VCC) on inputs and outputs
- Lines protected to 1000V peak-peak and 7-kV electrostatic
- Over and under-voltage protection to ±36V
- Input rate is 2k samples/sec with hysteresis enabled
- Outputs provide drive capability of 80 mA/channel, resetable fuse protected to 100mA
- Inputs have 1024 point programmable low and high hysteresis settings
- Peak detection 1ms
- Triggering, edge detection, event time stamping is available on digital inputs at software level
- Power consumption: 2.5W at full load



1.1 Device architecture



The DIO-40x layers have similar architecture. The I/O part of the layer is isolated from the logic interface via optocouplers.

1.2 Layer connectors and wiring

DNA-DIO-401

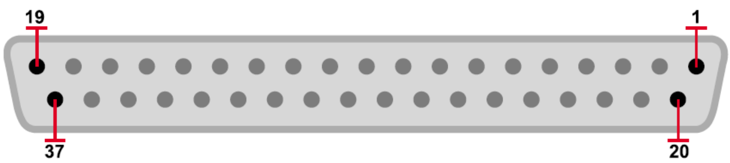
*VCC	37	19	VCC*
DGND	36	18	VCC*
DIN23	35	17	DGND
DIN21	34	16	DIN22
DIN20	33	15	DGND
DIN18	32	14	DIN19
DIN17	31	13	DGND
DIN15	30	12	DIN16
DIN14	29	11	DGND
DIN12	28	10	DIN13
DIN11	27	9	DGND
DIN9	26	8	DIN10
DIN8	25	7	DGND
DIN6	24	6	DIN7
DIN5	23	5	DGND
DIN3	22	4	DIN4
DIN2	21	3	DGND
DIN0	20	2	DIN1
		1	DGND

DNA-DIO-402

*VCC	37	19	VCC*
DGND	36	18	VCC*
DOUT23	35	17	DGND
DOUT21	34	16	DOUT22
DOUT20	33	15	DGND
DOUT18	32	14	DOUT19
DOUT17	31	13	DGND
DOUT15	30	12	DOUT16
DOUT14	29	11	DGND
DOUT12	28	10	DOUT13
DOUT11	27	9	DGND
DOUT9	26	8	DOUT10
DOUT8	25	7	DGND
DOUT6	24	6	DOUT7
DOUT5	23	5	DGND
DOUT3	22	4	DOUT4
DOUT2	21	3	DGND
DOUT0	20	2	DOUT1
		1	DGND

DNA-DIO-405[1]

*VCC	37	19	VCC*
DGND	36	18	VCC*
DOUT11	35	17	DGND
DOUT9	34	16	DOUT10
DOUT8	33	15	DGND
DOUT6	32	14	DOUT7
DOUT5	31	13	DGND
DOUT3	30	12	DOUT4
DOUT2	29	11	DGND
DOUT0	28	10	DOUT1
DIN11	27	9	DGND
DIN9	26	8	DIN10
DIN8	25	7	DGND
DIN6	24	6	DIN7
DIN5	23	5	DGND
DIN3	22	4	DIN4
DIN2	21	3	DGND
DIN0	20	2	DIN1
		1	DGND



[1]Please notice that DIO-405 outputs are numbered from *DOut0* through *DOut11*. All layers in the DIO-40x family have similar connector layout.

Note the **VCC*** pins. This layer must be supplied power in one of two forms:

- By use of the VCC pins on the DNA-STP-37 or STP-37D or DNA-DIO-O22 terminal panels: connect a 5-36V source to the VCC pins.
- By use of the PC-902 power conversion layers, which supply power internally and will not break any isolation.

When power is provided to the layer, the RDY LED turns on. When no power is supplied, the RDY LED is off, and the DNA-DIO-40x layer will not operate.

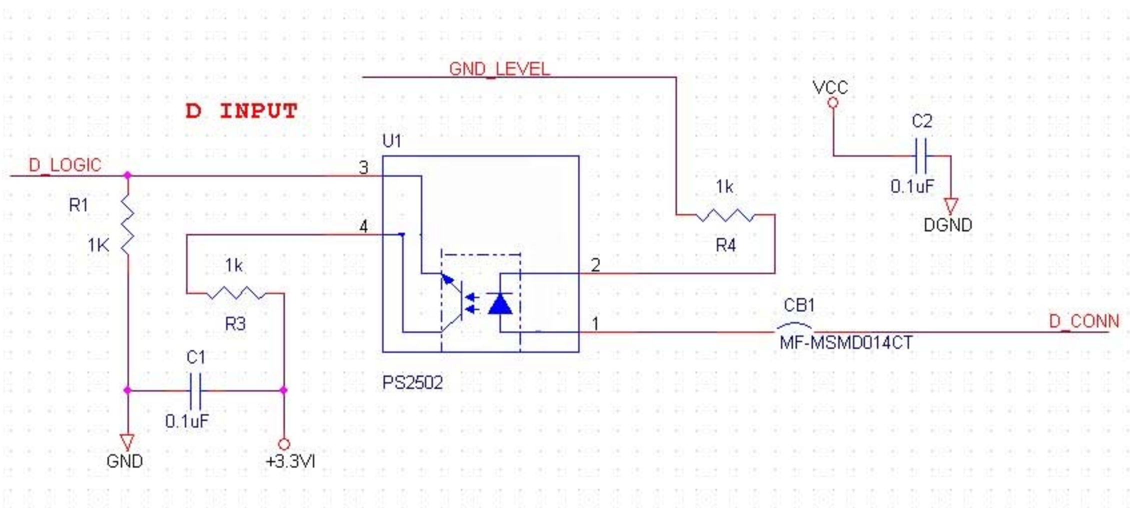
> ***CAUTION!*** *To prevent damage to board components, VCC* must always be equal to or greater than the DIN voltage.*

1.3 Layer capabilities

Inputs and outputs of these layers are powered externally. The user has to supply from 5V to 24V external power to *VCC* line. Depending on power supply, the layer accepts the following levels:

VCC	Input "0"	Input "1"	Output "0"	Output "1"
5V	1.2V	3.0V	0.6V	4.5V
24V	5V	12V	2V	22V
36V	7V	12V	-	-

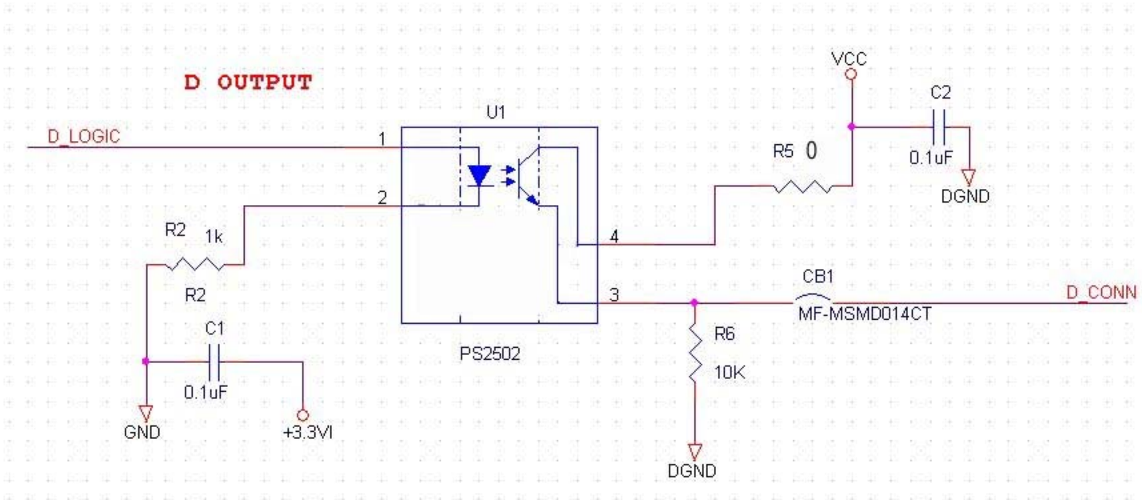
Every input circuit is built as follows:



To switch input to a logical one, the user should provide current flowing through the LED in the optical isolator. The minimum current requirement is 2.4mA. The current is limited by resistor R4 and can be as high as 36mA at the maximum input voltage.

The user can put a current limiting resistor in series with input to limit both current flowing through the LED, and the power dissipation inside the PowerDNA cube. *VCC* is required to power ground level DACs to provide ground level reference. Inputs will not work properly without supplying *VCC* unless ground layer feature is disabled internally by shorting ground level to *DGND* by jumpers.

Every output circuit is built as follows:



The maximum current thru the transistor should is limited to 100mA by the *CB1* fuse. User should supply *VCC* to collector of the transistor.

For testing, place a 1k to 10k resistor in-line between the Digital Output and ground. The voltage across the resistor is the output, plus loss.

2 Programming using the UeiDaq Framework

This section describes how to control the PowerDNA DIO-401/2/5 using the UeiDaq's framework API.
The UeiDaq framework is object oriented and its objects can be manipulated in the same manner from different development environments such as Visual C++, Visual Basic or LabVIEW.
The following section will focus on the C++ API but the concept stays the same no matter what programming language you use.
Please refer to the "UeiDaq Framework User Manual" to get more information on using other programming languages.

2.1 Creating a session

The Session object controls all operations on your PowerDNA device. Therefore, the first task is to create a session object:

```
CUeiSession session;
```

2.2 Configuring the resource string

The framework uses resource strings to select which device, subsystem and channels to use within a session. The resource string syntax is similar to a web URL:
<device class>://<IP address>/<Device Id>/<Subsystem><Channel list>

For PowerDNA, the device class is **pdna**.
For example, the following resource string selects digital input channels 0,1,2,3 on device 1 at IP address 192.168.100.2: "pdna://192.168.100.2/Dev1/Di0:3"

Note In the framework, a digital channel corresponds to a physical port on the device. You cannot configure a session to only access a subset of the lines within a digital port.

```
// Configure session to read from port 0 on device 1
di_session.CreateDIChannel("pdna://192.168.100.2/Dev1/Di0");

// Configure session to write to port 0 on device 1
do_session.CreateDOChannel("pdna://192.168.100.2/Dev1/Do0");
```

Note Sessions are unidirectional. If your device has both input and output ports or has bidirectional ports, you need to configure two sessions: one for input and one for output.

2.3 Configuring the timing

You can configure the DIO-401/2/5 to run in simple mode (point by point) or buffered mode (ACB mode).
In simple mode, the delay between samples is determined by software on the host computer.
In buffered mode, the delay between samples is determined by the DIO-401/2/5 on-board clock.

The following sample shows how to configure the simple mode. Please refer to the "UeiDaq Framework User's Manual" to learn how to use the other timing modes.

```
di_session.ConfigureTimingForSimpleIO();
```

2.4 Configuring the hysteresis

The PowerDNA DIO-401/2/5 layers are equipped with a hysteresis circuitry whose low and high threshold levels can be programmed using custom properties.

- "lowhysteresis":A floating-point value representing the low hysteresis voltage as a percentage of the power supply voltage (Vcc).
- "highhysteresis": A floating-point value representing the high hysteresis voltage as a percentage of the power supply voltage (Vcc).

```
// Program low threshold to 10% and high threshold to 90%
double lowHyst = 0.1;
double highHyst = 0.9;
di_session.SetCustomProperty("lowhysteresis", sizeof(double),
&lowHyst);
di_session.SetCustomProperty("highhysteresis", sizeof(double),
&highHyst);
```

2.5 Reading and Writing data

Reading data from the DIO-401/2/5 is done using a reader object.
The following sample code shows how to create a scaled reader object and read samples.

```
// Create a reader and link it to the session's stream
CUeiDigitalReader reader(di_session.GetDataStream());

// read one scan, the buffer must be big enough to contain
// one value per channel
uInt16 data;
reader.ReadSingleScan(&data);
```

Writing data is done using a writer object. The following sample shows how to create a writer object and write data .

```
// Create a writer and link it to the session's stream
CUeiDigitalWriter writer(do_session.GetDataStream());

// write one scan, the buffer must contain
// one value per channel
uInt16 data = 0xFEFE;
writer.WriteSingleScan(&data);
```

2.6 Cleaning-up the session

The session object will clean itself up when it goes out of scope or when it is destroyed. However, you can manually clean up the session (to reuse the object with a different set of channels or parameters).

```
di_session.CleanUp();
```

3 Programming using the Low-Level API

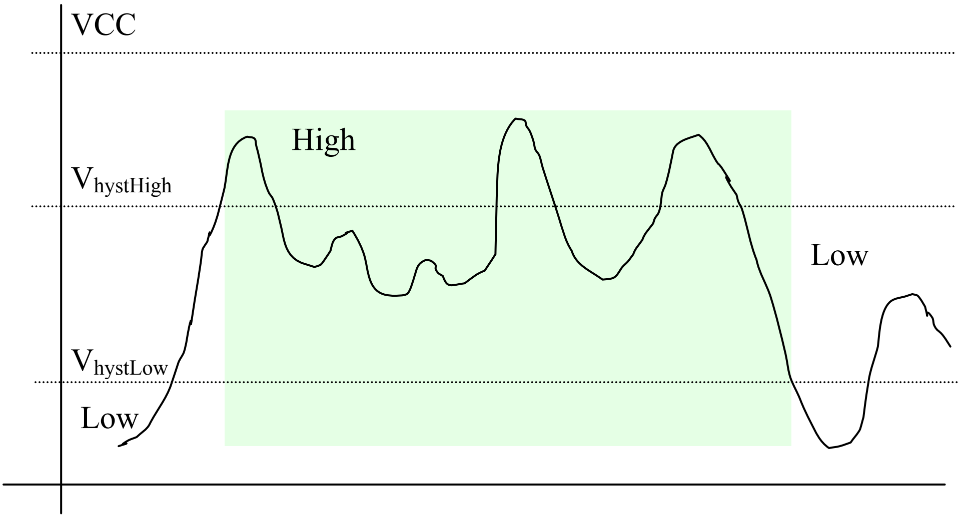
This section describes how to program the PowerDNA cube using the low-level API. The low-level API offers direct access to PowerDNA DAQBios protocol and also allows you to directly access device registers.
We recommend that you use the UeiDaq framework (*see Section 2 above*) which is easier to use.
You should only need to use the low-level API if you are using an operating system other than Windows.

3.1 Programming hysteresis

The ground level of the inputs can be set from *DGND* level to *VCC* level in 1024 steps (increments). For the optical isolator to open input level, it should be above ground level to at least 2.4V to supply enough current for isolator LED.
When programmable hysteresis mode is disabled, input becomes "1" if input voltage is 2.4V above selected ground level (to provide enough current to the isolating LED.)
When programmable hysteresis mode is selected, the device logic constantly changes ground level between two programmed levels. This change of ground level occurs at 2kHz rate. Every time the logic changes ground level, it performs "read". Then the logic produces output based on two consecutive reads at low and high ground level. The following table summarizes the result.

Logic level\ Read result	Read at low	Read at High	Result
	0	0	0
	1	0	Keep previous value
	1	1	1

The following diagram shows the hysteresis feature. The input stays at "0" until it crosses both low and high ground levels. If the signal falls below high ground level but never crosses low ground level (for more than 1ms) it remains at "1".



Hysteresis is a specific feature of DIO-40x layers. To access this feature, you should enable it in the configuration word:

```
#define DQ_L401_HYSTEN      (1UL<<18)   // hysteresis programming is
enabled
```

By default, hysteresis levels are selected at 25% of VCC (low) and 75% of VCC (high). User can set hysteresis levels using the layer-specific function:

```
DqAdv40xSetHyst(int hd, int devn, uint16 level0,
                uint16 level1)
```

`level0` and `level1` are 10-bit relative values for low and high hysteresis levels.

3.2 Data representation

Layer \ Bits	31…24	23…12	11…0
DIO-401	reserved	DIn23…12	DIn11…0
DIO-402	reserved	DOut23…12	DOut11…0
DIO-405	reserved	N/A	DIn/Out11…0

Data representation is straightforward.
Please note that output lines on DIO-405 layer used to occupy bits 11…0. Thus, to set up all lines into one, you have to write 0x000fff to DIO-405. State of bits 31…12 don't matter.

3.3 Configuration settings

Configuration setting are passed in `DqCmdSetCfg()` function.
Not all configuration bits apply to DIO-40x layers.

The following bits are used:

```
#define DQ_LN_MAPPED     (1L<<15)  // For WRRD (DMAP) devices (automatically
selected)
#define DQ_LN_ACTIVE     (1L<<1)   // "STS" LED status
#define DQ_LN_ENABLED    (1L<<0)   // enable operations
```

The AO-40x has a range of layer-specific settings as follows.

Upper part of the configuration word – DIO-40x specific:

```
#define DQ_L401_HYSTEN      (1UL<<18)   // hysteresis programming is
enabled
```

The following modes are reserved for future use:

```
#define DQ_L401_MODESCAN   (FIFO_MODESCAN)  // single scan update mod (no
buffer)
#define DQ_L401_MODEDGE    (1UL << 16)      // edge detect mode
#define DQ_L401_MODEFIFO   (FIFO_MODEFIFO)  // continuous acquisition with FIFO
                                            // (simplified buffer)
#define DQ_L401_MODECONT   (FIFO_MODECONT)  // continuous acquisition
(buffered)
```

`DQ_LN_ACTIVE` is needed to switch on "STS" LED on CPU layer.
`DQ_LN_ENABLE` enables all operations with the layer

3.4 Channel list settings

Channel list is not required.

3.5 Layer-specific commands and parameters

There are two layer-specific functions defined:

- `DqAdv40xWrite()`
  This function writes 24-bit word to the DIO-40x layer using `DQCMD_WRCHNL.`
- `DqAdv40xRead()`
  This function reads input status using `DQCMD_RDCHNL`.
- `DqAdv40xSetHyst()`
  This function sets hysteresis levels.

These functions can be called anytime in configuration and operation mode.

3.6 Using layer in ACB mode

DIO-40x layers currently do not support ACB mode.

3.7 Using layer in DMap mode

This example shows communication between two layers: a layer 0 DI-401, and a layer 1 DO-402.

For a DIO-405, `DEVNIN` and `DEVNOUT` would be the same, and we'd assign a value only to bits 0-11 of `ooffset`, and read bits 0-11 of `ioffset`.

```
#include "PDNA.h"
```

1. Start DQE engine

```
#ifndef _WIN32
    DqInitDAQLib();
#endif

    // Start engine
    DqStartDQEngine(1000*10, &pDqe, NULL);

    // open communication with IOM
    DqOpenIOM(IOM_IPADDR0, DQ_UDP_DAQ_PORT, TIMEOUT_DELAY,
&DQRdCfg);
```

```
    // Set hysteresis at this point
    DqAdv40xSetHyst(hd0, DEVNIN, 0x132, 0x2CA);

    // Receive IOM crucial identification data
    DqCmdEcho(hd0, DQRdCfg);

    for (i = 0; i < DQ_MAXDEVN; i++) {
        if (DQRdCfg->devmod[i]) {
            printf("Model: %x Option: %x\n", DQRdCfg->devmod[i],
DQRdCfg->option[i]);
        } else {
            break;
        }
    }
```

2. Create and initialize host and IOM sides

```
    DqDmapCreate(pDqe, hd0, &pBcb, UPDATE_PERIOD, &dmapin,
&dmapout);
```

3. Add channels into DMap

```
    DqDmapSetEntry(pBcb, DEVNIN, DQ_SS0IN, 0, DQ_ACB_DATA_RAW, 1,
&ioffset);
    DqDmapSetEntry(pBcb, DEVNOUT, DQ_SS0OUT, 0, DQ_ACB_DATA_RAW,
1, &ooffset));

    DqDmapInitOps(pBcb);
    DqeSetEvent(pBcb,
DQ_eDataAvailable|DQ_ePacketLost|DQ_eBufferError|DQ_ePacketOOB);
```

4. Start operation

```
    DqeEnable(TRUE, &pBcb, 1, FALSE);
```

5. Process data

```
    while (keep_looping) {

        DqeWaitForEvent(&pBcb, 1, FALSE, timeout, &eventsin);

        if (eventsin & DQ_eDataAvailable) {
            datarcv++;
            printf("\ndata %08x ", *(uint32*)ioffset);
            *(uint32*)ooffset = datarcv;
        }
```

```
    }
```

6. Stop operation

```
    DqeEnable(FALSE, &pBcb, 1, FALSE);
```

7. Clean up

```
    DqDmapDestroy(pBcb);
    DqStopDQEngine(pDqe);
    DqCloseIOM(hd0);
#ifndef _WIN32
    DqCleanUpDAQLib();
#endif
```

4 Appendix

Appendix A - Accessories

The following cables and STP boards are available for the DIO-401/2/5 layer.

DNA-PC-902
+24V power conversion layer; supplies +24V to external devices at up to 40W

DNA-CBL-37
3ft, 37-way flat ribbon cable; connects layers to terminal panel.

DNA-DIO-O22
Accessory panel for PowerDNA DIO layers

DNA-STP-37
37-way screw terminal panel

DNA-STP-37D
37-way direct-connect screw terminal panel

Appendix B - Layer verification

The DIO-40x layers do not require calibration.
Layer verification is performed using “simod 1” command. To access it, the user should attach serial interface to the PowerDNA cube and run serial terminal program on the host PC. For DIO-40x “simod 1” command allows to read and write port (“r” and “w” command) as well as select hysteresis DAC (“1” and “2”) and adjust it using “[,],{,}” keys.
“q” or Esc causes the routine to exit.
The verification is done by setting up hysteresis levels (default are 25% for low and 75% for high ground levels) and continuously reading inputs while changing voltage on inputs. The easiest way to verify output is to attach LEDs between layer outputs and DGND in series with proper resistors. For example, you can use 2 to 4.7 KOhm resistors to limit current flowing thru LEDs.