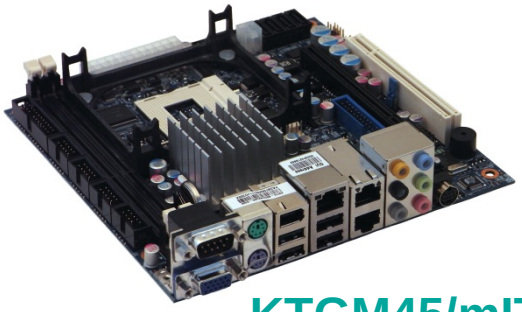
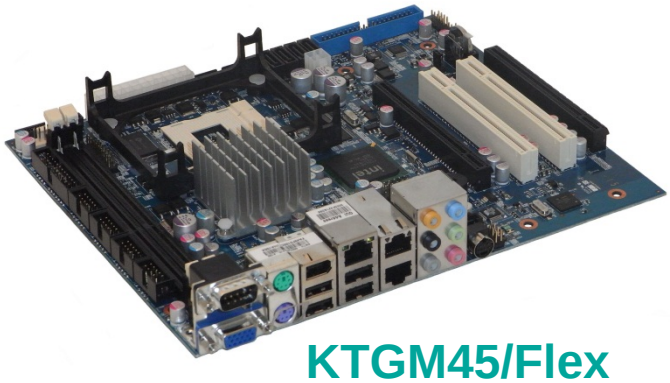
» Kontron User's Guide «



KTGM45/mITX



KTGM45/Flex

KTGM45/ATXE

KTGM45 Users Guide

KTD-N0793-L

Document revision history.

Revision	Date	By	Comment
L	Sept. 14th 2011	MLA	Added System Sensor position to pictures. Added available power load info when using +12V only input.
K	Aug. 29th 2011	MLA	Correction to KTGM45 variant table. More clear description of PCIe support. Removed “pending” for ESD/EMI standard conformity. Warning removed on page 17. TV-out connector not mounted. CPU socket info updated.
J	Jan. 21st 2011	MLA	Corrected version of the Standard 60950-1. Added info about Storage conditions. Added info of Memory Test.
I	Jan. 10th 2011	MLA	GMA X4500HD corrected to GMA 4500MHD (+related corrections). MTBF update.
H	Dec. 22nd 2010	MLA	SATA4/5 swapped on mITX page 24. ATXPWR connector types corrected. Added Bios setting “Boot Fail Option”. Added note to the “Boot Display Device” setting when using ADD2-LVDS card. Update of chapter “System Memory Support”. Updated CF details page 12 and 39. Corrected miniPCIe pin 7 and pin 24 info.
G	Oct. 18th 2010	MLA	Corrections to List of Supported Processors. Note for RAID selection in BIOS. Corrections to PCI slot. Connector list correction.
F	Sep. 1st 2010	MLA	PCIe x4 fully changed to PCIe x1. Minor layout corrections. Added note for using both On-board Graphics and PCIe card.
E	Aug. 31st 2010	MLA	P7350 added. P8800 Thermal Guideline value corrected. P8400 Speed corrected. Chapter 2.4 corrections. Note for minimum RPM when using Fan PN 1036-2048. Support for ADD2-CRT added. Some pictures updated.
0-D	-	MLA	Revision text removed in revision K

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- CPU Board
  1. Type.
  2. Part Number (find PN on label)
  3. Serial Number if available (find SN on label)
- Configuration
  1. CPU Type, Clock speed
  2. DRAM Type and Size.
  3. BIOS Revision (Find the Version Info in the BIOS Setup).
  4. BIOS Settings different than *Default* Settings (Refer to the BIOS Setup Section).
- System
  1. O/S Make and Version.
  2. Driver Version numbers (Graphics, Network, and Audio).
  3. Attached Hardware: Harddisks, CD-rom, LCD Panels etc.

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1. Damage, deterioration or malfunction resulting from:
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   B. Repair or attempted repair by anyone not authorized by KONTRON Technology.
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2. ANY OTHER DAMAGES, WHETHER INCIDENTAL, CONSEQUENTIAL OR OTHERWISE.
3. ANY CLAIM AGAINST THE CUSTOMER BY ANY OTHER PARTY.

Contents

Introduction

This manual describes the KTGM45/mITX, KTGM45/Flex and KTGM45/ATXE boards made by KONTRON Technology A/S. The boards will also be denoted KTGM45 family if no differentiation is required.

The KTGM45 boards supports the Intel® Core™ 2 Extreme Mobile Processor (Penryn), the Intel® Core™2 Quad Mobile processor (Penryn) Q9100, the Intel® Core™2 Duo Mobile processor (Penryn) and Intel® Celeron® (Meron). At least one type Intel® Core™2 Duo processor (Penryn) has successfully been tested.

KTGM45 variants	Format	PCI	PCIe x1	miniPCIe	ETH	Firewire	CF	HP RTC
KTGM45/mITX Plus	mITX	1	-	1	3	2	1	1
KTGM45/mITX Std	mITX	1	-	1	3	2	-	-
KTGM45/mITX Basic	mITX	1	-	1	1	-	-	-
KTGM45/Flex	Flex	2	1	-	3	2	-	-
KTGM45/ATXE	ATX	5	1	-	3	2	-	1

Use of this Users Guide implies a basic knowledge of PC-AT hard- and software. This manual is focused on describing the KTGM45 Board's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure stated in the following chapter before switching-on the power.

All configuration and setup of the CPU board is either done automatically or manually by the user via the CMOS setup menus. Only exception is the Clear CMOS jumper (J13).

1 Installation procedure

1.1 Installing the board

To get the board running, follow these steps. In some cases the board shipped from KONTRON has already components like DRAM, CPU and cooler mounted. In this case relevant steps below, can be skipped.

1. **Turn off the PSU (Power Supply Unit)**

Warning: Turn off PSU (Power Supply Unit) completely (no mains power connected to the PSU) or leave the Power Connectors unconnected while configuring the board. Otherwise components (RAM, LAN cards etc.) might get damaged.
Do not use PSU's without 3.3V monitoring watchdog, which is standard feature in ATX PSU's. Running the board without 3.3V connected will damage the board after a few minutes.

2. **Insert the DDR3 DIMM 240pin DRAM module(s)**
   Be careful to push it in the slot(s) before locking the tabs. For a list of approved DDR3 DIMM modules contact your Distributor or FAE. DDR3-800/1066 DIMM 240pin (PC3-6400/PC3-8500) are supported.

3. **Install the processor**
   The CPU is keyed and will only mount in the CPU socket in one way. Use the handle to open/ close the CPU socket. Penryn and Meron CPU's via mPGA479 or mPGA478 ZIF Socket are supported, refer to supported processor overview for details.

4. **Cooler Installation**
   Use heat paste or adhesive pads between CPU and cooler and connect the Fan electrically to the FAN_CPU connector.

5. **Connecting Interfaces**
   Insert all external cables for hard disk, keyboard etc. A CRT monitor must be connected in order to change CMOS settings.

6. **Connect and turn on PSU**
   Connect PSU to the board by the ATX/BTXPWR and the 4-pin ATX+12V connectors. Alternatively use only the 4-pin ATX+12V connector if single voltage operation (+12V +/-5%) is requested. Notice that single voltage operation has limited power support for add-on cards etc. Turn on power.

7. **Power Button**
   The PWRBTN_IN must be toggled to start the Power supply; this is done by shorting pins 16 (PWRBTN_IN) and pin 18 (GND) on the FRONTPNL connector (see Connector description). A "normally open" switch can be connected via the FRONTPNL connector.

8. **BIOS Setup**
   Enter the BIOS setup by pressing the <Del> key during boot up.
   Enter Exit Menu and Load Optimal Defaults.
   Refer to the "BIOS Configuration / Setup" section of this manual for details on BIOS setup.

Note: To clear all CMOS settings, including Password protection, move the Clear CMOS jumper in the Clear CMOS position (with or without power) for ~10 sec. This will Load Failsafe Defaults and make sure Secure CMOS is disabled.

9. **Mounting the board to chassis**

Warning: When mounting the board to chassis etc. please notice that the board contains components on both sides of the PCB which can easily be damaged if board is handled without reasonable care. A damaged component can result in malfunction or no function at all.

When fixing the Motherboard on a chassis it is recommended using screws with integrated washer and having diameter of ~7mm.

Note: Do not use washers with teeth, as they can damage the PCB and may cause short circuits.

1.2 Requirement according to IEC60950

Users of KTGM45 family boards should take care when designing chassis interface connectors in order to fulfil the IEC60950 standard:

When an interface/connector has a VCC (or other power) pin, which is directly connected to a power plane like the VCC plane:

To protect the external power lines of the peripheral devices, the customer has to take care about:

- That the wires have suitable rating to withstand the maximum available power.
- That the enclosure of the peripheral device fulfils the fire protecting requirements of IEC60950.

Lithium Battery precautions:

CAUTION! Danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by manufacturer. Dispose of used batteries according to the manufacturer's instructions.	**VORSICHT!** Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch den selben oder einen vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.
ADVARSEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.	**ADVARSEL** Eksplosjonsfare ved feilaktig skifte av batteri. Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten. Brukte batterier kasseres i henhold til fabrikantens instruksjoner.
VARNING Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.	**VAROITUS** Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laltevalmistajan suosittelemaan tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

2 System specification

2.1 Component main data

The table below summarizes the features of the KTGM45/mITX and KTGM45/Flex embedded motherboards.

Form factor	KTGM45/mITX: miniITX (170,18 mm by 170,18 mm) KTGM45/Flex: Flex-ATX (190,5 mm by 228,6 mm) KTGM45/ATXE: ATX (190,5 mm by 304,0 mm)
Processor	Support the following Penryn and Meron CPU's via mPGA479 or mPGA478 ZIF Socket • Intel® Core™ 2 Extreme Mobile Processor (Penryn) • Intel® Core™2 Quad Mobile processor (Penryn) Q9100 • Intel® Core™2 Duo Mobile processor (Penryn) • Intel® Celeron® (Meron) Up to 1066MHz system bus and 1/3/6/12MB internal cache.
Memory	• 2 pcs DDR3 DIMM 240pin DRAM sockets • Dual channel interleaved mode support • Support for DDR3 800/1066MHz (PC3-6400/PC3-8500) • Support system memory from 512MB and up to 2x 4GB. Note: Less than 4GB displayed in System Properties using 32bit OS (Shared Video Memory/PCI resources is subtracted) • ECC not supported
Chipset	Intel GM45+ICH9ME Chipset consisting of: • Intel® 82GM45 Graphics Memory Controller Hub (GMCH) • Intel® ICH9ME I/O Controller Hub
RTC	• RTC (Real Time Clock) HP (High Precision) (not available on KTGM45/mITX Std/Basic). Precision is +/-10 sec/month in the temperature range 0 – 60ºC.
Security	• Intel® Integrated TPM 1.2 support
Management	• Intel® Active Management Technology (Intel® AMT) 4.0
Video	Intel Gen 5.0 integrated graphics engine (Intel® GMA 4500MHD) • DVMT 5.0 (Dynamic Video Memory Technology), allowing up to more than 512MB dynamically allocated Video Memory (System memory is allocated when it is needed). • On-board support for analogue CRT and LVDS panel. • Analogue CRT Display Support (on-board), 300-MHz, 24 bit integrated RAMDAC with support for analogue monitors up to QXGA (2048x1536 pixels) @ 75 Hz • LVDS panel Support (on-board), 18/24 bit colour in up to WUXGA (1920x1200 pixels @60 Hz and SPWG (VESA) colour coding. OpenLDI /JEIDA colour coding 18 bit colour with or without Dithering). • (TV-out connector not mounted, Component, S-Video and Composite interfaces, NTSC/PAL and HDTV Graphics mode. 10-bit DAC. Macrovision not supported). • Multiplexed PCIe x16, SDVO and TMDS. • PCIe x16 (PCI Express 2.0) support also PCIe Graphics card. • SDVO (Serial Digital Video Out) ports (2 channels) for additional ADD2 (Advanced Digital Display 2) cards supporting second CRT monitor or Dual LVDS/DVI panels. • TMDS (Transition Minimized Differential Signalling) (3 channels) for additional, HDMI support with HDCP and HD Audio, DVI support, or DP (DisplayPort) support with 8/10 bit colours in WQXGA (2560x1600 pixels) and HDCP. Dual independent pipes for Mirror and Dual independent display support with combinations of SDVO/TMDS port devices and on-board CRT/LVDS.
Audio	Audio, 7.1 Channel High Definition Audio Codec using the VIA 1708B codec • Line-out • Line-in • Surround output: SIDE, LFE, CEN, BACK and FRONT • Microphone: MIC1 and MIC2 • CDROM in • SPDIF (electrical Interface only) • On-board speaker

(Continues)

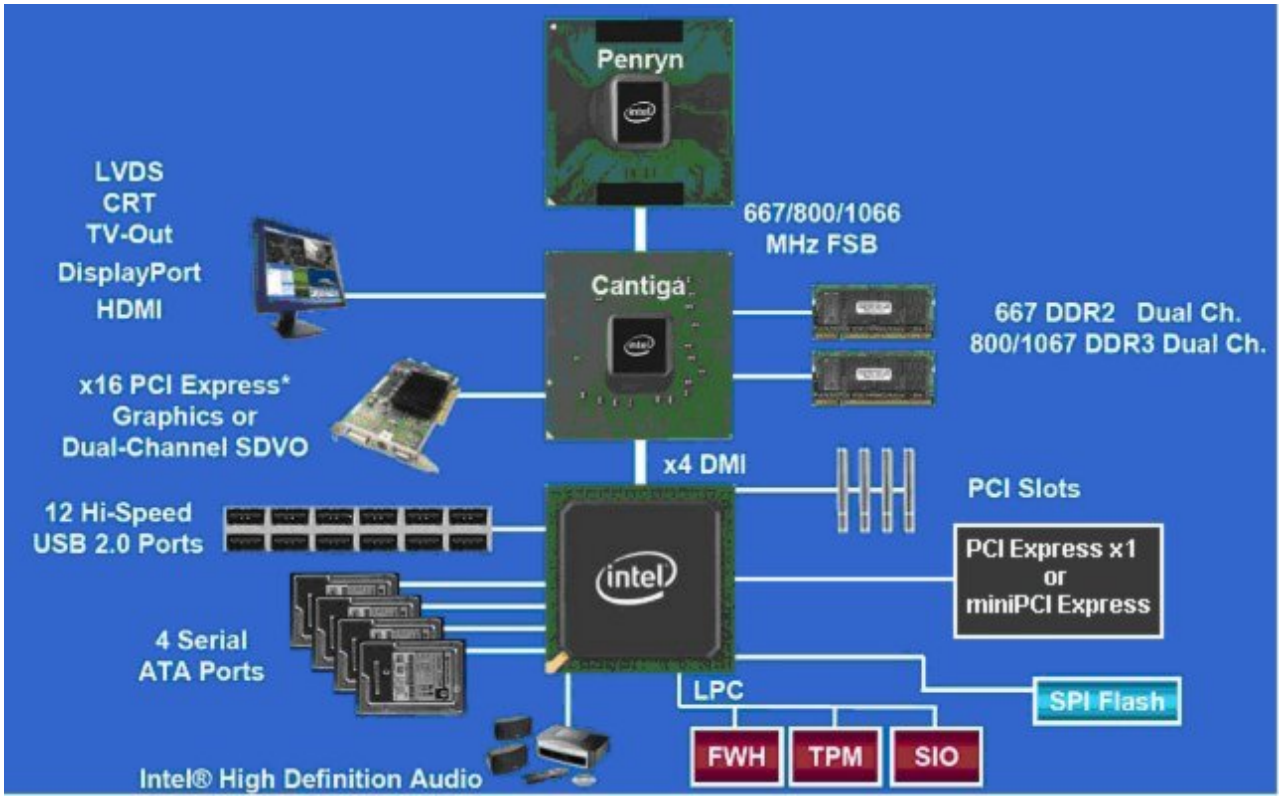
I/O Control	Two Winbond W83627DHG LPC Bus I/O Controllers
Peripheral interfaces	• Four USB 2.0 ports on I/O area • Eight USB 2.0 ports on internal pinrows • One IEEE 1394a-2000 (up to 400M bits/s) on I/O area (not available on KTGM45/mITX Basic) • One IEEE 1394a-2000 (up to 400M bits/s) on internal pinrows (not available on KTGM45/mITX Basic) • Four Serial ports (RS232) • Four Serial ATA-300 IDE interfaces with RAID 0/1 support • One PATA 66/100/133 interface with support for 2 devices • CF (Compact Flash) interface (KTGM45/mITX Plus only) supporting CF type I and II complying with +5V supply and Vih min. 2.0V and Vil max. 0.8V. (UDMA2 max.). Note that only one PATA device is supported when CF is used and only by use of 40-wire cable (not 80-wire cable). Optionally use SATA devices. • PS/2 keyboard and mouse ports
LAN Support	• 1x 10/100/1000Mbits/s LAN (ETHER1) using Intel® Boazman-LM WG82567LM Gigabit PHY connected to ICH9M Integrated GbE MAC supporting AMT 4.0 • 2x 10/100/1000Mbits/s LAN (ETHER2/ETHER3)using Intel® Hartwell 82574L PCI Express controllers (not available on KTGM45/mITX Basic) • PXE Netboot supported. • Wake On LAN (WOL) supported (only on ETHER1).
BIOS	• Kontron Technology / AMI BIOS (core version) • Support for Advanced Configuration and Power Interface (ACPI 3.0b), Plug and Play o Suspend To Ram o Suspend To Disk o Intel Speed Step • Secure CMOS/ OEM Setup Defaults • “Always On” BIOS power setting • RAID Support (RAID modes 0 and 1)
Expansion Capabilities	• PCI Bus routed to PCI slot(s) (PCI Local Bus Specification Revision 2.3) o KTGM45/mITX: 1 slot PCI 2.3, 32 bits, 33 MHz, 5V compliant o KTGM45/Flex: 2 slots PCI 2.3, 32 bits, 33 MHz, 5V compliant o KTGM45/ATXE: 5 slots PCI 2.3, 32 bits, 33 MHz, 5V compliant • PCI-Express bus routed to PCIe (PCI-Express) slot(s) (PCIe 1.1) o KTGM45/mITX: 1 slot PCIe x16 (PCIe 2.0) 1 slot miniPCI-Express (PCIe 1.1) o KTGM45/Flex: 1 slot PCIe x16 (PCIe 2.0) 1 slot PCIe x1 (x16 connector) (PCIe 1.1) o KTGM45/ATXE: 1 slot PCIe x16 (PCIe 2.0) 1 slot PCIe x1 (x16 connector) (PCIe 1.1) • SMBus routed to FEATURE, PCI slot, PCI Express • LPC Bus routed to TPM connector (not available on KTGM45/mITX) • DDC Bus routed to CRT connector • 8 x GPIOs (General Purpose I/Os) routed to FEATURE connector
Hardware Monitor Subsystem	• Smart Fan control system, support Thermal® and Speed® cruise for three on-board Fan control connectors: FAN_CPU, FAN_SYS and FEATURE (AUXFAN in BIOS) • Three thermal inputs: CPU die temperature, System temperature and External temperature input routed to FEATURE connector. (Precision +/- 3ºC) • Voltage monitoring • Intrusion (Case Open) detect input
Power Supply Unit	ATX/BTX (w. ATX+12V) PSU for full PCI/PCIe load. Alternatively +12V single supply via ATX+12V (4-pole) connector, but with limitation to PCI/PCIe load.
Operating Systems Support	• WinXP • WinVista • Windows 7 • Linux (limitations may apply)

(Continues)

Environmental Conditions	**Operating**: 0°C – 60°C operating temperature (forced cooling). It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within allowed temperature range. 10% - 90% relative humidity (non-condensing) **Storage**: -20°C – 70°C; lower limit of storage temperature is defined by specification restriction of on-board CR2032 battery. Board with battery has been verified for storage temperature down to -40°C by Kontron. 5% - 95% relative humidity (non-condensing) **Electro Static Discharge (ESD) / Radiated Emissions (EMI):** All Peripheral interfaces intended for connection to external equipment are ESD/ EMI protected. EN 61000-4-2:2000 ESD Immunity EN55022:1998 class B Generic Emission Standard. **Safety:** IEC 60950-1: 2005, 2nd Edition UL 60950-1 CSA C22.2 No. 60950-1 Product Category: Information Technology Equipment Including Electrical Business Equipment Product Category CCN: NWGQ2, NWGQ8 File number: E194252 **Theoretical MTBF:** 407.023 / 221.169 hours @ 40ºC / 60ºC for the KTGM45/mITX 476.953 / 244.536 hours @ 40ºC / 60ºC for the KTGM45/Flex 352.559 / 174.306 hours @ 40ºC / 60ºC for the KTGM45/ATXE **Restriction of Hazardous Substances (RoHS):** All boards in the KTGM45 family are RoHS compliant. **Capacitor utilization:** No Tantalum capacitors on board Only Japanese brand Solid capacitors rated for 100 ºC used on board
Battery	Exchangeable 3.0V Lithium battery for on-board Real Time Clock and CMOS RAM. Manufacturer Panasonic / Part-number CR-2032L/BN, CR2032NL/LE or CR-2032L/BE. Approximate 6 years retention. Current draw is 4µA when PSU is disconnected. **CAUTION: Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.**

2.2 System overview

The block diagram below shows the architecture and main components of the KTGM45. The two key components on the board are the Intel® GM45 (Cantiga) and Intel® ICH9ME Chipset.
Some components (PCI Slots, PCI Express and miniPCI Express) are optional depending on board type.



2.3 Processor Support Table

The KTGM45 is designed to support the following PGA478 processors (up to 60W power consumption):

Intel® Core™ 2 Extreme Mobile Processor (Penryn)

Intel® Core™ 2 Quad Mobile Processor (Penryn)

Intel® Core™ 2 Duo Mobile Processor (Penryn)

Intel® Core™ 2 Duo Processor (Penryn)

Intel® Celeron® (Penryn)

Intel® Celeron® (Meron)

In the following list you will find all CPU's supported by the chipset in according to Intel but also other CPU's if successfully tested.

Embedded CPU's are indicated by green text, successfully tested CPU's are indicated by **highlighted** text, successfully tested embedded CPU's are indicated by **green and highlighted** text and failed CPU's are indicated by red text.

Some processors in the list are distributed from Kontron, those CPU's are marked by an * (asterisk). However please notice that this marking is only guide line and maybe not fully updated.

Processor Brand	Clock Speed [GHz]	Bus Speed [MHz]	Cache [MB]	CPU Number	sSpec no.	Stepping	Thermal Guideline [Watt]
Intel® Core™2 Extreme Mobile (Penryn)	**3.06**	**1066**	**6**	**X9100**	**SLB48**	**C0**	**45**
	2.53	**1066**	**12**	**QX9300**	**SLB5J**	**E0**	**45**
Intel® Core™2 Quad Mobile (Penryn)	**2.26**	**1066**	**12**	**Q9100 ***	**SLB5G**	**E0**	**45**
Intel® Core™ 2 Duo Mobile (Penryn)	3.06	1066	6	T9900	SLGEE	E0	35
	2.93	1066	6	T9800	SLGES	E0	35
	2.80	1066	6	P9700	SLGQS	E0	28
	2.80	**1066**	**6**	**T9600**	**SLG9F**	**E0**	**35**
	2.80	1066	6	T9600	SLB47	C0	35
	2.66	1066	6	P9600	SLGE6	E0	25
	2.66	1066	6	T9550	SLGE4	E0	35
	2.66	1066	3	P8800	SLGLR	R0	25
	2.53	**1066**	**6**	**T9400 ***	**SLGE5**	**E0**	**35**
	2.53	**1066**	**6**	**P9500**	**SLB4E**	**C0**	**25**
	2.53	1066	6	P9500	SLGE8	E0	25
	2.53	1066	6	T9400	SLB46	C0	35
	2.53	1066	3	P8700	SLGFE	R0	25
	2.40	1066	3	P8600	SLGA4	M0	25
	2.40	1066	3	P8600	SLGFD	R0	25
	2.26	**1066**	**3**	**P8400 ***	**SLGFC**	**R0**	**25**
	2.26	1066	3	P8400	SLGCL	R0	25
	2.26	1066	3	P8400	SLGCF	R0	25
	2.26	1066	3	P8400	SLGCQ	R0	25
	2.26	1066	3	P8400	SLGCC	R0	25
	2.26	1066	3	P8400	SLB3R	M0	25
	2.26	1066	3	P8400	SLB3Q	M0	25
Intel® Core™2 Duo (Penryn)	**2.00**	**1066**	**3**	**P7350**	**SLB53**	**M0**	**25**
Intel® Celeron™ (Penryn)	2.20	800	1	900	SLGLQ	R0	35
	1.90	**800**	**1**	**T3100 ***	**SLGEY**	**R0**	**35**
Intel® Celeron™ (Merom)	2.16	667	1	585	SLB6L	M0	31
	2.00	**667**	**1**	**575 ***	**SLB6M**	**M0**	**31**
	1.83	667	1	T1700	SLB6H	M0	35
	1.66	667	1	T1600	SLB6J	M0	35

2.4 System Memory support

The KTGM45 board has two DDR3 DIMM sockets and support the following memory features:

- 1.5V (only) 240-pin DDR3 SDRAM DIMMs with gold-plated contacts
- DDR3-800 (PC3-6400) and DDR3-1066 (PC3-8500)
- DDR3-800/1066 DIMM with SPD timings supported
- Unbuffered, single-sided x8/x16 or double-sided x8/x16 DIMMs
- Supports one or two rank populated DIMM's.
- 8GB (2x 4GB) max. total system memory using 64-bit OS. (Shared Video Memory is subtracted).
- 4GB maximum total system memory using 32-bit OS. ~3GB is displayed in System Properties. (Shared Video Memory is subtracted).
- Minimum total system memory: 512 MB
- Non-ECC DIMMs

The installed DDR3 SDRAM should support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read and configure the memory controller for optimal performance. If non-SPD memory is used, the BIOS will attempt to configure the memory settings, but performance and reliability may be impacted.

Memory Operating Frequencies
Regardless of the DIMM type used, the memory frequency will either be equal to or less than the processor system bus frequency. For example, if DDR3 800 memory is used with an 800 MHz system bus frequency processor, the memory clock will operate at 400 MHz. The table below lists the resulting operating memory frequencies based on the combination of DIMMs and processors.

DIMM Type	Module name	Memory Data transfers [Mill/s]	Processor system bus frequency [MHz]	Resulting memory clock frequency [MHz]	Peak transfer rate [MB/s]
DDR3 800	PC3-6400	800	667	333	5300
DDR3 800	PC3-6400	800	800	400	6400
DDR3 800	PC3-6400	800	1066	400	6400
DDR3 1066	PC3-8500	1066	667	333	5300
DDR3 1066	PC3-8500	1066	800	400	6400
DDR3 1066	PC3-8500	1066	1066	533	8533

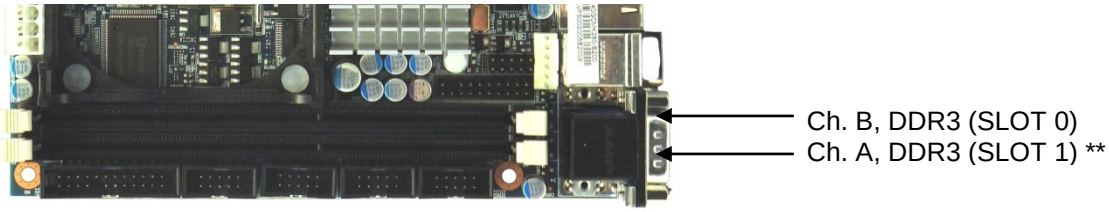
Notes: Kontron offers the following memory modules:
- P/N 1028-6891, DDR3-RAM, **1GB**, 240p, 1066MHZ, PC3-8500, DIMM
- P/N 1030-5722, DDR3-RAM, **1GB**, 240p, 1333MHZ, PC3-10600, DIMM
- P/N 1030-5747, DDR3-RAM, **2GB**, 240p, 1066MHZ, PC3-8500, DIMM
- P/N 1028-6892, DDR3-RAM, **2GB**, 240p, 1333MHZ, PC3-10600, DIMM
- P/N 825534, DDR3-RAM, **4GB**, 240P, 1333MHZ, PC3-10600, DIMM
- Faster RAM than PC3-10600 can be used but will run at lower speed.

Memory Configurations
The KTGM45 boards support the following three types of memory organization:

1. Dual channel (Interleaved) mode. This mode offers the highest throughput. Dual channel mode is enabled when the installed memory capacities of both DIMM channels are equal. Technology and device width can vary from one channel to the other but the installed memory capacity for each channel must be equal. If different speeds DIMMs are used between channels, the slowest memory timing will be used.

2. Single channel (Asymmetric) mode. This mode is equivalent to single channel bandwidth operation. This mode is used when only a single DIMM is installed or the memory capacities of channel A is bigger than of channel B. Technology and device width can vary from one channel to the other. If different speeds DIMMs are used between channels, the slowest memory timing will be used.

3. Flex mode. This mode provides the most flexible performance characteristics and is used if both channels are populated and at the same time the memory capacities of channel A is smaller than of channel B. Channel B will be divided into two parts. One part of channel B is used together with channel A and mapped to dual channel operation. The second part of channel B is mapped to single channel operation.



**** Note:**
Regardless of the memory configuration used (Dual Channel, Single Channel or Flex) the SLOT 1 **must** always be populated. This is a requirement of the Intel® Management Engine.

The below tables shows examples of possible Memory slot configurations for the support of the various Memory modes.

Dual Channel Interleaved Mode Configurations	
DDR3 SLOT 1 (Ch. A)	DDR3 SLOT 0 (Ch. B)
1 GB	1 GB
2 GB	2 GB

(The capacity of the Ch. A equals the capacity of Ch. B).

Single Channel Asymmetric Mode Configurations	
DDR3 SLOT 1 (Ch. A)	DDR3 SLOT 0 (Ch. B)
1 GB	
2 GB	

Dual Channel Flex Mode Configurations	
DDR3 SLOT 1 (Ch. A)	DDR3 SLOT 0 (Ch. B)
2 GB	1GB
1 GB	2 GB

The first 1GB of each of the Channels (A and B) will be used in Interleaved Mode and the remaining RAM will be used in Asymmetric Mode.

2.5 KTGM45 Graphics Subsystem

The KTGM45 use the Intel GM45 chipset for the graphical control. This chipset contains two separate, mutually exclusive graphics options. Either the Intel® GMA 4500MHD graphics engine (contained within the GM45 GMCH) is used, or a PCI Express x16 add-in card can be used. When a PCI Expressx16 add-in card is installed, the GMA 4500MHD graphics controller is disabled.

Dual independent pipe support, Mirror and Dual independent display support.
Dual Display support with combinations of SDVO/TMDS (Serial Digital Video Out/Transition Minimized Differential Signalling) port devices and on-board CRT/LVDS (Low Voltage Differential Signalling).

2.5.1 Intel® GMA 4500MHD

Features of the Intel GMA (Graphic Media Accelerator) 4500MHD graphics controller includes:

- High quality graphics engine supporting
  - DirectX10 and OpenGL 2.1 compliant
  - Shader Model 4.0 support
  - Intel ® Clear Video Technology
  - Core frequency of 533 MHz
  - Memory Bandwidth up to 17GB/s
  - 10 Execution Units
  - 1.6 GP/s and 2.7 GP/S pixel rate (DP output)
  - Hardware Acceleration full MPEG2, full VC-1 and full AVC
  - Full 1080p HD Video playback inclusive Blu-ray
  - Multiple Overlay Functionality
  - Dynamic Video Memory Technology (DVMT 5.0) support up to more than 512 MB

- Analogue Display (CRT)
  - 300 MHz Integrated 24-bit RAMDAC
  - Up to QXGA (2048x1536 pixels) @ 75 Hz refresh

- LVDS panel Support (on-board), 18/24 bit colours in up to WUXGA (1920x1200 pixels) @60 Hz and SPWG (VESA) colour coding. OpenLDI (JEIDA) colour coding is 18 bit with or without Dithering. Note that on-board LVDS port is disabled if ADD2-LVDS card is used.

- (TV-out connector not mounted, Component, S-Video and Composite interfaces, NTSC/PAL and HDTV Graphics mode. 10-bit DAC. Macrovision not supported).

- Multiplexed PCIe x16, SDVO and TMDS.
  - PCIe x16 (PCI Express 2.0) supports also PCIe Graphics card. Using PCIe Graphics card in combination with on-board graphics (VGA or LVDS) is possible if BIOS (from version KTGM4506) setting *Boots Graphic Adaptor Priority = IGD*. In this case on-board graphic will be Primary desktop and PCIe Graphics will be extended desktop. Note that PCIe Graphics driver shall be installed before the Intel Graphics driver.
  - SDVO ports (2 channels) for additional ADD2 (Advanced Digital Display 2) cards supporting second CRT monitor, LVDS or DVI (Digital Visual Interface) panel(s).
  - TMDS (2 channels) for additional, HDMI (High-Definition Multimedia Interface) support with HDCP (High-bandwidth Digital Content Protection) and HD Audio, DVI support, or DP (DisplayPort) support with 8/10 bit colours in WQXGA (2560x1600 pixels) and HDCP.
  - DVI, HDMI and DP support Hot-Plug.

2.5.2 DVMT 5.0 support

DVMT (Dynamic Video Memory Technology driven by OS driver) enables enhanced graphics and memory performance through highly efficient memory utilization. DVMT ensures the most efficient use of available system memory for maximum 2-D/3-D graphics performance. More than 512 MB of system memory can be allocated to DVMT on systems that have 1GB or more of total system memory installed. DVMT returns system memory back to the operating system when the additional system memory is no longer required by the graphics subsystem.

DVMT will always use a minimal fixed portion of system physical memory (as set in the BIOS Setup) for compatibility with legacy applications. An example of this would be when using VGA graphics under DOS. Once loaded, the operating system and graphics drivers allocate additional system memory to the graphics buffer as needed for performing graphics functions.

2.5.3 ADD2 card support

The KTGM45 board routes two multiplexed SDVO ports that are each capable of driving up to a 200 MHz pixel clock to the PCI Express x16 connector. The SDVO ports can be paired for a dual channel configuration to support up to a 400 MHz pixel clock. When an ADD2 (Advanced Digital Display) card is detected, the Intel GMA 4500 graphics controller is enabled and the PCI Express x16 connector is configured for SDVO mode. SDVO mode enables the SDVO ports to be accessed by the ADD2 card. An ADD2 card can either be configured to support simultaneous display with the primary VGA display or can be configured to support dual independent display as an extended desktop configuration with different colour depths and resolutions.

ADD2 cards can be designed to support one or two of the following configurations:
- LVDS
- DVI output (DVI-D)
- VGA output
- HDTV output

Currently available Kontron ADD2 cards
- P/N 820950, ADD2-LVDS-Dual (LVDS displays must have same display resolution and timing)
- P/N 820951, ADD2-DVI-Dual-Internal
- P/N 820952, ADD2-DVI-Dual
- P/N 820954, ADD2-CRT

Please visit the Kontron website (www.kontron.com) for details.

2.5.4 PCIe Passive Graphic card support

The KTGM45 board routes two TMDS ports that are each capable of driving up to a 200 MHz pixel clock to the PCI Express x16 connector. When a TMDS card is detected, the Intel GMA 4500 graphics controller is enabled and the PCI Express x16 connector is configured for TMDS mode. A TMDS card can either be configured to support simultaneous display with the primary VGA display or can be configured to support dual independent display as an extended desktop configuration with different colour depths and resolutions.

PCIe Passive Graphic cards can be designed to support the following configurations:
- TMDS for DVI 1.0
- Display Port
- HDMI support

Currently available Kontron PCIe Passive Graphic cards:
- P/N 820977, KT-PCIe-DVI-HDMI-I, (HDMI, and DVI with TMDS option).

Please visit the Kontron website (www.kontron.com) for details.

2.6 Power Consumption

In order to ensure safe operation, the ATX12V power supply must monitor the supply voltage and shut down if the supplies are out of range – refer to the hardware manual for the actual power supply specification.

The KTGM45/Flex board is powered through the ATX/BTX connector and ATX+12V connector. Both connectors must be used in according to the ATX12V PSU standard.

Optionally single +12V power supply unit can be used via ATX+12V connector when power line requirements for PCIe card, PCI card and "device on 24-pole plug" is below 7.6A on 3.3V, 5A on 5V, 25W on 3.3V and 5V in common, and 5A on 12V.

The requirements to the supply voltages are as follows:

Supply	Min	Max	Note
VCC3.3	3.168V	3.432V	Should be ±4% for compliance with the ATX specification
Vcc	4.75V	5.25V	Should be ±5% for compliance with the ATX specification. Should be minimum 5.00V measured at USB connectors in order to meet the requirements of USB standard.
+12V	11.4V	12.6V	Should be ±5% for compliance with the ATX specification
–12V	–13.2V	–10.8V	Should be ±10% for compliance with the ATX specification
-5V	-5,50V	-4.5V	Not required for the KTGM45 boards
5VSB	4.75V	5.25V	Should be ±5% for compliance with the ATX specification

Static Power Consumption

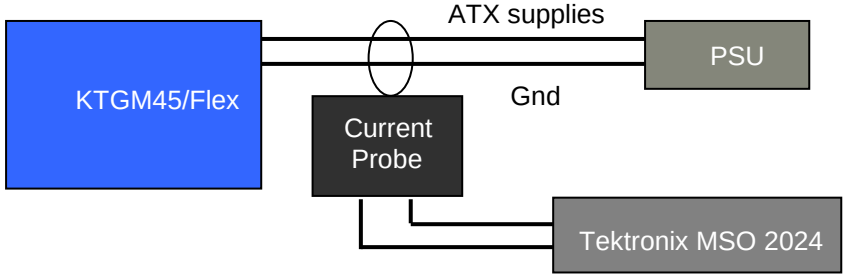
The power consumption of the KTGM45/Flex Board is measured under:

1- DOS, idle, mean
2- WindowsXP, Running 3DMARK 2001 & CPU BURN, mean
3- S1, mean
4- S3, mean
5- S4, mean

The following items were used in the test setup:

1. **Low Power Setup**: 2.0GHz (Celeron 575) & 1x 1GB Samsung 2Rx8 PC3-10600U-09-00-A0 DDR3 Ram
   High Power Setup: 2.53GHz (T9400) Core Duo & 2x 2GB Samsung 2Rx8 PC3-10600U-09-00-A0 DDR3 Ram
2. 12V active cooler (Kontron PN 823132).
3. USB Keyboard/Mouse (Logitech Corded Media Keyboard / Logitech First/Pilot Wheel MSE)
4. TFT (Samsung SyncMaster 953bw)
5. HD (Seagate Barracuda ST380815AS - 7200.10 - 80 GB)
6. ATX PSU (SHG computers - SCP400LN-PL)
7. Tektronix MSO 2024
8. Fluke Current Probe 80i-100S AC/DC

Test setup



Note: The Power consumption of CRT, HD and Fan is not included.

Low Power Setup (Celeron 575 + 1GB RAM) results:

DOS Idle, Mean, No external load		
Supply	Current draw	Power consumption
+12V	1.82A	21.84W
+5V	0.295A	1.475W
+3V3	1.4A	4.62W
-12V	-	0W
5VSB	-	0W
Total		27.935W
+12V only	2.7A	32.4W

Windows XP, mean 3DMARK2001 (Game 1 – Car Chase test) & CPUBURN		
Supply	Current draw	Power consumption
+12V	2.3A	27.6W
+5V	0.25A	1.25W
+3V3	1.14A	3.76W
-12V	0.05A	0.6W
5VSB	-	0W
Total		33.21W
+12V only	3.15A	37.8W

S1 Mode, Mean, No external load		
Supply	Current draw	Power consumption
+12V	1.33A	15.96W
+5V	0.15A	0.75W
+3V3	1.1A	3.63W
-12V	-	0W
5VSB	-	0W
Total		20.34W
+12V only	1.94A	23.28W

S3 Mode, Mean, No external load		
Supply	Current draw	Power consumption
+12V	0.00A	0W
+5V	0.00A	0W
+3V3	0.00A	0W
-12V	0.00A	0W
5VSB	0.13A	0.65W
Total		0.65W
+12V only	0.542A	6.504W

S4 Mode, Mean, No external load		
Supply	Current draw	Power consumption
+12V	0.00A	0W
+5V	0.00A	0W
+3V3	0.00A	0W
-12V	0.00A	0W
5VSB	0.1A	0.5W
Total		0.5W
+12V only	0.49A	5.88W

High Power Setup (Core 2 Duo Mobile T9400 + 1GB RAM) results:

DOS Idle, Mean, No external load		
Supply	Current draw	Power consumption
+12V	1.87A	22.44W
+5V	0.297A	1.485W
+3V3	1.38A	4.554W
-12V	-	0W
5VSB	-	0W
Total		28.479W
+12V only	2.76A	33.12W

Windows XP, mean 3DMARK2001 (Game 1 – Car Chase test) & CPUBURN		
Supply	Current draw	Power consumption
+12V	3.58A	42.96W
+5V	0.282A	1.41W
+3V3	1.48A	4.884W
-12V	0.052A	0.624W
5VSB	-	0W
Total		49.875W
+12V only	4.43A	53.16W

S1 Mode, Mean, No external load		
Supply	Current draw	Power consumption
+12V	1.29A	15.48W
+5V	0.158A	0.79W
+3V3	1.05A	3.465W
-12V	-	0W
5VSB	-	0W
Total		19.735W
+12V only	1.97A	23.64W

S3 Mode, Mean, No external load		
Supply	Current draw	Power consumption
+12V	0.00A	0W
+5V	0.00A	0W
+3V3	0.00A	0W
-12V	0.00A	0W
5VSB	0.49A	2.25W
Total		2.25W
+12V only	0.555A	6.66W

S4 Mode, Mean, No external load		
Supply	Current draw	Power consumption
+12V	0.00A	0W
+5V	0.00A	0W
+3V3	0.00A	0W
-12V	0.00A	0W
5VSB	0.50A	2.5W
Total		2.5W
+12V only	0.555A	6.66W

3 Connector Definitions

The following sections provide pin definitions and detailed description of all on-board connectors.

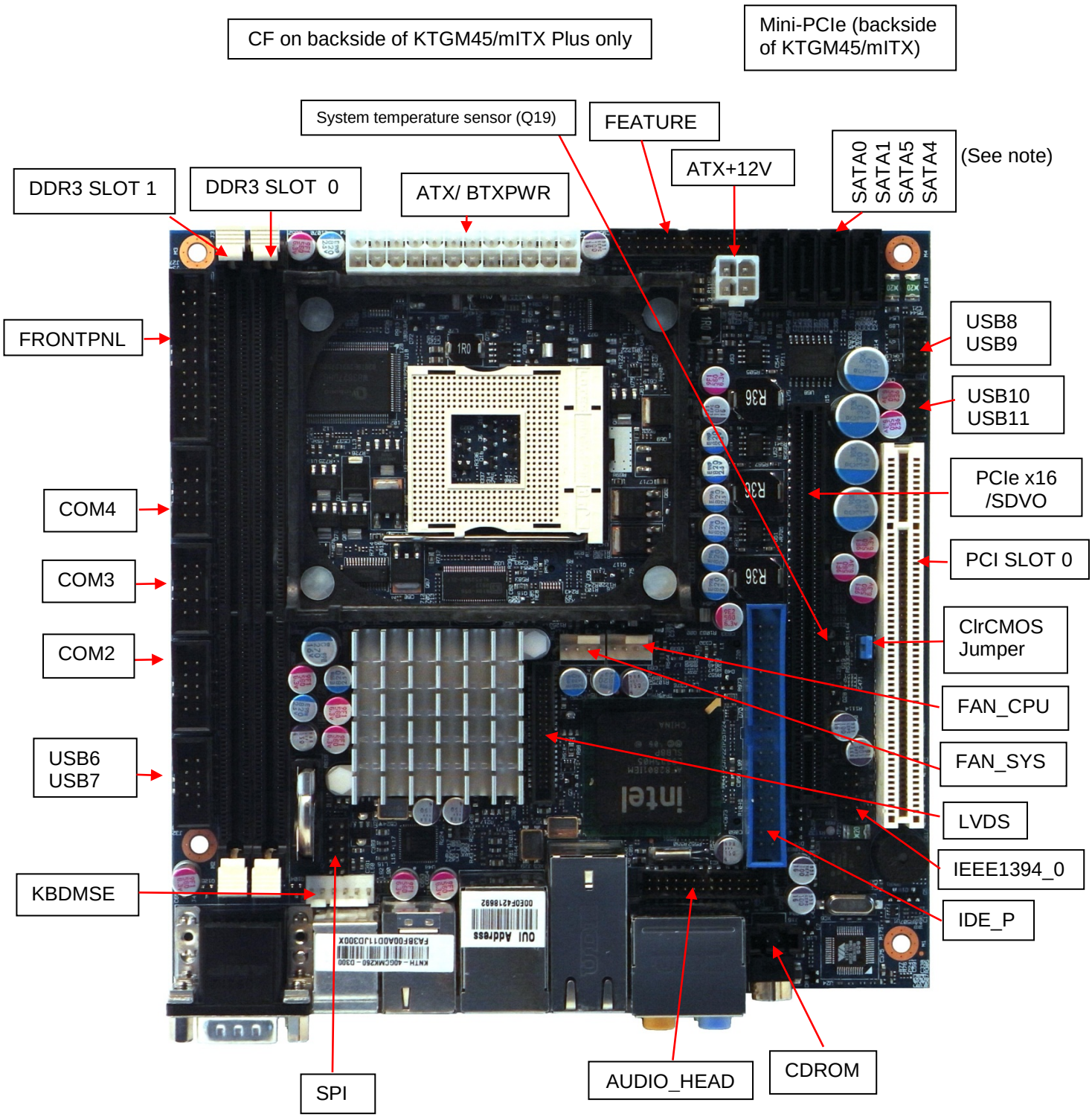
The connector definitions follow the following notation:

Column name	Description
Pin	Shows the pin-numbers in the connector. The graphical layout of the connector definition tables is made similar to the physical connectors.
Signal	The mnemonic name of the signal at the current pin. The notation “XX#” states that the signal “XX” is active low.
Type	AI: Analogue Input. AO: Analogue Output. I: Input, TTL compatible if nothing else stated. IO: Input / Output. TTL compatible if nothing else stated. IOT: Bi-directional tristate IO pin. IS: Schmitt-trigger input, TTL compatible. IOC: Input / open-collector Output, TTL compatible. IOD: Input / Output, CMOS level Schmitt-triggered. (Open drain output) NC: Pin not connected. O: Output, TTL compatible. OC: Output, open-collector or open-drain, TTL compatible. OT: Output with tri-state capability, TTL compatible. LVDS: Low Voltage Differential Signal. PWR: Power supply or ground reference pins.
	Ioh: Typical current in mA flowing out of an output pin through a grounded load, while the output voltage is > 2.4 V DC (if nothing else stated). Iol: Typical current in mA flowing into an output pin from a VCC connected load, while the output voltage is < 0.4 V DC (if nothing else stated).
Pull U/D	On-board pull-up or pull-down resistors on input pins or open-collector output pins.
Note	Special remarks concerning the signal.

The abbreviation *TBD* is used for specifications which are not available yet or which are not sufficiently specified by the component vendors.

3.1 Connector layout

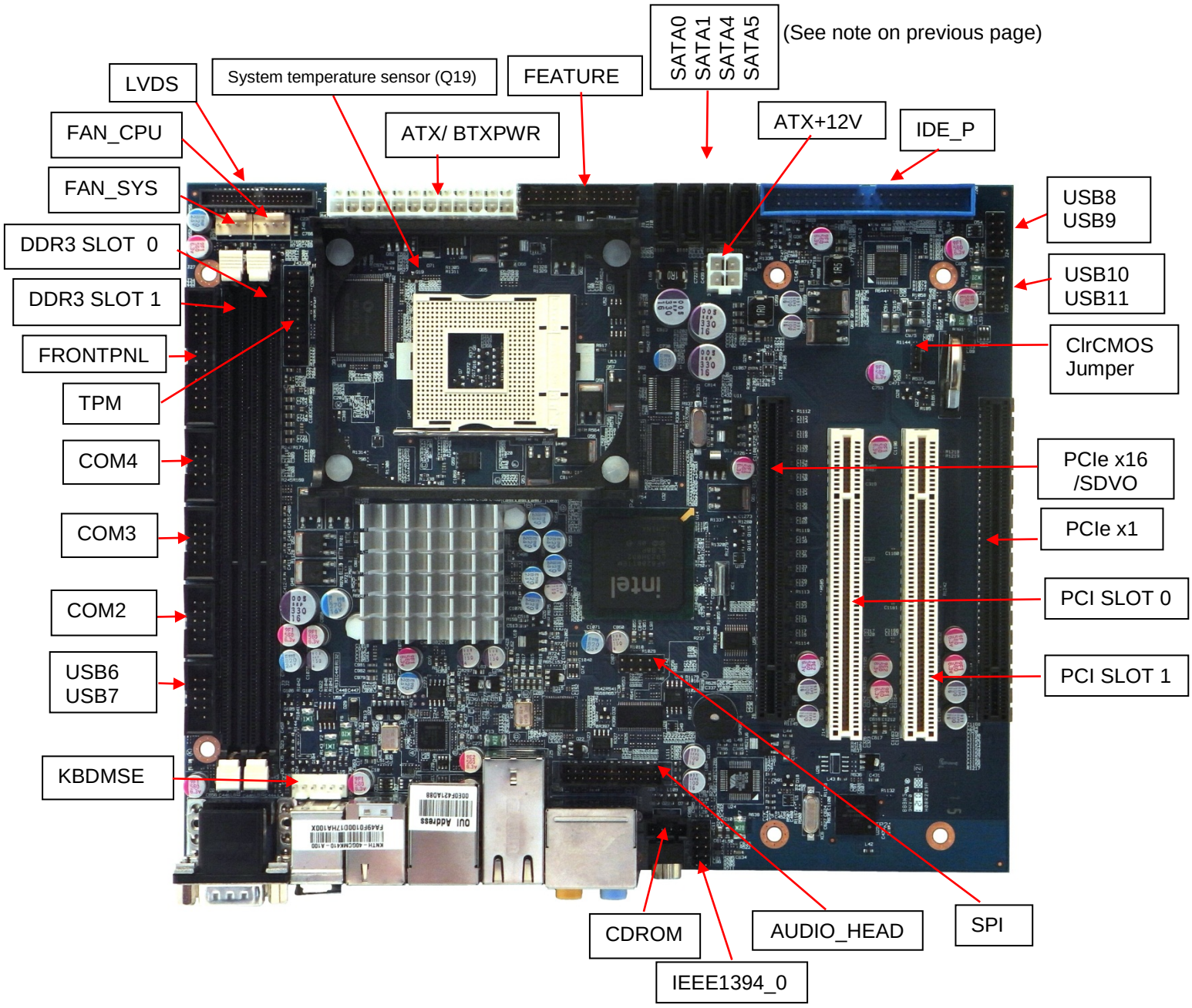
3.1.1 KTGM45/mITX



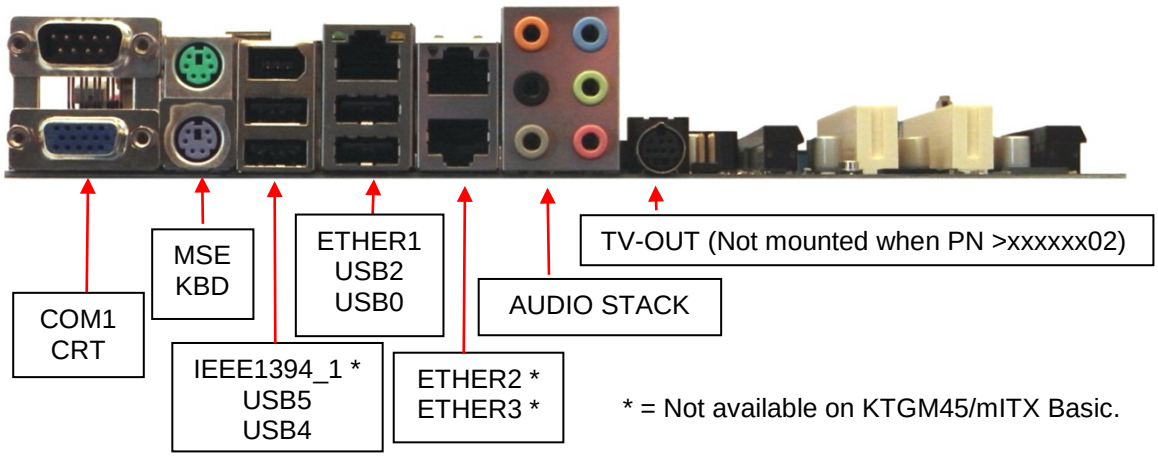
Note: In according to Intel ICH9ME chipset specification the SATA ports 2 and 3 are not functional.

Connectors in IO Bracket area see next page.

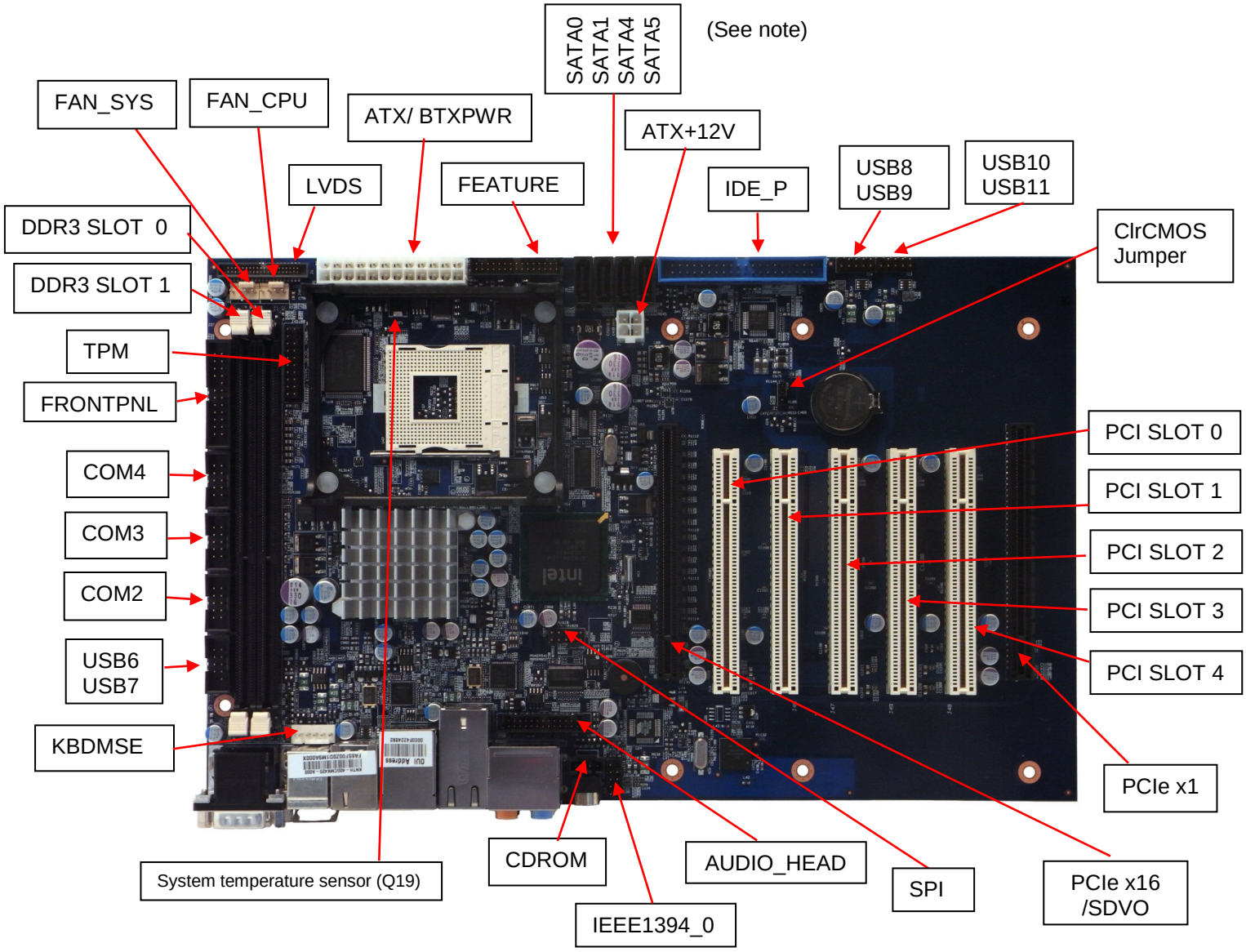
3.1.2 KTGM45/Flex



3.1.3 KTGM45 - IO Bracket area



3.1.4 KTGM45/ATXE



Note: In according to Intel ICH9ME chipset specification the SATA ports 2 and 3 are not functional.

3.2 Power Connector (ATX/BTXPWR)

The KTGM45 boards are designed to be supplied from a standard ATX (or BTX) power supply or by single +12V. Use of BTX supply is not required for operation, but may be required to drive high-power PCIe cards. In case of the KTGM45/mITX or in case of other versions of KTGM45 where the total power load from PCI and PCIe slots are limited to one full load for each type of connector, then the ATX/BTXPWR connector can be unconnected, so that the ATX+12V is the only voltage (12V +/-5%) supplied.

ATX/ BTX Power Connector:

Note	Type	Signal	PIN		Signal	Type	Note
	PWR	3V3	12	24	GND	PWR	
	PWR	+12V	11	23	5V	PWR	
	PWR	+12V	10	22	5V	PWR	
	PWR	SB5V	9	21	5V	PWR	
	I	P_OK	8	20	-5V	PWR	1
	PWR	GND	7	19	GND	PWR	
	PWR	5V	6	18	GND	PWR	
	PWR	GND	5	17	GND	PWR	
	PWR	5V	4	16	PSON#	OC	
	PWR	GND	3	15	GND	PWR	
	PWR	3V3	2	14	-12V	PWR	
	PWR	3V3	1	13	3V3	PWR	

Note 1: -5V supply is not used on-board.

See chapter “Power Consumption” regarding input tolerances on 3.3V, 5V, SB5V, +12 and -12V (also refer to ATX specification version 2.2).

ATX+12V-4pin Power Connector:

Note	Type	Signal	PIN		Signal	Type	Note
	PWR	GND	2	4	+12V	PWR	1
	PWR	GND	1	3	+12V	PWR	1

Note 1: Use of the 4-pin ATX+12V Power Connector is required for operation of the KTGM45 boards.

Signal	Description
P_OK	P_OK is a power good signal and should be asserted high by the power supply to indicate that the +5VDC and +3.3VDC outputs are above the undervoltage thresholds of the power supply. When this signal is asserted high, there should be sufficient energy stored by the converter to guarantee continuous power operation within specification. Conversely, when the output voltages fall below the undervoltage threshold, or when mains power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, P_OK should be de-asserted to a low state. The recommended electrical and timing characteristics of the P_OK (PWR_OK) signal are provided in the *ATX12V Power SupplyDesign Guide*. It is strongly recommended to use an ATX or BTX supply with the KTGM45 boards, in order to implement the supervision of the 5V and 3V3 supplies. These supplies are not supervised on-board the KTGM45 boards.
PS_ON#	Active low open drain signal from the board to the power supply to turn on the power supply outputs. Signal must be pulled high by the power supply.

3.3 Keyboard and Mouse connectors

Attachment of a keyboard or PS/2 mouse adapter can be done through the stacked PS/2 mouse and keyboard connector (MSE & KBD).

Both interfaces utilize open-drain signalling with on-board pull-up.

The PS/2 mouse and keyboard is supplied from SB5V when in standby mode in order to enable keyboard or mouse activity to bring the system out from power saving states. The supply is provided through a 1.1A resettable fuse.

3.3.1 MINI-DIN Keyboard and Mouse Connector (KBD)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	-	NC	6 5	MSCLK	IOD	/14mA	2K7	
	-	-	PWR	5V/SB5V	4 3	GND	PWR	-	-	
	-	-	-	NC	2 1	MSDAT	IOD	/14mA	2K7	
	-	-	-	NC	6 5	KBDCLK	IOD	/14mA	2K7	
	-	-	PWR	5V/SB5V	4 3	GND	PWR	-	-	
	-	-	-	NC	2 1	KBDDAT	IOD	/14mA	2K7	

Signal Description – Keyboard & and mouse Connector (MSE & KBD), see below.

3.3.2 Keyboard and Mouse pinrow Connector (KBDMSE)

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	KBDCLK	IOD	/14mA	2K7	
2	KBDDAT	IOD	/14mA	2K7	
3	MSCLK	IOD	/14mA	2K7	
4	MSDAT	IOD	/14mA	2K7	
5	5V/SB5V	PWR	-	-	
6	GND	PWR	-	-	

Signal Description – Keyboard & and mouse Connector (KBDMSE).

Signal	Description
MSCLK	Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse.
MSDAT	Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse.
KDBCLK	Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard.
KBDDAT	Bi-directional serial data line used to transfer data from or commands to the PC-AT keyboard.

3.4 Display connector

The KTGM45 family provides on-board Analogue CRT interface, on-board LVDS panel interface and on-board TV-Out, however the TV-out connector is not mounted. Additionally there is support for ADD2 card (or similar) through the on-board PCI Express x16 connector, with extension capability for support of dual DVI, dual LVDS, VGA and HDMI + DVI.

If a PCI Express x16 Graphics add-in card is used, the on-board Graphics controller (GMA 4500) is disabled.

3.4.1 CRT Connector (CRT)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
						6	GND	PWR	-	-	
	/75R	-	A0	RED	1	11	NC	-	-	-	
						7	GND	PWR	-	-	
	/75R	-	A0	GREEN	2	12	DDCDAT	IO	TBD	2K2	
						8	GND	PWR	-	-	
	/75R	-	A0	BLUE	3	13	HSYNC	O	TBD		
						9	5V	PWR	-	-	1
	-	-	-	NC	4	14	VSYNC	O	TBD		
						10	GND	PWR	-	-	
	-	-	PWR	GND	5	15	DDCCLK	IO	TBD	2K2	

Signal Description - CRT Connector:

Pin	Signal	Description
1	RED	Analogue output carrying the red colour signal to the CRT. For 75 Ohm cable impedance.
2	GREEN	Analogue output carrying the green colour signal to the CRT. For 75 Ohm cable impedance.
3	BLUE	Analogue output carrying the blue colour signal to the CRT. For 75 Ohm cable impedance.
4	NC	No Connection
5-8	GND	
9	5V	This 5V supply is fused by a 1.1A resettable fuse.
10	GND	
11	NC	No Connection
12	DDCDAT	Display Data Channel Data. Used as data signal to/from monitors with DDC interface.
13	HSYNC	CRT horizontal synchronization output.
14	VSYNC	CRT vertical synchronization output.
15	DDCCLK	Display Data Channel Clock. Used as clock signal to/from monitors with DDC interface.

3.4.2 LVDS Flat Panel Connector (LVDS)

Note	Type	Signal	PIN		Signal	Type	Note
Max. 0.5A	PWR	+12V	1	2	+12V	PWR	Max. 0.5A
Max. 0.5A	PWR	+12V	3	4	+12V	PWR	Max. 0.5A
Max. 0.5A	PWR	+12V	5	6	GND	PWR	Max. 0.5A
Max. 0.5A	PWR	+5V	7	8	GND	PWR	Max. 0.5A
Max. 0.5A	PWR	LCDVCC	9	10	LCDVCC	PWR	Max. 0.5A
2K2Ω, 3.3V	OT	DDC CLK	11	12	DDC DATA	OT	2K2Ω, 3.3V
3.3V level	OT	BKLTCTL	13	14	VDD ENABLE	OT	3.3V level
3.3V level	OT	BKLTEN#	15	16	GND	PWR	Max. 0.5A
	LVDS	LVDS A0-	17	18	LVDS A0+	LVDS	
	LVDS	LVDS A1-	19	20	LVDS A1+	LVDS	
	LVDS	LVDS A2-	21	22	LVDS A2+	LVDS	
	LVDS	LVDS ACLK-	23	24	LVDS ACLK+	LVDS	
	LVDS	LVDS A3-	25	26	LVDS A3+	LVDS	
Max. 0.5A	PWR	GND	27	28	GND	PWR	Max. 0.5A
	LVDS	LVDS B0-	29	30	LVDS B0+	LVDS	
	LVDS	LVDS B1-	31	32	LVDS B1+	LVDS	
	LVDS	LVDS B2-	33	34	LVDS B2+	LVDS	
	LVDS	LVDS BCLK-	35	36	LVDS BCLK+	LVDS	
	LVDS	LVDS B3-	37	38	LVDS B3+	LVDS	
Max. 0.5A	PWR	GND	39	40	GND	PWR	Max. 0.5A

Note 1: The KTGM45 on-board LVDS connector supports single and dual channel, 18/24bit SPWG panels up to the resolution 1600x1200 or 1920x1080 and with limited frame rate some 1920x1200.

Signal Description – LVDS Flat Panel Connector:

Signal	Description
LVDS A0..A3	LVDS A Channel data
LVDS ACLK	LVDS A Channel clock
LVDS B0..B3	LVDS B Channel data
LVDS BCLK	LVDS B Channel clock
BKLTCTL	Backlight control (1), PWM signal to implement voltage in the range 0-3.3V
BKLTEN#	Backlight Enable signal (active low) (2)
VDD ENABLE	Output Display Enable.
LCDVCC	VCC supply to the flat panel. This supply includes power-on/off sequencing. The flat panel supply may be either 5V DC or 3.3V DC depending on the CMOS configuration. Maximum load is 1A at both voltages.
DDC CLK	DDC Channel Clock

Note 1: Windows API will be available to operate the BKLTCTL signal. Some Inverters have a limited voltage range 0- 2.5V for this signal: If voltage is > 2.5V the Inverter might latch up. Some Inverters generates noise on the BKLTCTL signal, resulting in making the LVDS transmission failing (corrupted picture on the display). By adding a 1Kohm resistor in series with this signal, mounted in the Inverter end of the cable kit, the noise is limited and the picture is stable.

Note 2: If the Backlight Enable is required to be active high then, check the following BIOS Chipset setting: Backlight Signal Inversion = Enabled.

3.4.3 TV-Out

The KTGM45 boards include layout for TV-Out connector, but TV-out connector is not mounted from the board PN revision xxxxxx03. Anyway the TV-out has support for (Analogue) Component Video (S-Video, YPbPr or RGB) and Composite Video Output (NTSC/ PAL output format).

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
						GND	PWR	-	-	
	/75Ω	-	AO	TVDACC	4 7 3	TVDACB	AO	-	/75Ω	
	-	-	PWR	GND	2 6 5 1	GND	PWR	-	-	
	-	-	-	NC		TVDACA	AO	-	/75Ω	

Pin	Signal	Description
3	TVDACB	TVDAC Channel B output supports: **Component Video - S-Video**: Luminance analogue signal **Component Video - YPbPr**: Luminance (Y) analogue signal **Component Video - RGB**: Green analogue signal (Composite Video: Not used)
4	TVDACC	TVDAC Channel C output supports: **Component Video - S-Video**: Chrominance analogue signal **Component Video - YPbPr**: Chrominance (Pr) analogue signal **Component Video - RGB**: Red analogue signal (Composite Video: Not used)
5	TVDACA	TVDAC Channel A output supports: (Component Video - S-Video: Not used) **Component Video - YPbPr**: Chrominance (Pb) analogue signal **Component Video - RGB**: Blue analogue signal **Composite Video**: CVBS signal

3.5 Firewire/IEEE1394 connectors

The KTGM45 support two IEEE Std 1394a-2000 fully compliant cable ports at 100M bits/s, 200M bits/s and 400M bits/s. (Not available on KTGM45/mITX Basic)

3.5.1 IEEE1394 connector (IEEE1304_1)

The pinout of the connector IEEE1394_1 (stacked together with USB Ports 4 and 5) is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN
				TPA1+	
				TPB1+	
				GND	
					1 3 5 2 4 6
1				+12V	
				TPB1-	
				TPA1-	

Note 1: The 12V supply for the IEEE1394_1 devices is on-board fused with a 1.5A reset-able fuse.

Signal	Description
TPA1+ TPA1–	Differential signal pair A
TPB1+ TPB1–	Differential signal pair B
+12V	+12V supply

3.5.2 IEEE1394 connector (IEEE1304_0)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
		-	-	TPA0+	1 2	TPA0-	-	-		
	-	-	PWR	GND	3 4	GND	PWR	-	-	
	-		-	TPB0+	5 6	TPB0-	-	-		
1	-	-	PWR	+12V	7 8	+12V	PWR	-	-	1
key	-	-	-	-	10	GND	PWR	-	-	

Note 1: The 12V supply for the IEEE1394_0 devices is on-board fused with a 1.5A reset-able fuse.

Signal	Description
TPA0+ TPA0–	Differential signal pair A
TPB0+ TPB0–	Differential signal pair B
+12V	+12V supply

3.6 PCI-Express connectors

The KTGM45/mITX supports one (x16) (16-lane) PCI Express port and one miniPCI Express port. KTGM45/Flex and KTGM45/ATXE supports one PCIe x16 port and one PCIe x1 port (in a x16 connector).

The 16-lane (x16) PCI Express (PCIe 2.0) port can be used for external PCI Express graphics card. It is located nearest the CPU. Maximum theoretical bandwidth using 16 lanes is 16 GB/s.

The PCI Express (x16) interface is multiplexed with the SDVO ports and TMDS ports.

The miniPCIe (PCIe 1.1) (KTGM45/mITX only) is located on the backside of the board.
Supports PCI Express GEN1 frequency of 1.25 GHz (supports 2.5 Gbit/s in each direction, 500 MB/s totally).

The 1-lane (x1) PCI Express (PCIe 1.1) port (KTGM45/Flex and KTGM45/ATXE only) is mechanically a x16 port and electrically a x1 port. It is located farthest away from CPU. Supports PCI Express GEN1 frequency of 1.25 GHz (supports 2.5 Gbit/s in each direction, 500 MB/s totally).

3.6.1 PCI-Express x16/SDVO Connector (PCIe x16/SDVO)

Note	Type	Signal	PIN		Signal	Type	Note
		+12V	B1	A1	NC		
		+12V	B2	A2	+12V		
		+12V	B3	A3	+12V		
		GND	B4	A4	GND		
		SMB_CLK	B5	A5	NC		
		SMB_DATA	B6	A6	NC		
		GND	B7	A7	NC		
		+3V3	B8	A8	NC		
		NC	B9	A9	+3V3		
		SB3V3	B10	A10	+3V3		
		WAKE#	B11	A11	RST#		
		NC	B12	A12	GND		
		GND	B13	A13	PCIE_x16 CLK		
		PEG_TXP[15]/SDVOB_RED	B14	A14	PCIE_x16 CLK#		
		PEG_TXN[15]/SDVOB_RED#	B15	A15	GND		
		GND	B16	A16	PEG_RXP[15]/SDVO_TVCLKIN		
		SDVO_CTRLCLK	B17	A17	PEG_RXN[15] / SDVO_TVCLKIN#		
		GND	B18	A18	GND		
		PEG_TXP[14]/SDVOB_GREEN	B19	A19	NC		
		PEG_TXN[14]/SDVOB_GREEN#	B20	A20	GND		
		GND	B21	A21	PEG_RXP[14]/SDVOB_INT		
		GND	B22	A22	PEG_RXN[14]/SDVOB_INT#		
		PEG_TXP[13]/SDVOB_BLUE	B23	A23	GND		
		PEG_TXN[13]/SDVOB_BLUE#	B24	A24	GND		
		GND	B25	A25	PEG_RXP[13]/SDVO_FLDSTALL		
		GND	B26	A26	PEG_RXN[13]/SDVO_FLDSTALL#		
		PEG_TXP[12]/SDVOB_CLKP	B27	A27	GND		
		PEG_TXN[12]/SDVOB_CLKN	B28	A28	GND		
		GND	B29	A29	PEG_RXP[12]		
		NC	B30	A30	PEG_RXN[12]		
		SDVO_CTRLDATA	B31	A31	GND		
		GND	B32	A32	NC		
		PEG_TXP[11]/SDVOC_RED	B33	A33	NC		
		PEG_TXN[11]/SDVOC_RED#	B34	A34	GND		
		GND	B35	A35	PEG_RXP[11]		

		GND	B36	A36	PEG_RXN[11]		
		PEG_TXP[10]/SDVOC_GREEN	B37	A37	GND		
		PEG_TXN[10]/SDVOC_GREEN#	B38	A38	GND		
		GND	B39	A39	PEG_RXP[10]/SDVOC_INT		
		GND	B40	A40	PEG_RXN[10]/SDVOC_INT#		
		PEG_TXP[9]/SDVOC_BLUE	B41	A41	GND		
		PEG_TXN[9]/SDVOC_BLUE#	B42	A42	GND		
		GND	B43	A43	PEG_RXP[9]		
		GND	B44	A44	PEG_RXN[9]		
		PEG_TXP[8]/SDVOC_CLKN	B45	A45	GND		
		PEG_TXN[8]/SDVOC_CLKP	B46	A46	GND		
		GND	B47	A47	PEG_RXP[8]		
		PRSNT#2	B48	A48	PEG_RXN[8]		
		GND	B49	A49	GND		
		PEG_TXP[7]	B50	A50	NC		
		PEG_TXN[7]	B51	A51	GND		
		GND	B52	A52	PEG_RXP[7]		
		GND	B53	A53	PEG_RXN[7]		
		PEG_TXP[6]	B54	A54	GND		
		PEG_TXN[6]	B55	A55	GND		
		GND	B56	A56	PEG_RXP[6]		
		GND	B57	A57	PEG_RXN[6]		
		PEG_TXP[5]	B58	A58	GND		
		PEG_TXN[5]	B59	A59	GND		
		GND	B60	A60	PEG_RXP[5]		
		GND	B61	A61	PEG_RXN[5]		
		PEG_TXP[4]	B62	A62	GND		
		PEG_TXN[4]	B63	A63	GND		
		GND	B64	A64	PEG_RXP[4]		
		GND	B65	A65	PEG_RXN[4]		
		PEG_TXP[3]	B66	A66	GND		
		PEG_TXN[3]	B67	A67	GND		
		GND	B68	A68	PEG_RXP[3]		
		GND	B69	A69	PEG_RXN[3]		
		PEG_TXP[2]	B70	A70	GND		
		PEG_TXN[2]	B71	A71	GND		
		GND	B72	A72	PEG_RXP[2]		
		GND	B73	A73	PEG_RXN[2]		
		PEG_TXP[1]	B74	A74	GND		
		PEG_TXN[1]	B75	A75	GND		
		GND	B76	A76	PEG_RXP[1]		
		GND	B77	A77	PEG_RXN[1]		
		PEG_TXP[0]	B78	A78	GND		
		PEG_TXN[0]	B79	A79	GND		
		GND	B80	A80	PEG_RXP[0]		
		NC	B81	A81	PEG_RXN[0]		
		NC	B82	A82	GND		

3.6.2 miniPCI-Express

The KTGM45/mITX supports one miniPCI Express port.

Note	Type	Signal	PIN		Signal	Type	Note
		WAKE#	1	2	+3V3		
		NC	3	4	GND		
		NC	5	6	+1.5V		
1		CLKREQ#	7	8	NC		
		GND	9	10	NC		
		PCIE_mini CLK#	11	12	NC		
		PCIE_mini CLK	13	14	NC		
		GND	15	16	NC		
		NC	17	18	GND		
		NC	19	20	W_Disable#		2
		GND	21	22	RST#		
		PCIE_RXN	23	24	+3V3 Dual		
		PCIE_RXP	25	26	GND		
		GND	27	28	+1.5V		
		GND	29	30	SMB_CLK		
		PCIE_TXN	31	32	SMB_DATA		
		PCIE_TXP	33	34	GND		
		GND	35	36	NC		
		NC	37	38	NC		
		NC	39	40	GND		
		NC	41	42	NC		
		NC	43	44	NC		
		NC	45	46	NC		
		NC	47	48	+1.5V		
		NC	49	50	GND		
		NC	51	52	+3V3		

Note 1: 4K7 ohm pull-up to 3V3.

Note 2: 2K2 ohm pull-up to 3V3 Dual.

3.6.3 PCI-Express x1 Connector (PCIe x16)

The KTGM45/Flex and KTGM45/ATXE supports one PCIe x1 in a x16 socket.

Note	Type	Signal	PIN		Signal	Type	Note
		+12V	B1	A1	NC		
		+12V	B2	A2	+12V		
		+12V	B3	A3	+12V		
		GND	B4	A4	GND		
		SMB_CLK	B5	A5	NC		
		SMB_DATA	B6	A6	NC		
		GND	B7	A7	NC		
		+3V3	B8	A8	NC		
		NC	B9	A9	+3V3		
		SB3V3	B10	A10	+3V3		
		WAKE#	B11	A11	RST#		
		NC	B12	A12	GND		
		GND	B13	A13	PCIE_x4 CLK		
		PCIE_TXP4	B14	A14	PCIE_x4 CLK#		
		PCIE_TXN4	B15	A15	GND		
		GND	B16	A16	PCIE_RXP4		
		NC	B17	A17	PCIE_RXN4		
		GND	B18	A18	GND		
		NC	B19	A19	NC		
		NC	B20	A20	GND		
		GND	B21	A21	NC		
		GND	B22	A22	NC		
		NC	B23	A23	GND		
		NC	B24	A24	GND		
		GND	B25	A25	NC		
		GND	B26	A26	NC		
		NC	B27	A27	GND		
		NC	B28	A28	GND		
		GND	B29	A29	NC		
		NC	B30	A30	NC		
		NC	B31	A31	GND		
		GND	B32	A32	NC		
		NC	B33	A33	NC		
		NC	B34	A34	GND		
		GND	B35	A35	NC		
		GND	B36	A36	NC		
		NC	B37	A37	GND		
		NC	B38	A38	GND		
		GND	B39	A39	NC		
		GND	B40	A40	NC		
		NC	B41	A41	GND		
		NC	B42	A42	GND		
		GND	B43	A43	NC		
		GND	B44	A44	NC		
		NC	B45	A45	GND		
		NC	B46	A46	GND		
		GND	B47	A47	NC		
		NC	B48	A48	NC		
		GND	B49	A49	GND		
		NC	B50	A50	NC		
		NC	B51	A51	GND		
		GND	B52	A52	NC		
		GND	B53	A53	NC		
		NC	B54	A54	GND		
		NC	B55	A55	GND		
		GND	B56	A56	NC		
		GND	B57	A57	NC		
		NC	B58	A58	GND		
		NC	B59	A59	GND		

		GND	B60	A60	NC		
		GND	B61	A61	NC		
		NC	B62	A62	GND		
		NC	B63	A63	GND		
		GND	B64	A64	NC		
		GND	B65	A65	NC		
		NC	B66	A66	GND		
		NC	B67	A67	GND		
		GND	B68	A68	NC		
		GND	B69	A69	NC		
		NC	B70	A70	GND		
		NC	B71	A71	GND		
		GND	B72	A72	NC		
		GND	B73	A73	NC		
		NC	B74	A74	GND		
		NC	B75	A75	GND		
		GND	B76	A76	NC		
		GND	B77	A77	NC		
		NC	B78	A78	GND		
		NC	B79	A79	GND		
		GND	B80	A80	NC		
		NC	B81	A81	NC		
		NC	B82	A82	GND		

3.7 Parallel ATA Hard Disk interface

The PATA Host Controller supports three types of data transfers:

- Programmed I/O (PIO): Processor is in control of the data transfer.
- Multi-word DMA (ATA-5): DMA protocol that resembles the DMA on the ISA bus. Allows transfer rates of up to 66MB/s.
- Ultra DMA: Synchronous DMA protocol that redefines signals on the PATA cable to allow both host and target throttling of data and transfer rates up to 100MB/s. Ultra DMA 100/66/33 are supported, a 80-wire cable is required.

One parallel ATA hard disk controller is available on the board – a primary controller. Standard 3½" hard disks or CD-ROM drives may be attached to the primary controller by means of the 40 pin IDC connector, PATA.

On the KTGM45/mITX Plus the parallel ATA hard disk controller is shared between the PATA connector and the CF connector.

If the CF connector is not used then two devices (a primary and a secondary device) are supported on the PATA interface. Otherwise if the CF connector is used then only one PATA device is supported and only by use of 40-wire cable (not 80-wire cable). Optionally use SATA HDD device(s).

In case CF card shall be used as hot plug device then it is recommended to use USB to CF adapter. (SATA to CF adapter doesn't support hot plug).

The signals used for the hard disk interface are the following:

Signal	Description
DAA2..0	Address lines, used to address the I/O registers in the IDE hard disk.
HDCSA1..0#	Hard Disk Chip-Select. HDCS0# selects the primary hard disk.
DA15..8	High part of data bus.
DA7..0	Low part of data bus.
IORA#	I/O Read.
IOWA#	I/O Write.
IORDYA#	This signal may be driven by the hard disk to extend the current I/O cycle.
RESETA#	Reset signal to the hard disk.
HDIRQA	Interrupt line from hard disk.
CBLIDA	This input signal (CaBLe ID) is used to detect the type of attached cable: 80-wire cable when low input, and 40-wire cable when 5V via 10Kohm (pull-up resistor).
DDREQA	Disk DMA Request might be driven by the IDE hard disk to request bus master access to the PCI bus. The signal is used in conjunction with the PCI bus master IDE function and is not associated with any PC-AT bus compatible DMA channel.
DDACKA#	Disk DMA Acknowledge. Active low signal grants IDE bus master access to the PCI bus.
HDACTA#	Signal from hard disk indicating hard disk activity. The signal level depends on the hard disk type, normally active low. The signals from primary and secondary controller are routed together through diodes and passed to the connector FEATURE.

The pinout of the connectors is defined in the following sections.

3.7.1 IDE Hard Disk Connector (PATA)

This connector can be used for connection of two primary IDE drives.

Note	Pull U/D	Ioh/ Iol	Type	Signal	PIN#		Signal	Type	Ioh/ Iol	Pull U/D	Note
	-	TBD	O	RESET_P#	1	2	GND	PWR	-	-	
	-	TBD	IO	DA7	3	4	DA8	IO	TBD	-	
	-	TBD	IO	DA6	5	6	DA9	IO	TBD	-	
	-	TBD	IO	DA5	7	8	DA10	IO	TBD	-	
	-	TBD	IO	DA4	9	10	DA11	IO	TBD	-	
	-	TBD	IO	DA3	11	12	DA12	IO	TBD	-	
	-	TBD	IO	DA2	13	14	DA13	IO	TBD	-	
	-	TBD	IO	DA1	15	16	DA14	IO	TBD	-	
	-	TBD	IO	DA0	17	18	DA15	IO	TBD	-	
	-	-	PWR	GND	19	20	KEY	-	-	-	
	-	-	I	DDRQA	21	22	GND	PWR	-	-	
	-	TBD	O	IOWA#	23	24	GND	PWR	-	-	
	-	TBD	O	IORA#	25	26	GND	PWR	-	-	
	4K7	-	I	IORDYA	27	28	GND	PWR	-	-	
	-	-	O	DDACKA#	29	30	GND	PWR	-	-	
	10K	-	I	HDIRQA	31	32	NC	-	-	-	
	-	TBD	O	DAA1	33	34	CBLIDA#	I	-		
	-	TBD	O	DAA0	35	36	DAA2	O	TBD	-	
	-	TBD	O	HDCSA0#	37	38	HDCSA1#	O	TBD	-	
	-	-	I	HDACTA#	39	40	GND	PWR	-	-	

3.7.2 Compact Flash Connector (CF)

This connector is mounted on the backside of the KTGM45/mITX Plus.

The CF socket support DMA/UDMA modules up to UDMA2.

Note: If the CF connector is used then only one PATA device is supported and only by use of 40-wire cable (not 80-wire cable). Optionally use SATA device(s). Normally CF is Master and then possible PATA device must be Slave.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
2	-	-	-	NC	26	1	GND	PWR	-	-	1
	-	TBD	IO	DA11	27	2	DB3	IO	TBD	-	
	-	TBD	IO	DA12	28	3	DB4	IO	TBD	-	
	-	TBD	IO	DA13	29	4	DB5	IO	TBD	-	
	-	TBD	IO	DA14	30	5	DB6	IO	TBD	-	
	-	TBD	IO	DA15	31	6	DB7	IO	TBD	-	
	-	TBD	O	HDCSA1#	32	7	HDCSA0#	O	TBD	-	
	-	-	-	NC	33	8	GND	PWR	-	-	
	-	TBD	O	IORA#	34	9	GND	PWR	-	-	
	-	TBD	O	IOWA#	35	10	GND	PWR	-	-	
	-	-	PWR	5V	36	11	GND	PWR	-	-	
	8K2	-	I	HDIRQA	37	12	GND	PWR	-	-	
	-	-	PWR	5V	38	13	5V	PWR	-	-	
	-	-	PWR	GND	39	14	GND	PWR	-	-	
	-	-	-	NC	40	15	GND	PWR	-	-	
	-	TBD	O	RESET_C#	41	16	GND	PWR	-	-	
	4K7	-	I	IORDYA	42	17	GND	PWR	-	-	
	-	-	I	DDRQA	43	18	DAA2	O	-	-	
	-	-	O	DDACKA#	44	19	DAA1	O	-	-	
	-	-	I	HDACTA#	45	20	DAA0	O	-	-	
	-	-	I	CBLIDA#	46	21	DB0	IO	TBD	-	
	-	TBD	IO	DB8	47	22	DB1	IO	TBD	-	
	-	TBD	IO	DB9	48	23	DB2	IO	TBD	-	
	-	TBD	IO	DB10	49	24	NC				
1	-	-	PWR	GND	50	25	NC	-	-	-	2

Note 1: Pin is longer than the average length of the other pins.
Note 2: Pin is shorter than the average length of the other pins.

3.8 Serial ATA Hard Disk interface

The KTGM45 boards have an integrated SATA Host controller that supports independent DMA operation on four ports and data transfer rates of up to 3.0Gb/s (300MB/s). The SATA controller supports AHCI mode and has integrated RAID functionality with support for RAID modes 0 and 1.

The board provides four Serial ATA (SATA) connectors which support one device per connector. The ICH9ME Serial ATA controller offers four independent Serial ATA ports with a theoretical maximum transfer rate of 3 Gbits/sec per port. One device can be installed on each port for a maximum of four Serial ATA devices. A point-to-point interface is used for host to device connections, unlike Parallel ATA IDE which supports a master/slave configuration and two devices per channel.

For compatibility, the underlying Serial ATA functionality is transparent to the operating system. The Serial ATA controller can operate in both legacy and native modes. In legacy mode, standard IDE I/O and IRQ resources are assigned (IRQ 14 and 15). In Native mode, standard PCI Conventional bus resource steering is used. Native mode is the preferred mode for configurations using the Windows XP and Windows Vista operating systems.

The KTGM45 supports the following RAID (Redundant Array of Independent Drives) levels:

- RAID 0 - data striping
- RAID 1 - data mirroring

3.8.1 SATA Hard Disk Connector (SATA0, SATA1, SATA4, SATA5)

Note: In according to Intel ICH9ME chipset specification the SATA ports 2 and 3 are not functional. Drivers, BIOS and this Users Guide do not refer to SATA port 2 and 3, but only SATA ports 1, 2, 4 and 5.

SATA:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	GND	PWR	-	-	
2	SATA* TX+				
3	SATA* TX-				
4	GND	PWR	-	-	
5	SATA* RX-				
6	SATA* RX+				
7	GND	PWR	-	-	

The signals used for the primary Serial ATA hard disk interface are the following:

Signal	Description
SATA* RX+ SATA* RX-	Host transmitter differential signal pair
SATA* TX+ SATA* TX-	Host receiver differential signal pair

“*” specifies 0, 1, 4, 5 depending on SATA port.

3.9 Serial Ports

Four RS232 serial ports are available on the KTGM45.

The typical definition of the signals in the COM ports is as follows:

Signal	Description
TxD	Transmitted Data, sends data to the communications link. The signal is set to the marking state (-12V) on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Received Data, receives data from the communications link.
DTR	Data Terminal Ready, indicates to the modem etc. that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready, indicates that the modem etc. is ready to establish a communications link.
RTS	Request To Send, indicates to the modem etc. that the on-board UART is ready to exchange data.
CTS	Clear To Send, indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect, indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator, indicates that the modem has received a ringing signal from the telephone line.

The connector pinout for each operation mode is defined in the following sections.

3.9.1 COM1 Connector

COM1 is RS232 port available in the IO Bracket area. The pinout of Serial ports Com1 is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	5						
						9	RI	I	-	/5K	
	-		O	DTR	4						
						8	CTS	I	-	/5K	
	-		O	TxD	3						
						7	RTS	O		-	
	/5K	-	I	RxD	2						
						6	DSR	I	-	/5K	
	/5K	-	I	DCD	1						

3.9.2 COM2 COM3 and COM4 Header Connectors

The pinout of Serial ports COM2, COM3 and COM4 is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
		-	I	DCD	1	2	DSR	I	-		
		-	I	RxD	3	4	RTS	O		-	
	-		O	TxD	5	6	CTS	I	-		
	-		O	DTR	7	8	RI	I	-		
	-	-	PWR	GND	9	10	5V	PWR	-	-	1

Note 1: The COM2, COM3 and COM4 5V supply is fused with individual 1.1A resettable fuses.

A DB9 adapter (ribbon cable) is available for connecting the COM ports to I/O front panel.

3.10 Ethernet Connectors

The KTGM45 boards supports three channels of 10/100/1000Mb Ethernet, one (ETHER1) is based on Intel® Boazman-LM WG82567LM Gigabit PHY with AMT 4.0 support and the two other controllers (ETHER2 & ETHER3) are based on Intel® Hartwell 82574L PCI Express controller. (ETHER2/ETHER3 are not available on KTGM45/mITX Basic).

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100MB and Category 5E, 6 or 6E with 1Gb LAN networks.

The signals for the Ethernet ports are as follows:

Signal	Description
MDI[0]+ / MDI[0]-	In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDI[1]+ / MDI[1]-	In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDI[2]+ / MDI[2]-	In MDI mode, this is the third pair in 1000Base-T, i.e. the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
MDI[3]+ / MDI[3]-	In MDI mode, this is the fourth pair in 1000Base-T, i.e. the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair.

Note: MDI = Media Dependent Interface.

3.10.1 Ethernet Connectors 1, 2 and 3 (ETHER1, ETHER2 and ETHER3)

Ethernet connector 1 is mounted together with USB Ports 0 and 2.
Ethernet connector 2 is mounted together with and above Ethernet connector 3.

The pinout of the RJ45 connectors is as follows:

Signal	PIN	Type	Ioh/Iol	Note
MDI0+				
MDI0-				
MDI1+				
MDI2+				
MDI2-				
MDI1-				
MDI3+				
MDI3-				
	8 7 6 5 4 3 2 1			

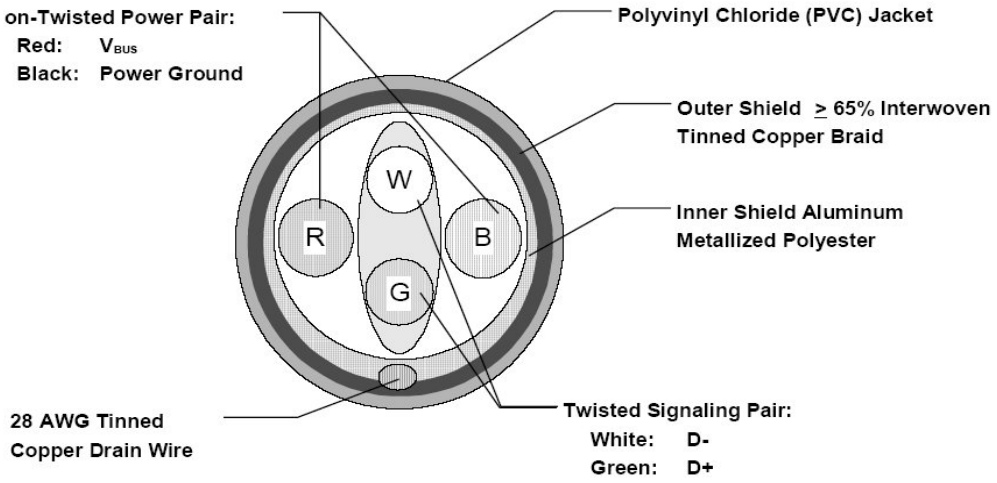
3.11 USB Connectors (USB)

The KTGM45 board contains two Enhanced Host Controller Interface (EHCI) host controllers that support USB 2.0 allowing data transfers up to 480Mb/s. The KTGM45 boards also contains Six Universal Host Controller Interface (UHCI Revision 1.1) controllers that support USB full-speed and low-speed signalling.
The KTGM45 board supports a total of twelve USB 2.0 ports. All twelve ports are high-speed, full-speed, and low-speed capable and USB Legacy mode is supported.

Over-current detection on all twelve USB ports is supported.

USB Port 0 and 2 are supplied on the combined ETHER1, USB0, and USB2 connector.
USB Ports 1 and 3 are supplied on the internal FRONTPNL connector; please refer to the FRONTPNL connector section for the pin-out.
USB Port 4 and 5 are supplied on the combined IEEE1394_1, USB4, and USB5 connector.
USB Port 6 and 7 are supplied on the USB6/7 internal pinrow connector.
USB Port 8 and 9 are supplied on the USB8/9 internal pinrow connector.
USB Port 10 and 11 are supplied on the USB10/11 internal pinrow connector.

Note: It is required to use only HiSpeed USB cable, specified in USB2.0 standard:



3.11.1 USB Connector 0/2 (USB0/2)

USB Ports 0 and 2 are mounted together with ETHER1 Ethernet port.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	-	-	PWR	5V/SB5V	1 2 3 4	GND	PWR	-	-	
	/15K	0.25/2	IO	USB2-		USB2+	IO	0.25/2	/15K	
1	-	-	PWR	5V/SB5V	1 2 3 4	GND	PWR	-	-	
	/15K	0.25/2	IO	USB0-		USB0+	IO	0.25/2	/15K	

Note 1: In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB0+ USB0- USB2+ USB2-	Differential pair works as Data/Address/Command Bus.
5V/SB5V	5V supply for external devices. SB5V is supplied during powerdown to allow wakeup on USB device activity. Protected by resettable 1.1A fuse covering both USB ports.

3.11.2 USB Connector 1/3 (USB1/3)

See Frontpanel Connector (FRONTPNL) description.

3.11.3 USB Connector 4/5 (USB4/5)

USB Ports 4 and 5 are mounted together with IEEE1394_1 port.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	-	-	PWR	5V/SB5V	1 2 3 4	GND	PWR	-	-	
	/15K	0.25/2	IO	USB5-		USB5+	IO	0.25/2	/15K	
1	-	-	PWR	5V/SB5V	1 2 3 4	GND	PWR	-	-	
	/15K	0.25/2	IO	USB4-		USB4+	IO	0.25/2	/15K	

Note 1: In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB4+ USB4- USB5+ USB5-	Differential pair works as Data/Address/Command Bus.
5V/SB5V	5V supply for external devices. SB5V is supplied during powerdown to allow wakeup on USB device activity. Protected by resettable 1.1A fuse covering both USB ports.

3.11.4 USB Connector 6/7 (USB6/7)

USB Ports 6 and 7 are available on the internal USB6/7 pinrow connector.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1		-	PWR	5V/SB5V	1 2	5V/SB5V	PWR	-		1
		-	IO	USB6-	3 4	USB7-	IO		-	
	-		IO	USB6+	5 6	USB7+	IO	-		
	-		PWR	GND	7 8	GND	PWR	-		
	-	-		KEY	9 10	NC		-	-	

Note 1: In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB6+ USB6- USB7+ USB7-	Differential pair works as Data/Address/Command Bus.
5V/SB5V	5V supply for external devices. SB5V is supplied during powerdown to allow wakeup on USB device activity. Protected by resettable 1.1A fuse covering both USB ports.

3.11.5 USB Connector 8/9 (USB8/9)

USB Ports 8 and 9 are supplied on the internal USB8/9 pinrow connector.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
1		-	PWR	5V/SB5V	1	2	5V/SB5V	PWR	-		1
		-	IO	USB8-	3	4	USB9-	IO		-	
	-		IO	USB8+	5	6	USB9+	IO	-		
	-		PWR	GND	7	8	GND	PWR	-		
	-	-		KEY	9	10	NC		-	-	

Note 1: In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB8+ USB8- USB9+ USB9-	Differential pair works as Data/Address/Command Bus.
5V/SB5V	5V supply for external devices. SB5V is supplied during powerdown to allow wakeup on USB device activity. Protected by resettable 1.1A fuse covering both USB ports.

3.11.6 USB Connector 10/11 (USB10/11)

USB Ports 10 and 11 are supplied on the internal USB10/11 pinrow connector.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
1		-	PWR	5V/SB5V	1	2	5V/SB5V	PWR	-		1
		-	IO	USB10-	3	4	USB11-	IO		-	
	-		IO	USB10+	5	6	USB11+	IO	-		
	-		PWR	GND	7	8	GND	PWR	-		
	-	-		KEY	9	10	NC		-	-	

Note 1: In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB10+ USB10- USB11+ USB11-	Differential pair works as Data/Address/Command Bus.
5V/SB5V	5V supply for external devices. SB5V is supplied during powerdown to allow wakeup on USB device activity. Protected by resettable 1.1A fuse covering both USB ports.

3.12 Audio Connectors

The on-board Audio circuit implements 7.1+2 Channel High Definition Audio with UAA (Universal Audio Architecture), featuring five 24-bit stereo DACs and three 20-bit stereo ADCs.

3.12.1 Audio Speakers, Line-In, Line-Out and Microphone

Audio Speakers, Line-in, Line-out and Microphone are available in the stacked audiojack connector. Below is shown audio stack configuration when configured for 8-channel audio.

Note	Type	Signal			Signal	Type	Note
	OA	CEN-OUT	TIP	TIP	LINE1-IN-L	IA	
	OA	LFE-OUT	RING	RING	LINE1-IN-R	IA	
	PWR	GND	SLEEVE	SLEEVE	GND	PWR	
	OA	REAR-OUT-L	TIP	TIP	FRONT-OUT-L	OA	
	OA	REAR-OUT-R	RING	RING	FRONT-OUT-R	OA	
	PWR	GND	SLEEVE	SLEEVE	GND	PWR	
	OA	SIDE-OUT-L	TIP	TIP	MIC1-L	IA	
	OA	SIDE-OUT-R	RING	RING	MIC1-R	IA	
	PWR	GND	SLEEVE	SLEEVE	GND	PWR	

Signal	Description	Note
FRONT-OUT-L	Front Speakers (Speaker Out Left).	
FRONT-OUT-R	Front Speakers (Speaker Out Right).	
REAR-OUT-L	Rear Speakers (Surround Out Left).	
REAR-OUT-R	Rear Speakers (Surround Out Right).	
SIDE-OUT-L	Side speakers (Surround Out Left)	
SIDE-OUT-R	Side speakers (Surround Out Right)	
CEN-OUT	Center Speaker (Center Out channel).	
LFE-OUT	Subwoofer Speaker (Low Freq. Effect Out).	
MIC1	MIC Input 1	
LINE1-IN	Line in 1 signals	

Port	2-channel	4-channel	6-channel	8-channel
Light Blue	Line in	Line in	Line in	Line in
Lime	Line out	Front speaker out	Front speaker out	Front speaker out
Pink	Mic in	Mic in	Mic in	Mic in
Audio header	-	-	-	Side speaker out
Audio header	-	Rear speaker out	Rear speaker out	Rear speaker out
Audio header	-	-	Center/ Subwoofer	Center/ Subwoofer

3.12.2 CDROM Audio Input (CDROM)

CD-ROM audio input may be connected to this connector. It may also be used as a secondary line-in signal.

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	CD_Left	IA	-	-	1
2	CD_GND	IA	-	-	
3	CD_GND	IA	-	-	
4	CD_Right	IA	-	-	1

Note 1: The definition of which pins are use for the Left and Right channels is not a worldwide accepted standard. Some CDROM cable kits expect reverse pin order.

Signal	Description
CD_Left CD_Right	Left and right CD audio input lines or secondary Line-in.
CD_GND	Analogue GND for Left and Right CD. (This analogue GND is **not** shorted to the general digital GND on the board).

3.12.3 Line2 and Mic2

Line2 and Mic2 are accessible via Feature Connector, see Feature connector description.

3.12.4 Audio Header (AUDIO_HEAD)

Note	Pull U/D	Ioh/ Iol	Type	Signal	PIN		Signal	Type	Ioh/ Iol	Pull U/D	Note
				LFE-OUT	1	2	CEN-OUT				
				AAGND	3	4	AAGND				
				FRONT-OUT-L	5	6	FRONT-OUT-R				
				AAGND	7	8	AAGND				
				REAR-OUT-L	9	10	REAR-OUT-R				
				SIDE-OUT-L	11	12	SIDE-OUT-R				
				AAGND	13	14	AAGND				
				MIC1-L	15	16	MIC1-R				
				AAGND	17	18	AAGND				
				LINE1-IN-L	19	20	LINE1-IN-R				
				NC	21	22	AAGND				
	-	-	PWR	GND	23	24	SPDIF-IN				
				SPDIF-OUT	25	26	GND	PWR	-	-	

Signal	Description	Note
FRONT-OUT-L	Front Speakers (Speaker Out Left).	
FRONT-OUT-R	Front Speakers (Speaker Out Right).	
REAR-OUT-L	Rear Speakers (Surround Out Left).	
REAR-OUT-R	Rear Speakers (Surround Out Right).	
SIDE-OUT-L	Side speakers (Surround Out Left)	
SIDE-OUT-R	Side speakers (Surround Out Right)	
CEN-OUT	Center Speaker (Center Out channel).	
LFE-OUT	Subwoofer Speaker (Low Freq. Effect Out).	
NC	No connection	
MIC1	MIC Input 1	
LINE1-IN	Line in 1 signals	
F-SPDIF-IN	S/PDIF Input	
F-SPDIF-OUT	S/PDIF Output	
AAGND	Audio Analogue ground	

3.13 Fan Connector (FAN_CPU)

The **FAN_CPU** is used for the connection of the FAN for the CPU.
The **FAN_SYS** can be used to power, control and monitor a fan for chassis ventilation etc.

The 4pin header is recommended to be used for driving 4-wire type Fan in order to implement FAN speed control. 3-wire Fan is also possible, but no fan speed control is integrated.

4-pin Mode:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	CONTROL	O	-	-	
2	SENSE	I	-	4K7	
3	+12V	PWR	-	-	
4	GND	PWR	-	-	

Signal	Description
CONTROL	PWM signal for FAN speed control
SENSE	Tacho signal from the fan for supervision. The signals shall be generated by an open collector transistor or similar. On-board is a pull-up resistor 4K7 to +12V. The signal has to be pulsed, typically twice per rotation.
12V	+12V supply for fan. A maximum of 2000mA can be supplied from this pin.
GND	Power Supply GND signal

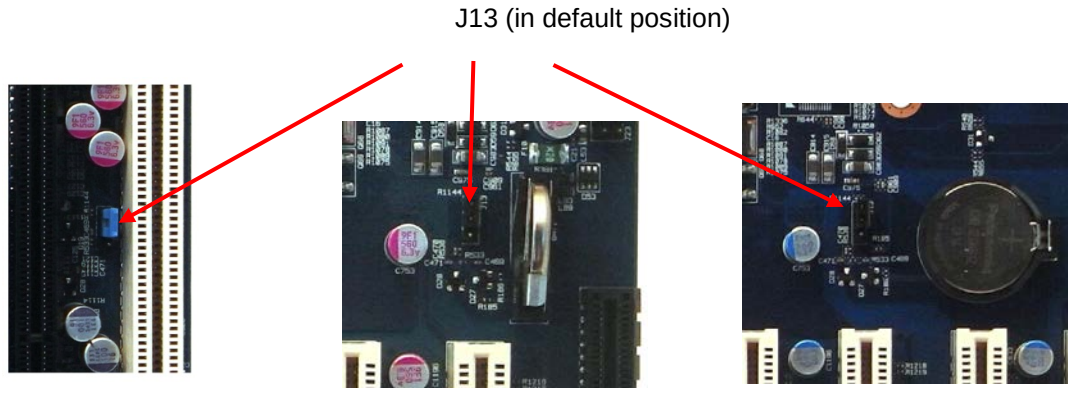
3-pin Mode:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
-					
2	SENSE	I	-	4K7	
3	+12V	PWR	-	-	
4	GND	PWR	-	-	

Signal	Description
SENSE	Tacho signal from the fan for supervision. The signals shall be generated by an open collector transistor or similar. On-board is a pull-up resistor 4K7 to +12V. The signal has to be pulsed, typically twice per rotation.
12V	+12V supply for fan. A maximum of 2000mA can be supplied from this pin.
GND	Power Supply GND signal

3.14 Clear CMOS Jumper (J13)

The Clear-CMOS Jumper (J13) is used to clear the CMOS content.



KTGM45/mITX KTGM45/Flex KTGM45/ATXE

J13		Description
pin1-2	pin2-3	
X	-	Default positions
-	X	Clear CMOS data *
-	-	Secure CMOS function is disabled and Default values are used

WARNING: Don't leave the jumper in this position, otherwise if power is disconnected the battery will fully depleted within a few weeks.

To clear CMOS settings, including Password protection, move the Clear CMOS jumper to pin 2-3 for a few seconds (~10 sec) (works with or without power connected to the system).

3.15 TPM Connector (TPM)

This TPM connector (not available on KTGM45/mITX) is in general unsupported. TPM is already included in the KTGM45 so TPM connector is not needed, however in special projects LPC interface might be of interest and then TMP connector is required.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	LPC CLK	1	2	GND				
	-	-	PWR	LPC FRAME#	3		KEY				
				LPC RST#	5	6	+5V				
				LPC AD3	7	8	LPC AD2				
				+3V3	9	10	LPC AD1				
				LPC AD0	11	12	GND				
				SMB_CLK	13	14	SMB_DATA				
				SB3V3	15	16	LPC SERIRQ				
				GND	17	18	CLKRUN#				
				SUS_STAT#	19	20	NC				

3.16 SPI Connector (SPI)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-			CLK	1	2	SB3V3	PWR	-	-	
	-		I	CS0#	3	4	GNT0#	IO		/1K3	
	10K/		I	CS1#	5	6	NC	-	-	-	
	10K/		I	MOSI	7	8	MFG#	IO		-	
	-		O	MISO	9	10	GND	PWR	-	-	

3.17 Front Panel Connector (FRONTPNL)

Note	Pull U/D	Ioh/ Iol	Type	Signal	PIN		Signal	Type	Ioh/ Iol	Pull U/D	Note
				USB10/11_5V	1	2	USB10/11_5V				
				USB1-	3	4	USB3-				
				USB1+	5	6	USB3+				
	-	-	PWR	GND	7	8	GND	PWR	-	-	
	-	-	-	NC	9	10	LINE2-IN-L	-	-	-	
	-	-	PWR	+5V	11	12	+5V	PWR	-	-	
			OC	HD_LED	13	14	SUS_LED				
	-	-	PWR	GND	15	16	PWRBTN_IN#				
				RSTIN#	17	18	GND	PWR	-	-	
				SB3V3	19	20	LINE2-IN-R	-	-	-	
				AGND	21	22	AGND				
				MIC2-L	23	24	MIC2-R				

Signal	Description
USB10/11_5V	5V supply for external devices. SB5V is supplied during powerdown to allow wakeup on USB device activity. Protected by resettable 1.1A fuse covering both USB ports.
USB1+ USB1-	Universal Serial Bus Port 1 Differentials: Bus Data/Address/Command Bus.
USB3+ USB3-	Universal Serial Bus Port 3 Differentials: Bus Data/Address/Command Bus.
+5V	Maximum load is 1A or 2A per pin if using IDC connector flat cable or crimp terminals respectively.
HD_LED	Hard Disk Activity LED (active low signal). Output is via 475Ω to OC.
SUS_LED	Suspend Mode LED (active high signal). Output is via 475Ω.
PWRBTN_IN#	Power Button In. Toggle this signal low to start the ATX / BTX PSU and boot the board.
RSTIN#	Reset Input. When pulled low for a minimum 16ms, the reset process will be initiated. The reset process continues even though the Reset Input is kept low.
LINE2-IN	Line in 2 signals
MIC2	MIC2-L and MIC2-R is second stereo microphone input.
SB3V3	Standby 3.3V voltage
AGND	Analogue Ground for Audio

Note 1: In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

3.18 Feature Connector (FEATURE)

Note	Pull U/D	Ioh/ Iol	Type	Signal	PIN		Signal	Type	Ioh/ Iol	Pull U/D	Note
2	2M/	-	I	INTRUDER#	1	2	GND	PWR	-	-	
			O	S5#	3	4	EXT_SMI#	I		4K7	3
			O	PWR_OK	5	6	SB5V	PWR	-	-	
	-	-	PWR	SB3V3	7	8	EXT_BAT	PWR	-	-	
	-	-	PWR	+5V	9	10	GND	PWR	-	-	
1	4K7/	/12mA	IOT	GPIO0	11	12	GPIO1	IOT	/12mA	4K7/	1
1	4K7/	/12mA	IOT	GPIO2	13	14	GPIO3	IOT	/12mA	4K7/	1
1	4K7/	/12mA	IOT	GPIO4	15	16	GPIO5	IOT	/12mA	4K7/	1
1	4K7/	/12mA	IOT	GPIO6	17	18	GPIO7	IOT	/12mA	4K7/	1
	-	-	PWR	GND	19	20	FAN3OUT	O		4K7	3
				FAN3IN	21	22	+12V	PWR	-	-	
				TEMP3IN	23	24	VREF				
	-	-	PWR	GND	25	26	IRRX				
				IRTX	27	28	GND	PWR	-	-	
1	4K7/			SMBC	29	30	SMBD			4K7/	1

Notes:

1. Pull-up to +3V3Dual (+3V3 or SB3V3).
2. Pull-up to on-board Battery.
3. Pull-up to +3V3.

Signal	Description
INTRUDER#	INTRUDER, may be used to detect if the system case has been opened. This signal's status is readable, so it may be used like a GPI when the Intruder switch is not required.
S5#	S5 sleep mode, active low output, optionally used to deactivate external system when in S5 sleep mode.
EXT_SMI#	External SMI, (active low input) signal can activate SMI interrupt.
PWR_OK	PoWeR OK, signal is high if no power failures are detected. (This is not the same as the P_OK signal generated by ATX PSU).
SB5V	StandBy +5V supply.
SB3V3	Max. load is 0.75A (1.5A < 1 sec.)
EXT_BAT	(EXTernal BATtery) option for connecting + terminal of an external primary cell battery (2.5 - 4.0 V) (– terminal connected to GND etc. pin 10). The external battery is protected against charging and can be used with or without the on-board battery installed.
+5V	Max. load is 0.75A (1.5A < 1 sec.)
GPIO0..7	General Purpose Inputs / Output. These Signals may be controlled or monitored through the use of the KT-API-V2 (Application Programming Interface).
FAN3OUT	FAN 3 speed control OUTput. This 3.3V PWM signal can be used as Fan control voltage (0–3.3V DC in 128 steps) via a Fan Driver Circuit (not included) to program Fan voltage. For more info, see W83627 datasheet. Default PMW output is 127 (100% = 3.3V).
FAN3IN	FAN3 Input. 0V to +3V3 amplitude Fan 3 tachometer input.
+12V	Max. load is 0.75A (1.5A < 1 sec.)
TEMP3IN	Temperature sensor 3 input. (Recommended: Transistor 2N3904, having emitter connected to GND (pin 25), collector and basis shorted and connected to pin 23. Further a resistor 30K/1% shall be connected between pin 23 - 24. (Precision +/- 3ºC).
VREF	Voltage REFerence, reference voltage to be used with TEMP3IN input.
IRRX	IR Receive input (IrDA 1.0, SIR up to 1.152K bps)
IRTX	IR Transmit output (IrDA 1.0, SIR up to 1.152K bps)
SMBC	SMBus Clock signal
SMBD	SMBus Data signal

3.19 PCI Slot Connector (PCI Slot)

Note	Type	Signal	Terminal S	Terminal C	Signal	Type	Note
	PWR	-12V	F01	E01	TRST#	O	
	O	TCK	F02	E02	+12V	PWR	
	PWR	GND	F03	E03	TMS	O	
NC	I	TDO	F04	E04	TDI	O	
	PWR	+5V	F05	E05	+5V	PWR	
	PWR	+5V	F06	E06	INTA#	I	
	I	INTB#	F07	E07	INTC#	I	
	I	INTD#	F08	E08	+5V	PWR	
NC	-	-	F09	E09	-	-	NC
NC	-	-	F10	E10	+5V (I/O)	PWR	
NC	-	-	F11	E11	-	-	NC
	PWR	GND	F12	E12	GND	PWR	
	PWR	GND	F13	E13	GND	PWR	
NC	-	-	F14	E14	GNT3#	OT	
	PWR	GND	F15	E15	RST#	O	
	O	CLKB	F16	E16	+5V (I/O)	PWR	
	PWR	GND	F17	E17	GNT0#	OT	
	I	REQ0#	F18	E18	GND	PWR	
	PWR	+5V (I/O)	F19	E19	PME#	I	
	IOT	AD31	F20	E20	AD30	IOT	
	IOT	AD29	F21	E21	+3.3V	PWR	
	PWR	GND	F22	E22	AD28	IOT	
	IOT	AD27	F23	E23	AD26	IOT	
	IOT	AD25	F24	E24	GND	PWR	
	PWR	+3.3V	F25	E25	AD24	IOT	
	IOT	C/BE3#	F26	E26	GNT1#	OT	
	IOT	AD23	F27	E27	+3.3V	PWR	
	PWR	GND	F28	E28	AD22	IOT	
	IOT	AD21	F29	E29	AD20	IOT	
	IOT	AD19	F30	E30	GND	PWR	
	PWR	+3.3V	F31	E31	AD18	IOT	
	IOT	AD17	F32	E32	AD16	IOT	
	IOT	C/BE2#	F33	E33	+3.3V	PWR	
	PWR	GND	F34	E34	FRAME#	IOT	
	IOT	IRDY#	F35	E35	GND	PWR	
	PWR	+3.3V	F36	E36	TRDY#	IOT	
	IOT	DEVSEL#	F37	E37	GND	PWR	
	PWR	GND	F38	E38	STOP#	IOT	
	IOT	LOCK#	F39	E39	+3.3V	PWR	
	IOT	PERR#	F40	E40	SDONE	IO	
	PWR	+3.3V	F41	E41	SB0#	IO	
	IOC	SERR#	F42	E42	GND	PWR	
	PWR	+3.3V	F43	E43	PAR	IOT	
	IOT	C/BE1#	F44	E44	AD15	IOT	
	IOT	AD14	F45	E45	+3.3V	PWR	
	PWR	GND	F46	E46	AD13	IOT	
	IOT	AD12	F47	E47	AD11	IOT	
	IOT	AD10	F48	E48	GND	PWR	
	PWR	GND	F49	E49	AD09	IOT	
SOLDER SIDE					**COMPONENT SIDE**		
	IOT	AD08	F52	E52	C/BE0#	IOT	
	IOT	AD07	F53	E53	+3.3V	PWR	
	PWR	+3.3V	F54	E54	AD06	IOT	
	IOT	AD05	F55	E55	AD04	IOT	
	IOT	AD03	F56	F56	GND	PWR	
	PWR	GND	F57	E57	AD02	IOT	
	IOT	AD01	F58	E58	AD00	IOT	
	PWR	+5V (I/O)	F59	E59	+5V (I/O)	PWR	
	IOT	ACK64#	F60	E60	REQ64#	IOT	
	PWR	+5V	F61	E61	+5V	PWR	
	PWR	+5V	F62	E62	+5V	PWR	

3.19.1 Signal Description – PCI Slot Connector

SYSTEM PINS	
CLK	Clock provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals, except RST#, INTA#, INTB#, INTC#, and INTD#, are sampled on the risingedge of CLK and all other timing parameters are defined with respect to this edge. PCI operates at 33MHz.
PME#	Power Management Event interrupt signal. Wake up signal.
RST#	Reset is used to bring PCI-specific registers, sequencers, and signals to a consistent state. What effect RST# has on a device beyond the PCI sequencer is beyond the scope of this specification, except for reset states of required PCI configuration registers. Anytime RST# is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be asynchronously tri-stated. SERR# (open drain) is floated. REQ# and GNT# must both be tri-stated (they cannot be driven low or high during reset). To prevent AD, C/BE#, and PAR signals from floating during reset, the central resource may drive these lines during reset (bus parking) but only to a logic low level–they may not be driven high. RST# may be asynchronous to CLK when asserted or deasserted. Although asynchronous, deassertion is guaranteed to be a clean, bounce-free edge. Except for configuration accesses, only devices that are required to boot the system will respond after reset.
ADDRESS AND DATA	
AD[31::00]	Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the clock cycle in which FRAME# is asserted. During the address phase AD[31::00] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases AD[07::00] contain the least significant byte (lsb) and AD[31::24] contain the most significant byte (msb). Write data is stable and valid when IRDY# is asserted and read data is stable and valid when TRDY# is asserted. Data is transferred during those clocks where both IRDY# and TRDY# are asserted.
C/BE[3::0]#	Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3::0]# define the bus command. During the data phase C/BE[3::0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE[0]# applies to byte 0 (lsb) and C/BE[3]# applies to byte 3 (msb).
PAR	Parity is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. (PAR has the same timing as AD[31::00], but it is delayed by one clock.) The master drives PAR for address and write data phases; the target drives PAR for read data phases.
INTERFACE CONTROL PINS	
FRAME#	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase or has completed.
IRDY#	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD[31::00]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
TRDY#	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD[31::00]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
STOP#	Stop indicates the current target is requesting the master to stop the current transaction.
LOCK#	Lock indicates an atomic operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked. A grant to start a transaction on PCI does not guarantee control of LOCK#. Control of LOCK# is obtained under its own protocol in conjunction with GNT#. It is possible for different agents to use PCI while a single master retains ownership of LOCK#. If a device implements Executable Memory, it should also implement LOCK# and guarantee complete access exclusion in that memory. A target of an access that supports LOCK# must provide exclusion to a minimum of 16 bytes (aligned). Host bridges that have system memory behind them should implement LOCK# as a target from the PCI bus point of view and optionally as a master.
IDSEL	Initialization Device Select is used as a chip select during configuration read and write transactions.
DEVSEL#	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

(Continues)

ARBITRATION PINS (BUS MASTERS ONLY)	
REQ#	Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ# which must be tri-stated while RST# is asserted.
GNT#	Grant indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNT# which must be ignored while RST# is asserted. While RST# is asserted, the arbiter must ignore all REQ# lines since they are tri-stated and do not contain a valid request. The arbiter can only perform arbitration after RST# is deasserted. A master must ignore its GNT# while RST# is asserted. REQ# and GNT# are tri-state signals due to power sequencing requirements when 3.3V or 5.0V only add-in boards are used with add-in boards that use a universal I/O buffer.
ERROR REPORTING PINS. The error reporting pins are required by all devices and maybe asserted when enabled	
PERR#	Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The PERR# pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected. (If sequential data phases each have a data parity error, the PERR# signal will be asserted for more than a single clock.) PERR# must be driven high for one clock before being tri-stated as with all sustained tri-state signals. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed. An agent cannot report a PERR# until it has claimed the access by asserting DEVSEL# (for a target) and completed a data phase or is the master of the current transaction.
SERR#	System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required. SERR# is pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of SERR# is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of SERR# to the deasserted state is accomplished by a weak pullup (same value as used for s/t/s) which is provided by the system designer and not by the 57signaling agent or central resource. This pull-up may take two to three clock periods to fully restore SERR#. The agent that reports SERR#s to the operating system does so anytime SERR# is sampled asserted.
INTERRUPT PINS (OPTIONAL). Interrupts on PCI are optional and defined as “level sensitive,” asserted low (negative true), using open drain output drivers. The assertion and deassertion of INTx# is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device deasserts its INTx# signal. PCI defines one interrupt line for a single function device and up to four interrupt lines for a multi-function device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning.	
INTA#	Interrupt A is used to request an interrupt.
INTB#	Interrupt B is used to request an interrupt and only has meaning on a multi-function device.
INTC#	Interrupt C is used to request an interrupt and only has meaning on a multi-function device.
INTD#	Interrupt D is used to request an interrupt and only has meaning on a multi-function device.

3.19.2 KTGM45 PCI IRQ & INT routing

Board type	Slot	REQ	GNT	IDSEL	INTA	INTB	INTC	INTD
KTGM45/mITX	0	REQ0#	GNT0#	AD16	INT_PIRQ#A	INT_PIRQ#B	INT_PIRQ#C	INT_PIRQ#D
KTGM45/Flex	0	REQ0#	GNT0#	AD16	INT_PIRQ#A	INT_PIRQ#B	INT_PIRQ#C	INT_PIRQ#D
	1	REQ1#	GNT1#	AD17	INT_PIRQ#E	INT_PIRQ#F	INT_PIRQ#G	INT_PIRQ#H
KTGM45/ATXE	0	REQ0#	GNT0#	AD16	INT_PIRQ#A	INT_PIRQ#B	INT_PIRQ#C	INT_PIRQ#D
	1	REQ1#	GNT1#	AD17	INT_PIRQ#E	INT_PIRQ#F	INT_PIRQ#G	INT_PIRQ#H
	2	REQ2#	GNT2#	AD18	INT_PIRQ#C	INT_PIRQ#D	INT_PIRQ#B	INT_PIRQ#A
	3	REQ3#	GNT3#	AD19	INT_PIRQ#D	INT_PIRQ#C	INT_PIRQ#F	INT_PIRQ#G
	4	REQ4#	GNT4#	AD20	INT_PIRQ#F	INT_PIRQ#G	INT_PIRQ#H	INT_PIRQ#E

When using the 820982 “PCI Riser - Flex - 2slot w. arbiter” the lower slot has IDSEL / IRQs routed straight through and the top slot has the routing: IDSEL=AD22, INT_PIRQ#F, INT_PIRQ#G, INT_PIRQ#H, INT_PIRQ#E. 820982 PCI Riser shall be plugged into Slot 0.

4 On-board - & mating connectors

Connector	On-board Connectors		Mating Connectors	
	Manufacturer	Type no.	Manufacturer	Type no.
FAN_CPU	Foxconn	HF2704E-M1	AMP	1375820-4 (4-pole)
FAN_SYS	AMP	1470947-1	AMP	1375820-3 (3-pole)
KBDMSE	Molex	22-23-2061	Molex	22-01-2065
CDROM	Foxconn	HF1104E	Molex	50-57-9404
	Molex	70543-0038		
SATA	Hon Hai	LD1807V-S52T	Molex	67489-8005
			Kontron	KT 821035 (cable kit)
ATXPWR	Molex	44206-0002	Molex	5557-24R
ATX+12V-4pin	Lotes	ABA-POW-003-K02	Molex	39-01-2045
LVDS	Don Connex	C44-40BSB1-G	Don Connex	A32-40-C-G-B-1
			Kontron	KT 821515 (cable kit)
			Kontron	KT 821155 (cable kit)
COM2, 3, 4	Wuerth	61201020621	Molex	90635-1103
			Kontron	KT 821016 (cable kit)
			Kontron	KT 821017 (cable kit)
USB6/7, 8/9, 10/11	Pinrex	512-90-10GBB2	Kontron	KT 821401 (cable kit)
USB1/USB3 (*)	(FRONTPNL)	-	Kontron	KT 821401 (cable kit)
IEEE1394			Kontron	KT 821040 (cable kit)
AUDIO_HEAD	Molex	87831-2620	Molex	51110-2651
			Kontron	KT 821043 (cable kit)
FRONTPNL	Pinrex	512-90-24GBB3	Molex	90635-1243
			Kontron	KT 821042 (cable kit)
FEATURE	Molex	87831-3020	Molex	51110-3051
			Kontron	KT 821041 (cable kit)

* USB1/USB3 is located in FRONTPNL connector. Depending on application the KT821401 can be used.

Note: Only one connector will be mentioned for each type of on-board connector even though several types with same fit, form and function are approved and could be used as alternative. Please also notice that standard connectors like DVI, PCIe, PCI, CF, Ethernet and USB is not included in the list.

5 System Resources

5.1 Memory Map

Address (hex)		Size	Description
00000000	0009FFFF	655360	System board
000A0000	000BFFFF	131072	PCI-bus
000A0000	000BFFFF	131072	Mobile Intel(R) 4 Series Express Chipset Family
000C0000	000CFFFF	65536	System board
000D0000	000DFFFF	65536	PCI-bus
000E0000	000FFFFF	131072	System board
00100000	3DBFFFFF	1034944512	System board
3DC00000	DFFFFFFF	2722103296	PCI-bus
D0000000	DFFFFFFF	268435456	Mobile Intel(R) 4 Series Express Chipset Family
E0000000	EFFFFFFF	268435456	Motherboard resources
F0000000	FED8FFFF	249102336	PCI-bus
FE000000	FE3FFFFF	4194304	Mobile Intel(R) 4 Series Express Chipset Family
FE600000	FE6FFFFF	1048576	Mobile Intel(R) 4 Series Express Chipset Family
FE7C0000	FE7DFFFF	131072	Intel(R) 82567LM Gigabit Network Connection
FE7F4000	FE7F7FFF	16384	Microsoft UAA-bus driver for High Definition Audio
FE7FA000	FE7FAFFF	131072	Intel(R) 82567LM Gigabit Network Connection
FE7FB000	FE7FB00F	16	PCI controller for simple communication
FE7FB400	FE7FB7FF	1024	Intel(R) ICH9 Family USB2 Enhanced Host Controller - 293C
FEAFB800	FEAFBBFF	1024	Intel(R) ICH9 Family USB2 Enhanced Host Controller - 293A
FE7FBC00	FE7FBCFF	256	Intel(R) ICH9 Family SMBus Controller - 2930
FE800000	FE8FFFFF	1048576	Intel(R) ICH9 Family PCI Express Root Port 2 - 2942
FE8FF000	FE8FFFFF	4096	OHCI Compliant IEEE 1394-Værtscontroller
FE900000	FE9FFFFF	1048576	Intel(R) ICH9 Family PCI Express Root Port 3 - 2944
FE9DC000	FE9DFFFF	16384	Intel(R) 82574L Gigabit Network Connection #2
FE9E0000	FE9FFFFF	131072	Intel(R) 82574L Gigabit Network Connection #2
FEA00000	FEAFFFFF	1048576	Intel(R) ICH9 Family PCI Express Root Port 4 - 2946
FEAE0000	FEAEFFFF	65536	PCI Standart PCI to PCI-Brigde
FEB00000	FEBFFFFF	1048576	Intel(R) ICH9 Family PCI Express Root Port 5 – 2948
FEBDC000	FEBDFFFF	16384	Intel(R) 82574L Gigabit Network Connection
FEBE0000	FEBFFFFF	131072	Intel(R) 82574L Gigabit Network Connection
FEC00000	FEC00FFF	4096	Motherboard resources
FED00000	FED003FF	1024	High Precision timer
FED10000	FED19FFF	40960	Motherboard resources
FED1C000	FED1FFFF	16384	Motherboard resources
FED20000	FED3FFFF	131072	Motherboard resources
FED40000	FED8FFFF	327680	Motherboard resources
FED90000	FFFFFFFF	19333120	System Board
FEE00000	FEE00FFF	4096	Motherboard resources
FFB00000	FFBFFFFF	1048576	Intel(R) 82802 Firmware-hub unit
FFC00000	FFEFFFFF	3145728	Motherboard resources
FFF00000	FFFFFFFF	1048576	Intel(R) 82802 Firmware-hub unit

5.2 PCI Devices

Bus #	Device #	Function #	Vendor ID	Device ID	Chip	Device Function
0	0	0	8086	2A40	GM45 Chipset	Host Bridge
0	2	0	8086	2A42	GM45 Chipset	VGA Controller
0	2	1	8086	2A43	GM45 Chipset	VGA Controller
0	3	0	8086	2A44	GM45 Chipset	Management Engine
0	25	0	8086	10F5	82567LM LAN	Gigabit Network Connection
0	26	0	8086	2937	ICH9R	USB Universal Host Controller
0	26	1	8086	2938	ICH9R	USB Universal Host Controller
0	26	2	8086	2939	ICH9R	USB Universal Host Controller
0	26	7	8086	293C	ICH9R	USB Universal Host Controller
0	27	0	8086	293E	ICH9R	High Definition Audio Controller
0	28	0	8086	2940	ICH9R	PCI to PCI Bridge
0	28	1	8086	2942	ICH9R	PCI to PCI Bridge
0	28	2	8086	2944	ICH9R	PCI to PCI Bridge
0	28	3	8086	2946	ICH9R	PCI to PCI Bridge
0	28	4	8086	2948	ICH9R	PCI to PCI Bridge
0	29	0	8086	2934	ICH9R	USB Universal Host Controller
0	29	1	8086	2935	ICH9R	USB Universal Host Controller
0	29	2	8086	2936	ICH9R	USB Universal Host Controller
0	29	7	8086	293A	ICH9R	USB Universal Host Controller
0	30	0	8086	2448	ICH9R	PCI to PCI Bridge
0	31	0	8086	2917	ICH9R	ISA Bridge
0	31	2	8086	2928	ICH9R	IDE Controller
0	31	3	8086	2930	ICH9R	SMBus Controller
0	31	5	8086	292D	ICH9R	IDE Controller
2	0	0	197B	2368	JMB368	IDE PATA Controller
3	0	0	11C1	5901	FW533 FireWire	FireWire Controller
4	0	0	8086	10D3	82574L LAN	Gigabit Network Connection
5	0	0	10B5	8505	PEX8505 PCI	PCI to PCI Bridge
6	1	0	10B5	8505	PEX8505 PCI	PCI to PCI Bridge
6	2	0	10B5	8505	PEX8505 PCI	PCI to PCI Bridge
6	3	0	10B5	8505	PEX8505 PCI	PCI to PCI Bridge
6	4	0	10B5	8505	PEX8505 PCI	PCI to PCI Bridge
11	0	0	8086	10D3	82574L LAN	Gigabit Network Connection

5.3 Interrupt Usage

IRQ	System timer	Keyboard	Communications port COM1 Selection in BIOS	Communications port COM2 Selection in BIOS	Communication port COM3/COM4 Selection in BIOS	System CMOS/real-time watch	Microsoft ACPI-compatible system	Numerical Data Processor	Primary IDE-channel	Secondary IDE-channel	Intel(R) 82574L Gigabit Network Connection	Intel(R) Management Engine Interface	Intel(R) GM45 Express Chipset	Intel(R) ICH9 PCI Express Root Port (5x)	Intel(R) ICH9 USB Enhanced Host Controller (x 2)	Intel(R) ICH9 USB Universal Host Controller (x 6)	Intel(R) ICH9 Serial ATA Storage Controller 2	Intel(R) 82567LM Gigabit Network Connection (x2)	Microsoft UAA-bus driver for High Definition Audio	PS2 Mouse	PCI to PCI Express bridge	OHCI Compliant IEEE 194 Controller	Notes
NMI																							
IRQ0	X																						
IRQ1		X																					
IRQ2																							
IRQ3				X																			
IRQ4			X																				
IRQ5																							
IRQ6																							
IRQ7																							
IRQ8						X																	
IRQ9							X																
IRQ10					X																		
IRQ11					X																		
IRQ12																				X			
IRQ13								X															
IRQ14									X														
IRQ15										X													
IRQ16											X	X	X	X		X		X			X		
IRQ17														X							X	X	
IRQ18														X	X	X					X		
IRQ19														X		X	X				X		
IRQ20																		X					
IRQ21																X							
IRQ22																			X				
IRQ23															X	X							
IRQ24																							
IRQ25																							
IRQ26																							

5.4 IO Map

Address range (hex)		Size	Description
0	F	16	DMA-controller
0	CF7	3320	PCI-bus
10	1F	16	Motherboard resources
20	21	2	Programmable interrupt controller
22	3F	30	Motherboard resources
40	43	4	System timer
44	5F	28	Motherboard resources
60	60	1	Standard keyboard
61	61	1	System Speaker
62	63	2	Motherboard resources
64	64	1	Standard keyboard
65	6F	11	Motherboard resources
70	71	2	System CMOS/Real time clock
72	7F	14	Motherboard resources
80	80	1	Motherboard resources
81	83	3	DMA-controller
84	86	3	Motherboard resources
87	87	1	DMA-controller
88	88	1	Motherboard resources
89	8B	3	DMA-controller
8C	8E	3	Motherboard resources
8F	8F	1	DMA-controller
90	9F	16	Motherboard resources
A0	A1	2	Programmable interrupt controller
A2	BF	30	Motherboard resources
C0	DF	32	DMA-controller
E0	EF	16	Motherboard resources
F0	FF	16	Numerical Data Processor
170	177	8	Secondary IDE-channel
1F0	1F7	8	Primary IDE-channel
274	277	4	ISAPNP read data port
279	279	1	ISAPNP read data port
2E8	2EF	8	Communications port (COM4)
2F8	2FF	8	Communications port (COM2)
376	376	1	Secondary IDE-channel
3B0	3BB	12	Mobile Intel(R) 4 Series Express Chipset Family
3C0	3DF	32	Mobile Intel(R) 4 Series Express Chipset Family
3E8	3EF	8	Communications port (COM3)
3F6	3F6	1	Primary IDE-channel
3F8	3FF	8	Communications port (COM1)
400	41F	32	Intel(R) ICH10 Family SMBus Controller - 3A60
4D0	4D1	2	Motherboard resources
500	57F	128	Motherboard resources
800	87F	128	Motherboard resources
A00	A0F	16	Motherboard resources
A10	A1F	16	Motherboard resources
A79	A79	1	ISAPNP read data port
D00	FFFF	62208	PCI-bus
9C00	9C07	8	Mobile Intel(R) 4 Series Express Chipset Family
A000	A01F	32	Intel(R) 82567LM Gigabit Network
A080	A09F	32	Intel(R) ICH9 Family USB Universal Host Controller - 2939
A400	A41F	32	Intel(R) ICH9 Family USB Universal Host Controller - 2938
A480	A49F	32	Intel(R) ICH9 Family USB Universal Host Controller - 2937
A800	A81F	32	Intel(R) ICH9 Family USB Universal Host Controller - 2936
A880	A89F	32	Intel(R) ICH9 Family USB Universal Host Controller - 2935
AC00	AC1F	32	Intel(R) ICH9 Family USB Universal Host Controller - 2934

B000	B00F	16	Intel(R) ICH9M/M-E 2 port Serial ATA Storage Controller 2 - 292D
B080	B08F	16	Intel(R) ICH9M/M-E 2 port Serial ATA Storage Controller 2 - 292D
B400	B403	4	Intel(R) ICH9M/M-E 2 port Serial ATA Storage Controller 2 - 292D
B480	B487	8	Intel(R) ICH9M/M-E 2 port Serial ATA Storage Controller 2 - 292D
B800	B803	4	Intel(R) ICH9M/M-E 2 port Serial ATA Storage Controller 2 - 292D
B880	B887	8	Intel(R) ICH9M/M-E 2 port Serial ATA Storage Controller 2 - 292D
C000	CFFF	4096	Intel(R) ICH9 Family PCI Express Root Port 1 - 2940
C400	C40F	16	Standard Dual Channel PCI IDE Controller
C480	C483	16	Standard Dual Channel PCI IDE Controller
C800	C807	8	Standard Dual Channel PCI IDE Controller
C880	C883	4	Standard Dual Channel PCI IDE Controller
CC00	CC07	8	Standard Dual Channel PCI IDE Controller
D000	DFFF	4096	Intel(R) ICH9 Family PCI Express Root Port 3 - 2944
DC00	DC1F	32	Intel(R) 82574L Gigabit Network Connection
E000	EFFF	4096	Intel(R) ICH9 Family PCI Express Root Port 5 - 2948
EC00	EC1F	32	Intel(R) 82574L Gigabit Network Connection
FF90	FF9F	16	Intel(R) ICH9M/M-E 2 port Serial ATA Storage Controller 1 - 2928
FFA0	FFAF	16	Intel(R) ICH9M/M-E 2 port Serial ATA Storage Controller 1 - 2928

6 BIOS

This section details specific BIOS features for the KTGM45 board.
The KTGM45 board is based on the AMI BIOS core version 8.00.16 with Kontron BIOS extensions.

6.1 System Management BIOS (SMBIOS/DMI)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components.

The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS.

The BIOS stores and reports the following SMBIOS information:
• BIOS data, such as the BIOS revision level
• Fixed-system data, such as peripherals, serial numbers, and asset tags
• Resource data, such as memory size, cache size, and processor speed
• Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT*, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

6.2 Legacy USB Support

Legacy USB support enables USB devices such as keyboards, mice, and hubs to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support is Disabled in the BIOS Setup.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

6.3 BIOS Update

The BIOS can be updated using Kontron utility called bf.exe, which are available on the Kontron Web site. The utility supports DOS and Windows environment. Before updating the BIOS, AMT related restrictions must be followed.

Warning: Do not attempts to ignore below steps as it might result in corrupted BIOS
Before BIOS update make sure there is only RAM in SLOT 0 (socket closest to the CPU).
After BIOS update make sure there is RAM in SLOT 1 (socket farthest away from the CPU)

.

7 BIOS setup

7.1 Introduction

The BIOS Setup is used to view and configure BIOS settings for the KTGM45 board. The BIOS Setup is accessed by pressing the DEL key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The Menu bar looks like this:

```
                              BIOS SETUP UTILITY
  Main    Advanced    PCIPnP    Boot    Security    Chipset    Exit
```

The available keys for the Menu screens are:

Select Menu: <←> or <→>
Select Item: <↑> or <↓>
Select Field: <Tab>
Change Field: <+> or <->
Help: <F1>
Save and Exit: <F10>
Exits the Menu: <Esc>

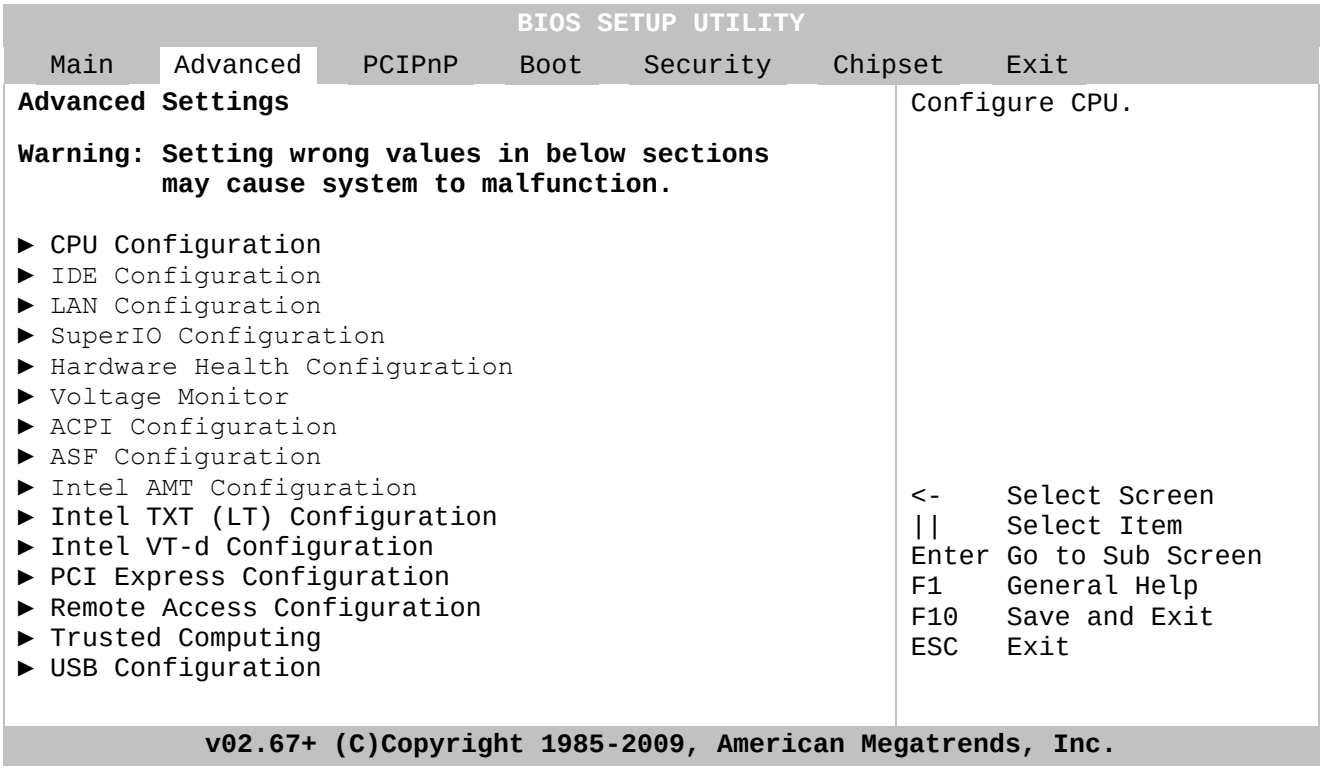
Please note that in the following the different BIOS Features will be described as having some options. These options will be selected automatically when loading either Failsafe Defaults or Optimal Defaults. The Default options will be indicated by the option in **bold**, but please notice that when Failsafe Defaults are loaded a few of the options, marked with "*", are now the default option.

7.2 Main Menu

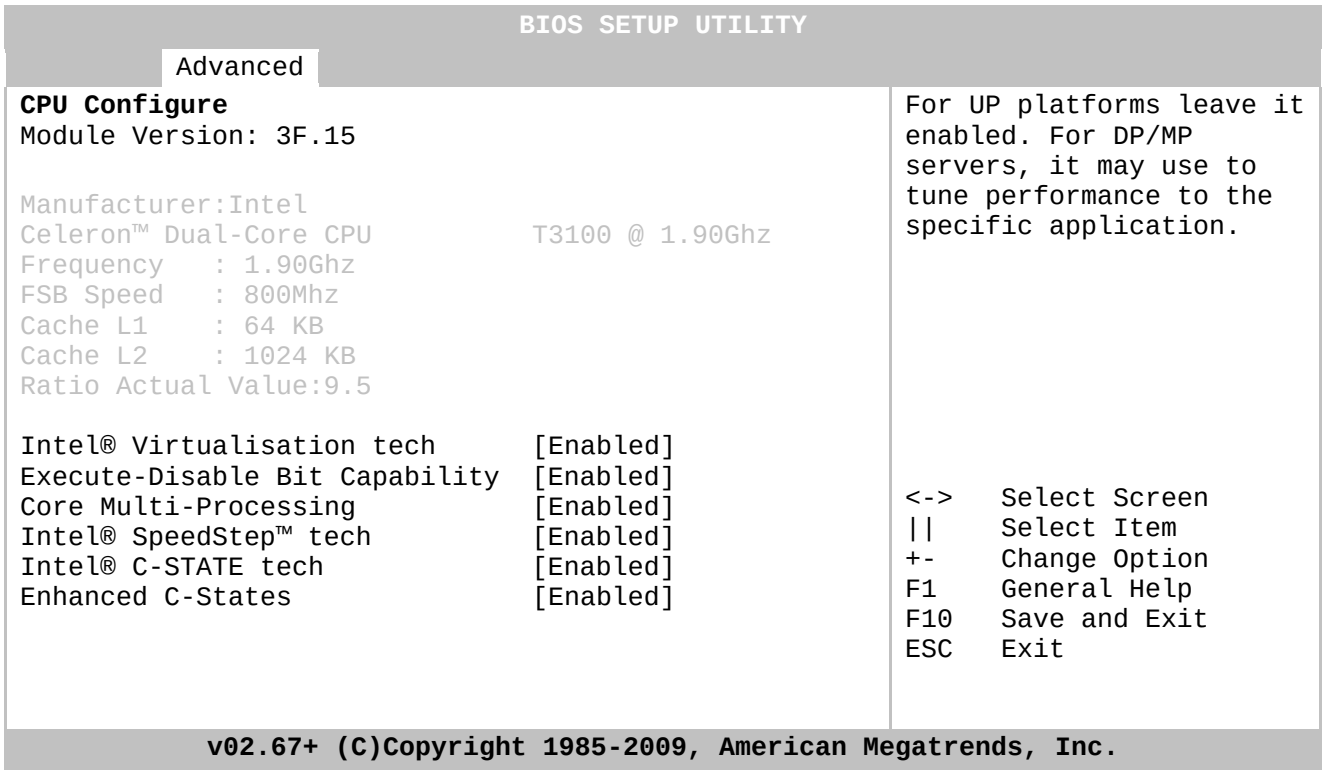
```
                              BIOS SETUP UTILITY
  Main    Advanced    PCIPnP    Boot    Security    Chipset    Exit
System Overview                                   Use [ENTER], [TAB] or
                                                  [SHIFT-TAB] to select a
AMIBIOS                                           field.
Version    : 08.00.16
Build Date: 11/19/10                              Use [+] or [-] to
ID         : KTGM4510                             configure system Time.
PCB ID     : 10
Serial #   : 00831693
Part   #   : 62400000

Processor
Celeron ™ Dual-Core CPU      T3100 @ 1.90GHz
Speed      : 1900MHz                              <->  Select Screen
                                                  ||   Select Item
System Memory                                     +-   Change Field
Size       : 2971MB                               Tab  Select Field
                                                  F1   General Help
System Time                  [10:18:13]           F10  Save and Exit
System Date                  [Thu 11/22/2010]     ESC  Exit
System Date/Time Backup      [Disabled]
          v02.67+ (C)Copyright 1985-2006, American Megatrends, Inc.
```

Feature	Options	Description
System Time	HH:MM:SS	Set the system time.
System Date	MM/DD/YYYY	Set the system date.
System Date/Time Backup	Enabled **Disabled**	Enabled then corrupted Date & Time will be recovered from HP RTC.

7.3 Advanced Menu

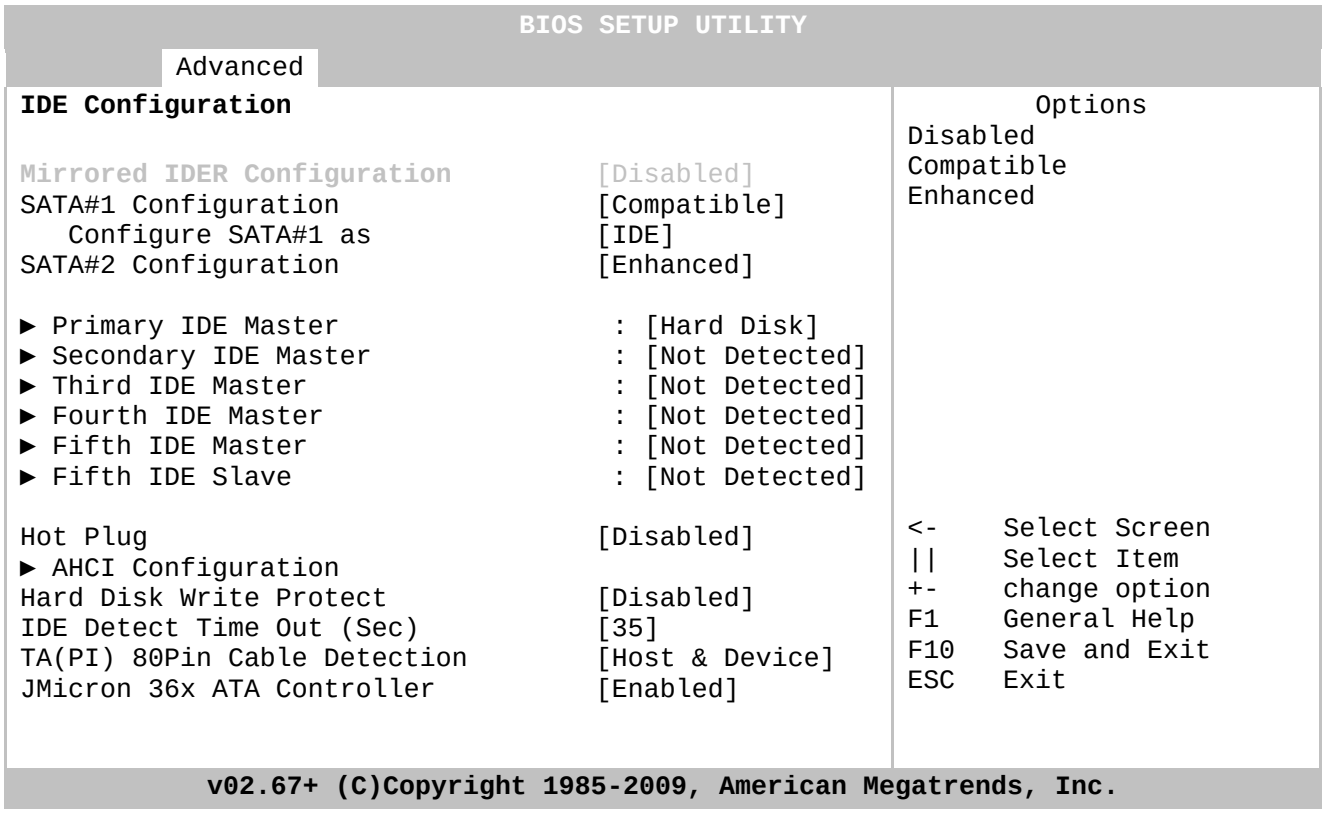


7.3.1 Advanced settings – CPU Configuration



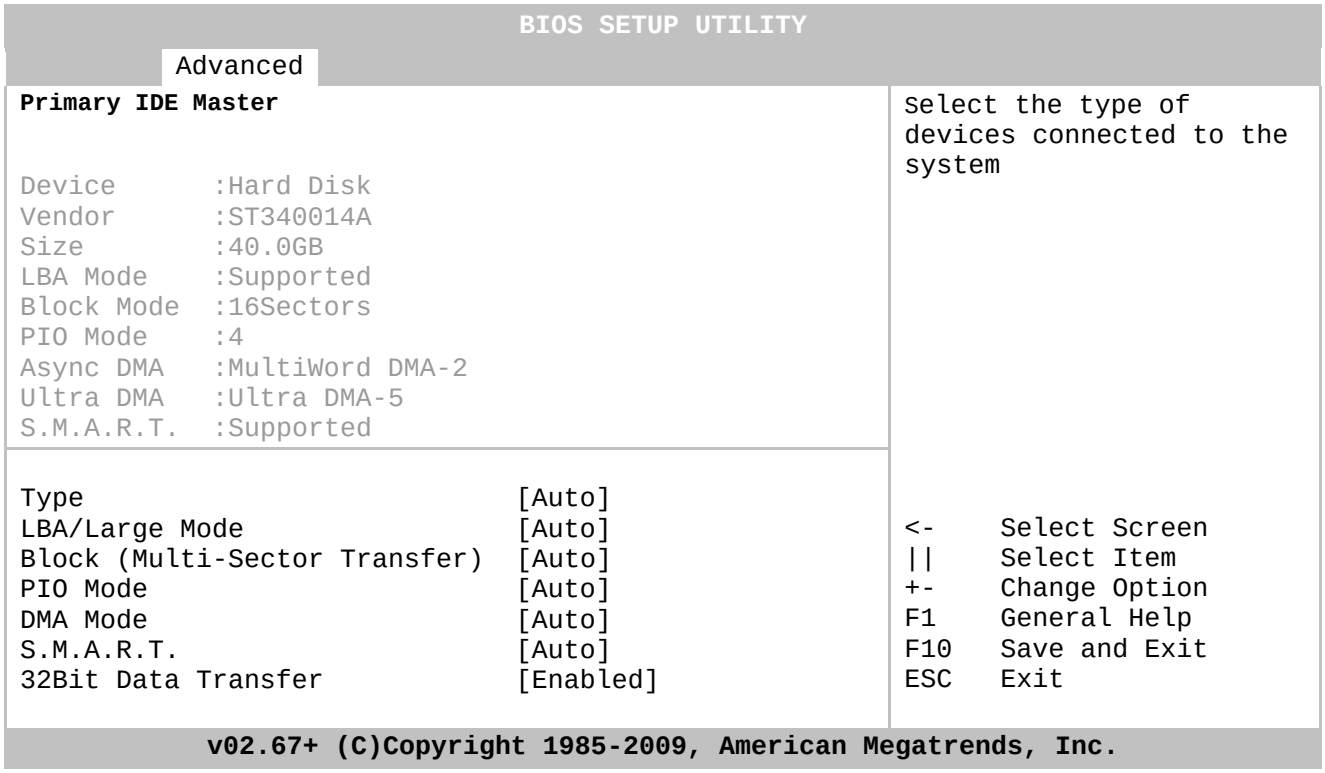
Feature	Options	Description
Intel® Virtualisation tech	Disabled **Enabled**	When enabled, A VMM can utilize the additional HW Caps. Provided by Intel® Virtualization Tech. Note: A full reset is required to change the setting.
Execute-Disable Bit Capability	Disabled **Enabled**	When disabled, force the XD feature flag to always return 0.
Core Multi-Processing	Disabled **Enabled**	When disabled, disable one execution core of each CPU die.
Intel® SpeedStep™ tech	Disabled **Enabled**	Disabled: Disable GV3 Enabled: Enable GV3
Intel® C-STATE tech	Disabled **Enabled**	CState: CPU idle is set to C2 C3 C4 State
Enhanced C-States	Disabled **Enabled**	CState: CPU idle is set to Enhanced C-States.

7.3.2 Advanced settings – IDE Configuration



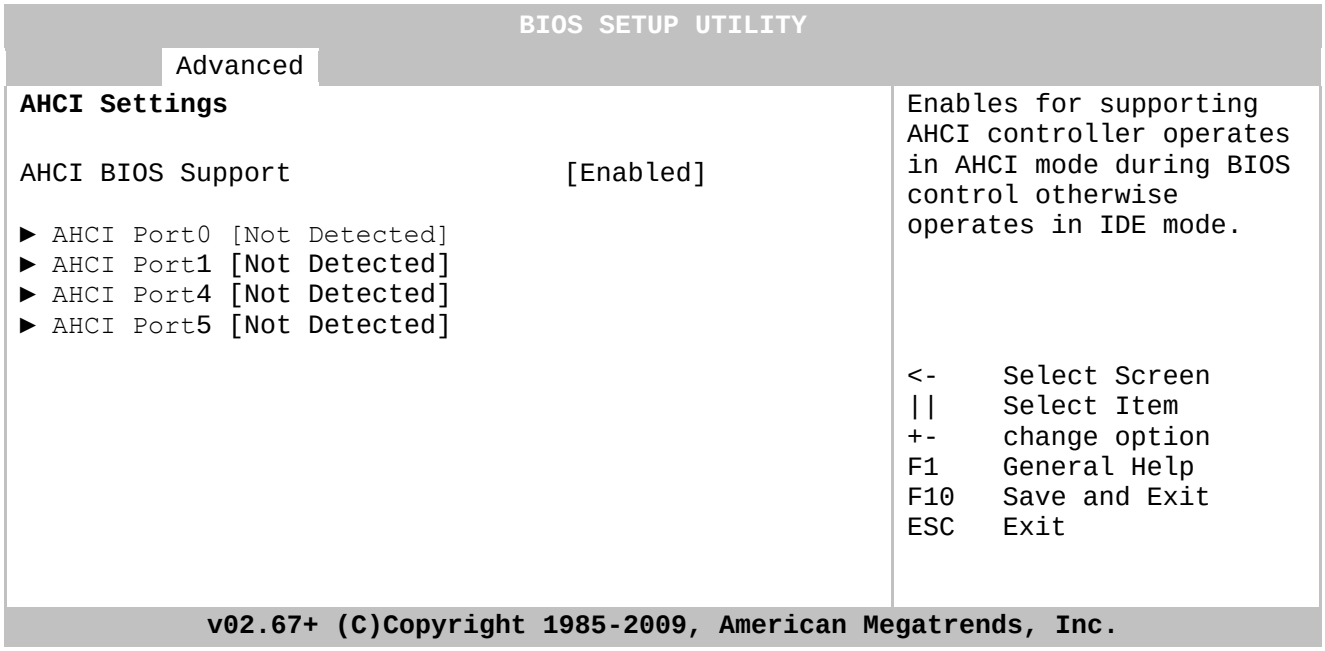
Feature	Options	Description
SATA#1 Configuration	Disabled **Compatible** Enhanced	Disabled Compatible Enhanced
Configure SATA#1 as	**IDE** RAID AHCI	IDE RAID AHCI
SATA#2 Configuration	Disabled **Enhanced**	Disabled Enhanced

Note: When RAID shall be used in XP then use “Floppy_F6” driver (load RAID driver via Floppy Disk). The RAID driver must be installed even if the OS shall be executed from a HDD not included in the RAID. When XP Installation CD is started then after approx. ½ minute it will for a few seconds ask you to press <F6> for special driver selection (do that). System will continue loading files but after a minute or so it will ask you to press the <S>-key. Now load the Floppy Disk and press the <S> key. Select the ”Intel(R) ICH9M-E/M SATA AHCI Controller". System will ask you for more special drivers, but just skip that by pressing <Enter>.

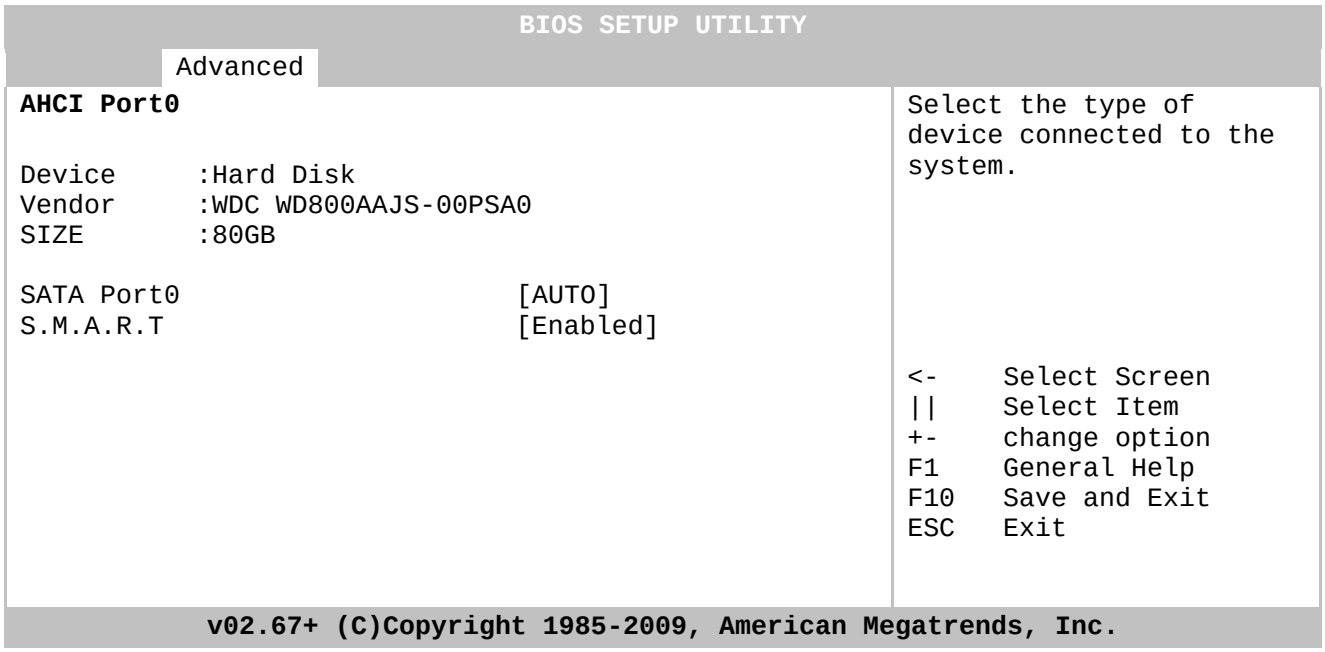


Feature	Options	Description
Type	Not Installed **Auto** CD/DVD ARMD	Select the type of device installed
LBA/Large Mode	Disabled **Auto**	Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads, and Sectors.
Block (Multi-Sector Transfer)	Disabled **Auto**	Select if the device should run in Block mode
PIO Mode	**Auto** 0 1 2 3 4	Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform.
DMA Mode	**Auto** SWDMA0 SWDMA1 SWDMA2 MWDMA0 MWDMA1 MWDMA2 UDMA0 UDMA1 UDMA2 UDMA3 UDMA4 UDMA5 UDMA6	Selects the Ultra DMA mode used for moving data to/from the drive. Autotype the drive to select the optimum transfer mode. **Note: To use UDMA Mode 2, 3, 4, 5 and 6 with a device, the harddisk cable used MUST be UDMA66/100 cable (80-conductor cable).**
S.M.A.R.T.	**Auto** Disabled Enabled	Select if the Device should be monitoring itself (Self-Monitoring, Analysis and Reporting Technology System)
32Bit Data Transfer	Disabled* **Enabled**	Select if the Device should be using 32Bit data Transfer

Feature	Options	Description
Hot Plug	**Disabled** Enabled	(Only available if SATA#1 is RAID or AHCI)



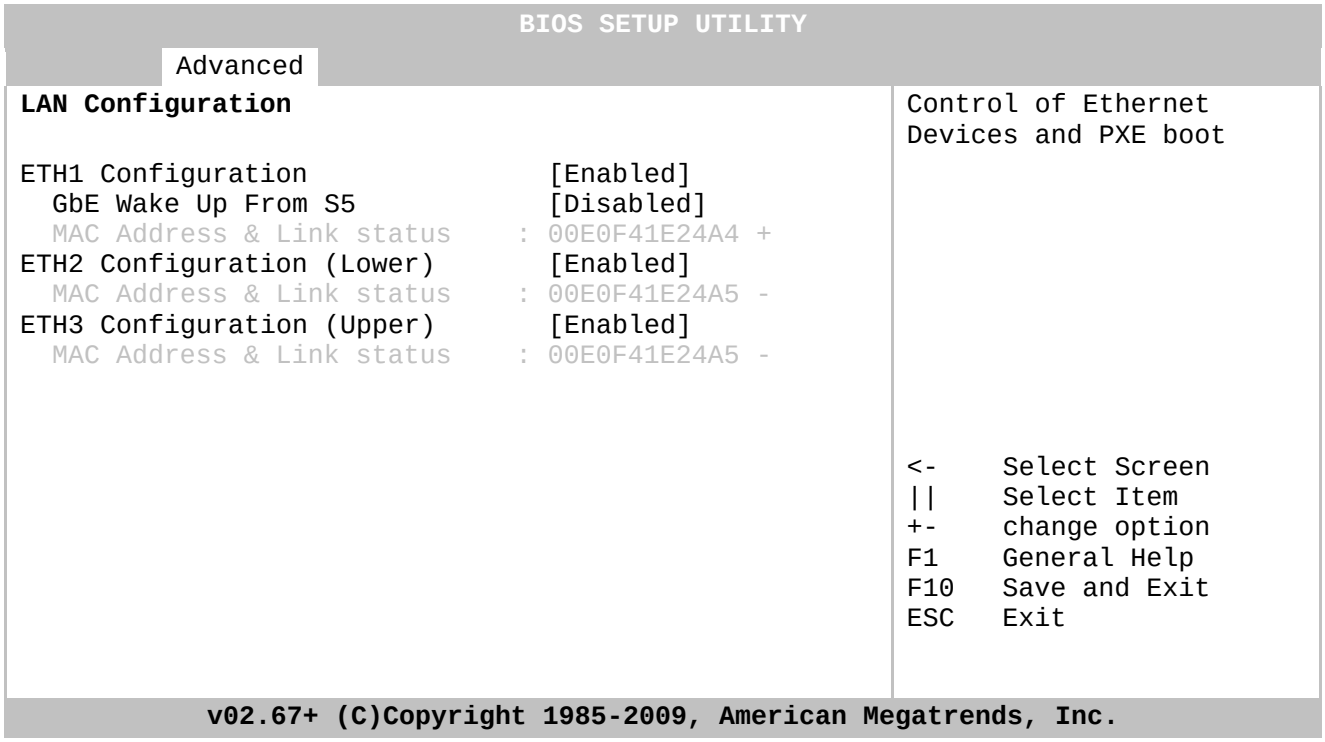
Feature	Options	Description
AHCI BIOS Support	Disabled **Enabled**	Enables for supporting AHCI controller operates in AHCI mode during BIOS control otherwise operates in IDE mode.



Feature	Options	Description
SATA Port0	**Auto** Not Installed	Select the type of device connected to the system.
S.M.A.R.T	**Enabled** Disabled	S.M.A.R.T. stands for Self-Monitoring, Analysis and Reporting Technology.

Feature	Options	Description
Hard Disk Write Protect	**Disabled** Enabled	Disable/Enable device write protection. This will be effective only if device is accessed through BIOS
IDE Detect Time Out (Sec)	0 5 10 15 20 25 30 **35**	Select the timeout value for detecting ATA/ATAPI device(s)
ATA(PI) 80Pin Cable Detection	**Host & Device** Host Device	Select the mechanism for detecting 80Pin ATA(PI) Cable
JMicron 36x ATA Controller	Disabled **Enabled**	Select ATA Controller Operate Mode

7.3.3 Advanced settings – LAN Configuration



Feature	Options	Description
ETH1 Configuration	Disabled **Enabled** With RPL/PXE boot	Disable/enable LAN or enabled with RPL/PXE boot
GbE Wake Up From S5	**Disabled** Enabled	WOL (Wake On Lan) (See note 3)

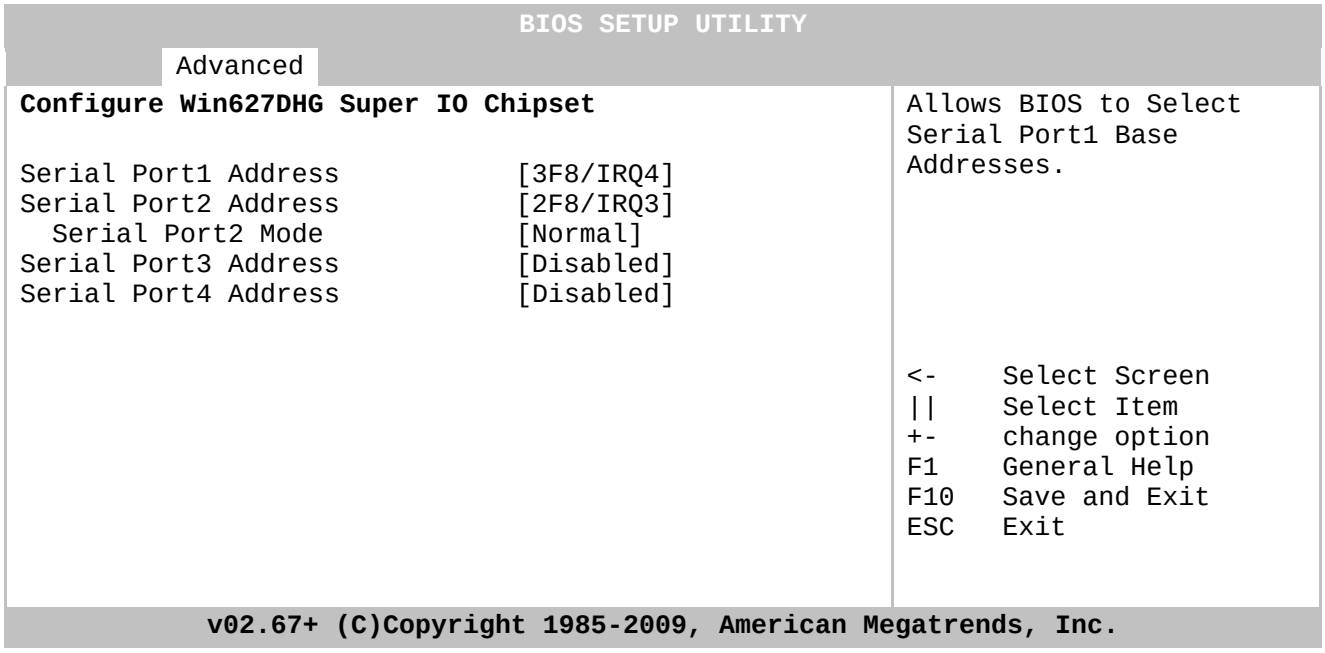
Feature	Options	Description
ETH2 Configuration (Lower)	Disabled **Enabled** With RPL/PXE boot	Disable/enable LAN or enabled with RPL/PXE boot

Feature	Options	Description
ETH3 Configuration (Upper)	Disabled **Enabled** With RPL/PXE boot	Disable/enable LAN or enabled with RPL/PXE boot

Notes:

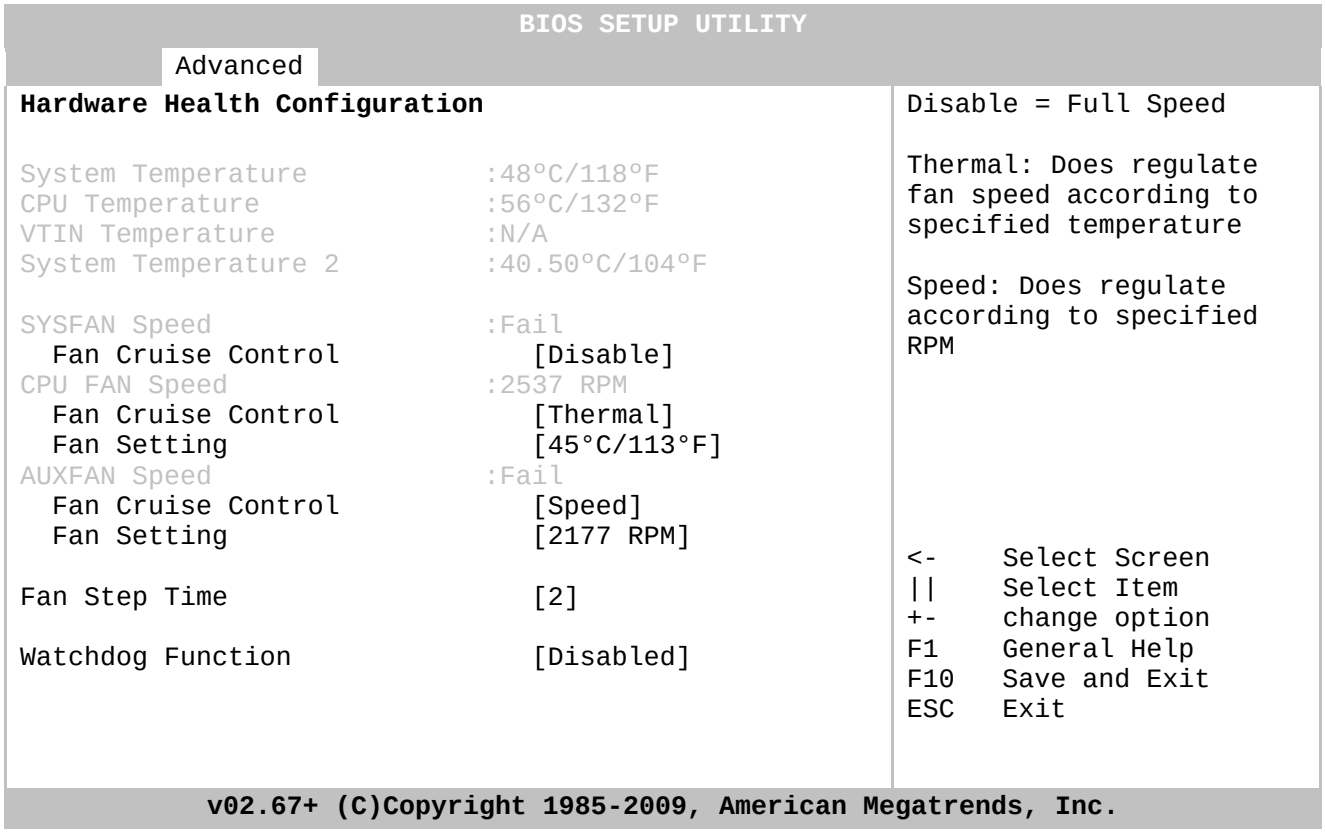
1. The “+” and “-“ (to the right of the MAC address) indicates if link is established or not.
2. ETH1 (and only ETH1) can be used for AMT.
3. WOL only possible if “Intel AMT Support” is enabled.

7.3.4 Advanced settings – Configure Win627DHG Super IO Chipset



Feature	Options	Description
Serial Port1 Address	Disabled **3F8/IRQ4** 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Select the BASE I/O address and IRQ. (The available options depend on the setup for the other Serial Ports).
Serial Port2 Address	**Disabled** 3F8/IRQ4 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Select the BASE I/O address and IRQ. (The available options depend on the setup for the other Serial Ports).
Serial Port2 Mode	**Normal** IrDA ASK IR	Select Mode for Serial Port2
If IrDA or ASK IR: IR Duplex Mode	Full Duplex **Half Duplex**	IrDA communication selection
Serial Port3 Address	**Disabled** 3F8 2F8 3E8 2E8	Allows BIOS to select Serial Port3 Base Addresses (The available options depend on the setup for the other Serial Ports).
Serial Port3 IRQ	IRQ3 IRQ4 IRQ10 **IRQ11**	Allows BIOS to select Serial Port3 IRQ. (The available options depend on the setup for the other Serial Ports).
Serial Port4 Address	**Disabled** 3F8 2F8 3E8 2E8	Allows BIOS to select Serial Port3 Base Addresses (The available options depend on the setup for the other Serial Ports).
Serial Port4 IRQ	IRQ3 IRQ4 **IRQ10** IRQ11	Allows BIOS to select Serial Port3 IRQ. (The available options depend on the setup for the other Serial Ports).

7.3.5 Advanced settings – Hardware Health Configuration



Feature	Options	Description
Fan Cruise Control	**Disabled** Thermal Speed	Select how the Fan shall operate. When set to Thermal, the Fan will start to run at the CPU die temperature set below. When set to Speed, the Fan will run at the fixed speed set below.
Fan Settings	1406-5625 RPM 30°-60°C	The fan can operate in Thermal mode or in a fixed fan speed mode
Fan Step Time	0, 1, **2**, 3, 4, 5, 6, 7	Fan regulation delay. (0 is fast and 7 is slow)
Watchdog	**Disabled** 15 seconds 30 seconds 1 minute 2 minutes 5 minutes 10 minutes	Adjust the amount of boot time allowed before system reset occurs. Refer to “KT-API-V2 User Manual” to control the Watchdog via API or refer to “KT-API-V2 User Manual DLL” how to control Watchdog via Windows DLL.

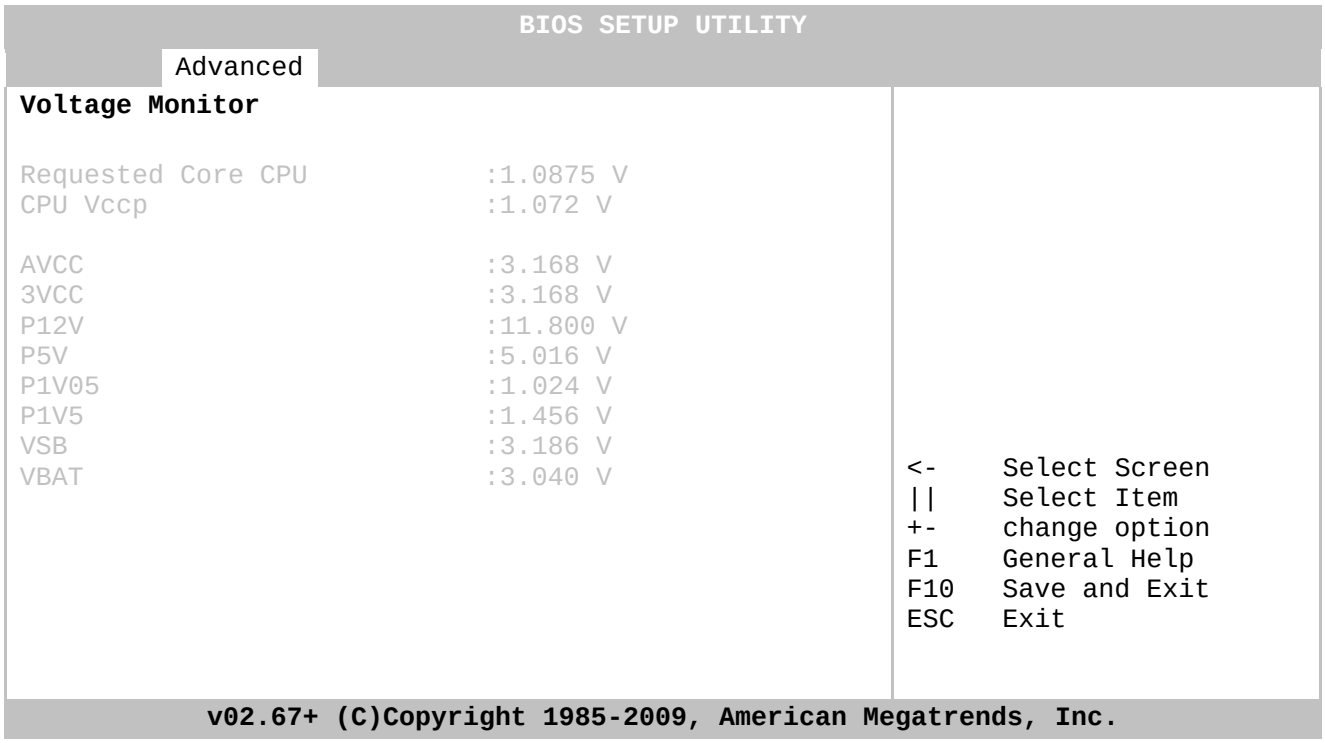
Notes: The AUXFAN is available via Feature Connector.

System Temperature is measured via IO Controller and temperature sensor transistor and this value can be used to setup SYSFAN for Thermal cruise control.

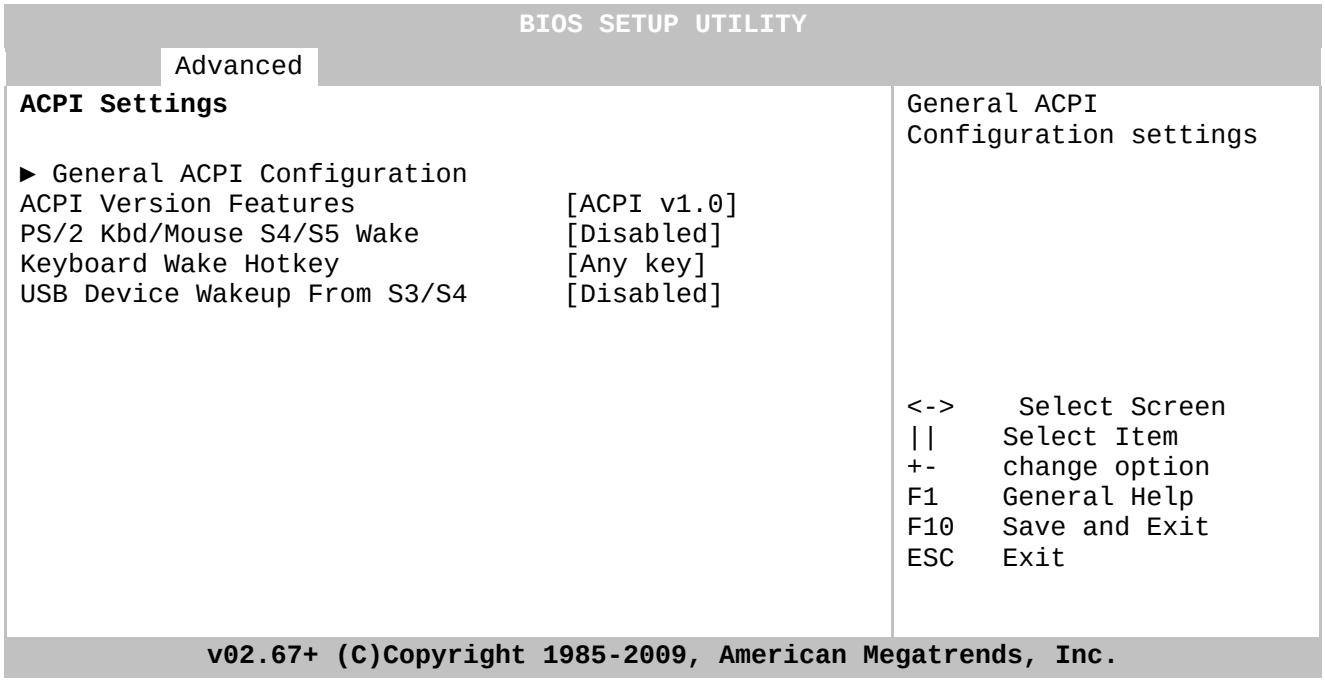
System Temperature 2 is measured via HP RTC circuit and is only used for readout in Hardware Health Configuration menu. (No calibration required, tolerance is +/- 3ºC)

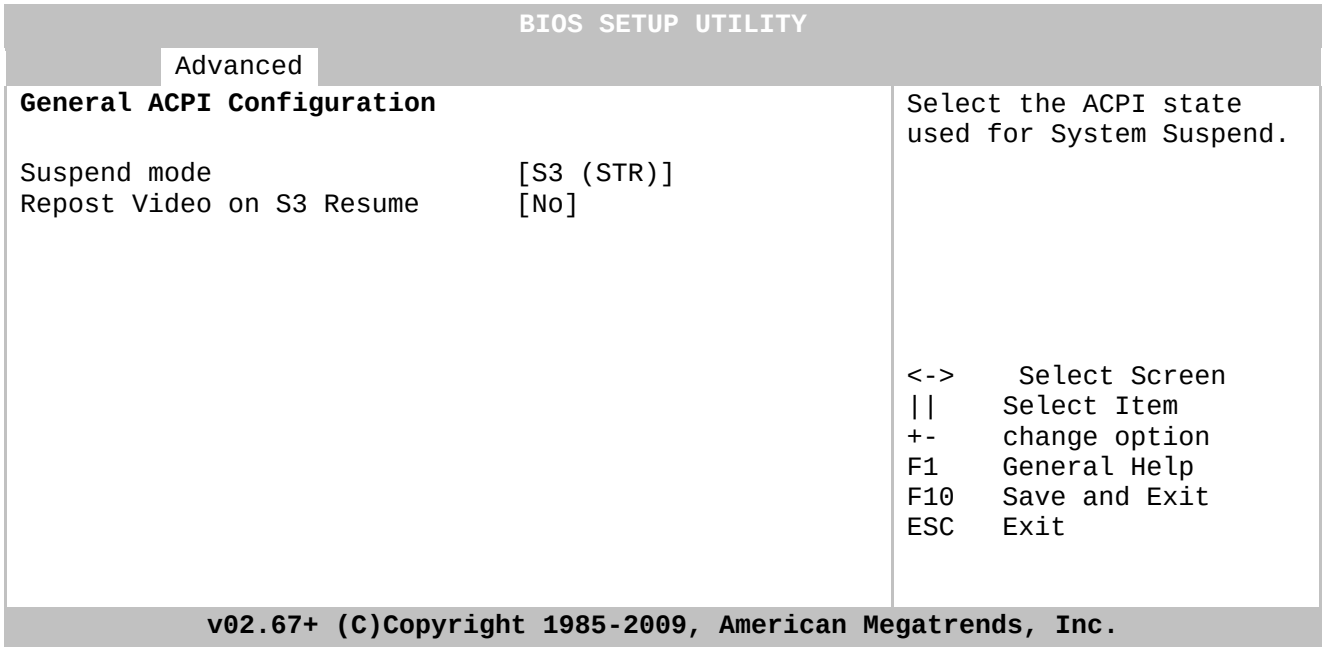
In Fan Cruise Control = Thermal, the BIOS setup PWM = 0% when no RPM is required, but fans like the one used in PN 1036-2048 has a minimum RPM (PWM = 0 – 30% => RPM=1200+/-250).

7.3.6 Advanced settings – Voltage Monitor



7.3.7 Advanced settings – ACPI Settings

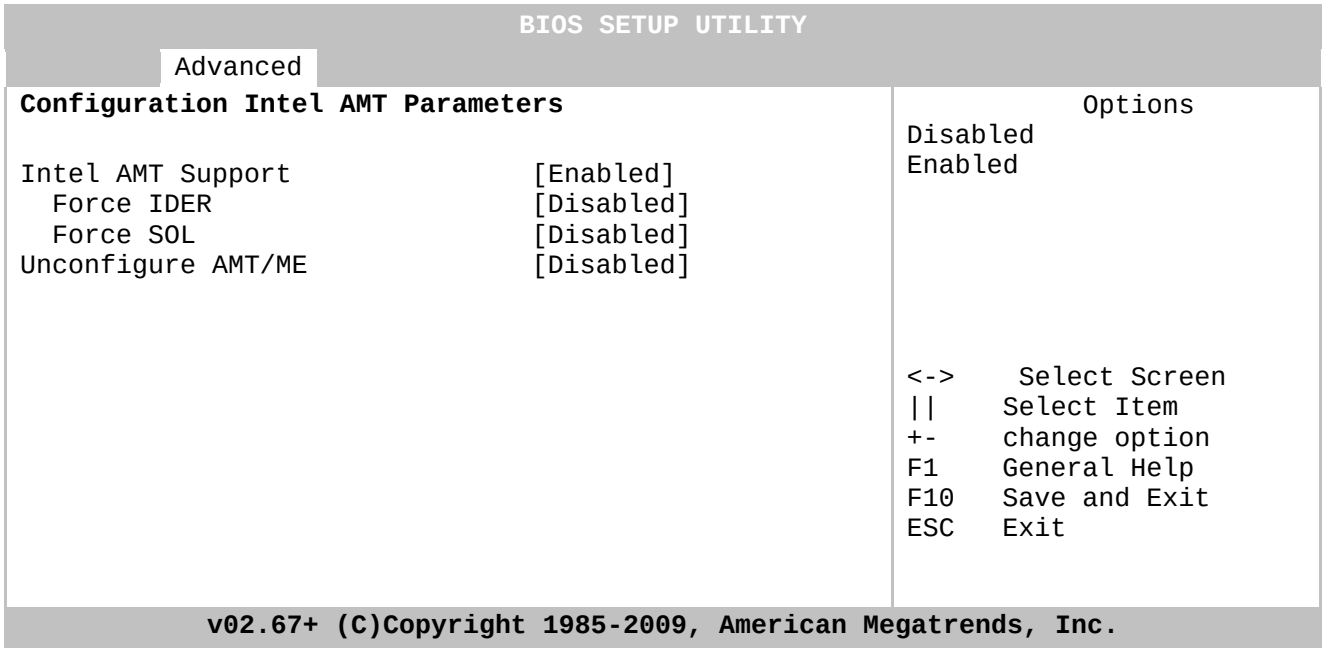




Feature	Options	Description
Suspend mode	S1 (POS) **S3 (STR)**	Select the ACPI state used for System Suspend
Repost Video on S3 Resume	**No** Yes	Determines whether to invoke VGA BIOS post on S3/STR resume

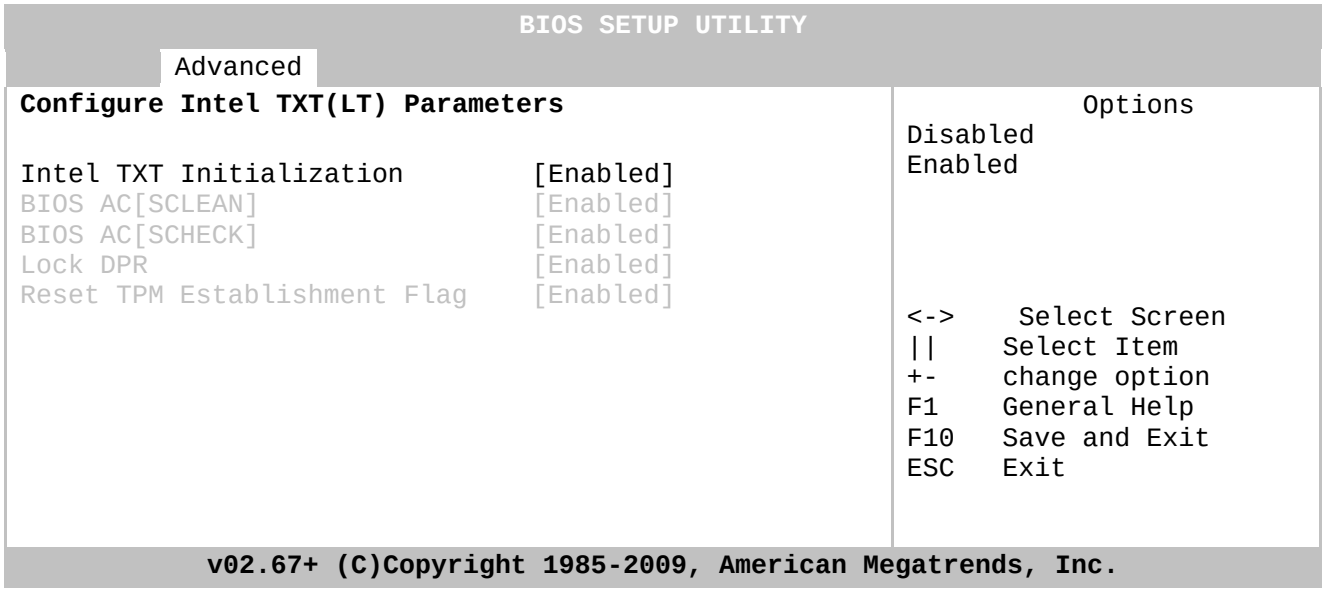
Feature	Options	Description
ACPI Version Features	**ACPI v1.0** ACPI v2.0 ACPI v3.0	Enabled RSDP pointers to 64-bit Fixed System Description Tabled. Different ACPI version has some addition.
PS/2 Kbd/Mouse S4/S5 Wake	**Disabled** Enabled	Enabled: The System can also be waked from S4 or S5. Disabled: PS/2 Kbd or Mouse can still wake system from S3
Keyboard Wake Hotkey	**Any key** “Space” “Enter” “Sleep button”	Any key “Space” “Enter” “Sleep button”
USB Device Wakeup from S3/S4	**Disabled** Enabled	Enabled/Disable USB Device Wakeup From S3/S4.

7.3.8 Advanced settings – Intel AMT Configuration



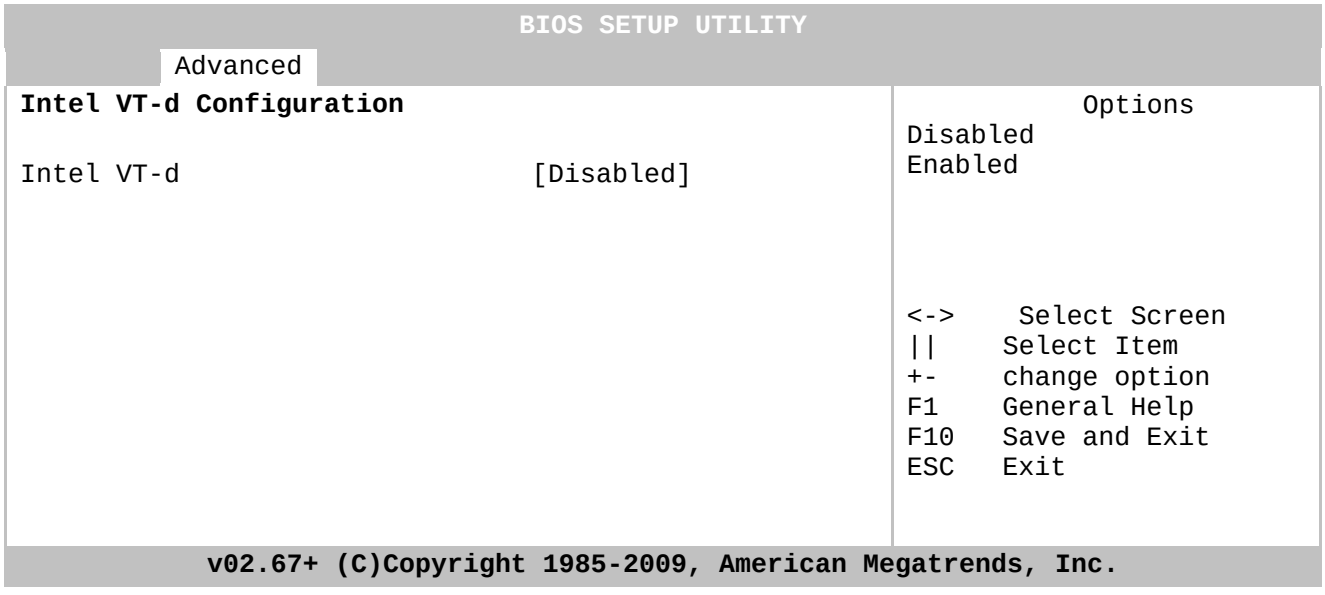
Feature	Options	Description
Intel AMT Support	**Disabled** Enabled	Options Disabled Enabled
Force IDER	**Disabled** IDER Pri. Master IDER Pri. Slave IDER Sec. Master IDER Pri. Slave	Options Disabled IDER Pri. Master IDER Pri. Slave IDER Sec. Master IDER Pri. Slave
Force SOL	**Disabled** Enabled	Options Disabled Enabled
Unconfigure AMT/ME	**Disabled** Enabled	Options Disabled Enabled

7.3.9 Advanced settings – Intel TXT(LT) Configuration



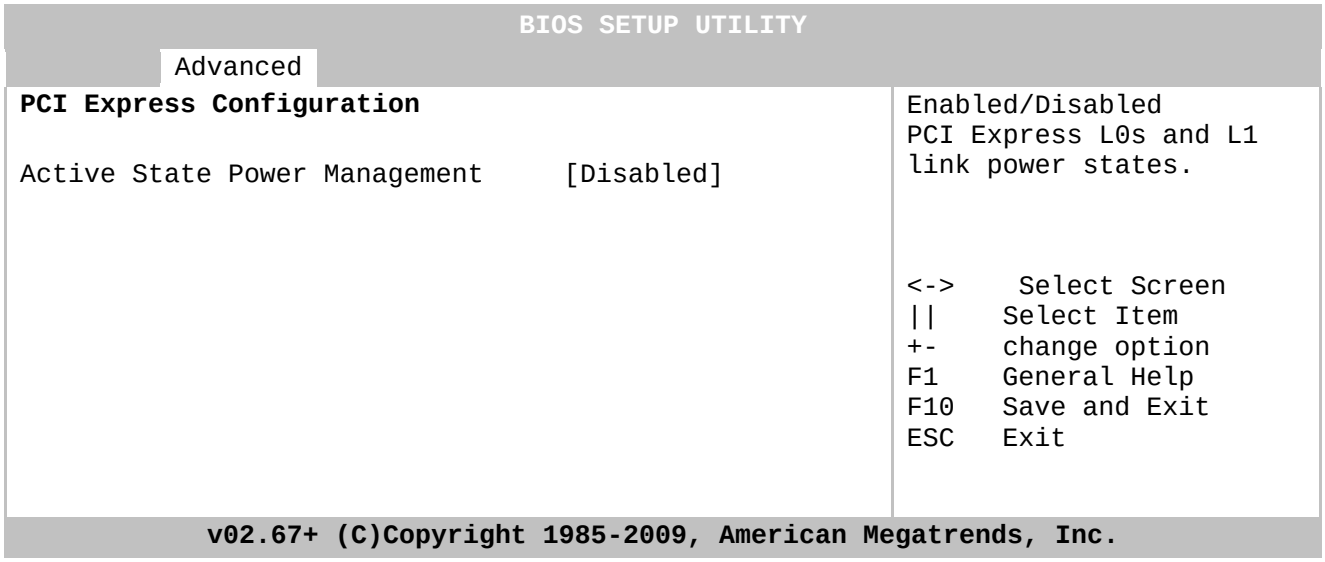
Feature	Options	Description
Intel TXT Initialization	**Disabled** Enabled	Disabled Enabled

7.3.10 Advanced settings – Intel VT-d Configuration



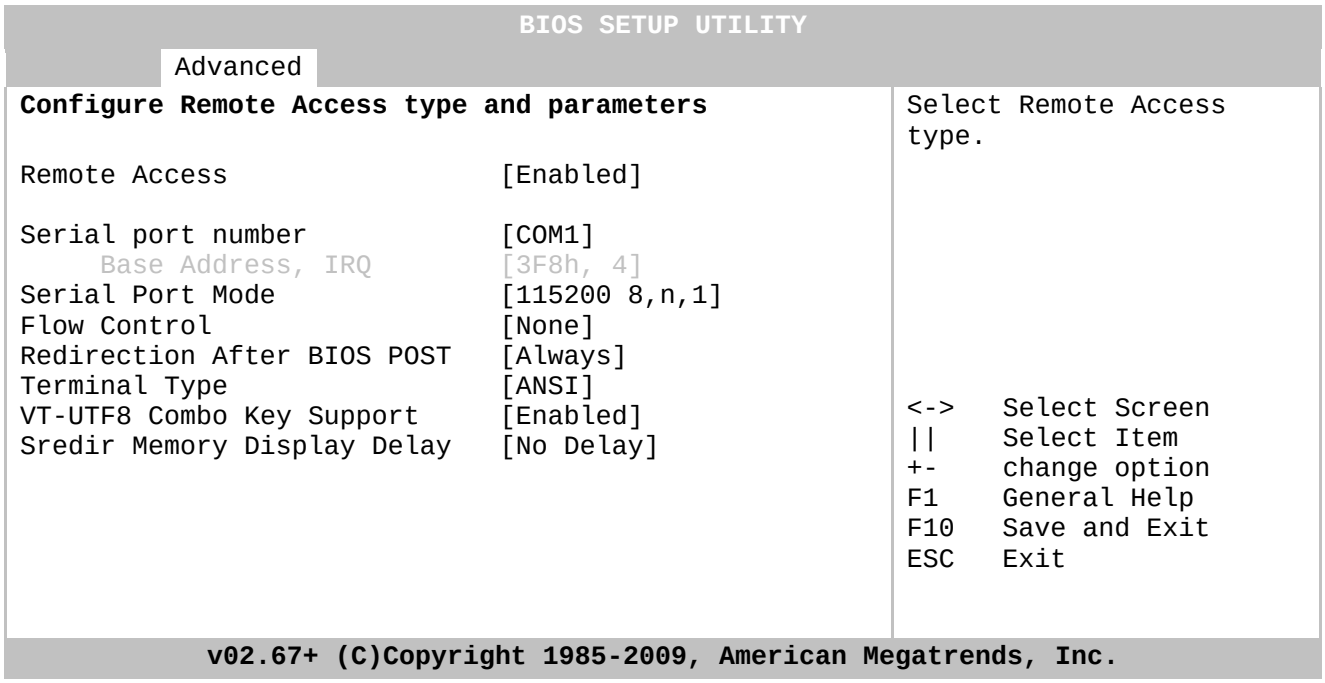
Feature	Options	Description
Intel VT-d	**Disabled** Enabled	Disabled Enabled

7.3.11 Advanced settings – PCI Express Configuration



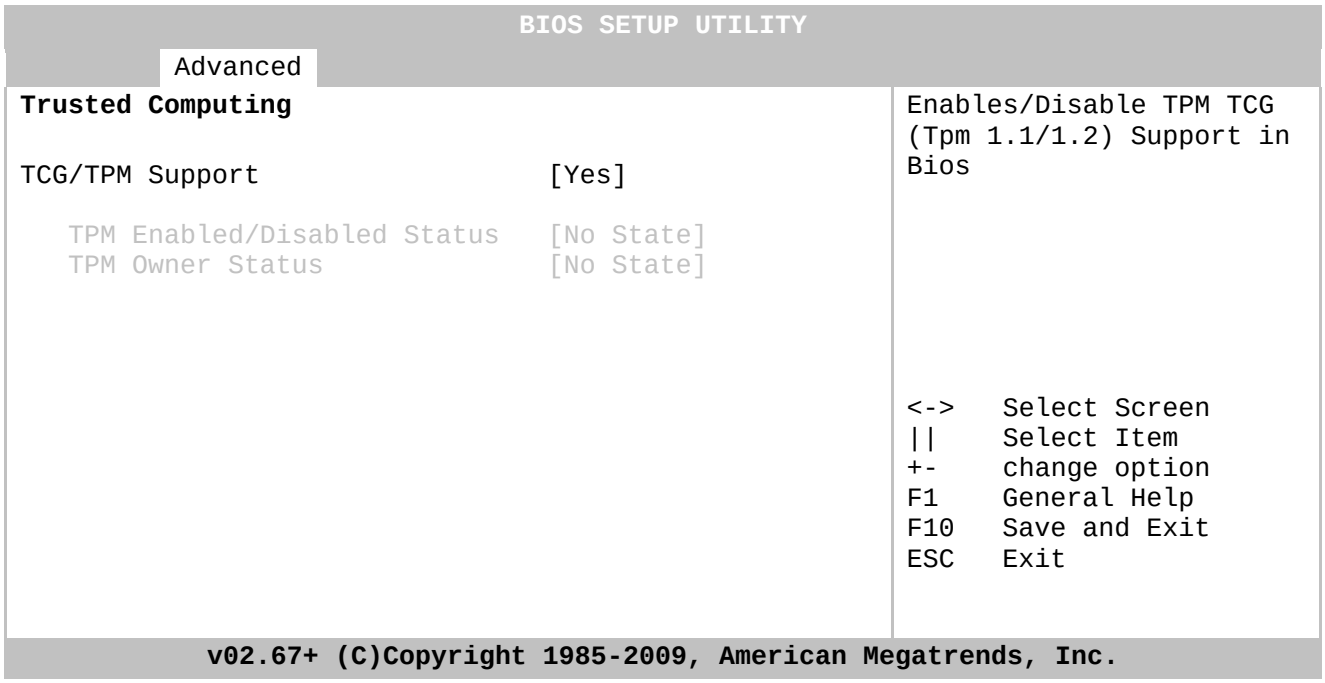
Feature	Options	Description
Active State Power Management	**Disabled** Enabled	Enabled/Disabled PCI Express L0s and L1 link power states.

7.3.12 Advanced settings – Remote Access Configuration



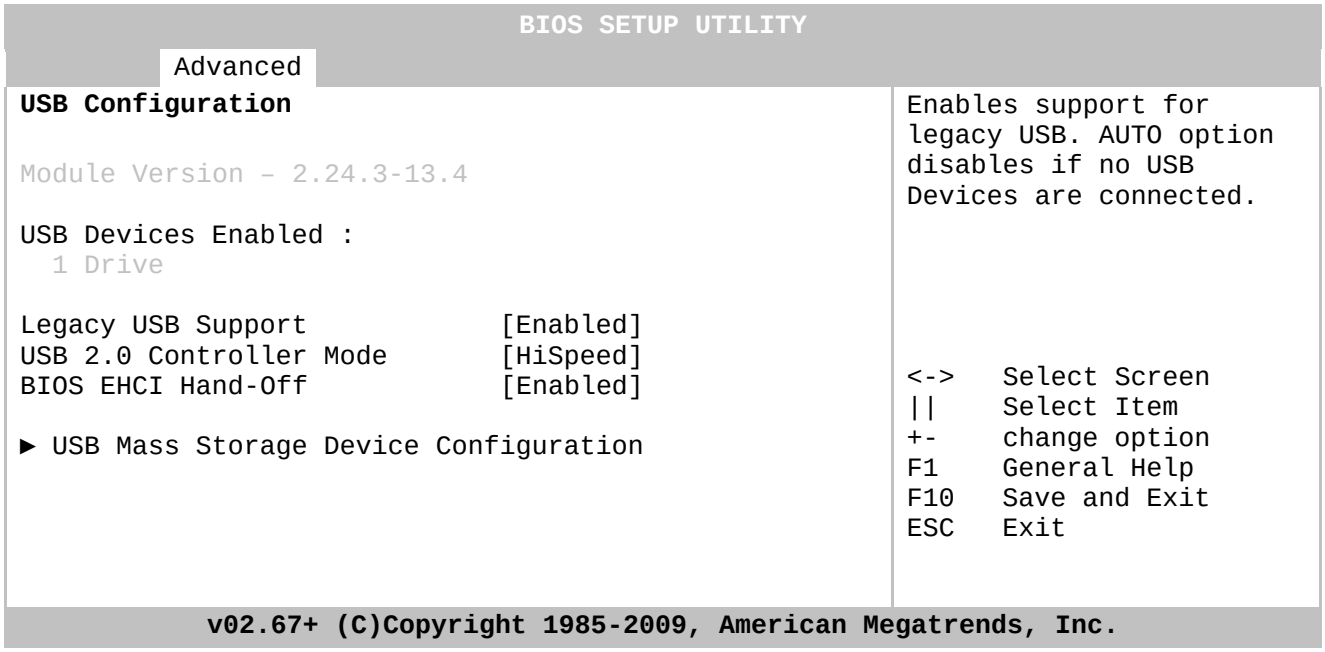
Feature	Options	Description
Remote Access	**Disabled** Enabled	When Enabled then a remote PC can via one of the serial ports behave like a TTY terminal, so that keyboard and monitor (in a terminal window) is emulated by the remote PC. As remote PC terminal program the Windows Hyperterminal can be used.
Serial port number	**COM1** COM2	Setup which comport that should be used for communication
Serial Port Mode	**115200 8 n** 1 57600 8 n 1 38400 8 n 1 19200 8 n 1 9600 8 n 1	Select the serial port speed
Flow Control	**None** Hardware Software	Select Flow Control for serial port
Redirection After BIOS POST	Disabled Boot Loader **Always**	How long shall the BIOS send the picture over the serial port
Terminal Type	**ANSI** VT100 VT-UTF8	Select the target terminal type
VT.UTF8 Combo Key Support	**Enabled** Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Sredir Memory Display Delay	**No Delay** Delay 1 Sec Delay 2 Sec Delay 4 Sec	Gives the delay in seconds to display memory information

7.3.13 Advanced settings – Trusted Computing



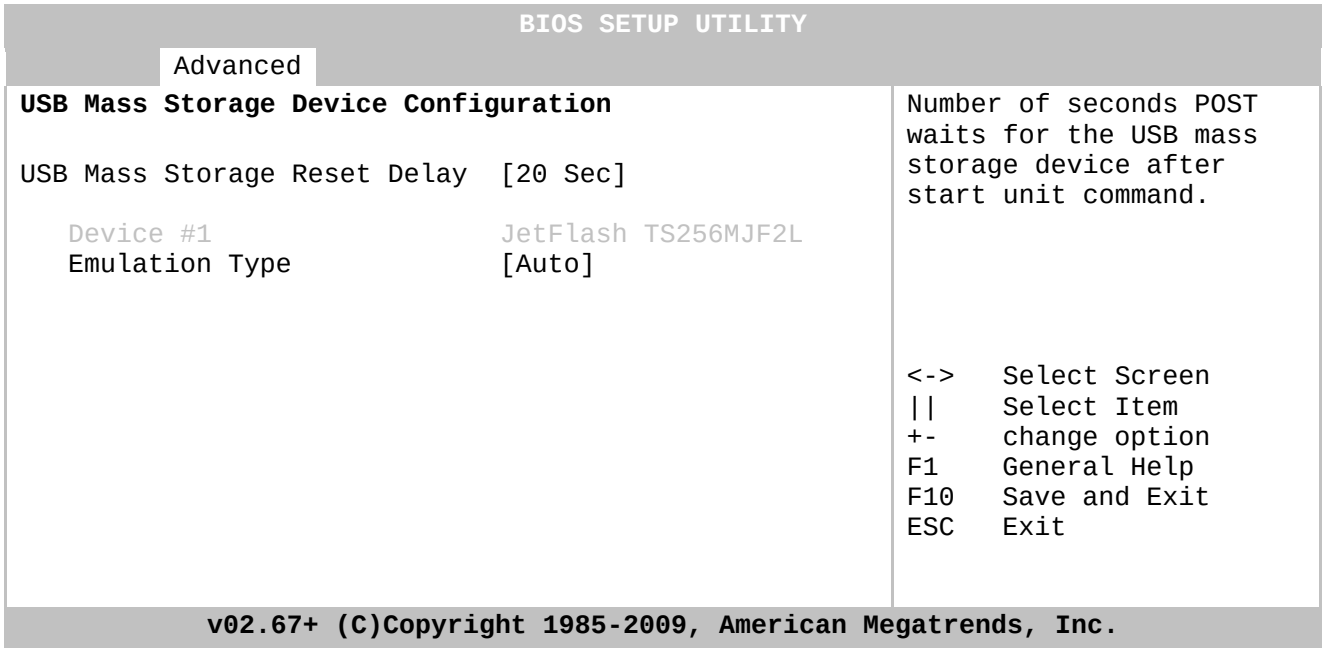
Feature	Options	Description
TCG/TPM Support	**No** Yes	Enables/Disable TPM TCG (TPM 1.1/1.2) Support.

7.3.14 Advanced settings – USB Configuration



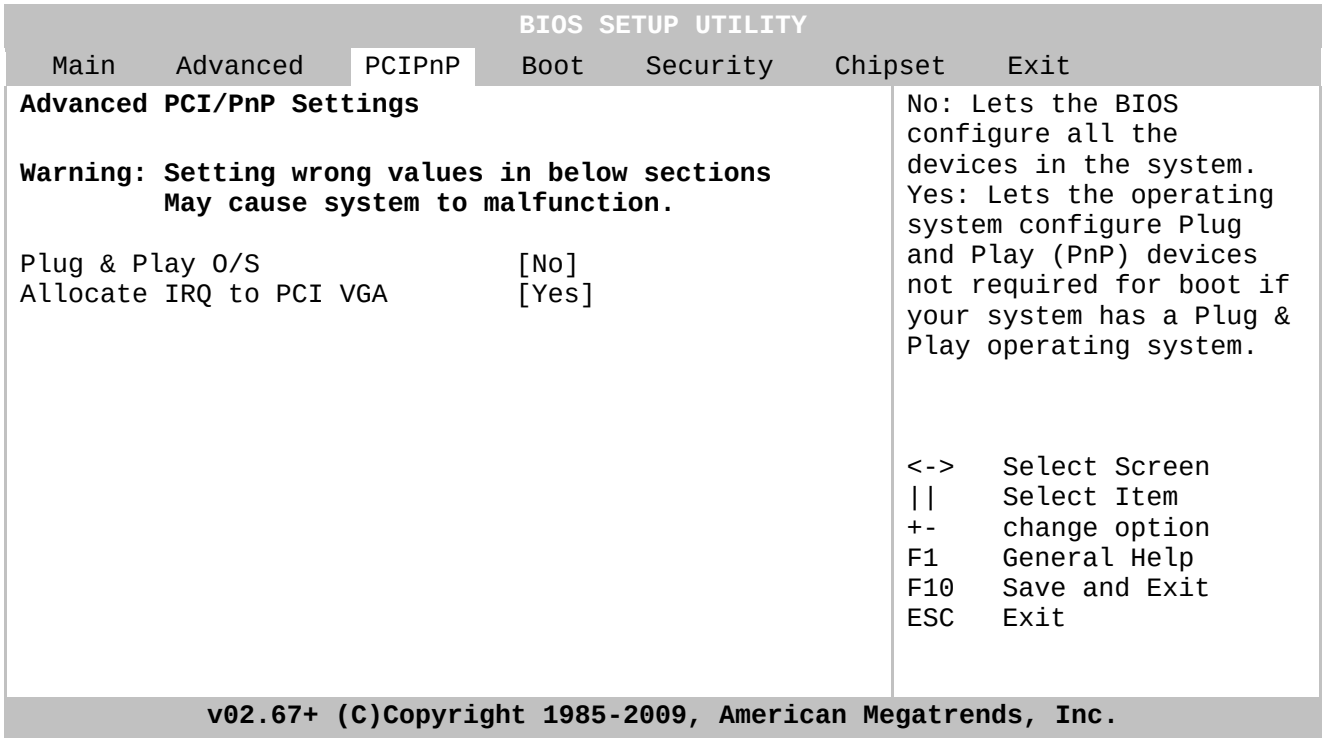
Feature	Options	Description
Legacy USB Support	Disabled **Enabled** Auto	Support for legacy USB Keyboard
USB 2.0 Controller Mode	FullSpeed* **HiSpeed**	Configure the USB 2.0 controller in HiSpeed (480Mbps) or FullSpeed (12Mbps). Note: This feature is not available when Failsafe Defaults are loaded, because USB2.0 controller is disabled as default.
BIOS EHCI Hand-Off	Disabled **Enabled**	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should claim by EHCI driver.

7.3.15 Advanced settings – USB Mass Storage Device Configuration



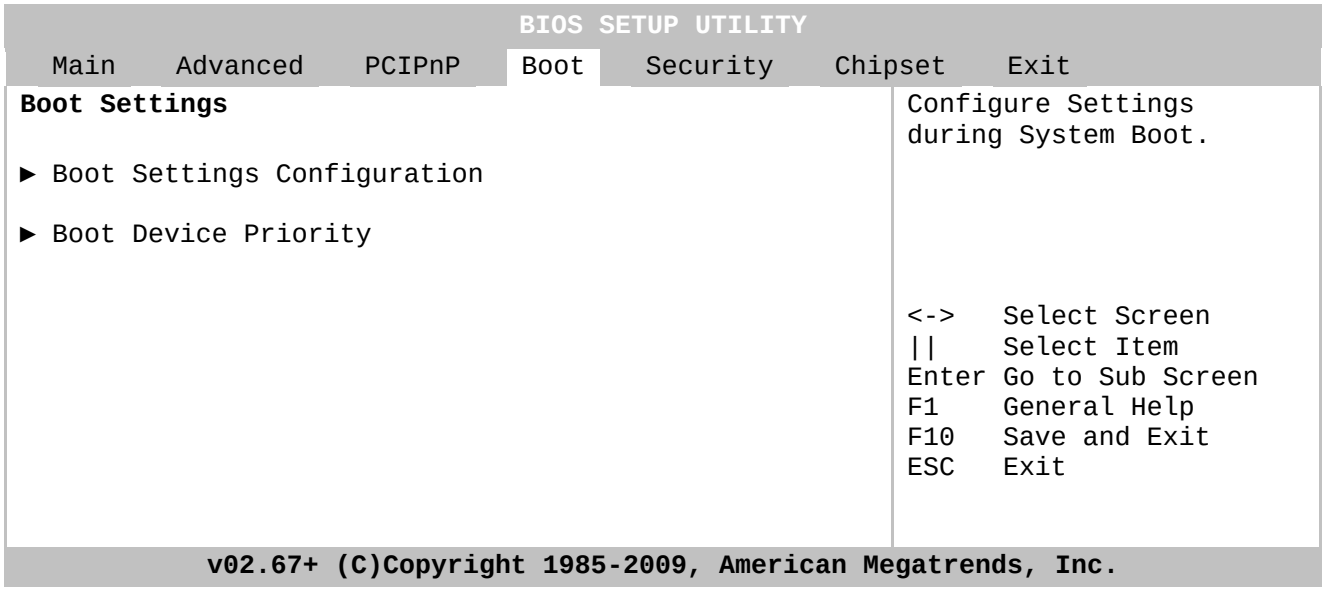
Feature	Options	Description
USB Mass Storage Reset Delay	10 Sec **20 Sec** 30 Sec 40 Sec	Number of seconds POST waits for the USB mass storage device after start unit command.
Emulation Type	**Auto** Floppy Forced FDD Hard Disk CDROM	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).

7.4 PCIpnp Menu

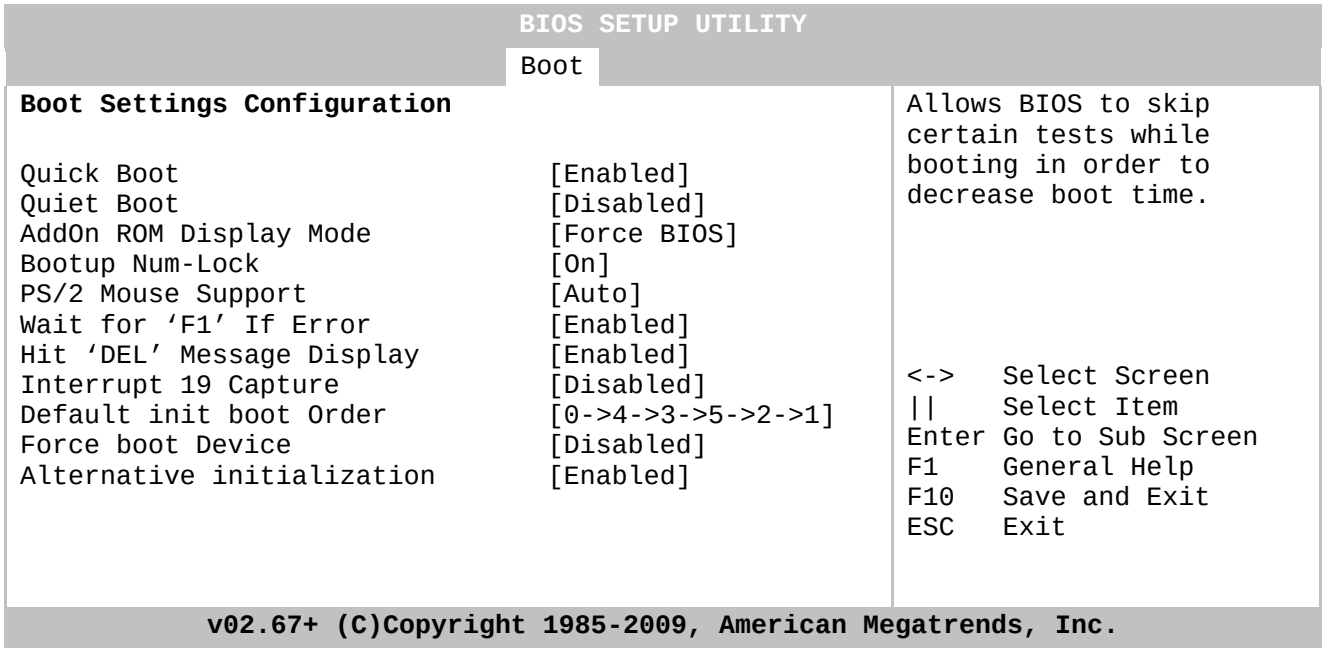


Feature	Options	Description
Plug & Play O/S	**No** Yes	No: Lets the BIOS configure all the devices in the system. Yes: Lets the operating system configure Plug and Play (PnP) devices not required for boot if your system has a Plug & Play operating system.
Allocate IRQ to PCI VGA	**Yes** No	Yes: Assigns IRQ to PCI VGA card if card requests IRQ. No: Does not assign IRQ to PCI VGA card even if card requests an IRQ

7.5 Boot Menu


BIOS SETUP UTILITY
Main Advanced PCIPnP Boot Security Chipset Exit
Boot Settings
▶ Boot Settings Configuration
▶ Boot Device Priority
Configure Settings during System Boot.
<-> Select Screen
|| Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit
v02.67+ (C)Copyright 1985-2009, American Megatrends, Inc.

7.5.1 Boot – Boot Settings Configuration



Feature	Options	Description
Quick Boot	**Enabled** Disabled	Allows BIOS to skip certain tests while booting in order to decrease boot time. When Disabled and right after power up then Memory Test is carried out.
Quiet Boot	**Disabled** Enabled Black Screen White Screen	Disabled: Displays normal POST messages. Enabled: Displays OEM Logo (no POST messages). Black Screen: No picture. White Screen: White picture.
AddOn ROM Display Mode	**Force BIOS** Keep current	Set display mode for Option ROM.
Bootup Num-Lock	Off **On**	Select Power-on state for numlock
PS/2 Mouse Support	Disabled Enabled **Auto**	Select support for PS/2 Mouse.
Wait for 'F1' If Error (see note List of errors)	Disabled **Enabled**	Wait for F1 key to be pressed if error occurs.
Hit 'DEL' Message Display	Disabled **Enabled**	Displays "Press DEL to run Setup" in POST.
Interrupt 19 Capture	**Disabled** Enabled	Enabled: Allows option ROMs to trap interrupt 19
Default init boot Order	**0->4->3->5->2->1** 0->4->3->5->1->2 1->2->3->5->0->4 3->5->1->2->0->4 3->0->4->1->2->5 2->1->0->4->3->5 2->0->4->3->1->5 3->1->0->4->2->5	Control how devices will be placed in the Boot Device Priority Menu: 0 = "Removables" 1 = "Hard disk" 2 = "Atapi cdrom" 3 = "BEV/on-board LAN" (see note) 4 = "USB" 5 = "External LAN"

(Continues)

Feature	Options	Description
Force boot Device	**Disabled** Primary IDE Master Primary IDE Slave Secondary IDE Master Secondary IDE Slave Third IDE Master Third IDE Slave 5th IDE Master 6th IDE Master RAID Any Harddrive (Above) Network	Overrides current boot setting. Device must be in the boot priority menu, though. If the device fails to boot, the system will NOT try other devices.
Boot Fail Option	**Wait Key Press** Retry Again Reboot System	Wait Key Press: Wait for manually activation of key before retrying booting sequence. Retry Again: Automatically and continuously retrying booting sequence. Reboot System: Automatically reboot system.
Alternative initialization	Disabled **Enabled**	Use of this can help some bad devices to work prober.

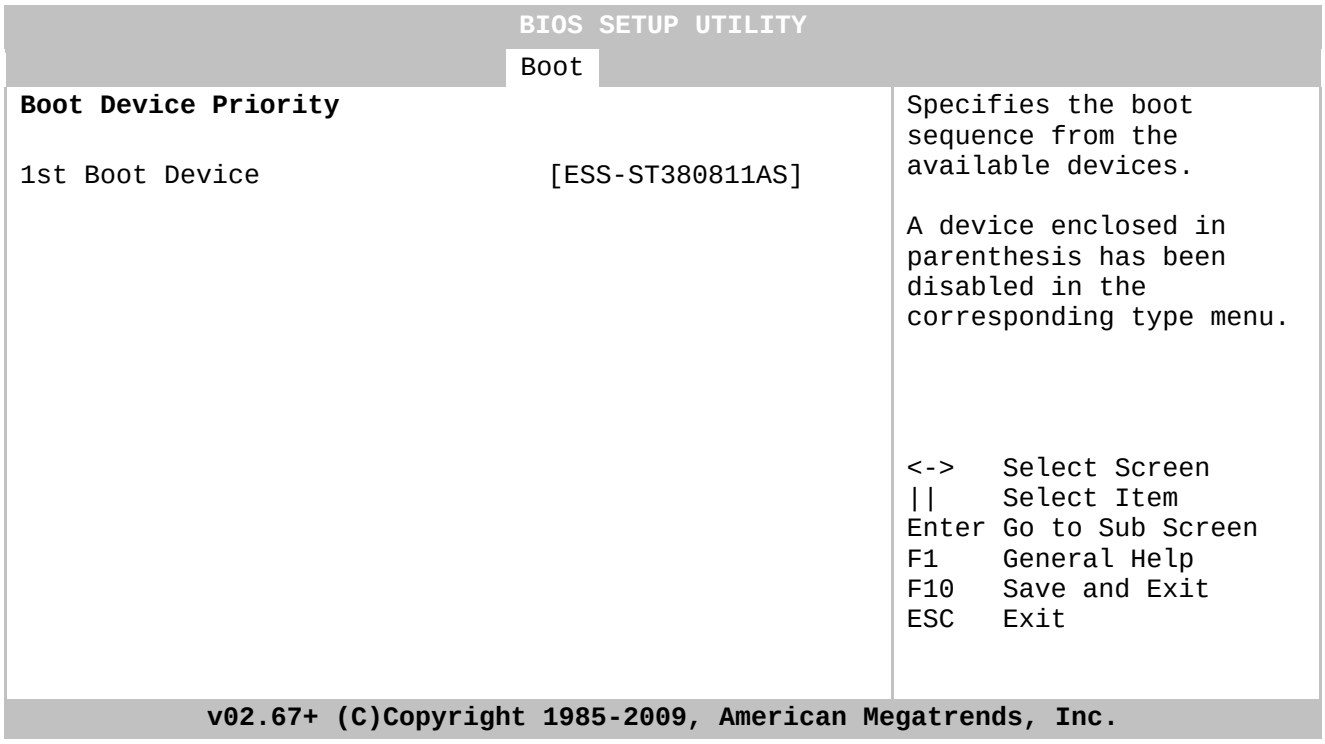
Notes:

List of errors:

<INS> Pressed
Timer Error
Interrupt Controller-1 error
Keyboard/Interface Error
Halt on Invalid Time/Date
NVRAM Bad
Primary Master Hard Disk Error
S.M.A.R.T HDD Error
Cache Memory Error
DMA Controller Error
Resource Conflict
Static Resource Conflict
PCI I/O conflict
PCI ROM conflict
PCI IRQ conflict
PCI IRQ routing table error

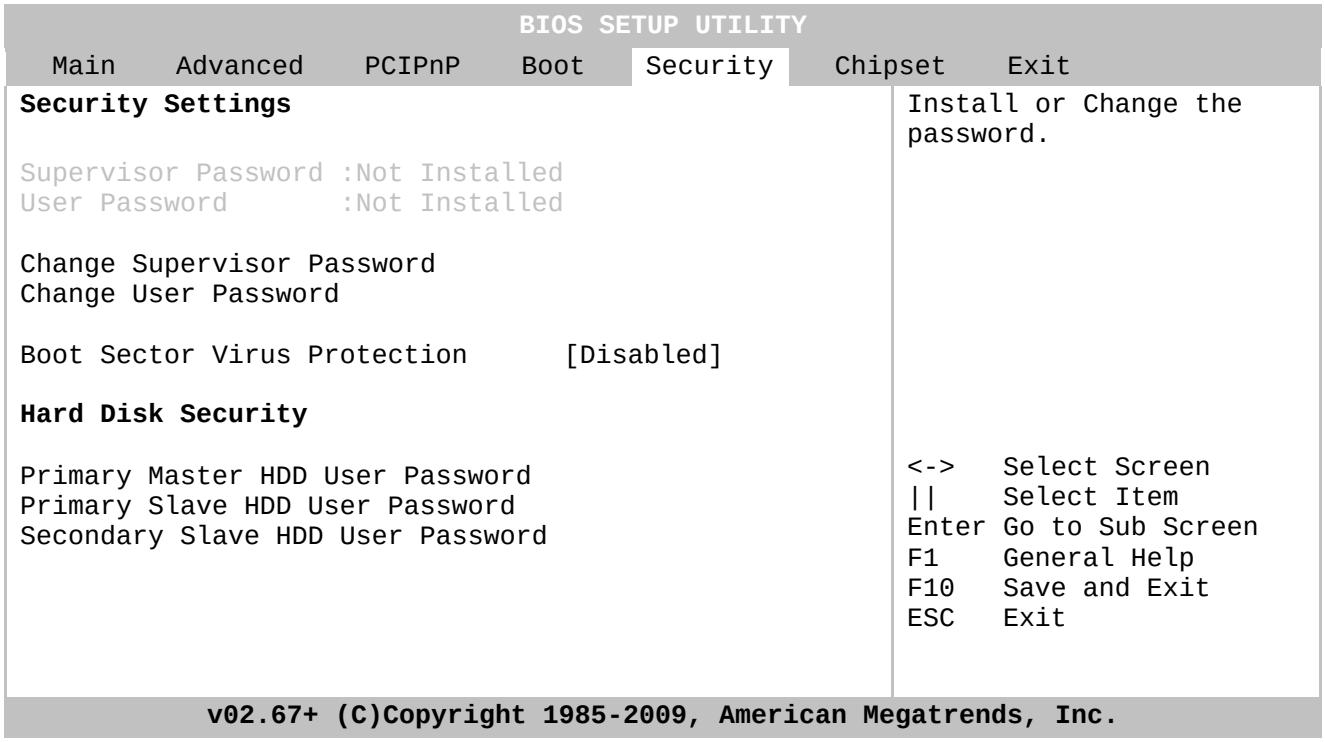
BEV (Bootstrap Entry Vector) list of devices (except External LAN) with bootable ROM. Included is on-board LAN.

7.5.2 Boot – Boot Device Priority



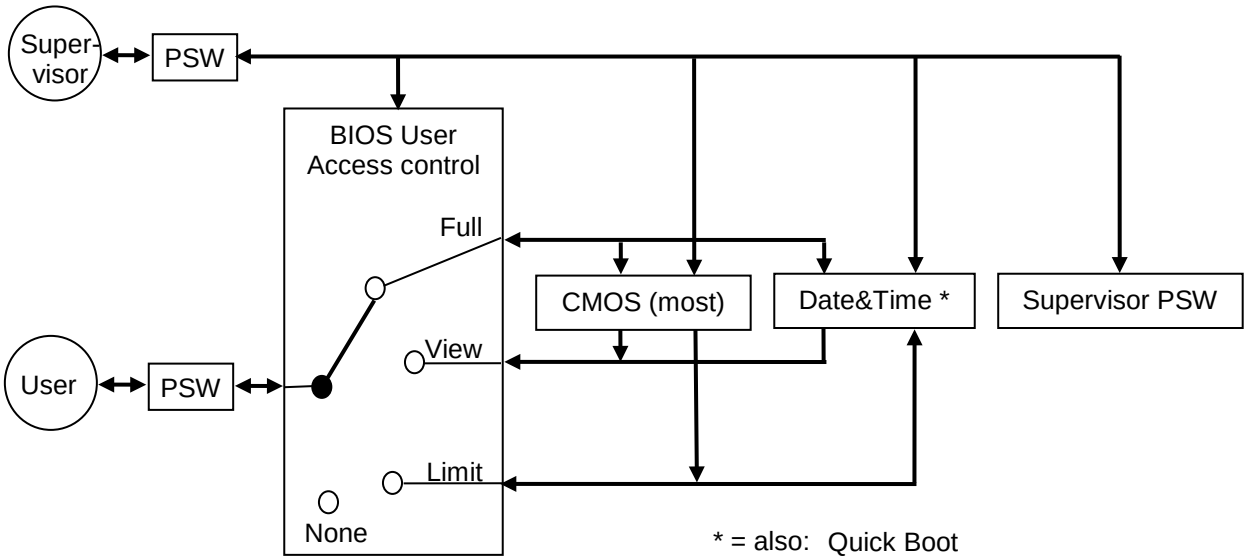
Note: When pressing <F11> while booting it is possible manually to select boot device.

7.6 Security Menu



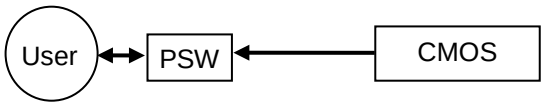
Feature	Options	Description
Change Supervisor Password	Password	When not cleared the advanced Supervisor Password protection system is enabled (see below diagram). Hereafter setting can only be accessed when entering BIOS as Supervisor.
User Access Level	**Full Access** View Only Limited No Access	Only visible if Supervisor Password is installed. Full Access: User can change all BIOS settings. View Only: User can only read BIOS settings. Limited: User can only read settings except: Date & Time, Quick Boot, Quiet Boot, Repost Video on S3 Resume, Active State Power-Management and Remote Access. No Access: User can not enter BIOS, but if Password Check = Always then User password will allow boot.
Change User Password	Password	Change the User Password
Password Check	**Setup** Always	Only visible if Password is installed. Setup: Protects only BIOS settings. Always: Protects both BIOS settings and Boot.
Boot Sector Virus Protection	Enabled **Disabled**	Will write protect the MBR when the BIOS is used to access the harddrive
HDD Password	Password	Locks the HDD with a password, the user needs to type the password on power on

Supervisor Password protection (setup Supervisor before User)

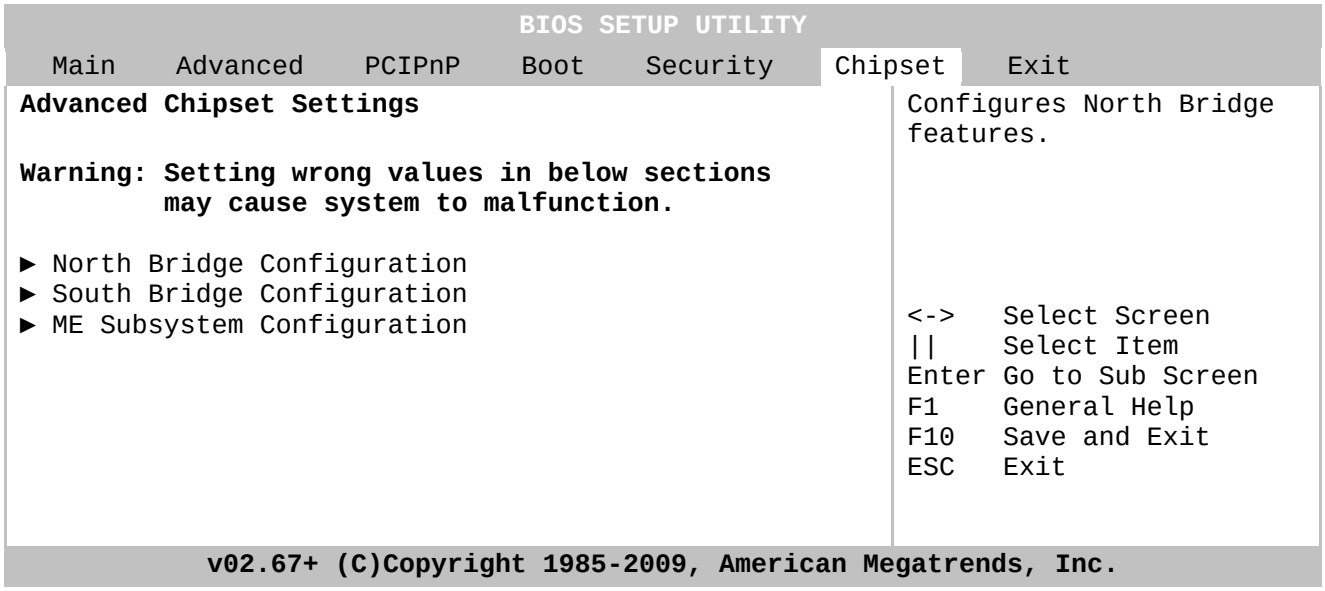


* = also: Quick Boot
Quiet Boot
Repost Video on S3 Resume
Active State Power-Management

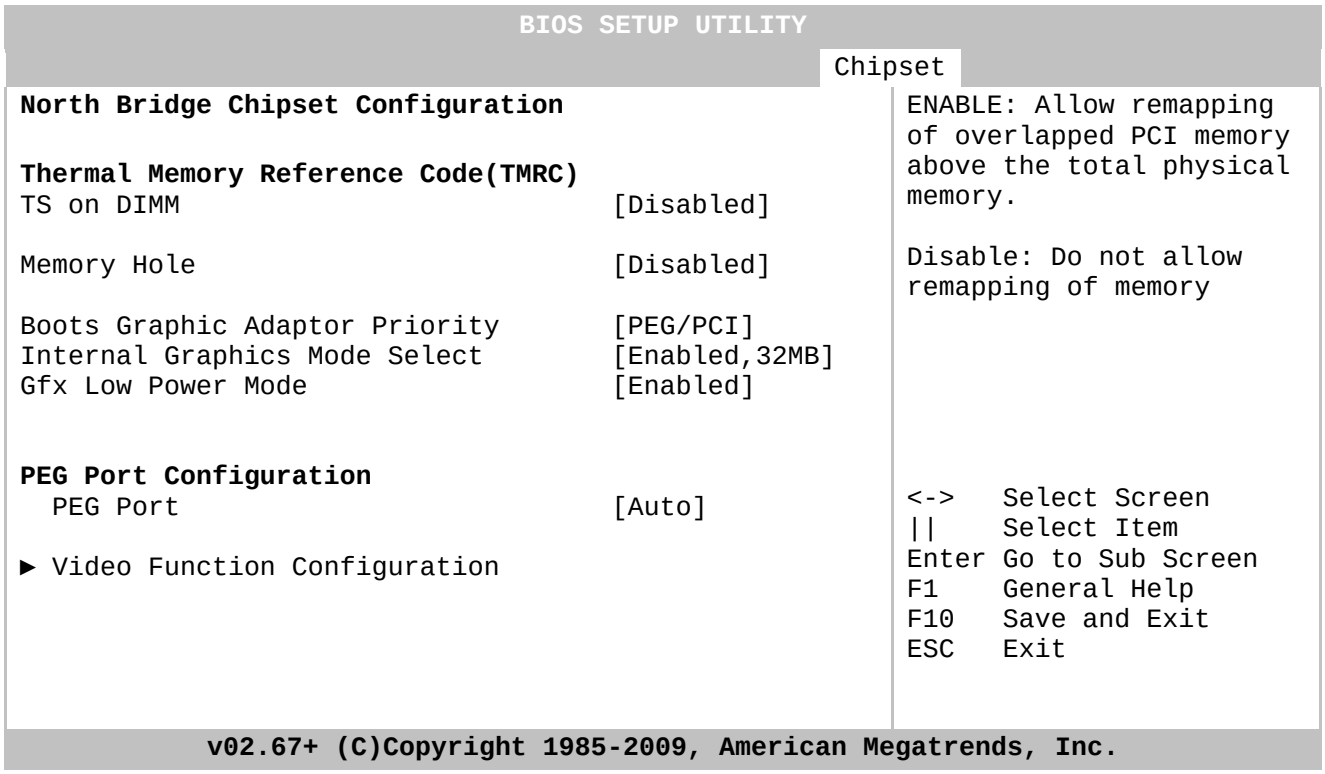
User Password protection only (no Supervisor Password used)



7.7 Chipset Menu



7.7.1 Advanced Chipset Settings – North Bridge Chipset Configuration

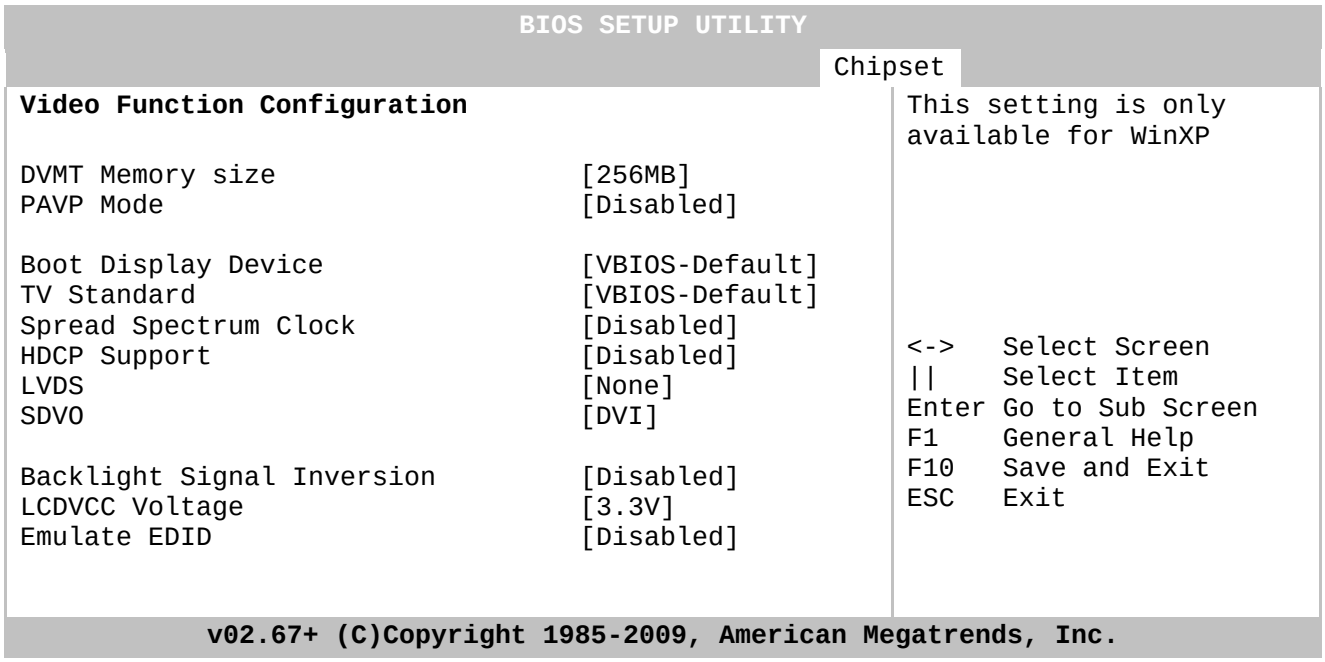


Feature	Options	Description
TS on DIMM	**Disabled** Enabled	Enable/Disable Thermal Sensor on DIMM.
Memory Hole	**Disabled** 15MB-16MB	Disabled 15MB-16MB
Boots Graphic Adaptor Priority	IGD PCI/IGD PCI/PEG PEG/IGD **PEG/PCI**	Select which graphics controller to use as the primary boot device.
Internal Graphics Mode Select	Disabled **Enabled, 32MB** Enabled, 64MB Enabled, 128MB	Select the amount of system memory used by the Integrated Graphic Device.
Gfx Low Power Mode	Disabled **Enabled**	This option is applicable for SFF only.
PEG Port	**Auto** Disabled Enable PEG Always	Auto Disabled Enable PEG Always

Notes: Memory Remap Feature should be Enabled when using 64bit OS and has effect if using more than 4GB of memory. If using 32bit OS and more than 3GB (max 4GB) then up to ½ GB might be lost if Memory Remap Feature is Enabled, so in general it is recommended to Disable the Memory Remap Feature when 32 bit OS is used.

Using PCIe Graphics card in combination with on-board graphics (VGA or LVDS) is possible if BIOS (from version KTGM4506) setting *Boots Graphic Adaptor Priority = IGD*. In this case on-board graphic will be Primary desktop and PCIe Graphics will be extended desktop. Note that PCIe Graphics driver shall be installed before the Intel Graphics driver.

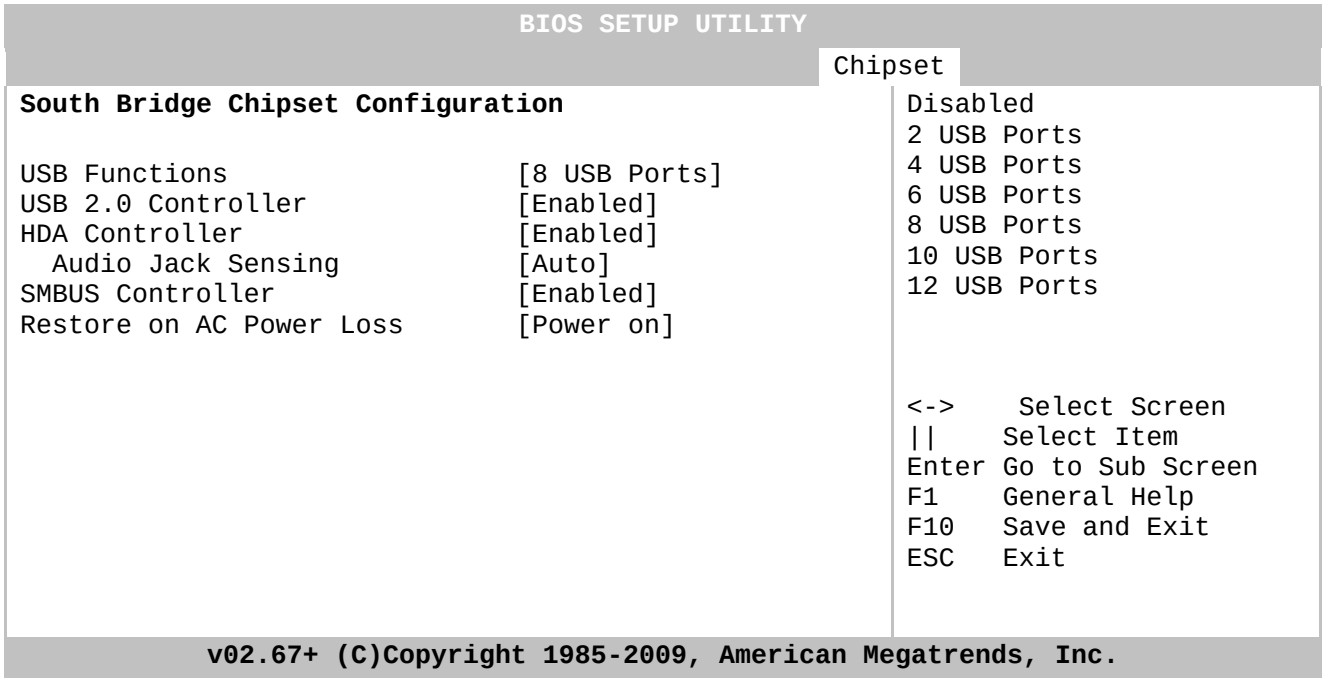
7.7.2 Advanced Chipset … – North Br. … – Video Function Configuration



Feature	Options	Description
DVMT Memory size	128MB **256MB** Maximum DVMT	This setting is only available for WinXP
PAVP Mode	**Disabled** Lite High	GMCH Protected Audio Video Path (PAVP) BIOS support.
Boot Display Device (see note)	**VBIOS-Default** CRT TV CRT+TV SDVO CRT+SDVO LVDS CRT+LVDS	Options VBIOS-Default CRT TV CRT+TV SDVO CRT+SDVO LVDS CRT+LVDS
TV Standard	**VBIOS-Default** NTSC PAL SECAM SMPTE240M ITU-R television SMPTE295M SMPTE296M EIA-770.2 EIA-770.3	Options VBIOS-Default NTSC PAL SECAM SMPTE240M ITU-R television SMPTE295M SMPTE296M EIA-770.2 EIA-770.3
Spread Spectrum	**Disabled** Enabled	Options Disabled Enabled
HDCP Support	**Disabled** Enabled	HDCP provisioning BIOS
LVDS	(see description ->)	Select Resolution, Manufacturer and Type no. for the actual LVDS display.
SDVO	DVI / LVDS / N/A	Display module V0.0
Backlight Signal Inversion	**Disabled** Enabled	Select Signal polarity
LVDVCC Voltage	**3.3V** 5V	Options 3.3V 5V
Emulate EDID	**Disabled** Enabled	Options Disabled Enabled

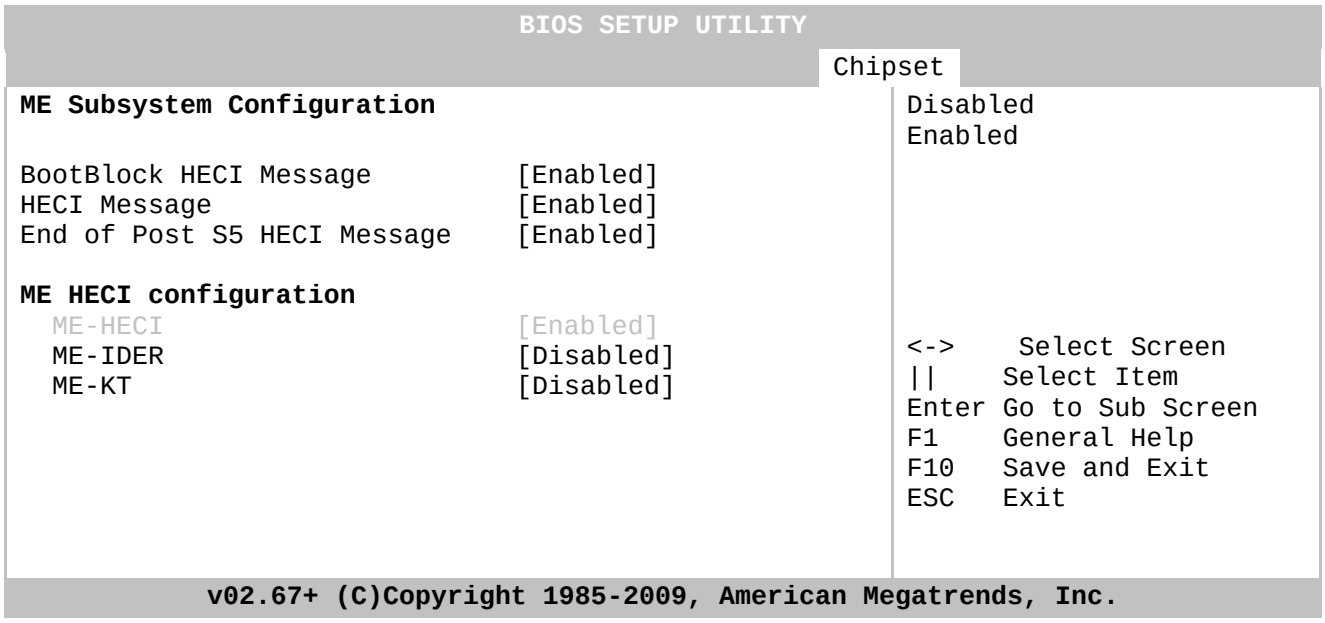
Note: When using ADD2-LVDS card then it is recommended using “LVDS” setting. In case of using ADD2-LVDS-Single alternatively use “VBIOS Defaults” setting. The “CRT+LVDS” setting is for on-board LVDS and do not compare with ADD2-LVDS card. The second LVDS port will only be available from OS.

7.7.3 Advanced Chipset Settings – South Bridge Chipset Configuration



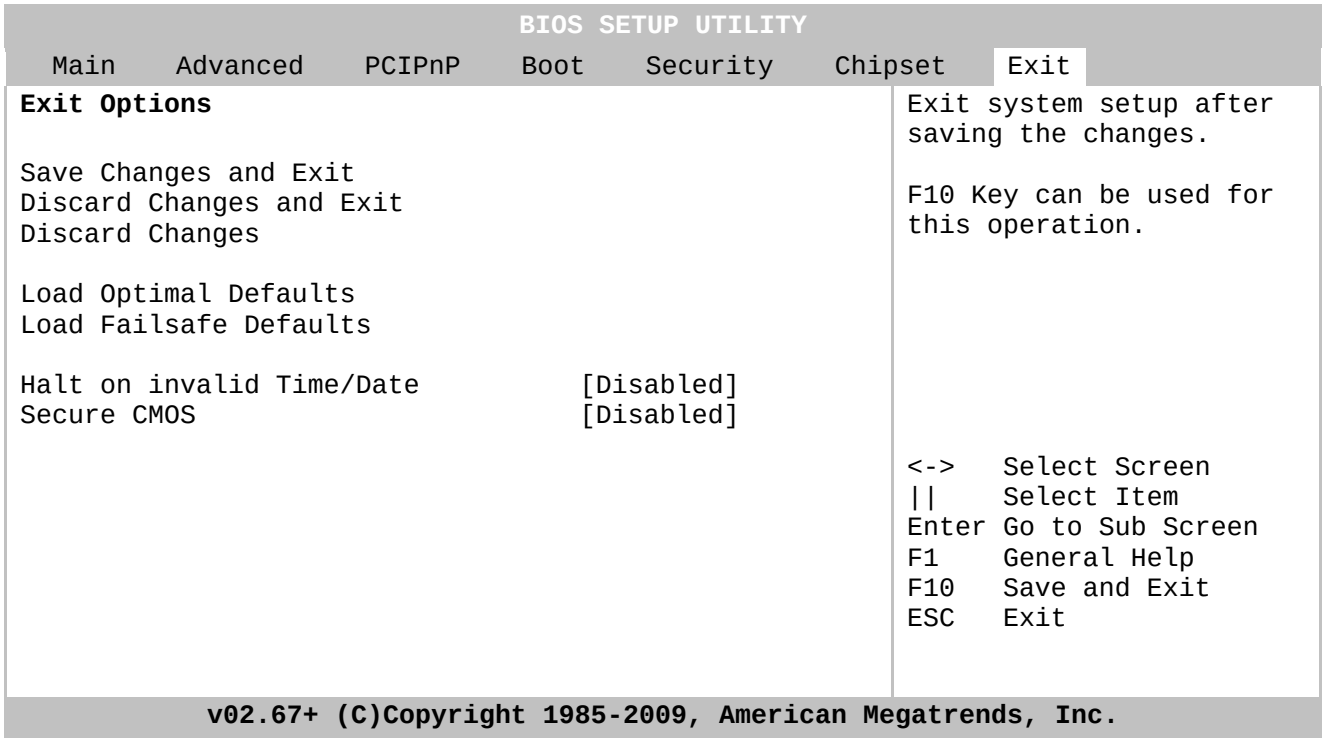
Feature	Options	Description
USB Functions	Disabled 2 USB Ports 4 USB Ports 6 USB Ports 8 USB Ports 10 USB Ports **12 USB Ports**	Disabled 2 USB Ports 4 USB Ports 6 USB Ports 8 USB Ports 10 USB Ports 12 USB Ports
USB 2.0 Controller	Disabled **Enabled**	If above function “USB Function” = 10 or 12 USB Ports then USB 2.0 Controller is always enabled
HDA Controller	Disabled **Enabled**	Disabled Enabled
Audio Jack Sensing	**Auto** Disabled	Auto: The insertion of audio jacks is auto determined. Disabled: Driver assumes that all jacks are inserted (useful when using Audio pinrow)
SMBUS Controller	**Enabled** Disabled	Disabled Enabled
Restore on AC Power Loss	Power Off **Power On** Last State	Power Off Power On Last State

7.7.4 Advanced Chipset Settings – ME Subsystem Configuration



Feature	Options	Description
BootBlock HECI Message	Disabled **Enabled**	Options Disabled Enabled
HECI Message	Disabled **Enabled**	Options Disabled Enabled
End of Post S5 HECI Message	Disabled **Enabled**	Options Disabled Enabled
ME HECI	Disabled **Enabled**	Options Disabled Enabled
ME-IDER	**Disabled** Enabled	Options Disabled Enabled
ME-KT	**Disabled** Enabled	Options Disabled Enabled

7.8 Exit Menu



Feature	Options	Description
Save Changes and Exit	Ok Cancel	Exit system setup after saving the changes
Discard Changes and Exit	Ok Cancel	Exit system setup without saving any changes
Discard Changes	Ok Cancel	Discards changes done so far to any of the setup questions
Load Optimal Defaults	Ok Cancel	Load Optimal Default values for all the setup questions
Load Failsafe Defaults	Ok Cancel	Load Failsafe Default values for all the setup questions
Halt on invalid Time/Date	Enabled **Disabled**	Enabled: System halt if incorrect Date & Time.
Secure CMOS	Enabled **Disabled**	Enable will store current CMOS in non-volatile ram. (For protection of CMOS data in case of battery failure etc.)

8 AMI BIOS Beep Codes

Boot Block Beep Codes:

Number of Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
3	Base Memory error
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

POST BIOS Beep Codes:

Number of Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
3	Base memory read/write test error
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

Troubleshooting POST BIOS Beep Codes:

Number of Beeps	Troubleshooting Action
1, 2 or 3	Reset the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond "all hope", eliminate the possibility of interference due to a malfunctioning add-in card. Remove all expansion cards, except the video adapter. • If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. • If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem happens again. This will reveal the malfunctioning card.
8	If the system video adapter is an add-in card, replace or reset the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

9 OS Setup

Use the Setup.exe files for all relevant drivers. The drivers can be found on KTGM45 Driver CD or they can be downloaded from the homepage http://www.kontron.com/

Please note that if Management Engine Driver is not installed then Windows Device Manager will show yellow exclamation mark on the PCI Communication Controller.