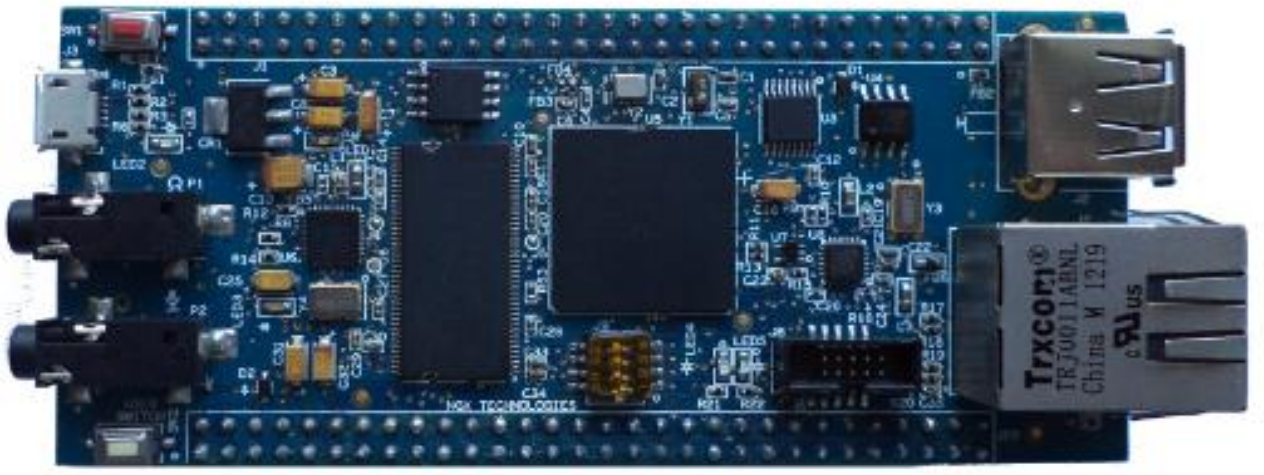
参考資料

LPC185x-Xplorer++



User Manuals for LPC185x-Xplorer++:
For KEIL MDK-ARM with ULINK2/ME: Click here

Sample projects for LPC185x-Xplorer++:
For KEIL MDK-ARM: Click here

USB Virtual Com INF file:
Click here to download USB Virtual Com INF file.

About NGX Technologies

NGX Technologies is a premier supplier of development tools for the ARM7, ARM Cortex M0, M3 and M4 series of microcontrollers. NGX provides innovative and cost effective design solutions for embedded systems. We specialize in ARM MCU portfolio, which includes ARM7, Cortex-M0, M3 & M4 microcontrollers. Our experience with developing evaluation platforms for NXP controller enables us to provide solutions with shortened development time thereby ensuring reduced time to market and lower development costs for our customers. Our cost effective and feature rich development tool offering, serves as a testimony for our expertise, cost effectiveness and quality.

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CE certification:

NGX Technologies LPC185X-Xplorer++ board has been tested for radiated emission as per EN55022 class A standard. The device is under the limits of the standard EN55022 class A and hence CE marked. No other test have been conducted other than the radiated emission (EN55022 class A standard). The device was tested with the ports like USB, Serial, and Power excluding the GPIO ports. Any external connection made to the GPIO ports may alter the EMC behavior. Usage of this device under domestic environment may cause unwanted interference with other electronic equipment's. User is expected to take adequate measures. The device is not intended to be used in and end product or any subsystem unless the user re-evaluates applicable directive/conformance.

Table of Contents

1.0 INTRODUCTION

This document is a 'Quick Start Guide' for LPC185X-Xplorer++; a cost effective evaluation platform for NXP's LPC185x MCU. This document focuses on the kit contents, board verification, possible debuggers and IDEs that can be used.

1.1 Possible Debuggers and IDEs that can be used

- **ULINK2 with KEIL uVision**
- **NXP LPCLink with LPCXpresso**
- **Red Probe+ with Red Suite from Code Red**
- **I-jet with IAR Embedded Workbench**
- **Segger JLink with IAR Embedded Workbench or KEIL uVision**

The LPC185x-Xplorer++ is packaged as shown in the following image.

TBD

Fig. 1

After unboxing the package you should find LPC185X-Xplorer++ Board, 'USB AM to Micro B' cable as shown in the following image.

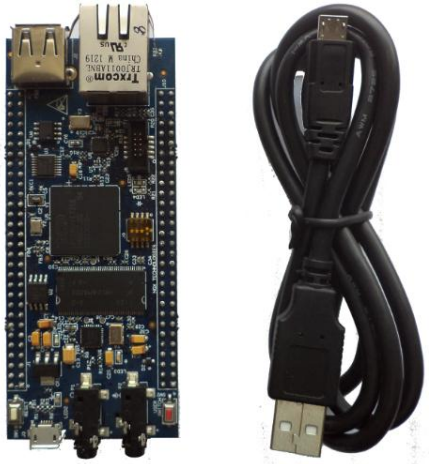


Fig. 2

1.2 ARM JTAG (20-pin) to Cortex JTAG (10-pin) Adapter

Please note that your existing debugger might be supporting only the '20-pin ARM JTAG connector'. In such scenarios one would require a '20-pin to 10-pin adaptor' and the necessary cables. The LPC185X-Xplorer++ has on board 'Cortex SWD/JTAG 10-pin male connector', the '20-pin to 10-pin adaptor' is not a part of the LPC185X-Xplorer++ package and user needs to buy them separately.

If the debugger supports the '10-pin Cortex header' one needs to have the 10-pin ribbon cable and can directly connect to the LPC185X-Xplorer++. Please note even the 10-pin ribbon cable is not a part of standard delivery and needs to be procured separately.

The picture below shows 20-pin ribbon cable, 10-pin ribbon cable and '20-pin to 10-pin adaptor'.

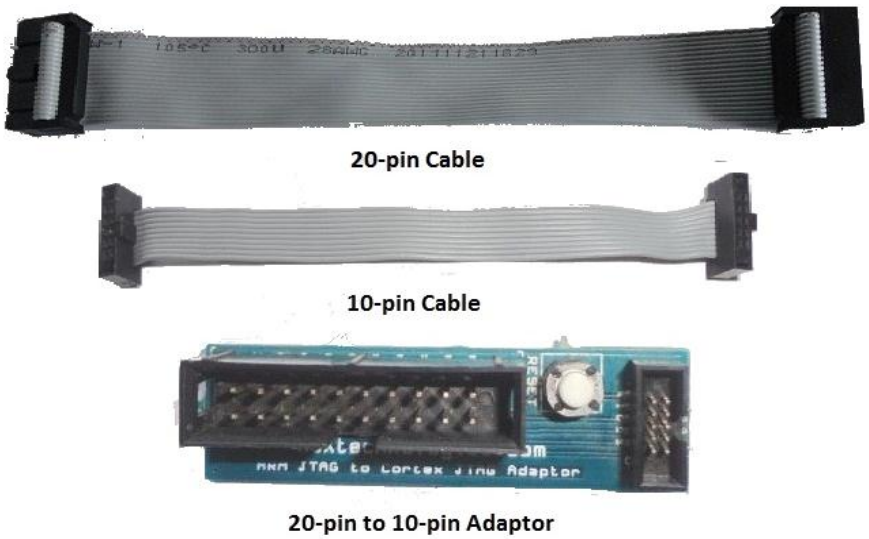


Fig. 3

1.3 ULINK-ME and KEIL

Connect one end of 10-pin ribbon cable ‘ULINK-ME 10-pin box header’ and other end to LPC185X-Xplorer++ as shown in the below image. The hardware setup is now ready for programing an LPC185X-Xplorer++ board with ULINK-ME and KEIL IDE. Please refer keil knowledgebase article for connecting ‘ULINK-ME 10-pin ribbon cable’ to NGX Xplorer++.

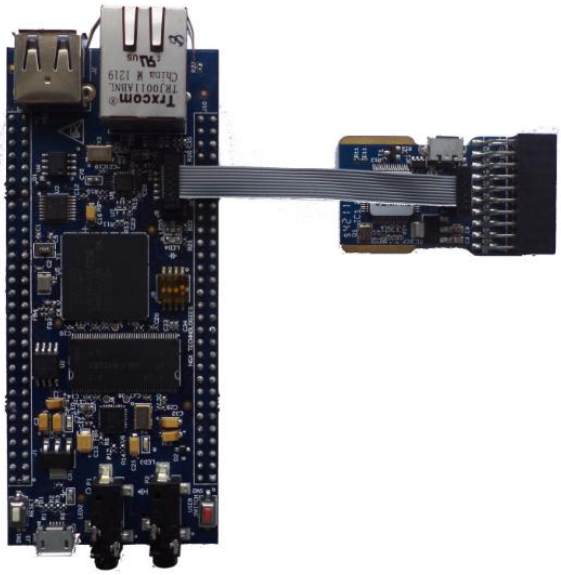


Fig. 4

1.4 ULINK2 and KEIL

Connect ‘ULINK2 20-pin cable’ to ‘20-pin to 10-pin adaptor’ and connect one end of 10-pin ribbon cable to ‘20-pin to 10-pin adaptor’ and other end to LPC185X-Xplorer++ as shown in the below image. The hardware setup is now ready for programing an LPC185X-Xplorer++ board with ULINK2 and KEIL IDE. Please refer keil knowledgebase article for connecting ULINK2 to NGX Xplorer++.

Fig. 5

2.0 LPC185X-Xplorer++ Overview

2.1 Introduction

The NGX LPC185X-Xplorer++ is a compact and versatile evaluation platform for the NXP's Cortex-M3 based MCUS. NGX's evaluation platforms are generally not tied up to any particular debugger or compiler/IDE. However it is not practical to test and ensure that the solution would work out of box with all the available debuggers and compilers/IDE. As long as the compiler supports the particular MCU and the debugger supports the standard debug interfaces like the SWD/JTAG you can use this platform with any tool. The board is supported by extensive sample examples allowing you to focus on the application development.

2.2 Board Features

Following are the salient features of the board

- Dimensions: 102mm x 43mm
- Controller: LPC185X, 256 pin BGA
- PCB: 6-layer (RoHS complaint)
- Two LEDs
- One user switch and one reset switch
- Boot select switch
- 32Mb Quad flash
- 32MB SDRAM
- On board crystals for controller, RTC and audio codec
- On board Ethernet PHY, 25 MHz Crystal and RJ45 connector with magnetics
- On board audio codec and audio jacks
- On board USB host port
- On board RS232 level
- On board USB port
- 10-pin cortex debug header
- Unused I/Os brought to a header.

2.3 BLOCK DIAGRAM

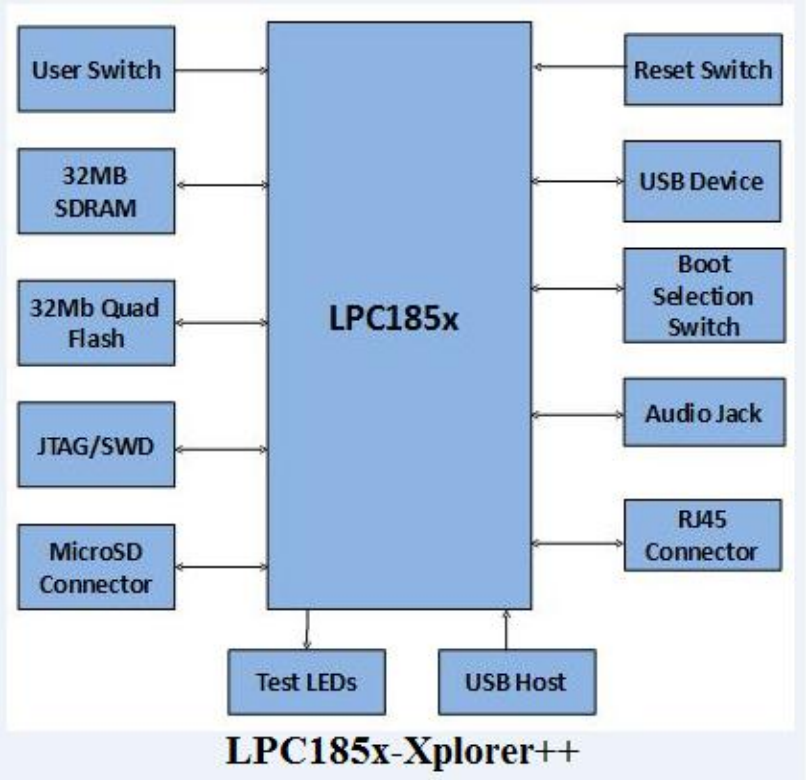


Fig. 6

2.4 LPC185X-Xplorer++pin out

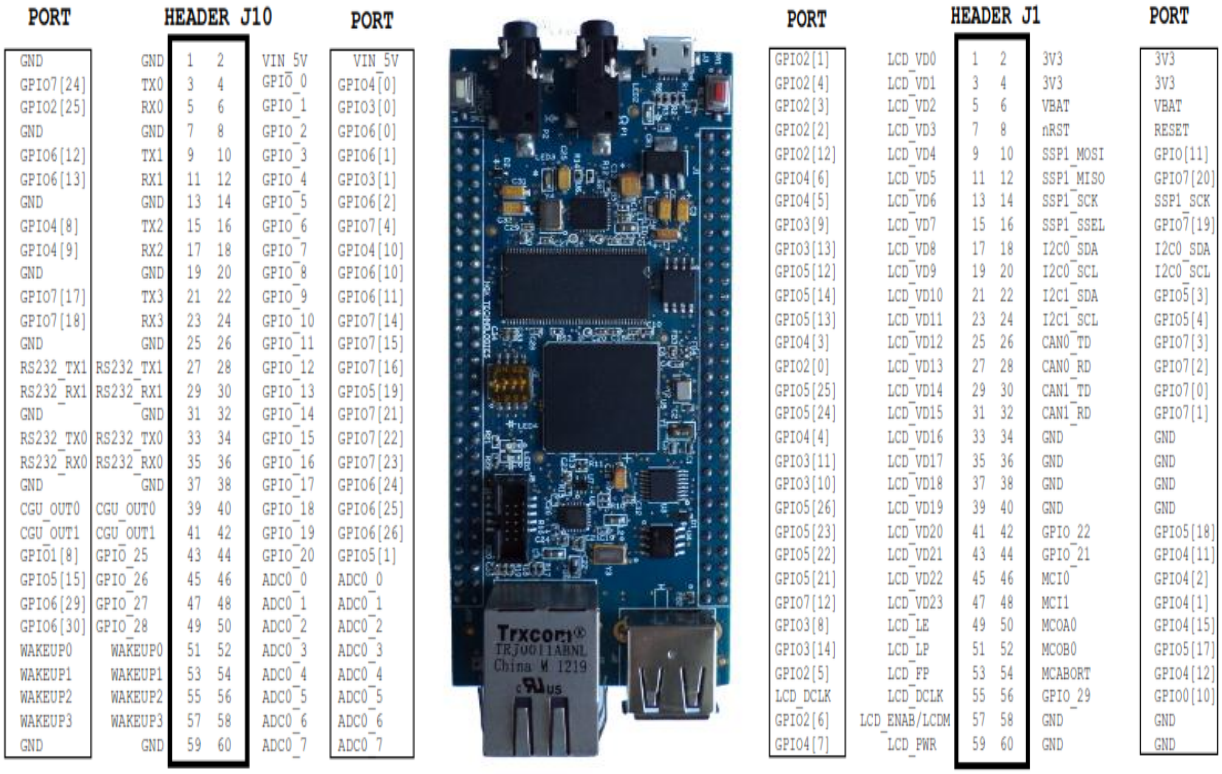


Fig.7

2.5 LPC185X description

The LPC185X is a high-performance, cost-effective Cortex-M3 microcontroller featuring up to 1 MB of flash and 136 kB of on-chip SRAM, 16 kB of EEPROM memory, a quad SPI Flash Interface (SPIFI), a State Configurable Timer (SCT)subsystem, two High-speed USB controllers, Ethernet, LCD, an external memory controller, and multiple digital and analog peripherals.

Processor core

- ARM Cortex-M3 processor, running at CPU frequencies of up to 180 MHz
- ARM Cortex-M3 built-in Memory Protection Unit (MPU) supporting eight regions.
- ARM Cortex-M3 built-in Nested Vectored Interrupt Controller (NVIC).
- Non-maskable Interrupt (NMI) input.
- JTAG and Serial Wire Debug, serial trace, eight breakpoints, and four watch points.
- Enhanced Trace Module (ETM) and Enhanced Trace Buffer (ETB) support.
- System tick timer.

On-chip memory

- Up to 1 MB on-chip dual bank flash memory with flash accelerator.
- 16 kB on-chip EEPROM data memory.
- 136 kB SRAM for code and data use.
- Multiple SRAM blocks with separate bus access.
- 64 kB ROM containing boot code and on-chip software drivers.
- 32-bit One-Time Programmable (OTP) memory for general-purpose use.

Clock generation unit

- Crystal oscillator with an operating range of 1 MHz to 25 MHz.
- 12 MHz internal RC oscillator trimmed to 1 % accuracy over temperature and voltage.
- Ultra-low power RTC crystal oscillator.
- Three PLLs allow CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. The second PLL is dedicated to the High-speed USB; the third PLL can be used as audio PLL.
- Clock output.

Configurable digital peripherals:

- State Configurable Timer (SCT) subsystem on AHB.
- Global Input Multiplexer Array (GIMA) allows to cross-connect multiple inputs and outputs to event driven peripherals like timers, SCT, and ADC0/1.

Serial interfaces:

- Quad SPI Flash Interface (SPIFI) with 1-, 2-, or 4-bit data at rates of up to 60 MB per second.
- 10/100T Ethernet MAC with RMII and MII interfaces and DMA support for high throughput at low CPU load. Support for IEEE 1588 time stamping/advanced time stamping (IEEE 1588-2008 v2).
- One High-speed USB 2.0 Host/Device/OTG interface with DMA support and on-chip high-speed PHY (USB0).
- One High-speed USB 2.0 Host/Device interface with DMA support, on-chip full-speed PHY and ULPI interface to an external high-speed PHY (USB1).
- USB interface electrical test software included in ROM USB stack.
- Four 550 UARTs with DMA support: one UART with full modem interface; one
- UART with IrDA interface; three USARTs support UART synchronous mode and a
- Smart card interface conforming to ISO7816 specification.
- Two C_CAN 2.0B controllers with one channel each.
- Two SSP controllers with FIFO and multi-protocol support. Both SSPs with DMA support.

- One Fast-mode Plus I2C-bus interface with monitor mode and with open-drain I/Opins conforming to the full I2C-bus specification. Supports data rates of up to1Mbit/s.
- One standard I2C-bus interface with monitor mode and standard I/O pins.
- Two I2S interfaces with DMA support, each with one input and one output.

Digital peripherals:

- External Memory Controller (EMC) supporting external SRAM, ROM, NOR flash, and SDRAM devices.
- LCD controller with DMA support and a programmable display resolution of up to1024Hx 768V. Supports monochrome and color STN panels and TFT color panels; supports 1/2/4/8 bpp Color Look-Up Table (CLUT) and 16/24-bit direct pixel mapping.
- SD/MMC card interface.
- Eight-channel General-Purpose DMA (GPDMA) controller can access all memories on the AHB and all DMA-capable AHB slaves.
- Up to 164 General-Purpose Input/Output (GPIO) pins with configurable pull-up/pull-down resistors.
- GPIO registers are located on the AHB for fast access. GPIO ports have DMA support.
- Up to 8 GPIO pins can be selected from all GPIO pins as edge and level sensitive interrupt sources.
- Two GPIO group interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
- Four general-purpose timer/counters with capture and match capabilities.
- One motor control PWM for three-phase motor control.
- One Quadrature Encoder Interface (QEI).
- Repetitive Interrupt timer (RI timer).
- Windowed watchdog timer.
- Ultra-low power Real-Time Clock (RTC) on separate power domain with 256 bytes of battery powered backup registers.
- Event recorder with three inputs to record event identification and event time; can be battery powered.
- Alarm timer; can be battery powered.

Analog peripherals:

- One 10-bit DAC with DMA support and a data conversion rate of 400kSamples/s.
- Two 10-bit ADCs with DMA support and a data conversion rate of 400kSamples/s.
- Up to eight input channels per ADC. Unique ID for each device.

Power:

- Single 3.3 V (2.2 V to 3.6 V) power supply with on-chip internal voltage regulator for the core supply and the RTC power domain.
- RTC power domain can be powered separately by a 3 V battery supply.
- Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
- Processor wake-up from Sleep mode via wake-up interrupts from various peripherals.
- Wake-up from Deep-sleep, Power-down, and Deep power-down modes via external interrupts and interrupts generated by battery powered blocks in the RTC power domain.
- Brownout detect with four separate thresholds for interrupt and forced reset.
- Power-On Reset (POR).

Note: LPC1850 do not have on-chip flash memory.

For the most updated information on the MCU please refer to NXP's website.

3.0 LPC185X-Xplorer++ verification

NGX's evaluation platforms ship with a factory-programmed test firmware that verifies all the on-board peripherals. It is highly recommended that you verify the board, before you start programming. Also this exercise helps you get acclimatized with the board quickly.

To run the tests you will need the following:

- LPC185X-Xplorer++
- Power: USB cable or external power supply (Alternatively the LPC185x-Xplorer++ has a 5V in pin available for powering through external power source)
- PC: With Windows7 or XP (32-bit or 64-bit)
- One USB AM to Micro B cable
- Micro SD card
- 2-GB USB pen drive
- Audio-out (Auxiliary) cable (3.5mm diameter connector)

3.1 Board Image with pointers to the peripherals

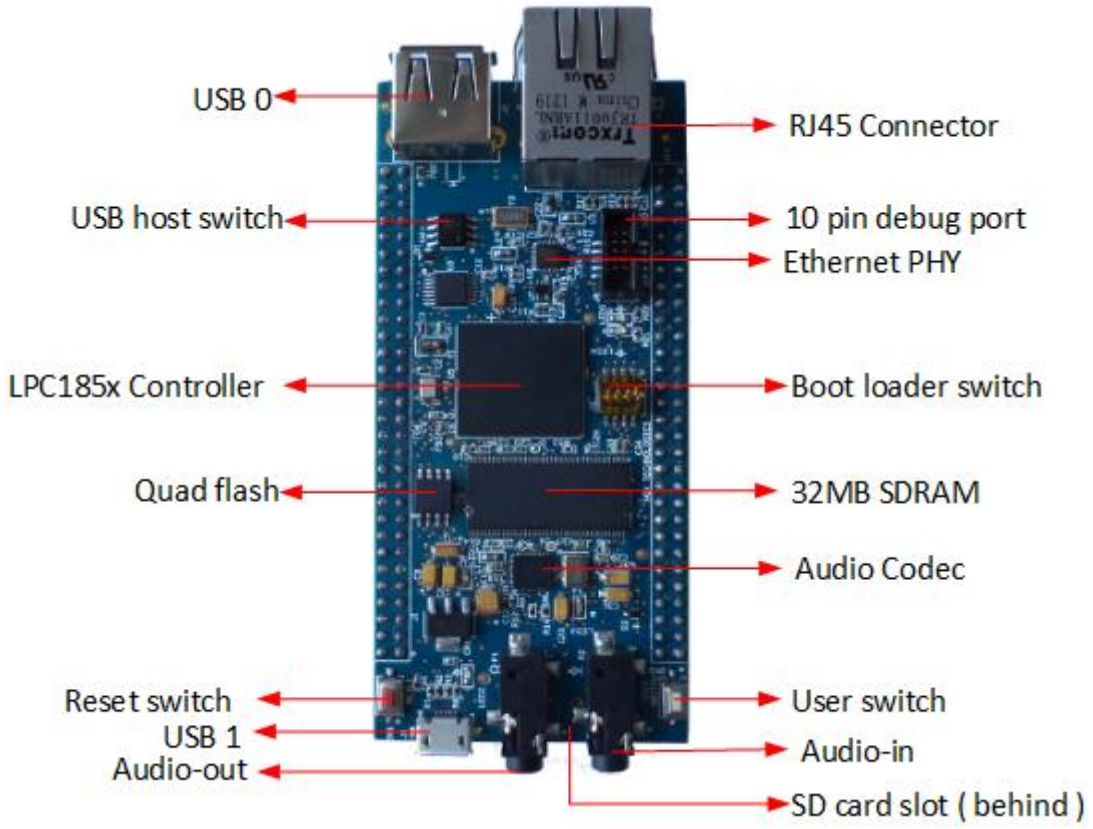


Fig.8

3.2 Powering the Board

The LPC185X-Xplorer++ can be powered through USB1, It is highly recommended that the user tests all the peripherals as soon as the board is received. A regulated supply can be supplied to the 5V pin on the LPC185X-Xplorer++ header.

Note: The USB power can source only up to 500 mA of current. For applications having higher current requirements we recommend to use an external power supply. Please note that the external power supply is not a part of standard delivery.

3.3 Verifying all the peripherals on LPC185X-Xplorer++

The following section focuses on the verification of all the peripherals supported on theLPC185X-Xplorer++. The order of the tests is mentioned in the same manner as the flow of the test firmware. We highly recommend that you follow the order of the test. The test firmware is designed in a manner that the user needs to spend as minimum time as possible to verify all the on-board peripherals. The test firmware executable resides on the Quad Flash. The BOOT select switch is configured to execute from the Quad Flash interface.

Note: The test firmware "Debug Messages" or flow might be changed in due course. Generally these are only cosmetic changes so that the usage is easier. If you observe a different message than the one mentioned in the Manual, do not worry and please proceed with the test.

***Important Note:* The user needs to press the RESET switch to be able to reset the controller. However for the power up reset (USB power cycle) the controller boots up fine.**

Power up the board over USB1 port and we are all set to verify the LPC185X-Xplorer++ peripherals. Before we get to the verification we need to install the Virtual COM port drivers needed for the LPC185X-Xplorer++ (USB1 port) to appear as a Virtual COM port (Used for viewing the debug messages on serial emulation tool). Fortunately, this is a one-time setup and fairly simple. On a Windows machine the user needs to point to the location of the INF file. Download INF file Click Here

Steps to install the VCOM drivers on windows 7 machine:

Step 1: Connect USB1 to the computer, Open device manager, you can find “NXP LPC18xx VCOM” new device listed under ‘Other devices’.

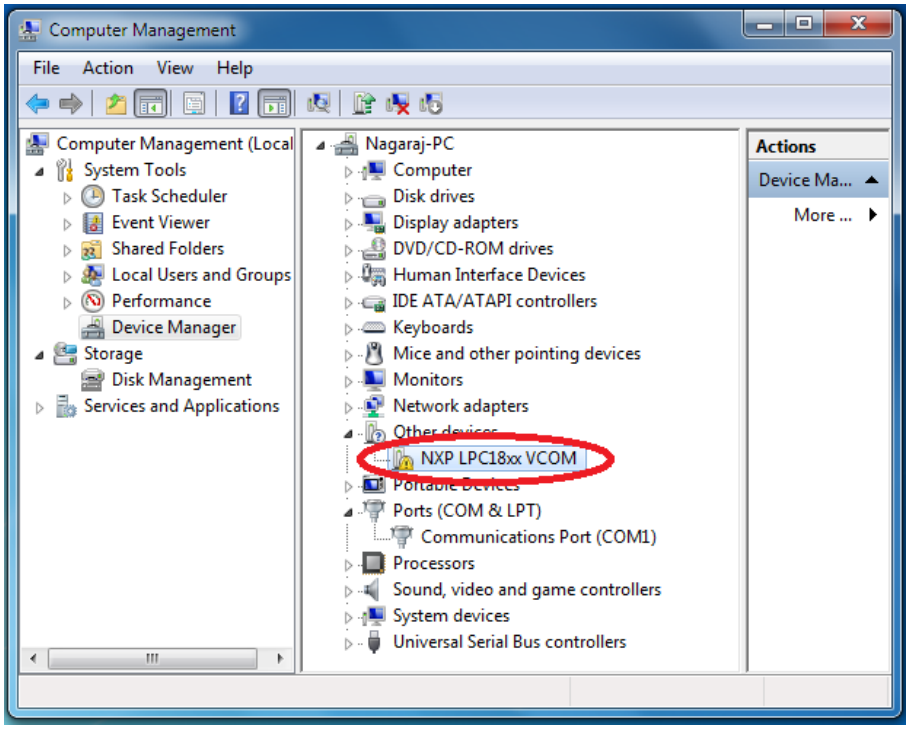


Fig.9

Step 2: Right click on the “NXP LPC18xx VCOM” and then left click on ‘Update Driver Software’.

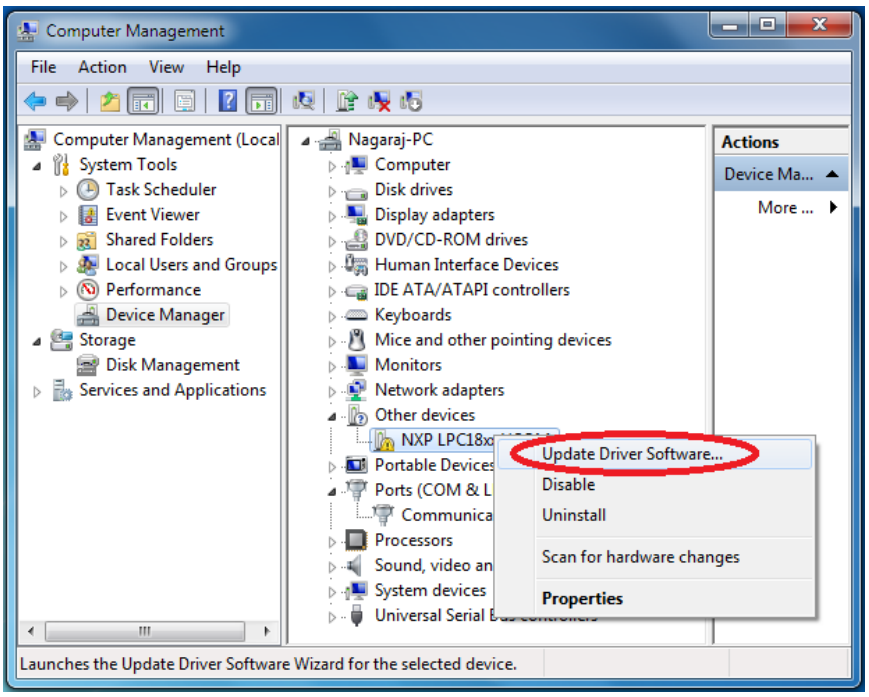


Fig.10

Step 3: Click on Browse my computer for driver software.

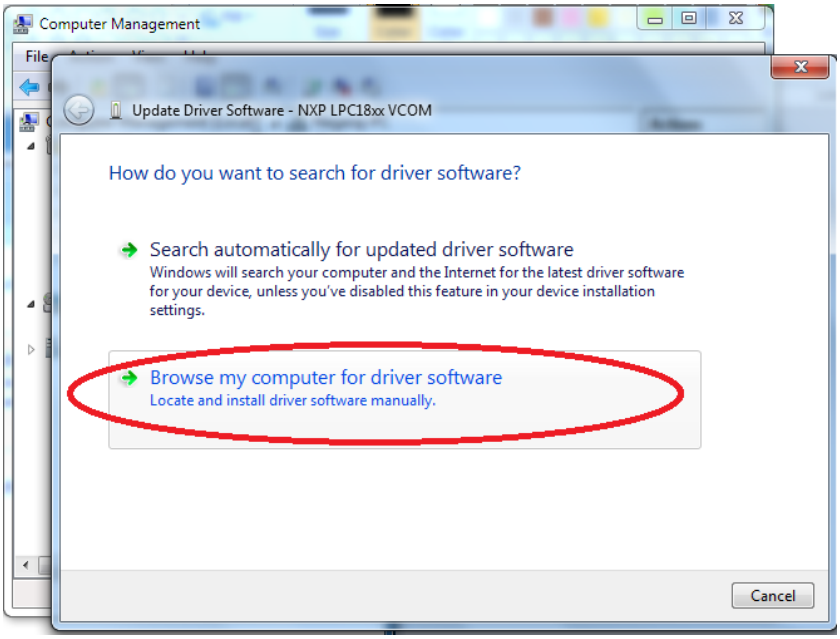


Fig.11

Step 4: Click Browse, select downloaded LPC1850-Xplorer++_Rev AR2_Keil\Usb1VcomLib folder and then click on OK.

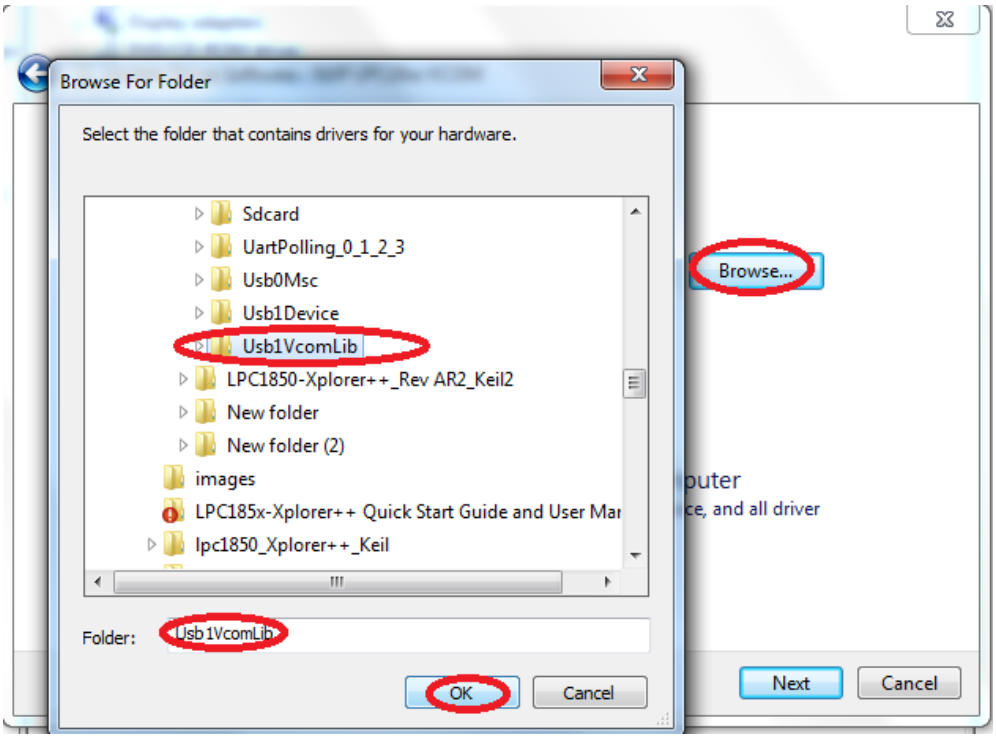


Fig.12

Step 5: Click on Next to continue driver installation.

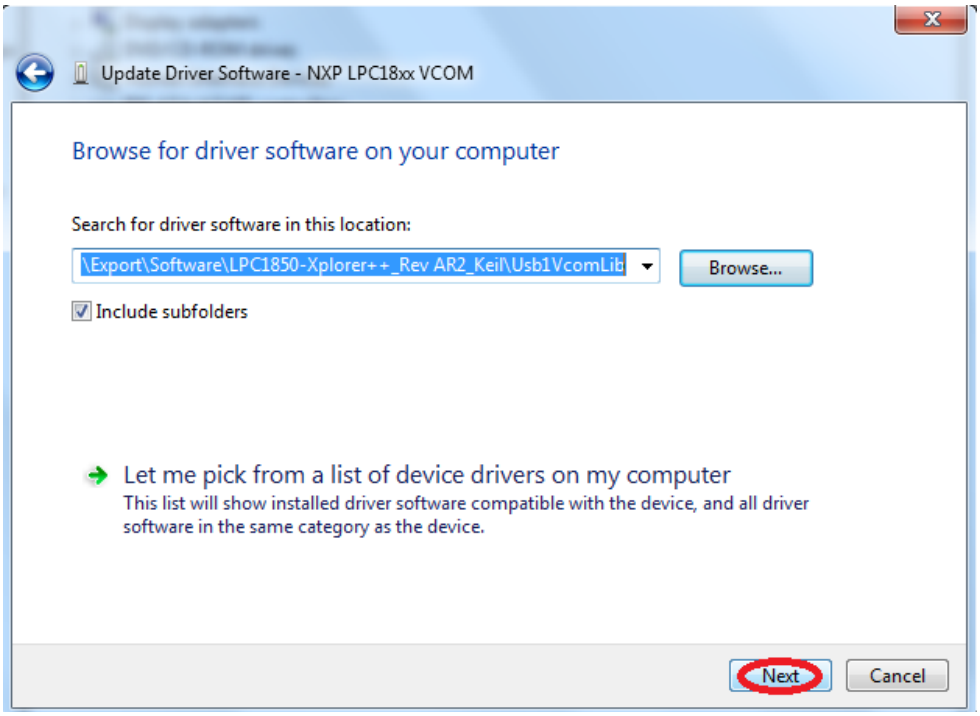


Fig.13

Step 6: Click on 'Install this driver software anyway'.

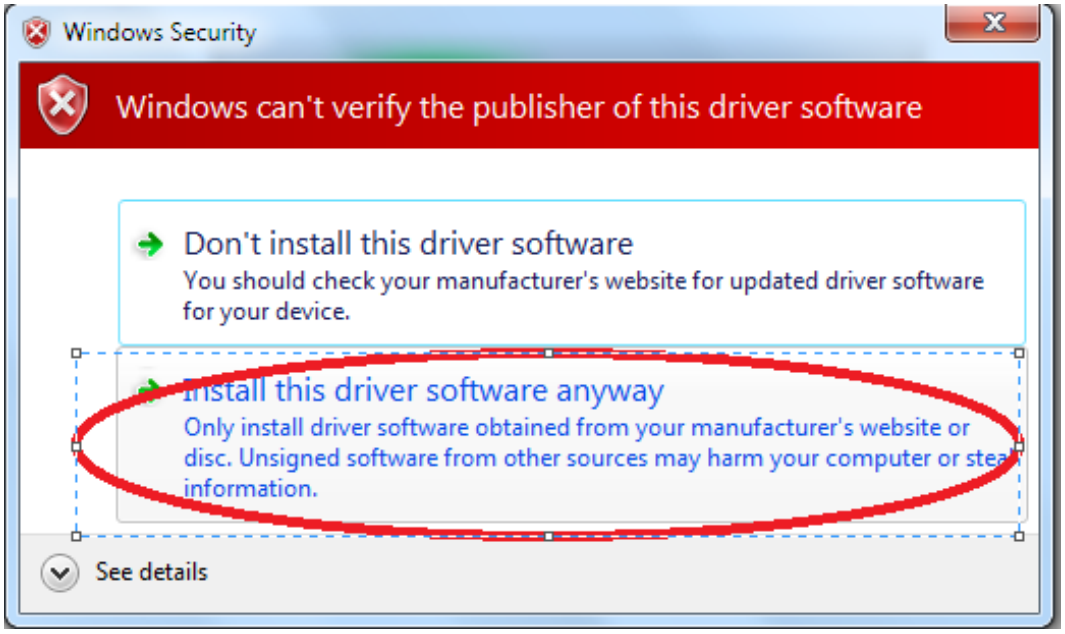


Fig.14

Step 7: The ‘LPC18xx USB VCom driver’ is successfully installed, click on close.

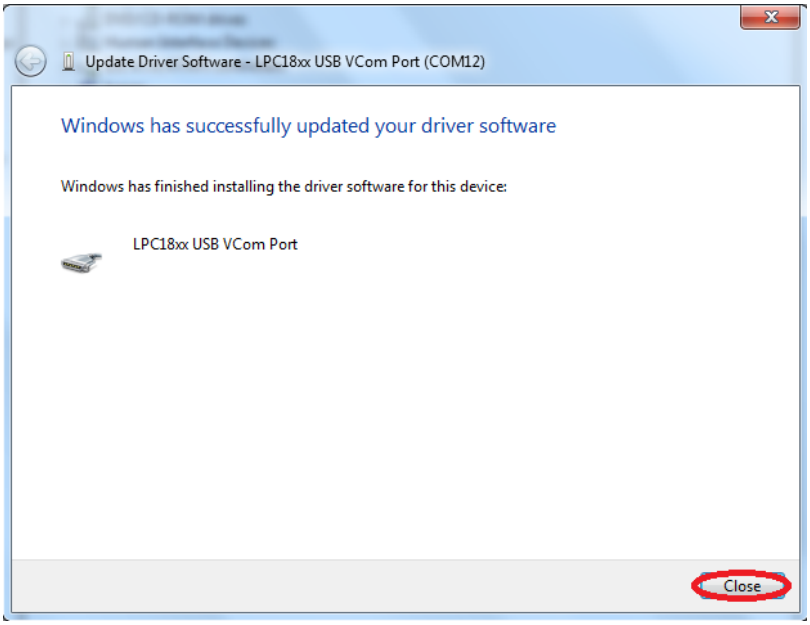


Fig.15

Step 8: Now ‘LPC18xx USB VCom Port’ (COM12) is ready to use.

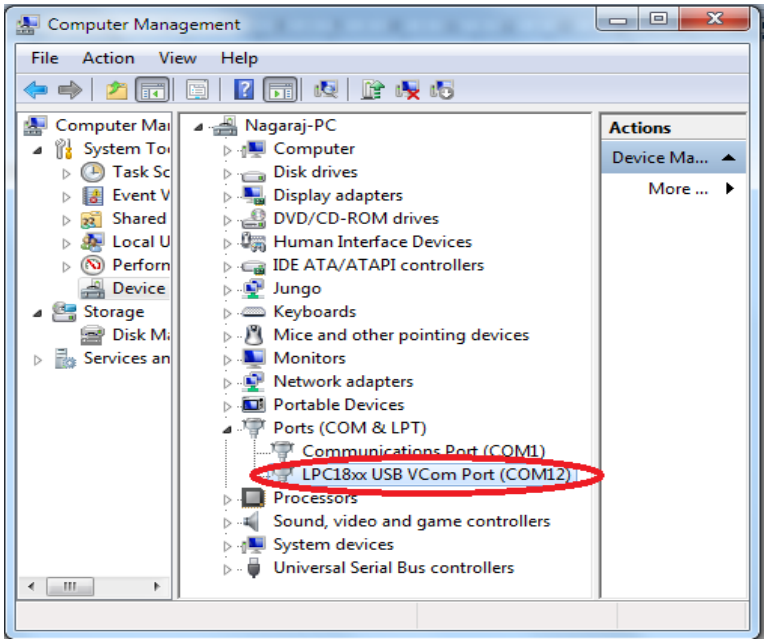
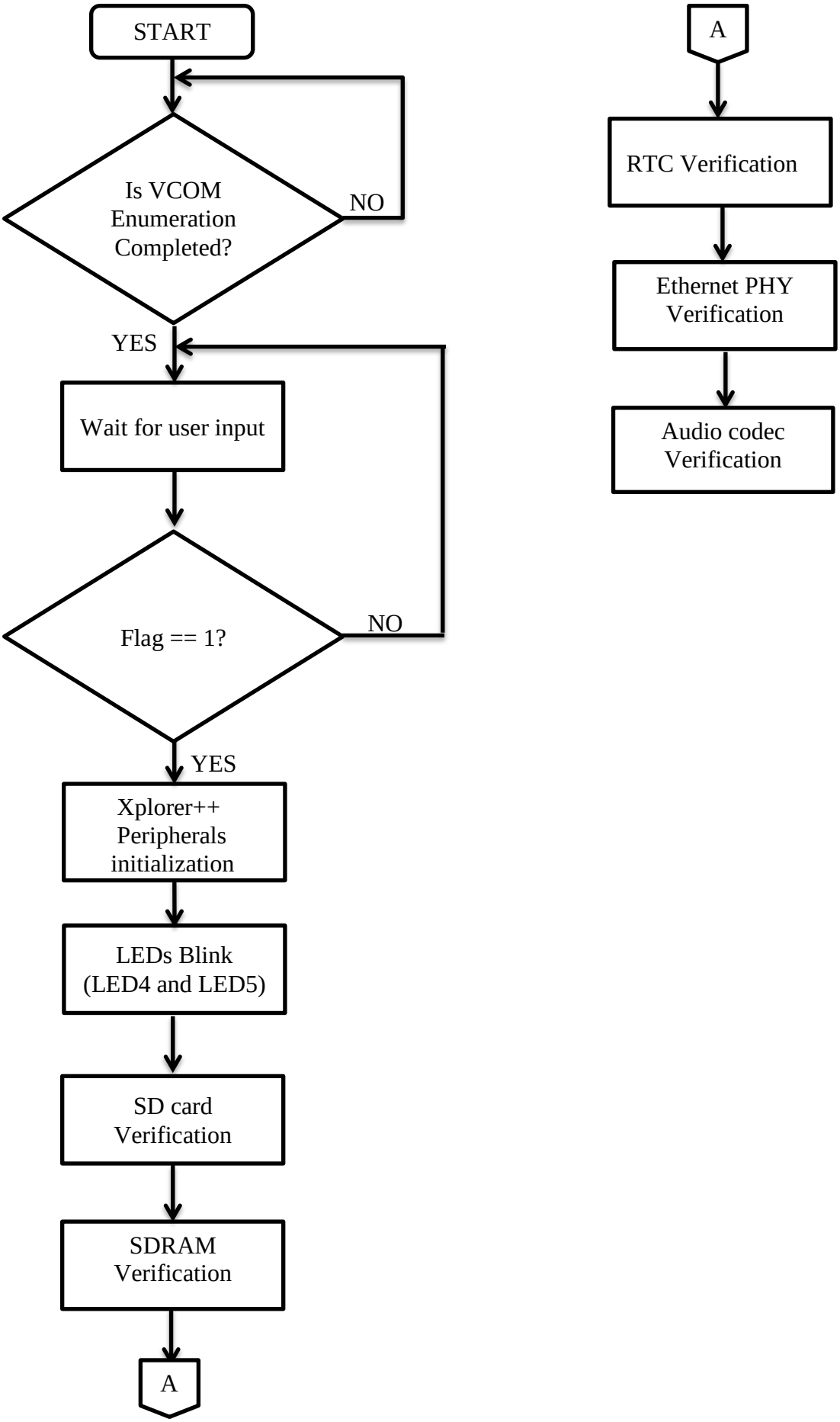


Fig.16

Note: The Virtual COM is listed under the device manager. Please note that the COM port list under the Device Manager is automatically updated with the COM port number for the Virtual COM. On our test machine COM12 is the virtual COM port. The COM12 will appear only if the Xplorer++ board is connected (USB1) to the PC. ***Every time the Xplorer++ is reset the user needs to close the Hyper Terminal application and restart it again.***

The orders in which the on-board peripherals are verified by the firmware are as follows:
Test Firmware Flowchart:



3.3.1 USB1 (Virtual COM port)

Test setup and verification:
For the very first time the windows machine will ask for the appropriate virtual COM drivers to be installed.

Steps to select 'USB1 VCOM port' on HyperTerminal in windows 7 machine:

Step 1: Open a HyperTerminal, type name and click on OK.

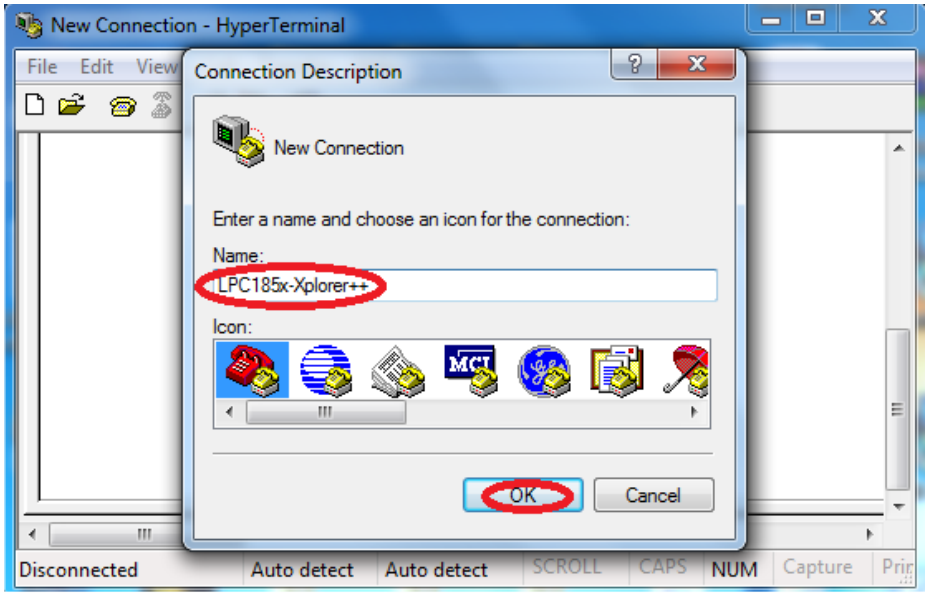


Fig.17

Step 2: Select 'USB1 Vcom Port' (COM12) and click on OK.

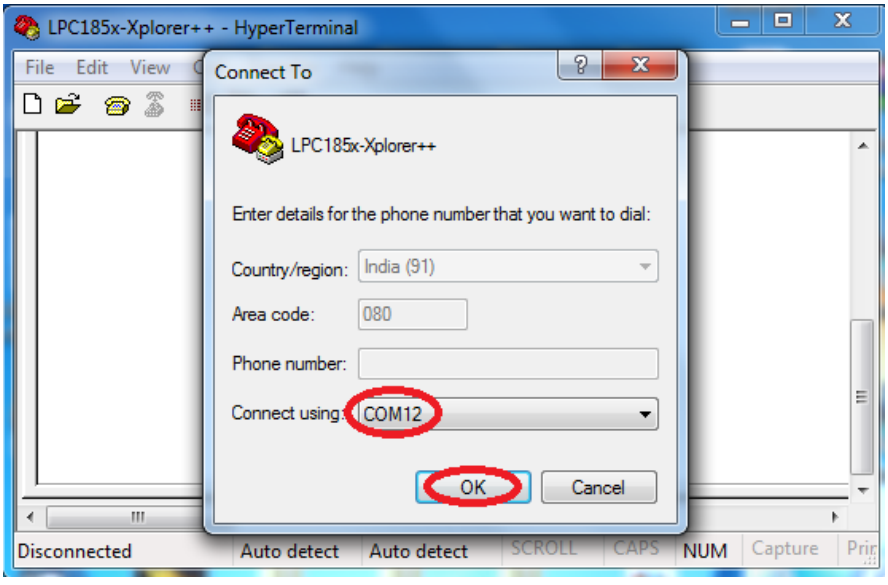


Fig.18

Step 3: Click on ‘Restore Defaults’ and click on OK.

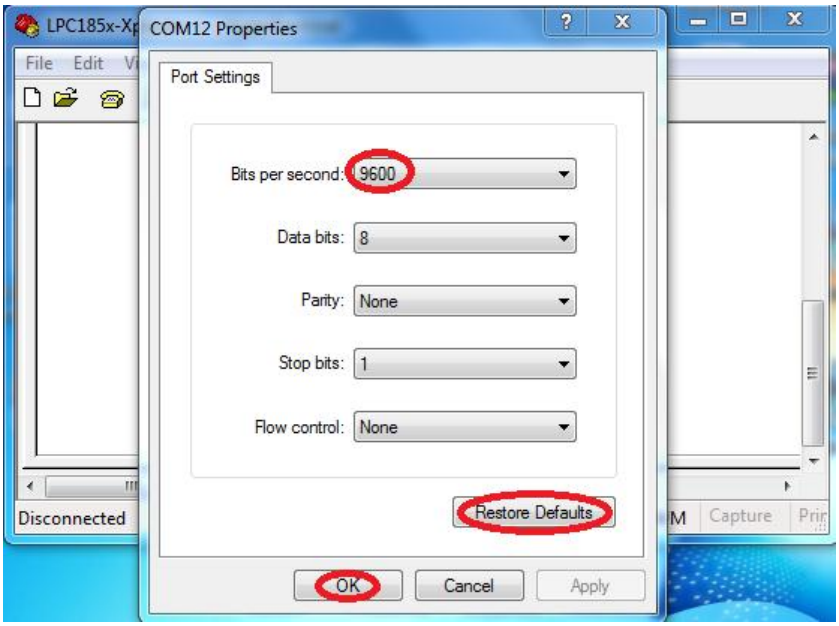


Fig.19

Step 4: Now the ‘USB1 VCom’ is ready to use.

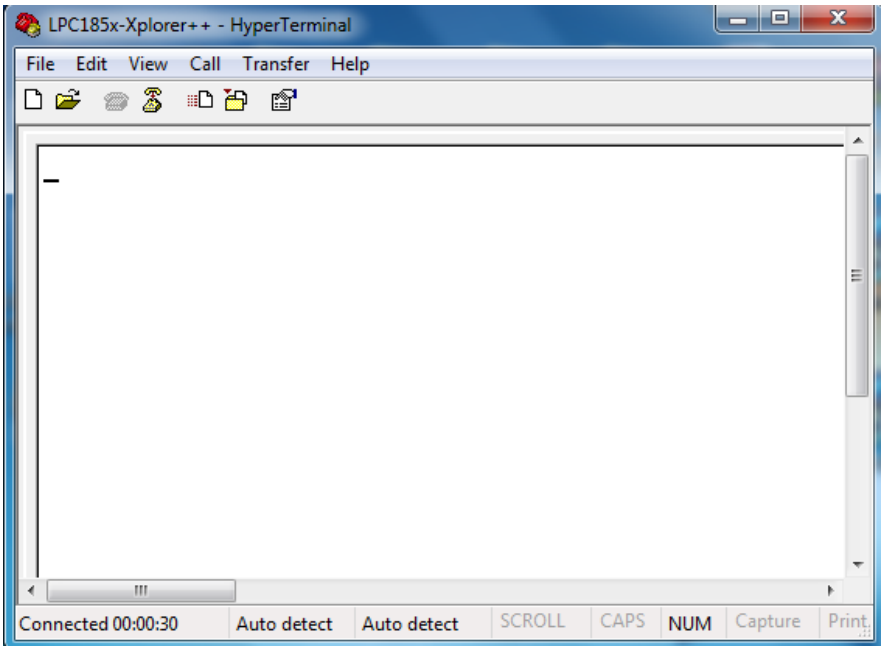


Fig.20

Note: You would not be able to proceed with the verification unless the Virtual COM drivers are installed. The firmware waits for the USB1 to enumerate as VCOM port.

3.3.2 User Input Switch

Test setup and verification:

Once the VCOM drivers are installed the Xplorer++ waits for the User Input Switch to be pressed. Only after detecting a user button (SW2) press the test firmware proceeds with validating other peripherals. This synchronization is necessary to ensure that the debug messages on the VCOM port can be viewed from the start of the test. Without this synchronization the test firmware would proceed with the debug messages being displayed, while the user is still configuring the Hyper-Terminal or other serial emulation tool.

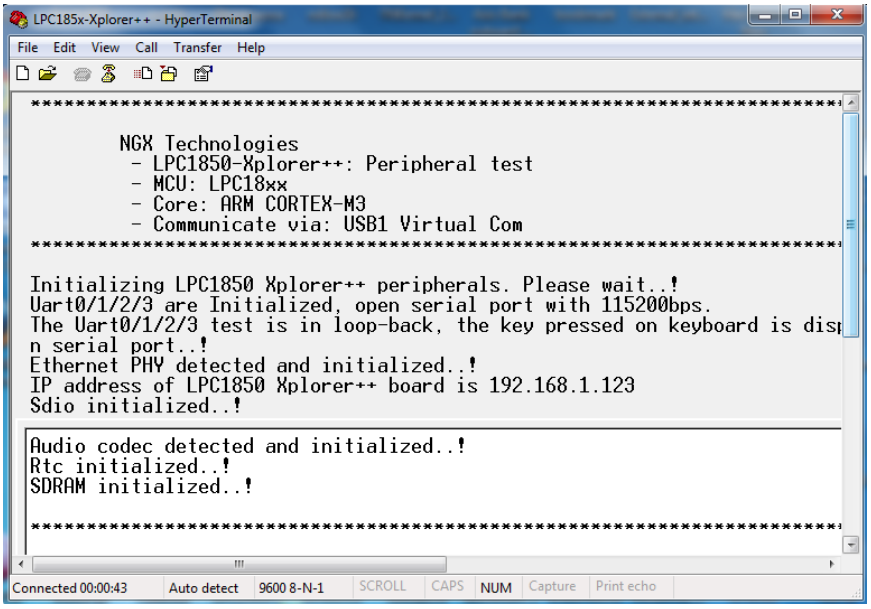


Fig.21

Once the hardware initialization is completed menu will be displayed as shown in the following image

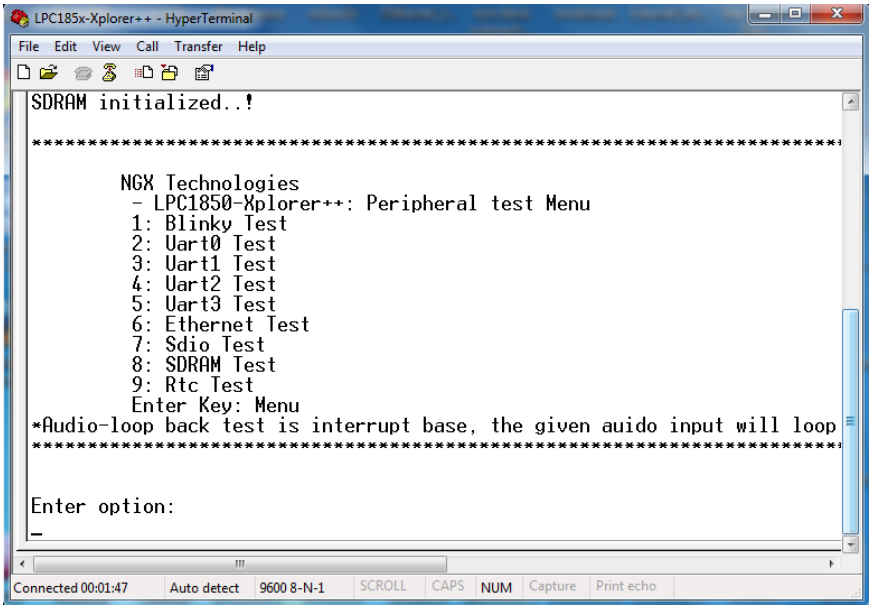


Fig.22

3.3.3 Test LEDs

Test setup and verification:
To test LEDs, enter option 1, the LED4 and LED5 on board starts blinking.

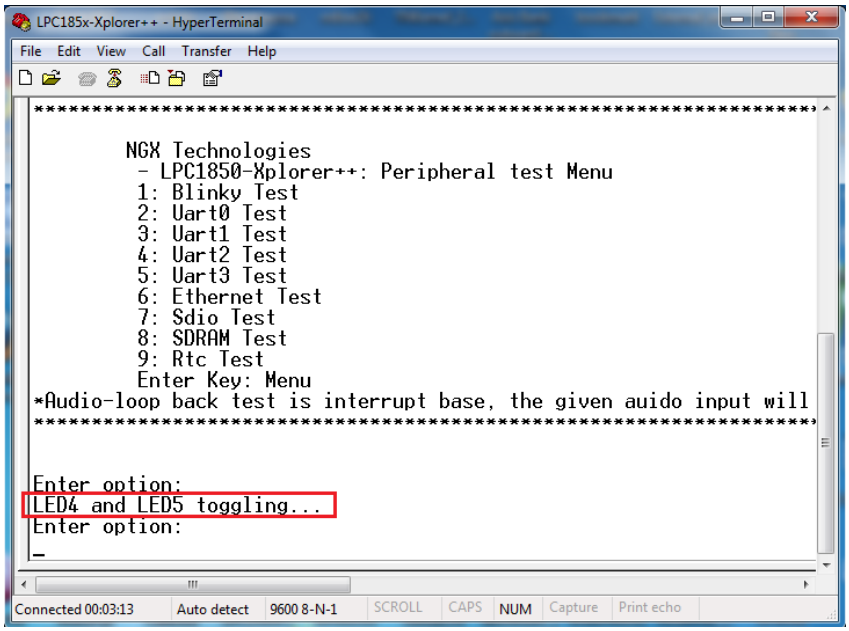


Fig.23

3.3.4 Micro SD connector

Test setup and verification:
To test SDIO enter option 7, the firmware validates the micro SD card interface by writing and reading a sector of the SD card connected. Please note that we need to use a micro SD card with FAT file system. The result of this test is displayed over the VCOM port.

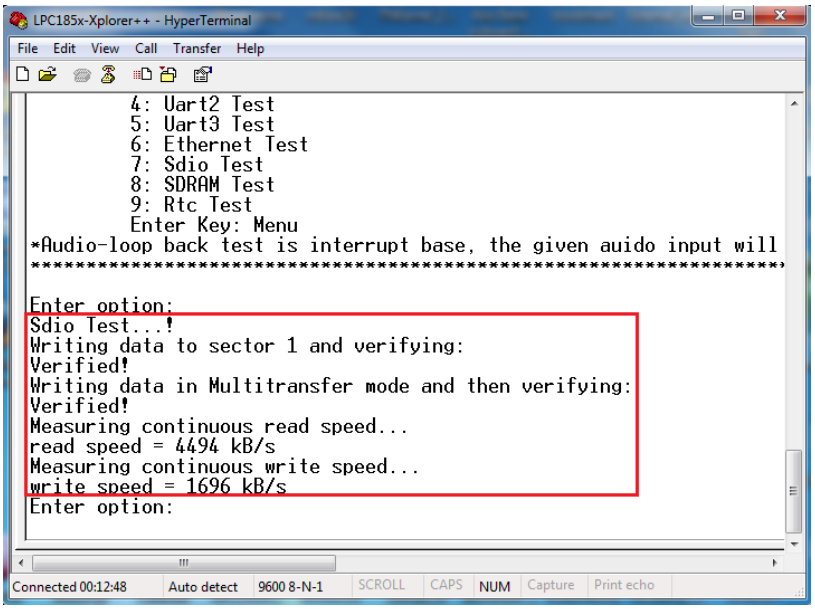


Fig.24

3.3.5 SDRAM

Test setup and verification:
To test SDRAM enter option 8, the result of this test is displayed over the VCOM port as shown in the following image.

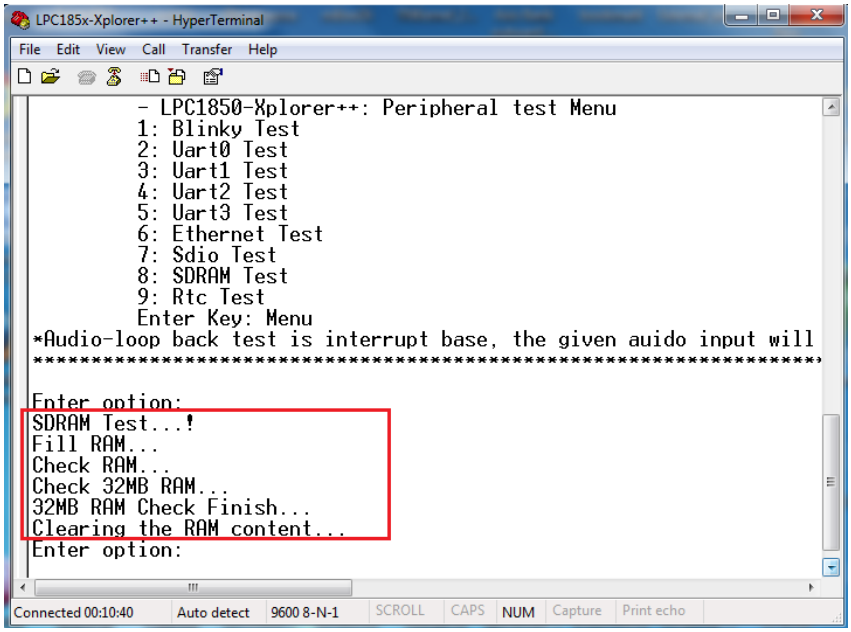


Fig.25

3.3.6 RTC

Test setup and verification:
To test RTC enter option 9, the time and date will be displayed over the VCOM port as shown in the following image.

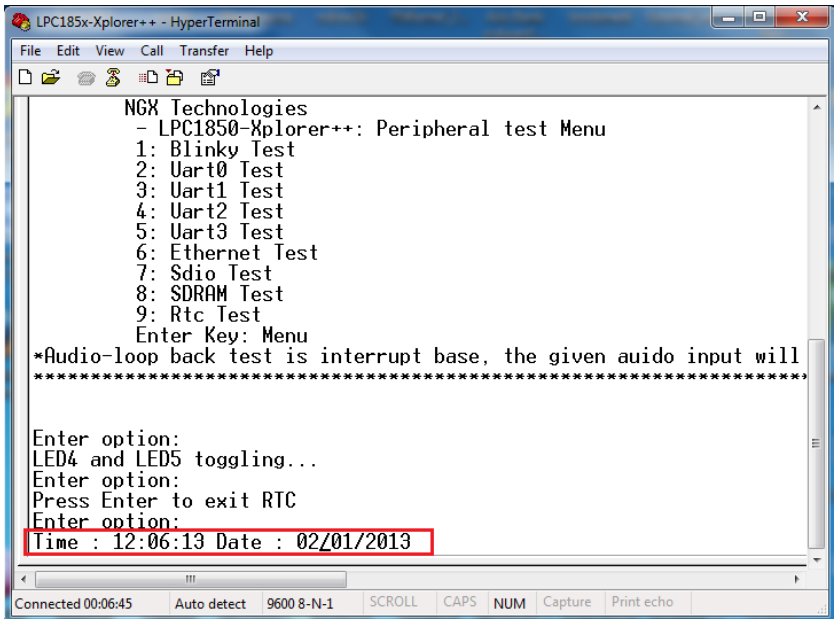


Fig.26

3.3.7 Ethernet

Test setup and verification:
To test Ethernet, enter option 6, the test firmware configures the LPC185x-Xplorer++ board as a webserver.

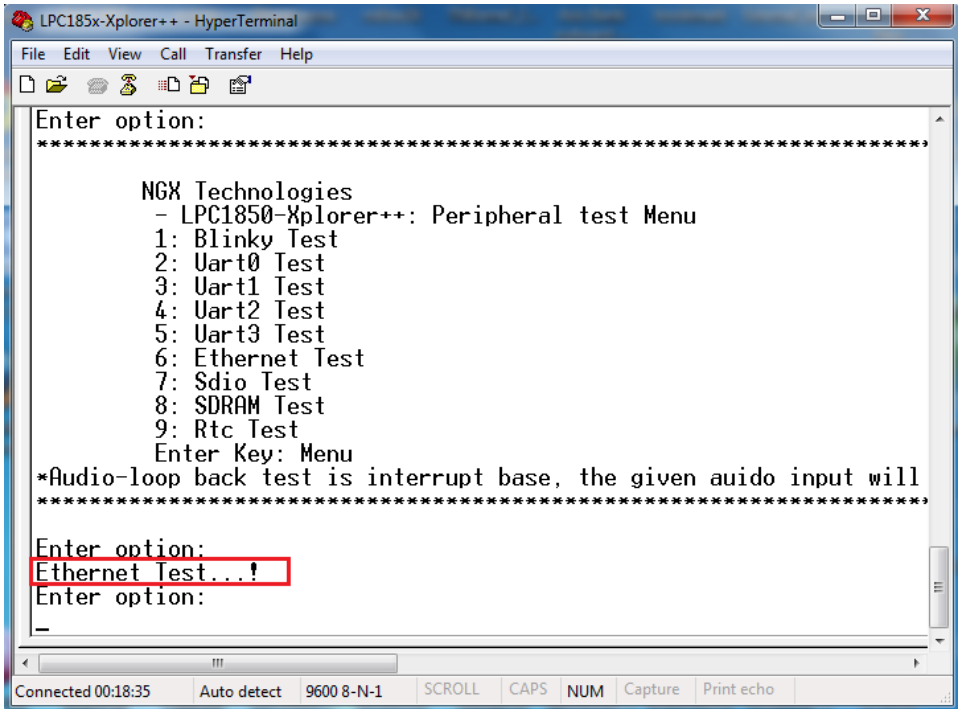


Fig.27

The Ethernet interface can be verified by either using a PING command in the windows command prompt.

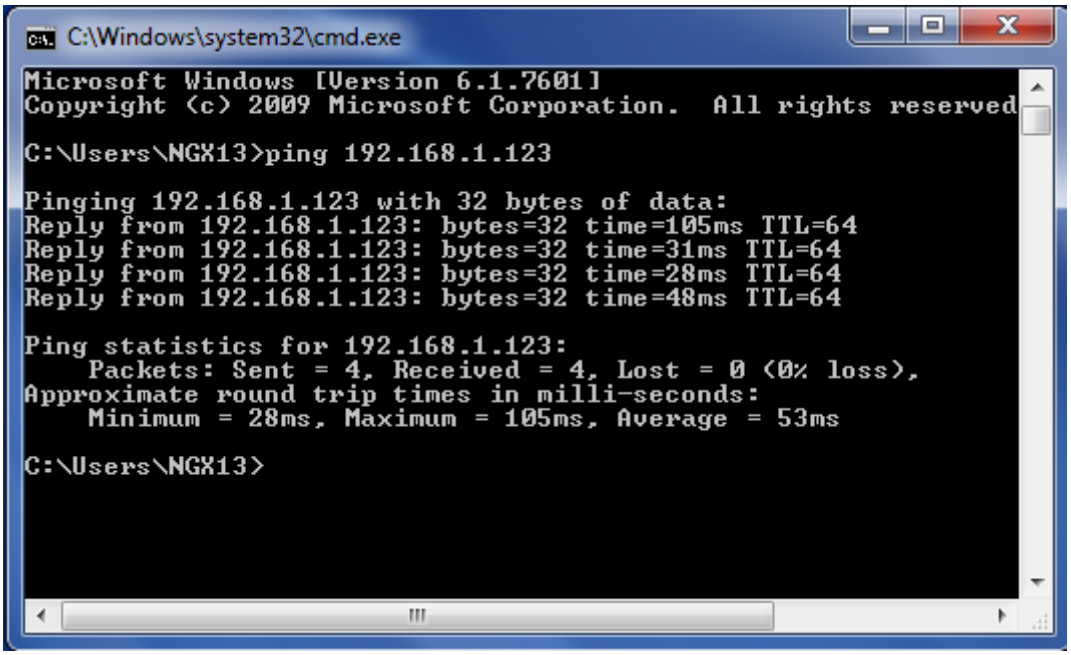


Fig.28

The IP address of the LPC185x-Xplorer++ board is configured as 192.168.1.123. Type the same IP address in the browser. Clicking the ON button will TURN-ON LED4 and clicking OFF button will TURN-OFF LED4.

Fig.29

3.3.8 Audio Interface

Test setup and verification:

For the audio interface the LPC185x-Xplorer++ incorporates external audio codec from NXP. The codec is interfaced to the MCU over I2S0 for data and over I2C0 for command interface. The test firmware verifies both the audio-in and audio-out path. To verify the audio interface the user needs to feed some audio data through the audio-in (LINE-IN) interface and then connect a headphone at the audio-out jack. If one is able to hear the same audio data that is being fed over audio-in interface, we have verified the audio interface.

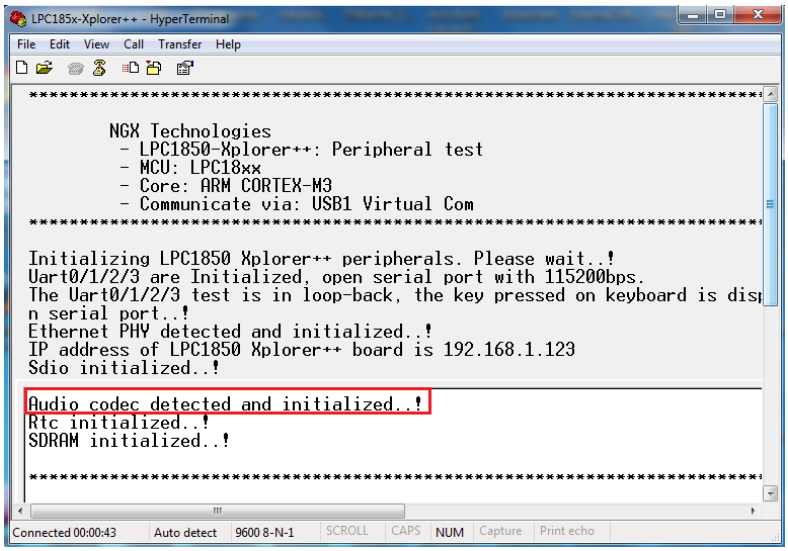


Fig.30

3.3.9 USB0_HOST

Test setup and verification:
Connect the USB AM to Micro cable to USB1 on board connector and PC and Flash the Usb0Msc binary and RESET the board. Open Hyper-Terminal and select Vcom port with 9600Mbps, insert the 2 GB pen drive to on board host connector, the content of first sector is displayed on Hyper-Terminal as shown in the following image.

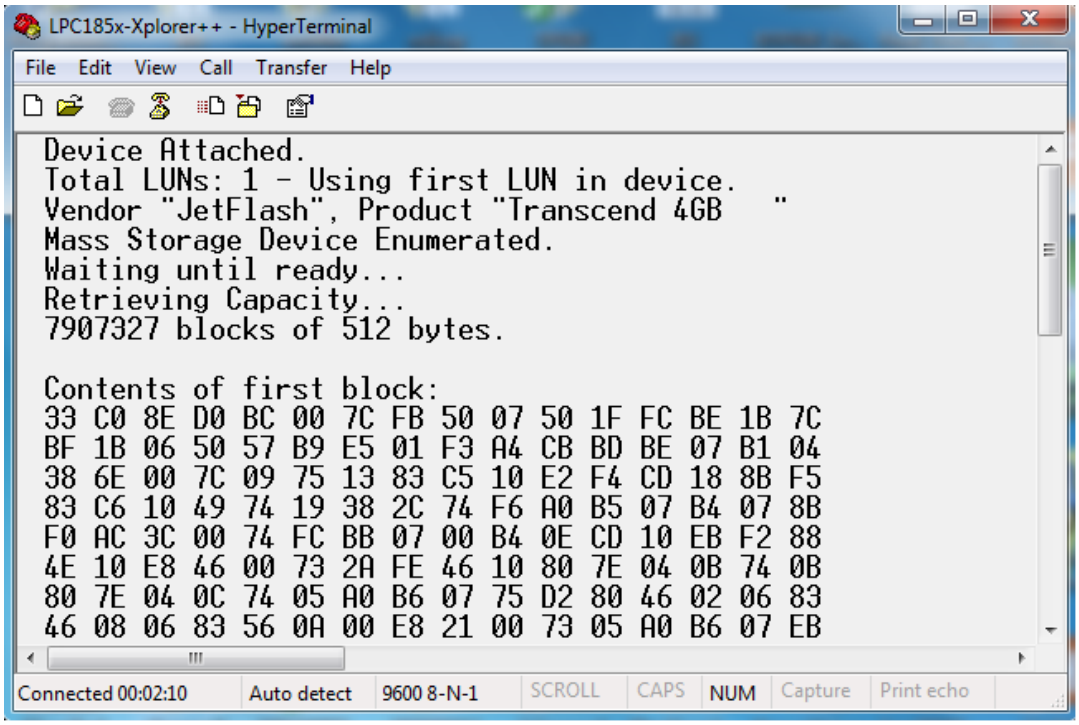


Fig.31

About this document:

Revision History

Version: V1 author: Veeresh Tumbaragi

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