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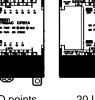
System Configuration

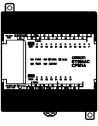
■ CPM1A Line-up

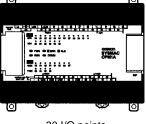
CPU with AC Power Supply

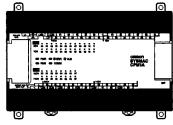
• DC input • RY output

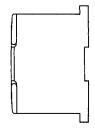












10 I/O points (Expansion not possible)

20 I/O points (Expansion not possible)

30 I/O points

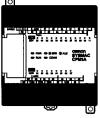
40 I/O points

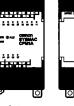
CPU with **DC** Power Supply

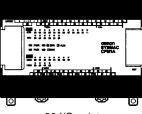
• DC input • RY output / TR output (Only DC power supply can be used with TR-output type.)

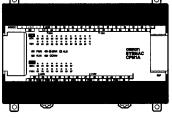


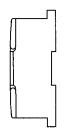












10 I/O points (Expansion not possible)

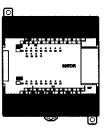
20 I/O points (Expansion not possible)

30 I/O points

40 I/O points

Expansion I/O Unit

- DC input
- RY output / TR output



20 I/O points

Expansion I/O Unit

- DC input
- RY output / TR output

CompoBus/S I/O Unit

CPM1A-SRT21

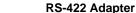




Analog I/O Unit



RS-232C Adapter





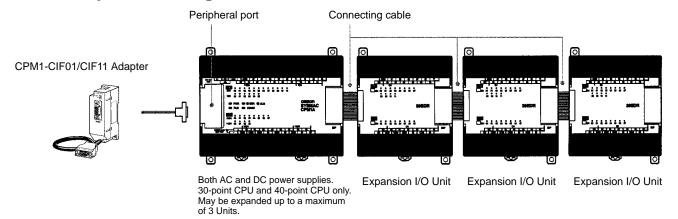
CPM1-CIF01



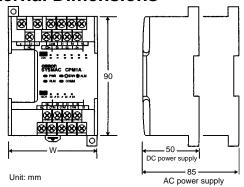
CPM1-CIF11

System Configuration

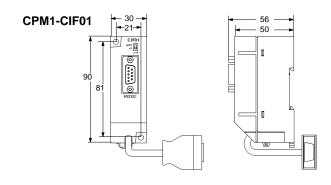
■ CPM1A System Configuration

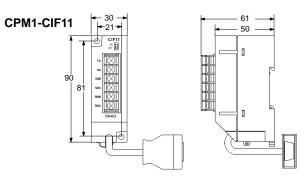


■ External Dimensions



Model	W (mm)
CPM1A-10CD□-A/D	66
CPM1A-20CD□-A/D	86
CPM1A-30CD□-A/D	130
CPM1A-40CD□-A/D	150
CPM1A-20ED□	86 (depth: 50 mm)
CPM1A-8E□/SRT21	66 (depth: 50 mm)
CPM1A-MAD01	66 (depth: 50 mm)





■ General Specifications

Iten	n	10-point I/O	20-point I/O	30-point I/O	40-point I/O	
Power supply voltage/	AC power supply	100 to 240 VAC, 50)/60 Hz			
frequency DC power supply		24 VDC				
Operating voltage	AC power supply	85 to 264 VAC				
range	DC power supply	20.4 to 26.4 VDC				
Power consumption	AC power supply	30 VAC max.		60 VAC max.		
	DC power supply	6 W max.		20 W max.		
Inrush current		30 A max.		60 A max.		
External power supply (AC only)	Power supply voltage	24 VDC				
	Power supply output capacity	200 mA		300 mA		
Insulation resistance		20 M Ω min. at 500 terminal.	VDC between the A	C terminals and the	protective earth	
Dielectric strength		2,300 VAC at 50/60 Hz for one minute with a leakage current of 10 mA max. between all the external AC terminals and the protective earth terminal.				
Noise resistance		1,500 V (peak to peak) with a pulse width of 0.1 to 1 μ s, and 1-ns rise time pulse (tested with a noise simulator)				
Vibration resistance		10 to 57 Hz with an amplitude of 0.075 mm, and 57 to 150 Hz with an acceleration of 9.8 m/s ² in the X, Y, and Z directions for 80 minutes each (i.e. swept for 8 minutes, 10 times).				
Shock resistance		147 m/s ² in the X, Y and Z directions 3 times each.				
Ambient temperature (o	perating)	0° to 55°C				
Ambient humidity (opera	ating)	10% to 90% (no condensation)				
Ambient environment (c	perating)	With no corrosive gas				
Ambient temperature (s	torage)	−20° to 75°C				
Terminal screw size		M3				
Power supply holding til	me	10 ms min. for AC models, and 2 ms min. for DC models				
Weight		AC model: 400 g max. DC model: 300 g max.	AC model: 500 g max. DC model: 400 g max.	AC model: 600 g max. DC model: 500 g max.	AC model: 700 g max. DC model: 600 g max.	

Note: 1. The specifications of the Expansion I/O Unit are the same as for the CPU except that the power is supplied from the CPU and the weight is 300 g.

2. TR output is only available to CPUs with DC power supply.

■ Performance Specifications

Item		10-point I/O	20-point I/O	30-point I/O	40-point I/O		
Control method		Stored program meth	nod				
I/O control method		Combination of the cyclic scan and immediate refresh processing methods.					
Programming language		Ladder diagram					
Instruction word		1 step per instruction	, 1 to 5 words per instru	ıction			
Types of	Basic instructions	14 types	14 types				
instructions	Special instructions	79 types, 139 instructions					
Instruction	Basic instructions	0.72 to 16.2 μs					
execution time	Special instructions	MOV instruction = 16	i.3 μs				
Program capacit	ty	2,048 words					
Maximum I/O points	CPU only	10 points (6 input/ 4 output points)	20 points (12 input/ 8 output points)	30 points (18 input/ 12 output points)	40 points (24 input/ 16 output points)		
	With Expansion I/O Unit			90 points (54 input/ 36 output points)	100 points (60 input/ 40 output points)		
Input bits		00000 to 00915 (Wo	ds 0 to 9)				
Output bits		01000 to 01915 (Wo	· · · · · · · · · · · · · · · · · · ·				
Work bits (IR Are	ea)	512: IR 20000 to IR 2	23115 (IR 200 to IR 231)			
Special bits (SR	Area)	384: SR 23200 to SR	25515 (SR 232 to SR	255)			
Temporary bits (•	8: TR 0 to TR 7					
Holding bits (HR	Area)	320: HR 0000 to HR 1915 (HR 00 to HR 19)					
Auxiliary bits (AF	R Area)	256: AR 0000 to AR 1515 (AR 00 to AR 15)					
Link bits (LR Are	ea)	256: LR 0000 to LR 1515 (LR 00 to LR 15)					
Timers/Counters	3	128: TIM/CNT 000 to 127 100-ms timer: TIM 000 to TIM 127 10-ms timer: TIM 000 to TIM 127 Decremental counter, reversible counter					
Data memory	Read/Write	1,024 words (DM 000	00 to DM 1023)				
	Read only	512 words (DM 6144	to DM 6655)				
Interrupt process External interrup		2 points (Response time of 0.3 ms max.) 4 points (Response time of 0.3 ms max.)					
Memory protecti	on	Maintains the contents of the HR, AR, Counter and Data Memory Areas.					
Memory backup		Flash memory: User program, data memory (Read only) (Non-battery powered storage)					
		Super capacitor: Data memory (Read/Write), holding bits, auxiliary memory bits, counter (20-day storage at an ambient temperature of 25°C)					
Self-diagnostic f	unction	CPU error (watchdog timer), memory errors, I/O bus errors					
Program check		No END instruction programming errors (constantly checked during operation)					
Pulse output		1 point: 2 kHz					
High-speed counter		1 point: Single phase at 5 kHz or two-phase at 2.5 kHz (linear counting method) Incremental mode: 0 to 65535 (16-bit) Decremental mode: -32767 to 32767 (16-bit)					
		1 point: Single phase at 5 kHz or two-phase at 2.5 kHz (linear counting method) Incremental mode: 0 to 65535 (16-bit) Decremental mode: -32767 to 32767 (16-bit)					
Quick-response inputs		Together with the external interrupt input (minimum pulse width of 0.2 ms)					
Input time constant		Can be set at 1 ms, 2 ms, 4 ms, 8 ms, 16 ms, 32 ms, 64 ms, or 128 ms.					
Analog settings		2 points: (0 to 200)					

Note: Bits that are not used for the I/O bits can be used as work bits.

■ I/O Specifications

Input Circuit

CPU

Item Specifications		Circuit
Input voltage	24 VDC +10%/_15%	Input
Input impedance	IN0000 to IN0002: 2 k Ω Others: 4.7 k Ω	LED
Input current (typical)	IN0000 to IN0002: 12 mA Others: 5 mA	IN 4.7 kΩ \$ The linternal Circuits
ON voltage	14.4 VDC min.	COM CIRCUITS
OFF voltage	5.0 VDC max.	7 i i
ON delay (see note 1)	1 to 128 ms max. (default: 8 ms) (see note 1)	Note The polarity of the input power supply can be either
OFF delay (see note 1)	1 to 128 ms max. (default: 8 ms) (see note 1)	positive or negative.

Note: 1. The actual ON/OFF delay includes an input constant of 1, 2, 4, 8, 16, 32, 64, or 128 ms (default: 8 ms).

2. The delays for IN0000 to IN0002 are as follows when used for the high-speed counter.

Input	Increment mode	Differential phase mode	
IN0000 (A-phase)	5 kHz	2.5 kHz	
IN0001 (B-phase)	Normal input		
IN0002 (Z-phase)	ON: 100 μs max. OFF: 500 μs max.		

3. The delays for IN0003 to IN0006 are as follows when used for the high-speed counter.

0.3 ms max. (From the time of input ON until the interrupt subroutine is executed.)	0.3 ms max. (From the time of input ON until the interrupt subroutine is executed.)
---	---

Expansion I/O Unit

Item	Specifications	Circuit
Input voltage	24 VDC, +10%/_15%	Input
Input impedance	4.7 kΩ	LED
Input current (typical)	5 mA	4.7 kΩ
ON voltage	14.4 VDC min.	IN Internal
OFF voltage	5.0 VDC max.	$\begin{array}{c c} & \vdots & $
ON delay	1 to 128 ms max. (default: 8 ms) (see note)	
OFF delay	1 to 128 ms max. (default: 8 ms) (see note)	Note The polarity of the input power supply can be either positive or negative.

Note: The actual ON/OFF delay includes an input constant of 1, 2, 4, 8, 16, 32, 64, or 128 ms (default: 8 ms).

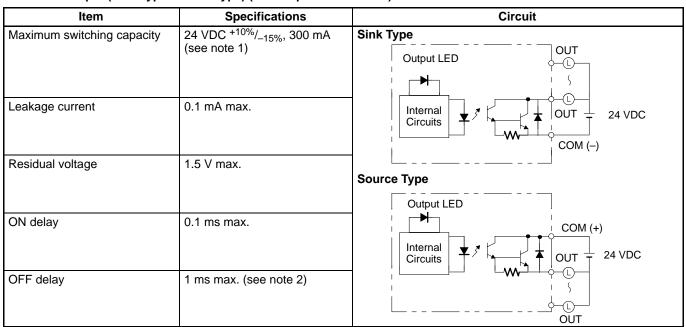
Output Circuit

CPU and Expansion I/O Unit

Relay Output

Item			Specifications	Circuit	
Maximum switching capacity		capacity	250 VAC/2 A (cos φ =1) 24 VDC/2 A (4 A/common)	Output OUT	
Minimum	switching o	capacity	5 VDC, 10 mA		
Relay service life	ay Electrical Resis- 300,000 times Internal		1 (X) U(I) (A) = =		
		Inductive load	100,000 times	Maximum 250 VAC: 2 A	
Mechanical		al	10 million times	24 VDC: 2 A	
ON delay			15 ms max.		
OFF dela	ay		15 ms max.		

Transistor Output (Sink Type/Source Type) (CPU/Expansion I/O Unit)



Note: 1. The maximum switching capacity of the CPM1A with transistor outputs (sink type and source type) are limited to the currents shown in the following table for the common and for the Unit.

Item	10CDT/	20CDT-D/	30CDT-D/	40CDT-D/	20EDT/	CPM1A-8ET/
	10CDT1-D	20CDT1-D	30CDT1-D	40CDT1-D	20EDT1	8ET1
Max. switching capacity	0.9 A/Unit	0.9 A/common 1.8 A/Unit	0.9 A/common 2.7 A/Unit	0.9 A/common 3.6 A/Unit	0.9 A/common 1.8 A/Unit	

2. When using the pulse output function of the CPM1A with transistor outputs (sink type and source type):
The output current must be within a range from 100 to 200 mA when using the output 01000 or 01001 as a pulse output with the maximum frequency of 2 kHz. The outputs 01000 and 01001 will vary depending on the output current.

Load current	OFF delay
100 to 200 mA	0.2 ms max.
0 to 300 mA except for the above range	0.5 ms max.

■ Analog I/O Unit

	Item	Voltage I/O	Current I/O	
Analog	Number of inputs	2	•	
inputs	Input signal range	0 to 10 V or 1 to 5 V	4 to 20 mA	
	Maximum rated input	±15 V	±30 mA	
	External input impedance	1 M Ω min.	250 Ω rated	
	Resolution	1/256	•	
	Overall precision	1.0% of full scale		
	Converted A/D data	8-bit binary		
Analog	Number of outputs	1		
output (See	Output signal range	0 to 10 V or -10 to 10 V	4 to 20 mA	
note 1.)	External output max. current	5 mA		
ĺ	External output allowed load resistance		350 Ω	
	Resolution	1/256 (1/512 when the output si	ignal range is -10 to 10 V.)	
	Overall precision	1.0% of full scale		
	Data setting	8-bit binary with sign bit		
Conversion time (See note 2.)		10 ms/Unit max.		
Isolation method		Photocoupler isolation between (There is no isolation between t		

Note 1. The voltage output and current output can be used at the same time, but the total output current cannot exceed 21 mA.

2. The conversion time is the total time for 2 analog inputs and 1 analog output.

■ CompoBus/S I/O Link Unit

Specifications

Item	Specification	
Model number	CPM1A-SRT21	
Master/Slave	CompoBus/S Slave	
Number of I/O bits	8 input bits, 8 output bits	
Number of words occupied in	1 input word, 1 output word	
CPM1A I/O memory	(Allocated in the same way as other Expansion Units)	
Node number setting	Set using the DIP switch.	

Note: See the CompoBus/S Catalog (Q103) for more details on CompoBus/S communications.

■ Communications Adapter Specifications

RS-232C Adapter and RS-422 Adapter

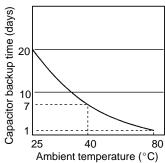
Item	Specifications				
	CPM1-CIF01	CPM1-CIF11			
Functions	Level conversion between the CMOS level (CPU side) and the RS-232C (peripheral device side)	Level conversion between the CMOS level (CPU side) and the RS-422 (peripheral device side)			
Insulation	The RS-232C (peripheral device side) is insulated by a DC/DC converter and photocoupler.	The RS-422 (peripheral device side) is insulated by a DC/DC converter and photocoupler.			
Power supply	Power is supplied by the CPU.				
Power consumption	0.3 A max.				
Transmission speed	38.4 Kbits/s max.				
Vibration resistance	10 to 57 Hz with an amplitude of 0.075 mm, and 57 to 150 Hz with an acceleration of 9.8 m/s ² in the X, Y and Z directions for 80 minutes each in accordance (i.e. swept for 8 minutes, 10 times).				
Shock resistance	147 m/s ² in the X, Y and Z directions 3 times each.				
Ambient temperature (operating)	0° to 55°C				
Ambient humidity (operating)	10% to 90% (with no condensation)				
Ambient environment (operating)	With no corrosive gas				
Ambient temperature (storage)	-20° to 75°C				
Weight	200 g max.				

■ Memory Backup

The user program and memory area data in the CPU Unit are backed up by either one of the following methods.

- Flash Memory: User program, read-only DM area (DM 6144 to DM 6599), and PC Setup area (DM 6600 to DM 6655).
- Internal Capacitor:
 DM areas other than the above, HR area, AR area, and Counter area.

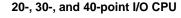
The capacitor provides backup for a power interruption lasting 20 days at room temperature. If the power is expected to remain OFF for a period exceeding this data backup period, consideration must be given to the design of the system so that no problems will occur when the set values become undefined ones. For further details, refer to *CPM1A Operation Manual (W317)*.

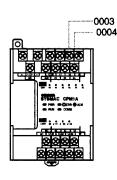


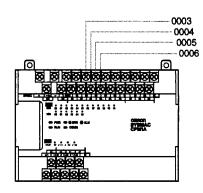
Input Interrupts

There are two input interrupts in the CPM1A 10-point I/O CPU and four in the 20-, 30-, and 40-point I/O CPUs. Input interrupts are available in two modes.

10-point I/O CPU



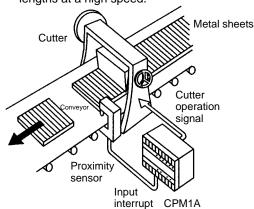




Application Example:

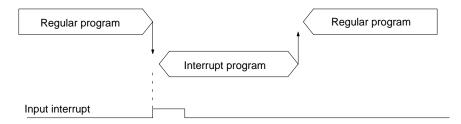
Cutting Metal Sheets to Specified Lengths

The proximity sensor detects the edge of a metal plate to operate the cutter. Metal sheets can be cut continuously to the specified lengths at a high speed.



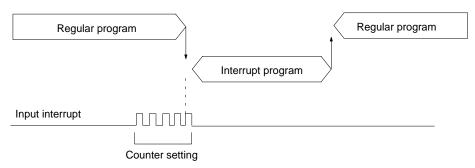
Input Interrupt Mode

If an input interrupt occurs, the regular program shuts down irrelevant of the cycle time, and the interrupt processing program is executed immediately.



Counter Mode

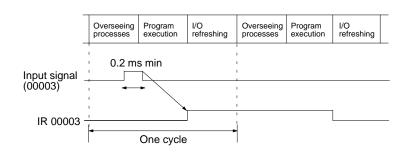
When the number of external signals counted at high speed reaches a specified number of counts, the regular program shuts down, and the interrupt processing program is executed at fixed counts. The count can be set between 0 and 65535.



■ Quick-response Inputs

There are two quick-response inputs for the CPM1A 10-point I/O CPU and four for the 20-, 30-, and 40-point I/O CPU (shared with the interrupt inputs). Since an internal buffer is provided, the quick-response input function can even detect signals modified within one cycle.

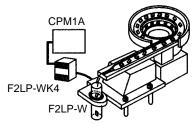
CPU	Input no.	Minimum input pulse width
10-point I/O CPU	00003 to 00004	0.2 ms
20-point, 30-point, 40-point I/O CPU	00003 to 00006	



Application Example:

Calculating the Number of Chips

The metal sensor counts the number of parts that have passed. Steady counting can be achieved even when the input-ON time is short.

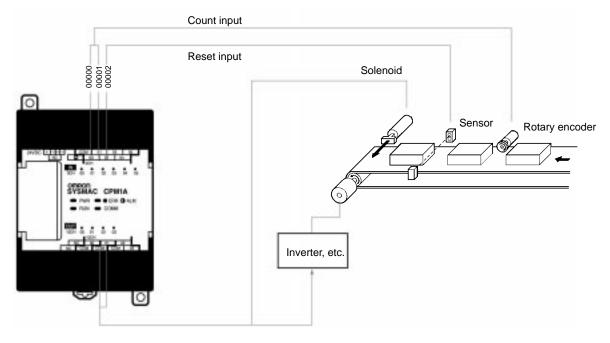


■ High-speed Counter

The CPM1A has a high-speed counter function that can be used in the incrementing and up/down mode. Using this function together with the input interrupts enables zone comparison control or target value control irrelevant of the cycle time.

	Item	Incrementing mode	Up/Down mode
Input no.	00000	Count input	A-phase input
	00001		B-phase input
	00002	Reset input	Z-phase input
Input method		Single-phase input	Phase-difference, 4× inputs
Count frequer	псу	5.0 kHz	2.5 kHz
Count range		0 to 65535	-32767 to 32767

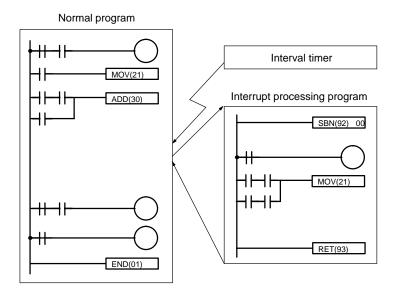
Note: When using in the incrementing mode, the input 00001 can be used as an input contact.



■ Interval Timer Interrupts

The CPM1A has one interval timer. The interval timer shuts down the regular program irrelevant of the point in the cycle once the time is up, and immediately executes an interrupt processing program. Interval timers are used in the following two modes.

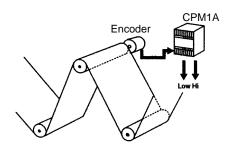
Item	One-shot mode	Scheduled interrupt mode
Operation	An interrupt is executed only once when the time is up.	Interrupts are executed repeatedly at fixed periods.
Setting time	0.5 ms to 319,968 ms (0.1-ms units)	



Application Example:

Computing the Sheet Speed

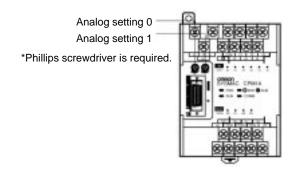
The number of pulse inputs is computed in the interrupt mode at a fixed time to calculate the speed.



Analog Setting

The CPM1A contains two analog setting controls that can be used for a broad range of analog timer and counter settings. Turning the setting control stores values of 0 to 200 (BCD data) in the SR area.

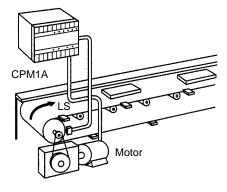
Analog setting	Storage area	Setting value (BCD)
Analog setting 0	SR 250	0000 to 0200
Analog setting 1	SR 251	



Application Example:

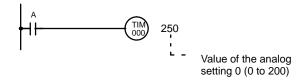
Tact Operation Control of Conveyor Lines

A conveyor can be stopped temporarily as required for assembly processes. When the timer function and limit switches are used in a combination, conveyors can be stopped for a fixed time or can be run at a constant speed for a fixed distance. Fine adjustment of the stopping time can be easily done by using the analog setting controls.

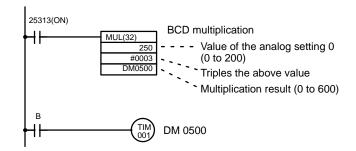


Program Example

1. Analog timer for 0.0 to 20.0 seconds



2. Analog timer for 0.0 to 60.0 seconds



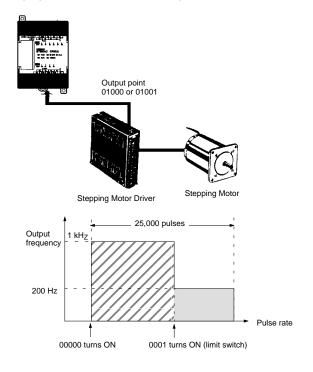
■ Pulse Output Function

The CPM1A with transistor output has a function that is capable of outputting a pulse of up to 2 kHz.

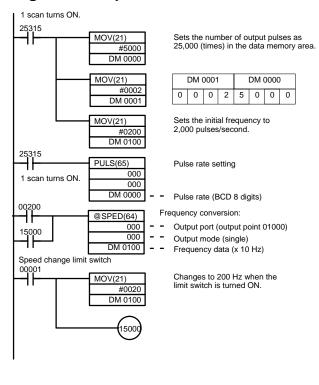
When used in combination with a Stepping Driver or Servodriver, positioning can be easily performed.

Application Example

Changing the speed of the Stepping Motor.



Program Example

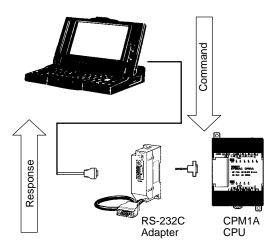


■ Communications

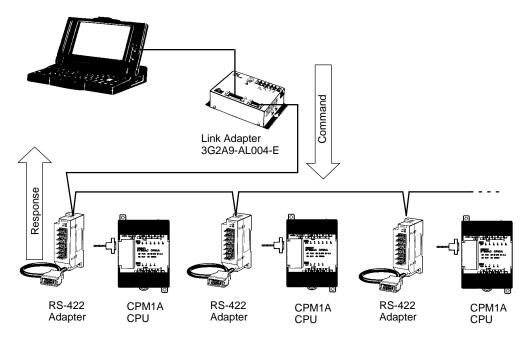
Host Link Communications

CPM1A host link communications consist of interactive procedures whereby the CPM1A returns a response to a command sent from the IBM PC/AT or compatible computer. These communications allow the IBM PC/AT or compatible computer to read and write in the CPM1A's I/O Areas and Data Memory Areas as well as in areas containing the status of various settings.

1:1 Host Link Communications



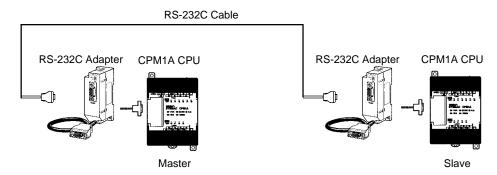
1:n Host Link Communications

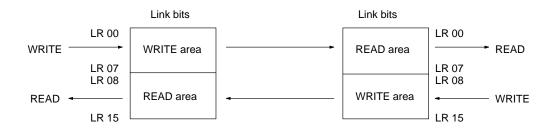


1:1 Links

With a 1:1 link, two CPM1As or a CPM1A and CQM1 or C200H are connected 1:1 with one side as the Master and the other as the Slave to provide an I/O link of a maximum of 256 points (LR 0000 to LR 1515).

Example of a 1:1 Link between CPM1As



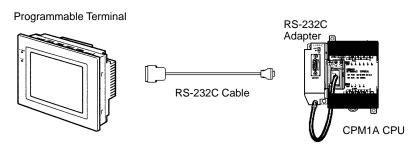


Limitations of the CPM1A 1:1 Link

CPM1A I/O links are limited to 16 words (LR 00 to LR 15). Therefore, use these 16 words (LR 00 to LR 15) on the CQM1 or C200H□ side when forming 1:1 links with a CQM1 or C200H□.

NT Links

High-speed communications can be achieved by providing a direct access through the use of the NT Link between the CPM1A and Programmable Terminal.



Summary of Programming Instructions

■ Function Code Chart

Table sym- bols	Details	Key operations for specifying program- ming instructions
0	Allocated to instruction keys on the Program- ming Console. These need not be specified with function codes.	
Code	Special instructions specified with function codes.	FUN - Code - WRITE

■ Differentiated Instructions

Differentiated instructions can sometimes be used for CPM1A special instructions. Instructions marked with (@) in the mnemonics can also be used as differentiated instructions. Here the input rise time (shift from OFF to ON) is used to execute the instruction in just one cycle.

To specify an instruction, press the NOT Key after the function code.

Example: Specifying the @MOV (21) instruction



■ Sequence Instructions

Sequence Input Instructions

Instruction	Mnemonic	Code	Function
LOAD	LD	0	Connects an NO condition to the left bus bar.
LOAD NOT	LD NOT	0	Connects an NC condition to the left bus bar.
AND	AND	0	Connects an NO condition in series with the previous condition.
AND NOT	AND NOT	0	Connects an NC condition in series with the previous condition.
OR	OR	0	Connects an NO condition in parallel with the previous condition.
OR NOT	OR NOT	0	Connects an NC condition in parallel with the previous condition.
AND LOAD	AND LD	0	Connects two instruction blocks in series.
OR LOAD	OR LD	0	Connects two instruction blocks in parallel.

Note: O: Instruction keys allocated to the Programming Console.

Sequence Output Instructions

Instruction	Mnemonic	Code	Function
OUTPUT	OUT	0	Outputs the result of logic to a bit.
OUT NOT	OUT NOT	0	Reverses and outputs the result of logic to a bit.
SET	SET	0	Force sets (ON) a bit.
RESET	RSET	0	Force resets (OFF) a bit.
KEEP	KEEP	11	Maintains the status of the designated bit.
DIFFER- ENTIATE UP	DIFU	13	Turns ON a bit for one cycle when the execution condition goes from OFF to ON.
DIFFER- ENTIATE DOWN	DIFD	14	Turns ON a bit for one cycle when the execution condition goes from ON to OFF.

Note: O: Instruction keys allocated to the Programming Console.

Sequence Control Instructions

Instruction	Mnemonic	Code	Function
NO OPERA- TION	NOP	00	
END	END	01	Required at the end of the program.
INTER- LOCK	IL	02	If the execution condition for IL(02) is OFF, all outputs are turned OFF and all timer PVs reset between IL(02) and the next ILC(03).
INTER- LOCK CLEAR	ILC	03	ILC(03) indicates the end of an interlock (beginning at IL(02)).
JUMP	JMP	04	If the execution condition for JMP(04) is ON, all instructions between JMP(04) and JME(05) are treated as NOP(00).
JUMP END	JME	05	JME(05) indicates the end of a jump (beginning at JMP(04)).

■ Timer/Counter Instructions

Instruction	Mnemonic	Code	Function
TIMER	TIM	0	An ON-delay (decrementing) timer.
COUNTER	CNT	0	A decrementing counter.
RE- VERSIBLE COUNTER	CNTR	12	Increases or decreases PV by one.
HIGH- SPEED TIMER	TIMH	15	A high-speed, ON-delay (decrementing) timer.

Note: O: Instruction keys allocated to the Programming Console.

■ Step Instructions

Instruction	Mnemonic	Code	Function
STEP DE- FINE	STEP	08	Defines the start of a new step and resets the previous step when used with a control bit. Defines the end of step execu- tion when used without a con- trol bit.
STEP START	SNXT	09	Starts the execution of the step when used with a control bit.

■ Increment/Decrement Instructions

Instruction	Mnemonic	Code	Function
INCRE- MENT	(@)INC	38	Increments the BCD content of the specified word by 1.
DECRE- MENT	(@)DEC	39	Decrements the BCD content of the specified word by 1.

■ BCD/Binary Calculation Instructions

Instruction	Mnemonic	Code	Function
BCD ADD	(@)ADD	30	Adds the content of a word (or a constant).
BCD SUB- TRACT	(@)SUB	31	Subtracts the content of a word (or constant) and CY from the content of a word (or constant).
BCD MUL- TIPLY	(@)MUL	32	Multiplies the contents of two words (or constants).
BCD DI- VIDE	(@)DIV	33	Divides the content of a word (or constant) by the content of a word (or constant).
BINARY ADD	(@)ADB	50	Adds the contents of two words (or constants) and CY.
BINARY SUB- TRACT	(@)SBB	51	Subtracts the content of a word (or constant) and CY from the content of a word (or constant).
BINARY MULTIPLY	(@)MLB	52	Multiplies the contents of two words (or constants).
BINARY DIVIDE	(@)DVB	53	Divides the content of a word (or constant) by the content of a word and obtains the result and remainder.
DOUBLE BCD ADD	(@)ADDL	54	Add the 8-digit BCD contents of two pairs of words (or constants) and CY.
DOUBLE BCD SUB- TRACT	(@)SUBL	55	Subtracts the 8-digit BCD contents of a pair of words (or constants) and CY from the 8-digit BCD contents of a pair of words (or constants).
DOUBLE BCD MUL- TIPLY	(@)MULL	56	Multiplies the 8-digit BCD contents of two pairs of words (or constants).
DOUBLE BCD DI- VIDE	(@)DIVL	57	Divides the 8-digit BCD contents of a pair of words (or constants) by the 8-digit BCD contents of a pair of words (or constants).

■ Data Conversion Instructions

Instruction	Mnemonic	Code	Function
BCD TO BINARY	(@)BIN	23	Converts 4-digit BCD data to 4-digit binary data.
BINARY TO BCD	(@)BCD	24	Converts 4-digit binary data to 4-digit BCD data.
4 TO 16 DECODER	(@)MLPX	76	Takes the hexadecimal value of the specified digit(s) in a word and turns ON the corresponding bit in a word(s).
16 TO 4 DECODER	(@)DMPX	77	Identifies the highest ON bit in the specified word(s) and moves the hexadecimal value(s) corresponding to its location to the specified digit(s) in a word.
ASCII CODE CONVERT	(@)ASC	86	Converts the designated digit(s) of a word into the equivalent 8-bit ASCII code.

Data Comparison Instructions

Instruction	Mnemonic	Code	Function
COMPARE	CMP	20	Compares two four-digit hexa- decimal values.
DOUBLE COMPARE	CMPL	60	Compares two eight-digit hexadecimal values.
BLOCK COMPARE	(@)BCMP	68	Judges whether the value of a word is within 16 ranges (defined by lower and upper limits).
TABLE COMPARE	(@)TCMP	85	Compares the value of a word to 16 consecutive words.

■ Data Movement Instructions

Instruction	Mnemonic	Code	Function
MOVE	(@)MOV	21	Copies a constant or the content of a word to a word.
MOVE NOT	(@)MVN	22	Copies the complement of a constant or the content of a word to a word.
BLOCK TRANS- FER	(@)XFER	70	Copies the content of a block of up to 1,000 consecutive words to a block of consecutive words.
BLOCK SET	(@)BSET	71	Copies the content of a word to a block of consecutive words.
DATA EX- CHANGE	(@)XCHG	73	Exchanges the content of two words.
SINGLE WORD DIS- TRIBUTE	(@)DIST	80	Copies the content of a word to a word (whose address is determined by adding an offset to a word address).
DATA COL- LECT	(@)COLL	81	Copies the content of a word (whose address is determined by adding an offset to a word address) to a word.
MOVE BIT	(@)MOVB	82	Copies the specified bit from one word to the specified bit of a word.
MOVE DIGIT	(@)MOVD	83	Copies the specified digits (4-bit units) from a word to the specified digits of a word.

■ Logic Instructions

Instruction	Mnemonic	Code	Function
COMPLE- MENT	(@)COM	29	Turns OFF all ON bits and turns ON all OFF bits in the specified word.
LOGICAL AND	(@)ANDW	34	Logically ANDs the corresponding bits of two words (or constants).
LOGICAL OR	(@)ORW	35	Logically ORs the corresponding bits of two words (or constants).
EXCLU- SIVE OR	(@)XORW	36	Exclusively ORs the corresponding bits of two words (or constants).
EXCLU- SIVE NOR	(@)XNRW	37	Exclusively NORs the corresponding bits of two words (or constants).

■ Shift Instructions

Instruction	Mnemonic	Code	Function
SHIFT REGISTER	SFT	○/10	Copies the specified bit (0 or 1) into the rightmost bit of a shift register and shifts the other bits one bit to the left.
WORD SHIFT	(@)WSFT	16	Creates a multiple-word shift register that shifts data to the left in one-word units.
ASYNCH- RONOUS SHIFT REGISTER	(@)ASFT	17	Creates a shift register that ex- changes the contents of adja- cent words when one is zero and the other is not.
ARITH- METIC SHIFT LEFT	(@)ASL	25	Shifts a 0 into bit 00 of the specified word and shifts the other bits one bit to the left.
ARITH- METIC SHIFT RIGHT	(@)ASR	26	Shifts a 0 into bit 15 of the specified word and shifts the other bits one bit to the right.
ROTATE LEFT	(@)ROL	27	Moves the content of CY into bit 00 of the specified word, shifts the other bits one bit to the left, and moves bit 15 to CY.
ROTATE RIGHT	(@)ROR	28	Moves the content of CY into bit 15 of the specified word, shifts the other bits one bit to the right, and moves bit 00 to CY.
ONE DIGIT SHIFT LEFT	(@)SLD	74	Shifts a 0 into the rightmost digit (4-bit unit) of the shift register and shifts the other digits one digit to the left.
ONE DIGIT SHIFT RIGHT	(@)SRD	75	Shifts a 0 into the leftmost digit (4-bit unit) of the shift register and shifts the other digits one digit to the right.
RE- VERSIBLE SHIFT REGISTER	(@)SFTR	84	Creates a single or multiple- word shift register that can shift data to the left or right.

Note: O: Instruction keys allocated to the Programming Console.

■ Special Calculation Instruction

Instruction	Mnemonic	Code	Function
BIT COUNTER	(@)BCNT		Counts the total number of bits that are ON in the specified block of words.

■ Subroutine Instructions

Instruction	Mnemonic	Code	Function
SUBROU- TINE EN- TER	(@)SBS	91	Executes a subroutine in the main program.
SUBROU- TINE ENTRY	SBN	92	Marks the beginning of a sub- routine program.
SUBROU- TINE RE- TURN	RET	93	Marks the end of a subroutine program.
MACRO	MCRO	99	Calls and executes the speci- fied subroutine, substituting the specified input and output words for the input and output words in the subroutine.

■ Interrupt Control Instructions

Instruction	Mnemonic	Code	Function
INTERVAL TIMER	(@)STIM	69	Controls interval timers used to perform scheduled interrupts.
INTER- RUPT CONTROL	(@)INT	89	Performs interrupt control, such as masking and unmask- ing the interrupt bits for I/O in- terrupts.

■ Peripheral Device Control Instructions

I/O Unit Instructions

Instruction	Mnemonic	Code	Function
7-SEG- MENT DE- CODER	(@)SDEC	78	Converts the designated digit(s) of a word into an 8-bit, 7-segment display code.
I/O RE- FRESH	(@)IORF	97	Refreshes the specified I/O word.

Display Instruction

Instruction	Mnemonic	Code	Function
MESSAGE	(@)MSG	46	Reads up to 8 words of ASCII code (16 characters) from memory and displays the message on the Programming Console or other Peripheral Device.

High-speed Counter Control Instructions

Instruction	Mnemonic	Code	Function
MODE CONTROL	(@)INI	61	Starts and stops counter op- eration, compares and changes counter PVs, and stops pulse output.
PV READ	(@)PRV	62	Reads counter PVs and status data.
COMPARE TABLE LOAD	(@)CTBL	63	Compares counter PVs and generates a direct table or starts operation.

Pulse Output Control Instructions

Instruction	Mnemonic	Code	Function
SPEED OUTPUT	(@)SPED	64	Outputs pulses at the specified frequency. The output frequency can be changed while the pulses are being output.
SET PULSES	(@)PULS	65	Outputs the specified number of pulses at the specified frequency. The pulse output cannot be stopped until the specified number of pulses have been output.

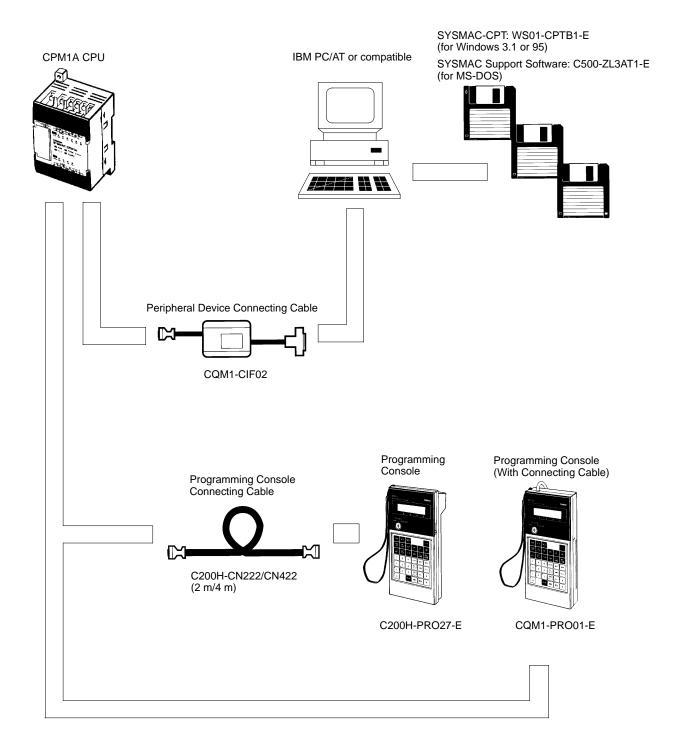
■ Damage Diagnosis Instructions

Instruction	Mnemonic	Code	Function
FAILURE ALARM	(@)FAL	06	Generates a non-fatal error when executed. The Error/ Alarm indicator flashes and the CPU continues operating.
SEVERE FAILURE ALARM	FALS	07	Generates a fatal error when executed. The Error/Alarm indicator lights and the CPU stops operating.

■ Special System Instructions

Instruction	Mnemonic	Code	Function
SET CARRY	(@)STC	40	Sets Carry Flag 25504 to 1.
CLEAR CARRY	(@)CLC	41	Sets Carry Flag 25504 to 0.

Peripheral Devices



Standard Models

■ CPU

Name	Power supply	Output method	Input points	Output points	Model	Standards
10-point I/O	AC power supply	Relay output	6 points	4 points	CPM1A-10CDR-A	U, C, N, L
	DC power supply	Relay output			CPM1A-10CDR-D	
		Transistor output (sink type)			CPM1A-10CDT-D	U, C, CE
		Transistor output (source type)			CPM1A-10CDT1-D	
20-point I/O	AC power supply	Relay output	12 points	8 points	CPM1A-20CDR-A	U, C, N, L
	DC power supply	Relay output			CPM1A-20CDR-D	
		Transistor output (sink type)			CPM1A-20CDT-D	U, C, CE
		Transistor output (source type)			CPM1A-20CDT1-D	
30-point I/O	AC power supply	Relay output	18 points	12 points	CPM1A-30CDR-A	U, C, N, L
	DC power supply	Relay output			CPM1A-30CDR-D	
		Transistor output (sink type)			CPM1A-30CDT-D	U, C, CE
		Transistor output (source type)			CPM1A-30CDT1-D	
40-point I/O	AC power supply	Relay output	24 points	16 points	CPM1A-40CDR-A	U, C, N, L
	DC power supply	Relay output			CPM1A-40CDR-D]
		Transistor output (sink type)			CPM1A-40CDT-D	U, C, CE
		Transistor output (source type)			CPM1A-40CDT1-D	

■ Expansion I/O Unit

Expansion Unit	Max. number of Units	Output type	Inputs	Outputs	N	<i>l</i> lodel	Standards
Expansion I/O	3 Units	Relay	12	8	Ø	CPM1A-20EDR1	U, C, CE
Units	max. (See	Transistor (sinking)			Eligina -	CPM1A-20EDT	U, C, CE
	note.)	Transistor (sourcing)			E	CPM1A-20EDT1	U, C, CE
	,		8		(a) (b) (c) (c) (c) (c) (c) (c) (c) (c) (c) (c	CPM1A-8ED	U, C, CE
		Relay		8	Hit	CPM1A-8ER	U, C, CE
		Transistor (sinking)		8	1111	CPM1A-8ET	U, C, CE
		Transistor (sourcing)			A III	CPM1A-8ET1	
Analog I/O Unit	3 Units max. (See note.)	Analog	2	1		CPM1A-MAD01	U, C, CE
CompoBus/S I/O Link Unit	3 Units max. (See note.)		I/O Link of and 8 outp	8 input bits ut bits		CPM1A-SRT21	U, C, CE

Note: Only one Expansion Unit can be connected if an NT-AL001 Adapter is connected to the CPU Unit's RS-232C port.

Standard Models

■ RS-232C Adapter, RS-422 Adapter, Connecting Cable, Link Adapter

Name	Function	Model	Standards
RS-232C Adapter	Converts peripheral port levels.	CPM1-CIF01	U, C, N, L, CE
RS-422 Adapter		CPM1-CIF11	
Connecting Cable	3.3-m cable used to connect IBM PC/AT or compatible personal computers.	CQM1-CIF02	U, C, N, L, CE
Link Adapter	Converts RS-232C and RS-422 levels.	3G2A9-AL004-E	

■ Programming Console

Name		Function	Model	Standards	
Programming Console		With a 2-m cable	CQM1-PRO01-E	U, C, N, CE	
			C200H-PRO27-E	U, C, CE	
		2-m Connecting Cable for C200H-PRO27-E	C200H-CN222		
		4-m Connecting Cable for C200H-PRO27-E	C200H-CN422		

■ Programming Software

Name	Operating system	Operating environment	Model
SYSMAC-CPT	Windows 3.1 or 95	Used in IBM PC/AT or compatible personal computers (i486DX/Pentium)	WS01-CPTB1-E
SYSMAC Support Software	MS-DOS Ver. 5.0 or later	Used in IBM PC/AT or compatible personal computers (i386/i486/Pentium)	C500-ZL3AT1-E



OMRON Corporation

Systems Components Division

66 Matsumoto Mishima-city, Shizuoka 411-8511

Japan Tel: (81)559-77-9633/Fax: (81)559-77-9097

Regional Headquarters

OMRON EUROPE B.V.

Wegalaan 67-69, NL-2132 JD Hoofddorp The Netherlands

Tel: (31)2356-81-300/Fax: (31)2356-81-388

OMRON ELECTRONICS, INC.

1 East Commerce Drive, Schaumburg, IL 60173 U.S.A.

Tel: (1)847-843-7900/Fax: (1)847-843-8568

OMRON ASIA PACIFIC PTE. LTD. 83 Clemenceau Avenue,

#11-01, UE Square,

Singapore 239920 Tel: (65)835-3011/Fax: (65)835-2711

Authorized Distributor:

