GBT-SCA

The **S**low **C**ontrol **A**dapter for the GBT system

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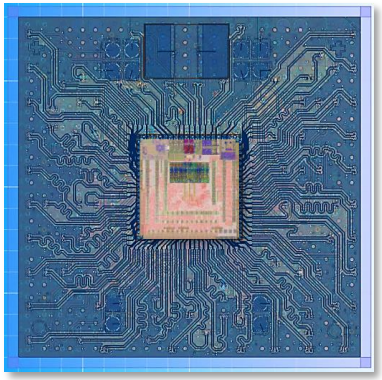
Outline:

- What the GBT-SCA is
- Interfaces and communication
- Prototypes testing status and results
- Practical information

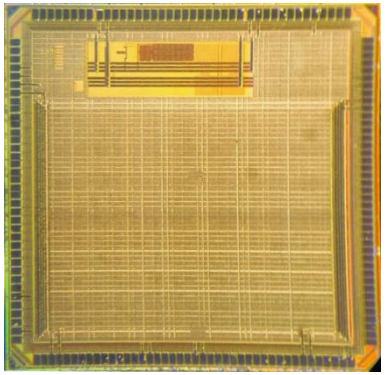
The GBT Chipset

- **GBTX:**
  - 4.8 Gb/s Transceiver
  - Manages the communications between the counting room and the frontend modules
- **GBT–SCA**
  - Slow Control Adapter
  - Experiment control and environment monitoring
- **GBTIA:**
  - 4.8 Gb/s Transimpedance Amplifier
  - Amplifies the weak photo-current detected by the PIN diode
- **GBLD:**
  - 4.8 Gb/s Laser Driver
  - Modulates laser current to achieve electro-optical conversion

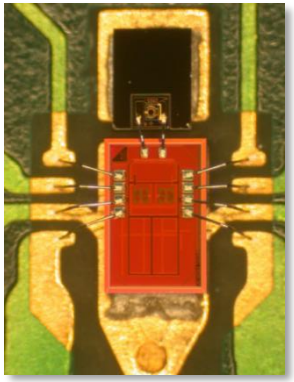
GBTX



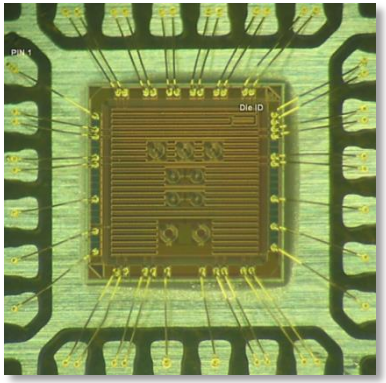
GBT-SCA



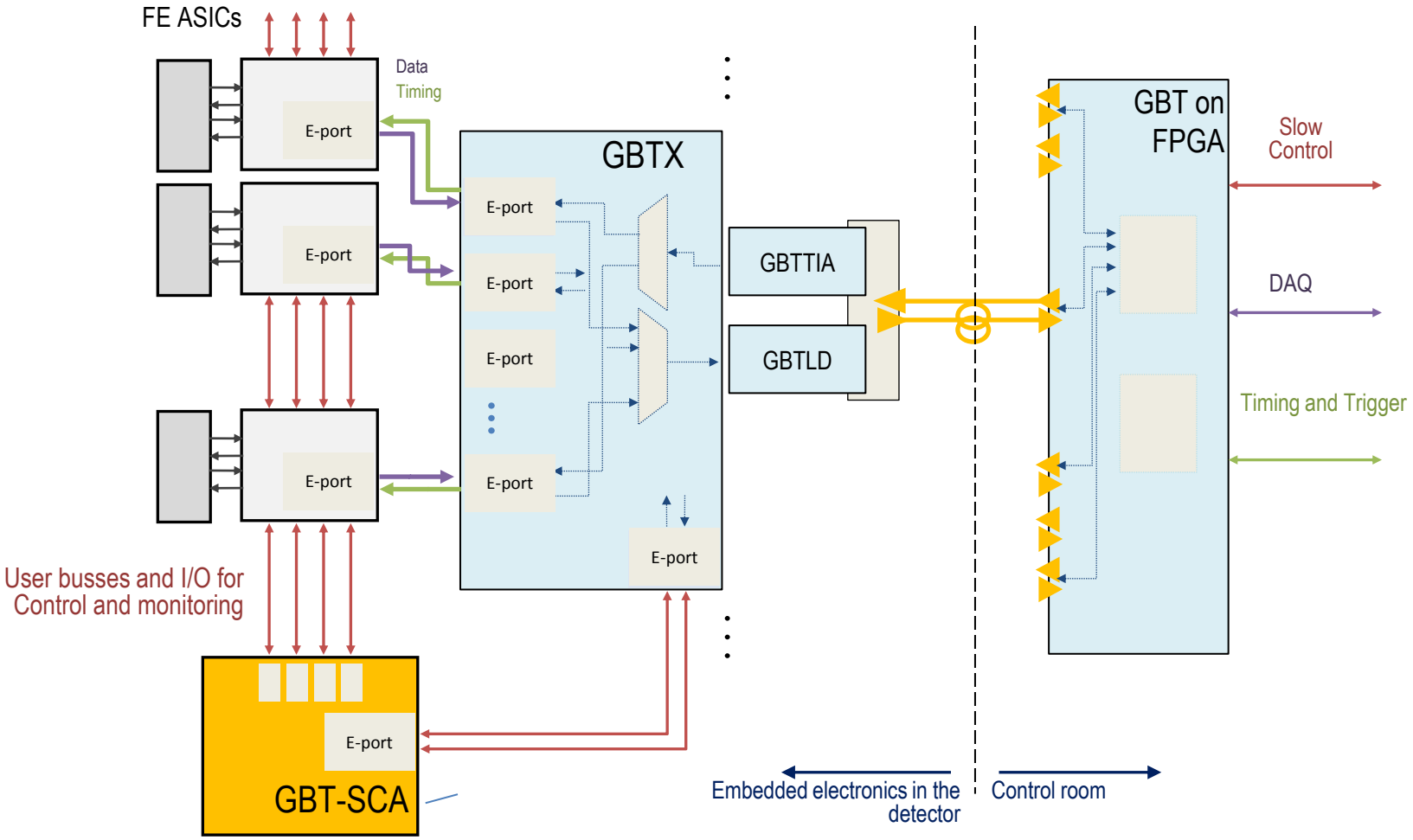
GBTIA



GBLD



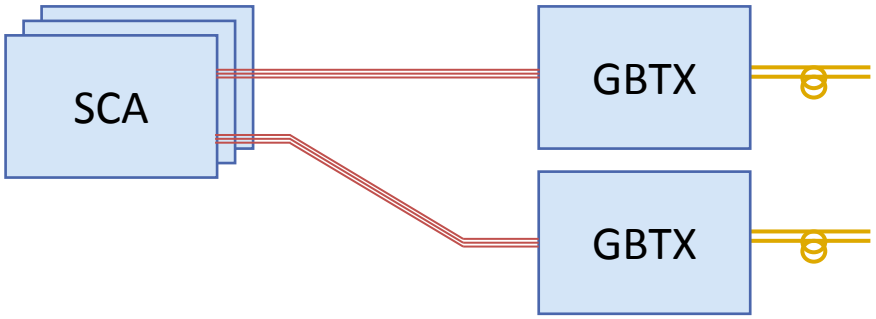
The SCA in the GBT system



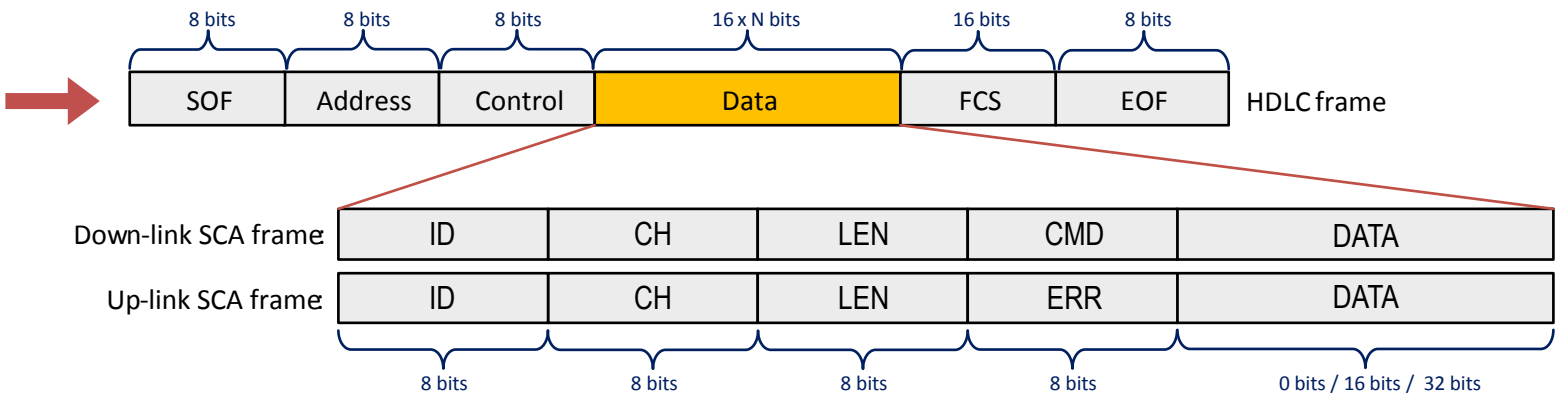
Communication

Successfully tested

- SCA ASIC can connect via an e-link to any e-port of the GBTX
- 40MHz double date rate (80 Mbps)
- Point-to-point network topology with fixed bandwidth allocated by the GBTX
- Double redundancy scheme allowing connection from two GBTX links.
  - Switching between masters requires a “CONNECT” command defined in the high-level communication protocol

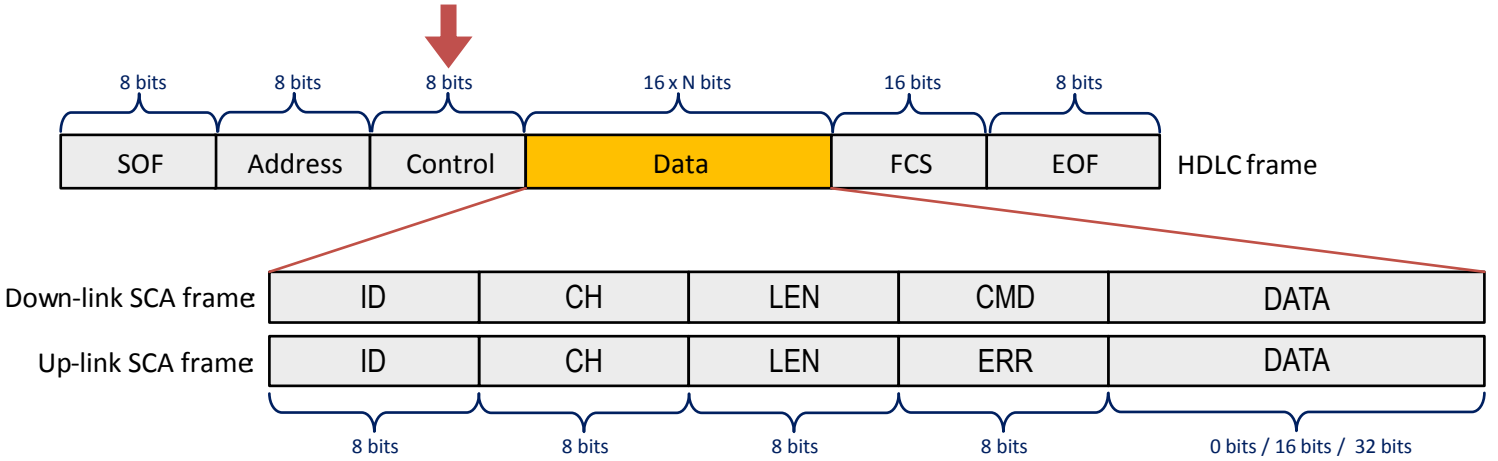


Communication protocol scheme



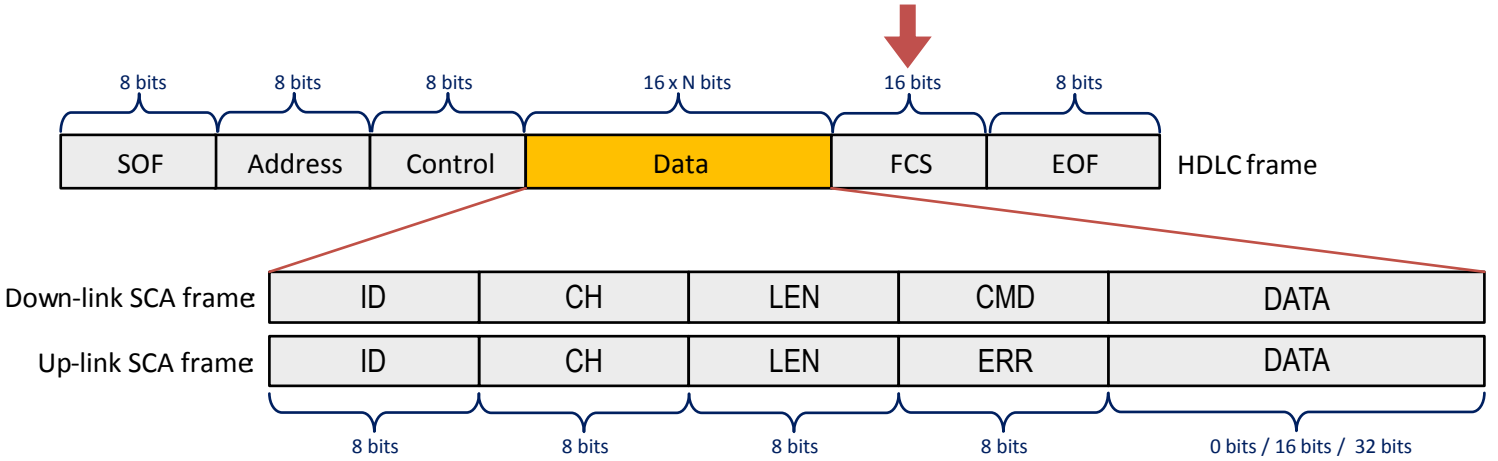
- The e-link ports implement a packet oriented full duplex transmission based on the HDLC standard (ISO/IEC 13239:2002)
  - Not deterministic!
- Bits within the frame are transmitted from the least significant to the most significant
- The frame delimiter is composed of six ‘1s’.
  The protocol assures that this combination is not found anywhere by stuffing a ‘0’ in any sequence of five consecutive ‘1’

Communication protocol scheme



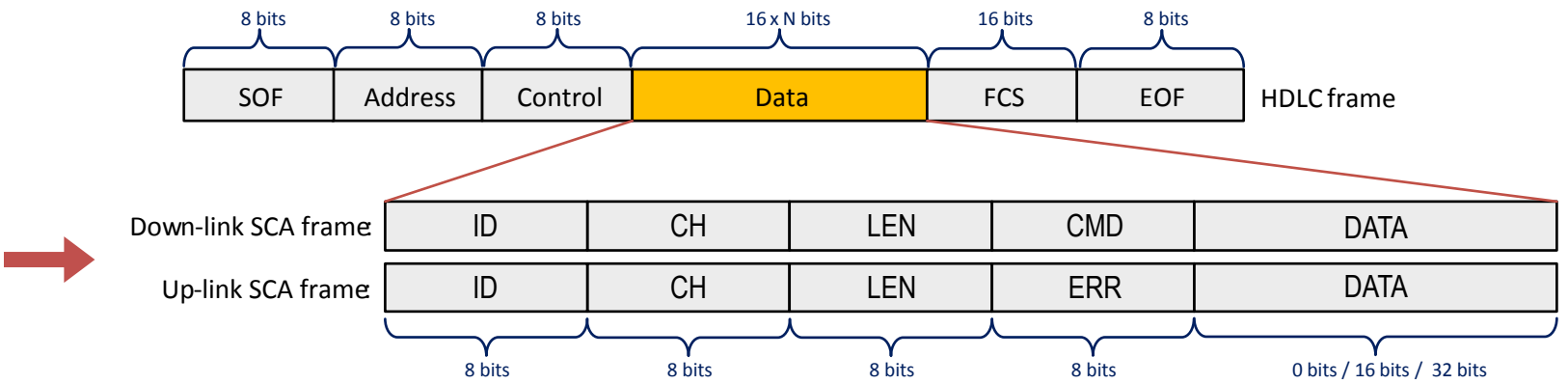
- The CONTROL field contains the frame sequence number of the currently transmitted frame and of the last correctly received frame to implement an acknowledgement handshake between the SCA and the control room electronics.
- The CONTROL field is also used to convey three supervisory level commands.
  - CONNECT To select the active interface between primary and auxiliary e-port
  - RESET To remotely reset the SCA chip
  - TEST Loopback mode for communication verification

Communication protocol scheme



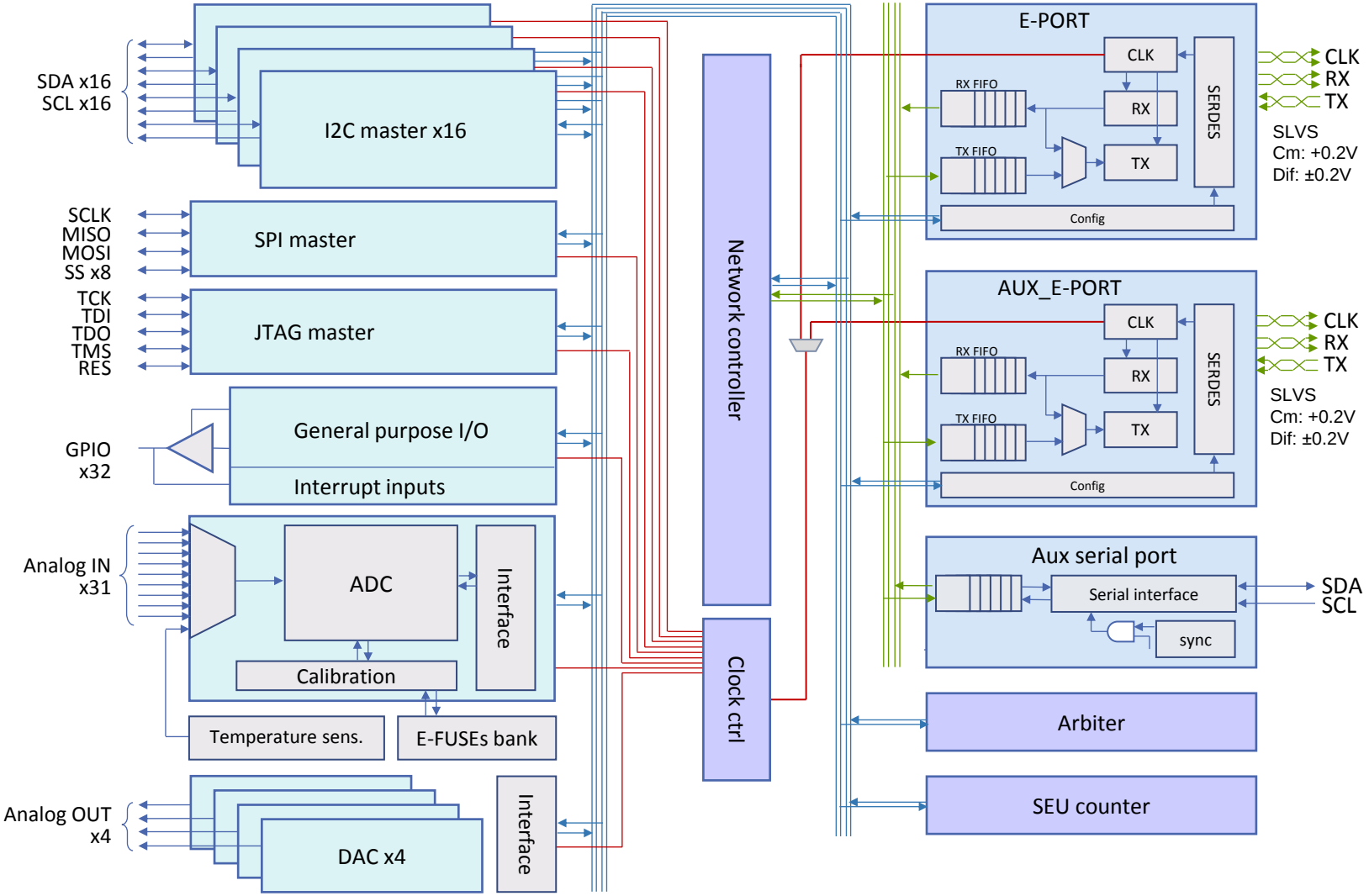
- The Frame Check Sequence (FCS field) is calculated over the address, control and information fields using a CCITT standard 16-bit CRC.

Communication protocol scheme



- Command oriented protocol to address the on-chip interface channels
  Bits within the field are transmitted from the least to the most significant bit
  - ID: Transaction identifier to associate 'request' packets to the corresponding 'replies'
    ID 0x00 and 0xff are reserved for spontaneously generated interrupt packets
  - CH: Define the destination channel interface in the SCA
  - CMD: indicates the operation to be performed
  - ERR: Indicate eventual error conditions encountered in the execution
  - DATA: Is a command dependent field whose length is defined by the LEN qualifier field

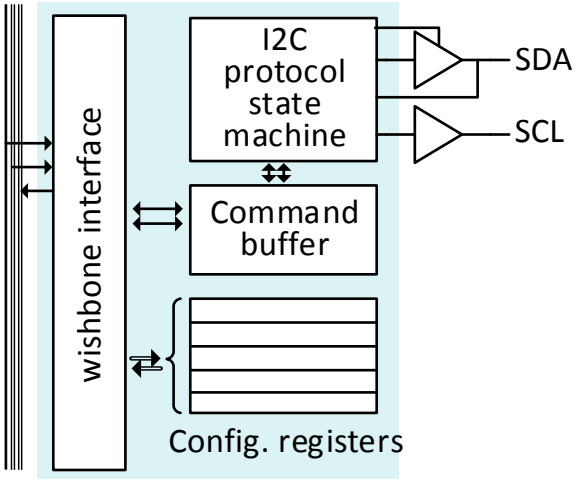
The GBT-SCA architecture



I^2C master

Successfully tested

- 16 independent I^2C master serial bus channels individually programmable.
- Data transfer rates from 100KHz to 1MHz.
- Implement 7-bits and 10-bits addressing standard.
- Read, Write and Read-Modify-Write operations
- Single-byte and multi-byte modes (up to 16)
- Reply packet return user data and status flags.

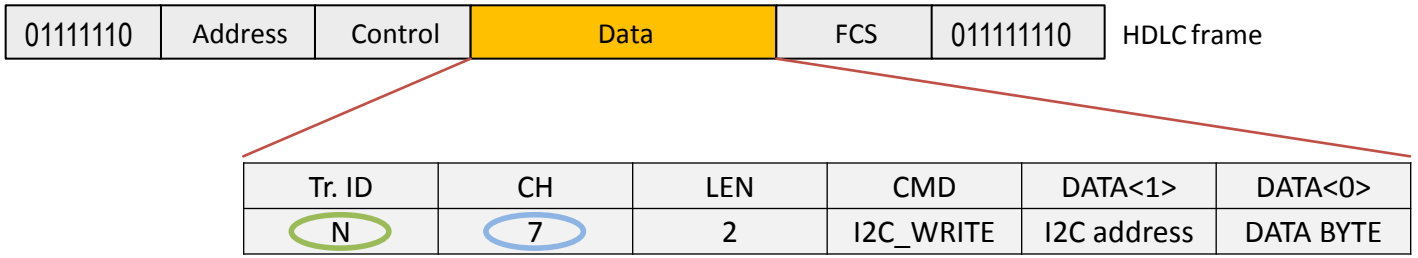


- SCL lines use digital IOs pads with 4mA drive strength configured as output.
- SDA lines use digital IOs pads with 4mA drive strength configured as bidirectional forcing only the ‘0’ value on the bus (open-drain emulated).
- Necessity of an external pull-up for the SDA lines.

Example of I^2C operation

- Supposing that you want to execute
  I2C single byte write operation , using the I2C master number 4, in 7bit addressing mode,

  The sent packet will be:



Tr. ID	CH	LEN	CMD	DATA<1>	DATA<0>
N	7	2	I2C_WRITE	I2C address	DATA BYTE

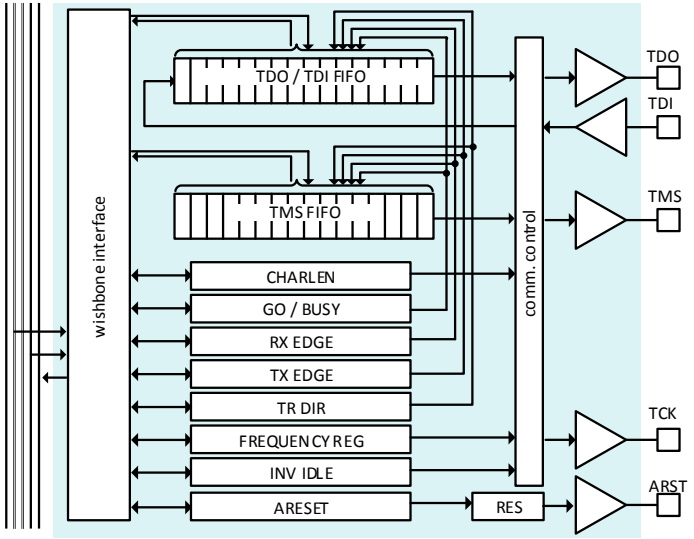
- And you will receive at the end of the operation:

Tr. ID	CH	LEN	ERR	DATA<1>	DATA<0>
N	7	2	0	Status (ACK)	-

JTAG master Interface

Successfully tested

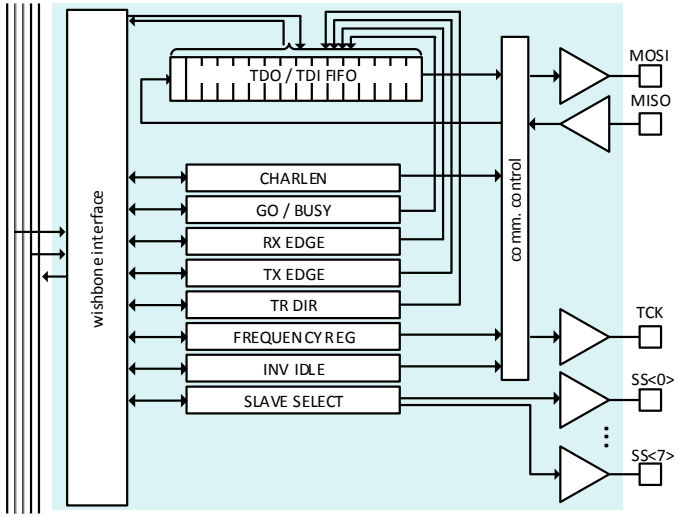
- Configurable bus transactions length up to 128-bit.
- Longer transactions are possible by segmenting on consecutive channel commands.
- Asynchronous reset line of configurable pulse width
- Bus frequency spans from 156KHz up to 20MHz in 128 user programmable steps.
- JTAG Tap controller state machine need to be implemented in the FPGA circuitry in the control room electronics.
- Use standard IBM 130 digital IOs library pads with 12mA drive strength.



SPI serial bus master Interface

Successfully tested

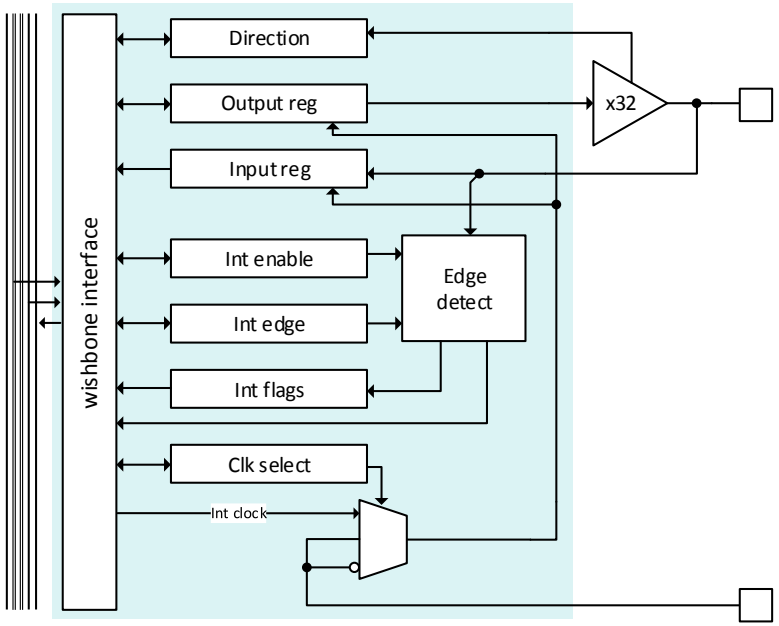
- Full duplex synchronous serial bus with configurable bus transactions up to 128-bit long.
- Longer transactions are possible by segmenting on consecutive channel commands.
- Supports all the standard SPI bus operating modes: 00, 01, 10 and 11.
- 8 individual slave select lines.
- Bus frequency spans from 156KHz up to 20MHz in 128 user programmable steps.
- Use standard IBM 130 digital IOs library pads with 12mA drive strength.



Parallel Interface Adapter

Successfully tested

- 32 General Purpose digital IO lines.
- Each line can be individually programmed as input or outpu.
- Input signals are sampled and registered at the raising or falling edges of the system clock or of an external strobe signal from the user's application connected on a dedicated input line.
- Any line configured as input can generate an interrupt request to the control room electronics.
- Use standard IBM 130 digital IOs library pads with 4mA drive strength.



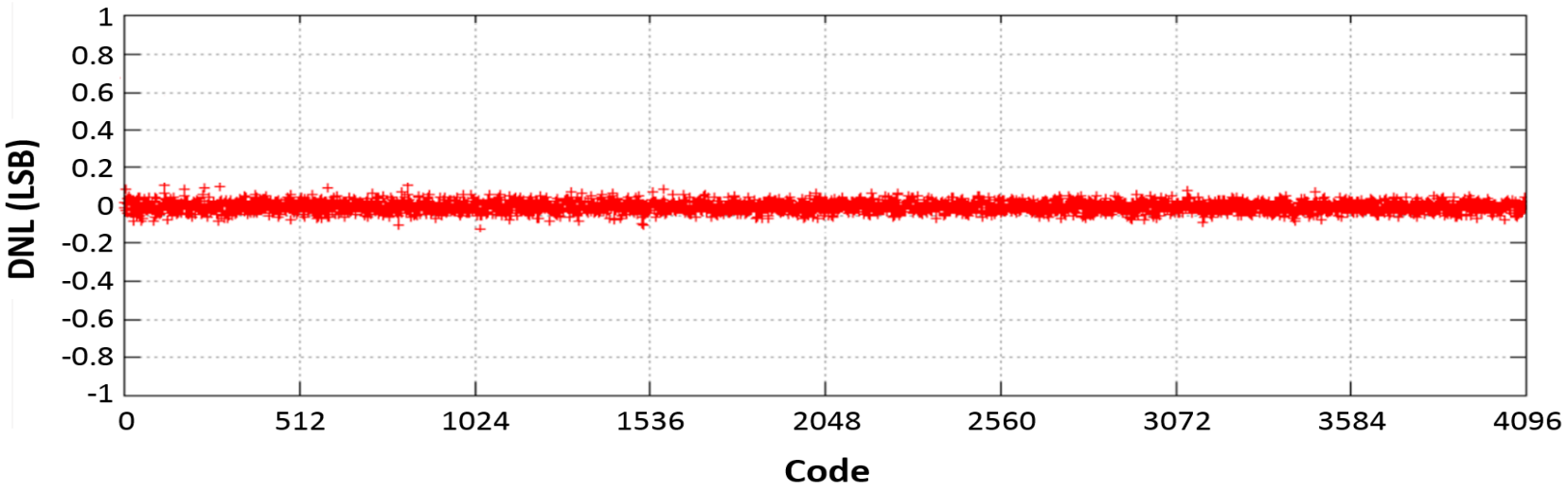
ADC

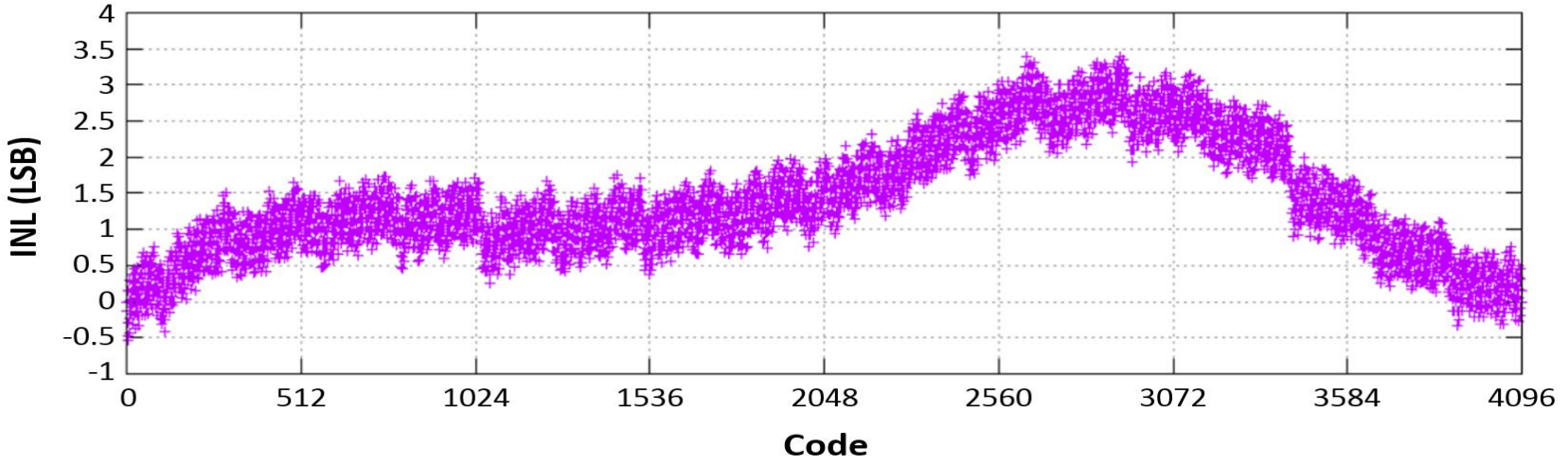
PRELIMINARY Test results

- **31 input** analog multiplexer connected to a **12-bit** analog to digital converter.
- One analog input internally connected to the embedded **temperature sensor**.
- All inputs feature a switchable **100uA current source** to facilitate the use of externally connected resistance temperature sensors (RTD).
- Time of conversion: **760uS** (compatible with the conversion requirements of slow varying parameters like detector leakage current and temperature, power supply voltages etc.)
- Analog input range: **0.0 V to 1.0 V**
- Implements internal **Gain correction** and **Offset cancellation**.
- The gain calibration coefficient is evaluated during the testing phase for every chip and stored on the on-chip e-fuse bank.
- The stored coefficient can be overridden to compensate for any possible drifts caused by the radiation environment.

ADC

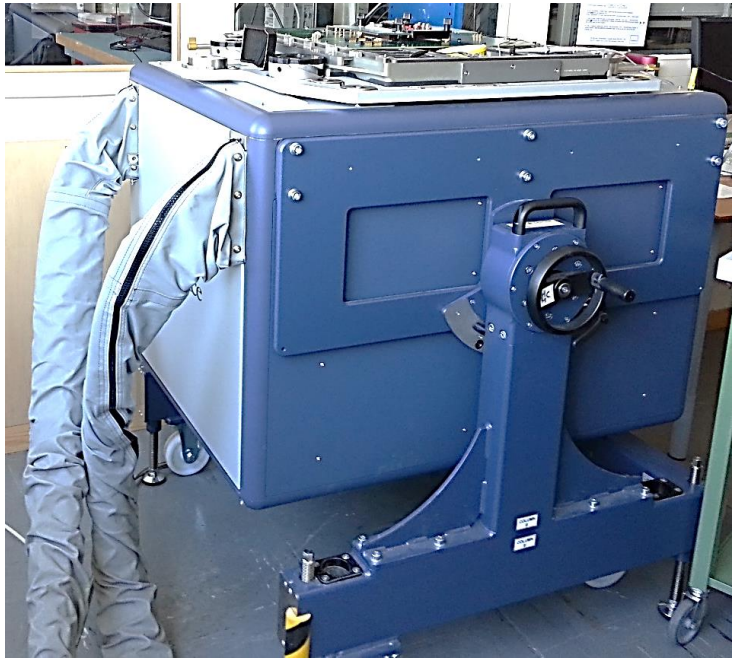
PRELIMINARY Test results





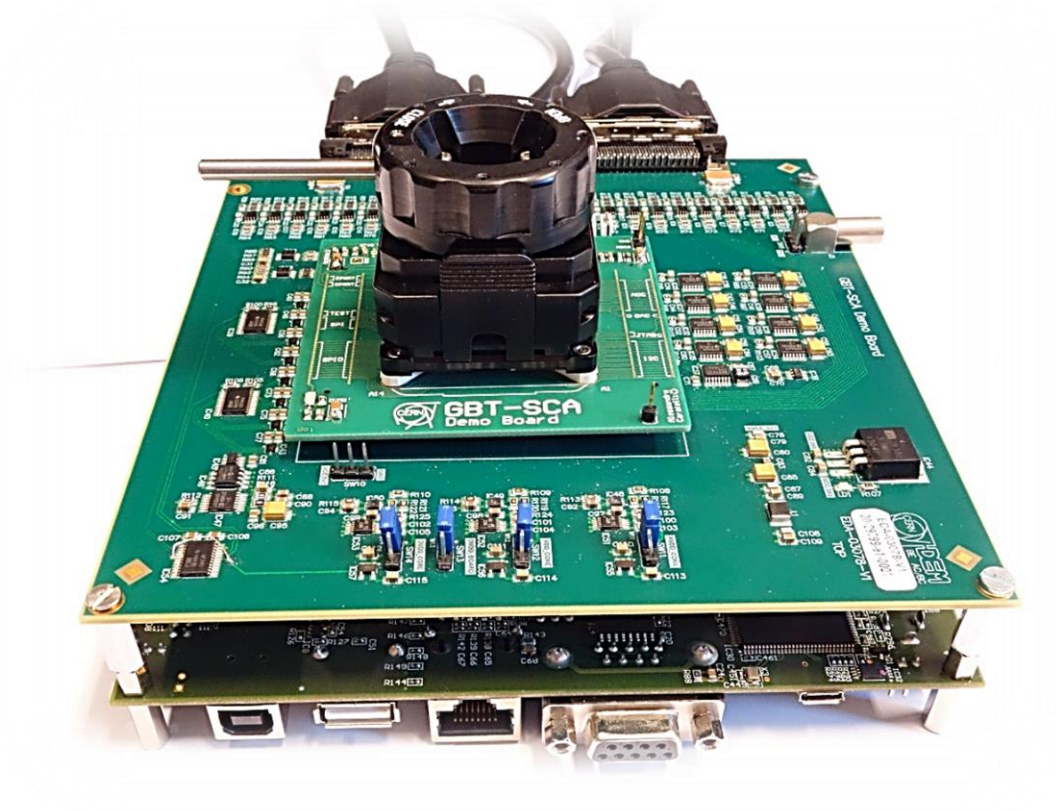
Prototype test bench

- For precise ADC and DAC characterization.
- For the final production testing



Stand-alone test-bench

- For functional verification (on bare-die)
- Irradiation performance testing (on bare-die and packaged parts)



Stand-alone test-bench

Software

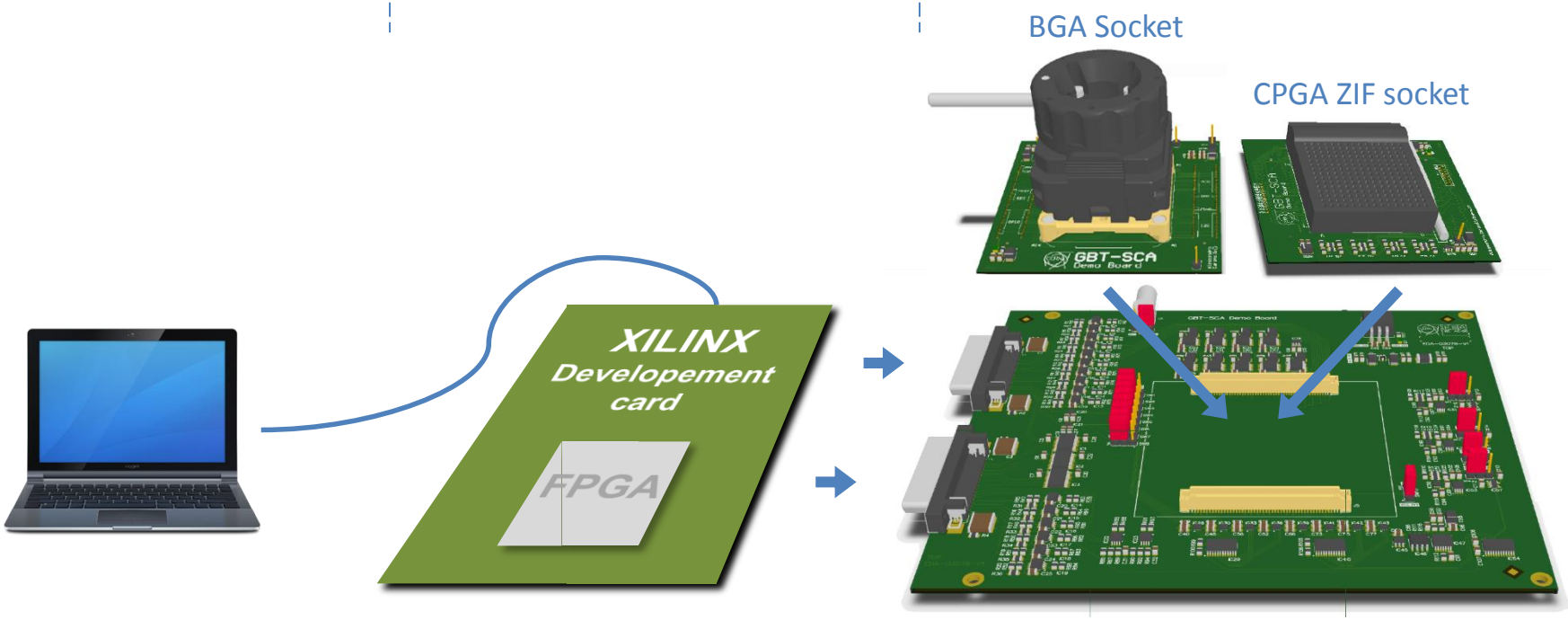
- Test routines *(python)*
- Interface *(python and C++)*
  - SCA access classes
  - PCB control classes
  - Slave interfaces classes

Firmware

- GBT-SCA communication handle
  - Tx and Rx FIFOs
  - HDLC encoding
- Slave interfaces
- PCB components control

Test Boards

- Interface board
  - Level translators
  - Voltage regulators
  - etc..
  - ADCs/DACs
  - Current monitors
- Load boards



Radiation Performances

Radiation tests will take place on the 20 April

- To address the **TID requirements**:
  - The SCA is implemented in a commercial 130 nm CMOS technology largely characterized for radiation tolerance
- To address the **SEUs requirements** :
  - The SCA adopt the Triple Modular Redundancy technique at the state machine level in the entire digital circuitry
  - The clock tree was also triplicated to mitigate the effects of SET.
  - The SCA SEUs robustness has been strongly verified at simulation level
- **SEUs tests** will take place on the April, 20th in Louvain-la-Neuve

Electrical characteristics

Standard Supplies by design:

- Digital supply voltage: 1.5 V
- Analog supply voltage: 1.5 V
- Periphery supply voltage: 1.5 V

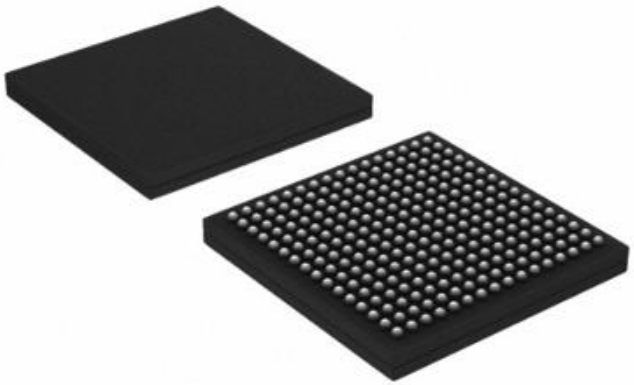
- The GBT-SCA digital functions have been successfully tested at 1.2V supply

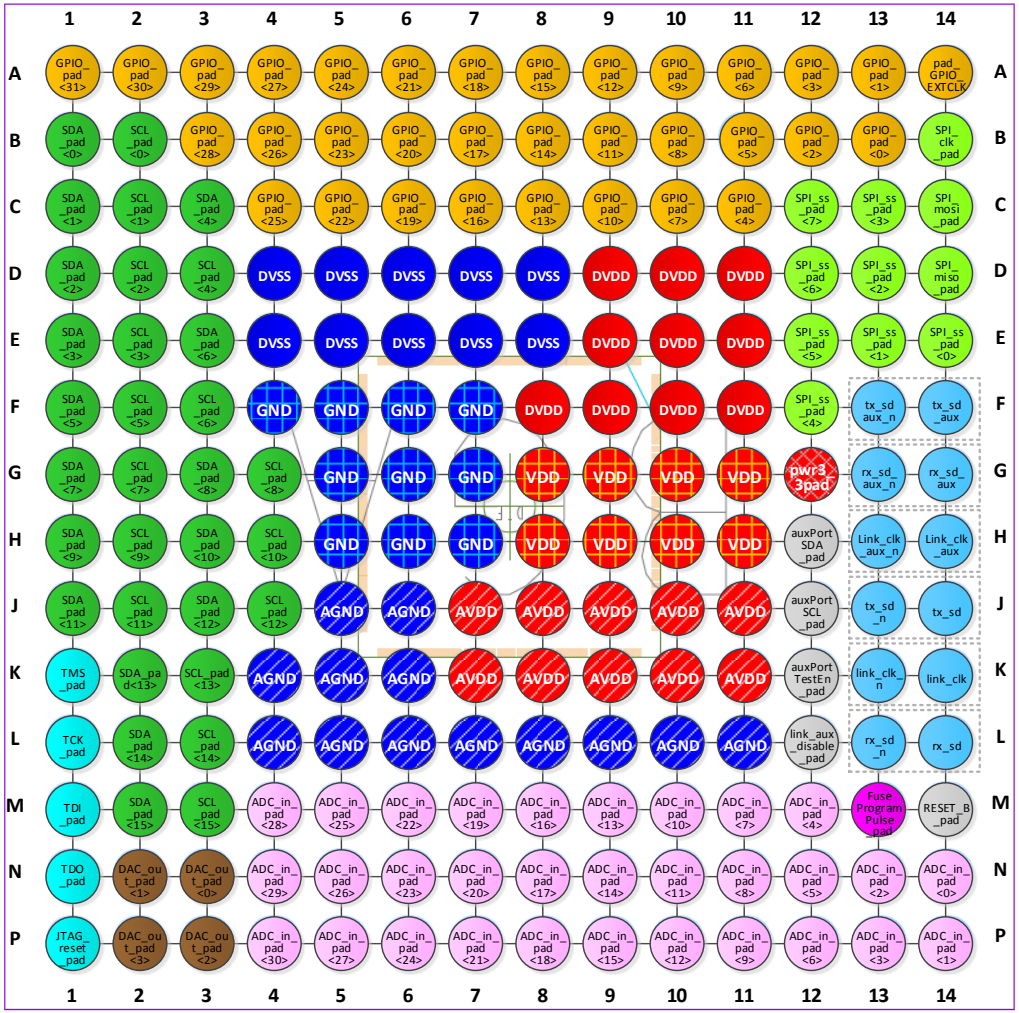
- ADC instead needs 1.5 V supply to correctly work

Packaging

Successfully tested

- Package: Low Profile Fine Pitch BGA (Chip Scale Package)
- Ball Pitch: 0.8 mm
- Size: 12 x 12 mm
- Height: 1.7 mm
- Pin count: 196





Others information

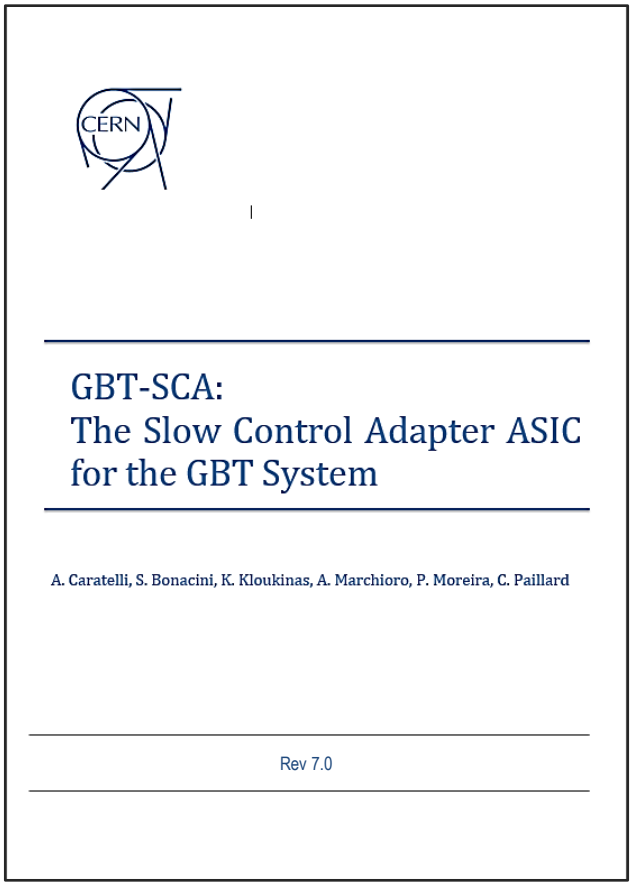
- 1st Prototype submitted for fabrication in July 2014
  - Part of the “GBT-chipset” MPW run
  - Received 2 wafers (~ 520 dies) in middle of November
    - 250 bare die chips
    - 208 BGA packaged chips (possibility to package 260 additional dies)
    - Distribute sample parts to system developers

User manual

Available on GBT sharepoint site:

https://espace.cern.ch/GBT-Project/GBT-SCA/Manuals/Forms/AllItems.aspx

Latest version: GBT-SCA_Manual_Rev7.0



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