ROBO-8110VG2AR

Single Host Board

User's Manual

Version 1.0

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How to Use This Manual

The manual describes how to configure your ROBO-8110VG2AR system to meet various operating requirements. It is divided into five chapters, with each chapter addressing a basic concept and operation of Single Host Board.

Chapter 1 : System Overview. Presents what you have in the box and give you an overview of the product specifications and basic system architecture for this series model of single host board.

Chapter 2 : Hardware Configuration. Shows the definitions and locations of Jumpers and Connectors that you can easily configure your system.

Chapter 3 : System Installation. Describes how to properly mount the CPU, main memory and Compact Flash to get a safe installation and provides a programming guide of Watch Dog Timer function.

Chapter 4 : BIOS Setup Information. Specifies the meaning of each setup parameters, how to get advanced BIOS performance and update new BIOS. In addition, POST checkpoint list will give users some guidelines of trouble-shooting.

Chapter 5 : Troubleshooting. Provides various useful tips to quickly get ROBO-8110VG2AR running with success. As basic hardware installation has been addressed in Chapter 3, this chapter will basically focus on system integration issues, in terms of backplane setup, BIOS setting, and OS diagnostics.

The content of this manual is subject to change without prior notice. These changes will be incorporated in new editions of the document. **Portwell** may make supplement or change in the products described in this document at any time.

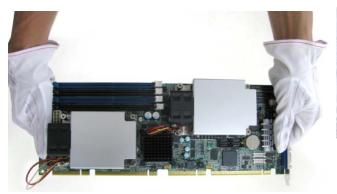
Updates to this manual, technical clarification, and answers to frequently asked questions will be shown on the following web site: http://www.portwell.com.tw/.

NoticeSBC Handling and Installation Notice

Handling and Installing SBC

Caution: Do not just hold any single side of the SBC; hold evenly on both sides!

- Heavy processor cooler may bend the SBC when SBC being held just on one side.
- The bending may cause soldering or components damaged.









■ Fix your SBC in System

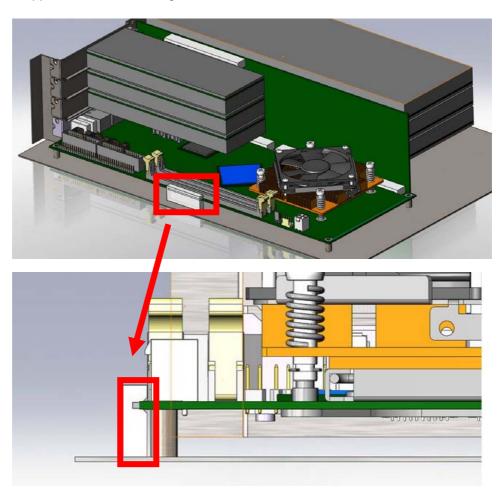
Caution: Suggest your S.I or vendor to use a metal bracket to hold/fix the desktop or server grade SBC to avoid the vibration damage during transportation. Heavy processor cooler may bend the SBC when systems are during transportation without any holder.

Example:

- 4U chassis:
 - → Use L type mental or plastic or rubber bracket to hold SBC.



 2U or 1U chassis: a mental bracket on the bottom of chassis to balance and support SBC from bending.



Chapter 1 System Overview

1.1 Introduction

ROBO-8110VG2AR, the PICMG 1.3 SHB (Single Host Board) supports the Intel® Core i3 and Xeon processor. The attractive Corei3 and Xeon E3-1200 family processors not only posses amazing parallel computing power but also support ECC memory. That makes the system more powerful.

The SHB adopted Intel® C206 chipset and Core i3/Xeon E3-1200 family processors. The Core i3/Xeon E3-1200 family processors integrated Intel® integrated graphics engine that supports 3D performance, DirectX 10.1, Shader model 4.0, and OpenGL 3.0. More than that, user could utilize even higher-end, the latest PCI Express x16 interface graphics card via backplane.

ROBO-8110VG2AR built with dual Intel® Gigabit Ethernet. Four DDR3 long DIMM sockets support system memory up to 16GB. Two SATA 600 ports and Four SATA 300 ports (dual ports via backplane) support RAID 0, 1, 5, 10. Support multiple display by DVI-I (DVI-D + VGA) on bracket and HDMI ports.

To meet bandwidth of storage and expansion cards requirement, the ROBO-8110VG2AR was designed flexible with four PCI Express lanes via backplane. Those four PCI Express lanes could be four PCI Express x1 links or one PCI Express x4 link by different bios support. Four PCI Express x1 links configuration can support more PCI Express x1 devices via backplane and one PCI Express x4 link configuration can support RAID card or special add-on cards such as image processing board. In addition, the flexible configuration can be leveraged with bridge on backplane to support more PCI or PCI-X slots that benefits industries with legacy support. PCI Express x16 from processors can be one PCI Express x16 or two PCI Express x8 or One PCI Express x8 + Two PCI Express x4 by jumper setting. It'll be very flexible for customer to adopt with server or non-server BP.

Advanced Management Technology (AMT) 7.0 is feature that ROBO-8110VG2AR equipped with Xeon E3-1200 family processors (Core i3 doesn't support AMT). This technology provides remote access capability via Intel® Gigabit Ethernet controller. The new technology is a hardware-based solution that uses out-of-band communication for system management access to client systems. Beside that, the hardware and software information can be gathering by 3rd party software then storage in SPI interface EEPROM. Therefore, asset management could be done at the same time.

ROBO-8110VG2AR features:

- Support Intel® Xeon E3-1200 family and Core i3 processor in an LGA1155 socket
- Two 240-pin DDR3 ECC SDRAM DIMM socket, support for DDR3 1333/1066 DIMMs, up to 16GB system memory
- Intel® Xeon E3-1200 family and Core i3 processor integrated graphic engine that supports MPEG-2 Decode, DirectX 10.1, OpenGL 3.0 and Shader Model 4.0
- Equipped dual Intel Gigabit Ethernet ports
- Support iAMT 7.0
- Support two SATA 600 and four SATA 300 ports (dual ports via backplane)
- One PCI Express x16 external expansion, one PCI Express x4 link (can be configured as four PCI Express x1) and four PCI devices via backplane

The PICMG 1.3 SHB is the best solution of applications such like flight simulation, image processing, broadcasting and so on that need performance of display and storage.

1.2 Check List

The ROBO-8110VG2AR package should cover the following basic items:

- ✓ One ROBO-8110VG2AR single host board
- ✓ One dual Serial ports cable kit
- ✓ One single Parallel port cable kit
- ✓ One FDD cable
- ✓ One 7-pin SATA 300 signal cable
- ✓ One SATA 600 signal cable
- ✓ One Installation Resources CD-Title

Optional: One bracket with PS/2 keyboard and mouse

If any of these items is damaged or missing, please contact your vendor and keep all packing materials for future replacement and maintenance.

1.3 Product Specification

Main processor

- Intel® Xeon E3-1200 family and Core i3 Processor

BIOS

AMI system BIOS with SPI Serial CMOS EEPROM with easy upgrade function ACPI, DMI, Green function and Plug and Play Compatible

Main Memory

- Support dual-channel DDR3 memory interface
- ECC, non-buffered DIMMs only
- Two DIMM sockets support 1333/1066 DDR3-SDRAM up to 16GB System Memory

L2 Cache Memory

Built-in Processor

Chipset

Intel® C206 chipset

Bus Interface

- Follow PICMG 1.3 Rev 1.0 standard (PCI Express and PCI)
- Support four PCI Express x1 (can be aggregated as one PCI Express x4) through backplane by different bios
- Support four PCI devices through backplane
- Support one PCI Express x16 or two PCI Express x8 or One PCI Express x8 + Two PCI Express x4 by jumper setting

SATA

- Four SATA 300 ports on-board (dual ports via backplane) and two SATA 600 ports

• Floppy Drive Interface

Support one FDD port up to two floppy drives and 5-1/4"(360K, 1.2MB), 3-1/2" (720K, 1.2MB, 1.44MB, 2.88MB) diskette format and 3-mode FDD

Serial Ports

Support one RS232 and one RS232/422/485 selectable ports

• Parallel Port

Support one parallel port with SPP, EPP and ECP modes

USB Interface

Support fourteen USB 2.0 (Universal Serial Bus) ports (two USB ports on bracket that dedicated to keyboard & mouse; eight USB ports on-board and four USB ports via backplane) for high-speed I/O peripheral devices

PS/2 Mouse and Keyboard Interface

Support one 10-pin header for external PS/2 keyboard/mouse connection

Auxiliary I/O Interfaces

System reset switch, external speaker, Keyboard lock and HDD active LED, etc

• Real Time Clock/Calendar (RTC)

Support Y2K Real Time Clock/Calendar with battery backup for 7-year data retention

Watchdog Timer

- Support WDT function through software programming for enable/disable and interval setting
- Generate system reset

On-board VGA

Processors integrated graphics, share system memory up to 1GB for system with greater than or equal to 192MB of system memory

On-board Ethernet LAN

Dual Intel® PCI Express x1 interface based Gigabit Ethernet to support RJ-45 connector

High Driving GPIO

Support 8 programmable high driving GPIO

Cooling Fans

Support one 4-pin power connector for CPU fan and one 3-pin power connector for system fan

System Monitoring Feature

Monitor CPU temperature, system temperature and major power sources, etc.

Bracket

Support dual Ethernet port with 2 indicators, dual USB ports and one DVI-I port

Outline Dimension (L X W)

338.5mm (13.33") X 126.39mm (4.98")

Power Requirements

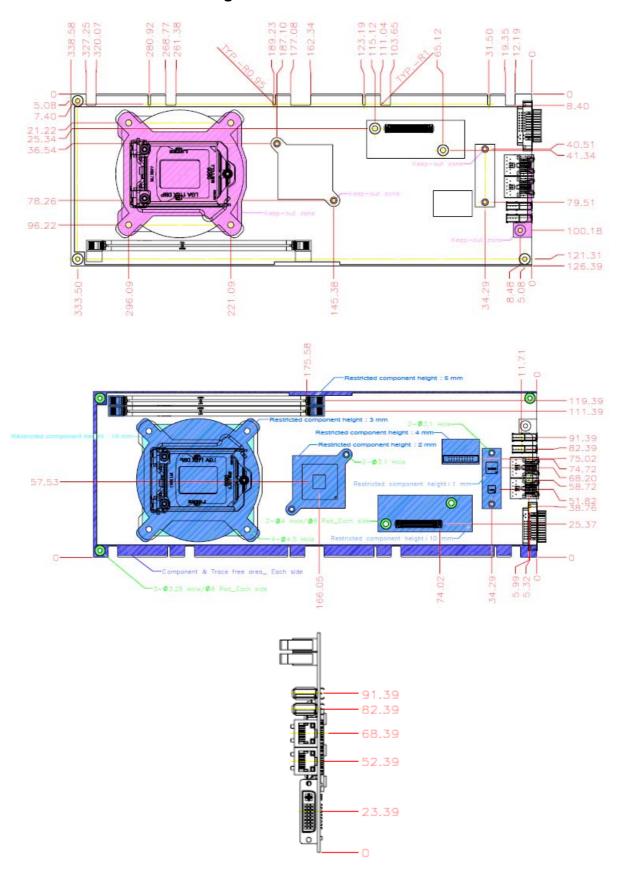
- +12V (CPU)@ 4.85A
- +12V (System)@ 2.43A
- +5V @ 3.4A
 - Test Programs: BurnIn Test V6.0
 - Run Time: Full loading
- Test configuration:

	System Configuration
CPU Type	Intel® Core™ i7-2600 Processor (8M Cache, 3.40 GHz) (ES)
SBC BIOS	Portwell, Inc. ROBO-8110VG2AR BIOS Rev.: R1.10.E1 (05132011)
Memory	Apacer PC3-8500 1GB*1 (E:PIDA J1108BABG-DJ-E)
VGA Card	Onboard Intel® C206 Chipset
VGA Driver	Intel® HD Graphics 1000 Family Version 6.14.10.5337
LAN Card	Onboard Intel® 82574L Gigabit Network Connection Controller
LAN Driver	Intel® 82574L Gigabit Network Connection Version 11.7.32.0
LAN Card	Onboard Intel® 82579LM Gigabit Network Connection Controller
LAN Driver	Intel® 82579LM Gigabit Network Connection Version 11.12.36.0
Audio Card	Onboard Realtek ALC662 High Definition Audio Controller
Audio Driver	Realtek ALC662 High Definition Audio Version 5.10.0.6343
Chip Driver	Intel® Chipset Device Software Version 9.2.0.1025
USB 2.0 Driver	Intel® 6 Series/C200 Series Chipset Family USB Enhanced Host Controller Version 9.2.0.1021
SCSI Card	Adaptec ASC-29160LP
SCSI HDD	Seagate ST39173W 8.47GB
SATA HDD	WD WD1002FAEX 1TB
FDD	SONY MPF920-E 1.44MB
CDROM	LITE-ON LH-20A1S DVD-ROM
Power Supply	FSP400-60PFN
Back plane	PBPE-07P4 (R0)
CPU Type	Intel® Xeon® CPU C5539 2.27GHz(ES) Bus Speed:133.3MHz L3:4M
SBC BIOS	Project Version:0ABRB 0.19 x64 Build Date:01/20/2010 10:10:10
Memory	Apacer ECC DDR3-1066 1GB (ELPIDA J1108BDBG-DJ-F)*2
VGA Card	Onboard XGI Volari Z7-Z9-Z9s-Z11 V1.11.03
VGA Driver	XGI Volari Z7-Z9-Z9s-Z11 Version 6.14.10.1110
LAN Card	Onboard Intel® 82574L Gigabit Network Connection
LAN Driver	Intel® 82574L Gigabit Network Connection Version 11.4.7.0
Chip Driver	Intel® Chipset Device Software Version 9.1.2.1002
USB 2.0 Driver	Intel®5 Series/3400 Series Chipset Family USB Enhanced Host
	Controller
CATA HDD	Ver:9.1.1.1013
SATA HDD	Seagate ST3160815AS
FDD	Teac 1.44
CDROM	Pioneer DVD-227A
Power Supply	FSP350-60GLC
Back plane	PBPE-06P2

• Operating Temperature: 0°C ~ 55°C (23°F ~ 140°F)

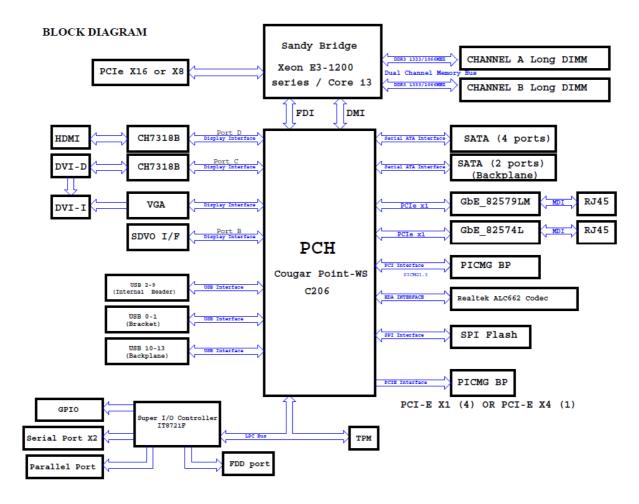
- Storage Temperature -20°C ~ 80°C
- Relative Humidity 5% ~ 90%, non-condensing

1.3.1 Mechanical Drawing



1.4 System Architecture

All of details operating relations are shown in ROBO-8110VG2AR series System Block Diagram.



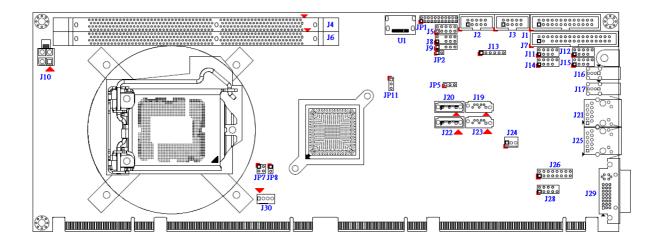
ROBO-8110VG2AR System Block Diagram

Chapter 2 Hardware Configuration

This chapter gives the definitions and shows the positions of jumpers, headers and connectors. All of the configuration jumpers on ROBO-8110VG2AR are in the proper position. The default settings shipped from factory are marked with an asterisk (*).

2.1 Jumper Setting

In general, jumpers on the single board computer are used to select options for certain features. Some of the jumpers are designed to be user-configurable, allowing for system enhancement. The others are for testing purpose only and should not be altered. To select any option, cover the jumper cap over (SHORT) or remove (NC) it from the jumper pins according to the following instructions. Here NC stands for "Not Connect".



JP1: COM2 (J3) Interface Selection

JP1	Function
5-6, 9-11, 10-12, 15-17, 16-18 Short	RS-232
3-4, 7-9, 8-10, 13-15, 14-16, 21-22 Short	RS-422
1-2, 7-9, 8-10, 19-20 Short	RS-485

JP2:ATX / AT Mode Select



JP2	Function	
1-2 Short	AT Mode	
1-2 Open	ATX Mode	

JP5: CMOS Clear



2 3

JP5	Function	
1-2 Short	Normal Operation	
2-3 Short	Clear CMOS Contents	

JP7: PCI Express Bifurcation Selection



JP7	Function		
Short (1-2, 3-4)	1 x8, 2 x4 PCI Express (Support Three slot)		
Short (1-2), Open(3-4)	2 x8 PCI Express (Support Two slot)		
Open (1-2, 3-4)	1 x16 PCI Express (Support One slot)		
Open (1-2), Short (3-4)	reserved		

JP8: VCCSA Voltage Selection



JP8	Function
1-2 Short	0.85 V
1-2 Open	0.925V

JP11: SPI FLASH ROM Selection

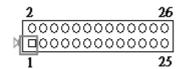
JP11	Function	
1-2 Short	Normal Operation ★	
2-3 Short	N/C	

2.2 Connector Allocation

 $\ensuremath{\mathrm{I/O}}$ peripheral devices and Flash disk will be connected to these interface connectors

CONNECTOR	FUNCTION	REMARK
J1	Parallel Port Connector	
J2	COM1 Serial Port 1 Connector	
J3	COM2 Serial Port 2 Connector	
J4 / J6	DDR3 Long SLOT	
J5	General Purpose I/O Connector	
J7	Floppy Connector	
J8	External PS/2 Keyboard/Mouse Connector	
J9	SMBus Connector	
J10	+12V Power Connector	Connect to CPU
J11/J12/J14/J1	Internal USB Connector	
5		
J16/J17	External USB Connector	
J13	CIR Connector	6x1 pin header
J20/J22	SATA 2 Connector	
J19/J23	SATA 3 Connector	
J21	Ethernet RJ-45 Connector (LAN 1)82574L	
J25	Ethernet RJ-45 Connector (LAN 2)82579LM	
J24	FAN 1 (SYSTEN FAN) Power Connector	
J30	FAN 2 (CPU FAN) Power Connector	
J26	Front Panel Pin HDR	
J28	Audio Connector	
J29	DVI Connector	
U1	HDMI Connector	

Parallel Port Connector (J1)



PIN No.	Signal Description	PIN No.	Signal Description
1	Strobe#	2	Auto Form Feed#
3	Data0	4	Error#
5	Data1	6	Initialization#
7	Data2	8	Printer Select IN#
9	Data3	10	Ground
11	Data4	12	Ground
13	Data5	14	Ground
15	Data6	16	Ground
17	Data7	18	Ground
19	Acknowledge#	20	Ground
21	Busy	22	Ground
23	Paper Empty	24	Ground
25	Printer Select	26	NC

<u>J2: COM1 Serial Port</u>



PIN No.	Signal Description
1	DCD
2	DSR
3	RXD
4	RTS
5	TXD
6	CTS
7	DTR
8	RI
9	Ground
10	N/C

J3: COM2 Serial Port 2 Connector



PIN No	Signal Description			
	RS-232	RS-422	RS-485	
1	DCD (Data Carrier Detect)	TX-	DATA-	
2	DSR (Data Set Ready)	N/C	N/C	
3	RXD (Receive Data)	TX+	DATA+	
4	RTS (Request to Send)	N/C	N/C	
5	TXD (Transmit Data)	RX+	N/C	
6	CTS (Clear to Send)	N/C	N/C	
7	DTR (Data Terminal Ready)	RX-	N/C	
8	RI (Ring Indicator)	N/C	N/C	
9	GND (Ground)	GND	GND	
10	N/C	N/C	N/C	

Note:

J3 (COM2) could be configurable as RS-232/422/485 with jumper JP1.

J5: General Purpose I/O Connector



PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO0	2	GPIO4
3	GPIO1	4	GPIO5
5	GPIO2	6	GPIO6
7	GPIO3	8	GPIO7
9	Ground	10	+5V

Note:

All General Purpose I/O ports can only apply to standard TTL \pm 5% signal level (0V/5V), and each Fan

J7:Floppy Interface



PIN No.	Signal Description	PIN No.	Signal Description
1	Ground	2	Density Select
3	Ground	4	N/C
5	N/C	6	N/C
7	Ground	8	Index#
9	Ground	10	Motor ENA#
11	Ground	12	N/C
13	Ground	14	Drive Select A#
15	Ground	16	N/C
17	Ground	18	Direction#
19	Ground	20	Step#
21	Ground	22	Write Data#
23	Ground	24	Write Gate#
25	Ground	26	Track 0#
27	Ground	28	Write Protect#
29	N/C	30	Read Data#
31	Ground	32	Head Select#
33	N/C	34	Disk Change#

<u>J8: External PS/2 Keyboard/Mouse Connector</u>



PIN No.	Signal Description	PIN No.	Signal Description
1	Mouse Data	2	Keyboard Data
3	N/C	4	N/C
5	Ground	6	Ground
7	PS2 Power	8	PS2 Power
9	Mouse Clock	10	Keyboard Clock

J9:SMBUS Connector



Pin No.	Signal Description
1	SMBus_CLK
2	N/C
3	Ground
4	SMBus_DAT
5	+5V

J10: +12V POWER Connector



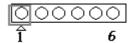
Pin No.	Signal Description	
1	Ground	
2	Ground	
3	+12V	

J11/J12/J14/J15: External USB Connector



PIN No.	Signal Description	PIN No.	Signal Description
1	5V Dual	2	5V Dual
3	USB-	4	USB-
5	USB+	6	USB+
7	Ground	8	Ground
	Key(no pin)	10	N/C

J13:CIR Connector



Pin No.	Signal Description
1	+5V
2	N/C
3	CIRRX
4	Ground
5	CIRTX
6	N/C

J24: System Fan Connector



Pin No.	Signal Description	
1	Ground	
2	Fan speed control	
3	Fan on/off output	

J30: CPU Fan Connector



Pin No.	Signal Description	
1	Ground	
2	+12V	
3	Fan on/off output	
4	Fan Speed control	

J26:Front Panel Pin HDR

2	16
00000	0000
N O O O	0000
1	15

PIN No.	Signal Description	PIN No.	Signal Description
1	PWR_LED(+)	2	Speaker(+)
3	PWR_LED(-)	4	N/C
5	J25 LAN1_ACT(+)	6	N/C
7	J25 LAN1_LINK(-)	8	Speaker(-)
9	J21 LAN2_LINK(-)	10	NC
11	J21 LAN2_ACT(+)	12	NC
13	HDD_LED(+)	14	NC
15	HDD_LED(-)	16	NC

J28: Audio MIC/Line-in/Line-out Connector



PIN No.	Signal Description	PIN No.	Signal Description
1	MIC with Reference	2	Analog Ground
	Voltage		_
3	Line-in Left Channel	4	Analog Ground
5	Line-in Right Channel	6	Analog Ground
7	Line-out Left Channel	8	Analog Ground
9	Line-out Right Channel	10	N/C

J28: Audio MIC/Line-in/Line-out Connector

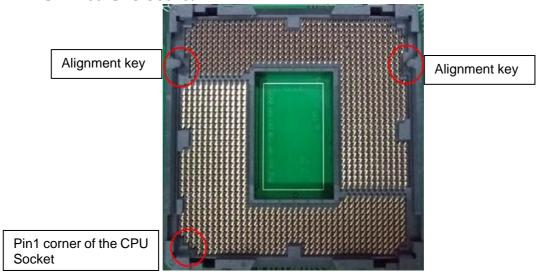
PIN No.	Signal Description	PIN No.	Signal Description	PIN No.	Signal Description
1	D2-	9	D1-	17	D0-
2	D2+	10	D1+	18	D0+
3	SHIELD1	11	SHIELD2	19	SHIELD3
4	D4-	12	D3-	20	D5-
5	D4+	13	D3+	21	D5+
6	DDCCLK	14	VCC	22	SHIELD4
7	DDCDATA	15	GND	23	CLK+
8	NC	16	HPDET	24	CLK-
C1	Red	CG1	CG1		
C2	Green	CG2	CG2		
C3	Blue				
C4	H_SYNC				
C5	A_GND1				
C6	A_GND2				
C1	Red				

Chapter 3 System Installation

This chapter provides you with instructions to set up your system. The additional information is enclosed to help you set up onboard PCI device and handle Watch Dog Timer (WDT) and operation of GPIO in software programming

3.1 Intel LGA-1155 Processor





• LGA-1155 CPU.



Please remember to locate the alignment keys on the CPU socket of the motherboard and the notches on the CPU $\,$

• LGA-1155 CPU Installation Steps

Before install the CPU, please make sure to turn off the power first!!

1. Open the load lever.



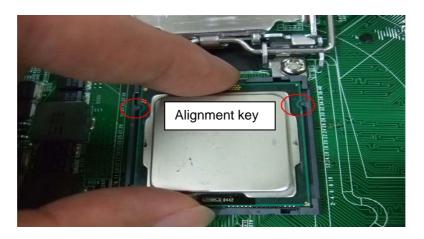
2. Lift the load lever up to fully open.



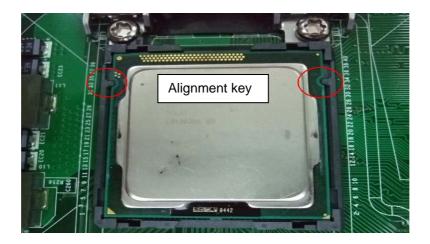
3. Remove the plastic cap on the CPU socket. Before you install the CPU, always cover it to protect the socket pin.



4. After confirming the CPU direction for correct mating, put down the CPU in the socket housing frame. Note that alignment keys are matched.



5. Make sure the CPU has been seated well into the socket. If not, take out the CPU and reinstall.



6. Engage the load lever while pressing down lightly onto the load plate.



7. Push the CPU socket lever back into its locked position.



8. Please make sure four hooks are in proper position before you install the cooler.

3.2 Main Memory

ROBO-8110VG2AR provide 2 x240 pin DIMM sockets (Dual Channel) which supports Dual channel 1066/1333 DDR3-SDRAM as main memory, Non-ECC (Error Checking and Correcting), non-register functions. The maximum memory can be up to 16GB. Memory clock and related settings can be detected by BIOS via SPD interface.

For system compatibility and stability, do not use memory module without brand. Memory configuration can be set to either one double-sided DIMM in one DIMM socket or two single-sided DIMM in both sockets.

Beware of the connection and lock integrity from memory module to socket. Inserting improperly it will affect the system reliability.

Before locking, make sure that all modules have been fully inserted into the card slots

Note:

To insure the system stability, please do not change any of DRAM parameters in BIOS setup to modify system the performance without acquired technical information.

3.3 Installing the Single Board Computer

To install your ROBO-8110VG2AR into standard chassis or proprietary environment, please perform the following:

- Step 1 : Check all jumpers setting on proper position
- Step 2: Install and configure CPU and memory module on right position
- Step 3: Place ROBO-8110VG2AR into the dedicated position in the system
- Step 4: Attach cables to existing peripheral devices and secure it

WARNING

Please ensure that SBC is properly inserted and fixed by mechanism.

Note:

Please refer to section 3.3.1 to 3.3.4 to install INF/VGA/LAN/Audio drivers.

3.3.1 Chipset Component Driver

ROBO-8110VG2AR uses Intel Cougar Point workstation C206 chipset. It's a new chipset that some old operating systems might not be able to recognize. To overcome this compatibility issue, for Windows Operating Systems such as Windows XP, please install its INF before any of other Drivers are installed. You can find very easily this chipset component driver in ROBO-8110VG2AR CD-title.

3.3.2 Intel® Integrated Graphics CMCH Chip

ROBO-8110VG2AR uses Intel® PCH integrated graphic engine to gain an outstanding graphic performance. ROBO-8110VG2AR supports DVI-I, HDMI dual display. This combination makes ROBO-8110VG2AR an excellent piece of multimedia hardware.

Drivers Support

Please find the Graphic drivers in the ROBO-8110VG2AR CD-title. Drivers support, Windows XP/Win7.

3.3.3 On-board Gigabit Ethernet Controllers

Drivers Support

Please find Intel 82579LM and 82574L LAN drivers in /Ethernet directory of ROBO-8110VG2AR CD-title. The drivers support Windows XP/Win7.

3.3.4 Audio Controller

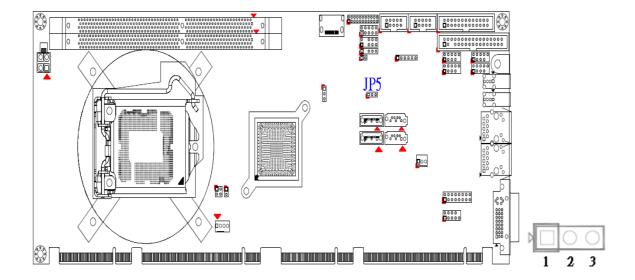
Please find Realtek ALC662-GR (High Definition Audio driver) form ROBO-8110VG2AR CD-title. The drivers support Windows XP/Win7.

3.4 Clear CMOS Operation

The following table indicates how to enable/disable Clear CMOS Function hardware circuit by putting jumpers at proper position.

JP5: CLEAR CMOS

JP5	Function		
1-2 Short	Normal Operation ★		
2-3 Short	Clear CMOS Contents		



3.5 WDT Function

The working algorithm of the WDT function can be simply described as a counting process. The Time-Out Interval can be set through software programming. The availability of the time-out interval settings by software or hardware varies from

boards to boards.

ROBO-8110VG2AR allows users control WDT through dynamic software programming. The WDT starts counting when it is activated. It sends out a signal to system reset or to non-maskable interrupt (NMI), when time-out interval ends. To

prevent the time-out interval from running out, a re-trigger signal will need to be

sent before the counting reaches its end. This action will restart the counting process.

A well-written WDT program should keep the counting process running under normal condition. WDT should never generate a system reset or NMI signal unless the system runs into troubles.

The related Control Registers of WDT are all included in the following sample program that is written in C language. User can fill a non-zero value into the Timeout Value Register to enable/refresh WDT. System will be reset after the Time-out

Value to be counted down to zero. Or user can directly fill a zero value into Timeout Value Register to disable WDT immediately. To ensure a successful accessing to the content of desired Control Register, the sequence of following program codes

should be step-by-step run again when each register is accessed.

Additionally, there are maximum 2 seconds of counting tolerance that should be

considered into user' application program. For more information about WDT, please refer to IT8728F/CXS data sheet.

There are two PNP I/O port addresses that can be used to configure WDT,

- 1) 0x2E:EFIR (Extended Function Index Register, for identifying CR index number)
- 2) 0x2F:EFDR (Extended Function Data Register, for accessing desired CR)

Below are some example codes, which demonstrate the use of WDT.

```
#include <stdio.h>
#include <conio.h>
#include <dos.h>

#define SIO_Port 0x2E
#define SIO_Port2 0x4E
#define GPIO_LDN 0x07

void Enter_IT872x_SIO() {
```

```
outportb(SIO_Port, 0x87);
         outportb(SIO_Port, 0x01);
         outportb(SIO_Port, 0x55);
         outportb(SIO_Port, 0x55);
}
void Set_LDN(unsigned char LDN) {
         outportb(SIO_Port, 0x07);
         outportb(SIO_Port+1, LDN);
         printf("LDN=%x\n", LDN);
}
void Set_Register(unsigned char offset, unsigned char value) {
         outportb(SIO_Port, offset);
         outportb(SIO_Port+1, value);
         printf("Write offset: %x = %x \ n", offset, value);
int main(void) {
         printf("test string\n");
         Enter_IT872x_SIO();
         Set_LDN(GPIO_LDN);
         Set_Register(0x72, 0xC0);
         Set_Register(0x73, 0x05);
         printf("System will reset in 5 seconds\n");
         return 0;
```

3.6 **GPIO**

The ROBO-8110VG2AR provides 8 programmable input or output ports that can be individually configured to perform a simple basic I/O function. Users can configure each individual port to become an input or output port by programming register bit of I/O Selection. To invert port value, the setting of Inversion Register has to be

made. Port values can be set to read or write through Data Register.

J5: General Purpose I/O Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO0	2	GPIO4
3	GPIO1	4	GPIO5
5	GPIO2	6	GPIO6
7	GPIO3	8	GPIO7
9	Ground	10	+5V

```
#include <stdio.h>
#include <conio.h>
#include <stdlib.h>
#define SIO_Port 0x2E
                         0x4E
#define SIO_Port2
#define GPIO_LDN
                          0x07
#define GPIO Base
                          0x0A00
//Enter SIO
void Enter_IT872x_SIO() {
        outp(SIO_Port, 0x87);
        outp(SIO_Port, 0x01);
        outp(SIO_Port, 0x55);
        outp(SIO_Port, 0x55);
```

}

```
//Select LDN
void Set_LDN(unsigned char LDN) {
         outp(SIO_Port, 0x07);
         outp(SIO_Port+1, LDN);
         //printf("LDN=%x\n", LDN);
}
//Set register offset to Value
void Set_Register(unsigned char offset, unsigned char value) {
         outp(SIO_Port, offset);
         outp(SIO_Port+1, value);
         //printf("Write offset:%x = %x\n", offset, value);
}
//Or register
void Or_Register(unsigned char offset, unsigned char value) {
         outp(SIO_Port, offset);
         outp(SIO_Port+1, inp(SIO_Port+1) | value);
         //printf("Write offset:%x = %x \n", offset, value);
}
//And register
void And_Register(unsigned char offset, unsigned char value) {
         outp(SIO_Port, offset);
         outp(SIO_Port+1, inp(SIO_Port+1) & value);
         //printf("Write offset:%x = %x \n", offset, value);
}
int main(void) {
```

```
int result;
printf("ROBO-8110 GPIO Test:\n");
//pin1 = 11
//pin3 = 12
//pin5 = 47
//pin7 = 50
//pin2 = 14
//pin4 = 35
//pin6 = 36
//pin8 = 37
Enter_IT872x_SIO();
Set_LDN(GPIO_LDN);
//Enable GPIO
//Or_Register(0xC0,0x46) //11,12,14
//Or_Register(0xC2,0xE0) //35,36,37
//Or_Register(0xC3,0x80) //47
//Or_Register(0xC4,0x01) //50
//Set Output
Or_Register(0xC8,0x06); //11,12
Or_Register(0xCB,0x80);
                         //47
Or_Register(0xCC,0x01);
                         //50
//Set Input
```

```
And_Register(0xC8,0xEF); //14
And_Register(0xCA,0x1F); //35,36,37
//output high
outp(GPIO_Base+0,0x06); //11,12
outp(GPIO_Base+3,0x80); //47
outp(GPIO_Base+4,0x01); //50
result=1;
if ((inp(GPIO_Base+0)&0x10)!=0x10) result=0;
if ((inp(GPIO\_Base+2)\&0xE0)!=0xE0) result=0;
if (result==0){
        printf("Test fail!!\n");
        return 1;
}
//output low
outp(GPIO_Base+0,inp(GPIO_Base+0)&0xF9);
                                                   //11,12
outp(GPIO_Base+3,inp(GPIO_Base+3)&0x7F);
                                                   //47
outp(GPIO_Base+4,inp(GPIO_Base+4)&0xFE);
                                                   //50
result=1;
if ((inp(GPIO_Base+0)&0x10)!=0x00) result=0;
if ((inp(GPIO\_Base+2)\&0xE0)!=0x00) result=0;
if (result==0){
```

```
printf("Test fail!!\n");
       return 1;
}
//Set Input
And_Register(0xC8,0xF9); //11,12
And_Register(0xCB,0x7F); //47
And_Register(0xCC,0xFE);//50
//Set output
Or_Register(0xC8,0x10);
                      //14
Or_Register(0xCA,0xE0); //35,36,37
//output high
outp(GPIO_Base+0,0x10); //14
outp(GPIO_Base+2,0xE0); //35,36,37
result=1;
if ((inp(GPIO_Base+0)&0x06)!=0x06) result=0; //11,12
if ((inp(GPIO_Base+3)&0x80)!=0x80) result=0; //47
if ((inp(GPIO_Base+4)&0x01)!=0x01) result=0; //50
if (result==0){
       printf("Test fail!!\n");
```

```
return 1;
        }
        //output low
        outp(GPIO_Base+0,inp(GPIO_Base+0)&0xEF);
                                                             //14
        outp(GPIO_Base+2,inp(GPIO_Base+2)&0x1F);
                                                             //35,36,37
        result=1;
        if ((inp(GPIO_Base+0)&0x06)!=0x00) result=0; //11,12
        if ((inp(GPIO_Base+3)&0x80)!=0x00) result=0; //47
        if ((inp(GPIO_Base+4)&0x01)!=0x00) result=0; //50
        if (result==0){
                 printf("Test fail!!\n");
                 return 1;
        }
        //getchar ();
        printf("Test Pass!!\n");
        return 1;
}
```

Chapter 4 BIOS Setup Information

RUBY-PB6511 uses AMI BIOS structure stored in Flash ROM. These BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power-off periods. When system is turned on, RUBY-PB6511 communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start up.

4.1 Entering Setup -- Launch System Setup

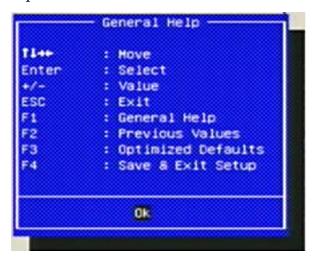
Power on the computer and the system will start POST (Power On Self Test) process. When the message below appears on the screen, press key will enter BIOS setup screen.

Press to enter SETUP

If the message disappears before responding and still wish to enter Setup, please restart the system by turning it OFF and On or pressing the RESET button. It can be also restarted by pressing <Ctrl>, <Alt>, and <Delete> keys on keyboard simultaneously.

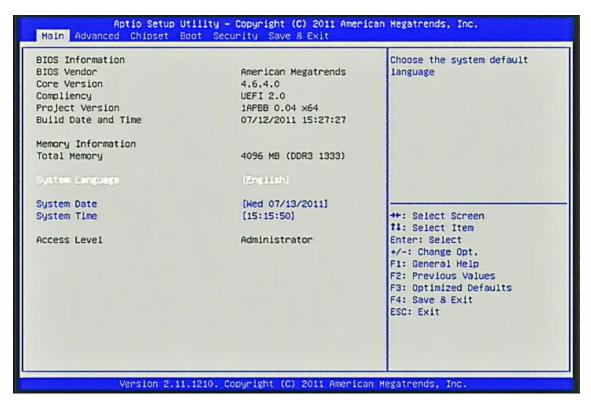
Press <F1> to Run SETUP or Resume

The BIOS setup program provides a General Help screen. The menu can be easily called up from any menu by pressing <F1>. The Help screen lists all the possible keys to use and the selections for the highlighted item. Press <Esc> to exit the Help screen.



4.2 Main

Use this menu for basic system configurations, such as time, date etc.



BIOS Information, Memory Information

These items show the firmware and memory specifications of your system. Read only.

<u>System Language</u> Choose the system default language.

Choices: English.

System Time

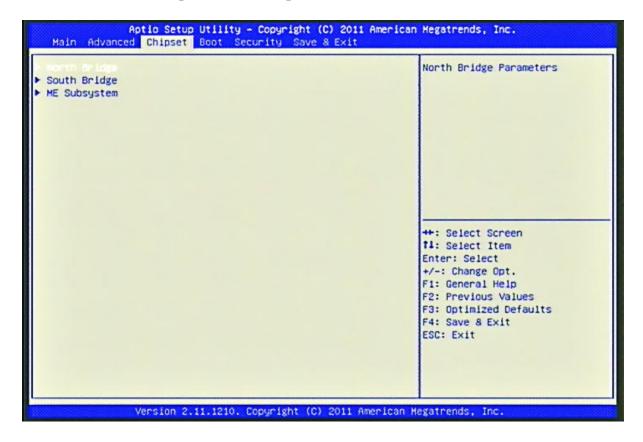
The time format is <Hour> <Minute> <Second>. Use [+] or [-] to configure system Time.

System Date

The date format is $\langle Day \rangle$, $\langle Month \rangle \langle Date \rangle \langle Year \rangle$. Use [+] or [-] to configure system Date.

4.3 Advanced

Use this menu to set up the items of special enhanced features.



Launch PXE OpROM

Enabled or Disabled Boot Option for Legacy Network Devices.

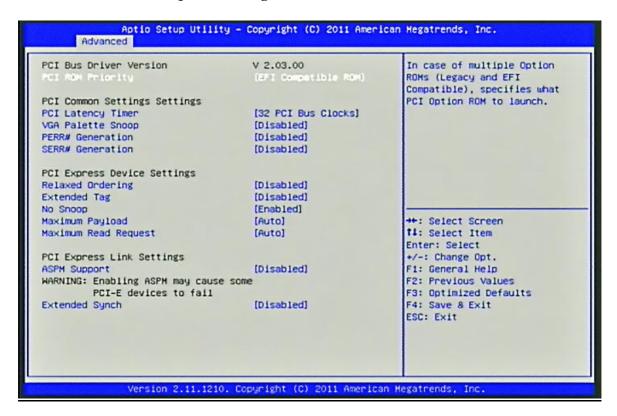
Choices: Disabled, Enabled.

Launch Storage OpROM

Enabled or Disabled Boot Option for Legacy Mass Storage devices.

PCI Subsystems Settings

PCI, PCI-X and PCI Express Settings.



PCI ROM Priority

In case of multiple Option ROMs (Legacy and EFI Compatible), specifies what PCO Option ROM to launch.

Choices: Legacy ROM, EFI Compatible ROM.

PCI Latency Timer

Value to be programmed into PCI Latency Timer Register.

Choices: 32 PCI Bus Clocks, 64 PCI Bus Clocks, 96 PCI Bus Clocks, 128 PCI Bus Clocks, 160 PCI Bus Clocks, 192 PCI Bus Clocks, 224 PCI Bus Clocks, 248 PCI Bus Clocks.

VGA Palette Snoop

Choices: Disabled, Enabled.

PERR# Generation

Enables or Disables PCI Device to Generate PERR#.

Choices: Disabled, Enabled.

SERR# Generation

Enables or Disables PCI Device to Generate SERR#.

Choices: Disabled, Enabled. Choices: Disabled, Enabled

Relaxed Ordering

Choices: Disabled, Enabled.

Extended Tag

If Enabled allows Device to use 8-bit Tag field as a requester.

Choices: Disabled, Enabled.

No Snoop

Choices: Disabled, Enabled.

Maximum Payload

Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.

Choices: Auto, 128 Bytes, 256 Bytes, 512 Bytes, 1024 Bytes, 2048 Bytes, 4096 Bytes.

Maximum Read Request

Set Maximum Read Request size of PCI Express Device or allow System BIOS to select the value.

Choices: Auto, 128 Bytes, 256 Bytes, 512 Bytes, 1024 Bytes, 2048 Bytes, 4096 Bytes.

ASPM Support

Set the ASPM Level: Force L0 - Force all links to L0 State: AUTO - BIOS auto

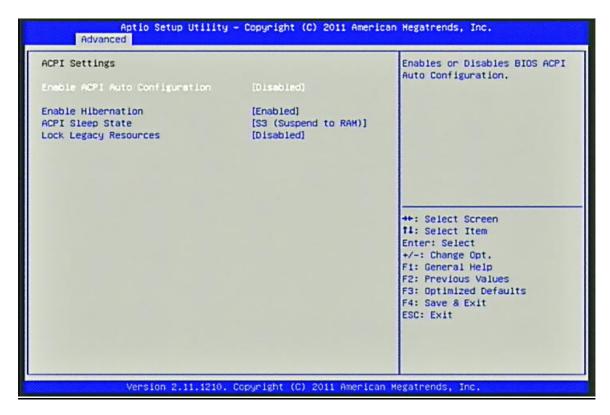
configure: DISABLE - Disables ASPM.

Choices: Disabled. Auto, Force L0.

Extended Synch

If Enabled allows generation of Extended Synchronization patterns.

ACPI Settings



Enabled ACPI Auto Configuration

Choices: Enabled, Disabled.

Enabled Hibernation

Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

Choices: Enabled, Disabled.

ACPI Sleep State

Select the highest ACPI Sleep state the system will enter when the SUSPEND button is pressed.

Choices: Suspend Disabled, S1 (CPU Stop Clock), S3 (Suspend to RAM).

Lock Legacy Resources

Enables or Disables Lock of Legacy Resources.

Choices: Enabled, Disabled.

Trusted Computing

```
Aptio Setup Utility - Copyright (C) 2011 American Megatrends, Inc.

Advanced

TPM Configuration
TPM Status Information
ND TPM Hardware

##: Select Screen
T1: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

Version 2.11.1210. Copyright (C) 2011 American Megatrends, Inc.
```

TPM SUPPORT

Enables or Disables TPM support.

The choice: Disabled, Enabled

WHEA Configuration



WHEA SUPPORT

Enables or Disables Windows Hardware Error Architecture.

The choice: Disabled, Enabled

S5 RTC Wake Settings

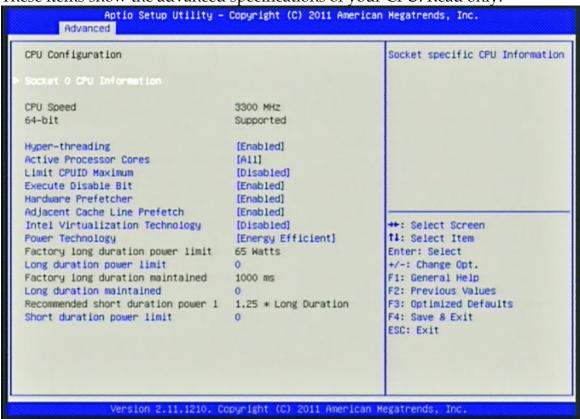


Wake system with Fixed Time

Enabled or Disabled system wake on alarm event. When Enabled, system will wake on the hr::min::sec specified.

CPU Configuration

These items show the advanced specifications of your CPU. Read only.



Hyper-Threading

Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled only one thread per enabled core is enabled.

Choices: Disabled, Enabled.

Active Processor Cores

Number of cores to Enabled in each processor package.

Choices: All, 1, 2, 3.

Limit CPUID Maximum

Disabled for Windows XP. Choices: Disabled, Enabled.

Execute Disabled Bit

XP can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, RedHat Enterprise 3 Update 3.).

Hardware Prefetcher

To turn on/off the MLC streamer prefetcher.

Choices: Disabled, Enabled.

Adjacent Cache Line Prefetch

To turn on/off the prefetching of adjacent cache lines.

Choices: Disabled, Enabled.

Intel Virtualization Technology

When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Choices: Disabled, Enabled.

Power Technology

Enabled the power management features.

Choices: Disabled, Energy Efficient, Custom.

Long duration power limit

Long duration power limit in Watts.

Choices: 0-255

Long duration maintained

Time window which the long duration power is maintained.

Choices: 0-32000

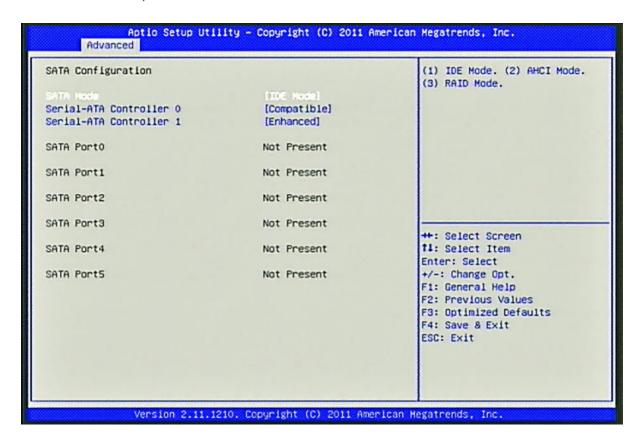
Short duration power limit

Short duration power limit in Watts.

Choices: 0-255

SATA Configuration

SATA Devices Configuration. Choices: Enabled, Disabled.



SATA Mode

Select IDE/AHCI Configuration.

Choices: Disable, IDE Mode, AHCI Mode.

Serial-ATA Controller 0

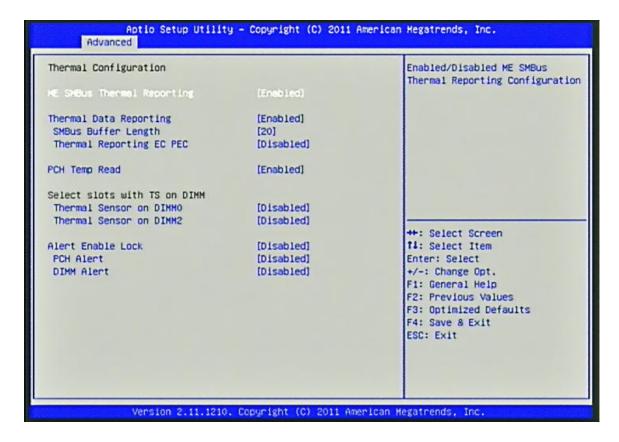
Enabled/Disabled Serial ATA Controller 0.

Choices: Disabled, Enhanced, Compatible.

Serial-ATA Controller 1

Enabled/Disabled Serial ATA Controller 1.

Thermal Configuration



ME SMBus Thermal Reporting

Enabled/Disabled ME SMBus Thermal Reporting Configuration.

Choices: Disabled, Enabled.

Thermal Data Reporting

Choices: Disabled, Enabled.

SMBus Buffer Length

SMBus Block Read message length for EC.

Choices: 1, 2, 5, 9, 10, 14, 20.

Thermal Reporting EC PEC

Enable Packet Error Checking (PEC) for SMBus Block Read.

Choices: Disabled, Enabled.

PCH Temp Read

PCH Temperature Read Enable. Choices: Disabled, Enabled.

Thermal Sensor on DIMM0

Thermal Sensor on DIMM2

Choices: Disabled, Enabled.

Alert Enable Lock

Lock all Alert Enable settings. Choices: Disabled, Enabled.

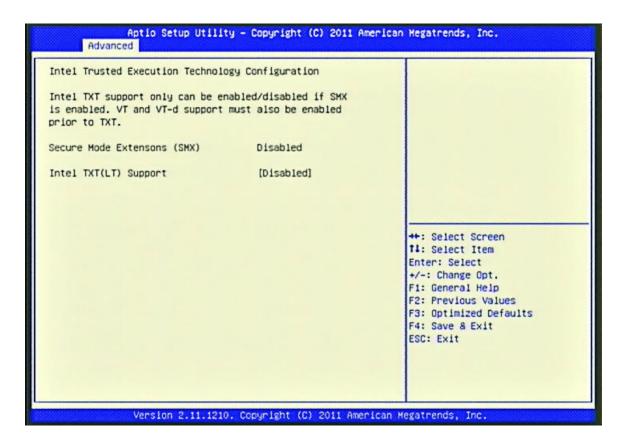
PCH Alert

Choices: Disabled, Enabled.

DIMM Alert

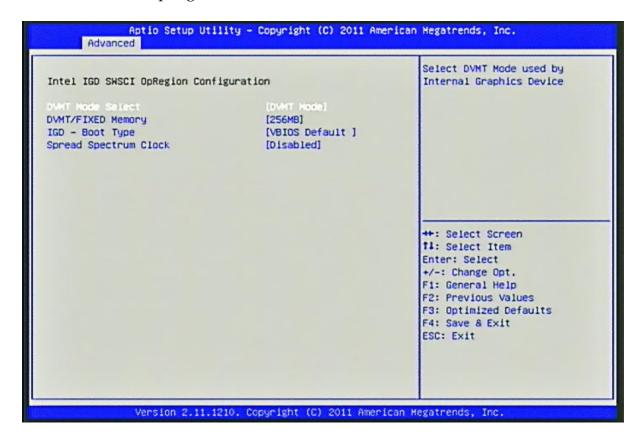
Choices: Disabled, Enabled.

Intel TXT(LT) Configuration



Intel IGD SWSCI Configuration

Intel IGD SWSCI OpRegion Function.



DVMT Mode

Select DVMT Mode used by Internal Graphic Device.

Choices: Fixed Mode, DVMT Mode.

DVMT/FIXED Memory

Select DVMT/FIXED Mode Memory size used by Internal Graphic Device.

Choices: 128MB, 256MB, Maximum.

IGD - Boot Type

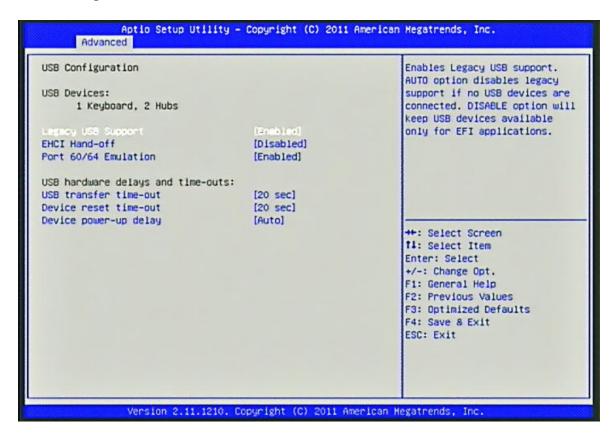
Select the Video Device which will be activated during POST. This has no effect if external graphics present.

Choices: VBIOS Default, CRT, EFP, EFP2, EFP3, CRT + EFP.

Spread Spectrum Clock

USB Configuration

USB Configuration Parameters.



Legacy USB Support

Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.

Choices: Disabled, Enabled, Auto.

EHCI Hand-Off

This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should claim by EHCI driver.

Choices: Disabled, Enabled.

Port 60/64 Emulation

Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.

Choices: Disabled, Enabled.

USB transfer time-out

The Time-out value for Control, Bulk, and Interrupt transfers.

Choices: 1 sec, 5 sec, 10 sec, 20 sec.

Device Reset time-out

USB mass storage device Start Unit command time-out.

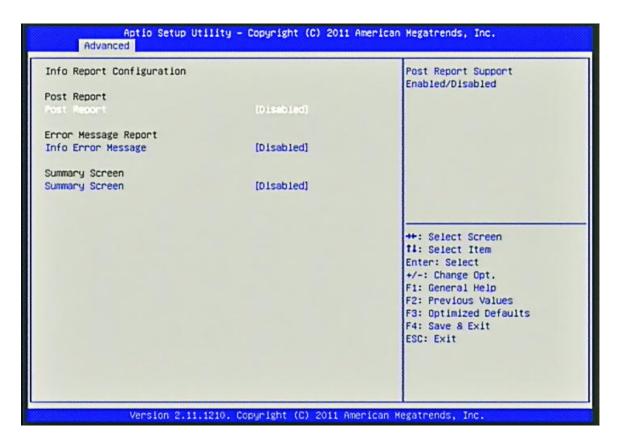
Choices: 10 sec, 20 sec, 30 sec, 40 sec.

Device Power-up delay

Maximum time the device will take before it properly reports itself to the Host Controller. 'AUTO' uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from Hub descriptor.

Choices: Auto, Manual.

Info Report Configuration



Post Report

Choices: Disabled, Enabled.

Info Error Message

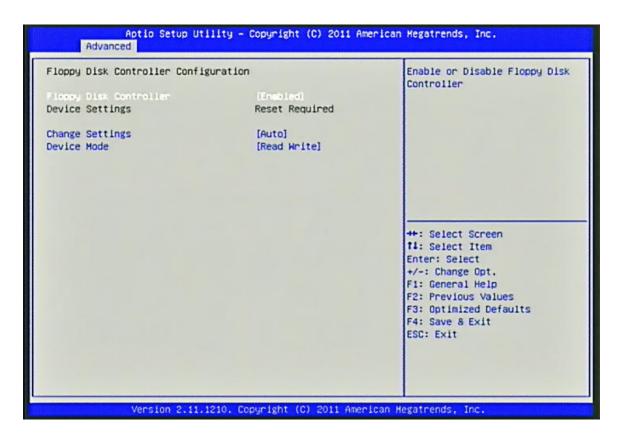
Choices: Disabled, Enabled.

Summary Screen

Super IO Configuration

```
Aptio Setup Utility - Copyright (C) 2011 American Hegatrends, Inc.
       Advanced
 Super IO Configuration
                                                                  Set Parameters of Floppy Disk
                                                                 Controller (FDC)
                                     IT8728
 Super IO Chip
Serial Port O Configuration
▶ Serial Port 1 Configuration
▶ Parallel Port Configuration
                                                                  ++: Select Screen
                                                                 t1: Select Item
                                                                 Enter: Select
                                                                 +/-: Change Opt.
                                                                 F1: General Help
                                                                 F2: Previous Values
                                                                 F3: Optimized Defaults
                                                                 F4: Save & Exit
                                                                 ESC: Exit
                 Version 2.11.1210. Copyright (C) 2011 American Hegatrends, Inc.
```

Floppy Disk Controller Configuration



Floppy Disk Controller

Choices: Disabled, Enabled

Change Settings

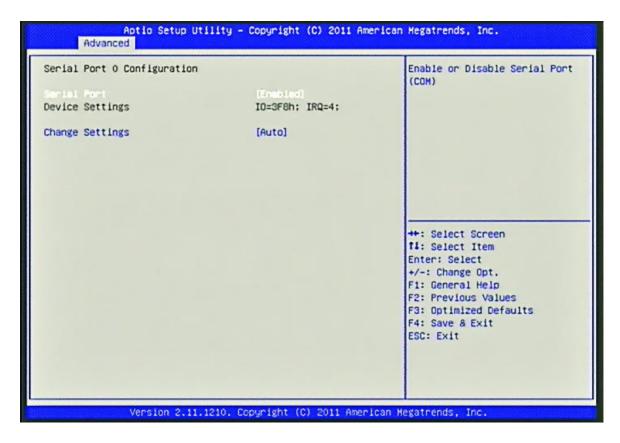
Choices: Auto, IO=3F0h; IRQ=6, DMA=2; IO=3F0h; IRQ=3,4,5,6,7,10,11,12, DMA=2, 3;

IO=370h; IRQ=3,4,5,6,7,10,11,12, DMA=2, 3;

Device Mode

Choices: Read Write, Write Protect

Serial Port 0/1 Configuration



Serial Port

Choices: Disabled, Enabled.

Change Settings

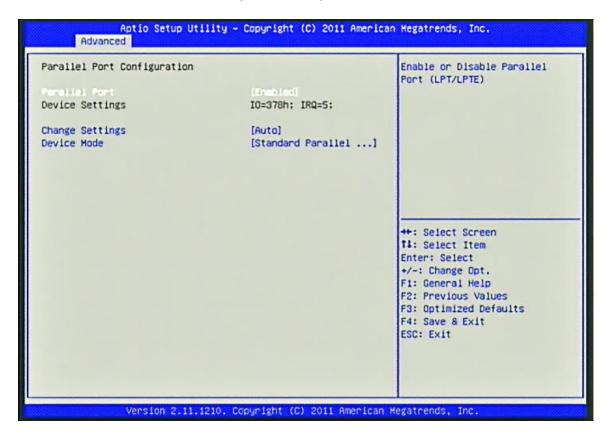
Select an optimal setting for Super IO Device.

Choices: Auto. IO=3F8h; IRQ=4, IO=3F8h; IRQ=3,4,5,6,7,10,11,12, IO=2F8h; IRQ=3,4,5,6,7,10,11,12, IO=2E8h; IRQ=3,4,5,6,7,10,11,12, IO=2E8h;

IRQ=3,4,5,6,7,10,11,12.

Parallel Port Configuration

Set Parameters of Parallel Port (LPT/LPTE)



Parallel Port

Choices: Disabled, Enabled.

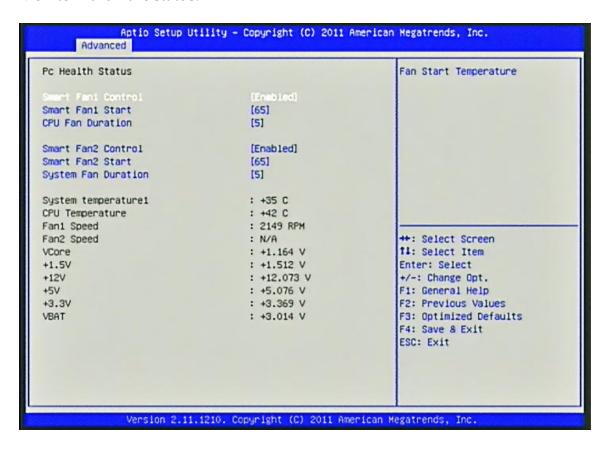
Change Settings

Select an optimal setting for Super IO device.

Choices: Auto. IO=378h; IRQ=5, IO=378h; IRQ=5,6,7,10,11,12, IO=278h; IRQ=5,6,7,10,11,12, IO=3BCh; IRQ=5,6,7,10,11,12, IO=378h; IO=278h; O=3BCh

H/W Monitor

Monitor hardware status.



Smart Fan1/2 Control

Smart CPU Fan Function.

Choices: Disabled, Enabled.

Smart Fan1/2 Start

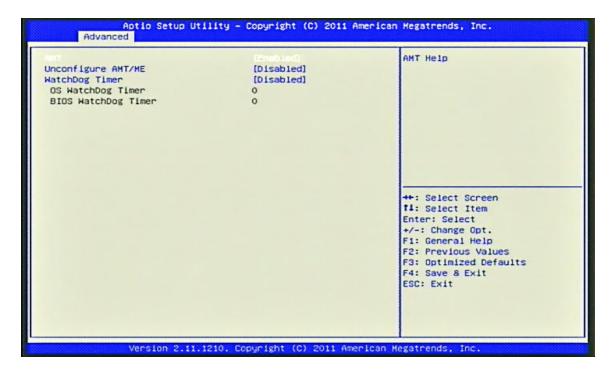
Smart CPU Fan start Temperature Setting.

Choices: 25, 30, 35, 40, 45, 50, 55, 60, 65, 70.

CPU/System Fan Duration

Choices: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10.

AMT Configuration



AMT

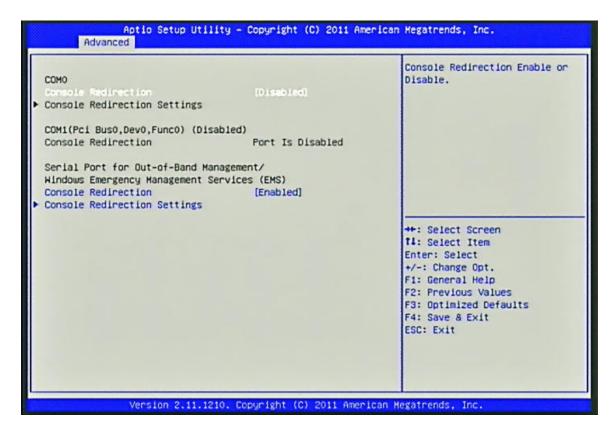
Choices: Disabled, Enabled,

Unconfigure AMT/ME

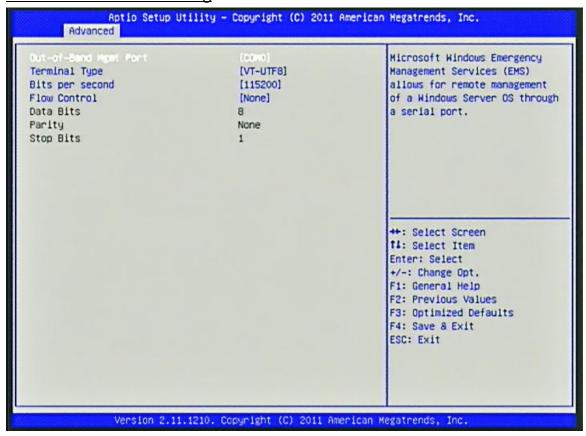
Choices: Disabled, Enabled,

WatchDog Timer

Serial Port Console Redirection



Console Redirection Setting



Out-Of-Band Mgmt Port

Choices: COM0, COM1

Terminal Type

Choices: VT100, VT100+, VT-uTF8, ANSI

Bits per second

Choices: 9600, 19200, 57600, 115200.

Flow Control

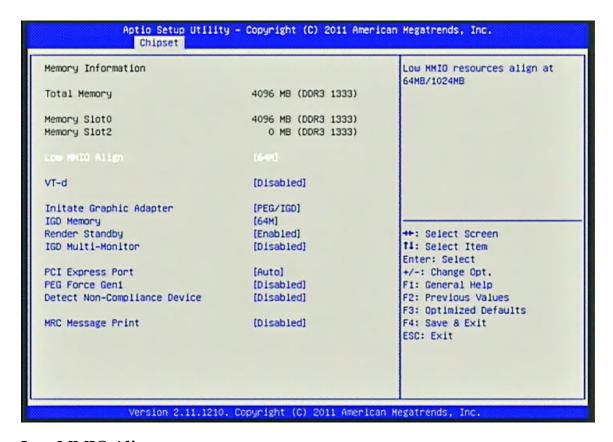
Choices: None, Hardware RTS/CTS, Software Xon/Xoff.

4.4 Chipset

This menu controls the advanced features of the onboard North Bridge and South Bridge



North Bridge



Low MMIO Align

Low MMIO resources align at 64MB/1024MB.

Choices: 64M, 1024M.

VT-d

Choices: Disabled, Enabled.

Intel Graphic Adapter

Select which graphics controller to use as the primary boot device.

Choices: IGD, PCI/IGD, PCI/PEG, PEG/IGD, PEG/PCI.

IGD Memory

IGD Share Memory Size.

Choices: Disabled, 32M~1024M...

Render Standby

Enable/Disable Render Standby by Internal Graphics Device.

Choices: Disabled, Enabled.

IGD Multi-Monitor

Enable/Disable IGD Multi-Monitor by Internal Graphics Device.

PCI Express Port

Choices: Disabled, Enabled, Auto.

PEG Force Gen1

PCI Express Port Force Gen1. Choices: Disabled, Enabled.

Detect Non-Compliance Device

Detect Non-Compliance PCI Express Device in PEG.

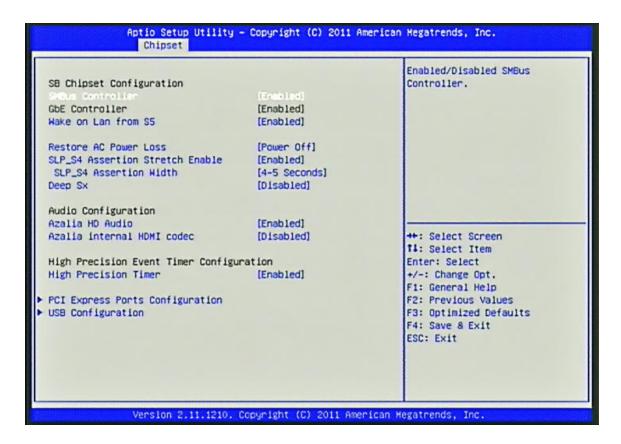
Choices: Disabled, Enabled.

MRC Message Print

Print Memory initialize message.

Choices: Disabled, Enabled.

South Bridge



SMBus Controller

Choices: Disabled, Enabled.

Wake on Lan from S5

Enabled/Disabled GbE control PME in S5.

Restore AC Power Loss

Specify what state to go to when power is re-applied after a power failure (G3 State).

Choices: Power Off, Power On, Last State.

SLP_S4 Assertion Stretch Enable

Enabled/Disabled SLP_S4# Assertion Stretch.

Choices: Disabled, Enabled.

SLP_S4 Assertion Stretch Width

Select a minimum assertion width of the SLP_S4# Assertion signal.

Choices: 1-2 Seconds, 2-3 Seconds, 3-4 Seconds, 4-5 Seconds.

Deep Sx

Deep Sx configuration. Note: Mobile platforms support Deep S4/S5 in DC only and Desktop platforms support Deep S4/S5 in AC only.

Choices: Disabled, Enabled in S5 (Battery), Enabled in S4 and S5 (Battery), Enabled in S4 and S5.

Azalia HD Audio

Enabled/Disabled Azalia HD Audio.

Choices: Disabled, Enabled.

Azalia Intermal HDMI codec

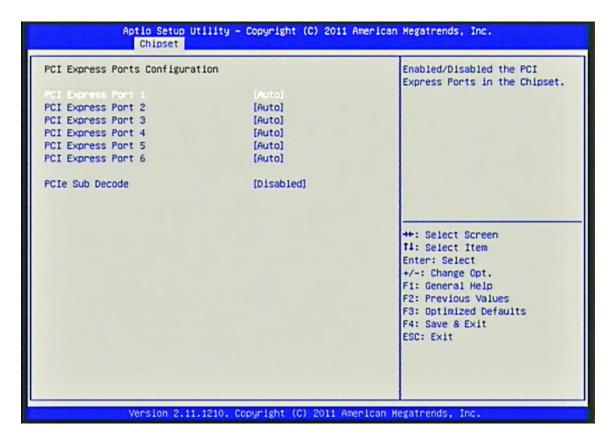
Enabled/Disabled internal HDMI codec for Azalia.

Choices: Disabled, Enabled.

High Precision Timer

Enabled/Disabled the High Precision Event Timer.

PCI Express Ports Configuration



PCI Express Port 1/2/3/4/5/6

Choices: Disabled, Enabled, Auto.

PCIe Sub Decode

Enabled/Disabled PCIe Sub Decode Port. (This option is available when Subtractive Decode Agent Enable. (PCHTrap9 [14] = '1b')

Software Memory Test

Choices: Disabled, Enabled.

Patrol Scrub

Choices: Disabled, Enabled.

Demand Scrub

Choices: Disabled, Enabled.

Fast MRC

Choices: Disabled, Enabled.

DDR3 Memory Operating Speed

Choices: Auto, 1333MHz, 1067MHz, 800MHz.

Memory Rank Margining

Choices: Auto, 1333MHz, 1067MHz, 800MHz.

Closed Loop Throttling

Choices: Disabled, Enabled.

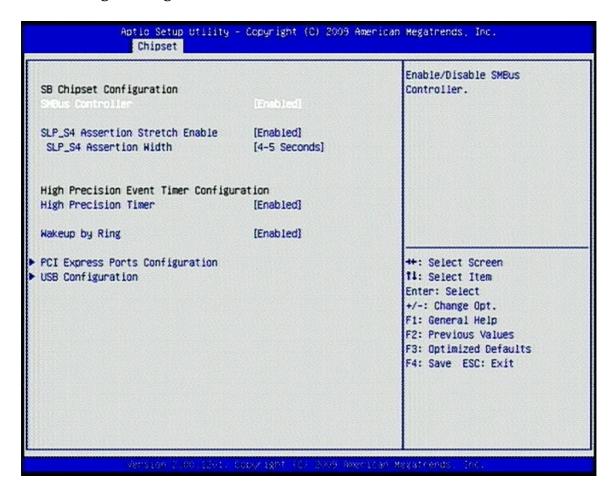
Open Loop Throttling

Choices: Disabled, Enabled.

DIMM Information

Display DIMM presence and size information.

South Bridge Configuration



SMBus Controller

Choices: Disabled, Enabled,

SLP_S4 Assertion Stretch Enable

Choices: Disabled, Enabled,

SLP_S4 Assertion Width

Choices: 1-2, 2-3. 3-4, 4-5 seconds

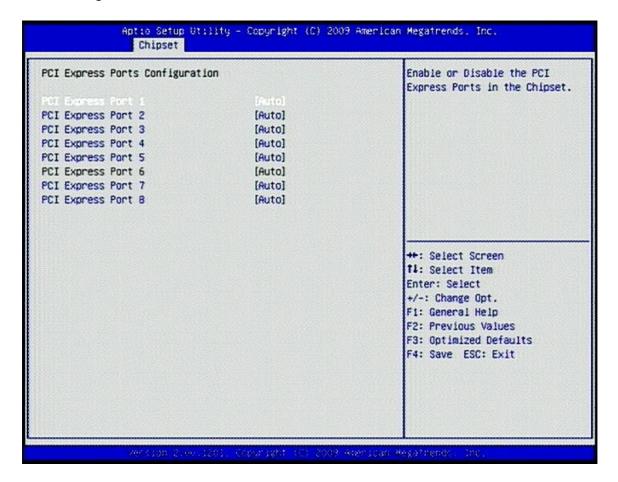
High Precision timer

Choices: Disabled, Enabled,

Wakeup by Ring

PCI Express Ports Configuration

All PCI Express Ports can be set as choices: Disabled, Enabled, Auto



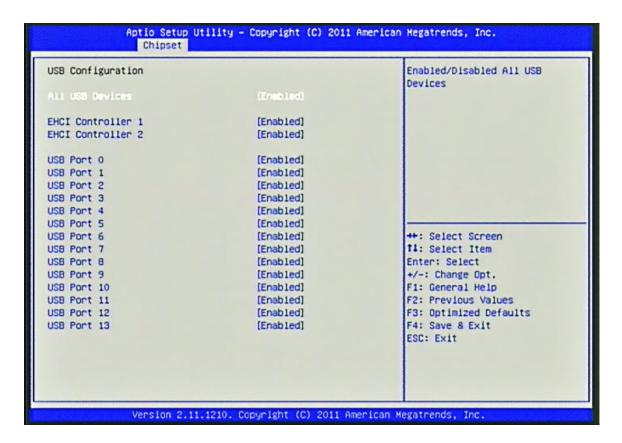
PCI Express Port 1/2/3/4/5/6

Choices: Disabled, Enabled, Auto.

PCIe Sub Decode

Enabled/Disabled PCIe Sub Decode Port. (This option is available when Subtractive Decode Agent Enable. (PCHTrap9 [14] = '1b')

USB Configuration



All USB Devices

Enabled/Disabled All USB Devices.

Choices: Disabled, Enabled.

EHCI Controller 1/2

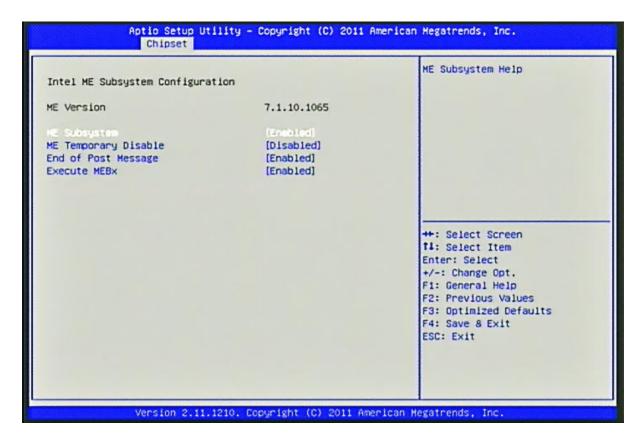
Enabled/Disabled USB2.0 (EHCI) Support.

Choices: Disabled, Enabled.

USB Port 0-13

Enabled/Disabled USB Port 0-13

ME Subsystem



ME Subsystem

Choices: Enabled, Disabled.

ME Temporary Disable

Choices: Enabled, Disabled.

End of Post Message

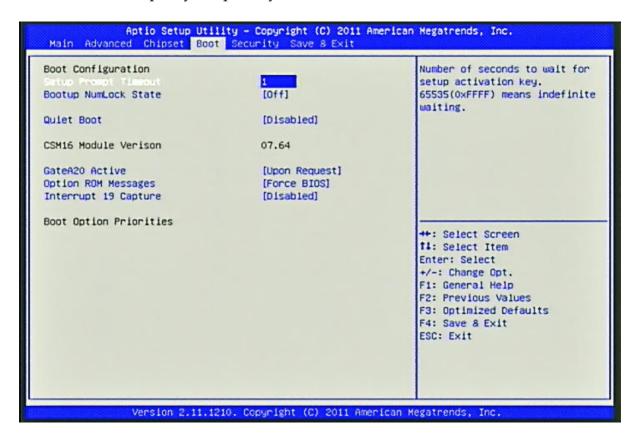
Choices: Enabled, Disabled.

Execute MEBx

Choices: Enabled, Disabled.

4.5 Boot

Use this menu to specify the priority of boot devices.



Setup Prompt Timeout

Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.

Choices: 1-65535.

Bootup Num-Lock State

Select the keyboard Numlock state.

Setting to [On] will turn on the Num Lock key when the system is powered on. Setting to [Off] will allow users to use the arrow keys on the numeric keypad.

Choices: On, Off.

Quiet Boot

Enables or disables Quiet Boot option.

This BIOS feature determines if the BIOS should hide the normal POST messages with the motherboard or system manufacturer's full-screen logo. When it is enabled, the BIOS will display the full-screen logo during the boot-up sequence, hiding normal POST messages.

When it is disabled, the BIOS will display the normal POST messages, instead of the full-screen logo.

Please note that enabling this BIOS feature often adds 2-3 seconds of delay to the booting sequence. This delay ensures that the logo is displayed for a sufficient amount of time. Therefore, it is recommended that you disabled this BIOS feature for a faster boot-up time.

Choices: Disabled, Enabled.

GateA20 Active

UPON REQUEST – GA20 can be disabled using BIOS services. ALWAYS – do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.

Choices: Upon Request, Always.

Option ROM Messages

Set Display mode for Option ROM.

This item is used to determine the display mode when an optional ROM is initialized during POST. When set to [Force BIOS], the display mode used by AMI BIOS is used. Select [Keep Current] if you want to use the display mode of optional ROM.

Choices: Force BIOS, Keep Current.

Interrupt 19 Capture

Enabled: Allows Option ROMs to trap Int 19.

Interrupt 19 is the software interrupt that handles the boot disk function. When Enabled, this BIOS feature allows the ROM BIOS of these host adaptors to "capture" Interrupt 19 during the boot process so that drives attached to these adaptors can function as bootable disks. In addition, it allows you to gain access to the host adaptor's ROM setup utility, if one is available.

When Disabled, the ROM BIOS of these host adaptors will not be able to "capture" Interrupt 19. Therefore, you will not be able to boot operating systems from any bootable disks attached to these host adaptors. Nor will you be able to gain access to their ROM setup utilities.

Choices: Disabled, Enabled.

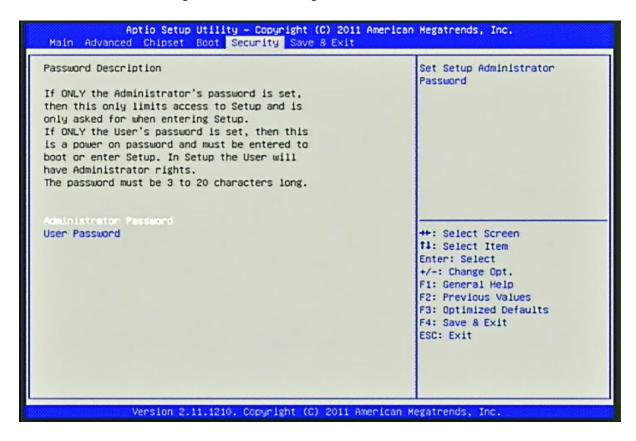
Boot Option #1

Sets the system boot order.

Choices: Built-in EFI Shell, other bootable devices, Disabled.

4.6 Security

Use this menu to set supervisor and user passwords.



Administrator Password

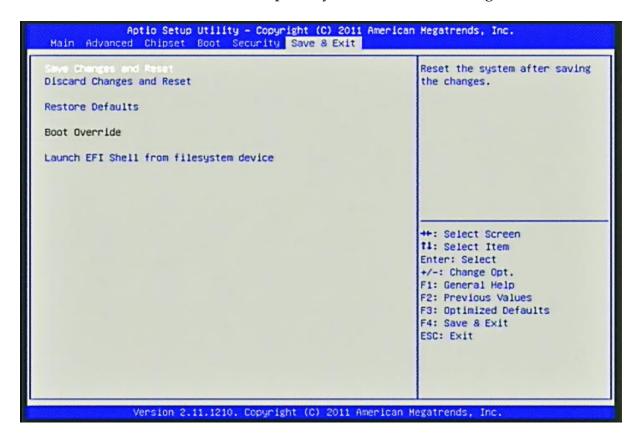
Set Setup Administrator Password.

User Password

Set User Password.

4.7 Save & Exit

This menu allows you to load the BIOS default values or factory default settings into the BIOS and exit the BIOS setup utility with or without changes.



Save Changes and Reset

Reset the system after saving the changes.

Pressing <Enter> on this item asks for confirmation: Save configuration and reset.

Discard Changes and Exit

Reset system setup without saving any changes.

Restore Defaults

Restore/Load Default values for all the setup options.

Launch EFI Shell from filesystem device

To enter the Built-in EFI shell for further modification such as upgrade BIOS.

Built-in EFI Shell

Boot into the initial shell environment, it can debug and dump the PCI Resource or jump to next bootable device. If it doesn't have boot device, it will return to BIOS setup menu. If you want to know the shell command, you can visit the Intel official hyperlink as below.

http://software.intel.com/en-us/articles/uefi-shell/#Internal_EFI_Shell_Comm ands

Chapter 5 Troubleshooting

This chapter provides a few useful tips to quickly get ROBO-8110VG2AR running with success. As basic hardware installation has been addressed in Chapter 2, this chapter will primarily focus on system integration issues, in terms of BIOS setting, and OS diagnostics.

5.1 Hardware Quick Installation

ATX Power Setting

Unlike other Single board computer, ROBO-8110VG2AR supports ATX only. Therefore, there is no other setting that really needs to be set up. However, there are only two connectors that must be connected—J10 (4 pins CPU +12V main power connector) & 24 pins ATX Power Connector.

Serial ATA Hard Disk Setting for IDE/AHCI

Unlike IDE bus, each Serial ATA channel can only connect to one SATA hard disk at a time; there are total six connectors, J19 & J20, J22, J23 Four ports on-board (those 4 Masters in Non-AHCI mode), two support 6Gb + two support 3Gb and two ports route to backplane support 3Gb, because SATA hard disk doesn't require setting up Master and Slave, which can reduce mistake of hardware installation. All you need to operate IDE and AHCI application for system, please follow up setting guide in BIOS programming (Table 5-1); Furthermore, you can consult chapter 4.3

Advanced "SATA Configuration" part of the "SATA Mode".

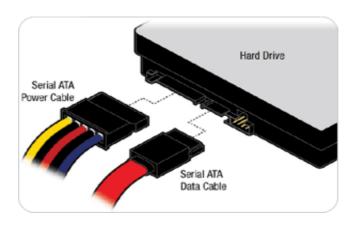
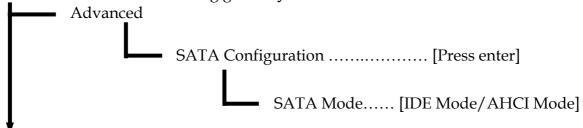


Table. 5-1 SATA Mode setting guide System BIOS Main Menu



5.2 BIOS Setting

It is assumed that users have correctly adopted modules and connected all the devices cables required before turning on ATX power. 240-pin DDR3 Memory, keyboard, mouse, SATA hard disk, VGA connector, device power cables, ATX accessories are good examples that deserve attention. With no assurance of properly and correctly accommodating these modules and devices, it is very possible to encounter system failures that result in malfunction of any device.

To make sure that you have a successful start with ROBO-8110VG2AR, it is recommended, when going with the boot-up sequence, to hit "DEL" key and enter the BIOS setup menu to tune up a stable BIOS configuration so that you can wake up your system far well.

Loading the default optimal setting

When prompted with the main setup menu, please scroll down to "Restore Defaults", press "Enter" and select "Yes" to load in default optimal BIOS setup. This will force your BIOS setting back to the initial factory configuration. It is recommended to do this so you can be sure the system is running with the BIOS setting that Portwell has highly endorsed. As a matter of fact, users can load the default BIOS setting any time when system appears to be unstable in boot up sequence.

Improper Disable Operation

There are too many occasions where users disable a certain device/feature in one application through BIOS setting. These variables may not be set back to the original values when needed. These devices/features will certainly fail to be detected.

When the above conditions happen, it is strongly recommended to check the BIOS settings. Make sure certain items are set as they should be. These include the Serial Port1/ Serial Port 2 ports, USB ports, external cache, on-board VGA and Ethernet.

It is also very common that users would like to disable a certain device/port to release IRQ resource. A few good examples are

Disable Serial Port1 to release IRQ #4 Disable Serial Port2 to release IRQ #3 Etc... A quick review of the basic IRQ mapping is given below for your reference.

IRQ#	Description
IRQ #0	System Timer
IRQ #1	Keyboard Event
IRQ #2	Usable IRQ
IRQ #3	COM2
IRQ #4	COM1
IRQ #5	Usable IRQ
IRQ #6	Diskette Event
IRQ #7	Usable IRQ
IRQ #8	Real-Time Clock
IRQ #9	Usable IRQ
IRQ #10	Usable IRQ
IRQ #11	Usable IRQ
IRQ #12	IBM Mouse Event
IRQ #13	Coprocessor Error
IRQ #14	Hard Disk Event
IRQ #15	Usable IRQ

5.3 FAQ

Symptom: SBC keeps beeping, and no screen has shown.

Solution: In fact, each beep sound represents different definition of error message. Please refer to table as following:

Beep sounds	Meaning	Action
One long beep with one	DRAM error	Change DRAM or reinstall it
short beeps		
One long beep	DRAM error	Change DRAM or reinstall it
constantly		_
One long beep with two	Monitor or Display	Please check Monitor connector
short beeps	Card error	whether it inserts properly
Beep rapidly	Power error warning	Please check Power mode
		setting

Information & Support

Question: I forget my password of system BIOS, what am I supposed to do?

Answer: You can simply short 2-3 pins on JP9 to clean your password.

Question: How to update the BIOS file of the ROBO-8110VG2AR?

Answer: 1. Please visit web site of the Portwell download center as below hyperlink and register an account.

http://www.portwell.com.tw/support/newmember.php

- 2. Input your User name and password to log in the download center.
- 3. Select the "Search download" to input the keyword "ROBO-8110VG2AR".
- 4. Find the "BIOS "page to download the ROM file and flash utility.
- 5. Execute the zip file to root of the bootable USB pen drive.
- 6. Insert your bootable USB pen drive in ROBO-8110VG2AR board and power-on.
- 7. Input the "AFUDOS XXXXX.ROM -p -b -n" to start to update BIOS. ("XXXXX" is the file name of the ROM file.)
- 8. Switch "Off" the Power Supply when you finished the update process.
- 9. To short the JP9 jumper from 1-2 short to 2-3 short 5 seconds then set back to 1-2 short. (Clear CMOS)
- 10. Switch "ON" the Power Supply then press the "del" key to BIOS to load "Restore Defaults" and then select "Save Changes and Exit" option.

Note:

Please visit our technical web site at

http://www.portwell.com.tw

For additional technical information, which is not covered in this manual, you can mail to tsd@mail.portwell.com.tw or you can also send mail to our sales, they will be very delighted to forward them to us.

System Memory Address Map

Each On-board device in the system is assigned a set of memory addresses, which also can be identical of the device. The following table lists the system memory address used for your reference.

Memory Area	Size	Description
0000-003F	1K	Interrupt Area
0040-004F	0.3K	BIOS Data Area
0050-006F	0.5K	System Data
0070-0E2E	54K	DOS
0E2F-0F6B	5K	Program Area
0F6C-9BFF	562K	[Available]

First Meg	eg Conventional memory end at 624K		
9C00-9D3F	5K	Extended BIOS Area	
9D40-9FFF	11K	Unused	
A000-AFFF	64K	VGA Graphics	
B000-B7FF	32K	Unused	
B800-BFFF	32K	VGA Text	
C000-CD7F	54K	Video ROM	
CD80-EFFF	138K	Unused	
F000-FFFF	64K	System ROM	
HMA	64K	First 64K Extended	

Interrupt Request Lines (IRQ)

Peripheral devices can use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Interrupt Request Lines IRQ			
IRQ#	Current Use	Default Use	
IRQ 0	System ROM	System Timer	
IRQ 1	System ROM	Keyboard Event	
IRQ 2	【Unassigned】	Usable IRQ	
IRQ 3	System ROM	COM2	
IRQ 4	System ROM	COM1	
IRQ 5	【Unassigned】	Usable IRQ	
IRQ 6	System ROM	Diskette Event	
IRQ 7	【Unassigned】	Usable IRQ	
IRQ 8	System ROM	Real-Time Clock	
IRQ 9	【Unassigned】	Usable IRQ	
IRQ 10	【Unassigned】	Usable IRQ	
IRQ 11	Video ROM	Usable IRQ	
IRQ 12	System ROM	IBM Mouse Event	
IRQ 13	System ROM	Coprocessor Error	
IRQ 14	System ROM	Hard Disk Event	
IRQ 15	【Unassigned】	Usable IRQ	