1746-SMPTE

User's Guide

by Alcorn McBride Inc.

Document Revision 1.0

September 1997

Every effort has been made to assure the accuracy of the information contained in this manual, and the reliability of the hardware and software. Errors sometimes can go undetected, however. If you find one, please bring it to our attention so that we can correct it for others.

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Welcome

Since the first V16 was introduced in 1986, Alcorn McBride has been providing high quality show control solutions to the entertainment industry. The 1746-SMPTE module brings that same power to the Allen-Bradley family of programmable logic controllers. We at Alcorn McBride are pleased to provide you with these tools. Good luck, have fun, and thanks for choosing Alcorn McBride!

What is SMPTE Time Code?

Think for a moment about any recorded performance. It could be a stereo recording of a symphony orchestra, a video of your child's birthday party, or your favorite motion picture. It would be very desirable to know the length of the performance, and to be able to jump in to any point in the recording accurately. Early systems provided such capabilities by linking a mechanical counter to the tape or film reels. By counting revolutions of the reel, one could return to the same point in the recording repeatably, and get some sense of the overall length of the piece.

Mechanical or electronic counters work very well. In fact, they are still in widespread use in much of today's audio and video equipment. However, they do have drawbacks, such as the lack of consistency from one machine to another, and the fact that the counts can change when the tape gets edited or copied.

A far more accurate system would encode the time information as a part of the presentation itself, perhaps as an additional track of a multi-track audio recording. This is exactly the technique that was standardized in 1981 by the Society of Motion Picture and Television Engineers (SMPTE) and subsequently adopted by the European Broadcast Union (EBU). The complete standard was published as ANSI V98.12M-1981, and is generally known as the SMPTE/EBU Longitudinal Time Code, or more simply, SMPTE Time Code.

To achieve film-like editing capability, SMPTE Time Code represents time in hours, minutes, seconds, and frames. The common frame rates are 24 frames per second for film work, 25 frames per second for European television, 30 frames per second for NTSC black and white television, and 29.97 frames per second for NTSC color television. A typical SMPTE readout looks like 02:28:35:15, indicating 2 hours, 28 minutes, 35 seconds, and 15 frames.

SMPTE Time Code is often used to synchronize various elements of a complex presentation. Equipment such as film projectors, video sources, audio systems, lighting consoles, and motion controllers can read the time code to remain at the proper point in the show at all times.

The 1746-SMPTE brings the ability to read and generate SMPTE/EBU time code to the Allen Bradley family of programmable logic controllers. The module is compatible with all processors in the SLC 500 family, including the 5/01, 5/02, 5/03, and 5/04 processors.

Technical Support

You can obtain information about specifying, installing, configuring, and programming your Alcorn McBride 1746-SMPTE from several sources:

For…	Contact…	When?…
Telephone Support	(407) 296-5800	M-F 9am–6pm (EST)
Fax Support	(407) 296-5801	M-F 9am-6pm (EST)
E-Mail Support	support@alcorn.com	Any Time

Installing the 1746-SMPTE

The Alcorn McBride 1746-SMPTE plugs directly into a standard SLC 500 PLC chassis. The module is compatible with all SLC modular processors, including the SLC 5/01, 5/02, 5/03, and 5/04.

Setting the SMPTE Output Level

If the module is being used to generate SMPTE time code, set the SMPTE time code output level before installing the module in the chassis. The 1746-SMPTE includes one eight-position switch, labeled SW1 on the circuit board, to select the output level, measured in volts peak to peak.

		Switch SW1 Settings							
		1	2	3	4	5	6	7	8
Output Level	4.0 Vpp	**On**	Off	Off	Off	Off	Off	Off	Off
	3.5 Vpp	Off	**On**	Off	Off	Off	Off	Off	Off
	3.0 Vpp	Off	Off	**On**	Off	Off	Off	Off	Off
	2.5 Vpp	Off	Off	Off	**On**	Off	Off	Off	Off
	2.0 Vpp	Off	Off	Off	Off	**On**	Off	Off	Off

Module Power Consumption

The 1746-SMPTE module draws a maximum of 0.350 Amps at 5 VDC. The module does not use the 24 VDC power supply.

Installing the Module in the SLC 500 Chassis

Attention! Never install or remove any module while power is applied.

Installing the Module

Align the module circuit board with the card guides in the chassis.

Gently push the module in until it is firmly seated, with the retaining clips engaged at the top and bottom.

Removing the Module

Press the retaining clips at the top and bottom of the module and slide the module straight out of the chassis.

Wiring the Module

Attention! Never wire any module while power is applied.

The module wiring terminals accept two wires per terminal (maximum) of 14 AWG or smaller stranded wire. Maximum screw torque is 8 in-lb.

The module terminal block is removable. Simply unscrew the upper right and lower left release screws and pull the entire terminal block straight out. When replacing the terminal block, alternate the tightening of the release screws to avoid cracking the block. Maximum screw torque is 8 in-lb.

SMPTE Input

When the 1746-SMPTE is used to read external time code, the signal is connected to this input. The input is transformer balanced with a 600 ohm characteristic input impedance, and can accept signals from 2 Vpp to 5 Vpp. Connect the positive drive to the terminal labeled 'IN (+)' and the negative drive to the terminal labeled 'IN (-)'. There is no terminal for the cable's shield; it should be connected to the chassis ground at the other end of the cable.

SMPTE Output

When the 1746-SMPTE is used to generate or regenerate time code, the signal comes out of this output. The output is transformer balanced to drive a 600 ohm load, and can output signals from 2 Vpp to 4 Vpp, as selected by switch SW1. Connect the terminal labeled 'OUT (+)' to the positive drive and the terminal labeled 'OUT (-)' to the negative drive. There is no terminal for the cable's shield; it should be connected to the chassis ground at the other end of the cable.

Module I/O Space

The 1746-SMPTE module uses ID code 3535, which indicates that it is a Class 1 module with I/O mix of 8 input words and 8 output words and I/O type of third party. All communications with the 1746-SMPTE takes place through the Output and Input Data Files. The module occupies eight words in the Output File and eight words in the Input File.

Output File

The eight words in the output file configure and control the SMPTE module.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	x	x	x	x	x	Frame Rate			Mode	Mute	x	Loop	x	Set	Stop	Run
1	Dropout Tolerance															
2	Set Hours								Set Minutes							
3	Set Seconds								Set Frames							
4	Loop Start Hours								Loop Start Minutes							
5	Loop Start Seconds								Loop Start Frames							
6	Loop End Hours								Loop End Minutes							
7	Loop End Seconds								Loop End Frames							

Module Output File

The next two chapters contain complete descriptions of the function of each word in the Output File.

Bits marked ‘x’ are reserved for future use. They should always be set to zero.

Input File

The eight words in the input file indicate module status to the PLC.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Hours															
1	Minutes															
2	Seconds															
3	Frames															
4	x	x	x	x	x	Drop	Gen	Lock	Frame Rate							
5	Error Codes															
6	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
7	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Module Input File

The next two chapters contain complete descriptions of the function of each word in the Input File.

Bits marked ‘x’ are reserved for future use. They are all set to zero.

Using the Module as a SMPTE Generator

The 1746-SMPTE contains a very versatile SMPTE generator, which has been designed for flexibility and ease of use. With this generator, one can easily accomplish many tasks:

- Produce SMPTE time code at all common frame rates.
- Roll time code from a start point to an end point.
- Create an automatic loop of time code that will continue running without further intervention.
- Create jumps or discontinuities in the time code.

Generator Theory of Operation

The SMPTE generator is always active in order to produce an internal frame clock. Every frame, the time code output advances by one frame (if the generator is running), or remains unchanged (if the generator is idling). When the generator is idling, the output can be muted to prevent transmitting the same SMPTE code over and over.

The generator constantly compares the SMPTE output to the user's Loop End Time (contained in the Output File). When the current time reaches the Loop End time, the generator will automatically jump to the Loop Start time or halt, depending on the setting of the Loop bit. The jump can be disabled by simply setting the Loop Start time equal to the Loop End time. In this case, the generator will either keep running or stop at the Loop End Time, depending on the setting of the Loop bit.

The output time code is always available to the PLC through the Input File. The PLC can use this information to trigger execution of rungs, or to reload the SMPTE generator at a specific time to create a controlled jump in the time code output.

The SMPTE generator follows a simple process to generate time code. Each frame, the module performs these tasks:

1. Convert the current time to a string of 80 bits and if the generator is not muted, send those bits out the SMPTE output.
2. If the STOP bit has changed from a zero to a one, switch the generator from RUNNING to IDLING.
3. If the RUN bit has changed from a zero to a one, switch the generator from IDLING to RUNNING.
4. If the SET bit has changed from a zero to a one, replace the current time with the user's new time code, otherwise, add one frame to the current time if running or leave the current time unchanged if idling.
5. If the current time matches the Loop End time, replace the current time with the Loop Start Time if the Loop bit is set (one), or switch from RUNNING to IDLING if the Loop bit is clear (zero).
6. If the unit is idling and the MUTE bit is set, mute the SMPTE output.
7. Make the time code available to the PLC through the Input File.

Configuring the Generator

The 1746-SMPTE generator is entirely controlled by words in the PLC Output File. See the Module I/O Space chapter for a diagram of the Output File.

Operating Mode

When the MODE bit is set (one), the module will generate SMPTE time code internally. When this bit is clear (zero) the module will read external SMPTE time code.

Frame Rate

The generated SMPTE frame rate is determined by this 3-bit field.

	Bit 0/10	Bit 0/9	Bit 0/8
30 fps	0	0	0
29.97 fps non-drop	0	0	1
29.97 fps drop	0	1	0
25 fps	0	1	1
24 fps	1	0	0
23.976 fps	1	0	1

The other two codes (110 and 111) are reserved for future use.

Loop Start, End Times

When the SMPTE output reaches the Loop End Time, it immediately jumps to the Loop Start Time if the LOOP bit is set, or halts if the LOOP bit is clear. Any invalid entries, such as minutes greater than 59, will be treated as if the entry were zero. An error bit will be set in the Input File to highlight the problem field.

Loop Behavior

If the LOOP bit is set (one), then when the SMPTE output reaches the Loop End Time, the generator will jump to the Loop Start Time and continue generating from there. If the LOOP bit is clear (zero), then the SMPTE output will stop at the Loop End Time. Notice that by setting the Loop Start Time equal to the Loop End Time, the module can be made to generate a continuous, unbroken 24 hour long loop of time code. Also, the Loop Start Time need not be smaller than the Loop End Time. Time code rolls over at 23:59:59:29, so the End Time will be reached eventually.

Mute Behavior

If the MUTE bit is set (one), then the SMPTE output is muted. Time code can continue to be generated internally, but the output does not send the code. It is as if the cable has been unplugged. If the MUTE bit is clear (zero), then the SMPTE output sends whatever time code is being produced internally.

Dropout Tolerance

Only the SMPTE reader uses this word. It may be set to any value when generating time code; the module will ignore it entirely.

Controlling the Generator

The 1746-SMPTE generator is entirely controlled by words in the PLC Output File. See the Module I/O Space chapter for a diagram of the Output File.

Note: The 1746-SMPTE samples the control bits once per frame. Pulses of less than 33 milliseconds will not activate the module properly.

Setting the Current Time

Whenever the SET bit transitions from a zero to a one, the SMPTE time in the Set Time words will be loaded into the SMPTE generator's output. The load occurs at the next frame edge, so the time can be altered while the generator is running or while it is idling. Any invalid entries, such as minutes greater than 59, will be treated as if the entry were zero. An error bit will be set in the Input File to highlight the problem field.

Starting the Generator

Whenever the RUN bit transitions from a zero to a one, the generator switches from IDLING to RUNNING. If the generator is already running, the rising edge on the RUN bit has no effect.

Stopping the Generator

Whenever the STOP bit transitions from a zero to a one, the generator switches from RUNNING to IDLING. If the generator is already idling, the rising edge on the STOP bit has no effect.

Monitoring the Status of the Generator

The 1746-SMPTE generator communicates its status to the PLC through the Input File. See the Module I/O Space chapter for a diagram of the Input File.

Current Time

The current output SMPTE time code is always available through four words in the PLC Input File.

Word 0, hours, will always be between 0 and 23, inclusive.

Word 1, minutes, will always be between 0 and 59, inclusive.

Word 2, seconds, will always be between 0 and 59, inclusive.

Word 3, frames, will always be between 0 and 29, inclusive.

Note: Word 3, frames, can change 30 times per second. This could impact your programming technique if your program's scan time exceeds 33 milliseconds.

Current Frame Rate

The low byte of word 1 in the Input File always contains the number 24, 25, or 30 to indicate the frame sequence of the output time code. For example, 24 frame time code always rolls over from frame number 23 to frame number 0. No distinction is made between 23.976 and 24 frame rates, or between 29.97 and 30 frame rates.

Locked

This bit will always be clear (zero) when generating time code. It is used only by the SMPTE reader to indicate incoming time code lock.

Self-Generating

Whenever the internal SMPTE generator is running, this bit in the Input File is set (one). If the internal generator switches into idle mode, this bit will be cleared.

Drop Frame

If the output time code has its drop frame flag set, then this bit will be set. If the output code is not a drop frame code, then this bit will be clear.

Error Codes

The bits in the error code word indicate invalid entries in the Output File.

Error Bit	Entry
0	Set Time Hours
1	Set Time Minutes
2	Set Time Seconds
3	Set Time Frames
4	Loop Start Time Hours
5	Loop Start Time Minutes
6	Loop Start Time Seconds
7	Loop Start Time Frames
8	Loop End Time Hours
9	Loop End Time Minutes
10	Loop End Time Seconds
11	Loop End Time Frames
12-15	Reserved for future use

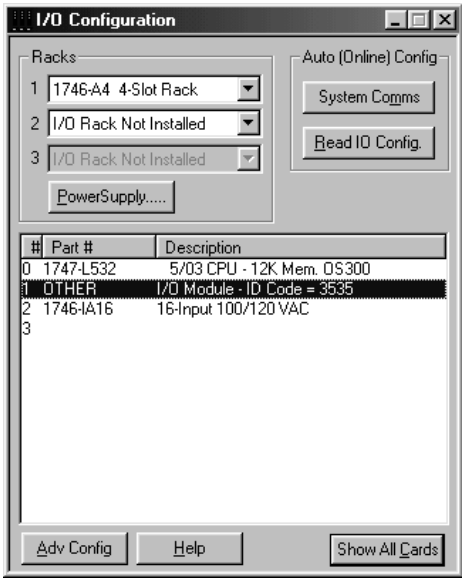
Any invalid entry in the Output File will cause the corresponding bit in the error code word to be set (one). For example, if the Loop End Time Minutes byte in the Output File contains a 63, which is an invalid number of minutes, then bit 9 of the error code word in the Input File will be set.

Invalid entries in the Output File are treated as if the entries were zero.

Typical Applications & Sample Rungs

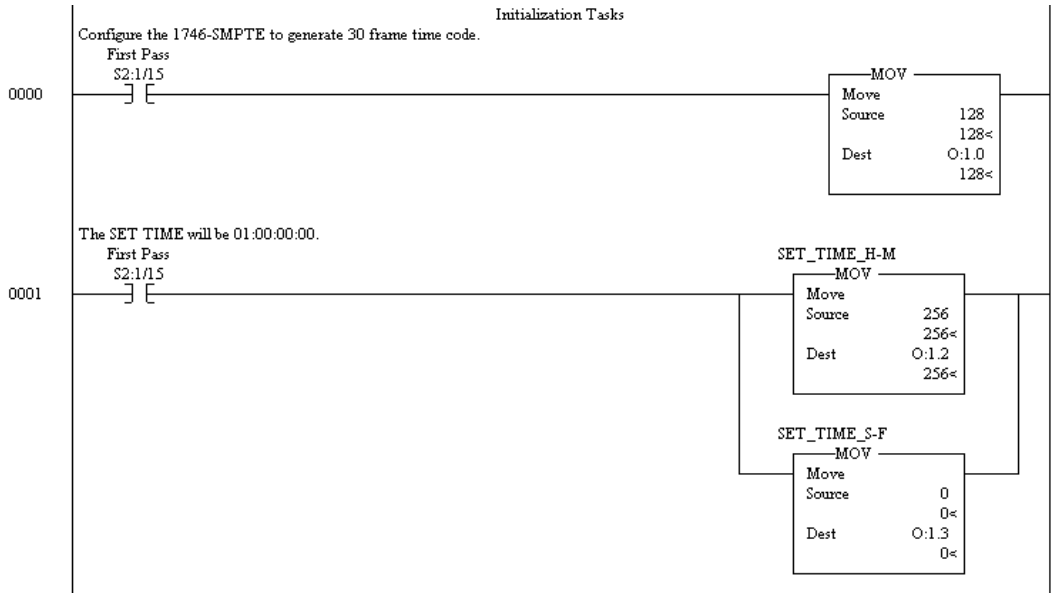
In this example, the 1746-SMPTE generates a short section of time code, under the control of two external inputs to the PLC.

The PLC includes a 5/03 processor, the Alcorn McBride 1746-SMPTE module, and a simple input module.

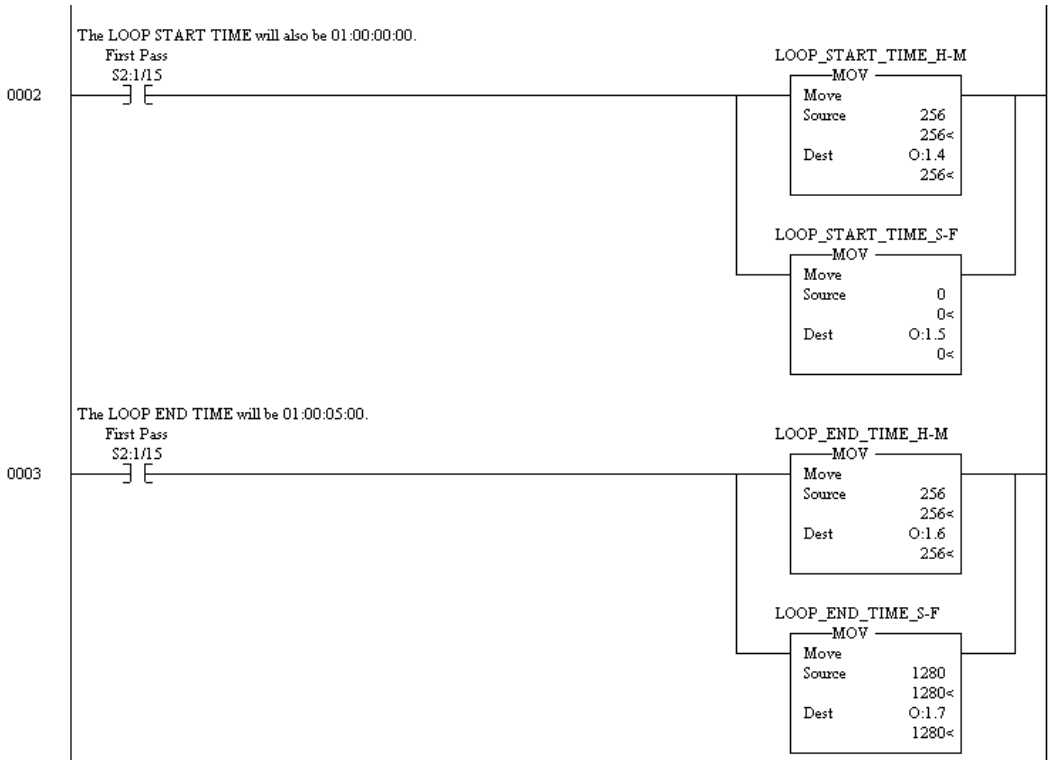


When the PLC switches to run mode, the first pass bit, S2:1/15, causes the following rungs to execute. Rung 0000 sets the generator's fundamental operating parameters, in word 0 of the output file. The value 128 causes bit 7 of word 0 to be set, and all other bits to be clear. Bit 7 is the operating mode: setting this bit configures the module to generate time code. Bits 10-8 determine the frame rate: the code 000 represents 30 frames per second. Bit 4 controls looping: clearing this bit causes the generator to stop when it reaches the end time.

Rung 0001 initializes the SET TIME to 01:00:00:00.

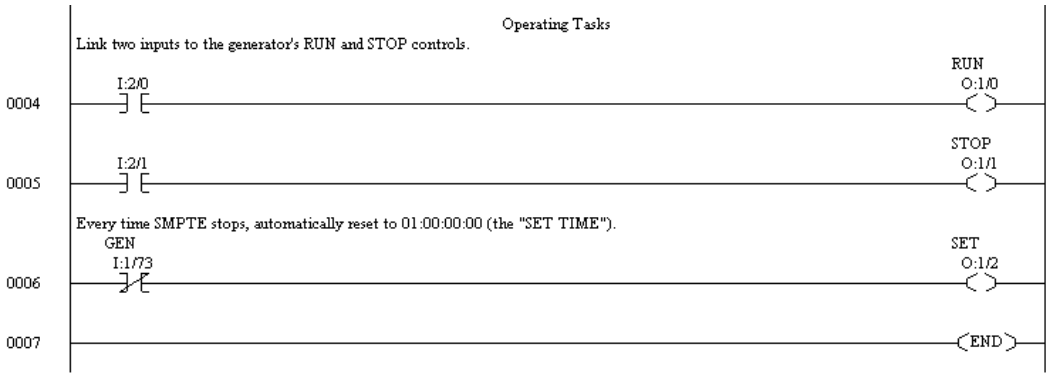


Continuing the initialization tasks, rungs 0002 and 0003 set the LOOP START TIME and the LOOP END TIME.



Once the PLC is running, rungs 0004 and 0005 continuously test two input bits and link them to the 1746-SMPTE RUN and STOP controls. These inputs can be used to give external equipment direct control over the SMPTE generator's operation.

Rung 0006 monitors the 'generate' status bit in the 1746-SMPTE input file to activate the SET control whenever the generator stops producing time code. This means that every time the generator stops, it is automatically reset to the SET time.



Using the Module as a SMPTE Reader

The 1746-SMPTE contains a robust SMPTE reader/regenerator, which has been designed for flexibility and ease of use.

- Read external SMPTE time code at all common frame rates.
- Automatically detect changes in frame rate.
- Regenerate fresh time code from a noisy or partially corrupted source.
- Flywheel through dropouts in the incoming time code, with adjustable tolerance.

Reader Theory of Operation

Whenever the 1746-SMPTE is in read mode, it constantly searches for valid incoming time code. As soon as two consecutive valid frames arrive, the reader locks its internal generator to the incoming code. As long as the incoming code remains valid, the generator remains in lock.

The reader constantly tests the incoming time code to be sure it remains good. This means that each frame must contain 80 good SMPTE bits, and also, the time code must be rolling forward one frame at a time or must be idling (no change in frame number).

If the incoming time code becomes corrupted, the internal generator will continue to produce time code through the dropout. The theory is that when good external code returns, the internal generator will still be in sync; the bad portion of the signal has been effectively eliminated.

If the external SMPTE returns and it does not match the internal generator, the internal time code will be locked to the external code after two consecutive valid frames arrive.

The dropout tolerance governs how long the internal generator will function in the absence of good external time code. If the external code drops out for more frames than the dropout tolerance setting, the internal generator goes into idle until good external code is restored.

The regenerated time code is always available to the PLC through the Input File. The PLC can use this information to trigger execution of rungs.

The SMPTE reader performs the following tasks each frame:

1. Receive and decode incoming SMPTE bits.
2. Verify that the received code matches the previously received code or is one frame greater than the previously received code.
3. Automatically detect the frame rate of the incoming code.
4. Lock the internal SMPTE generator to the received code's frame edge.
5. If the incoming code has dropped out, advance the internal generator by one frame.
6. If the signal loss has lasted longer than the dropout tolerance, stop the internal generator.
7. Make the current internal time and frame rate available to the PLC through the Input File.
8. Indicate external lock and internal generate status to the PLC through the Input File.

Configuring the Reader

The 1746-SMPTE reader/regenerator is entirely controlled by words in the PLC Output File. See the Module I/O Space chapter for a diagram of the Output File.

Operating Mode

When the MODE bit is set (one), the module will generate SMPTE time code internally. When this bit is clear (zero) the module will read and regenerate external SMPTE time code.

Dropout Tolerance

If incoming SMPTE time code drops out or becomes corrupt, the 1746-SMPTE will flywheel, or self-generate, time code to cover the gap. The DROPOUT TOLERANCE word sets how many frames of self-generation are allowed before the unit stops self-generating and goes IDLE. A setting of zero frames selects infinite tolerance; the unit will *never* stop self-generation.

Frame Rate

The SMPTE frame rate is automatically determined from the incoming time code. The three-bit Frame Rate field in the PLC Output File is ignored.

Set Time, Loop Start Time, Loop End Time

These words are ignored by the SMPTE reader.

Set Bit, Loop Bit

These bits are not used by the SMPTE reader.

Controlling the Reader

The 1746-SMPTE reader/regenerator is entirely controlled by words in the PLC Output File. See the Module I/O Space chapter for a diagram of the Output File.

Note: The 1746-SMPTE samples the control bits in the output file once per frame. Control pulses of less than 33 milliseconds duration may not activate the module reliably.

Starting the Reader

Whenever the RUN bit transitions from a zero to a one, the reader begins searching for incoming time code. If the reader is already running, the rising edge on the RUN bit has no effect.

When the operating mode is switched from generate to read, or upon entering read mode on powerup, the module automatically begins searching for incoming time code. It is not necessary to activate the RUN bit in this case.

Stopping the Generator

Whenever the STOP bit transitions from a zero to a one, the reader stops searching for incoming time code, and the internal generator goes idle. If the reader is already inactive, the rising edge on the STOP bit has no effect.

Mute Behavior

If the MUTE bit is set (one), then the SMPTE output is muted. Time code can continue to be received, but the output does not retransmit the code. It is as if the output cable has been unplugged. If the MUTE bit is clear (zero), then the SMPTE output sends a regenerated copy of whatever time code is being received.

Monitoring the Status of the Reader

The 1746-SMPTE reader/regenerator communicates its status to the PLC through the Input File. See the Module I/O Space chapter for a diagram of the Input File.

Current Time

The current incoming SMPTE time code is always available through four words in the PLC Input File.

Word 0, hours, will always be between 0 and 23, inclusive.

Word 1, minutes, will always be between 0 and 59, inclusive.

Word 2, seconds, will always be between 0 and 59, inclusive.

Word 3, frames, will always be between 0 and 29, inclusive.

Note: Word 3, frames, can change 30 times per second. This could impact your programming technique if your program's scan time exceeds 33 milliseconds.

Current Frame Rate

The low byte of word 1 in the Input File always contains the number 24, 25, or 30 to indicate the frame sequence of the incoming time code. No distinction is made between 23.976 and 24 frame rates, or between 29.97 and 30 frame rates.

Locked

When the received time code is valid, this bit in the Input File is set (one). If the received time code drops out or becomes corrupt, this bit is cleared.

Self-Generating

Whenever the internal SMPTE generator is running, this bit in the Input File is set (one). If the internal generator switches into idle mode, this bit will be cleared.

Drop Frame

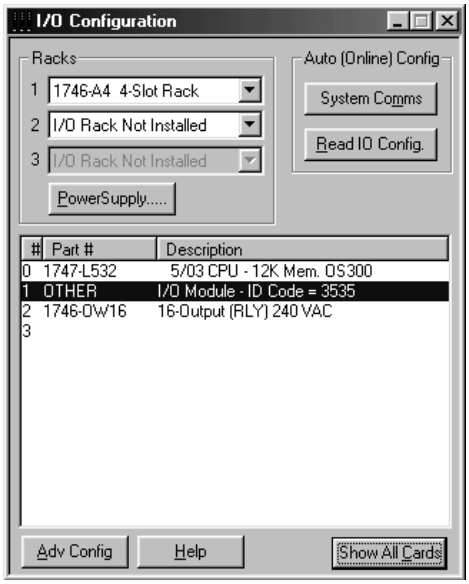
If the incoming time code has its drop frame flag set, then this bit will be set. If the incoming code is not a drop frame code, then this bit will be clear.

Error Codes

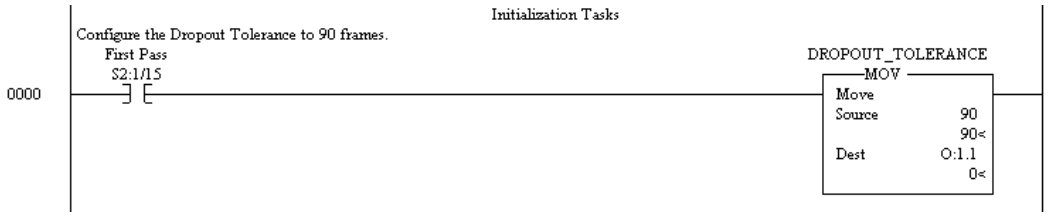
The bits in the error code word indicate invalid entries in the Output File time fields. The SMPTE reader does not produce any additional error codes. See the Generator chapter for a complete description of the error codes.

Typical Applications & Sample Rungs

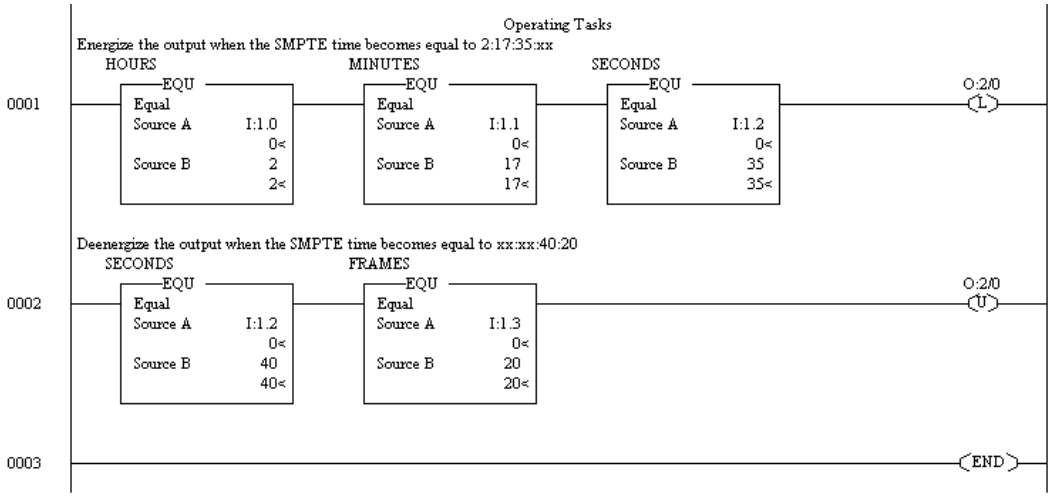
This PLC includes a 5/03 processor, the Alcorn McBride 1746-SMPTE module, and a basic relay output module.



When the PLC switches to run mode, the first pass bit, S2:1/15, causes the following rung to execute. The rung sets the reader's dropout tolerance to 90 frames.



Once the PLC is running, the following rungs continuously test the incoming SMPTE code for specific times. When those times occur, an output bit becomes energized (rung 3) or deenergized (rung 4). This output bit could be used to trigger the execution of additional rungs, or could simply activate some device external to the PLC. Notice that the RUN control bit, O:1/0, was not needed in this example: The 1746-SMPTE automatically entered RUN mode upon startup. Also notice that this program's scan time is fast enough to easily handle the rapidly changing 'frames' word.



Thanks for purchasing the Alcorn McBride 1746-SMPTE module. We hope you'll find that it makes your PLC programming job a little bit easier.