CHAPTER 4

BIOS Setup Information

The ROBO-308 is equipped with the AMI BIOS stored in Flash ROM. This BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power off periods. When system is turned on, the ROBO-308 communicates with peripheral devices and check its hardware resources against the configuration information stored in the CMOS memory. If an error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start-up.

4.1 Entering Setup

Turn on or reboot the computer. When the message "Hit <DEL> if you want to run SETUP" appears, press <Del> key immediately to enter BIOS setup program.

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by "COLD START" which includes turning it OFF then ON or touch the "RESET" button. You may also restart by "WARM START" to simultaneously press <Ctrl>, <Alt>, and <Delete> keys. If you do not press the keys at the right time and the system does not boot, an error message will be displayed and you will again be asked to,

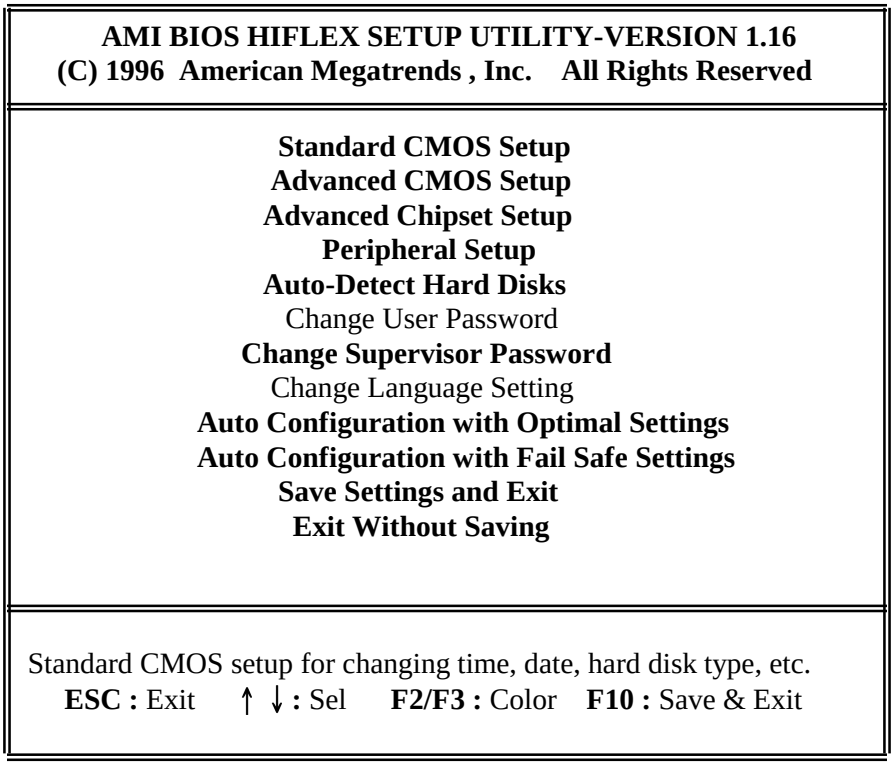
Press <F1> to Run SETUP or Resume

In HIFLEX BIOS setup, you can use the keyboard to choose among options or modify the system parameters to reflect the options installed in the system. The below table will show you all of keystroke functions in BIOS setup.

EDITING KEYS	FUNCTION
<Tab>	Move to the next field
← ↑ → ↓	Move the next field to the left, above, right, or below
<Enter>	Select in the current field
+ / –	Increments / Decrements a value
<Esc>	Close the current operation and return to previous level
<PgUp>	Returns to the previous option
<PgDn>	Advances to the next option
<F2>/<F3>	Select background color
<F10>	Show "Save current settings and exit (Y/N)" in main menu

4.2 Main Menu

Once you enter AMI BIOS CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from ten setup functions and two exit choices. Use arrow keys to select among the items and press <Enter> to accept or enter the sub-menu.



NOTE : It is strongly recommended to reload Optimal Setting for losing CMOS data or updating new BIOS.

4.3 Standard CMOS Setup Menu

This setup page includes all the items in a standard compatible BIOS. Use the arrow keys to highlight the item and then use the <PgUp>/<PgDn> or <+>/<-> keys to select the value or number you want in each item and press <Enter> key to certify it.

Follow command keys in CMOS Setup table to change **Date**, **Time**, **Drive type**, **Video display**, and **Memory assignment**.

4.4 Advanced CMOS Setup Menu

This setup includes all of the advanced features in system. The detail descriptions are specify as belows.

Boot Up Sequence

This category includes six items to determine which drive computer searches first for the disk operating system (DOS). The emulation type of ARMD is hidden and set to "Auto" to support general drive type. The reference default setting is :

* 1ST Boot Device	IDE-0
* 2ND Boot Device	Floppy
* 3RD Boot Device	ARMD-HDD
* 4TH Boot Device	Disabled
* Boot From Card BIOS	Yes
* Try Other Boot Devices	Yes
* S.M.A.R.T. for Hard Disks	Disabled

There are many of choices for the boot device. User can select "Disabled", "IDE-0", "IDE-1", "IDE-2", "IDE-3, "Floppy", "ARMD-FDD", "ARMD-HDD ", or "CDROM".

Boot Up Num-Lock

Set this option to *off* to turn the Num Lock key off when the computer is booted so you can use the arrow keys on both the numeric keypad and the keyboard. The settings are *On* or *Off*. The default setting is *On*.

Floppy Drive Swap

Set this option to *Enabled* to permit drives A: and B: to be swapped. The settings Are *Enabled* or *Disabled*. The default setting is *Disabled*.

Floppy Drive Seek

Set this option to *Enabled* to specify that floppy drive A: will perform a Seek operation at system boot. The settings are *Disabled* or *Enabled*. The optimal default setting is *Disabled*.

Floppy Access Control

This option will be effective only if Floppy is accessed through BIOS INT 40H function.

HDD Access Control

The default setting is “Normal”, the other one is “Read Only”.

PS/2 Mouse Support

Select “Enabled” (default setting) to enable PS/2 mouse function or set “Disabled” to release IRQ12 interrupt for other ISA-bus I/O devices.

Primary Display

This option specifies the type of display monitor and adapter in the computer. The Settings are *Absent*, *VGA/EGA*, *CGA40x25*, *CGA80x25*, or *Mono*. The optimal default setting is VGA/EGA. If you choose *Absent*, the “CMOS Display Type Wrong” message will be ignored for mismatch display card and CMOS setting.

System Keyboard

This option will be used to neglect “keyboard error” while you choose *Absent* setting in your BIOS setup and system has no keyboard attached.

Password Check

This option enables password checking every time the computer is powered on Or every time BIOS Setup is executed. The optimal default is *Setup*.

Setup : This option will force system to check password before running Setup if you have already entered the current user password in "Change User Password". At that time, the system will be only able to boot but deny Setup accessing.

Always : Password prompt appears every boot-up. The system will not boot and deny accessing of Setup for wrong password. The best way is to clear CMOS or try to reload BIOS Setup to wake up system.

System BIOS Cacheable

The default option is "Enabled". You can choose this option to enhance system performance by shadowing function. The "Disabled" will ignore this BIOS shadow function.

Shadow Memory (from address C000 – DFFF, 32K per segment)

Each of segments provides two options *Disabled* or *Enabled* for faster adapter's ROM execution. But this shadow function is Chipset oriented and dependent on system hardware feature. The default setting for each of all segments is assigned to "Disabled". It includes address C000, C800, D000, and D800.

4.5 Advanced Chipset Setup Menu

This setup is very important to keep system stability. If you are not technical People, don't attempt to change any parameters. The best way is to choose optimal default setting.

AT Bus Clock

The options are 14.318/2, PCLK2/3, PCLK2/4, PCLK2/5, PCLK2/6, PCLK2/8, PCLK2/10, and PCLK2/12. Select optimal AT-bus clock to meet different speed of I/O devices. The mnemonic name PCLK2 means doubled CPU clock (80MHz). To make sure the system can boot normally, the default ATCLK is "14.318/2".

Slow Refresh

There are three options 15us, 60us, and 120us used to control DRAM refresh Period. To get higher system performance, we can slow down refresh period for some DRAM products. The default setting is "120us".

Memory Hole At 15 – 16M

This option allows the end user to specify the location of a memory hole for memory space requirement from ISA-bus cards. The optimal default setting is "Disbaled". If you choose the "Enabled", the on board 15M ～16M range memory will not be recognized, and will be treated as ISA range.

RAS Precharge Time

This option controls the RAS pre-charge high time in row miss and refresh cycle. The default setting is *1.5T*. The "T" represents the cycle period of the CPU clock (80 MHz). For no brand or poor DRAM, you can choose *3.5T*.

RAS Active Time Insert Wait

Enabling this option to insert 1T wait state to support lower speed of DRAM. The settings are *Disabled* and *Enabled*. The optimal default setting is *Disabled*.

CAS Precharge Time Insert Wait

Enabling this option to insert 1T wait state to support lower speed of DRAM. Whenever memory read or write, it will insert 1T wait between the falling edge of both RAS and CAS to implement it. The settings are *Disabled* and *Enabled*. The optimal default setting is *Disabled*.

Memory Write Insert Wait

Enabling this option to insert 1T wait state to support lower speed of DRAM. The settings are *Disabled* and *Enabled*. The optimal default setting is *Disabled*.

Memory Miss Read Insert Wait

Enabling this option to insert 1T wait state to support lower speed of DRAM. When memory read miss, we can add 1T wait between the falling edge of both RAS and CAS to implement it. The settings are *Disabled* and *Enabled*. The

optimal default setting is *Disabled*.

I/O Recovery

This option controls the I/O recovery function through the general purpose I/O port control to support slower speed of ISA card. The default setting is *Enabled*, and the other one is *Disabled*.

I/O Recovery Period

For old slow ISA cards, I/O recovery time must be added to back ISA I/O commands. If an I/O writes too fast, the previous I/O write data will be overlaid by the later one, so the card will fail. You can select I/O recovery period from 0us to 3.5us (step by 0.25us). The default setting is 0.75us.

On-Chip I/O Recovery

By enabling this option to control on-chip I/O recovery. The settings are *Disabled* and *Enabled*. The default setting is *Disabled*.

16Bit ISA Insert Wait

Enable this option to insert 1 wait state for 16 bit ISA cycle. The settings are *Disabled* and *Enabled*. The optimal default setting is *Enabled*.

Watch Dog Timer (WDT)

This option controls built-in Watch-Dog Timer function. If this option is enabled, the other three sub-items can be controlled by manual selection. The settings are *Disabled* and *Enabled*. The default setting is *Disabled*.

WDT Timeout Period Select

This option provides seven parts of timeout periods 16/24/32/64/128/256/512 sec to support system monitoring on power on stage. The optimal default setting is 512 seconds.

When WDT Timeout, Then Issue →

Select this option to decide which signals *IRQ3/4/5/6/7/9/10/11/12/14/15*, *NMI*, and *Reset* will be used to report WDT event. The default setting is *Reset*.

Once WDT Timeout, Then Disable WDT

If this option is set as *No*, the system reset will be generated repeatedly after timeout and rebooting. The settings are *Yes* and *No*. The optimal default setting is *Yes*.

4.6 Peripheral Setup Menu

This section describes I/O resources assignment for all of on-board peripheral devices.

Hard disk Delay

Using this options to support older HDD for demanding of power on delay. The settings are *Disabled*, *3sec*, *5sec*, *10sec*, and *15sec*. The optimal default setting is *Disabled*.

Onboard IDE

This option specifies the channel used by the IDE controller. The settings are *Disabled*, *Primary*, or *Secondary*. The optimal default setting is *Primary*.

On Board FDC

There are two settings *Disabled* and *Enabled* for this option. If user wants to install different add-on super I/O card to connect floppy drives, set this field to *Disabled*. The optimal default setting is *Enabled*.

On Board Serial Port 1

This option enables on board serial port 1 (SIO1) and specifies the base I/O Port address for this serial communication port 1. The settings are *Disabled*, *3F8h/COM1*, *2F8h/COM2*, *3E8h/COM3*, and *2E8h/COM4*. The default setting is *3F8h/COM1*.

On Board Serial Port 2

This option enables on board serial port 2 (SIO2) and specifies the base I/O Port address for this serial communication port 2. The basic settings are *Disabled*,

2F8h/COM2, and *2E8h/COM4*. But it depends on serial por 1 setting. If we disable the SIO1, the SIO2 will have five settings *Disabled*, *3F8h/COM1*, *2F8h/COM2*, *3E8h/COM3*, and *2E8h/COM4*. In addition, If we choose the *2F8h/COM2* or 2E8h/COM4 for SIO1, only two three settings *Disabled*, *3F8h/COM1*, *3E8h/COM3* for SIO2. On the other hand, SIO2 will possess another three settings for SIO1 *3F8h/COM1*or *3E8h/COM3* assignment. The default setting is *3F8h/COM1*.

Serial Port 2 Mode

If user chooses "Disabled" setting for On Board Serial Port 2, the Serial Port 2 Mode will be not available (N/A). Otherwise, there are two settings *Normal* and *SIR* (standard infrared) for this mode. The optimal default setting is *Normal*. This "Normal" option will force IR functions to N/A state.

On Board Parallel Port

There are four suboptions **Parallel Port Mode**, **EPP Version**, **Parallel Port DMA Channel** and **Parallel Port IRQ** used to control on-board parallel port interface. For this On Board Parallel Port, the settings are *Disabled*, *378h*, *278h*, and *3BCh*. The optimal default setting is *378h*.

◎ **Parallel Port Mode :**
The Parallel Port Mode includes five options "Normal", "Bi-Dir", "EPP", "ECP", and "ECP+EPP". The optimal default setting is *Normal*.

Setting	Description
Normal	Uni-direction operation at normal speed
Bi-Dir	Bi-direction operation at normal speed
EPP	The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the Existing parallel port signals to provide asymmetric bidirectional data transfer driven by the host device.
ECP	The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve data transfer rates up to 2.5 Megabits Per second. ECP provides symmetric bidirectional Communication.
ECP + EPP	The parallel port can be used with devices that adhere to the ECPand EPP specification. This port provides symmetric and asymmetric bidirectional data transfer driven by the host device.

◎ **EPP Version :**

This option is only valid if the **Parallel Port Mode** option is set to *EPP*. This option specifies the version of the Enhanced Parallel Port specification that will be used by AMIBIOS. The settings are *1.7* or *1.9*. The optimal default setting is *1.7*.

◎ **Parallel Port DMA Channel :**

This option is only available if the setting of the **Parallel Port Mode** option is ECP. This option sets the DMA channel used by ECP-capable parallel port.

The settings are *1* and *3* (DMA channel 3). The optimal default setting is *3*.

◎ **Parallel Port IRQ :**

This option is only valid if the **Onboard Parallel Port** option is not set to *Disabled*. This option sets the IRQ used by the parallel port. The settings are *5* and 7. The optimal default setting is *7*.

4.7 BIOS POST Check Point List

AMIBIOS provides all IBM standard Power On Self Test (POST) routines as well as enhanced AMIBIOS POST routines. The POST routines support CPU internal diagnostics. The POST checkpoint codes are accessible via the Manufacturing Test Port (I/O port 80h).

Whenever a recoverable error occurs during the POST, the system BIOS will display an error message describing the message and explaining the problem in detail so that the problem can be corrected.

During the POST, the BIOS signals a checkpoint by issuing one code to I/O address 80H. This code can be used to establish how far the BIOS has executed through the power-on sequence and what test is currently being performed. This is done to help troubleshoot faulty system board.

If the BIOS detects a terminal error condition, it will halt the POST process and attempt to display the checkpoint code written to port 80H. If the system hangs before the BIOS detects the terminal error, the value at port 80H will be

the last test performed. In this case, the terminal error cannot be displayed on the screen. The following POST checkpoint codes are valid for all AMIBIOS products with a core BIOS date of 07/15/95 version 6.24 (Enhanced).

Uncompressed Iniyialization Codes — The uncompressed initialization checkpoint hex codes are listed in order of execution :

Code	Description
D0	NMI is disabled. CPU ID saved. INIT code checksum verification will be started.
D1	Initializing the DMA controller, performing the keyboard controller BAT test, starting memory refresh, and going to 4GB flat mode.
D3	To start memory sizing.
D4	Returning to real mode. Executing any OEM patches and setting the stack next.
Code	**Description**
D5	Passing control to the uncompressed code in shadow RAM at E000:0000h. The INIT code is copied to segment 0 and control will betransferred to segment 0.
D6	Control is in segment 0. Next, checking if <Ctrl><Home> was pressed and verifying the system BIOS checksum. If either <Ctrl><Home> was pressed or the system BIOS checksum is bad, next will go to checkpoint code E0h. Otherwise, going to checkpoint code D7h.
D7	To pass control to interface module.
D8	Main BIOS runtime code is to be decompressed.
D9	Passing control to the main system BIOS in shadow RAM next.

Bootblock Recovery Codes — The bootblock recovery checkpoint hex codes are listed in order of execution :

Code	Description
E0	The onboard floppy controller if available is initialized. Next, beginning the Base 512KB memory test.
E1	Initializing the interrupt vector table next.
E2	Initializing the DMA and Interrupt controllers next.
E6	Enabling the floppy drive controller and Timer IRQs. Enabling internal cache memory.
ED	Initializing the floppy drive.
EE	Start looking for a diskette in drive A: and read first sector of the diskette.
EF	A read error occurred while reading the floppy drive in drive A: .
F0	Next, searching for the AMIBOOT.ROM file in the root directory.
F1	The AMIBOOT.ROM file is not in the root directory.
F2	Next, reading and analyzing the floppy diskette FAT to find the clusters occupied by the AMIBOOT.ROM file.
F3	Start reading AMIBOOT.ROM file, cluster by cluster.
F4	The AMIBOOT.ROM file is not the correct size.
F5	Next, disabling internal cache memory.
FB	Next, detecting the type of Flash ROM.

FC	Erasing the Flash ROM.
FD	Programming the Flash ROM
FF	Flash ROM programming was successful. Next, restarting the system BIOS.

Uncompressed Initialization Codes — The following runtime checkpoint hex codes are listed in order of execution. These codes are uncompressed in F0000h shadow RAM.

Code	Description
03	The NMI is disabled. Next, checking for a soft reset or a power on condition.
05	The BIOS stack has been built. Next, disabling cache memory.
Code	**Description**
06	Uncompressing the POST code next.
07	Next, initializing the CPU and the CPU data area.
08	The CMOS checksum calculation is done next.
0B	Next, performing any required initialization before the keyboard BAT Command is issued.
0C	The keyboard controller input buffer is free. Next, issuing the BAT Command to the keyboard controller.
0E	The keyboard controller BAT command result has been verified. Next, performing any necessary INIT after the K/B controller BATcommand test.
0F	The keyboard command byte is written next.
10	Next, issuing the pin 23 and 24 blocking and unblocking commands.
11	Next, checking if the <End> or <Ins> keys were pressed during power on.
12	To initialize CMOS if the *initialize CMOS RAM in every boot* is set or the <End> key is pressed. Going to disable DMA and Interrupt controllers.
13	The video display has been disabled. Port B has been initialized. Next, initializing the chipset.
14	The 8254 timer test will begin next.
19	The 8254 timer test is over. Starting the memory refresh test next.
1A	The memory refresh line is toggling. Checking the 15us on/off time next.
23	Reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors.
24	The configuration or setup required before interrupt vector initialization has completed. Interrupt vector init. is about to begin
25	Interrupt vector initialization is done. Clearing the password if the POST DIAG switch is on.
27	Any initialization before setting video mode to be done.
28	Going for monochrome mode and color mode setting.
2A	Bus initialization system, static, output devices will be done next, if present.
2B	Passing control to the video ROM to perform any required configuration before the video ROM test.
2C	To look for optional video ROM and give control.
2D	The video ROM has returned control to BIOS POST. Performing any

	Required processing after the video ROM had control.
2E	Completed podt-video ROM test processing. If the EGA/VGA controller is not found, performing the display memory read/write test next.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. Look for retrace checking next.
31	Display memory R/W test or retrace checking failed. To do alternate display retrace checking.
32	Alternate display memory R/W test passed. To look for the alternate display retrace checking.
34	Video display checking is over. Setting the display mode next.
37	The display mode is set. Displaying the power on message next.
38	Initializing the bus input, IPL, and general devices next, if present.
39	Displaying bus initialization error message.
3A	The new cursor position has been read and saved. Displaying the *Hit <DEL>* message next.
Code	**Description**
40	Preparing the descriptor tables next.
42	Entering protected mode for the memory test next.
43	Entered protected mode. Enabling interrupts for diagnostics mode next.
44	Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next.
45	Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next.
46	The memory wraparound test has completed. The memory size calculation has been done. Writing patterns to test memory next.
47	The memory pattern has been written to extended memory. Writing patterns to the base 640 KB memory test.
48	Patterns written in base memory. Determining the amount of memory below 1MB next.
49	The amount of memory below 1MB has been found and verified. Determining the amount of memory above 1MB memory next.
4B	The amount of memory above 1MB has been found and verified. Checking for a soft reset and clearing the memory below 1MB for the soft reset next. If this is a power on situation, going to checkpoint 4Eh next.
4C	The memory below 1MB has been cleared via a soft reset. Clearing the memory above 1MB next.
4D	The memory above 1MB has been cleared via soft reset. Saving the memory size next. Going to checkpoint 52h next.
4E	The memory test started, but not as the result of a soft reset. Displaying the first 64KB memory size next.
4F	Memory size display started. This will be updated during memory test. Performing the sequential and random memory test next.
50	Memory testing/initialization below 1MB completed. Going to adjust displayed memory size for relocation and shadowing.
51	The memory size display was adjusted for relocation and shadowing. Testing the memory above 1MB next.
52	The memory above 1MB has been tested and initialized. Saving the memory size information next.

53	The memory size information and the CPU registers are saved. Entering real mode next.
54	Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next.
57	The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next.
58	The memory size was adjusted for relocation and shadowing. Clearing the *Hit <DEL>* message next.
59	The *Hit <DEL>* message is cleared. The *<WAIT…>* message is displayed. Staring the DMA and interrupt controller test next.
60	The DMA page register test passed. To do DMA#1 base register test.
62	DMA#1 base register test passed. To do DMA#2 base register test.
65	DMA#2 base register test passed. To program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next.
Code	**Description**
81	A keyboard reset error or stuck key was found. Issuing the keyboard Controller interface test command next.
82	The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
83	Command byte written, Global data init done. To check for lock-key.
84	Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next.
85	The memory size check is done. Displaying a soft error and checking for a Password or bypassing Setup next.
86	Password checked. About to do programming before setup.
87	The programming before Setup has completed. Uncompressing the Setup code and executing the AMIBIOS Setup utility next.
88	Returned from CMOS setup program and screen is cleared. About to do Programming after setup.
89	The programming after Setup has completed. Displaying the power on screen message next.
8B	The first screen message has been displayed. The <WAIT…> message is displayed. Performaing the PS/2 mouse check and extended BIOS data area allocation check next.
8C	Programming the Setup options next.
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	The floppy drive controller has been configured. Configuring the hard disk drive controller next.
95	Initializing the bus option ROMs from C800 next.
96	Initializing before passing control to the adaptor ROM at C800.
97	Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next.
98	The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.

99	Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after setting the RS-232 base address. Performing any required Initialization before the Coprocessor test next.
9C	Required initialization before the Coprocessor test is over. Initializing the Coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after Coprocessor test.
9E	Initialization after the Coprocessor test is complete. Checking the extended Keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next.
A2	Displaying any soft errors next.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Memory wait state programming is over. Clearing the screen and enabling parity and the NMI next.
A7	NMI and parity enabled. Performing any initialization required before Passing control to the adaptor ROM at E000 next.
Code	**Description**
A8	Initialization before passing control to the adaptor ROM at E000h completed. Passing control to the adaptor ROM at E000h next.
A9	Returned from adaptor ROM at E000h control. Performing any initialization required after the E000 option ROM had control next.
AA	Initialization after E000 option ROM control has completed. Displaying the system configuration next.
AB	Building the multiprocessor table, if necessary.
AC	Uncompressing the DMI data and initializing DMI POST next.
B0	The system configuration is displayed.
B1	Copying any code to specific areas.
00	Code copying to specific areas is done. Passing control to INT 19 h boot loader next.

4.10 Flash BIOS Utility

Utilize AMI Flash BIOS programming utility to update on-board BIOS for the future new BIOS version. Please contact your technical window to get this utility if necessary.

NOTE : Remark or delete any installed Memory Management Utility (such as EMM386.EXE, QEMM.EXE, …, etc.) in the CONFIG.SYS files before running Flash programming utility. Please keep tightly contact with your technical window to get newest version of BIOS utility.