MVME1603/MVME1604 Single Board Computer Installation and Use

V1600-1A/IH4

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Preface

The *MVME1603/MVME1604 Single Board Computer Installation and Use* manual provides general product information along with hardware preparation, installation, and operating instructions. A functional description and various types of interfacing information for the MVME1603/MVME1604 family of Single Board Computers is also included.

This manual is intended for anyone who wants to design OEM systems, supply additional capability to an existing compatible system, or work in a lab environment for experimental purposes.

A basic knowledge of computers and digital logic is assumed. To use this manual, you should be familiar with the publications listed in Appendix A of this manual.

The MVME1603/1604 family of Single Board Computers has two parallel branches based on two distinct versions of the base board. Both versions are populated with a number of similar plug-together components, which are listed in the following table..

Base Board	Processor Module		DRAM	Transition Module
MVME1600-001	PM603-00*x*	PM604-00*x* PM604-01*x*	RAM104-00*x*	MVME760
	PM603-01*x*			
	PM603-02*x*			
	PM603-03*x*			
MVME1600-011	PM603-00*x*	PM604-00*x* PM604-01*x*	RAM104-00*x*	MVME712M
	PM603-01*x*			
	PM603-02*x*			
	PM603-03*x*			

Throughout this manual, a convention is used which precedes data and address parameters by a character identifying the numeric format as follows:

$	dollar	specifies a hexadecimal character
%	percent	specifies a binary number
&	ampersand	specifies a decimal number

Unless otherwise specified, all address references are in hexadecimal.
An asterisk (*) following the signal name for signals which are level-significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge-significant denotes that the actions initiated by that signal occur on high-to-low transition.

In this manual, *assertion* and *negation* are used to specify forcing a signal to a particular state. In particular, *assertion* and *assert* refer to a signal that is active or true; *negation* and *negate* indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent.

Data and address sizes are defined as follows:

A byte is eight bits, numbered 0 through 7, with bit 0 being the least significant.

A half word is 16 bits, numbered 0 through 15, with bit 0 being the least significant.

A word is 32 bits, numbered 0 through 31, with bit 0 being the least significant.

A double word is 64 bits, numbered 0 through 63, with bit 0 being the least significant.

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Safety Summary
Safety Depends On You

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola, Inc. assumes no liability for the customer's failure to comply with these requirements.

The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor AC power cable. The power cable must be plugged into an approved three-contact electrical outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

Do Not Operate in an Explosive Atmosphere.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

Keep Away From Live Circuits.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone.

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Use Caution When Exposing or Handling the CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

Do Not Substitute Parts or Modify Equipment.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

All Motorola PWBs (printed wiring boards) are manufactured by UL-recognized manufacturers, with a flammability rating of 94V-0.

WARNING

This equipment generates, uses, and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used in a cabinet with adequate EMI protection.

CE

European Notice: Board products with the **CE** marking comply with the EMC Directive (89/336/EEC). Marking a system with the **CE** symbol indicates compliance of that Motorola system to the applicable directives of the European Community. A system with the **CE** marking meets or exceeds the following technical standards:

EN55022 (CISPR 22): Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment. Tested to Equipment Class B.

EN50082-1, 1992: Electromagnetic Compatibility -- Generic Immunity Standard, Part 1: Residential, Commercial and Light Industry.

IEC801-2: Electromagnetic Compatibility for Industrial Process Measurement and Control Equipment, Part 2: Electrostatic Discharge Requirements.

IEC801-3: Electromagnetic Compatibility for Industrial Process Measurement and Control Equipment, Part 3: Radiated Electromagnetic Field Requirements.

IEC801-4: Electromagnetic Compatibility for Industrial Process Measurement and Control Equipment, Part 4: Electrical Fast Transient/Burst Requirements.

The product also fulfills EN60950 (product safety) which is essentially the requirement for the Low Voltage Directive (73/23/EEC).

In accordance with European Community directives, a “Declaration of Conformity” has been made and is on file at Motorola, Inc. - Computer Group, 27 Market Street, Maidenhead, United Kingdom, SL6 8AE.

This board product was tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a **CE**-marked system will maintain the required EMC/safety performance.

Contents

CHAPTER 1 Hardware Preparation and Installation

Introduction 1-1
Equipment Required 1-2
Overview of Startup Procedure 1-5
Unpacking Instructions 1-6
Hardware Configuration 1-6
MVME1600-001 Base Board Preparation 1-7
- SCSI Bus Terminator Selection (J7) 1-7
- General-Purpose Software-Readable Header (J8) 1-8
- Console Port Configuration 1-9
- VMEbus System Controller Selection (J9) 1-10
- Serial Port 3 Clock Configuration (J10) 1-11
- Serial Port 4 Clock Configuration (J13) 1-13
- Remote Status and Control 1-13

MVME760 Transition Module Preparation 1-14
- Configuration of Serial Ports 3 and 4 1-15

MVME1600-011 Base Board Preparation 1-18
- Serial Port 4 DCE/DTE Selection (J7) 1-18
- Serial Port 4 Clock Selection (J8/15/16) 1-20
- Serial Port 4 I/O Path Selection (J9) 1-21
- VMEbus System Controller Selection (J10) 1-22
- Serial Port 3 I/O Path Selection (J13) 1-23
- General-Purpose Software-Readable Header (J14) 1-23
- Remote Status and Control 1-25

MVME712M Transition Module Preparation 1-27
- Serial Ports 1-4 DCE/DTE Configuration 1-29
- Serial Port 4 Clock Configuration 1-29

Hardware Installation 1-32
- ESD Precautions 1-32

PM603/604 Processor/Memory Mezzanine 1-33
RAM104 Memory Mezzanine Installation 1-35
MVME1603/1604 VMEmodule Installation 1-38
MVME760 Transition Module Installation 1-39
MVME712M Transition Module Installation 1-42
System Considerations 1-45
- MVME1600-001 Base Board 1-46
- MVME1600-011 Base Board 1-47

CHAPTER 2 Operating Instructions

Introduction 2-1
Applying Power 2-1
ABORT Switch (S1) 2-1
RESET Switch (S2) 2-2
Front Panel Indicators (DS1 - DS6) 2-3
Memory Maps 2-4
MPU Bus Memory Map 2-4
Normal Address Range 2-4
PCI Local Bus Memory Map 2-9
VMEbus Memory Map 2-10
Programming Considerations 2-17
PCI Arbitration 2-18
Interrupt Handling 2-20
Machine Check Interrupt (MCP*) 2-21
Maskable Interrupts 2-21
VMEchip2 Interrupts 2-23
Z8536 and Z85230 Interrupts 2-23
DMA Channels 2-24
Sources of Reset 2-24
Endian Issues 2-25
Processor/Memory Domain 2-25
PCI Domain 2-28
VMEbus Domain 2-28

CHAPTER 3 Functional Description

Introduction 3-1
Features 3-1
General Description 3-3
Block Diagram 3-4
SCSI Interface 3-6
SCSI Termination 3-6
Ethernet Interface 3-7
Graphics Interface 3-8
PCI Mezzanine Interface 3-9
VMEbus Interface 3-10
ISA Super I/O Device (ISASIO) 3-10
Asynchronous Serial Ports 3-10
Parallel Port 3-11
Disk Drive Controller 3-12

Keyboard and Mouse Interface....3-12
ISA Bridge Controller....3-12
Real-Time Clock and NVRAM....3-13
Programmable Timers....3-14
Interval Timers....3-14
16-Bit Timers....3-15
VMEchip2 Timers....3-15
Serial Communications Interface....3-15
Z8536 CIO Device....3-16
Board Configuration Register....3-16
P2 Signal Multiplexing....3-17
ABORT Switch (S1)....3-19
RESET Switch (S2)....3-20
Front Panel Indicators (DS1 - DS6)....3-21
Polyswitches (Resettable Fuses)....3-22
MVME1600-001 Base Board....3-22
MVME1600-011 Base Board....3-23
Speaker Control....3-24
PM603/604 Processor/Memory Mezzanine Module....3-24
RAM104 Memory Module....3-26
MVME760 Transition Module....3-27
Serial Interface Modules....3-27
MVME712M Transition Module....3-28

CHAPTER 4 Connector Pin Assignments

Common Connectors....4-2
LED Mezzanine Connector....4-3
MPU Mezzanine Connector....4-3
CPU Connector....4-6
DRAM Expansion Connectors....4-10
PCI Mezzanine Card Connectors....4-11
VMEbus Connector P1....4-11
Ethernet 10BaseT Connector....4-14
Disk Drive Connector....4-15
MVME1600-001 Connectors....4-16
VMEbus Connector P2....4-16
SCSI Connector....4-16
Graphics Connector....4-18
Keyboard and Mouse Connectors....4-19
Ethernet AUI Connector....4-20

Parallel I/O Connector 4-21
Serial Ports 1 and 2 4-22
Serial Ports 3 and 4 4-23
MVME1600-011 Connectors 4-24
VMEbus Connector P2 4-24
SCSI Connector 4-24
Ethernet AUI Connector 4-27
Parallel I/O Connector 4-28
Serial Ports 1-4 4-29

CHAPTER 5 PPCBug

Overview 5-1
Memory Requirements 5-2
PPCBug Implementation 5-2
Using the Debugger 5-3
Debugger Commands 5-4
Diagnostic Tests 5-7

CHAPTER 6 CNFG and ENV Commands

Overview 6-1
CNFG - Configure Board Information Block 6-2
ENV - Set Environment 6-3
Configuring the PPCBug Parameters 6-3
Configuring the VMEbus Interface 6-12
Slave Address Decoders 6-13

APPENDIX A Related Documentation

Motorola Computer Group Documents A-1
Manufacturers' Documents A-3
Related Specifications A-8

APPENDIX B Specifications

Specifications B-1
Cooling Requirements B-2
EMC Compliance B-3

APPENDIX C Serial Interconnections

Introduction C-1
Asynchronous Serial Ports C-1
Synchronous Serial Ports C-2
EIA-232-D Connections C-3
Interface Characteristics C-4
EIA-530 Connections C-5
Interface Characteristics C-8
Proper Grounding C-9

APPENDIX D Troubleshooting CPU Boards: Solving Startup Problems

Introduction D-1

GLOSSARY

Abbreviations, Acronyms, and Terms to Know GL-1

FIGURES

Figure 1-1. MVME1600-001 Base Board Block Diagram 1-3
Figure 1-2. MVME1600-011 Base Board Block Diagram 1-4
Figure 1-3. MVME1600-001 Switches, Headers, Connectors, Fuses, LEDs 1-12
Figure 1-4. MVME760 Connector and Header Locations 1-17
Figure 1-5. MVME1600-011 Switches, Headers, Connectors, Fuses, LEDs 1-19
Figure 1-6. MVME712M Connector and Header Locations 1-28
Figure 1-7. J15 Clock Line Configuration 1-29
Figure 1-8. MVME1600-011 Serial Port 4 Clock Configuration 1-30
Figure 1-9. P2 Adapter Component Placement 1-31
Figure 1-10. PM603/PM604 Placement on MVME1603/1604 1-34
Figure 1-11. RAM104 Placement on PM603/PM604 1-36
Figure 1-12. MVME760/MVME1600-001 Cable Connections 1-41
Figure 1-13. MVME712M/MVME1600-011 Cable Connections 1-44
Figure 2-1. IBC Arbiter Configuration Diagram 2-19
Figure 2-2. MVME1603/MVME1604 Interrupt Architecture 2-20
Figure 2-3. IBC Interrupt Handler Block Diagram 2-22
Figure 2-4. Big-Endian Mode 2-26
Figure 2-5. Little-Endian Mode 2-27
Figure 3-1. MVME1603/MVME1604 Block Diagram 3-5

TABLES

Table 1-1. Startup Overview 1-5
Table 1-2. Remote Reset Connector J1 Interconnect Signals 1-14
Table 1-3. Remote Reset Connector J4 Interconnect Signals 1-26
Table 2-1. Processor View of the Memory Map 2-5
Table 2-2. PCI Configuration Space Memory Map 2-6
Table 2-3. ISA/PCI I/O Space Memory Map 2-7
Table 2-4. PCI View of the Memory Map 2-9
Table 2-5. VME2PCI View of the Memory Map 2-11
Table 2-6. VMEchip2 Memory Map (Sheet 1 of 3) 2-12
Table 2-6. VMEchip2 Memory Map (Sheet 2 of 3) 2-14
Table 2-6. VMEchip2 Memory Map (Sheet 3 of 3) 2-17
Table 2-7. PCI Arbitration Assignments 2-19
Table 2-8. IBC DMA Channel Assignments 2-24
Table 3-1. MVME1603/MVME1604 Features 3-1
Table 3-2. P2 Multiplexing Sequence 3-18
Table 3-3. Fuse Assignments by Base Board 3-22
Table 3-4. Minimum ROMFAL and ROMNAL Values 3-26
Table 3-5. Module Type Identification 3-27
Table 4-1. LED Mezzanine Connector 4-3
Table 4-2. MPU Mezzanine Connector 4-4
Table 4-3. CPU Connector 4-7
Table 4-4. DRAM Mezzanine—Connector 1 4-10
Table 4-5. DRAM Mezzanine—Connector 2 4-11
Table 4-6. PCI Mezzanine Card Connector 4-12
Table 4-7. VMEbus Connector P1 4-13
Table 4-8. Ethernet 10BaseT Connector 4-14
Table 4-9. Disk Drive Mezzanine Connector 4-15
Table 4-10. SCSI Connector 4-17
Table 4-11. Graphics Connector 4-18
Table 4-12. Keyboard Connector 4-19
Table 4-13. Mouse Connector 4-19
Table 4-14. Ethernet AUI Connector (MVME760) 4-20
Table 4-15. Parallel I/O Connector (MVME760) 4-21
Table 4-16. Serial Connections—Ports 1 and 2 (MVME760) 4-22
Table 4-17. Serial Connections—Ports 3 and 4 (MVME760) 4-23
Table 4-18. VMEbus Connector P2 4-25
Table 4-19. SCSI Connector (MVME712M) 4-26

Table 4-20. Ethernet AUI Connector (MVME712M) 4-27
Table 4-21. Parallel I/O Connector (MVME712M)..... 4-28
Table 4-22. Serial Connections—MVME712M Ports 1-4..... 4-29
Table 4-23. Serial Connections—MVME1600-011 Ports 3 and 4 4-30
Table 5-1. Debugger Commands 5-4
Table 5-2. Diagnostic Test Groups..... 5-7
Table A-1. Motorola Computer Group Documents A-2
Table A-2. Manufacturers' Documents A-3
Table A-3. Related Specifications A-8
Table B-1. MVME1600-001/MVME1600-011 Specifications B-1
Table C-1. MVME1600-001/MVME1600-011 Serial Ports C-1
Table C-2. EIA-232-D Interconnect Signals C-3
Table C-3. EIA-232-D Interface Transmitter Characteristics C-5
Table C-4. EIA-232-D Interface Receiver Characteristics C-5
Table C-5. MVME760 EIA-530 Interconnect Signals C-6
Table C-6. EIA-530 Interface Transmitter Characteristics C-8
Table C-7. EIA-530 Interface Receiver Characteristics C-9
Table D-1. Basic Troubleshooting Steps for ALL CPU Boards D-1
Table D-2. Troubleshooting MVME1603/MVME1604 Boards D-3

Hardware Preparation and Installation

1

Introduction

This manual provides general product information along with hardware preparation, installation and operating instructions for the MVME1603/1604 family of Single Board Computers.

The MVME1603/1604 is a double-high VMEmodule equipped with a PowerPC™ Series microprocessor. The MVME1603 is equipped with a PowerPC 603 microprocessor; the MVME1604 has a PowerPC 604 microprocessor. 256KB of level 2 (L2) cache memory is available as an option on both versions.

The MVME1603/1604 family has two parallel branches based on two distinct versions (MVME1600-001 and MVME1600-011) of the base board. The differences between the MVME1600-001 and the MVME1600-011 lie mainly in the area of I/O handling; the logic design is the same for both versions.

In either case, the complete MVME1603/1604 consists of the base board plus:

- A processor/memory module (PM603 or PM604) with optional L2 cache
- An LED mezzanine (MEZLED) to supply status indicators and Reset/Abort switches
- A DRAM module (RAM104) for additional memory
- An optional PCI mezzanine card (PMC) for additional versatility

The block diagrams in Figures 1-1 and 1-2 illustrate the architecture of the MVME1600-001 and the MVME1600-011 base boards.

Equipment Required

The following equipment is required to complete an MVME1603/ 1604 system:

- VME system enclosure
- System console terminal
- Transition module (MVME760 for the MVME1600-001 base boards, MVME712M for the MVME1600-011) and connecting cables
- Disk drives (and/or other I/O) and controllers
- Operating system (and/or application software)

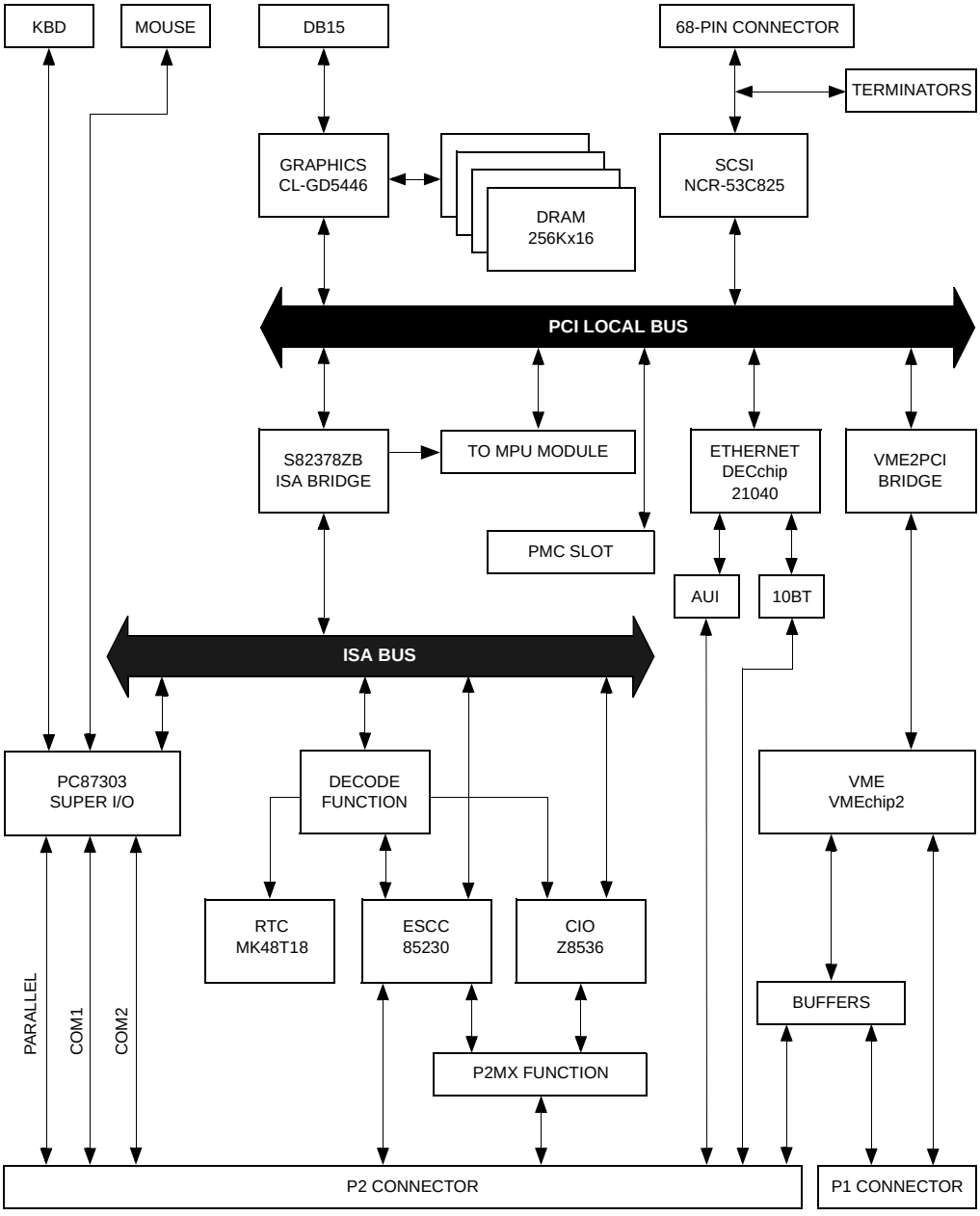


Figure 1-1. MVME1600-001 Base Board Block Diagram

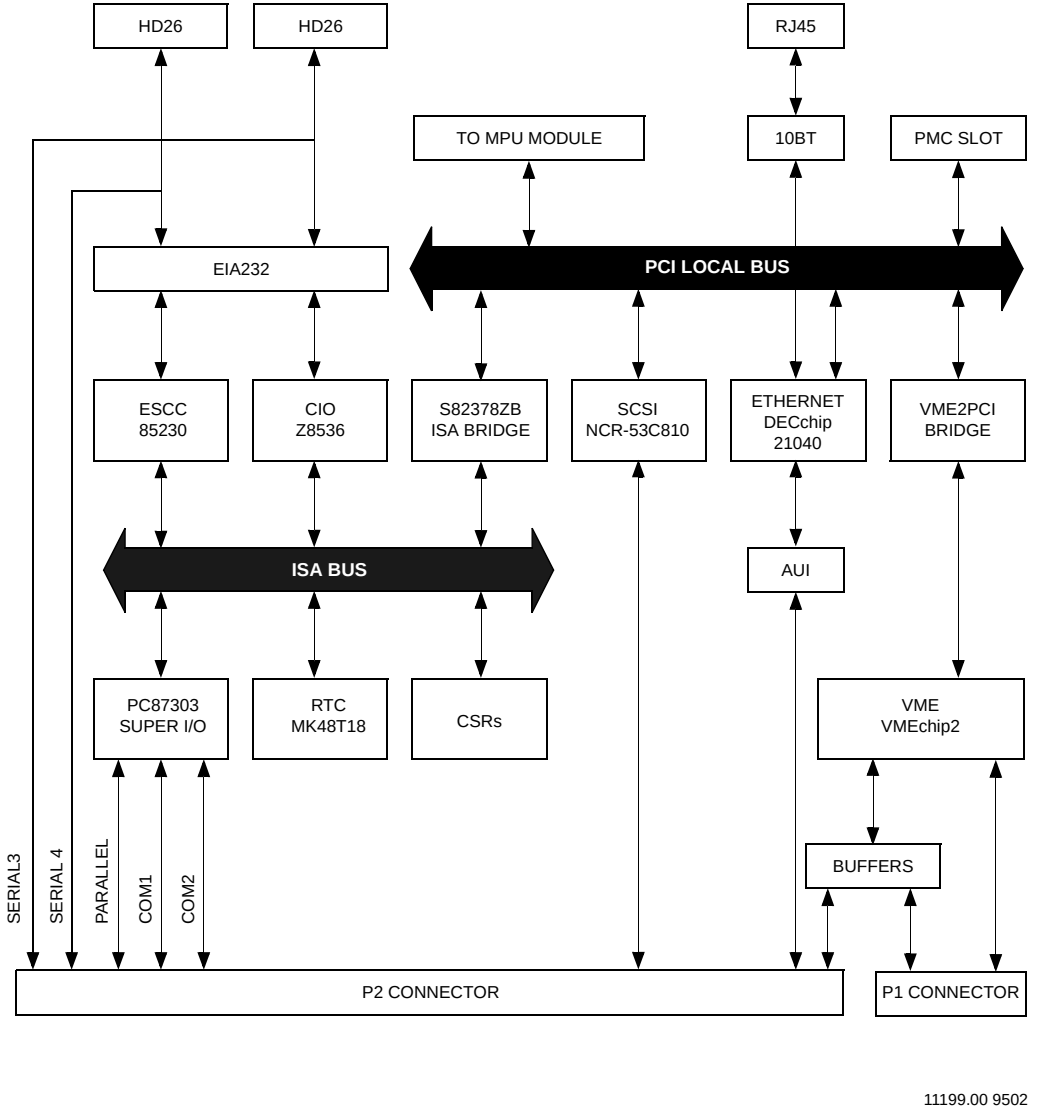


Figure 1-2. MVME1600-011 Base Board Block Diagram

Overview of Startup Procedure

The following table lists the things you will need to do before you can use this board and tells you where to find the information that you need to perform each step. Please read this entire chapter, including all **Caution** and **Warning** notes, before you begin.

Table 1-1. Startup Overview

What you need to do...	Refer to...	On page...
Unpack the hardware.	*Unpacking Instructions*	1-6
Configure the hardware by setting jumpers on the boards and transition modules.	*MVME1600-001 Base Board Preparation* and *MVME760 Transition Module Preparation*	1-7 and 1-15
	MVME1600-011 Base Board Preparation and *MVME712M Transition Module Preparation*	1-18 and 1-27
Ensure processor and memory mezzanines are properly installed on the base board.	*PM60x Processor/Memory Mezzanine Installation* and *RAM104 Memory Mezzanine Installation*	1-33 and 1-35
Install the MVME1603/1604 VMEmodule in the chassis.	*MVME1603/1604 VMEmodule Installation*	1-37
Install the transition module in the chassis.	*MVME760 Transition Module Installation* or *MVME712M Transition Module Installation*	1-39 or 1-42
Connect a console terminal.	*Console Port Configuration*	1-9
Connect any other equipment you will be using.	*Connector Pin Assignments*	4-1
	For more information on optional devices and equipment, refer to the documentation provided with the equipment.	
Power up the system.	*Switches and LEDs*	2-1
	Troubleshooting the MVME1603/1604; Solving Start-Up Problems	D-1
Note that the debugger prompt appears.	*Using the Debugger*	5-3
	You may also wish to obtain the *PPCBug Firmware Package User's Manual* listed in Appendix A.	A-1
Initialize the clock.	*Debugger Commands*, Set Time and Date (**SET**)	5-6
Examine and/or change environmental parameters.	*CNFG and ENV Commands*	6-1
Program the board as needed for your applications.	MVME1603/1604 Programmer's Reference Guide listed in Appendix A.	A-1

Unpacking Instructions

Note If the shipping carton is damaged upon receipt, request that the carrier's agent be present during the unpacking and inspection of the equipment.

Unpack the equipment from the shipping carton. Refer to the packing list and verify that all items are present. Save the packing material for storing and reshipping of equipment.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage circuits.

Hardware Configuration

To produce the desired configuration and ensure proper operation of the MVME1603/1604, you may need to carry out certain modifications before installing the module.

The MVME1603/1604 provides software control over most options: by setting bits in control registers after installing the MVME1603/ 1604 in a system, you can modify its configuration. (The MVME1603/1604 control registers are described in Chapter 3, and/or in the *MVME1603/MVME1604 Single Board Computer Programmer's Reference Guide* as listed under *Related Documentation* in Appendix A.)

Some options, however, are not software-programmable. Such options are controlled through manual installation or removal of header jumpers or interface modules on the base board or the associated modules.

MVME1600-001 Base Board Preparation

Figure 1-3 illustrates the placement of the switches, jumper headers, connectors, and LED indicators on the MVME1600-001. Manually configurable items on the base board include:

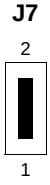
- SCSI bus terminator selection (J7)
- General-purpose software-readable header (J8)
- VMEbus system controller selection (J9)
- Serial Port 3 clock configuration (J10)
- Serial Port 4 clock configuration (J13)

Serial ports on the associated MVME760 transition module are also manually configurable. For a discussion of the configurable items on the transition module, refer to the user's manual for the MVME760 (part number VME760UA) as necessary.

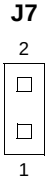
The MVME1600-001 has been factory tested and is shipped with the configurations described in the following sections. The MVME1600-001's required and factory-installed Debug Monitor, PPCBug, operates with those factory settings.

SCSI Bus Terminator Selection (J7)

The MVME1600-001 provides terminators for the SCSI bus. The SCSI terminators are enabled or disabled by a jumper on header J7. The SCSI terminators may be configured as follows.



On-Board SCSI Bus Termination Enabled
(factory configuration)



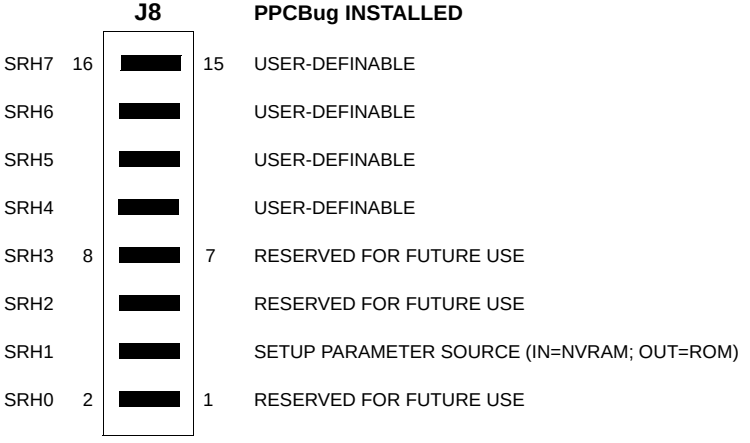
On-Board SCSI Bus Termination Disabled

General-Purpose Software-Readable Header (J8)

Header J8 provides eight readable jumpers. These jumpers can be read as a register at ISA I/O address $80000801. Bit 0 is associated with header pins 1 and 2; bit 7 is associated with pins 15 and 16. The bit values are read as a zero when the jumper is installed, and as a one when the jumper is removed. The PowerPC firmware (PPCBug) reserves the four lower-order bits, SRH3 to SRH0. They are defined as shown in the list below:

Low-Order Bit	Pins	Definition
Bit #0 (SRH0)	1—2	Reserved for future use.
Bit #1 (SRH1)	3—4	With the jumper installed between pins 3 and 4 (factory configuration), the debugger uses the current user setup/operation parameters in NVRAM. When the jumper is removed (making the bit a **1**), the debugger uses the default setup/operation parameters in ROM instead. Refer to the **ENV** command description in Chapter 6 for the ROM defaults.
Bit #2 (SRH2)	5—6	Reserved for future use.
Bit #3 (SRH3)	7—8	Reserved for future use.

The four higher-order bits, SRH4 to SRH7, are user-definable. They can be allocated as necessary to specific applications. The MVME1600-001 is shipped from the factory with J8 set to all zeros (jumpers on all pins).



Console Port Configuration

On the MVME1600-001 base board, either the standard serial console port (COM1) or the on-board video (VGA) port can serve as the PPCBug firmware console port.

The firmware checks for the presence of a connected keyboard and a connected mouse. If either device is connected to the PowerPC system and a firmware-supported video card/video device is found, the firmware is automatically brought up on the connected video terminal. If neither a mouse nor keyboard is connected, the firmware is brought up on the serial port (COM1). It is also brought up on the serial port (COM1) if no video terminal is found.

The following table shows how the display device is determined:

Mouse Connected	Keyboard Connected	On-Board VGA Device Present	Firmware Displayed on
Yes	Yes	Yes	VGA terminal
Yes	No	Yes	VGA terminal
No	Yes	Yes	VGA terminal
No	No	Yes	Serial port (COM1)
No	No	No	Serial port (COM1)
No	Yes	No	Serial port (COM1)

Notes If the mouse is connected but the keyboard is not, and the supported VGA device exists, the firmware is displayed on the video terminal. Because a keyboard is necessary for interactive use on a video terminal, however, the firmware will display a “Keyboard not connected” message. In order to use the firmware, you must then plug the keyboard in.

Conversely, if you remove the VGA monitor, also remove the keyboard and mouse to avoid unexpected behavior by the firmware.

If you plan to use a terminal other than a VGA device as the firmware console, set it up as follows:

- Eight bits per character
- One stop bit per character
- Parity disabled (no parity)
- Baud rate of 9600 baud

9600 baud is the power-up default for serial ports on MVME1603/ 1604 boards. After power-up you can reconfigure the baud rate if you wish, via the PPCBug firmware's Port Format (**PF**) command. Whatever the baud rate, the terminal must perform some type of hardware handshaking — either XON/OFF or via the CTS line.

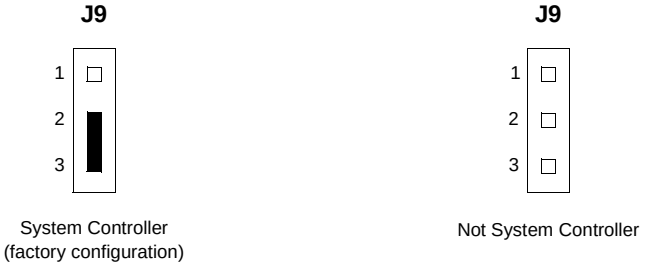
VMEbus System Controller Selection (J9)

The MVME1600-001 is factory-configured in system controller mode (i.e., a jumper is installed across pins 2 and 3 of header J9). This means that the MVME1600-001 assumes the role of system controller at system power-up or reset.

Leave the jumper installed across pins 2 and 3 if you intend to operate the MVME1600-001 as system controller in all cases.

Remove the jumper from J9 if the MVME1600-001 is not to operate as system controller under any circumstances.

Note that when the MVME1600-001 is functioning as system controller, the SYS LED is turned on.



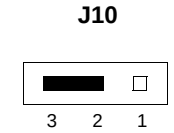
System Controller
(factory configuration)

Not System Controller

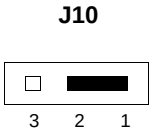
Serial Port 3 Clock Configuration (J10)

You can configure Serial port 3 on the MVME1600-001 to use the clock signals provided by the TXC signal line. Header J10 configures port 3 to either drive or receive TXC. The factory configuration has port 3 set to receive TXC.

To complete the configuration of the TXC clock line, you must also set serial port 3 clock configuration header J9 on the MVME760 transition module, described later in this chapter. For details on the configuration of that header, refer to the *MVME760 Transition Module* section or to the user's manual for the MVME760 (part number VME760UA).



Receive TXC
(factory configuration)



Drive TXC

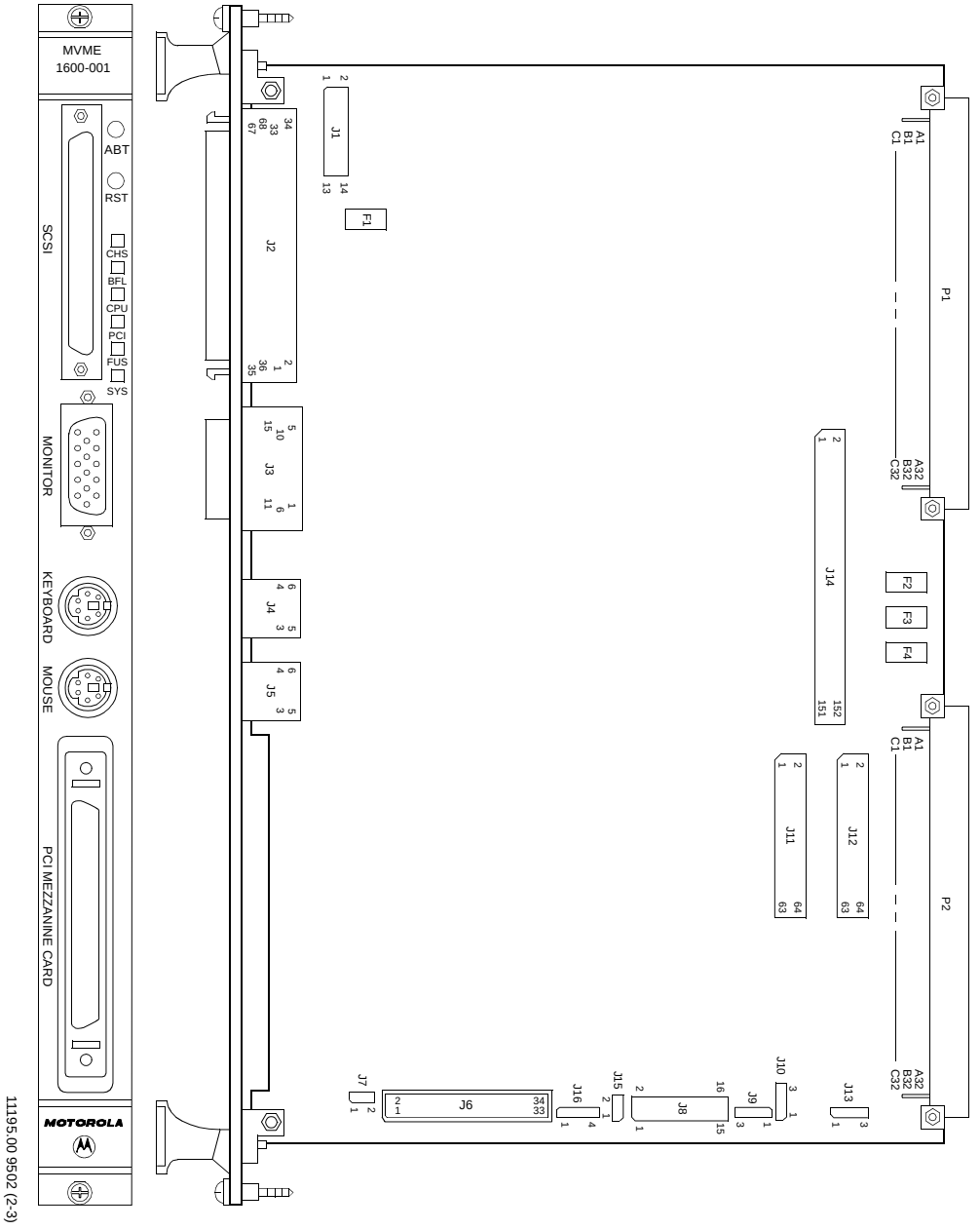
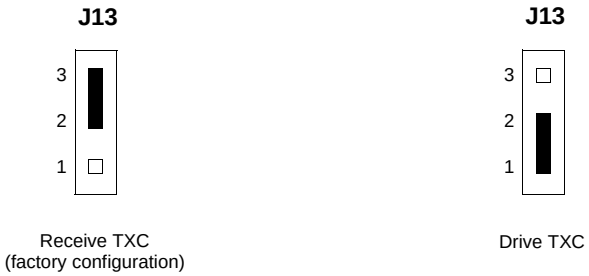


Figure 1-3. MVME1600-001 Switches, Headers, Connectors, Fuses, LEDs

Serial Port 4 Clock Configuration (J13)

You can configure Serial port 4 on the MVME1600-001 to use the clock signals provided by the TXC signal line. Header J13 configures port 4 to either drive or receive TXC. The factory configuration has port 4 set to receive TXC.

To complete the configuration of the TXC clock line, you must also set serial port 4 clock configuration header J8 on the MVME760 transition module (described later in this chapter). For details on the configuration of that header, refer to the *MVME760 Transition Module* section or to the user's manual for the MVME760 (part number VME760UA).



Receive TXC
(factory configuration)

Drive TXC

Remote Status and Control

The MVME1600-001 front panel LEDs and switches are mounted on a removable mezzanine board. Removing the LED mezzanine makes the mezzanine connector (J1, a keyed double-row 14-pin connector) available for service as a remote status and control connector. This allows a system designer to construct a RESET/LED panel that can be located apart from the MVME1600-001. Maximum cable length is 15 feet.

In this application, J1 can be connected to a user-supplied external cable to carry the signals for remote reset, abort, the LEDs, and a general-purpose I/O signal. The I/O signal is a general-purpose interrupt pin which can also function as a trigger input. The interrupt pin is level programmable.

Table 1-2 lists the pin numbers, signal mnemonics, and signal descriptions for J1.

Table 1-2. Remote Reset Connector J1 Interconnect Signals

Pin Number	Signal Mnemonic	Signal Name and Description
1		Not used.
2	RESETSW*	**RESET Switch**. Signal goes low when the RESET switch is pressed. It may be forced low externally for a remote reset.
3	IRQ	**Interrupt Request**. General-purpose interrupt input line.
4	ABORTSW*	**ABORT Switch**. Signal goes low when the ABORT switch is pressed. It may be forced low externally for a remote abort.
5	PCILED*	**PCI LED**. Signal goes low when the PCI LED illuminates.
6	FAILLED*	**FAIL LED**. Signal goes low when the FAIL LED illuminates.
7	LANLED*	**LAN LED**. Signal goes low when the LAN LED illuminates.
8	STATLED*	**STATUS LED**. Signal goes low when the STATUS LED illuminates.
9	FUSELED*	**RPWR LED**. Signal goes low when the FUSE LED illuminates.
10	RUNLED*	**RUN LED**. Signal goes low when the RUN LED illuminates.
11	SCSILED*	**SCSI LED**. Signal goes low when the SCSI LED illuminates.
12	SCONLED*	**SCON LED**. Signal goes low when the SCON LED illuminates.
13	+5VRMT	**+5 Vdc Power**. Fused through fuse F1; +5 Vdc power to a user-supplied external connection.
14	SPKR	**Speaker**. Speaker output line.

MVME760 Transition Module Preparation

The MVME760 transition module (Figure 1-4) is used in conjunction with the MVME1600-001 base board. The features of the MVME760 include:

- A parallel printer port

- An Ethernet interface supporting both AUI and 10BaseT connections
- Two EIA-232-D asynchronous serial ports (identified as COM1 and COM2 on the front panel)
- Two synchronous serial ports (ports 3 and 4)

Configuration of Serial Ports 3 and 4

The synchronous serial ports, Serial Port 3 and Serial Port 4, are configurable via a combination of serial interface modules (SIMs) and jumper settings. The following table lists the synchronous serial ports with their corresponding SIM connectors and jumper headers.

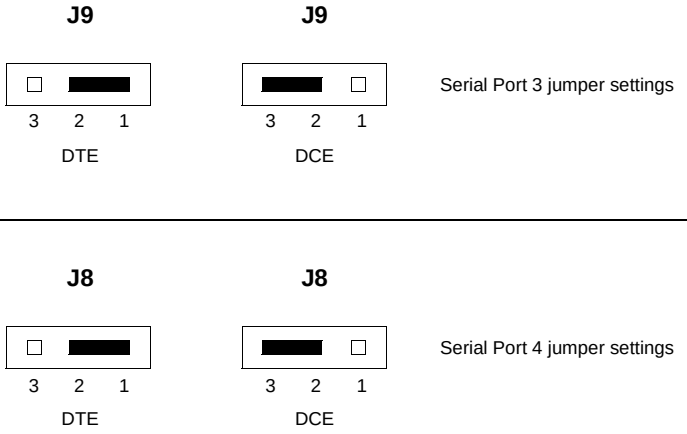
Synchronous Port	Board Connector	Panel Connector	SIM Connector	Jumper Header
Port 3	J7	SERIAL 3	J6	J9
Port 4	J2	None	J4	J8

Port 3 is routed both to board connector J7 and to the HD26 front panel connector marked SERIAL 3. Port 4 is available only at board connector J2. Four serial interface modules are available:

- EIA-232-D (DCE and DTE)
- EIA-530 (DCE and DTE)

You can change Serial Ports 3 and 4 from an EIA-232-D to an EIA-530 interface (or vice-versa) by mounting the appropriate SIM705 series interface module and setting the corresponding jumper. SIMs can be ordered separately as required.

Headers J9 and J8 are used to configure Serial Port 3 and Serial Port 4, respectively. With the jumper in position 1-2, the port is configured as a DTE. With the jumper in position 2-3, the port is configured as a DCE. *The jumper setting of the port should match the configuration of the corresponding SIM module*.



When installing the SIM modules, note that the headers are keyed for proper orientation.

For further information on the preparation of the transition module, refer to the user's manual for the MVME760 (part number VME760A/UM) as necessary.

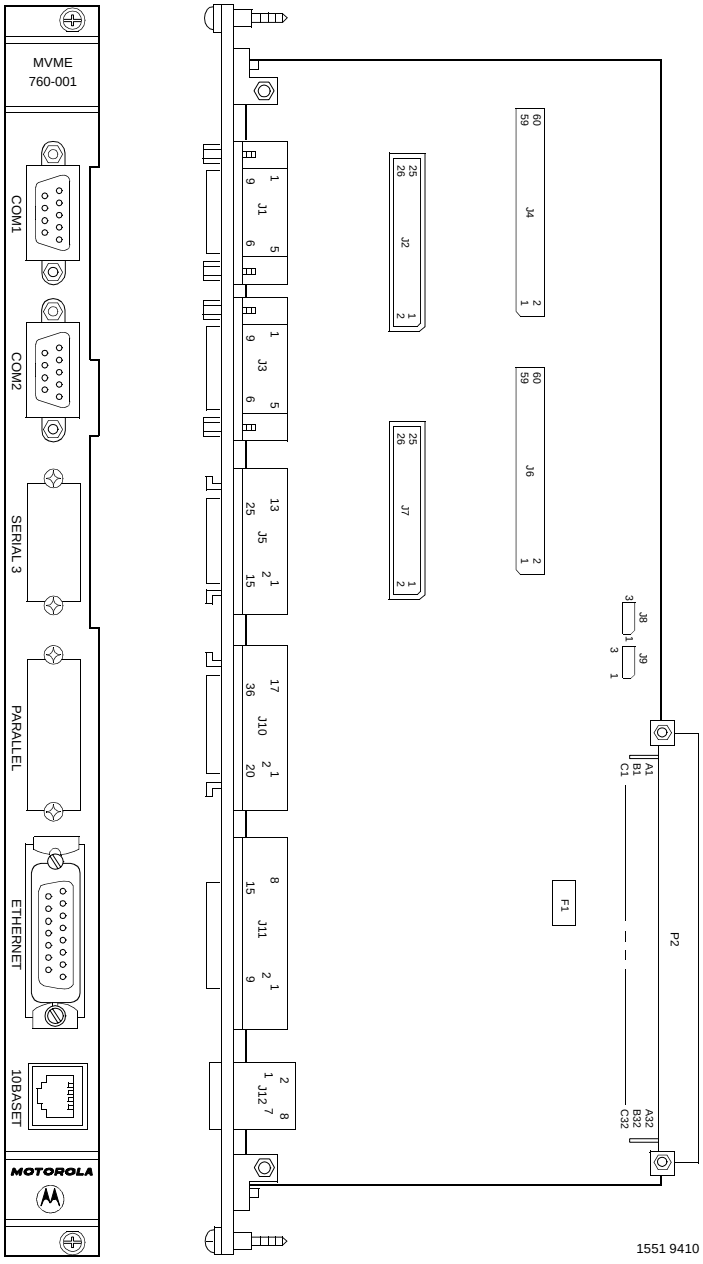


Figure 1-4. MVME760 Connector and Header Locations

MVME1600-011 Base Board Preparation

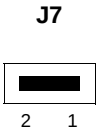
Figure 1-5 illustrates the placement of the switches, jumper headers, connectors, and LED indicators on the MVME1600-011. Manually configurable items on the base board include:

- Serial Port 4 DCE/DTE selection (J7)
- Serial Port 4 clock selection (J8, J15, J16)
- Serial Port 4 I/O path selection (J9)
- VMEbus system controller selection (J10)
- Serial Port 3 I/O path selection (J13)
- General-purpose software-readable header (J14)

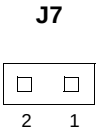
Serial ports on the associated MVME712M transition module are also manually configurable. For a discussion of the configurable items on the transition module, refer to the user's manual for the MVME712M (part number MVME712M) as necessary. The MVME1600-011 has been factory tested and is shipped with the configurations described in the following sections. The required and factory-installed Debug Monitor, PPCBug, operates with those factory settings.

Serial Port 4 DCE/DTE Selection (J7)

Serial port 4 on the MVME1600-011 is DCE/DTE configurable. Header J7 sets a configuration bit for serial port 4 in the Z8536 ID register. Software reads the bit as either a DCE or DTE value and configures the port accordingly. Header J7 may be configured as follows.



Jumper On = DTE in ID Register
(factory configuration)



Jumper Off = DCE in ID Register

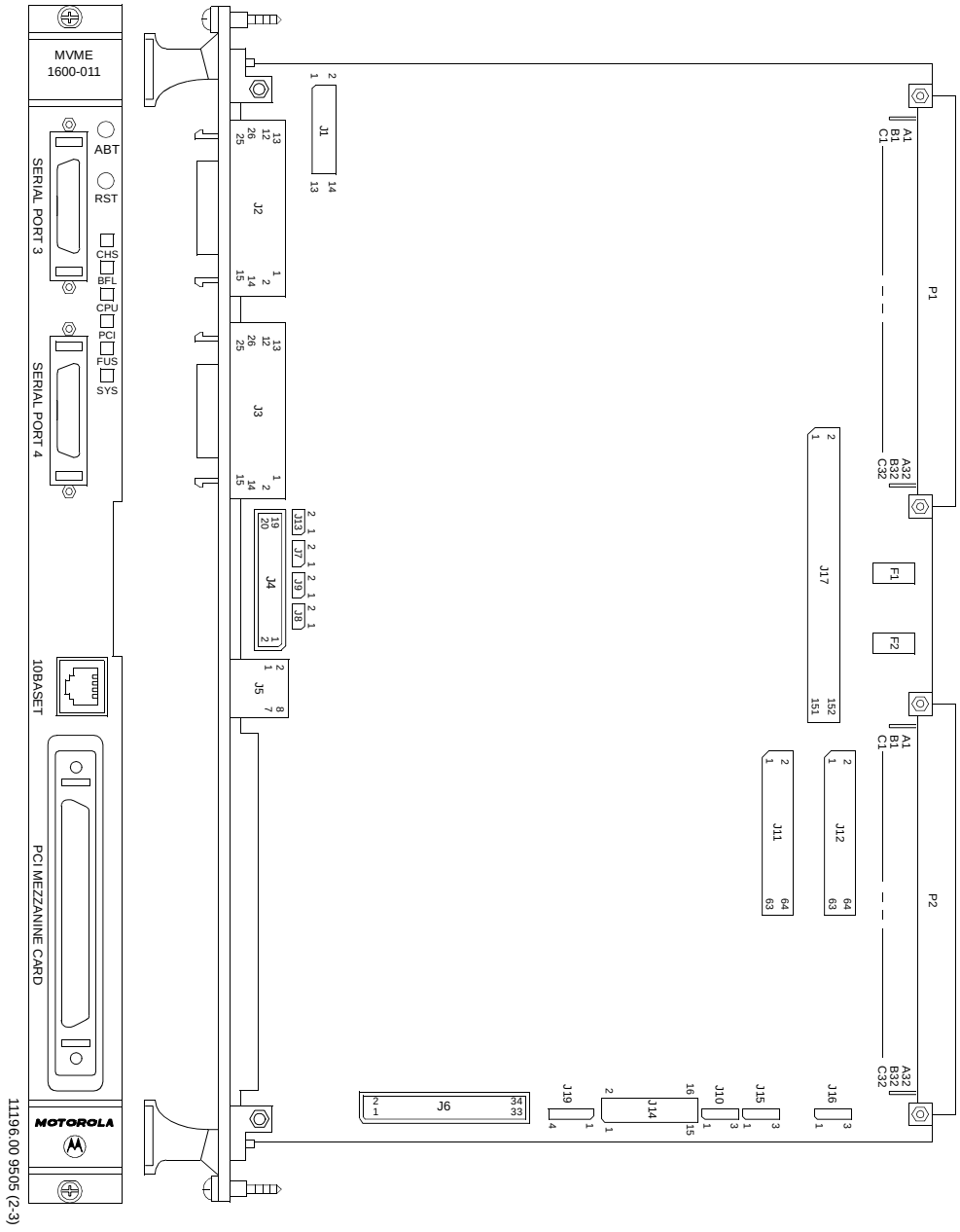
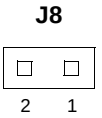
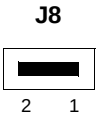


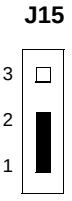
Figure 1-5. MVME1600-011 Switches, Headers, Connectors, Fuses, LEDs

Serial Port 4 Clock Selection (J8/15/16)

The MVME1600-011 is shipped from the factory with Serial Port 4 configured for asynchronous communications (i.e., the internal clock is used). Port 4 can be configured for synchronous communications as well. It can either drive (using the internal clock) or receive (using an external clock) the Receive and Transmit clock signals. To select synchronous communications for the Serial Port 4 connection, install jumpers on headers J8, J15, and J16 in one of the configurations shown below.







Drive TRXC4 Signal

Receive TRXC4 Signal
(Factory configuration)

Drive RTXC4 Signal

Receive RTXC4 Signal
(Factory configuration)

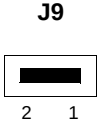
To complete the configuration of the clock lines, you must also set serial port 4 clock configuration header J15 on the MVME712M transition module (described later in this chapter). For details on the configuration of that header, refer to the *MVME712M Transition Module* section or to the user's manual for the MVME712M (part number MVME712M).

Serial Port 4 I/O Path Selection (J9)

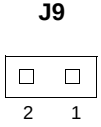
On the MVME1600-011, serial port 4's I/O signals are routed to backplane connector P2 and to front panel connector J3. Header J9 determines the state of the DSR, RI, and TM signals on serial port 4.

With a jumper installed on J9, DSR, RI, and TM come from the front panel.

With the jumper removed, P2 I/O is selected. The DSR, RI, and TM signals are not supported in this case, so DSR is held true while RI and TM are held false.



Jumper On = Front Panel I/O
DSR, RI, and TM from front panel
to 8536 device



Jumper Off = P2 I/O (factory configuration)
DSR to 8536 device held true
RI and TM to 8536 device held false

VMEbus System Controller Selection (J10)

The MVME1600-011 is factory-configured in system controller mode (i.e., a jumper is installed across pins 2 and 3 of header J10). This means that the MVME1600-011 assumes the role of system controller at system power-up or reset.

Leave the jumper installed across pins 2 and 3 if you intend to operate the MVME1600-011 as system controller in all cases.

Remove the jumper from J10 if the MVME1600-011 is not to operate as system controller under any circumstances.

Note that when the MVME1600-011 is functioning as system controller, the SYS LED is turned on.

System Controller
(factory configuration)

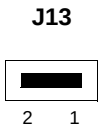
Not System Controller

Serial Port 3 I/O Path Selection (J13)

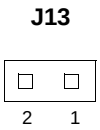
On the MVME1600-011, serial port 3's I/O signals are routed to backplane connector P2 and to front panel connector J2. Header J13 determines the state of the DSR, RI, and TM signals on serial port 3.

With a jumper installed on J13, DSR, RI, and TM come from the front panel.

With the jumper removed, P2 I/O is selected. The DSR, RI, and TM signals are not supported in this case, so DSR is held true while RI and TM are held false.



Jumper On = Front Panel I/O
DSR, RI, and TM from front panel
to 8536 device



Jumper Off = P2 I/O (factory configuration)
DSR to 8536 device held true
RI and TM to 8536 device held false

General-Purpose Software-Readable Header (J14)

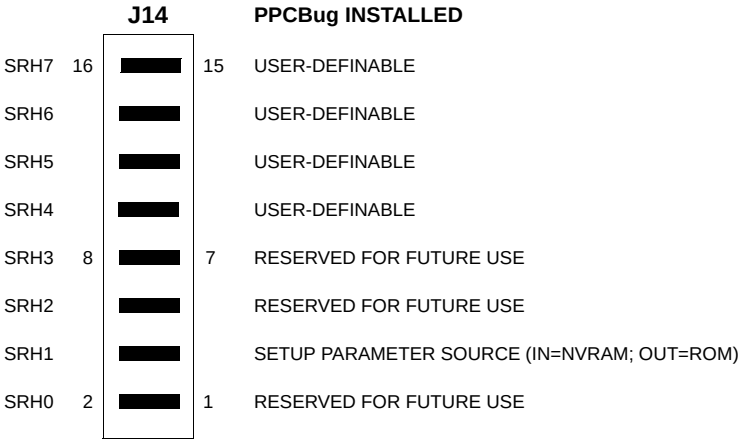
Header J14 provides eight readable jumpers. These jumpers can be read as a register at ISA I/O address $80000801. Bit 0 is associated with header pins 1 and 2; bit 7 is associated with pins 15 and 16. The bit values are read as a zero when the jumper is installed, and as a one when the jumper is removed.

The PowerPC firmware (PPCBug) reserves the four lower-order bits, SRH3 to SRH0. They are defined as shown in the following list:

Low-Order Bit	Pins	Definition
Bit #0 (SRH0)	1—2	Reserved for future use.
Bit #1 (SRH1)	3—4	With the jumper installed between pins 3 and 4 (factory configuration), the debugger uses the current user setup/operation parameters in NVRAM. When the jumper is removed (making the bit a **1**), the debugger uses the default setup/operation parameters in ROM instead. Refer to the **ENV** command description in Chapter 6 for the ROM defaults.
Bit #2 (SRH2)	5—6	Reserved for future use.
Bit #3 (SRH3)	7—8	Reserved for future use.

The four higher-order bits, SRH4 to SRH7, are user-definable. They can be allocated as necessary to specific applications.

The MVME1600-011 is shipped from the factory with J14 set to all zeros (jumpers on all pins).



Remote Status and Control

The remote status and control connector, J4, is a keyed double-row 20-pin connector located behind the front panel of the MVME1600-011. It connects to a user-supplied external cable and carries the signals for remote reset, abort, the LEDs, and three general-purpose I/O signals. This allows a system designer to construct a RESET/LED panel that can be located remotely from the MVME1600-011. This feature is similar to the remote connector provided on the MVME167 and MVME187 Single Board Computers; maximum cable length is 15 feet.

The general-purpose I/O signals include two TTL-level I/O pins and one general-purpose interrupt pin which can also function as a trigger input. The interrupt pin is level programmable.

Table 1-3 lists the pin numbers, signal mnemonics, and signal descriptions for J4.

Table 1-3. Remote Reset Connector J4 Interconnect Signals

Pin Number	Signal Mnemonic	Signal Name and Description
1	+5VRMT	**+5 Vdc Power**. Fused through fuse F1; +5 Vdc power to a user-supplied external connection.
2	LANLED*	**LAN LED**. Signal goes low when the LAN LED illuminates.
3	FUSELED*	**RPWR LED**. Signal goes low when the FUSE LED illuminates.
4	SCSILED*	**SCSI LED**. Signal goes low when the SCSI LED illuminates.
5	PCILED*	**PCI LED**. Signal goes low when the PCI LED illuminates.
6		10KΩ pullup line.
7	RUNLED*	**RUN LED**. Signal goes low when the RUN LED illuminates.
8	STATLED*	**STATUS LED**. Signal goes low when the STATUS LED illuminates.
9	FAILLED*	**FAIL LED**. Signal goes low when the FAIL LED illuminates.
10		10KΩ pullup line.
11	SCONLED*	**SCON LED**. Signal goes low when the SCON LED illuminates.
12	ABORTSW*	**ABORT Switch**. Signal goes low when the ABORT switch is pressed. It may be forced low externally for a remote abort.
13	RESETSW*	**RESET Switch**. Signal goes low when the RESET switch is pressed. It may be forced low externally for a remote reset.
14, 15	GND	**Ground**.
16		10KΩ pullup line.
17		Not used.
18	IRQ	**Interrupt Request**. General-purpose interrupt input line.
19	SPKR	**Speaker**. Speaker output line.
20	GND	**Ground**.

MVME712M Transition Module Preparation

The MVME712M transition module (Figure 1-6) and P2 adapter board are used in conjunction with the MVME1600-011 base board. The features of the MVME712M include:

- A parallel printer port (through the P2 adapter)
- An Ethernet interface supporting AUI connections (through the P2 adapter)
- Four EIA-232-D multiprotocol serial ports (through the P2 adapter)
- An SCSI interface (through the P2 adapter) for connection to both internal and external devices
- Socket-mounted SCSI terminating resistors for end-of-cable or middle-of-cable configurations
- Provision for modem connection
- Green LED for SCSI terminator power; yellow LED for Ethernet transceiver power

The features of the P2 adapter board include:

- A 50-pin connector for SCSI cabling to the MVME712M and/or to other SCSI devices
- Socket-mounted SCSI terminating resistors for end-of-cable or middle-of-cable configurations
- Fused SCSI teminator power developed from the +5Vdc present at connector P2
- A 64-pin DIN connector to interface the EIA-232-D, parallel, SCSI, and Ethernet signals to the MVME712M

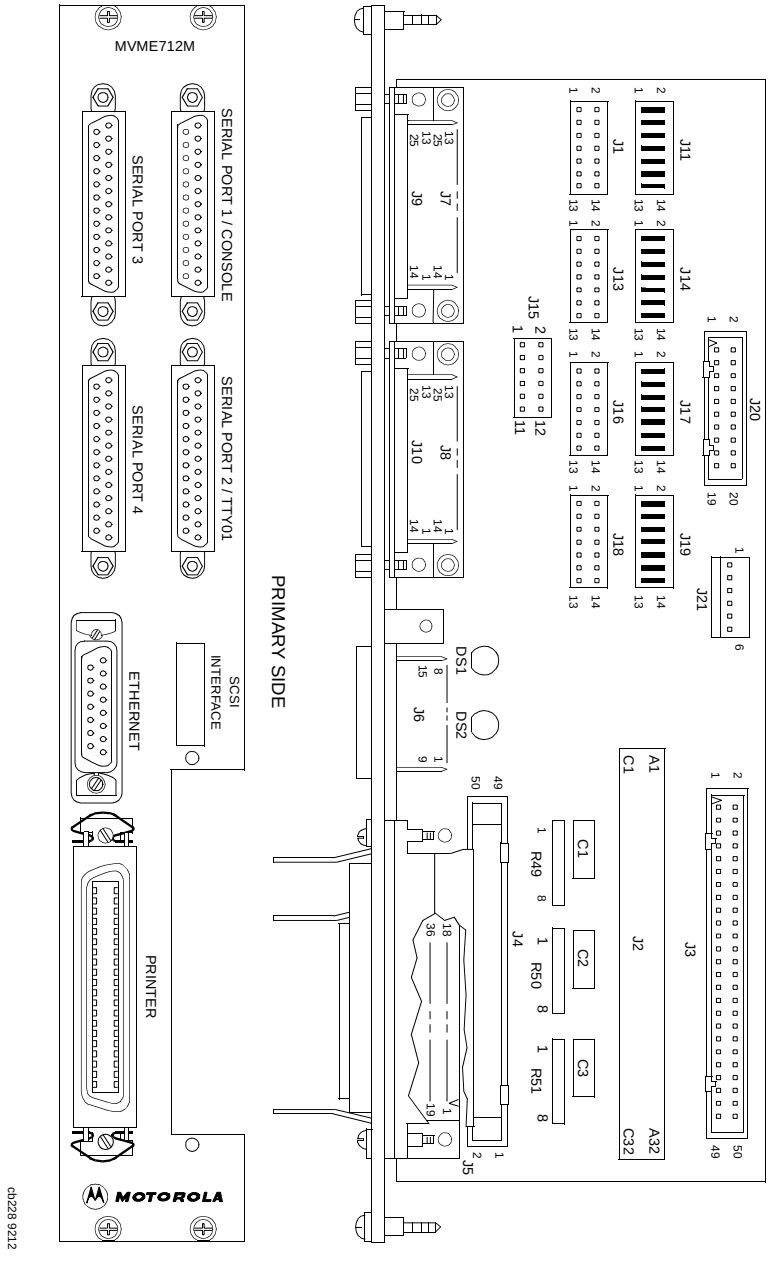


Figure 1-6. MVME712M Connector and Header Locations

Serial Ports 1-4 DCE/DTE Configuration

Serial ports 1 through 4 are configurable as modems (DCE) for connection to terminals, or as terminals (DTE) for connection to modems. The MVME712M is shipped with the serial ports configured for DTE operation.

Serial port DCE/DTE configuration is accomplished by positioning jumpers on one of two headers per port.The following table lists the serial ports with their corresponding jumper headers.

Serial Port	Board Connector	Panel Connector	Jumper Header
Port 1	J7	SERIAL PORT 1/ CONSOLE	J1/J11
Port 2	J8	SERIAL PORT 2/ TTY	J16/J17
Port 3	J9	SERIAL PORT 3	J13/J14
Port 4	J10	SERIAL PORT 4	J18/J19

Serial Port 4 Clock Configuration

Port 4 can be configured via J15 (Figure 1-7) to use the TrxC4 and RtxC4 signal lines. Part of the configuration must be done with headers J8, J15, and J16 on the MVME1600-011 (Figure 1-8).

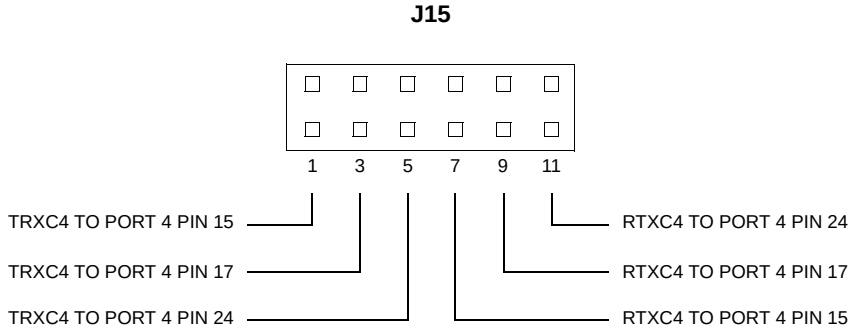


Figure 1-7. J15 Clock Line Configuration

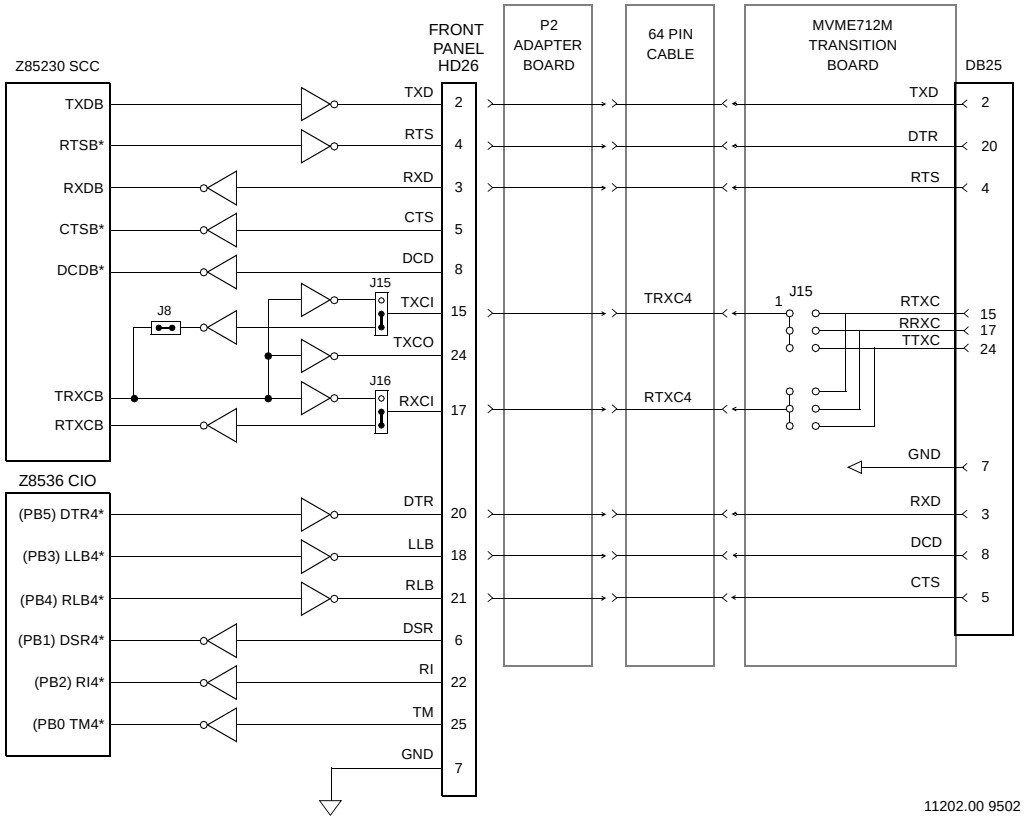


Figure 1-8. MVME1600-011 Serial Port 4 Clock Configuration

Preparation of the P2 adapter for the MVME712M consists of removing or installing the SCSI terminating resistors. Figure 1-9 illustrates the location of the resistors, fuse, and connectors.

For further information on the preparation of the transition module and the P2 adapter, refer to the user's manual for the MVME712M (part number MVME712M) as necessary.

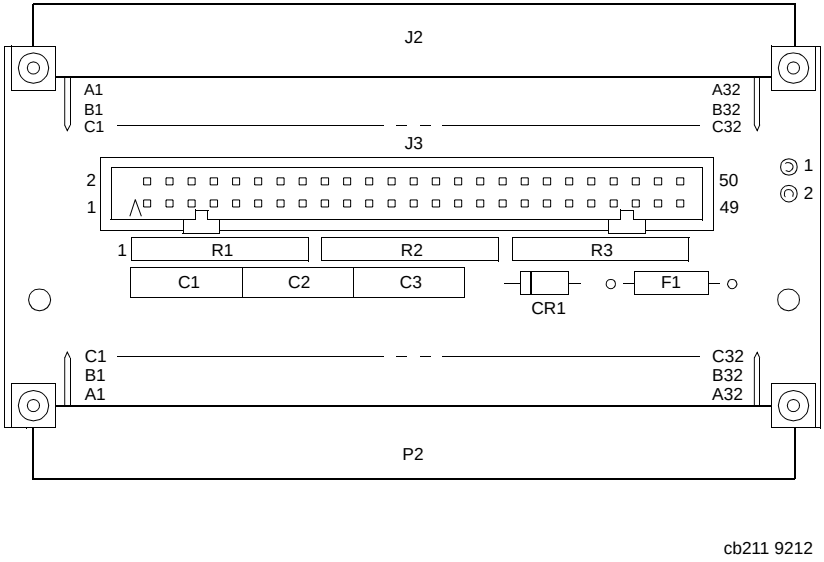


Figure 1-9. P2 Adapter Component Placement

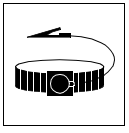
Hardware Installation

The following sections discuss the placement of the various mezzanine cards on the the MVME1600-001 and the MVME1600-011 base boards, the installation of the complete MVME1603/1604 VMEmodule assembly and corresponding transition module into a VME chassis, and the system considerations relevant to the installation. Before installing the MVME1603/1604, ensure that the serial ports and all header jumpers are configured as desired.

In most cases, the mezzanine cards—the processor/memory module, the LED mezzanine, the DRAM module, and (if applicable) the optional PCI mezzanine—are already in place on the MVME1603/1604. The user-configurable jumpers are accessible with the mezzanines installed.

Should it be necessary to install mezzanines on the base board, refer to the following sections for a brief description of the installation procedure. If necessary, you can find additional information in the user's manuals for the individual mezzanine cards.

ESD Precautions



Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components, such as disk drives, computer boards, and memory modules, can be extremely sensitive to ESD. After removing the component from the system or its protective wrapper, place the component flat on a grounded, static-free surface (and in the case of a board, component side up). Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available at electronics stores) that is attached to an unpainted metal part of the system chassis.

PM603/604 Processor/Memory Mezzanine

To install a PM603 or PM604 processor/memory mezzanine on an MVME1603/1604 main module, refer to Figure 1-10 and proceed as follows:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the VMEmodules.

Caution

Inserting or removing modules with power applied may result in damage to module components.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

3. Carefully remove the MVME1603/1604 from its VMEbus card slot and lay it flat, with connectors P1 and P2 (the rear panel) facing you.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits

Caution

The 192MB module is a factory-installed option. It is recommended that you do not attempt to remove it, as the components could easily be damaged.

4. Place the PM603 or PM604 mezzanine module on top of the MVME1603/1604, with the cutout corner at the upper right. Connector J5 at the bottom edge of the PM603 or PM604 should connect smoothly with its corresponding connector on the MVME1603/1604.

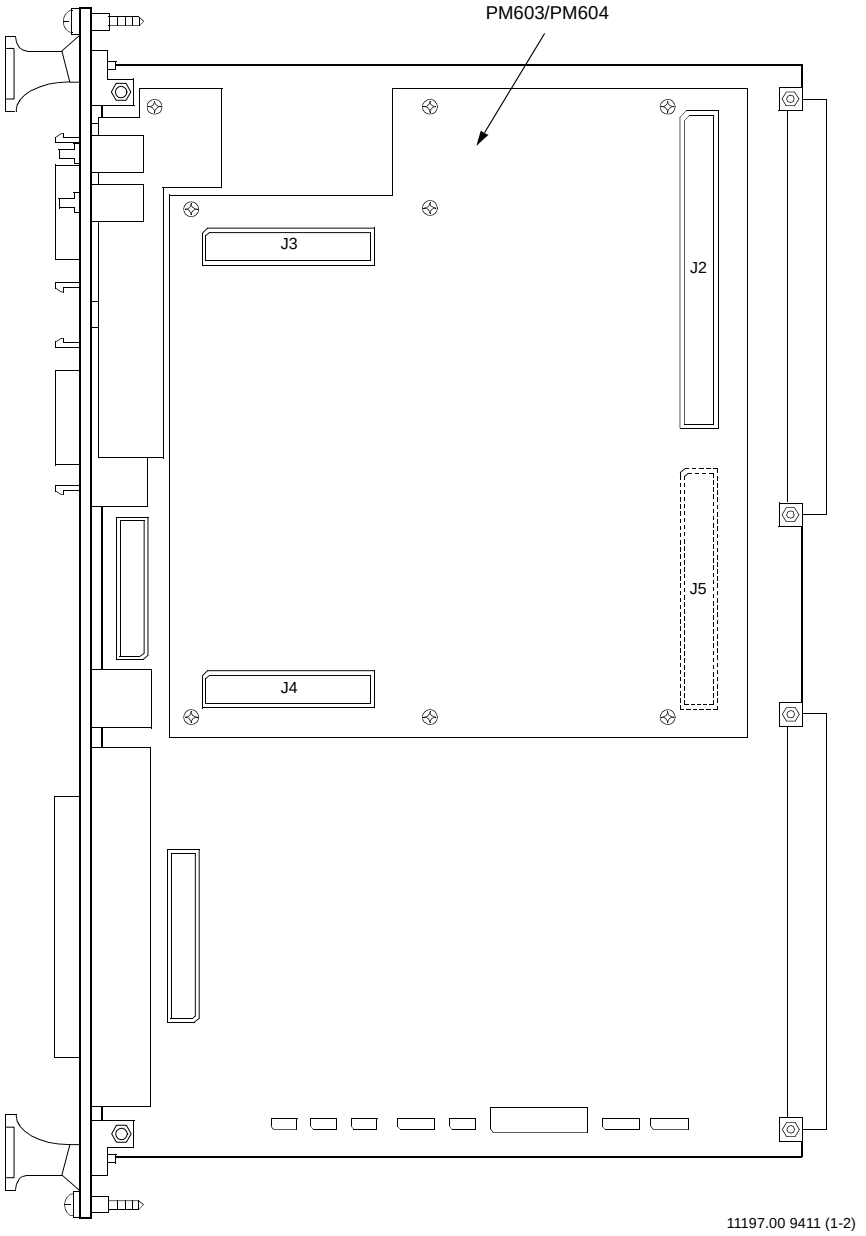


Figure 1-10. PM603/PM604 Placement on MVME1603/1604

5. Align the standoffs on the MVME1603/1604 board with the holes at the edges of the PM603 or PM604 mezzanine, insert the Phillips screws through the holes in the mezzanine and the spacers, and tighten the screws.
6. Reinstall the MVME1603/1604 assembly in its proper card slot. Be sure the module is seated properly in the backplane connectors. Do not damage or bend connector pins.
7. Replace the chassis or system cover(s), reconnect the system to the AC or DC power source, and turn the equipment power on.

RAM104 Memory Mezzanine Installation

The RAM104 DRAM mezzanine mounts on top of the PM603 or PM604 processor/memory mezzanine. To install a RAM104 mezzanine, refer to Figure 1-11 and proceed as follows:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the VMEmodules.


Caution

Inserting or removing modules with power applied may result in damage to module components.


Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

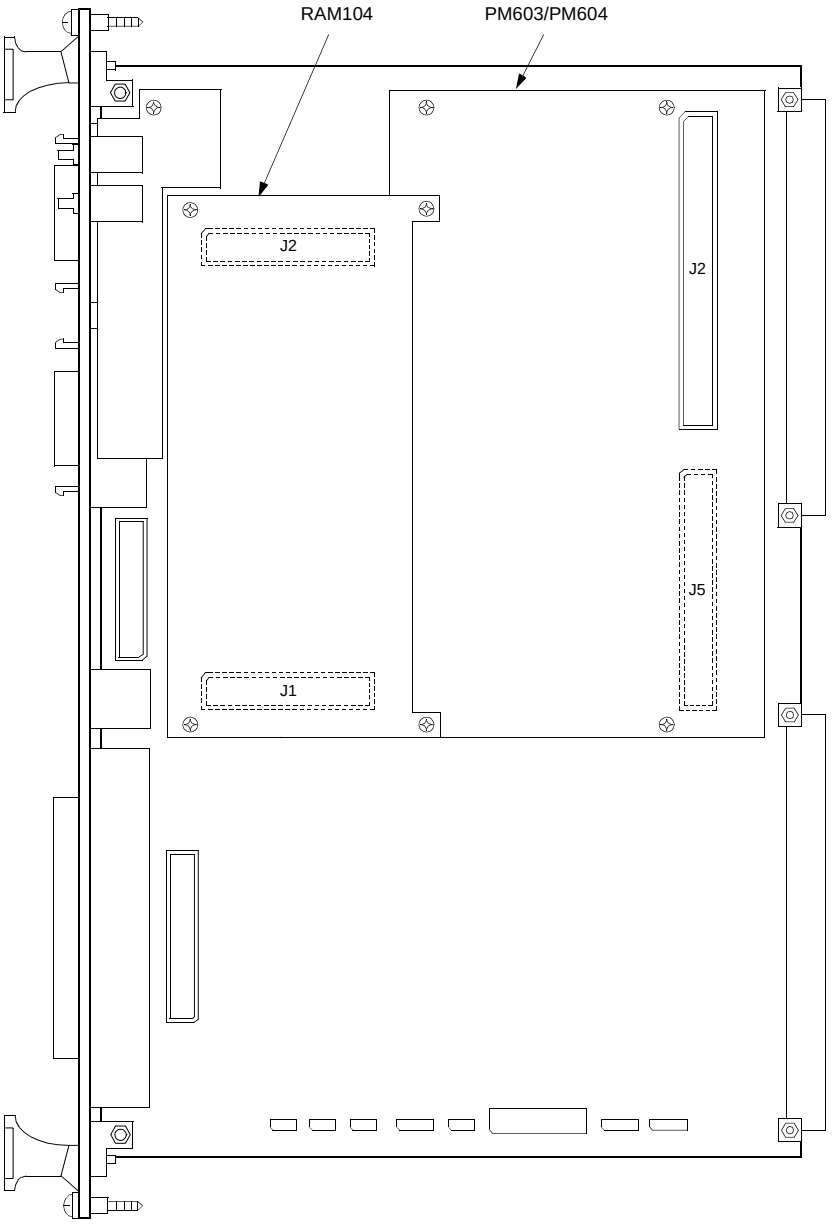


Figure 1-11. RAM104 Placement on PM603/PM604

3. Carefully remove the MVME1603/1604 from its VMEbus card slot and lay it flat on an ESD mat, component side up, with connectors P1 and P2 facing you and the PM603/PM604 corner cutout at the upper right. The ESD mat should be on a firm, flat surface.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits

4. Remove the four short Phillips screws from the holes at the top corners and the middle of the PM603/PM604.
5. Pick up the RAM104 mezzanine module, and note the positions of the male guide pins on the RAM104 connectors J1 and J2 at its left and right edges. Also note the positions of the female guide pins on the PM603/PM604 connectors. Align the RAM104 connectors J2 and J1 with the corresponding connectors J3 and J4 on the PM603/PM604, without actually setting the RAM104 on the PM603/PM604.
6. Place the RAM104 mezzanine module on top of the PM603 or PM604 mezzanine. Do NOT press the boards together yet.
7. Visually verify that the male guide pins on the RAM104 connectors are aligned with the female guide pins on the PM603/PM604 connectors. You can only see the guide pins from the sides. Do NOT press the boards together yet.

Caution

Failure to properly align the connectors on the RAM104 and the PM603/PM604 may result in damage to the modular components.

8. Place your thumbs on the top side of the RAM104 mezzanine module, in the middle of and behind each connector (J1 and (J2). Press firmly down with both thumbs until the RAM104 and the PM603/PM604 click together.
9. Visually verify that the connectors are fully seated. Connectors J2 and J1 at the left and right edges of the RAM104 should be connected with the corresponding connectors J3 and J4 on the PM603/PM604.
10. Insert two long Phillips screws through the holes at the top corners of the RAM104 module and into the standoffs on the MVME160x.

Install two similar screws in the bottom (tabbed) corners of the RAM104. Tighten the screws.

11. Reinstall the MVME1603/1604 assembly in its proper card slot. Be sure the module is seated properly in the backplane connectors. Do not damage or bend connector pins.

12. Replace the chassis or system cover(s), reconnect the system to the AC or DC power source, and turn the equipment power on.

MVME1603/1604 VMEmodule Installation

With mezzanine boards installed and headers properly configured, proceed as follows to install the MVME1603/1604 in the VME chassis:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.

2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the VMEmodules.

Caution

Inserting or removing modules with power applied may result in damage to module components.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

3. Remove the filler panel from the card slot where you are going to install the MVME1603/1604.
   – If you intend to use the MVME1603/1604 as system controller, it must occupy the leftmost card slot (slot 1). The system controller must be in slot 1 to correctly initiate the bus-grant daisy-chain and to ensure proper operation of the IACK daisy-chain driver.

– If you do not intend to use the MVME1603/1604 as system controller, it can occupy any unused double-height card slot.

4. Slide the MVME1603/1604 into the selected card slot. Be sure the module is seated properly in the P1 and P2 connectors on the backplane. Do not damage or bend connector pins.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits

5. Secure the MVME1603/1604 in the chassis with the screws provided, making good contact with the transverse mounting rails to minimize RF emissions.

6. On the chassis backplane, remove the INTERRUPT ACKNOWLEDGE (IACK) and BUS GRANT (BG) jumpers from the header for the card slot occupied by the MVME1603/1604.

Note Some VME backplanes (e.g., those used in Motorola ‘‘Modular Chassis’’ systems) have an autojumpering feature for automatic propagation of the IACK and BG signals. Step 6 does not apply to such backplane designs.

7. Replace the chassis or system cover(s), cable peripherals to the panel connectors as appropriate, reconnect the system to the AC or DC power source, and turn the equipment power on.

MVME760 Transition Module Installation

The MVME760 transition module is used in conjunction with the MVME1600-001 base board. With the MVME1603/1604 installed, refer to Figure 1-12 and proceed as follows to install an MVME760 transition module:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the VMEmodules.

Caution

Inserting or removing modules with power applied may result in damage to module components.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

3. Remove the filler panel(s) from the appropriate card slot(s) at the front or rear of the chassis. (You may need to shift other modules in the chassis to allow space for the cables connected to the MVME760 transition module.)
4. Attach the flat ribbon cable supplied with the MVME760 to the P2 backplane connector at the slot occupied by the MVME1600-001 base board. Route the cable to P2 on the transition module. Be sure to orient cable pin 1 with connector pin 1.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits

5. Secure the MVME760 in the chassis with the screws provided, making good contact with the transverse mounting rails to minimize RF emissions.
6. Replace the chassis or system cover(s), making sure no cables are pinched. Cable the peripherals to the panel connectors, reconnect the system to the AC or DC power source, and turn the equipment power on.

Note Not all peripheral cables are provided with the MVME760; you may need to fabricate or purchase certain cables. (Motorola recommends shielded cable for all peripheral connections to minimize radiation.)

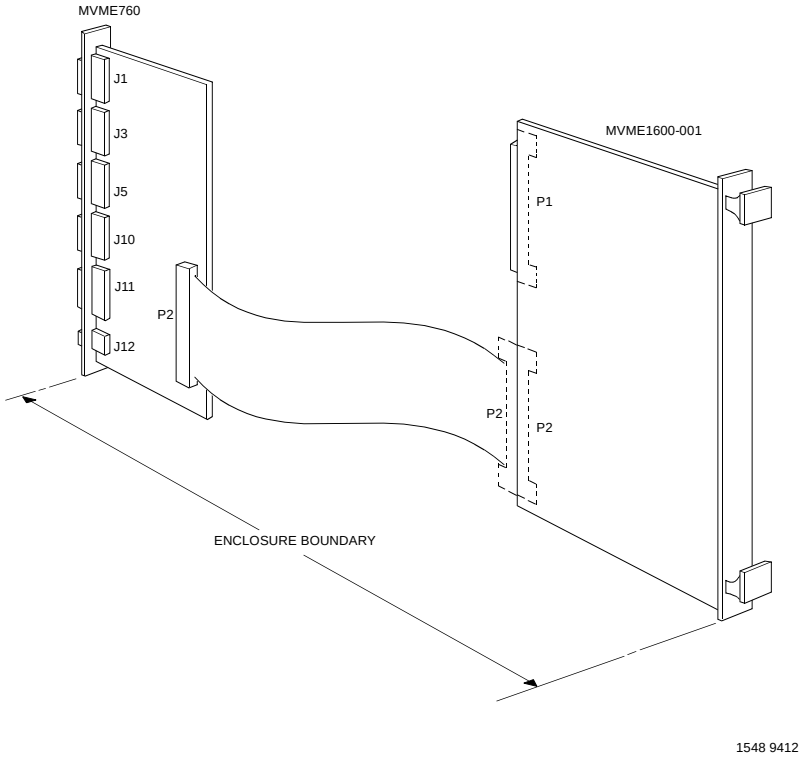


Figure 1-12. MVME760/MVME1600-001 Cable Connections

MVME712M Transition Module Installation

The MVME712M transition module is used in conjunction with the MVME1600-011 base board. With the MVME1603/1604 installed, refer to Figure 1-13 and proceed as follows to install an MVME712M transition module:

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the VMEmodules.

Caution

Inserting or removing modules with power applied may result in damage to module components.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

3. Remove the filler panel(s) from the appropriate card slot(s) at the front or rear of the chassis. (You may need to shift other modules in the chassis to allow space for the MVME712M, which has a double-wide front panel.)
4. Attach the P2 adapter board and cable(s) to the P2 backplane connector at the slot occupied by the MVME1600-011 base board.
5. Route the 64-conductor cable to P2 on the transition module. Be sure to orient cable pin 1 with connector pin 1.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage these circuits

6. Secure the MVME712M in the chassis with the screws provided, making good contact with the transverse mounting rails to minimize RF emissions.
7. Route the 50-conductor cable to the internal or external SCSI devices as appropriate to your system configuration. Be sure to orient cable pin 1 with connector pin 1.

Note The SCSI cabling can be configured in a number of ways to accommodate various device and system configurations. Figure 1-13 shows a possible configuration for use with internal SCSI devices. For more detailed information on installing the P2 adapter board and the MVME712M transition module, refer to the *MVME712M Transition Module and P2 Adapter Board User's Manual*.

8. Replace the chassis or system cover(s), making sure no cables are pinched. Cable the peripherals to the panel connectors, reconnect the system to the AC or DC power source, and turn the equipment power on.

Note Not all peripheral cables are provided with the MVME712M; you may need to fabricate or purchase certain cables. (Motorola recommends shielded cable for all peripheral connections to minimize radiation.)

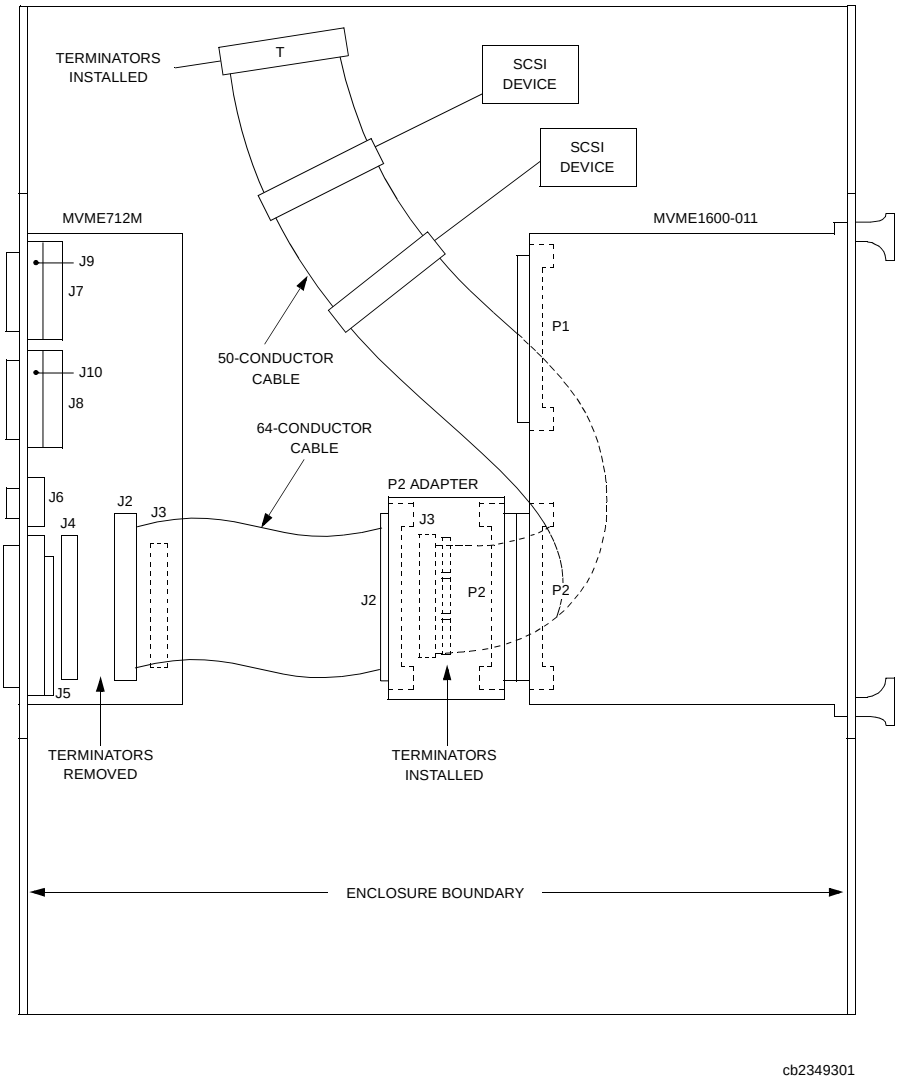


Figure 1-13. MVME712M/MVME1600-011 Cable Connections

System Considerations

The MVME1603/1604 draws power from VMEbus backplane connectors P1 and P2. P2 is also used for the upper 16 bits of data in 32-bit transfers, and for the upper 8 address lines in extended addressing mode. The MVME1603/1604 may not function properly without its main board connected to VMEbus backplane connectors P1 and P2.

Whether the MVME1603/1604 operates as a VMEbus master or as a VMEbus slave, it is configured for 32 bits of address and 32 bits of data (A32/D32). However, it handles A16 or A24 devices in the address ranges indicated in Chapter 2. D8 and/or D16 devices in the system must be handled by the PowerPC™ processor software. Refer to the memory maps in Chapter 2.

The MVME1603/1604 contains shared onboard DRAM (and, optionally, secondary cache memory) whose base address is software-selectable. Both the onboard processor and offboard VMEbus devices see this local DRAM at base physical address $00000000, as programmed by the PPCBug firmware. This may be changed via software to any other base address. Refer to the *MVME1603/MVME1604 Single Board Computer Programmer's Reference Guide* for more information.

If the MVME1603/1604 tries to access offboard resources in a nonexistent location and is not system controller, and if the system does not have a global bus timeout, the MVME1603/1604 waits forever for the VMEbus cycle to complete. This will cause the system to lock up. There is only one situation in which the system might lack this global bus timeout: when the MVME1603/1604 is not the system controller and there is no global bus timeout elsewhere in the system.

Multiple MVME1603/1604s may be installed in a single VME chassis. In general, hardware multiprocessor features are supported.

Note If you are installing multiple MVME1603/1604s in an MVME945 chassis, do not install an MVME1603/1604 in slot 12. The extra thickness of the module may cause clearance difficulties in that slot position.

Other MPUs on the VMEbus can interrupt, disable, communicate with, and determine the operational status of the processor(s). One register of the GCSR (global control/status register) set includes four bits that function as location monitors to allow one MVME1603/1604 processor to broadcast a signal to any other MVME1603/1604 processors. All eight registers are accessible from any local processor as well as from the VMEbus.

The MVME1600-001 and MVME1600-011 base boards draw +5Vdc, +12Vdc, and –12Vdc power from the VMEbus backplane through connectors P1 and P2. The 3.3Vdc power (used by the ISA Super I/O device on the base board, and by the PM603 or PM604 processor/memory mezzanine) is derived on-board from the +5Vdc.

MVME1600-001 Base Board

The MVME1600-001 base board furnishes +12Vdc, –12Vdc, and +5Vdc power to the MVME760 transition module through polyswitches (resettable fuses) F4, F2, and F3. The MVME760 uses these voltage sources to power the serial port drivers and any LAN transceivers connected to the transition module. The FUS LED (DS5) on the MVME1600-001 front panel illuminates when all three voltages are available.

The fused +5Vdc power is also supplied to the base board's keyboard and mouse connectors and to the 14-pin combined LED-mezzanine/remote-reset connector, J1.

In addition, the MVME1600-001 base board provides +5Vdc to the SCSI bus TERMPWR signal through fuse F1, located near the front panel SCSI connector. The FUS LED (DS5) on the front panel monitors the SCSI bus TERMPWR signal along with the other operating voltages; when the MVME1600-001 is connected to an SCSI bus, either directly or via the MVME760 module, SCSI terminator power helps illuminate the FUS LED.

Note Because any device on the SCSI bus can provide TERMPWR, and because the FUS LED monitors the status of several voltages, the LED does not directly indicate the condition of any single fuse. If the LED flickers or goes out, check all the fuses (polyswitches).

The MVME1600-001 base board supplies a SPEAKER_OUT signal to the 14-pin combined LED-mezzanine/remote-reset connector, J1. When J1 is used as a remote reset connector with the LED mezzanine removed, the SPEAKER_OUT signal can be cabled to an external speaker. For the pin assignments of J1, refer to Table 1-2.

MVME1600-011 Base Board

The MVME1600-011 base board provides +5Vdc power to the remote LED/switch connector (J4) through a 1A fuse (F1) located between P1 and P2. (J4 provides a separate connection point for a remote control and indicator panel, making it unnecessary to share the LED mezzanine connector for that purpose.) If none of the LEDs light and the ABORT and RESET switches do not operate, check fuse F1.

The MVME1600-011 base board provides +12Vdc power to the Ethernet transceiver interface through a 1A fuse (F2) located between P1 and P2. The FUS LED lights to indicate that +12Vdc is available. With the MVME712M transition module connected, the yellow DS1 LED on the MVME712M also signals the availability of LAN power, indicating in turn that the fuse is good. If the Ethernet transceiver fails to operate, check fuse F2.

The MVME1600-011 base board supplies SCSI terminator power through a 1A fuse (F1) located on the P2 adapter board. If the fuse is blown, the SCSI device(s) may function erratically or not at all. With the P2 adapter board cabled to an MVME712M and with an SCSI bus connected to the MVME712M, the green DS2 LED on the MVME712M illuminates when SCSI terminator power is available. If the DS2 LED flickers during SCSI bus operation, check fuse F1 on the P2 adapter board.

Like the MVME1600-001 base board, the MVME1600-011 supplies a SPEAKER_OUT signal to the 14-pin LED mezzanine connector, J1. Unlike the MVME1600-001 base board, the MVME1600-011 also applies the SPEAKER_OUT signal to the dedicated remote status and control connector, J4. The LED mezzanine need not be removed to cable the SPEAKER_OUT signal to an external speaker. For the pin assignments of J4, refer to Table 1-3.

Operating Instructions 2

Introduction

This chapter provides information for use of the MVME1603/1604 family of Single Board Computers in a system configuration. Here you will find the power-up procedure and descriptions of switches and LEDs; memory maps; and software initialization.

Applying Power

After you have verified that all necessary hardware preparation has been done, that all connections have been made correctly, and that the installation is complete, you can power up the system. When power is applied, the PPCBug firmware executes various self-tests and then displays the debugger prompt `PPC1-Bug` (if the firmware is in Bug mode). If the firmware was previously placed in System mode, it displays the prompt `PPC1-Diag`, performs self-tests, and tries to autoboot. You can press ESC to skip the self-tests, or press ABORT or BREAK to interrupt them.

For further information on the PPCBug firmware, refer to Chapter 5, *PPCBug*, Appendix D, *Troubleshooting CPU Boards*, or to the *PPCBug Firmware Package User's Manual*.

The MVME1603/1604 front panel has ABORT and RESET switches and six LED (light-emitting diode) status indicators (CHS, BFL, CPU, PCI, FUS, SYS). The switches and LEDs are mounted on an LED mezzanine board that plugs into the base board.

ABORT Switch (S1)

When activated by software, the ABORT switch can generate an interrupt signal from the base board to the processor at a user-programmable level. The interrupt is normally used to abort program execution and return control to the PPCBug debugger firmware located in the

MVME1603/1604 EPROM and Flash memory. The interrupt signal reaches the processor module via ISA bus interrupt line IRQ8*. The signal is also available at pin PB7 of the Z8536 CIO device, which handles various status signals, serial I/O lines, and counters.

The interrupter connected to the ABORT switch is an edge-sensitive circuit, filtered to remove switch bounce.

RESET Switch (S2)

The RESET switch resets all onboard devices; it also drives a SYSRESET* signal if the MVME1603/1604 is the system controller. The RESET switch may be disabled by software.

The VMEchip2 includes both a global and a local reset driver. When the VMEchip2 operates as the VMEbus system controller, the reset driver provides a global system reset by asserting the VMEbus signal SYSRESET*. A SYSRESET* signal may be generated by the RESET switch, a power-up reset, a watchdog timeout, or by a control bit in the LCSR in the VMEchip2. SYSRESET* remains asserted for at least 200 ms, as required by the VMEbus specification.

Similarly, the VMEchip2 supplies an input signal and a control bit to initiate a local reset operation. By setting a control bit, software can maintain a board in a reset state, disabling a faulty board from participating in normal system operation. The local reset driver is enabled even when the VMEchip2 is not system controller. Local resets may be generated by the RESET switch, a power-up reset, a watchdog timeout, a VMEbus SYSRESET*, or a control bit in the GCSR.

Note For an MVME1603/1604 without the VMEbus option (i.e., with no VMEchip2), the LCSR control bit is not available to reset the module. In this case, the watchdog timer is allowed to time out to reset the MVME1603/1604.

Front Panel Indicators (DS1 - DS6)

There are six LEDs on the MVME1603/1604 front panel: CHS, BFL, CPU, PCI, FUS, and SYS.

- CHS (DS1, yellow). Checkstop; driven by the MPC603/604 status lines on the MVME1603/1604. Lights when a halt condition from the processor is detected.
- BFL (DS2, yellow). Board Failure; lights when the BRDFAIL* signal line is active.
- CPU (DS3, green). CPU activity; lights when the DBB* (Data Bus Busy) signal line on the processor bus is active.
- PCI (DS4, green). PCI activity; lights when the IRDY* (Initiator Ready) signal line on the PCI bus is active. This indicates that the PCI mezzanine (if installed) is active.
- FUS (DS5, green). Fuse OK; lights when +5Vdc, +12Vdc, and –12Vdc power is available from the base board to the transition module and remote devices.

Note The circuitry monitored by the FUS LED differs between the MVME1600-001 and MVME1600-011 versions of the base board. The differences are detailed under the respective base board descriptions in Chapter 1.

Because the FUS LED monitors the status of several voltages on the MVME1600-001, it does not directly indicate the condition of any single fuse. If the LED flickers or goes out, check all the fuses (polyswitches).

- SYS (DS6, green). System Controller; lights when the VMEchip2 in the MVME1603/1604 is the VMEbus system controller.

2

Memory Maps

There are three points of view for memory maps:

- The mapping of all resources as viewed by the processor (MPU bus memory map)
- The mapping of onboard resources as viewed by PCI local bus masters (PCI bus memory map)
- The mapping of onboard resources as viewed by VMEbus masters (VMEbus memory map)

The following sections describe the MVME1603/1604 memory organization from the above three points of view. Additional, more detailed memory maps can be found in the *Programmer's Reference Guide* (part number V1600-1A/PG).

MPU Bus Memory Map

The MPU bus memory map is split into different address spaces by the Transfer Type (TT) signals. The local resources respond to the normal access and interrupt acknowledge codes.

Normal Address Range

The memory map of devices that respond to the normal address range is shown in the following tables. The normal address range is defined by the TT signals on the MPU bus. For the MVME1603/1604, transfer types 0, 1, and 2 define the normal address range. Table 2-1 defines the entire map ($00000000 to $FFFFFFFF). Many areas of the map are user-programmable, and suggested uses are shown in the table. The cache inhibit function is programmable in the PowerPC 603/604 microprocessor MMU. The onboard I/O space must be marked ''cache inhibit'' and serialized in its page table. Table 2-2 further defines the map for the local I/O devices (accessible through the directly mapped PCI Configuration Space).

Table 2-1. Processor View of the Memory Map

Processor Address		Size	PCI Address Generated		Definition	Notes
Start	End		Start	End		
00000000	7FFFFFFF	2GB			DRAM - Not Forwarded to PCI	
80000000	807FFFFF	8MB	00000000	007FFFFF	ISA/PCI I/O Space	1, 2, 6
80800000	80FFFFFF	8MB	00800000	00FFFFFF	PCI Configuration Space (Direct Map)	3
81000000	BF7FFFFF	1GB-24MB	01000000	3F7FFFFF	PCI I/O Space	
BF800000	BFFFFFEF	8MB -16B			Reserved	
BFFFFFF0	BFFFFFFF	16B	3FFFFFF0	3FFFFFFF	PCI IACK/ Special Cycles	7
C0000000	C0FFFFFF	16MB	00000000	00FFFFFF	PCI/ISA Memory Space	
C1000000	FEFFFFFF	1GB-32MB	01000000	3EFFFFFF	PCI Memory Space	
FF000000	FF07FFFF	512KB			EPROM/FLASH Bank 0	4
FF080000	FF0FFFFF	512KB			EPROM/FLASH Bank 1	4
FF100000	FFEFFFFF	14MB			Reserved	4, 5
FFF00000	FFF7FFFF	512KB			EPROM/FLASH Bank 0 Repeat	4
FFF80000	FFFFFFFF	512KB			EPROM/FLASH Bank 1 Repeat	4

Notes

1. PCI configuration accesses to CF8 (Configuration Address) and CFC (Configuration Data) are supported by the MPC105 PCI bridge/memory controller as specified in the PCI Specification Revision 2.0.
2. Both Contiguous and Discontiguous mappings are supported by the MVME1603/1604. Refer to the *ISA/PCI I/O Space Mapping* table for more details.
3. This space is used for Direct Mapped PCI Configuration Space accesses. Refer to the *PCI Configuration Space Mapping* section for more details.
4. EPROM/FLASH decoding repeats every 1MB for this entire 16MB range.
5. The usage of this 14MB address range for EPROM/FLASH is not recommended, since future PowerPC products will redefine this area.
6. The M48T18 RTC and NVRAM device is mapped in this area. Refer to the *ISA/PCI I/O Space Mapping* table for more details.
7. A read of any byte within this 16-byte range (BFFFFFF0 through BFFFFFFF) causes a PCI IACK cycle. The data read is the IACK vector.

Table 2-2 focuses on the map for the local I/O devices (accessible through the directly mapped PCI Configuration Space).

Table 2-2. PCI Configuration Space Memory Map

IDSEL	Processor Address		PCI Address Generated		Definition
	Start	End	Start	End	
	80800000	808007FF	00800000	008007FF	Reserved
A11	80800800	808008FF	00800800	008008FF	IBC Configuration Registers (PCI/ISA bridge)
	80800900	80800FFF	00800900	00800FFF	Reserved
A12	80801000	808010FF	00801000	008010FF	53C810/825 Configuration Registers (SCSI)
	80801100	80801FFF	00801100	00801FFF	Reserved
A13	80802000	808020FF	00802000	008020FF	VME2PCI Configuration Registers (VMEbus)
	80802100	80803FFF	00802100	00803FFF	Reserved
A14	80804000	808040FF	00804000	008040FF	DECchip 21040 Configuration Registers (Ethernet)
	80804100	80807FFF	00804100	00807FFF	Reserved
A15	80808000	808080FF	00808000	008080FF	GD5446 Configuration Registers (graphics)
	80808100	8080FFFF	00808100	0080FFFF	Reserved
A16	80810000	808100FF	00810000	008100FF	PMC Slot Configuration Registers (PCI Mezzanine)
	80810100	80FFFFFF	00810100	00FFFFFF	Reserved

Note Accesses to *Reserved* space may select multiple devices and produce unpredictable results.

Table 2-3 focuses on the mapping of the ISA/PCI I/O space from the processor view of the memory map.

Table 2-3. ISA/PCI I/O Space Memory Map

ISA I/O Address	Processor Address		Function	Notes
	Contiguous	Discontiguous		
0000-000F	8000 0000 - 8000 000F	8000 0000 - 8000 000F	IBC: DMA1 Registers & Control	2
0020-0021	8000 0020 - 8000 0021	8000 1000 - 8000 1001	IBC: Interrupt 1 Control & Mask	2
0040-0043	8000 0040 - 8000 0043	8000 2000 - 8000 2003	IBC: Timer Counter 1 Registers	2
0060	8000 0060	8000 3000	IBC: Reset Ubus IRQ12	2
0061	8000 0061	8000 3001	IBC: NMI Status and Control	2
0064	8000 0064	8000 3004	ISASIO: Keyboard Controller Port	3
0074	8000 0074	8000 3014	NVRAM/RTC Address Strobe 0	
0075	8000 0075	8000 3015	NVRAM/RTC Address Strobe 1	
0077	8000 0077	8000 3017	NVRAM/RTC Data Port	
0080-0090	8000 0080 - 8000 0090	8000 4000 - 8000 4010	IBC: DMA Page Registers	2
0092	8000 0092	8000 4012	IBC: Port 92 Register	2
0094-009F	8000 0094 - 8000 009F	8000 4014 - 8000 401F	IBC: DMA Page Registers	2
00A0-00A1	8000 00A0 - 8000 00A1	8000 5000 - 8000 5001	IBC: Interrupt 2 Control & Mask	2
00C0-00CF	8000 00C0 - 8000 00CF	8000 6000 - 8000 600F	IBC: DMA2 Address Registers	2
00D0-00DF	8000 00D0 - 8000 00DF	8000 7000 - 8000 700F	IBC: DMA2 Control Registers	2
02F8-02FF	8000 02F8 - 8000 02FF	8001 7018 - 8001 701F	ISASIO: Serial Port 2 (COM2)	3
0398	8000 0398	8001 C018	ISASIO Index Register	2
0399	8000 0399	8001 C019	ISASIO Data Register	2
03BC-03BF	8000 03BC - 8000 03BF	8001 D01C - 8001 D01F	ISASIO: Parallel Port (LPT1)	3
03F0-03F7	8000 03F0 - 8000 03F7	8001 F010 - 8001 F017	ISASIO: Floppy Drive Controller (FDC)	3
03F8-03FF	8000 03F8 - 8000 03FF	8001 F018 - 8001 F01F	ISASIO: Serial Port 1 (COM1)	3
040A	8000 040A	8002 000A	IBC: Scatter/Gather Interrupt Status Register	2

Table 2-3. ISA/PCI I/O Space Memory Map (Continued)

ISA I/O Address	Processor Address		Function	Notes
	Contiguous	Discontiguous		
040B	8000 040B	8002 000B	IBC: DMA1 Extended Mode Register	2
0410-041F	8000 0410 - 8000 041F	8002 0010 - 8002 001F	IBC: DMA Scatter/Gather Command and Status Registers	2
0420-042F	8000 0420 - 8000 042F	8002 1000 - 8002 100F	IBC: DMA CH0-CH3 Scatter/Gather Descriptor Table Pointers	2
0430-043F	8000 0430 - 8000 043F	8002 1010 - 8002 101F	IBC: DMA CH4-CH7 Scatter/Gather Descriptor Table Pointers	2
0481-048B	8000 0481 - 8000 048B	8002 4001 - 8002 400B	IBC: DMA High Page Registers	2
04D0	8000 04D0	8002 6010	IBC: INT1 Edge Level Control	2
04D1	8000 04D1	8002 6011	IBC: INT2 Edge Level Control	2
04D6	8000 04D6	8002 6016	IBC: DMA2 Extended Mode Register	2
0C04	8000 0C04	8006 0004	IBC: Power Control Output Port	2, 4
0C01	8000 0C01	8006 0001	IBC: Test Mode Control Port/Shadow Register of Port 70	2, 4
0800	8000 0800	8004 0000	CPU Configuration Register	4, 6
0801	8000 0801	8004 0001	Software Readable Header	4
0802	8000 0802	8004 0002	Board Configuration Register	4
0803	8000 0803	8004 0003	Reserved	4
0804	8000 0804	8004 0004	DRAM Size Register	4, 6
0805	8000 0805	8004 0005	Reserved	4
0806	8000 0807	8004 0006	Reserved	4
0807	8000 0807	8004 0007	Reserved	4
0820	8000 0820	8004 1000	Reserved for Cooling Monitor	4
0830	8000 0830	8004 1010	Reserved for Audio	4
0840	8000 0840	8004 2000	Z85230: Port B (Serial Port 4) Control	4
0841	8000 0841	8004 2001	Z85230: Port B (Serial Port 4) Data	4
0842	8000 0842	8004 2002	Z85230: Port A (Serial Port 3) Control	4
0843	8000 0843	8004 2003	Z85230: Port A (Serial Port 3) Data	4
0844	8000 0844	8004 2004	Z8536 CIO: Port C's Data Register	4
0845	8000 0845	8004 2005	Z8536 CIO: Port B's Data Register	4
0846	8000 0846	8004 2006	Z8536 CIO: Port A's Data Register	4
0847	8000 0847	8004 2007	Z8536 CIO: Control Register	4
084F	8000 084F	8004 200F	Z85230/Z8536 Pseudo IACK	4, 5

Notes

1. All ISA I/O locations not specified in this table are reserved.
2. These locations are internally decoded by the IBC (PCI/ISA bridge).
3. These locations are internally decoded by the ISASIO (ISA Super I/O controller).
4. These locations are either not specified by the PowerPC Reference Platform (PRP) specification or are not PRP-compliant. They may overlap some other functions specified by the PRP specification.
5. An IACK vector is returned from either the Z8536 or the Z85230 when this location is read.
6. These registers physically reside on the PM603/604 module.
7. The board comes up in contiguous mode. Contiguous and discontiguous modes are programmed by the MPC105 PCI bridge/memory controller.

Caution

The PPCBug debugger and several operating systems execute in contiguous mode. If this is changed to discontiguous mode, PPCBug will cease to function correctly.

PCI Local Bus Memory Map

Table 2-4 shows the mapping of onboard resources from the point of view of the PCI local bus.

Table 2-4. PCI View of the Memory Map

PCI Address		Size	Processor Bus Address		Definition	Notes
Start	End		Start	End		
00000000	00FFFFFF	16MB	Not forwarded to MPU bus		PCI/ISA Memory Space	1, 2
01000000	7FFFFFFF	2GB-16MB	Not forwarded to MPU bus		PCI Memory Space	2
80000000	FFFFFFFF	2GB	00000000	7FFFFFFF	Onboard DRAM (via MPC105)	
00000000	FFFFFFFF	4GB	Not forwarded to MPU bus		PCI/ISA I/O Space	

Notes

1. The IBC (PCI/ISA bridge) performs subtractive decoding in this range and forwards the PCI memory cycle to the ISA if DEVSEL∗ is not detected.
2. The VME2PCI ASIC can be programmed to claim some of this address range to forward the PCI memory cycle to the VMEchip2.

VMEbus Memory Map

The VMEbus is programmable. The mapping of local resources as viewed by VMEbus masters varies among applications.

The VMEchip2 ASIC includes a user-programmable map decoder for the VMEbus-to-local-bus interface. The map decoder enables you to program the starting and ending address and the modifiers to which the MVME1603/1604 responds.

The VMEchip2 also includes a user-programmable map decoder for the GCSRs (global control/status registers, accessible from both the VMEbus and the local bus). The GCSR map decoder allows you to program the starting address of the GCSRs in the VMEbus short I/O space.

The VME2PCI ASIC supplies the interface between the PCI local bus and the VMEchip2 ASIC. Table 2-5 shows the mapping of onboard resources from the point of view of the VME2PCI.

Table 2-5. VME2PCI View of the Memory Map

Processor Address	PCI Configuration Address	Register Name	Read/Write	Reset Value (Hexadecimal)
80802000	00802000	PCI Vendor ID	R	1057h
80802002	00802002	PCI Device ID	R	4800h
80802004	00802004	PCI Command	R/W	0000h
80802006	00802006	PCI Status	R/W	0000h
80802008	00802008	PCI Revision ID	R	01
80802009	00802009	PCI Class Code	R	068000h
8080200C	0080200C	PCI Cache Line Size	R/W	00h
8080200D	0080200D	PCI Latency Timer	R/W	00h
8080200E	0080200E	PCI Header Type	R	00h
80802010	00802010	PCI I/O Base Address	R/W	00000001h
80802014	00802014	PCI Memory Base Address	R/W	00000000h
8080203C	0080203C	PCI Interrupt Line	R/W	00h
8080203D	0080200D	PCI Interrupt Pin	R	01h
8080203E	0080200E	PCI Minimum Grant	R	00
8080203F	0080200F	PCI Maximum Latency	R	00
80802040	00802040	Slave Starting Address 1	R/W	0000h
80802042	00802042	Slave Ending Address 1	R/W	0000h
80802044	00802044	Slave Address Offset 1	R/W	0000h
80802046	00802046	Slave Address Enable 1	R/W	00h
80802048	00802048	Slave Starting Address 2	R/W	0000h
8080204A	0080204A	Slave Ending Address 2	R/W	0000h
8080204C	0080204C	Slave Address Offset 2	R/W	0000h
8080204D	0080204D	Slave Address Enable 2	R/W	00h
80802050	00802050	Interrupt Status and Control	R/W	0000h

Table 2-6 shows the mapping of onboard resources from the point of view of the VMEchip2.

2

Table 2-6. VMEchip2 Memory Map (Sheet 1 of 3)

VMEchip2 LCSR Base Address = $BASE + 0000

OFFSET:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	SLAVE ENDING ADDRESS 1															
4	SLAVE ENDING ADDRESS 2															
8	SLAVE ADDRESS TRANSLATION ADDRESS 1															
C	SLAVE ADDRESS TRANSLATION ADDRESS 2															
10					ADDER 2	SNP 2		WP 2	SUP 2	USR 2	A32 2	A24 2	BLK D64 2	BLK 2	PRGM 2	DATA 2
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
14	MASTER ENDING ADDRESS 1															
18	MASTER ENDING ADDRESS 2															
1C	MASTER ENDING ADDRESS 3															
20	MASTER ENDING ADDRESS 4															
24	MASTER ADDRESS TRANSLATION ADDRESS 4															
28	MAST D16 EN	MAST WP EN	MASTER AM 4						MAST D16 EN	MAST WP EN	MASTER AM 3					
2C	GCSR GROUP SELECT								GCSR BOARD SELECT				MAST 4 EN	MAST 3 EN	MAST 2 EN	MAST 1 EN
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
30											WAIT RMW	ROM ZERO	DMA TB SNP MODE		SRAM SPEED	
34																
38	DMA CONTROLLER															
3C	DMA CONTROLLER															
40	DMA CONTROLLER															
44	DMA CONTROLLER															
48		TICK 2/1	TICK IRQ 1 EN	CLR IRQ	IRQ STAT	VMEBUS INTERRUPT LEVEL			VMEBUS INTERRUPT VECTOR							

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLAVE STARTING ADDRESS 1															
SLAVE STARTING ADDRESS 2															
SLAVE ADDRESS TRANSLATION SELECT 1															
SLAVE ADDRESS TRANSLATION SELECT 2															
				ADDER 1	SNP 1		WP 1	SUP 1	USR 1	A32 1	A24 1	BLK D64 1	BLK 1	PRGM 1	DATA 1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASTER STARTING ADDRESS 1															
MASTER STARTING ADDRESS 2															
MASTER STARTING ADDRESS 3															
MASTER STARTING ADDRESS 4															
MASTER ADDRESS TRANSLATION SELECT 4															
MAST D16 EN	MAST WP EN	MASTER AM 2						MAST D16 EN	MAST WP EN	MASTER AM 1					
IO2 EN	IO2 WP EN	IO2 S/U	IO2 P/D	IO1 EN	IO1 D16 EN	IO1 WP EN	IO1 S/U	ROM SIZE		ROM BANK B SPEED			ROM BANK A SPEED		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ARB ROBN	MAST DHB	MAST DWB		MST FAIR	MST RWD	MASTER VMEBUS		DMA HALT	DMA EN	DMA TBL	DMA FAIR	DM RELM		DMA VMEBUS	
DMA TBL INT	DMA LB SNP MODE			DMA INC VME	DMA INC LB	DMA WRT	DMA D16	DMA D64 BLK	DMA BLK	DMA AM 5	DMA AM 4	DMA AM 3	DMA AM 2	DMA AM 1	DMA AM 0
LOCAL BUS ADDRESS COUNTER															
VMEBUS ADDRESS COUNTER															
BYTE COUNTER															
TABLE ADDRESS COUNTER															
DMA TABLE INTERRUPT COUNT				MPU CLR STAT	MPU LBE ERR	MPU LPE ERR	MPU LOB ERR	MPU LTO ERR	DMA LBE ERR	DMA LPE ERR	DMA LOB ERR	DMA LTO ERR	DMA TBL ERR	DMA VME ERR	DMA DONE

1360 9403

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2

Table 2-6. VMEchip2 Memory Map (Sheet 2 of 3)

VMEchip2 LCSR Base Address = $BASE + 0000
OFFSET:

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
4C								ARB BGTO EN	DMA TIME OFF			DMA TIME ON			VME GLOBAL TIMER	
50	TICK TIMER 1															
54	TICK TIMER 1															
58	TICK TIMER 2															
5C	TICK TIMER 2															
60		SCON	SYS FAIL	BRD FAIL STAT	PURS STAT	CLR PURS STAT	BRD FAIL OUT	RST SW EN	SYS RST	WD CLR TO	WD CLR CNT	WD TO STAT	TO BF EN	WD SRST LRST	WD RST EN	WD EN
64	PRE															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
68	AC FAIL IRQ	AB IRQ	SYS FAIL IRQ	MWP BERR IRQ	PE IRQ	IRQ1E IRQ	TIC2 IRQ	TIC1 IRQ	VME IACK IRQ	DMA IRQ	SIG3 IRQ	SIG2 IRQ	SIG1 IRQ	SIG0 IRQ	LM1 IRQ	LM0 IRQ
6C	EN IRQ 31	EN IRQ 30	EN IRQ 29	EN IRQ 28	EN IRQ 27	EN IRQ 26	EN IRQ 25	EN IRQ 24	EN IRQ 23	EN IRQ 22	EN IRQ 21	EN IRQ 20	EN IRQ 19	EN IRQ 18	EN IRQ 17	EN IRQ 16
70																
74	CLR IRQ 31	CLR IRQ 30	CLR IRQ 29	CLR IRQ 28	CLR IRQ 27	CLR IRQ 26	CLR IRQ 25	CLR IRQ 24	CLR IRQ 23	CLR IRQ 22	CLR IRQ 21	CLR IRQ 20	CLR IRQ 19	CLR IRQ 18	CLR IRQ 17	CLR IRQ 16
78		AC FAIL IRQ LEVEL				ABORT IRQ LEVEL				SYS FAIL IRQ LEVEL				MST WP ERROR IRQ LEVEL		
7C		VME IACK IRQ LEVEL				DMA IRQ LEVEL				SIG 3 IRQ LEVEL				SIG 2 IRQ LEVEL		
80		SW7 IRQ LEVEL				SW6 IRQ LEVEL				SW5 IRQ LEVEL				SW4 IRQ LEVEL		
84		SPARE IRQ LEVEL				VME IRQ 7 IRQ LEVEL				VME IRQ 6 IRQ LEVEL				VME IRQ 5 IRQ LEVEL		
88	VECTOR BASE REGISTER 0				VECTOR BASE REGISTER 1				MST IRQ EN	SYS FAIL LEVEL	AC FAIL LEVEL	ABORT LEVEL	GPIOEN			
8C																

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VME ACCESS TIMER		LOCAL BUS TIMER		WD TIME OUT SELECT				PRESCALER CLOCK ADJUST							
COMPARE REGISTER															
COUNTER															
COMPARE REGISTER															
COUNTER															
OVERFLOW COUNTER 2					CLR OVF 2	COC EN 2	TIC EN 2	OVERFLOW COUNTER 1					CLR OVF 1	COC EN 1	TIC EN 1
SCALER															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SW7 IRQ	SW6 IRQ	SW5 IRQ	SW4 IRQ	SW3 IRQ	SW2 IRQ	SW1 IRQ	SW0 IRQ	SPARE	VME IRQ7	VME IRQ6	VME IRQ5	VME IRQ4	VME IRQ3	VME IRQ2	VME IRQ1
EN IRQ 15	EN IRQ 14	EN IRQ 13	EN IRQ 12	EN IRQ 11	EN IRQ 10	EN IRQ 9	EN IRQ 8	EN IRQ 7	EN IRQ 6	EN IRQ 5	EN IRQ 4	EN IRQ 3	EN IRQ 2	EN IRQ 1	EN IRQ 0
SET IRQ 15	SET IRQ 14	SET IRQ 13	SET IRQ 12	SET IRQ 11	SET IRQ 10	SET IRQ 9	SET IRQ 8								
CLR IRQ 15	CLR IRQ 14	CLR IRQ 13	CLR IRQ 12	CLR IRQ 11	CLR IRQ 10	CLR IRQ 9	CLR IRQ 8								
	P ERROR IRQ LEVEL				IRQ1E IRQ LEVEL				TIC TIMER 2 IRQ LEVEL				TIC TIMER 1 IRQ LEVEL		
	SIG 1 IRQ LEVEL				SIG 0 IRQ LEVEL				LM 1 IRQ LEVEL				LM 0 IRQ LEVEL		
	SW3 IRQ LEVEL				SW2 IRQ LEVEL				SW1 IRQ LEVEL				SW0 IRQ LEVEL		
	VME IRQ 4 IRQ LEVEL				VMEB IRQ 3 IRQ LEVEL				VME IRQ 2 IRQ LEVEL				VME IRQ 1 IRQ LEVEL		
GPIOO				GPIOI				GPI							
								MP IRQ EN	REV EROM	DIS SRAM	DIS MST	NO EL BBSY	DIS BSYT	EN INT	DIS BGN

1361 9403

← This sheet begins on facing page.

Table 2-6. VMEchip2 Memory Map (Sheet 3 of 3)

VMEchip2 GCSR Base Address = $BASE + 0100

Offsets																	
VME-bus	**Local Bus**	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	CHIP REVISION								CHIP ID							
2	4	LM3	LM2	LM1	LM0	SIG3	SIG2	SIG1	SIG0	RST	ISF	BF	SCON	SYSFL	X	X	X
4	8	GENERAL PURPOSE CONTROL AND STATUS REGISTER 0															
6	C	GENERAL PURPOSE CONTROL AND STATUS REGISTER 1															
8	10	GENERAL PURPOSE CONTROL AND STATUS REGISTER 2															
A	14	GENERAL PURPOSE CONTROL AND STATUS REGISTER 3															
C	18	GENERAL PURPOSE CONTROL AND STATUS REGISTER 4															
E	1C	GENERAL PURPOSE CONTROL AND STATUS REGISTER 5															

Programming Considerations

Good programming practice dictates that only one MPU at a time have control of the MVME1603/1604 control registers. Of particular note are:

- Registers that modify the address map
- Registers that require two cycles to access
- VMEbus interrupt request registers

PCI Arbitration

There are 6 potential PCI bus masters on the MVME1603/MVME1604 single-board computer:

- MPC105 (PCI/MPU bus bridge and memory controller)
- IBC (PCI/ISA bus bridge controller)
- DECchip 21040 Ethernet controller
- 53C825 (or 53C810) SCSI controller
- VME2PCI ASIC (PCI/VMEchip2 interface ASIC
- PMC (PCI mezzanine card) slot

The IBC supplies the PCI arbitration support for these six devices. The IBC supports flexible arbitration modes of fixed priority, rotating priority, and mixed priority.

The IBC registers that control the arbitration mode are the PCI Arbiter Priority Control (PAPC) Register and the PCI Arbiter Priority Control Extension (ARBPRIX) Register. The PAPC register and the ARBPRIX register default to 04 (hex) and 00 (hex) respectively. This default configuration puts the CPU (MPC105) at the highest priority level. Refer to the S82378ZB Reference Manual for programming information.

The following figure shows the arbitration configuration diagram of the IBC. Additional details on PCI arbitration can be found in the *Programmer's Reference Guide* (part number V1600-1A/PG).

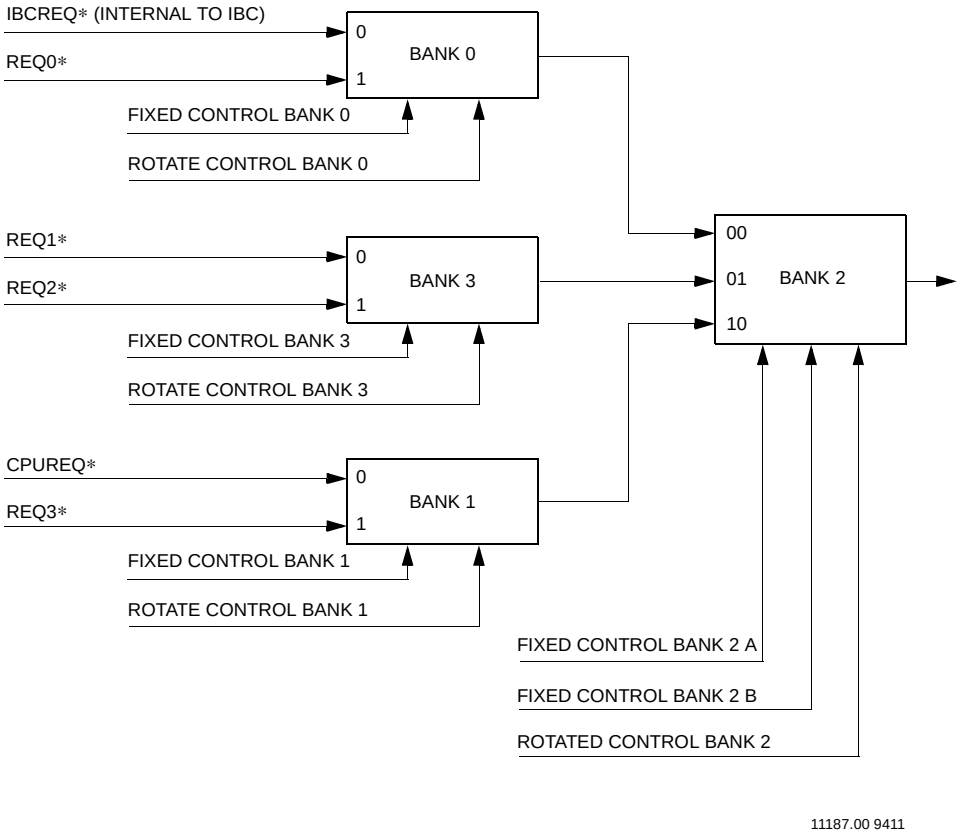


Figure 2-1. IBC Arbiter Configuration Diagram

The PCI arbitration assignments for all PCI masters on the MVME1603/MVME1604 are as follows:

Table 2-7. PCI Arbitration Assignments

PCI BUS REQUEST	CPUREQ*	IBCREQ*	REQ0*	REQ1*	REQ2*	REQ3*
PCI MASTER	CPU (MPC105)	IBC (Internal)	SCSI (53C825)	LANC (DECchip 21040)	VME (VME2PCI)	PMC Slot

Interrupt Handling

The MVME1603/MVME1604 supports both maskable and non-maskable interrupts. The following figure illustrates the interrupt architecture.

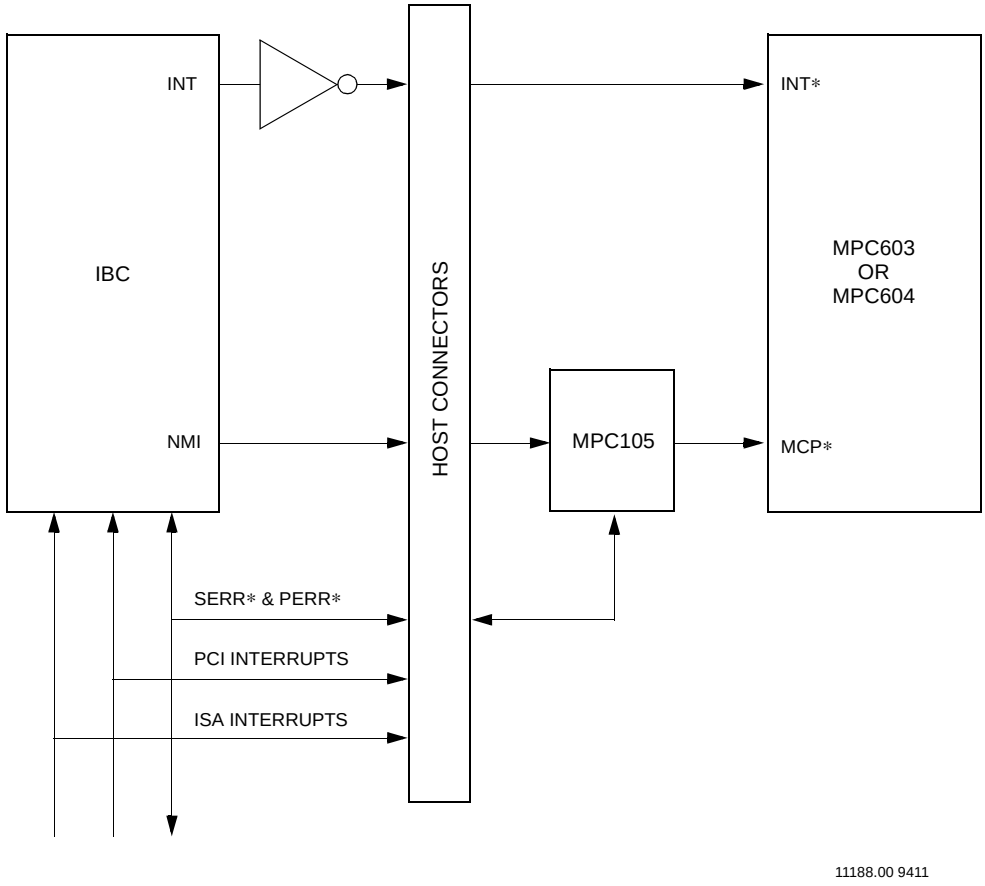


Figure 2-2. MVME1603/MVME1604 Interrupt Architecture

Machine Check Interrupt (MCP∗)

The IBC can be programmed to assert NMI when it detects either SERR∗ low on the PCI Local Bus or IOCHK∗ low on the ISA bus. However, IOCHK∗ is not used on the MVME1603/MVME1604. The MPC105 will assert MCP∗ to the processor upon detecting a high level on NMI from the IBC.

Note that MPC105 also monitors SERR∗ and PERR∗. It can be programmed to asserted MCP∗ when it detects a low level on either SERR∗ or PERR∗.

The MPC105 can also be programmed to assert MCP∗ under many other conditions. Refer to the *Programmer's Reference Guide* (part number V1600-1A/PG) for additional information on the MCP∗ interrupt signal.

Maskable Interrupts

The IBC supports 15 interrupt requests. These 15 interrupts are ISA-type interrupts that are functionally equivalent to two 82C59 interrupt controllers. Except for IRQ0, IRQ1, IRQ2, IRQ8∗, and IRQ13, each of the interrupt lines can be configured for either edge-sensitive or level-sensitive mode by programming the appropriate ELCR registers in the IBC.

The IBC also supports four PCI interrupts: INT3∗-INT0∗. The IBC has four PIRQ Route Control Registers to allow each PCI interrupt line to be routed to any of eleven ISA interrupt lines (IRQ0, IRQ1, IRQ2, IRQ8∗, and IRQ13 are reserved for ISA system interrupts). Since PCI interrupts are defined as level-sensitive, software must program the selected IRQ(s) for level-sensitive mode. Note that more than one PCI interrupt can be routed to the same ISA IRQ line.

The following figure shows the IBC interrupt structure. Additional details on interrupt assignments can be found in the *Programmer's Reference Guide* (part number V1600-1A/PG).

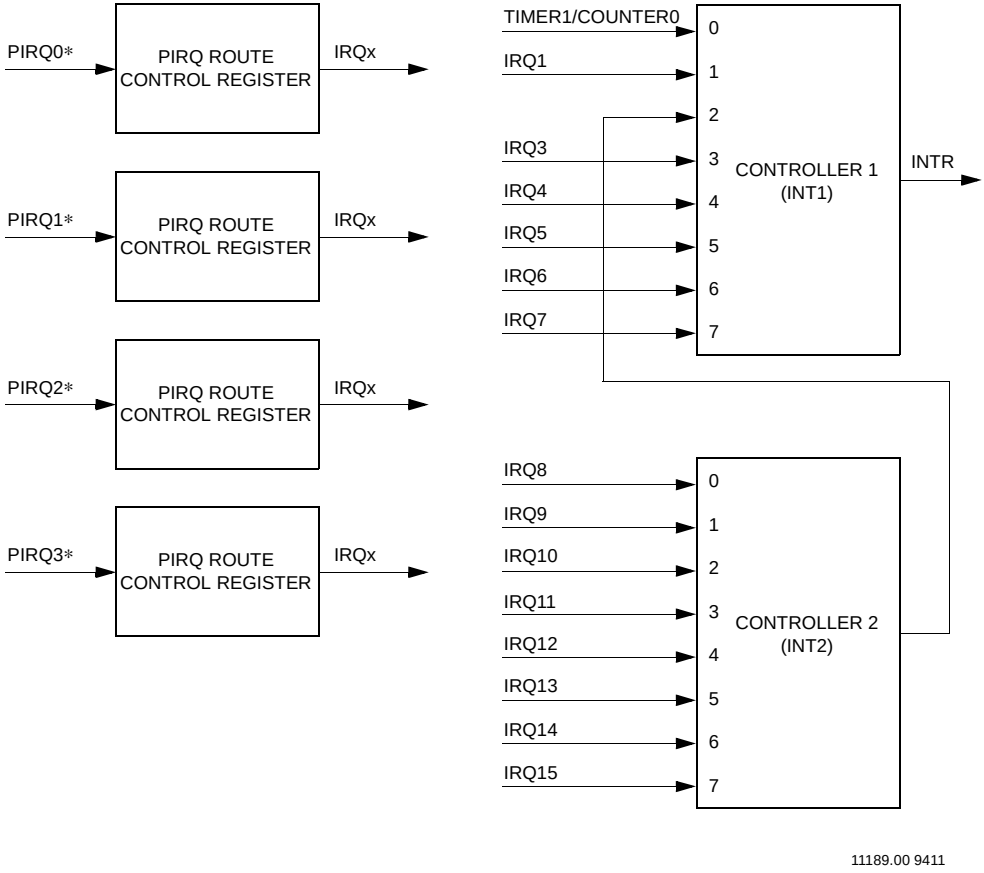


Figure 2-3. IBC Interrupt Handler Block Diagram

VMEchip2 Interrupts

VMEchip2 interrupts consist of interrupts from the VMEbus IRQ lines and from the VMEchip2 internal resources (i.e., DMA and Timers). You can program the VMEchip2 interrupt control registers as though the system were MC68040-based (i.e., with interrupt priority levels from 1 through 7). When an interrupt is pending, the VMEchip2 asserts three encoded interrupt request lines (IPL2∗-IPL0∗) to the VME2PCI device. An interrupt is then issued by the VME2PCI device to the processor through the IBC.

After learning from the IBC that the source of the interrupt is the VME2PCI, the software determines the interrupt level to acknowledge the VMEchip2 by examining the ILVL status bits of the Interrupt Control and Status Register in the VME2PCI ASIC. Finally, to get the interrupt vector from the VMEchip2, the interrupt handling routine must read the appropriate Pseudo IACK Registers.

Z8536 and Z85230 Interrupts

After learning from the IBC that the source of the interrupt is the Z85230/Z8536 devices, the software can either poll the two devices or perform an 8-bit read access to the Z85230/Z8536 Pseudo IACK Register to get the interrupt vector. Refer to the Z85230 and the Z8536 Data Sheets for programming information and additional information about their interrupt structures.

ABT (Abort) Interrupt

The MVME1603/MVME1604 can be programmed to generate an interrupt to the processor via ISA Interrupt IRQ8∗ when the ABORT switch is activated (refer also to the *ABORT Switch* section at the beginning of this chapter). The ABORT∗ signal is also routed to pin PB7 of the Z8536 device. Refer to the 82C378ZB and the Z8536 Data Sheets for programming information.

DMA Channels

The IBC supports seven DMA channels. These DMA channels are allocated as follows:

Table 2-8. IBC DMA Channel Assignments

IBC Priority	IBC Label	Controller	DMA Assignment	DMA Request Polarity
1	Channel 0	DMA1	Serial Port 3 Receiver (Z85230 Port A Rx)	High
2	Channel 1		Serial Port 3 Transmitter (Z85230 Port A Tx)	High
3	Channel 2		Reserved for Floppy Drive Controller	High
4	Channel 3		Parallel Port	High
5	Channel 4	DMA2	Not available - Cascaded from DMA1	N/A
6	Channel 5		Serial Port 4 Receiver (Z85230 Port B Rx)	High
7	Channel 6		Serial Port 4 Transmitter (Z85230 Port B Tx)	High
8	Channel 7		Not Used	High

Sources of Reset

The MVME1603/MVME1604 SBC has six equally powerful potential sources of reset:

1. Power-on reset
2. RESET switch
3. ALT_RST* function controlled by the Port 92 register in the IBC (resets the VMEbus when the MVME1603/MVME1604 is system controller)
4. Keyboard Reset function from the keyboard controller in the ISASIO (ISA Super I/O) device
5. Reset sources from the VMEchip2: the VMEbus SYSRESET*, Watchdog Reset, and Software Reset functions.

6. When the MVME1603/MVME1604 is operating as the VMEbus System Controller, an HRESET* signal will also cause a VMEbus SYSRESET*.

Endian Issues

The MVME1603/MVME1604 supports both little-endian (e.g. Windows NT) and big-endian software (e.g. AIX). The PowerPC processor and the VMEbus are inherently big-endian, while the PCI bus is inherently little-endian. The following figures illustrate how the MVME1603/MVME1604 handles the endian issue in big-endian and little-endian modes:

Processor/Memory Domain

The MPC603/604 processor can operate in both big-endian and little-endian mode. However, it always treats the external processor/memory bus as big-endian by performing *address rearrangement and reordering* when running in little-endian mode.

Role of the MPC105

Because the PCI bus is little-endian, the MPC105 performs byte swapping in both directions (from PCI to memory and from the processor to PCI) to maintain address invariance while programmed to operate in big-endian mode with the processor and the memory subsystem.

In little-endian mode, the MPC105 *reverse-rearranges* the address for PCI-bound accesses and *rearranges* the address for memory-bound accesses (from PCI). In this case, no byte swapping is done.

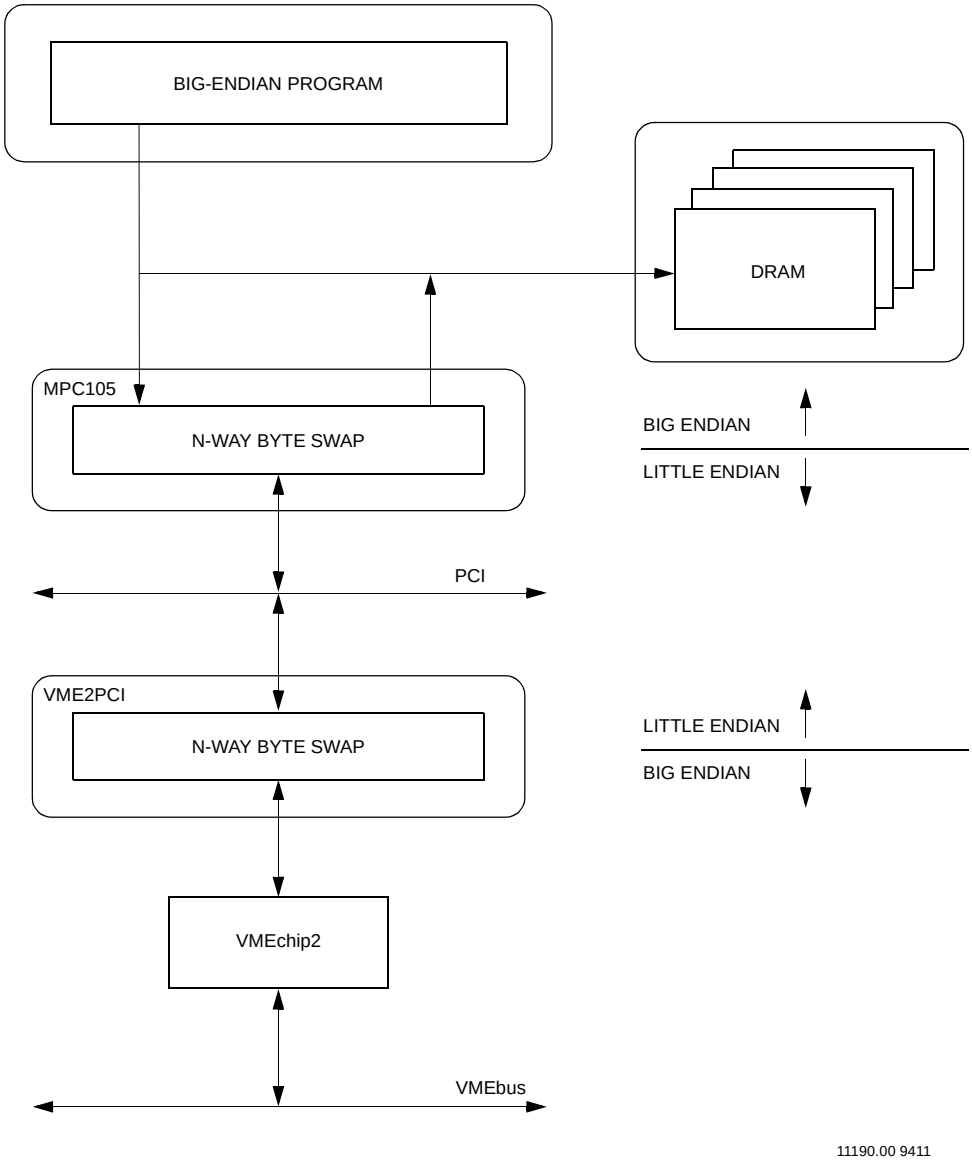


Figure 2-4. Big-Endian Mode

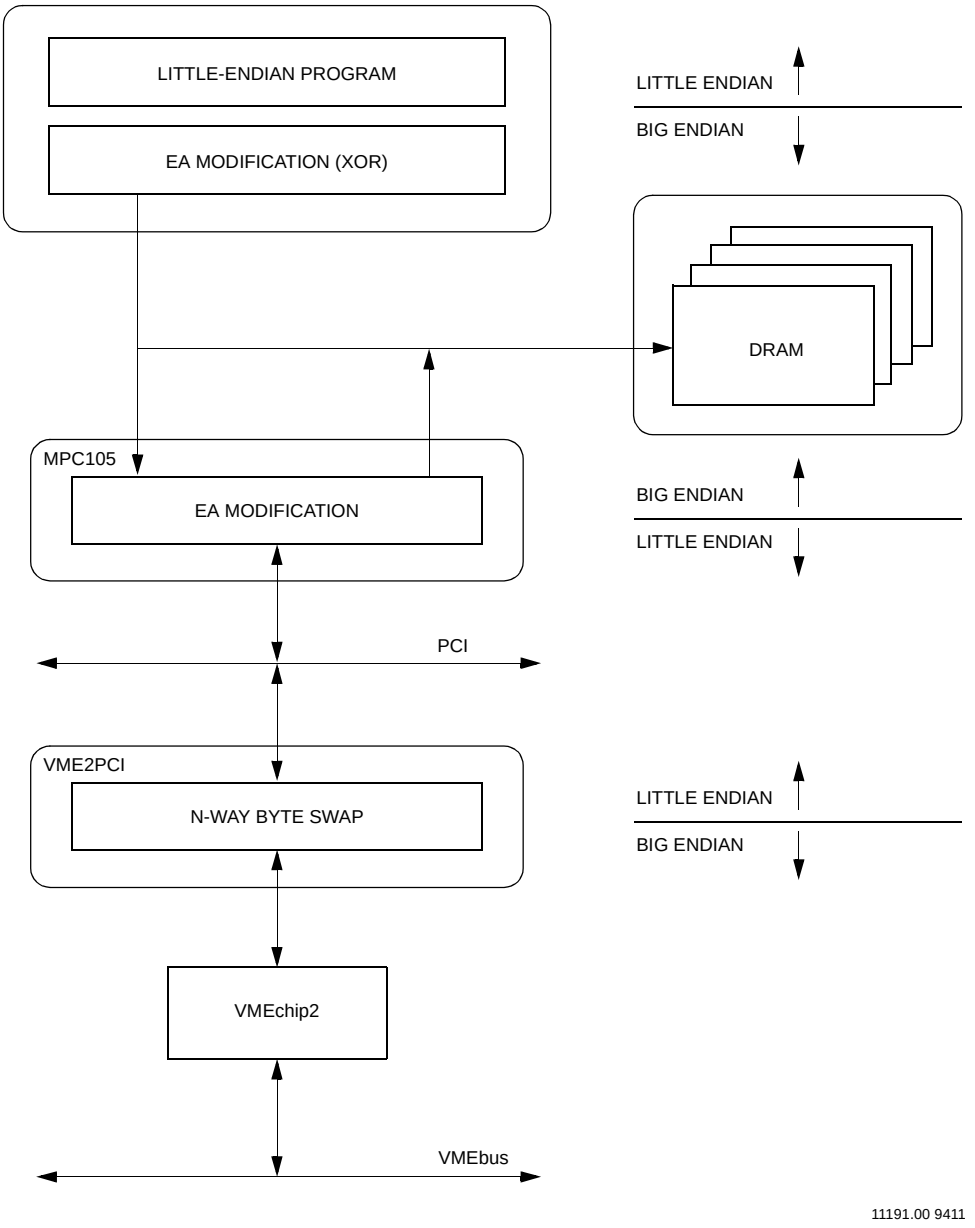


Figure 2-5. Little-Endian Mode

PCI Domain

The PCI bus is inherently little-endian and all devices connected directly to PCI will operate in little-endian mode, regardless of the mode of operation in the processor's domain.

53C825 or 53C810(SCSI)

SCSI is byte-stream-oriented; the byte having the lowest address in memory is the first one to be transferred regardless of the endian mode. Since the MPC105 maintains address invariance in both little-endian and big-endian mode, there should be no endian issues for the SCSI data. Big-endian software must still be aware of the byte-swapping effect when accessing the registers of the 53C825 or 53C810, however.

DEC21040 (Ethernet)

Ethernet is also byte-stream-oriented; the byte having the lowest address in memory is the first one to be transferred regardless of the endian mode. Since the MPC105 maintains address invariance in both little-endian and big-endian mode, there should be no endian issues for the Ethernet data. Big-endian software must still be aware of the byte-swapping effect when accessing the registers of the DEC21040, however.

GD5446 (Graphics)

Big-endian graphic software must take the effects of byte-swapping on big-endian software into account.

Role of the VME2PCI

Because PCI is little-endian and the VMEbus is big-endian, the VME2PCI performs byte swapping in both directions (from PCI to VMEbus and from VMEbus to PCI) to maintain address invariance, regardless of the mode of operation in the processor's domain.

VMEbus Domain

The VMEbus is inherently big-endian. All devices connected directly to the VMEbus are expected to operate in big-endian mode, regardless of the mode of operation in the processor's domain.

In big-endian mode, byte-swapping is performed first by the VME2PCI and then by the MPC105. The result has the desirable effect of being transparent to the big-endian software.

In little-endian mode, however, software must take the byte-swapping effect of the VME2PCI and the address *reverse-rearranging* effect of the MPC105 into account.

Functional Description 3

Introduction

This chapter describes the MVME1603/MVME1604 single-board computer on a block diagram level. The *General Description* provides an overview of the MVME1603/MVME1604, followed by a detailed description of several blocks of circuitry. Figure 3-1 shows a block diagram of the overall board architecture.

Detailed descriptions of other MVME1603/MVME1604 blocks, including programmable registers in the ASICs and peripheral chips, can be found in the *Programmer's Reference Guide* (part number V1600-1A/PG). Refer to it for a functional description of the MVME1603/MVME1604 in greater depth.

Features

The following table summarizes the features of the MVME1600-001- and MVME1600-011-based MVME1603/MVME1604 single-board computers.

Table 3-1. MVME1603/MVME1604 Features

Feature	Description	Models
Microprocessor	MPC603 PowerPC™ processor	MVME1603
	MPC604 PowerPC™ processor	MVME1604 (2 slots)
DRAM	Up to 64MB on processor module	All models
	8MB-64MB on RAM104 module (192MB available as factory order only)	All models
L2 cache memory	(Optional) 256KB on processor module	PM603-02*x*, PM604-01*x*
Boot ROM	Two 32-pin PLCC sockets (1MB Flash)	All models
Software-readable header	8-bit readable header (4 bits reserved for firmware, 4 bits user-definable)	All models

Table 3-1. MVME1603/MVME1604 Features (Continued)

Feature	Description	Models
Real-time clock	8KB NVRAM with RTC and battery backup (SGS-Thomson M48T18)	All models
Switches	RESET and ABORT	All models
Status LEDs	Six: CHS, BFL, CPU, PCI, FUS, and SYS	All models
Tick timers	Four programmable 16-bit timers (one in S82378ZB ISA bridge; three in Z8536 CIO device)	All models
Watchdog timer	Provided in VMEchip2	All models
Interrupts	Eight software interrupts	All models
VME I/O	VMEbus P2 connector	All models
Serial I/O	2 async ports, 2 sync/async ports via P2 and MVME760 transition module (async: PC87303 SIO; sync: Zilog 85230 ESCC)	MVME1600-001 base board
	2 async ports via P2 and MVME712M transition module; 2 sync/async ports via P2 and MVME712M or front panel	MVME1600-011 base board
Parallel I/O	IEEE1284 Bidirectional parallel port (PC87303 SIO) via P2 and transition module	All models
SCSI I/O	16-bit SCSI interface (NCR 53C825) via front panel	MVME1600-001 base board
	8-bit SCSI interface (NCR 53C810) via P2 and MVME712M transition module	MVME1600-011 base board
Ethernet I/O	AUI and 10BaseT connections via P2 and MVME760 transition module	MVME1600-001 base board
	AUI connection via P2 and MVME712M transition module; 10BaseT connection via front panel	MVME1600-011 base board
PCI interface	One IEEE P1386.1 PCI Mezzanine Card (PMC) slot	All models
Keyboard/mouse interface	Support for keyboard and mouse input (PC87303 SIO) via front panel	MVME1600-001 base board
Graphics port	Super VGA high-resolution color graphics (CL-GD5446 graphics accelerator)	MVME1600-001 base board

Table 3-1. MVME1603/MVME1604 Features (Continued)

Feature	Description	Models
Floppy disk controller	Support for floppy disk drive (PC87303 SIO) via connectors on base board	All models
VMEbus interface	VMEbus system controller functions	All models
	VMEbus-to-local-bus interface (A24/A32, D8/D16/D32/block transfer [D8/D16/D32/D64])	
	Local-bus-to-VMEbus interface (A16/A24/A32, D8/D16/D32)	
	VMEbus interrupter	
	VMEbus interrupt handler	
	Global CSR for interprocessor communications	
	DMA for fast local memory/VMEbus transfers (A16/A24/A32, D16/D32/D64)	

General Description

The MVME1603/1604 is a VMEmodule single-board computer equipped with a PowerPC™ Series microprocessor. The MVME1603 is equipped with a PowerPC 603 microprocessor; the MVME1604 has a PowerPC 604. 256KB L2 cache memory is available as an option on certain models of the MVME1603 and the MVME1604.

The MVME1603/1604 family has two parallel branches based on two distinct versions (MVME1600-001 and MVME1600-011) of the base board. The differences between the MVME1600-001 and the MVME1600-011 lie mainly in the area of I/O handling; the logic design is the same for both versions.

As shown in the *Features* section, The MVME1603/MVME1604 offers many standard features desirable in a computer system—such as synchronous and asynchronous serial ports, parallel port, boot ROM and DRAM, SCSI, Ethernet, provision for a disk drive mezzanine, and (MVME1600-001 base board only) keyboard, mouse, and graphics

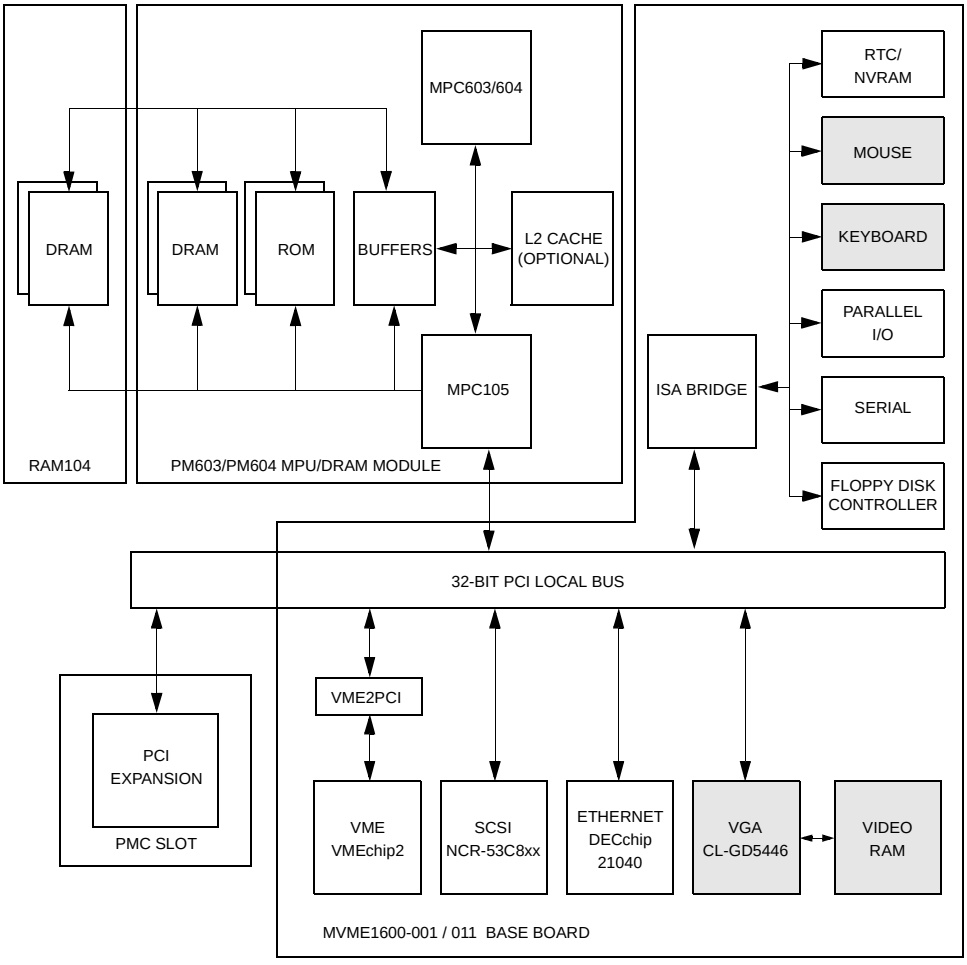
support—in a one- or two-slot VME package. Its flexible mezzanine architecture allows relatively easy upgrades of the processor and/or memory.

A key feature of the MVME1603/MVME1604 family is the PCI (Peripheral Component Interconnect) bus. In addition to the on-board local bus peripherals, the PCI bus supports an industry-standard mezzanine interface, IEEE P1386.1 PMC (PCI Mezzanine Card).

PMC modules offer a variety of possibilities for I/O expansion through FDDI (Fiber Distributed Data Interface), ATM (Asynchronous Transfer Mode), graphics, Ethernet, or SCSI ports. Both base boards support PMC front panel I/O.

Block Diagram

Figure 3-1 is a block diagram of the MVME1603/MVME1604's overall architecture. Shaded areas of the diagram apply to MVME1600-001-based versions only.



NOTES : 1. SHADED BOXES ARE MVME1600-001 FEATURES ONLY.
2. SCSI CONTROLLER IS NCR-53C825 ON MVME1600-001, NCR-53C810 ON -011.

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Figure 3-1. MVME1603/MVME1604 Block Diagram

SCSI Interface

The MVME1603/MVME1604 supports mass storage subsystems through the industry-standard SCSI bus. These subsystems may include hard and floppy disk drives, streaming tape drives, and other mass storage devices. The SCSI interface is implemented using the NCR 53C825 (on the MVME1600-001 base board) or NCR 53C810 (on the MVME1600-011 base board) SCSI I/O controller at a clock speed of 40MHz. The SCSI I/O controller connects directly to the PCI local bus.

The MVME1600-001 base board has an industry-standard 68-pin high-density SCSI connector on the front panel (as illustrated in Figure 1-3).

The MVME1600-011 base board routes its SCSI lines through the P2 connector to the MVME712M transition module (as illustrated in Figure 1-13). The SCSI control lines have filter networks to minimize the effects of VMEbus signal noise at P2.

The SCSI bus is 16 bits wide in MVME1600-001-based versions of the MVME1603/MVME1604, and 8 bits wide in MVME1600-011-based versions. Refer to Chapter 4 for the pin assignments of the MVME1600-001 front panel SCSI connector. Refer to the MVME712M *User's Manual* for the pin assignments of the transition module SCSI connectors used in the MVME1600-011 SCSI implementation. Refer to the NCR 53C825 and 53C810 user's guides and the MVME1603/MVME1604 *Programmer's Reference Guide* for detailed programming information.

SCSI Termination

The individual configuring the system must ensure that the SCSI bus is properly terminated at both ends.

The MVME1600-001 base board provides onboard SCSI bus termination. The terminators can be enabled or disabled by a jumper (J7—described in Chapter 1). If the SCSI bus ends at the MVME1603/MVME1604 module, then SCSI termination must be enabled. +5Vdc power to the SCSI bus TERMPWR signal and termination resistors is supplied through a fuse (F1) and diode.

The MVME1600-011 base board uses the sockets provided for SCSI bus terminators on the P2 adapter board. If the SCSI bus ends at the adapter board, then termination resistors must be installed on the adapter board. +5Vdc power to the SCSI bus TERMPWR signal and termination resistors is supplied through a fuse located on the adapter board.

Ethernet Interface

The MVME1603/MVME1604 uses Digital Equipment's DECchip 21040 LAN controller to implement an Ethernet interface that supports both AUI and 10BaseT connections. The balanced differential transceiver lines for AUI and 10BaseT are coupled via on-board transformers.

The MVME1600-001 base board routes its AUI and 10BaseT lines through the P2 connector to the MVME760 transition module (as illustrated in Figure 1-12 on page 1-41). The MVME760 front panel has an industry-standard DB15 connector and 8-pin RJ45 connector for the AUI and 10BaseT connections respectively (see Figure 1-4 on page 1-17).

The MVME1600-011 base board uses an 8-pin RJ45 on its front panel for 10BaseT lines (see Figure 1-5 on page 1-19) and routes its AUI lines through the P2 connector to the MVME712M transition module (as illustrated in Figure 1-13 on page 1-44). The MVME712M front panel has an industry-standard DB15 connector for the AUI connections (see Figure 1-6 on page 1-28).

Every MVME1603/MVME1604 is assigned an Ethernet station address. The address is $08003E2*xxxxx*, where *xxxxx* is the unique 5-nibble number assigned to the board (i.e., every board has a different value for *xxxxx*).

Each MVME1603/MVME1604 displays its Ethernet station address on a label attached to backplane connector P2. In addition, the six bytes including the Ethernet station address are stored in the NVRAM (BBRAM) configuration area specified by boot ROM. That is, 08003E2*xxxxx* is stored in NVRAM. At an address of $FFFC1F2C, the upper four bytes (08003E2*x*) can be read. At an address of $FFFC1F30, the lower two bytes (*xxxx*) can be read. The MVME1603/MVME1604 debugger, PPCBug, has the capability to retrieve or set the Ethernet station address.

If the data in the NVRAM is lost, use the number on the label on backplane connector P2 to restore it.

Refer to Chapter 4 for the pin assignments of the MVME1600-011 front panel 10BaseT connector. Refer to the MVME712M *User's Manual* for the pin assignments of the transition module AUI connector. Refer to the MVME760 *User's Manual* for the pin assignments of the transition module AUI and 10BaseT connectors used in the MVME1600-001 Ethernet implementation. Refer to the BBRAM/TOD Clock memory map description in the MVME1603/MVME1604 *Programmer's Reference Guide* for detailed programming information.

Note The MVME1603/MVME1604 will support either AUI or 10BaseT Ethernet connections, but not both at the same time. To switch from one type to the other, do the following:

1. Bring the MVME1603/MVME1604 up in PPCBug.
2. Remove the current Ethernet cable and connect the one you wish to use.
3. Reset the MVME1603/MVME1604 by pressing the RESET switch or typing the debug command **RESET**.

The new connection is automatically recognized by the LAN controller.

Graphics Interface

MVME1600-001-based versions of the MVME1603/MVME1604 have a Super VGA (Video Graphics Array) color graphics interface implemented with a Cirrus Logic CL-GD5446 graphics accelerator. The CL-GD5446 supports pixel clock rates of up to 110MHz. Its internal palette DAC is configurable for industry-standard 16- or 256-color VGA modes. The DAC is also extensible to high- and true-color modes of 32 thousand or 16.7 million colors.

Depending on the color selection and bits-per-pixel mode, the CL-GD5446 device supports resolutions of up to 1280 x 1024. 2MB of video buffer memory (in the form of four 256K x 16, 40-pin SOJ, 60ns DRAM chips) are available to the CL-GD5446.

The VGA port routes the graphics data to an industry-standard 3-row DB15 connector on the front panel of the MVME1600-001 base board (as illustrated in Figure 1-3).

Refer to Chapter 4 for the pin assignments of the MVME1600-001 front panel VGA connector. Refer to Cirrus Logic's CL-GD5446 *Technical Reference Manual* for detailed programming information.

PCI Mezzanine Interface

A key feature of the MVME1603/MVME1604 family is the PCI (Peripheral Component Interconnect) bus. In addition to the on-board local bus devices (SCSI, Ethernet, graphics, etc.), the PCI bus supports an industry-standard mezzanine interface, IEEE P1386.1 PMC (PCI Mezzanine Card).

PMC modules offer a variety of possibilities for I/O expansion through FDDI (Fiber Distributed Data Interface), ATM (Asynchronous Transfer Mode), graphics, Ethernet, or SCSI ports. Both versions of the base board support PCI front panel I/O.

The MVME1603/MVME1604 supports one PMC slot. Two 64-pin connectors on the base board (J11 and J12) interface with 32-bit IEEE P1386.1 PMC-compatible mezzanines to add any desirable function. The PCI Mezzanine Card slot has the following characteristics:

Mezzanine Type	PMC (PCI Mezzanine Card)
Mezzanine Size	S1B: Single width, standard depth (75mm x 150mm) with front panel
PMC Connectors	J11 and J12 (32-Bit PCI with front-panel I/O only)
Signaling Voltage	V_{io} = 5.0Vdc

Refer to Chapter 4 for the pin assignments of the PMC connectors. For detailed programming information, refer to the PCI bus descriptions in the MVME1603/MVME1604 *Programmer's Reference Guide* and to the user documentation for the PMC modules you intend to use.

VMEbus Interface

The VMEchip2 ASIC, in tandem with the VME2PCI ASIC, constitutes the VMEbus interface. The VMEchip2 interfaces an MC68040-style local bus to the VMEbus. The VME2PCI interfaces the PCI bus to an MC68040-style local bus. When the VMEchip2 and the VME2PCI chips are used together, they form a PCI-bus-to-VMEbus interface.

The VMEchip2/VME2PCI combination provides:

- The local-bus-to-VMEbus interface
- The VMEbus-to-local-bus interface
- The DMA controller functions of the local VMEbus

The VMEchip2 includes Global Control and Status Registers (GCSRs) for interprocessor communications. It can provide the VMEbus system controller functions as well. For detailed programming information, refer to the VMEchip2 and VME2PCI discussions in the MVME1603/MVME1604 *Programmer's Reference Guide.*

ISA Super I/O Device (ISASIO)

The MVME1603/MVME1604 uses a PC87303 ISASIO chip from National Semiconductor to implement certain segments of the P2 and front-panel I/O:

- Two asynchronous serial ports (COM1 and COM2) via P2 and transition module
- IEEE1284 bidirectional parallel port via P2 and transition module
- Disk drive support via drive connector J6 and power connector J16 (on the MVME1600-001) or J19 (on the MVME1600-011)
- Keyboard and mouse interface (MVME1600-001 base board only)

Asynchronous Serial Ports

The two asynchronous ports provided by the ISASIO device employ TTL-level signals that are routed to the P2 connector. The TTL output lines are buffered through TTL drivers and series resistors. The EIA-232-D drivers and receivers that complete the serial interface are located on the MVME760 (for the MVME1600-001 base board) or MVME712M (for the MVME1600-011 base board) transition module.

Hardware initializes the two serial ports as COM1 and COM2 with ISA I/O base addresses of $3F8 and $2F8 respectively. This default configuration also assigns COM1 to IBC (ISA/PCI Bridge Controller) interrupt request line IRQ4 and COM2 to IRQ3. You can change the default configuration by reprogramming the ISASIO device. For detailed programming information, refer to the PCI and ISA bus discussions in the MVME1603/MVME1604 *Programmer's Reference Guide* and to the vendor documentation for the ISASIO device.

Parallel Port

The parallel port is an IEEE P1284 printer interface implemented with the ISASIO device. All parallel I/O interface signals are routed to P2 through series damping resistors.

Hardware initializes the parallel port as PPT1 with an ISA IO base address of $3BC. This default configuration also assigns the parallel port to IBC (ISA/PCI Bridge Controller) interrupt request line IRQ7. You can change the default configuration by reprogramming the ISASIO device. For detailed programming information, refer to the PCI and ISA bus discussions in the MVME1603/MVME1604 *Programmer's Reference Guide* and to the vendor documentation for the ISASIO device.

Disk Drive Controller

The ISASIO device incorporates a low- and high-density disk drive controller for use with an optional disk drive. The disk drive may take the form of a mezzanine board or a separate module. The drive interfaces with the ISASIO controller via base board connector J6. The unit receives power via connector J16 (on the MVME1600-001) or J19 (on the MVME1600-011).

The ISASIO disk drive controller is compatible with the DP8473, 765A, and N82077 devices commonly used to implement floppy disk controllers. Software written for those devices may be used without change to operate the ISASIO controller. The ISASIO device may be used to support any of the following devices:

- 3½-inch 1.44MB floppy disk drive
- 5¼-inch 1.2MB floppy disk drive
- Standard 250kbps to 2Mbps tape drive system

Keyboard and Mouse Interface

On the MVME1600-001 base board, the ISASIO device provides ROM-based keyboard and mouse interface control. The front panel of the MVME1600-001 board has two 6-pin circular DIN connectors for keyboard and the mouse connections.

ISA Bridge Controller

The MVME1603/MVME1604 uses an Intel S82378ZB bridge controller to supply the interface between the PCI local bus and the ISA system I/O bus (diagrammed in Figure 1-1 and Figure 1-2 for the two base boards).

The ISA bridge controller provides the following functions:

- PCI bus arbitration for:
  - The MPC105 (PCI/MPU bus bridge and memory controller)
  - The SCSI controller
  - the Ethernet controller
  - The VME2PCI ASIC
  - The PMC (PCI Mezzanine Card) slot
- ISA bus arbitration for DMA devices
- ISA interrupt mapping for four PCI interrupts
- Interrupt controller functionality to support 14 ISA interrupts
- Edge/level control for ISA interrupts
- Seven independently programmable DMA channels
- One 16-bit timer
- Three interval counters/timers

The base address of the configuration space for the ISA bridge controller is at $00800800 in the PCI Configuration area.

Real-Time Clock and NVRAM

The MVME1603/MVME1604 employs an SGS-Thomson surface-mount M48T18 RAM and clock chip to provide 8KB of non-volatile static RAM and a real-time clock. This chip provides a clock, oscillator, crystal, power failure detection, memory write protection, 8KB of NVRAM, and a battery in a package consisting of two parts:

- A 28-pin 330mil SO device containing the real-time clock, the oscillator, power failure detection circuitry, 8KB of SRAM, and gold-plated sockets for a SNAPHAT battery
- A SNAPHAT battery housing a crystal along with the battery

The SNAPHAT battery package is mounted on top of the MT48T18 device. The battery housing is keyed to prevent reverse insertion.

The clock furnishes seconds, minutes, hours, day, date, month, and year in BCD 24-hour format. Corrections for 28-, 29- (leap year), and 30-day months are made automatically. The clock generates no interrupts. Although the M48T18 is an 8-bit device, 8-, 16-, and 32-bit accesses from the ISA bus to the M48T18 are supported. Refer to the MVME1603/MVME1604 *Programmer's Reference Guide* and to the M48T18 data sheet for detailed programming and battery life information.

Programmable Timers

Among the resources available to the local processor are a number of programmable timers. Timers are incorporated into the ISA bridge controller, the Z8536 CIO device (diagrammed in Figure 1-1 and Figure 1-2 for the two base boards), and the VMEchip2. They can be programmed to generate periodic interrupts to the processor.

Interval Timers

The ISA bridge controller has three built-in counters that are equivalent to those found in an 82C54 programmable interval timer. These counters are grouped into one timer unit, Timer 1, in the IBC. Each counter output has a specific function:

- Counter 0 is associated with interrupt request line IRQ0. It can be used for system timing functions, such as timer interrupt for a time-of-day.
- Counter 1 generates a refresh request signal for ISA memory. This timer is not used in the MVME1603/MVME1604.
- Counter 2 provides the tone for the speaker output function on the ISA bridge controller (the SPEAKER_OUT signal which can be cabled to an external speaker via the remote reset connector).

The interval timers use the OSC clock input as their clock source. The MVME1603/MVME1604 module drives the OSC pin with a 14.31818 MHz clock source.

16-Bit Timers

Four 16-bit timers are available on the MVME1603/MVME1604. The ISA bridge controller supplies one 16-bit timer; the Z8536 CIO device provides the other three. For information on programming these timers, refer to the data sheets for the S82378ZB ISA bridge controller and the Z8536 CIO device.

VMEchip2 Timers

Two 32-bit programmable tick timers are available in the optional VMEchip2 ASIC. Refer to the VMEchip2 description in the MVME1603/MVME1604 *Programmer's Reference Guide* for detailed programming information.

Note It is advisable to avoid using these timers for system timing functions, since the VMEchip2 may not be present in all versions of the MVME1603/MVME1604 module.

Serial Communications Interface

The MVME1603/MVME1604 uses a Zilog Z85230 ESCC (Enhanced Serial Communications Controller) to implement the two synchronous/asynchronous serial communications interfaces, which are routed through P2 for the MVME1600-001 base board and through the front panel for the MVME1600-011 base board. The Z85230 supports synchronous (SDLC/HDLC) and asynchronous protocols. The MVME1603/MVME1604 hardware supports asynchronous serial baud rates of 110B/s to 38.4KB/s.

Each interface supports the CTS, DCD, RTS, and DTR control signals as well as the TxD and RxD transmit/receive data signals, and TxC/RxC synchronous clock signals. Since not all modem control lines are available in the Z85230, a Z8536 CIO is used to provide the missing modem lines.

In the MVME1600-001 base board, all modem control lines from the ESCC are multiplexed/demultiplexed through P2 by a multiplexing function (P2MX, described later in this chapter) due to the pin limitations of the P2 connector.

A PAL device performs decoding of register accesses and pseudo interrupt acknowledge cycles for the Z85230 and the Z8536 in ISA I/O space. The ISA bridge controller supplies DMA support for the Z85230.

The Z85230 receives a 10MHz clock input. The Z85230 supplies an interrupt vector during pseudo interrupt acknowledge cycles. The vector is modified within the Z85230 according to the interrupt source. Interrupt request levels are programmed via the ISA bridge controller. Refer to the Z85230 data sheet and to the MVME1603/ MVME1604 *Programmer's Reference Guide* for further information.

Z8536 CIO Device

The Z8536 CIO device complements the Z85230 ESCC by supplying signals for Abort interrupt status, fuse status, and SCSI terminator status and control, as well as furnishing modem control lines not provided by the Z85230 ESCC. In addition, the Z8536 CIO device has three independent 16-bit counters/timers.

For MVME1600-001 base boards, the Z8536 CIO device also provides a means of requesting the module ID of the two synchronous/asynchronous serial ports that reside on the MVME760 transition module. Refer to the Z8536 data sheet and to the MVME1603/MVME1604 *Programmer's Reference Guide* for further information.

Board Configuration Register

The Board Configuration Register is an 8-bit read-only register containing the details of the MVME1603/MVME1604 single-board computer's configuration. This register is located on the base board at ISA I/O address $0802.

Board Configuration Register - $0802								
BIT	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0

Board Configuration Register - $0802								
FIELD	GIOP*	SCCP*		PMCP*	VMEP*	GFXP*	LANP*	SCSIP*
OPER	R	R	R	R	R	R	R	R
RESET	N/A	N/A	1	N/A	N/A	N/A	N/A	N/A

GIOP* Transition module present. If set, the MVME760 transition module is not connected. If cleared, the MVME760 module is connected. (MVME1600-001 base boards only; not applicable to MVME1600-011 boards.)

SCCP* Z85230 ESCC present. If set, there is no on-board synchronous serial support (the ESCC not present). If cleared, the Z85230 ESCC is installed and there is on-board support for synchronous serial communication.

PMCP* PMC present. If set, no PCI mezzanine card is installed in the PMC slot. If cleared, the PMC slot contains a PCI mezzanine card.

VMEP* VMEbus present. If set, there is no VMEbus interface. If cleared, the VMEbus interface is supported.

GFXP* Graphics present. If set, no graphics interface is installed. If cleared, onboard graphics are available (MVME1600-001 base board only; the MVME1600-011 has no graphics capability).

LANP* Ethernet present. If set, no Ethernet transceiver interface is installed. If cleared, there is on-board Ethernet support.

SCSIP* SCSI present. If set, there is no on-board SCSI interface. If cleared, on-board SCSI is supported.

P2 Signal Multiplexing

Due to the limited availability of pins in the P2 backplane connector, the MVME1600-001 base board multiplexes and demultiplexes certain synchronous I/O control signals that pass between the base board and the MVME760 transition module. This is a hardware function that is entirely transparent to software.

Four signals are involved in the P2 multiplexing function: MXDO, MXDI, MXCLK, and MXSYNC*.

MXDO is a time-multiplexed data output line from the main board and MXDI is a time-multiplexed line from the MVME760 module. MXCLK is a 10MHz bit clock for the MXDO and MXDI data lines. MXSYNC* is asserted for one bit time at time slot 15 (refer to the following table) by the MVME1600-001 base board. The MVME760 transition module uses MXSYNC* to synchronize with the base board.

A 16-to-1 multiplexing scheme is used with MXCLK's 10MHz bit rate. Sixteen time slots are defined and allocated as follows:

Table 3-2. P2 Multiplexing Sequence

MXDO (From Base Board)		MXDI (From MVME760)	
Time Slot	**Signal Name**	**Time Slot**	**Signal Name**
0	RTS3	0	CTS3
1	DTR3	1	DSR3/MID1
2	LLB3/MODSEL	2	DCD3
3	RLB3	3	TM3/MID0
4	RTS4	4	RI3
5	DTR4	5	CTS4
6	LLB4	6	DSR4/MID3
7	RLB4	7	DCD4
8	IDREQ*	8	TM4/MID2
9	Reserved	9	RI4
10	Reserved	10	LANPWR
11	Reserved	11	Reserved
12	Reserved	12	Reserved
13	Reserved	13	Reserved
14	Reserved	14	Reserved
15	Reserved	15	GENIO_PRESENT*

ABORT Switch (S1)

The ABORT switch is located on the LED mezzanine. When activated by software, the ABORT switch can generate an interrupt signal from the base board to the processor at a user-programmable level. The interrupt is normally used to abort program execution and return control to the PPCBug debugger firmware located in the MVME1603/1604 EPROM and Flash memory. The interrupt signal reaches the processor module via ISA bus interrupt line IRQ8∗ . The signal is also available at pin PB7 of the Z8536 CIO device, which handles various status signals, serial I/O lines, and counters.

The interrupter connected to the ABORT switch is an edge-sensitive circuit, filtered to remove switch bounce.

RESET Switch (S2)

The RESET switch is located on the LED mezzanine. The RESET switch resets all onboard devices; it also drives a SYSRESET* signal if the MVME1603/1604 is the system controller. The RESET switch may be disabled by software.

The VMEchip2 includes both a global and a local reset driver. When the VMEchip2 operates as the VMEbus system controller, the reset driver provides a global system reset by asserting the VMEbus signal SYSRESET*. A SYSRESET* signal may be generated by the RESET switch, a power-up reset, a watchdog timeout, or by a control bit in the LCSR in the VMEchip2. SYSRESET* remains asserted for at least 200 ms, as required by the VMEbus specification.

Similarly, the VMEchip2 provides an input signal and a control bit to initiate a local reset operation. By setting a control bit, software can maintain a board in a reset state, disabling a faulty board from participating in normal system operation. The local reset driver is enabled even when the VMEchip2 is not the system controller. A local reset may be generated by the RESET switch, a power-up reset, a watchdog timeout, a VMEbus SYSRESET* signal, or a control bit in the GCSR.

Note For an MVME1603/1604 without the VMEbus option (i.e., with no VMEchip2), the LCSR control bit is not available to reset the module. In this case, the watchdog timer is allowed to time out to reset the MVME1603/1604.

Front Panel Indicators (DS1 - DS6)

There are six LEDs on the MVME1603/1604 front panel: CHS, BFL, CPU, PCI, FUS, and SYS.

- CHS (DS1, yellow). Checkstop; driven by the MPC603/604 status lines on the MVME1603/1604. Lights when a halt condition from the processor is detected.
- BFL (DS2, yellow). Board Failure; lights when the BRDFAIL* signal line is active.
- CPU (DS3, green). CPU activity; lights when the DBB* (Data Bus Busy) signal line on the processor bus is active.
- PCI (DS4, green). PCI activity; lights when the IRDY* (Initiator Ready) signal line on the PCI bus is active. This indicates that the PCI mezzanine (if installed) is active.
- FUS (DS5, green). Fuse OK; lights when +5Vdc, +12Vdc, and –12Vdc power is available from the base board to the transition module and remote devices.

Note The circuitry monitored by the FUS LED differs between the MVME1600-001 and MVME1600-011 versions of the base board. The differences are detailed under the respective base board descriptions in Chapter 1.

Because the FUS LED monitors the status of several voltages on the MVME1600-001, it does not directly indicate the condition of any single fuse. If the LED flickers or goes out, check all the fuses (polyswitches).

- SYS (DS6, green). System Controller; lights when the VMEchip2 in the MVME1603/1604 is the VMEbus system controller.

Polyswitches (Resettable Fuses)

The MVME1600-001 and MVME1600-011 base boards draw fused +5Vdc, +12Vdc, and –12Vdc power from the VMEbus backplane through connectors P1 and P2. The 3.3Vdc power (used by the ISA Super I/O device on the base board, and by the PM603 or PM604 processor/memory mezzanine) is derived on-board from the +5Vdc. The following table lists the fuses with the voltages they protect on the respective base boards.

Table 3-3. Fuse Assignments by Base Board

Fuse	MVME1600-001	MVME1600-011
F1	+5Vdc (SCSI)	+5Vdc
F2	–12Vdc	+12Vdc
F3	+5Vdc	
F4	+12Vdc	

MVME1600-001 Base Board

The MVME1600-001 base board furnishes +12Vdc, –12Vdc, and +5Vdc power to the MVME760 transition module through polyswitches (resettable fuses) F4, F2, and F3. The MVME760 uses these voltage sources to power the serial port drivers and any LAN transceivers connected to the transition module. The FUS LED (DS5) on the MVME1600-001 front panel illuminates when all three voltages are available.

The fused +5Vdc power is also supplied to the base board's keyboard and mouse connectors and to the 14-pin combined LED-mezzanine/remote-reset connector, J1.

In addition, the MVME1600-001 base board provides +5Vdc to the SCSI bus TERMPWR signal through fuse F1, located near the front panel SCSI connector. The FUS LED (DS5) on the front panel monitors the SCSI bus TERMPWR signal along with the other operating voltages; when the MVME1600-001 is connected to an SCSI bus, either directly or via the MVME760 module, SCSI terminator power helps illuminate the FUS LED.

Note Because any device on the SCSI bus can provide TERMPWR, and because the FUS LED monitors the status of several voltages, the LED does not directly indicate the condition of any single fuse. If the LED flickers or goes out, check all the fuses (polyswitches).

MVME1600-011 Base Board

The MVME1600-011 base board provides +5Vdc power to the remote LED/switch connector (J4) through a 1A fuse (F1) located between P1 and P2. (J4 provides a separate connection point for a remote control and indicator panel, making it unnecessary to share the LED mezzanine connector for that purpose.) If none of the LEDs light and the ABORT and RESET switches do not operate, check fuse F1.

The MVME1600-011 base board provides +12Vdc power to the Ethernet transceiver interface through a 1A fuse (F2) located between P1 and P2. The FUS LED lights to indicate that +12Vdc is available. With the MVME712M transition module connected, the yellow DS1 LED on the MVME712M also signals the availability of LAN power, indicating in turn that the fuse is good. If the Ethernet transceiver fails to operate, check fuse F2.

The MVME1600-011 base board supplies SCSI terminator power through a 1A fuse (F1) located on the P2 adapter board. If the fuse is blown, the SCSI device(s) may function erratically or not at all. With the P2 adapter board cabled to an MVME712M and with an SCSI bus connected to the MVME712M, the green DS2 LED on the MVME712M illuminates when SCSI terminator power is available. If the DS2 LED flickers during SCSI bus operation, check fuse F1 on the P2 adapter board.

Speaker Control

The MVME1600-001 base board supplies a SPEAKER_OUT signal to the 14-pin combined LED-mezzanine/remote-reset connector, J1. When J1 is used as a remote reset connector with the LED mezzanine removed, the SPEAKER_OUT signal can be cabled to an external speaker to obtain a beep tone. For the pin assignments of J1, refer to Table 1-2.

Like the MVME1600-001 base board, the MVME1600-011 supplies a SPEAKER_OUT signal to the 14-pin LED mezzanine connector, J1. Unlike the MVME1600-001 base board, the MVME1600-011 also applies the SPEAKER_OUT signal to its dedicated remote status and control connector, J4. The LED mezzanine need not be removed to cable the SPEAKER_OUT signal to an external speaker. For the pin assignments of J4, refer to Table 1-3.

PM603/604 Processor/Memory Mezzanine Module

The PM603 or PM604 is the processor/memory mezzanine module that (together with an LED mezzanine, an optional RAM104 DRAM module, and an optional PCI mezzanine card) plugs into the MVME1600-001 or MVME1600-011 base board to make a complete single-board computer. See Figure 1-10.

You have the choice of a PowerPC603™ module (the PM603) or a PowerPC604™ module (the PM604) with from 8MB to 64MB of DRAM, or up to 128MB of DRAM with a RAM104. 256KB of L2 cache is available as an option. There is no parity or ECC protection on the DRAM.

The PowerPC603 is a 64-bit processor with 16KB or 32KB on-chip cache (8KB/16KB data cache and 8KB/16KB instruction cache). The PowerPC604 is a 64-bit processor with 32 KB on-chip cache (16KB data cache and 16KB instruction cache).

The MPC105 bridge/memory controller located on the processor/memory mezzanine provides the bridge between the PowerPC microprocessor bus and the PCI local bus. The memory is kept on the processor bus to get the optimum performance from the designs. Electrically, the processor/memory module is a PCI connection.

MPC604 boards have double-wide front panels to accommodate a heat sink on the PowerPC604 that protrudes into the adjacent VME slot.

The PM603/PM604 module accommodates additional memory. RAM104 modules of 8, 16, 32, or 64MB DRAM are available for memory expansion.

A 192MB memory module is available for the PM604 module as a factory-installed option.

The processor module has sockets for 1MB of Flash memory. The onboard monitor/debugger, PPCBug, resides in the Flash chips. PPCBug provides:

- A boot loader and extensive onboard diagnostics
- A single-line assembler/disassembler
- The capability to save and restore a configuration through NVRAM
- A remote boot capability

Under normal operation, the Flash devices are in “read-only” mode, their contents are pre-defined, and they are protected against inadvertent writes due to loss of power conditions. However, for programming purposes, programming voltage is always supplied to the devices and the Flash contents may be modified by executing the proper program command sequence. Refer to the third-party data sheet for further device-specific information and/or to the PFLASH PPCBug command.

Flash device speed is 150 ns. For this speed, software must not program ROMFAL (first access length) and ROMNAL (last access length) in the MPC105 device with values lower than the following minimum values for various processor external clock frequencies (hardware does not support the burst for which NAL is used):

Table 3-4. Minimum ROMFAL and ROMNAL Values

Processor External Bus Speed	ROMFAL Minimum Value	ROMNAL Minimum Value	8-Bit Access Times (Number of Clocks)	64-Bit Single/Burst Access Times (Number of Clocks)
25 MHz	1	1	4	32/32-32-32-32
33 MHz	2	2	5	40/40-40-40-40
40 MHz	3	3	6	48/48-48-48-48
50 Mhz	5	5	8	64/64-64-64-64
66 MHz	7	7	10	80/80-80-80-80

RAM104 Memory Module

The RAM104 is the optional DRAM memory mezzanine module that (together with a PM603 or PM604 processor/memory mezzanine, an LED mezzanine, and an optional PCI mezzanine card) plugs into the base board to make a complete MVME1603 or MVME1604 single-board computer. See Figure 1-11.

RAM104 modules of 8, 16, 32, or 64MB are available for memory expansion. There is no parity or ECC protection on the DRAM.

The addition of the memory module on the processor/memory module makes a stack three boards high. An MVME1603 SBC maintains a single VME slot width with this stacking, although it does brush the inter-card buffer zone. MVME1604 SBCs have a heatsink on the PowerPC604 that extends well into the adjacent VME slot, so MVME604 boards have double-wide front panels.

MVME760 Transition Module

The MVME760 transition module (Figure 1-4) is used in conjunction with the MVME1600-001 base board. The features of the MVME760 include:

- A parallel printer port
- An Ethernet interface supporting both AUI and 10BaseT connections
- Two EIA-232-D asynchronous serial ports (identified as COM1 and COM2 on the front panel)
- Two synchronous serial ports (ports 3 and 4)

Serial Interface Modules

The synchronous serial ports on the MVME760 are configurable via serial interface modules (SIMs), used in conjunction with the appropriate jumper settings. The SIMs are small plug-in printed circuit boards which contain all the circuitry needed to convert a TTL-level port to the standard voltage levels needed by various industry-standard serial interfaces, such as EIA-232, EIA-530, etc. The following types of SIMs are available:

Table 3-5. Module Type Identification

Model Number	Module Type	Part Number
SIM705-001	EIA-232 DCE	01-W3876B*xx*
SIM705-002	EIA-232 DTE	01-W3877B*xx*
SIM705-003	EIA-530 DCE	01-W3878B*xx*
SIM705-004	EIA-530 DTE	01-W3879B*xx*

For additional information about serial interface modules, refer to the MVME760 *User's Manual* (part number VME760A/UM) and to the SIM705 *Installation Guide* (part number SIM705A/IH).

MVME712M Transition Module

The MVME712M transition module (Figure 1-6) and P2 adapter board are used in conjunction with the MVME1600-011 base board. The features of the MVME712M include:

- A parallel printer port (through the P2 adapter)
- An Ethernet interface supporting AUI connections (through the P2 adapter)
- Four EIA-232-D multiprotocol serial ports (through the P2 adapter)
- An SCSI interface (through the P2 adapter) for connection to both internal and external devices
- Socket-mounted SCSI terminating resistors for end-of-cable or middle-of-cable configurations
- Provision for modem connection
- Green LED for SCSI terminator power; yellow LED for Ethernet transceiver power

The features of the P2 adapter board include:

- A 50-pin connector for SCSI cabling to the MVME712M and/or to other SCSI devices
- Socket-mounted SCSI terminating resistors for end-of-cable or middle-of-cable configurations
- Fused SCSI teminator power developed from the +5Vdc present at connector P2
- A 64-pin DIN connector to interface the EIA-232-D, parallel, SCSI, and Ethernet signals to the MVME712M

Connector Pin Assignments

4

This chapter summarizes the pin assignments for the following groups of interconnect signals for the MVME1603/MVME1604:

- Connectors with pin assignments common to both the MVME1600-001 and MVME1600-011 base boards

Connector	Table
LED Mezzanine connector	4-1
MPU Mezzanine connector	4-2
CPU connector	4-3
DRAM Mezzanine connectors	4-4, 4-5
PCI Mezzanine connector	4-6
VMEbus connector P1	4-7
Ethernet 10BaseT connector	4-8
Disk Drive connector	4-9

- Connectors with pin assignments specific to the MVME1600-001 base board

Connector	Table
VMEbus P2 connector	4-10
SCSI connector	4-11
Graphics connector	4-12
Keyboard and Mouse connectors	4-13, 4-14
Ethernet AUI connector (MVME760)	4-15
Parallel I/O connector(MVME760)	4-16
Serial Ports 1 and 2 (MVME760)	4-17
Serial Ports 3 and 4 (MVME760)	4-18

- Connectors with pin assignments specific to the MVME1600-011 base board

Connector	Table
VMEbus P2 connector	4-19
SCSI connector (at MVME712M)	4-20
Ethernet AUI connector	4-21
Parallel I/O connector	4-22
Serial Ports 1-4 (at MVME712M)	4-23
Serial Ports 3 and 4 (at front panel)	4-24

The following tables furnish pin assignments only. For detailed descriptions of the various interconnect signals, consult the support information documentation package for the MVME1603/ MVME1604 SBC or the support information sections of the MVME760 or MVME712M transition module documentation as necessary.

Common Connectors

The following tables describe connectors used with the same pin assignments by both the MVME1600-001 and the MVME1600-011 base boards.

LED Mezzanine Connector

A 16-pin connector (J1 on the base board) supplies the interface between the base board and the LED mezzanine module. On the base board, this connector is a 2x7 header. On the LED mezzanine, it is a 2x7 surface-mount socket strip. The pin assignments are as follows:

Table 4-1. LED Mezzanine Connector

1	GND	RESETSW*	2
3	IRQ_5	ABORTSW*	4
5	PCILED*	FAILLED*	6
7	LANLED*	STATLED*	8
9	FUSELED*	RUNLED*	10
11	SBSYLED*	SCONLED*	12
13	+5V	SPKR	14

MPU Mezzanine Connector

A 152-pin connector (J14 on the MVME1600-001 base board, J17 on the MVME1600-011) supplies the interface between the base board and the MPU mezzanine module. The pin assignments are listed in the following table.

Table 4-2. MPU Mezzanine Connector

1	PCICLK1		PCICLK2	2
3	PCICLK3		PCICLK4	4
5	GND		GND	6
7	CKSTOP*		CPULED*	8
9	IBCINT*		ABORT*	10
11	LANINT*		VME2PCIINT*	12
13	SCSIINT*		GRINT*	14
15	PMCIRQ*		KBIRQ	16
17	MOUSEIRQ		COM1IRQ	18
19	COM2IRQ	GND	PARPTIRQ	20
21	CIO_IRQ*		SCC_IRQ*	22
23	FLPYIRQ*		IRQ_B*	24
25	SMI*		SRESET*	26
27	NMI		LBRESET*	28
29	TBEN		PURESET*	30
31	TCK		TDO1	32
33	TDI1		TMS	34
35	PMCP*		TRST*	36
37	PMCREQ*		PMCGNT*	38
39	ISA_MSTR*		FLSHREQ*	40
41	SD7		FLSHACK*	42
43	SD6		Reserved	44
45	SD5		RAMCFG*	46
47	SD4		CPUCNFG*	48
49	SD3		X_IOR*	50
51	SD2		X_IOW*	52
53	SD1		SA1	54
55	SD0		SA0	56
57	–12V	+5V	+12V	58
59	SERR*		PERR*	60
61	SDONE		LOCK*	62
63	SBO*		DEVSEL*	64
65	GND		GND	66
67	IRDY*		TRDY*	68
69	FRAME*		STOP*	70
71	GND		GND	72
73	PCIGNT*		ACK64*	74
75	PCIREQ*		REQ64*	76

Table 4-2. MPU Mezzanine Connector (Continued)

77	Reserved		PAR	78
79	CBE0*		CBE1*	80
81	CBE2*		CBE3*	82
83	AD0		AD1	84
85	AD2		AD3	86
87	AD4		AD5	88
89	AD6		AD7	90
91	AD8		AD9	92
93	AD10		AD11	94
95	AD12	GND	AD13	96
97	AD14		AD15	98
99	AD16		AD17	100
101	AD18		AD19	102
103	AD20		AD21	104
105	AD22		AD23	106
107	AD24		AD25	108
109	AD26		AD27	110
111	AD28		AD29	112
113	AD30		AD31	114
115	PCI_RESV5		PAR64	116
117	CBE4*		CBE5*	118
119	CBE6*		CBE7*	120
121	AD32		AD33	122
123	AD34		AD35	124
125	AD36		AD37	126
127	AD38		AD39	128
129	AD40		AD41	130
131	AD42		AD43	132
133	AD44	+3.3V	AD45	134
135	AD46		AD47	136
137	AD48		AD49	138
139	AD50		AD51	140
141	AD52		AD53	142
143	AD54		AD55	144
145	AD56		AD57	146
147	AD58		AD59	148
149	AD60		AD61	150
151	AD62		AD63	152

CPU Connector

A 190-pin connector (J2 on the PM603/PM604 processor/memory mezzanine module) provides access to the processor bus (MPU bus) and some MPC105 bridge/memory controller signals. It can be used to add L2 cache memory (refer to the PM603/PM604 *User's Manual*) or to upgrade the processor. The pin assignments are listed in the following table.

Table 4-3. CPU Connector

1	PA0		PA1	2
3	PA2		PA3	4
5	PA4		PA5	6
7	PA6		PA7	8
9	PA8		PA9	10
11	PA10		PA11	12
13	PA12		PA13	14
15	PA14		PA15	16
17	PA16		PA17	18
19	PA18	GND	PA19	20
21	PA20		PA21	22
23	PA22		PA23	24
25	PA24		PA25	26
27	PA26		PA27	28
29	PA28		PA29	30
31	PA30		PA31	32
33	PA_PAR0		PA_PAR1	34
35	PA_PAR2		PA_PAR3	36
37	APE*		RSRV*	38
39	PD0		PD1	40
41	PD2		PD3	42
43	PD4		PD5	44
45	PD6		PD7	46
47	PD8		PD9	48
49	PD10		PD11	50
51	PD12		PD13	52
53	PD14		PD15	54
55	PD16		PD17	56
57	PD18	+5V	PD19	58
59	PA20		PD21	60
61	PD22		PD23	62
63	PD24		PD25	64
65	PD26		PD27	66
67	PD28		PD29	68
69	PD30		PD31	70
71	PD32		PD33	72
73	PD34		PD35	74
75	PD36		PD37	76

Table 4-3. CPU Connector (Continued)

77	PD38		PD39	78
79	PD40		PD41	80
81	PD42		PD43	82
83	PD44		PD45	84
85	PD46		PD47	86
87	PD48		PD49	88
89	PA50		PD51	90
91	PD52		PD53	92
93	PD54		PD55	94
95	PD56	GND	PD57	96
97	PD58		PD59	98
99	PD60		PD61	100
101	PD62		PD63	102
103	PDPAR0		PDPAR1	104
105	PDPAR2		PDPAR3	106
107	PDPAR4		PDPAR5	108
109	PDPAR6		PDPAR7	110
111	No Connection		No Connection	112
113	DPE*		DBDIS*	114
115	TT0		TSIZ0	116
117	TT1		TSIZ1	118
119	TT2		TSIZ2	120
121	TT3		TC0	122
123	TT4		TC1	124
125	CI*		TC2	126
127	WT*		CSE0	128
129	GLOBAL*		CSE1	130
131	SHARED*		DBWO*	132
133	AACK*	+3.3V	TS*	134
135	ARTY*		XATS*	136
137	DRTY*		TBST*	138
139	TA*		No Connection	140
141	TEA*		No Connection	142
143	No Connection		DBG*	144
145	No Connection		DBB*	146
147	No Connection		ABB*	148
149	TCLK_OUT		CPUGNT*	150
151	L2PRSNT0*		CPUREQ*	152

Table 4-3. CPU Connector (Continued)

153	L2ADSC*		IBCINT*	154
155	L2BAA*		MCHK*	156
157	L2DIRTYI*		SMI*	158
159	L2DIRTYO*		CKSTPI*	160
161	L2DOE*		CKSTPO*	162
163	L2DWE1*		HALTED (N/C)	164
165	L2HIT*		TLBISYNC*	166
167	L2TALE		TBEN	168
169	L2TALOE*		SUSPEND*	170
171	L2TOE*	GND	DRVMOD0	172
173	L2TWE*		DRVMOD1 (N/C	174
175	L2TV		NAPRUN (N/C	176
177	L2PRSNT1*		QREQ*	178
179	SRESET*		QACK*	180
181	HRESET*		CPUTDO	182
183	GND		CPUTDI	184
185	CPUCLK1		CPUTCK	186
187	CPUCLK2		CPUTMS	188
189	CPUCLK3		CPUTRST*	190

DRAM Expansion Connectors

Two 100-pin connectors (J3 and J4 on the PM603/PM604 processor/memory mezzanine module) supply the interface between the processor/memory mezzanine and the RAM104 DRAM mezzanine. The pin assignments are listed in the following two tables.

Table 4-4. DRAM Mezzanine—Connector 1

1	GND	MA_BB0	2	51	GND	BCASB7*	52
3	MA_BB1	MA_BB2	4	53	BMD0	GND	54
5	MA_BB3	GND	6	55	GND	BMD1	56
7	GND	MA_BB4	8	57	BMD2	GND	58
9	MA_BB5	MA_BB6	10	59	GND	BMD3	60
11	MA_BB7	GND	12	61	BMD4	GND	62
13	GND	MA_BB8	14	63	GND	BMD5	64
15	MA_BB9	MA_BB10	16	65	BMD6	+5V	66
17	MA_BB11	GND	18	67	+5V	BMD7	68
19	GND	BWEB2*	20	69	BMD8	GND	70
21	BRASB0*	GND	22	71	GND	BMD9	72
23	GND	BRASB1*	24	73	BMD10	+5V	74
25	BRASB2*	GND	26	75	+5V	BMD11	76
27	GND	BRASB3*	28	77	BMD12	GND	78
29	BRASB4*	GND	30	79	GND	BMD13	80
31	GND	BRASB5*	32	81	BMD14	+5V	82
33	BRASB6*	GND	34	83	+5V	BMD15	84
35	GND	BRASB7*	36	85	BMD16	GND	86
37	BCASB0*	GND	38	87	GND	BMD17	88
39	GND	BCASB1*	40	89	BMD18	+5V	90
41	BCASB2*	GND	42	91	+5V	BMD19	92
43	GND	BCASB3*	44	93	BMD20	GND	94
45	BCASB4*	GND	46	95	GND	BMD21	96
47	GND	BCASB5*	48	97	BMD22	+5V	98
49	BCASB6*	GND	50	99	+5V	BMD23	100

Table 4-5. DRAM Mezzanine—Connector 2

1	BWEB3*	GND	2	51	GND	BMD48	52
3	GND	BMD24	4	53	BMD49	GND	54
5	BMD25	GND	6	55	GND	BMD50	56
7	GND	BMD26	8	57	BMD51	+3.3V	58
9	BMD27	GND	10	59	+3.3V	BMD52	60
11	GND	BMD28	12	61	BMD53	GND	62
13	BMD29	GND	14	63	GND	BMD54	64
15	GND	BMD30	16	65	BMD55	+3.3V	66
17	BMD31	GND	18	67	+3.3V	BMD56	68
19	GND	BMD32	20	69	BMD57	GND	70
21	BMD33	GND	22	71	GND	BMD58	72
23	GND	BMD34	24	73	BMD59	+3.3V	74
25	BMD35	GND	26	75	+3.3V	BMD60	76
27	GND	BMD36	28	77	BMD61	GND	78
29	BMD37	GND	30	79	GND	BMD62	80
31	GND	BMD38	32	81	BMD63	+3.3V	82
33	BMD39	GND	34	83	+3.3V	BDP0	84
35	GND	BMD40	36	85	BDP1	BDP2	86
37	BMD41	GND	38	87	BDP3	GND	88
39	GND	BMD42	40	89	GND	BDP4	90
41	BMD43	GND	42	91	BDP5	BDP6	92
43	GND	BMD44	44	93	BDP7	+3.3V	94
45	BMD45	GND	46	95	+3.3V	No Conn.	96
47	GND	BMD46	48	97	B3SIZ0	B3SIZ1	98
49	BMD47	GND	50	99	B4SIZ0	B4SIZ1	100

PCI Mezzanine Card Connectors

Two 64-pin connectors (J11 and J12 on the base board) supply the interface between the base board and an optional PCI mezzanine card (PMC). The pin assignments are listed in the following table.

VMEbus Connector P1

Two 96-pin connectors (P1 and P2) supply the interface between the base board and the VMEbus. P1 provides power and VME signals for 24-bit addressing and 16-bit data. Its pin assignments are set by the VMEbus specification. They are listed in Table 4-7.

Table 4-6. PCI Mezzanine Card Connector

	J11				J12		
1	TCK	–12V	2	1	+12V	TRST*	2
3	GND	INTA*	4	3	TMS	TDO2	4
5	INTB*	INTC*	6	5	TDO1	GND	6
7	PNCP*	+5V	8	7	GND	Not Used	8
9	INTD*	Not Used	10	9	Not Used	Not Used	10
11	GND	Not Used	12	11	Pull-up	+3.3V	12
13	CLK	GND	14	13	LBRESET*	Pull-down	14
15	GND	PMCGNT*	16	15	+3.3V	Pull-down	16
17	PMCREQ*	+5V	18	17	Not Used	GND	18
19	+5V	AD31	20	19	AD30	AD29	20
21	AD28	AD27	22	21	GND	AD26	22
23	AD25	GND	24	23	AD24	+3.3V	24
25	GND	CBE3*	26	25	IDSEL	AD23	26
27	AD22	AD21	28	27	+3.3V	AD20	28
29	AD19	+5V	30	29	AD18	GND	30
31	+5V	AD17	32	31	AD16	CBE2*	32
33	FRAME*	GND	34	33	GND	Not Used	34
35	GND	IRDY*	36	35	TDRY*	+3.3V	36
37	DEVSEL*	+5V	38	37	GND	STOP*	38
39	GND	LOCK*	40	39	PERR*	GND	40
41	SDONE*	SBO*	42	41	+3.3V	SERR*	42
43	PAR	GND	44	43	CBE1*	GND	44
45	+5V	AD15	46	45	AD14	AD13	46
47	AD12	AD11	48	47	GND	AD10	48
49	AD09	+5V	50	49	AD08	+3.3V	50
51	GND	CBE0*	52	51	AD07	Not Used	52
53	AD06	AD05	54	53	+3.3V	Not Used	54
55	AD04	GND	56	55	Not Used	GND	56
57	+5V	AD03	58	57	Not Used	Not Used	58
59	AD02	AD01	60	59	GND	Not Used	60
61	AD00	+5V	62	61	ACK64*	+3.3V	62
63	GND	REQ64*	64	63	GND	Not Used	64

Table 4-7. VMEbus Connector P1

	Row A	Row B	Row C	
1	VD0	VBBSY*	VD8	1
2	VD1	VBCLR*	VD9	2
3	VD2	VACFAIL*	VD10	3
4	VD3	VBGIN0*	VD11	4
5	VD4	VBGOUT0*	VD12	5
6	VD5	VBGIN1*	VD13	6
7	VD6	VBGOUT1*	VD14	7
8	VD7	VBGIN2*	VD15	8
9	GND	VBGOUT2*	GND	9
10	VSYSCLK	VBGIN3*	VSYSFAIL*	10
11	GND	VBGOUT3*	VBERR*	11
12	VDS1*	VBR0*	VSYSRESET*	12
13	VDS0*	VBR1*	VLWORD	13
14	VWRITE*	VBR2*	VAM5	14
15	GND	VBR3*	VA23	15
16	VDTACK*	VAM0	VA22	16
17	GND	VAM1	VA21	17
18	VAS*	VAM2	VA20	18
19	GND	VAM3	VA19	19
20	VIACK*	GND	VA18	20
21	VIACKIN*	VSERCLK	VA17	21
22	VIACKOUT*	VSERDAT	VA16	22
23	VAM4	GND	VA15	23
24	VA7	VIRQ7*	VA14	24
25	VA6	VIRQ6*	VA13	25
26	VA5	VIRQ5*	VA12	26
27	VA4	VIRQ4*	VA11	27
28	VA3	VIRQ3*	VA10	28
29	VA2	VIRQ2*	VA9	29
30	VA1	VIRQ1*	VA8	30
31	–12V	+5VSTDBY	+12V	31
32	+5V	+5V	+5V	32

Ethernet 10BaseT Connector

The MVME1603/MVME1604 provides both AUI and 10BaseT LAN connections. The 10BaseT interface is implemented with a standard RJ45 socket. For MVME1600-001 base boards, the RJ45 connector is located on the MVME760 transition module; for MVME1600-011 base boards, it is located on the front panel of the board itself. The pin assignments are listed in the following table.

Table 4-8. Ethernet 10BaseT Connector

1	ENTD
2	ENTD*
3	ENRD
4	No Connection
5	No Connection
6	ENRD*
7	No Connection
8	No Connection

Disk Drive Connector

A 34-pin connector (J6 on the base board) supplies the interface between the base board and an optional disk drive. The disk drive may take the form of a mezzanine board or a separate module. The pin assignments are listed in the following table.

Table 4-9. Disk Drive Mezzanine Connector

1	GND	F_DENSEL	2
3	GND	No Connection	4
5	GND	F_MSEN0	6
7	No Connection	F_INDEX*	8
9	GND	F_MTR0*	10
11	GND	F_DR1*	12
13	No Connection	F_DR0*	14
15	GND	F_MTR1*	16
17	F_MSEN1	F_DIR*	18
19	GND	F_STEP*	20
21	GND	F_WDATA*	22
23	GND	F_WGATE*	24
25	GND	F_TRK0*	26
27	GND	F_WP*	28
29	GND	F_RDATA*	30
31	GND	F_HDSEL*	32
33	GND	F_DSKCHG*	34

MVME1600-001 Connectors

The following tables summarize the pin assignments of connectors that are specific to MVME1603/MVME1604 modules based on the MVME1600-001 base board, used with MVME760 transition modules.

VMEbus Connector P2

Two 96-pin connectors (P1 and P2) supply the interface between the base board and the VMEbus. P1 provides power and VME signals for 24-bit addressing and 16-bit data. Its pin assignments are set by the VMEbus specification. P2 rows A and C provide power and interface signals to the MVME760 transition module. P2 row C supplies the base board with power, with the upper eight VMEbus address lines, and with an additional 16 VMEbus data lines. The pin assignments for P2 are listed in the following table.

SCSI Connector

The SCSI connector for the MVME1600-001 base board is a 68-pin high-density connector located on the front panel. The pin assignments for the SCSI connector are listed in Table 4-19.

Table 4-10. SCSI Connector

1	GND	SCSID12*	35
2	GND	SCSID13*	36
3	GND	SCSID14*	37
4	GND	SCSID15*	38
5	GND	SCSCDP1	39
6	GND	SCSID0*	40
7	GND	SCSID1*	41
8	GND	SCSID2*	42
9	GND	SCSID3*	43
10	GND	SCSID4*	44
11	GND	SCSID5*	45
12	GND	SCSID6*	46
13	GND	SCSID7*	47
14	GND	SCSCDP0	48
15	GND	GND	49
16	GND	GND	50
17	SCSI_TP	SCSI_TP	51
18	SCSI_TP	SCSI_TP	52
19	No Connection	No Connection	53
20	GND	GND	54
21	GND	SATN*	55
22	GND	GND	56
23	GND	SBSY*	57
24	GND	SACK*	58
25	GND	SRST*	59
26	GND	SMSG*	60
27	GND	SSEL*	61
28	GND	SC_D*	62
29	GND	SREQ*	63
30	GND	SI_O*	64
31	GND	SCSID8*	65
32	GND	SCSID9*	66
33	GND	SCSID10*	67
34	GND	SCSID11*	68

Graphics Connector

The MVME1600-001 base board has a DB15 graphics connector located on the front panel. The pin assignments for the graphics connector are listed in the following table.

Table 4-11. Graphics Connector

1	GIRED
2	GIGREEN
3	GIBLUE
4	GIP2
5	GND
6	GND
7	GND
8	GND
9	No Connection
10	GND
11	GIP0
12	GIP1
13	GIHSYNC
14	GIVSYNC
15	GIP3

Keyboard and Mouse Connectors

The MVME1600-001 base board has two 6-pin circular DIN connectors for the keyboard and mouse located on the front panel. The pin assignments for those connectors are listed in the following two tables.

Table 4-12. Keyboard Connector

1	K_DATA
2	No Connection
3	GND
4	+5VKBM
5	K_CLK
6	No Connection

Table 4-13. Mouse Connector

1	M_DATA
2	No Connection
3	GND
4	+5VKBM
5	M_CLK
6	No Connection

Ethernet AUI Connector

The MVME1603/MVME1604 provides both AUI and 10BaseT LAN connections. For the MVME1600-001 base board, the AUI interface is implemented with a DB15 (J11) connector located on the MVME760 transition module. The pin assignments are listed in the following table.

Table 4-14. Ethernet AUI Connector (MVME760)

1	GND
2	C+
3	T+
4	GND
5	R+
6	GND
7	No Connection
8	GND
9	C-
10	T-
11	GND
12	R-
13	+12V
14	GND
15	No Connection

Parallel I/O Connector

Both versions of the base board provide parallel I/O connections. For the MVME1600-001 base board, the parallel interface is implemented with an IEEE P1284 36-pin connector (J10) located on the MVME760 transition module. The pin assignments are listed in the following table.

Table 4-15. Parallel I/O Connector (MVME760)

1	PRBSY	GND	19
2	PRSEL	GND	20
3	PRACK*	GND	21
4	PRFAULT*	GND	22
5	PRPE	GND	23
6	PRD0	GND	24
7	PRD1	GND	25
8	PRD2	GND	26
9	PRD3	GND	27
10	PRD4	GND	28
11	PRD5	GND	29
12	PRD6	GND	30
13	PRD7	GND	31
14	INPRIME*	GND	32
15	PRSTB*	GND	33
16	SELIN*	GND	34
17	AUTOFD*	GND	35
18	Pull-up	No Connection	36

Serial Ports 1 and 2

The MVME1603/MVME1604 provides both asynchronous (ports 1 and 2) and synchronous/asynchronous (ports 3 and 4) serial connections. For the MVME1600-001 base board, the asynchronous interface is implemented with a pair of DB9 connectors (COM1 and COM2) located on the MVME760 transition module. The pin assignments are listed in the following table.

Table 4-16. Serial Connections—Ports 1 and 2 (MVME760)

1	SP*n*DCD
2	SP*n*RD
3	SP*n*TD
4	SP*n*DTR
5	GND
6	SP*n*DSR
7	SP*n*RTS
8	SP*n*CTS
9	SP*n*RI

Serial Ports 3 and 4

For the MVME1600-001 base board, the synchronous/ asynchronous interface for ports 3 and 4 is implemented with a pair of 26-pin 3M-type ribbon connectors (J7 and J2) located on the board surface of the MVME760 transition module. In addition, serial port 3 has an HD26 front panel connector (J5). The pin assignments for serial ports 3 and 4 are listed in the following table.

Table 4-17. Serial Connections—Ports 3 and 4 (MVME760)

Panel Connector		Ribbon Connector
1	No Connection	1
2	TXD*n*	3
3	RXD*n*	5
4	RTS*n*	7
5	CTS*n*	9
6	DSR*n*	11
7	GND	13
8	DCD*n*	15
9	SP*n*_P9	17
10	SP*n*_P10	19
11	SP*n*_P11	21
12	SP*n*_P12	23
13	SP*n*_P13	25
14	SP*n*_P14	2
15	TXCI*n*	4
16	SP*n*_P16	6
17	RXCI*n*	8
18	LLB*n*	10
19	SP*n*_P19	12
20	DTR*n*	14
21	RLB*n*	16
22	RI*n*	18
23	SP*n*_P23	20
24	TXCO*n*	22
25	TM*n*	24
26	No Connection	26

MVME1600-011 Connectors

The following tables summarize the pin assignments of connectors that are specific to MVME1603/MVME1604 modules based on the MVME1600-011 base board, used with MVME712M transition modules.

VMEbus Connector P2

Two 96-pin connectors (P1 and P2) supply the interface between the base board and the VMEbus. P1 provides power and VME signals for 24-bit addressing and 16-bit data. Its pin assignments are set by the VMEbus specification. P2 rows A and C provide power and interface signals to the MVME712M transition module. P2 row C supplies the base board with power, with the upper eight VMEbus address lines, and with an additional 16 VMEbus data lines. The pin assignments for P2 are listed in the following table.

SCSI Connector

The SCSI connector for the MVME1600-011 base board is a 50-pin connector located on the front panel of the MVME712M transition module. The pin assignments for the SCSI connector are listed in Table 4-19.

Table 4-18. VMEbus Connector P2

	Row A	Row B	Row C	
1	SCSID0	+5V	ENC*	1
2	SCSID1	GND	ENC	2
3	SCSID2	RETRY*	ENT*	3
4	SCSID3	VA24	ENT	4
5	SCSID4	VA25	ENR*	5
6	SCSID5	VA26	ENR	6
7	SCSID6	VA27	+12VLAN	7
8	SCSID7	VA28	PR_STD	8
9	SCSIDPO	VA29	PR_DATA0	9
10	SATN*	VA30	PR_DATA1	10
11	SBSY*	VA31	PR_DATA2	11
12	SACK*	GND	PR_DATA3	12
13	SRST*	+5V	PR_DATA4	13
14	SMSG*	VD16	PR_DATA5	14
15	SSEL*	VD17	PR_DATA6	15
16	SC_D*	VD18	PR_DATA7	16
17	SREQ*	VD19	PR_ACK*	17
18	SI_O*	VD20	PR_BSY	18
19	TXD3	VD21	PR_PE	19
20	RXD3	VD22	PR_SLCT	20
21	RTS3	VD23	PR_INIT*	21
22	CTS3	GND	PR_ERR*	22
23	DTR3	VD24	TXD1	23
24	DCD3	VD25	RXD1	24
25	TXD4	VD26	RTS1	25
26	RXD4	VD27	CTS1	26
27	RTS4	VD28	TXD2	27
28	TRXC4	VD29	RXD2	28
29	CTS4	VD30	RTS2	29
30	DTR4	VD31	CTS2	30
31	DCD4	GND	DTR2	31
32	RTXC4	+5V	DCD2	32

Table 4-19. SCSI Connector (MVME712M)

1	GND	DB00*	26
2	GND	DB01*	27
3	GND	DB02*	28
4	GND	DB03*	29
5	GND	DB04*	30
6	GND	DB05*	31
7	GND	DB06*	32
8	GND	DB07*	33
9	GND	DBP*	34
10	GND	GND	35
11	GND	GND	36
12	GND	GND	37
13	Reserved	TERMPWR	38
14	GND	GND	39
15	GND	GND	40
16	GND	ATN*	41
17	GND	GND	42
18	GND	BSY*	43
19	GND	ACK*	44
20	GND	RST*	45
21	GND	MSG*	46
22	GND	SEL*	47
23	GND	D/C*	48
24	GND	REQ*	49
25	GND	O/I*	50

Ethernet AUI Connector

The MVME1603/MVME1604 provides both AUI and 10BaseT LAN connections. For the MVME1600-011 base board, the AUI interface is implemented with a DB15 connector located on the MVME712M transition module. The pin assignments are listed in the following table.

Table 4-20. Ethernet AUI Connector (MVME712M)

1	No Connection
2	C+
3	T+
4	No Connection
5	R+
6	GND
7	No Connection
8	No Connection
9	C-
10	T-
11	No Connection
12	R-
13	+12V
14	No Connection
15	No Connection

Parallel I/O Connector

Both versions of the base board provide parallel I/O connections. For the MVME1600-011 base board, the parallel interface is implemented with a 36-pin Centronics-type socket connector located on the MVME712M transition module. The pin assignments are listed in the following table.

Table 4-21. Parallel I/O Connector (MVME712M)

1	PRSTB*	GND	19
2	PRD0	GND	20
3	PRD1	GND	21
4	PRD2	GND	22
5	PRD3	GND	23
6	PRD4	GND	24
7	PRD5	GND	25
8	PRD6	GND	26
9	PRD7	GND	27
10	PRACK*	GND	28
11	PRBSY	GND	29
12	PRPE	GND	30
13	PRSEL	INPRIME*	31
14	No Connection	PRFAULT*	32
15	No Connection	No Connection	33
16	GND	No Connection	34
17	No Connection	No Connection	35
18	No Connection	No Connection	36

Serial Ports 1-4

For the MVME1600-011 base board, the interface for asynchronous ports 1 and 2 and for synchronous/asynchronous ports 3 and 4 is implemented with four EIA-232-D DB25 connectors (J7-J10) located on the front panel of the MVME712M transition module. In addition, ports 3 and 4 have HD26 front panel connectors (J2, J3) on the base board. The pin assignments for serial ports 1-4 on the MVME712M are listed in the following table.

Table 4-22. Serial Connections—MVME712M Ports 1-4

1	No Connection
2	ETXD*n*
3	ERXD*n*
4	ERTS*n*
5	ECTS*n*
6	EDSR*n*
7	GND
8	EDCD*n*
9	No Connection
10	No Connection
11	No Connection
12	No Connection
13	No Connection
14	No Connection
15	ERTXC (*Port 4 only*)
16	No Connection
17	ERRXC (*Port 4 only*)
18	No Connection
19	No Connection
20	EDTR*n*
21	No Connection
22	No Connection
23	No Connection
24	ETTXC (*Port 4 only*)
25	No Connection

The pin assignments for serial ports 3 and 4 at the MVME1600-011 front panel are listed in the following table.

Table 4-23. Serial Connections—MVME1600-011 Ports 3 and 4

1	No Connection
2	TXD*n*
3	RXD*n*
4	RTS*n*
5	CTS*n*
6	SP*n*DSR
7	GND
8	DCD*n*
9	No Connection
10	No Connection
11	No Connection
12	No Connection
13	No Connection
14	No Connection
15	SP*n*TXC
16	No Connection
17	SP*n*RXC
18	SP*n*LL
19	No Connection
20	DTR*n*
21	SP*n*RL
22	SP*n*RI
23	No Connection
24	SP*n*TXCO
25	SP*n*TM
26	No Connection

For detailed descriptions of the various interconnect signals, consult the support information documentation package for the MVME1603/MVME1604 SBC or the support information sections of the MVME760 or MVME712M transition module documentation as necessary.

Overview

The PowerPC debugger, PPCBug, is a powerful evaluation and debugging tool for systems built around Motorola PowerPC microcomputers. Facilities are available for loading and executing user programs under complete operator control for system evaluation.

The PowerPC debugger provides a high degree of functionality and user friendliness, and yet stresses portability and ease of maintenance. It achieves good portability and comprehensibility because it was written entirely in the C programming language, except where necessary to use assembler functions.

PPCBug includes commands for display and modification of memory, breakpoint and tracing capabilities, a powerful assembler and disassembler useful for patching programs, and a ‘‘self-test at power-up’’ feature which verifies the integrity of the system.

Various PPCBug routines that handle I/O, data conversion, and string functions are available to user programs through the System Call handler.

PPCBug consists of three parts:

- A command-driven user-interactive software debugger. It is hereafter referred to as “the debugger” or “PPCBug.”
- A set of command-driven diagnostics, which is hereafter referred to as “the diagnostics.”
- A user interface which accepts commands from the system console terminal.

When using PPCBug, you will operate out of either the debugger directory or the diagnostic directory. The debugger prompt (`PPC1-Bug` or `PPC1-Diag`) tells you the current directory.

Because PPCBug is command-driven, it performs its various operations in response to user commands entered at the keyboard. The flow of control in PPCBug is described in the *PPCBug Firmware Package User's Manual.* When you enter a command, PPCBug executes the command and the prompt reappears. However, if you enter a command that causes execution of user target code (e.g., **GO**), then control may or may not return to PPCBug, depending on the outcome of the user program.

The PPCBug is similar to previous Motorola firmware debugging packages (e.g., MVME147Bug, MVME167Bug, MVME187Bug), with differences due to microprocessor architectures. These are primarily reflected in the instruction mnemonics, register displays, addressing modes of the assembler/disassembler, and the passing of arguments to the system calls.

Memory Requirements

PPCBug requires a total of 512KB of read/write memory (i.e., DRAM). The debugger allocates this space from the top of memory. For example, a system containing 64MB ($04000000) of read/write memory will place the PPCBug memory page at locations $03F80000 to $03FFFFFF.

PPCBug Implementation

PPCBug is written largely in the C programming language, providing benefits of portability and maintainability. Where necessary, assembly language has been used in the form of separately compiled program modules containing only assembler code. No mixed-language modules are used.

Physically, PPCBug is contained in two socketed 32-pin PLCC/CLCC FLASH devices that together provide 1MB of storage. The executable code is checksummed at every power-on or reset firmware entry, and the result (which includes a precalculated checksum contained in the FLASH devices), is tested for an expected zero.

Using the Debugger

PPCBug is command-driven; it performs its various operations in response to commands that you enter at the keyboard. When the `PPC1-Bug` prompt appears on the screen, the debugger is ready to accept debugger commands. When the `PPC1-Diag` prompt appears on the screen, the debugger is ready to accept diagnotics commands. To switch from one mode to the other, enter **SD**.

What you key in is stored in an internal buffer. Execution begins only after you press the Return or Enter key. This allows you to correct entry errors, if necessary, with the control characters described in the *PPCBug Firmware Package User's Manual*, Chapter 1.

After the debugger executes the command, the prompt reappears. However, if the command causes execution of user target code (for example **GO**) then control may or may not return to the debugger, depending on what the user program does. For example, if a breakpoint has been specified, then control returns to the debugger when the breakpoint is encountered during execution of the user program. Alternately, the user program could return to the debugger by means of the System Call Handler routine RETURN (described in the *PPCBug Firmware Package User's Manual*, Chapter 5). For more about this, refer to the **GD**, **GO**, and **GT** command descriptions in the *PPCBug Firmware Package User's Manual*, Chapter 3.

A debugger command is made up of the following parts:

- The command name, either uppercase or lowercase (e.g., **MD** or **md**).
- Any required arguments, as specified by command.
- At least one space before the first argument. Precede all other arguments with either a space or comma.
- One or more options. Precede an option or a string of options with a semicolon (**;**). If no option is entered, the command's default option conditions are used.

Debugger Commands

The individual debugger commands are listed in the following table. The commands are described in detail in the *PPCBug Firmware Package User's Manual*, Chapter 2.

Note You can list all the available debugger commands by entering the Help (**HE**) command alone. You can view the syntax for a particular command by entering **HE** and the command mnemonic, as listed below.

Table 5-1. Debugger Commands

Command	Description
AS	One Line Assembler
BC	Block of Memory Compare
BF	Block of Memory Fill
BI	Block of Memory Initialize
BM	Block of Memory Move
BR	Breakpoint Insert
NOBR	Breakpoint Delete
BS	Block of Memory Search
BV	Block of Memory Verify
CM	Concurrent Mode
NOCM	No Concurrent Mode
CNFG	Configure Board Information Block
CS	Checksum
DC	Data Conversion
DMA	Block of Memory Move
DS	One Line Disassembler
DU	Dump S-Records
ECHO	Echo String
ENV	Set Environment
GD	Go Direct (Ignore Breakpoints)
GEVBOOT	Global Environment Variable Boot
GEVDEL	Global Environment Variable Delete

Table 5-1. Debugger Commands (Continued)

Command	Description
GEVDUMP	Global Environment Variable(s) Dump
GEVEDIT	Global Environment Variable Edit
GEVINIT	Global Environment Variable Initialization
GEVSHOW	Global Environment Variable(s) Display
GN	Go to Next Instruction
GO	Go Execute User Program
GT	Go to Temporary Breakpoint
HE	Help
IOC	I/O Control for Disk
IOI	I/O Inquiry
IOP	I/O Physical (Direct Disk Access)
IOT	I/O Teach for Configuring Disk Controller
LO	Load S-Records from Host
MA	Macro Define/Display
NOMA	Macro Delete
MAE	Macro Edit
MAL	Enable Macro Listing
NOMAL	Disable Macro Listing
MAR	Load Macros
MAW	Save Macros
MD, MDS	Memory Display
MENU	System Menu
MM	Memory Modify
MMD	Memory Map Diagnostic
MS	Memory Set
MW	Memory Write
NAB	Automatic Network Boot
NBH	Network Boot Operating System, Halt
NBO	Network Boot Operating System
NIOC	Network I/O Control
NIOP	Network I/O Physical
NIOT	Network I/O Teach (Configuration)
NPING	Network Ping

Table 5-1. Debugger Commands (Continued)

Command	Description
OF	Offset Registers Display/Modify
PA	Printer Attach
NOPA	Printer Detach
PBOOT	Bootstrap Operating System
PF	Port Format
NOPF	Port Detach
PFLASH	Program FLASH Memory
PS	Put RTC into Power Save Mode
RB	ROMboot Enable
NORB	ROMboot Disable
RD	Register Display
REMOTE	Remote
RESET	Cold/Warm Reset
RL	Read Loop
RM	Register Modify
RS	Register Set
SD	Switch Directories
SET	Set Time and Date
SYM	Symbol Table Attach
NOSYM	Symbol Table Detach
SYMS	Symbol Table Display/Search
T	Trace
TA	Terminal Attach
TIME	Display Time and Date
TM	Transparent Mode
TT	Trace to Temporary Breakpoint
VE	Verify S-Records Against Memory
VER	Revision/Version Display
WL	Write Loop

Caution Although a command to allow the erasing and reprogramming of FLASH memory is available to you, keep in mind that reprogramming any portion of FLASH memory will erase everything currently contained in FLASH, including the PPC1Bug debugger.

Diagnostic Tests

The individual diagnostic test sets are listed in the following table. The diagnostics are described in the *PPC1Bug Diagnostics Manual.*

Table 5-2. Diagnostic Test Groups

Test Set	Description	Applicability
DEC21040	DECchip 21040 Ethernet Controller Tests	All MVME1603/1604
I82378	i82378 PCI/ISA Bridge Tests	All MVME1603/1604
KBD87303	PC87303 Keyboard/Mouse Tests	Not applicable to versions with “-011” base board
L2CACHE	Level 2 Cache Tests	MVME1603/1604 with L2 cache only
NCR	NCR 53C825/53C810 SCSI-2 I/O Processor Tests	All MVME1603/1604
PAR87303	PC87303/87323 Parallel Port Test	All MVME1603/1604
PC16550	PC16550 UART Tests	All MVME1603/1604
PCIBUS	Generic PCI/PMC Slot Test	All MVME1603/1604
RAM	Local RAM Tests	All MVME1603/1604
RTC	MK48T18 Real-Time Clock Tests	All MVME1603/1604
SCC	Z85230 Serial Communication Controller Tests	All MVME1603/1604
VGA544x	Video Diagnostics Tests	Not applicable to versions with “-011” base board
VME2	VMEchip2 VME Interface ASIC Tests	All MVME1603/1604
Z8536	Z8536 Counter/Timer Tests	All MVME1603/1604

Notes You may enter command names in either uppercase or lowercase.

Some diagnostics depend on restart defaults that are set up only in a particular restart mode. Refer to the documentation on a particular diagnostic for the correct mode.

CNFG and ENV Commands 6

Overview

You can use the factory-installed debug monitor, PPCBug, to modify certain parameters contained in the PowerPC board's Non-Volatile RAM (NVRAM), also known as Battery Backed-up RAM (BBRAM).

- The Board Information Block in NVRAM contains various elements concerning operating parameters of the hardware. Use the PPCBug command **CNFG** to change those parameters.
- Use the PPCBug command **ENV** to change configurable PPCBug parameters in NVRAM.

The **CNFG** and **ENV** commands are both described in the *PPCBug Firmware Package User's Manual* (part number PPCBUGA1/UM). Refer to that manual for general information about their use and capabilities.

The following paragraphs present additional information about **CNFG** and **ENV** that is specific to the PPCBug debugger, along with the parameters that can be configured with the **ENV** command.

CNFG - Configure Board Information Block

Use this command to display and configure the Board Information Block, which is resident within the NVRAM. The board information block contains various elements detailing specific operational parameters of the PowerPC board. The board structure for the PowerPC board is as shown in the following example for an MVME1603-001:

```
Board (PWA) Serial Number     = “MOT001673590   ”
Board Identifier              = “MVME1603-001   ”
Artwork (PWA) Identifier      = “01-w3015F01A   ”
MPU Clock Speed               = “066            ”
Bus Clock Speed               = “033            ”
Ethernet Address              = 08003E20C983
Local SCSI Identifier         = “07”
System Serial Number          = “1463725        ”
System Identifier             = “Motorola MVME1603-00x”
```

The parameters that are quoted are left-justified character (ASCII) strings padded with space characters, and the quotes (“) are displayed to indicate the size of the string. Parameters that are not quoted are considered data strings, and data strings are right-justified. The data strings are padded with zeroes if the length is not met.

The Board Information Block is factory-configured before shipment. There is no need to modify block parameters unless the NVRAM is corrupted.

Refer to the *Programmer’s Reference Guide* (part number V1600-1A/PG) for the actual location and other information about the Board Information Block.

Refer to the *PPCBug Firmware Package User's Manual* (part number PPCBUGA1/UM) for a description of **CNFG** and examples.

ENV - Set Environment

Use the **ENV** command to view and/or configure interactively all PPCBug operational parameters that are kept in Non-Volatile RAM (NVRAM).

Refer to the *PPCBug Firmware Package User's Manual* for a description of the use of **ENV**. Additional information on registers in the VMEchip2 and VME2PCI ASICs that affect these parameters is contained in your PowerPC board programmer's reference guide.

Listed and described below are the parameters that you can configure using **ENV**. The default values shown were those in effect when this publication went to print.

Configuring the PPCBug Parameters

The parameters that can be configured using **ENV** are:

```
Bug or System environment [B/S] = S?
```

B Bug is the mode where no system type of support is displayed. However, system-related items are still available.

S System is the standard mode of operation, and is the default mode if NVRAM should fail. System mode is defined in the *PPCBug Firmware Package User's Manual*. (Default)

```
Field Service Menu Enable [Y/N] = Y?
```

Y Display the field service menu. (Default)

N Do not display the field service menu.

```
Remote Start Method Switch [G/M/B/N] = B?
```

The Remote Start Method Switch is used when the MVME1603/MVME1604 is cross-loaded from another VME-based CPU, to start execution of the cross-loaded program.

G Use the Global Control and Status Register (GCSR, located in the VMEchip2 on PowerPC board series modules) to pass and start execution of the cross-loaded program.

M Use the Multiprocessor Control Register (MPCR) in shared RAM to pass and start execution of the cross-loaded program.

B Use both the GCSR and the MPCR methods to pass and start execution of the cross-loaded program. (Default)

N Do not use any Remote Start Method.

```
Probe System for Supported I/O Controllers [Y/N] = Y?
```

Y Accesses will be made to the appropriate system buses (e.g., VMEbus, local MPU bus) to determine the presence of supported controllers. (Default)

N Accesses will not be made to the VMEbus to determine the presence of supported controllers.

```
Auto-Initialize of NVRAM Header Enable [Y/N] = Y?
```

Y NVRAM (PReP partition) header space will be initialized automatically during board initialization. (Default)

N NVRAM header space will not be initialized automatically during board initialization.

```
Network PReP-Boot Mode Enable [Y/N] = Y?
```

Y Enable PReP-style network booting (same boot image from a network interface as from a mass storage device). (Default)

N Do not enable PReP-style network booting.

```
Negate VMEbus SYSFAIL* Always [Y/N] = N?
```

Y Negate the VMEbus SYSFAIL* signal during board initialization.

N Negate the VMEbus SYSFAIL* signal after successful completion or entrance into the bug command monitor. (Default)

```
Local SCSI Bus Reset on Debugger Startup [Y/N] = Y?
```

Y Local SCSI bus is reset on debugger setup. (Default)

N Local SCSI bus is not reset on debugger setup.

```
Local SCSI Bus Negotiations Type [A/S/N] = A?
```

A Asynchronous SCSI bus negotiation. (Default)

S Synchronous SCSI bus negotiation.

N None.

```
Local SCSI Data Bus Width [W/N] = N?
```

W Wide SCSI (16-bit bus).

N Narrow SCSI (8-bit bus). (Default)

```
NVRAM Bootlist (GEV.fw-boot-path) Boot Enable [Y/N] = Y?
```

Y Give boot priority to devices defined in the *fw-boot-path* global environment variable (GEV). (Default)

N Do not give boot priority to devices listed in the *fw-boot-path* GEV.

Note When enabled, the GEV (Global Environment Variable) boot takes priority over all other boots, including Autoboot and Network Boot.

```
NVRAM Bootlist (GEV.fw-boot-path) Boot at power-up only [Y/N] = N?
```

Y Give boot priority to devices defined in the *fw-boot-path* GEV at power-up reset only.

N Give power-up boot priority to devices listed in the *fw-boot-path* GEV at any reset. (Default)

```
NVRAM Bootlist (GEV.fw-boot-path) Boot Abort Delay = 5?
```

The time in seconds that a boot from the NVRAM boot list will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds. (Default = 5 seconds)

```
Auto Boot Enable [Y/N]   = Y?
```

Y The Autoboot function is enabled. (Default)

N The Autoboot function is disabled.

```
Auto Boot at power-up only [Y/N] = N?
```

Y Autoboot is attempted at power-up reset only.

N Autoboot is attempted at any reset.(Default)

```
Auto Boot Scan Enable [Y/N]   = Y?
```

Y If Autoboot is enabled, the Autoboot process attempts to boot from devices specified in the scan list (e.g., FDISK/CDROM/TAPE/HDISK). (Default)

N If Autoboot is enabled, the Autoboot process uses the Controller LUN and Device LUN to boot.

```
Auto Boot Scan Device Type List = FDISK/CDROM/TAPE/HDISK?
```

The listing of boot devices displayed if the Autoboot Scan option is enabled. If you modify the list, follow the format shown above (uppercase letters, using forward slash as separator).

```
Auto Boot Controller LUN   = 00?
```

Refer to the *PPCBug Firmware Package User's Manual* for a listing of disk/tape controller modules currently supported by PPCBug. (Default = $00)

```
Auto Boot Device LUN    = 00?
```

Refer to the *PPCBug Firmware Package User's Manual* for a listing of disk/tape devices currently supported by PPCBug. (Default = $00)

```
Auto Boot Partition Number = 00?
```

Which disk "partition" is to be booted, as specified in the PowerPC Reference Platform (PRP) specification. If set to zero, the firmware will search the partitions in order (1, 2, 3, 4) until it finds the first "bootable" partition. That is then the partition that will be booted. Other acceptable values are 1, 2, 3, or 4. In these four cases, the partition specified will be booted without searching.

```
Auto Boot Abort Delay = 7?
```

The time in seconds that the Autoboot sequence will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds. (Default = 7 seconds)

```
Auto Boot Default String [NULL for an empty string] = ?
```

You may specify a string (filename) which is passed on to the code being booted. The maximum length of this string is 16 characters. (Default = null string)

```
ROM Boot Enable [Y/N] = N?
```

Y The ROMboot function is enabled.

N The ROMboot function is disabled. (Default)

```
ROM Boot at power-up only [Y/N] = Y?
```

Y ROMboot is attempted at power-up only. (Default)

N ROMboot is attempted at any reset.

```
ROM Boot Enable search of VMEbus [Y/N] = N?
```

Y VMEbus address space, in addition to the usual areas of memory, will be searched for a ROMboot module .

N VMEbus address space will not be accessed by ROMboot. (Default)

```
ROM Boot Abort Delay = 5?
```

The time in seconds that the ROMboot sequence will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds. (Default = 5 seconds)


```
ROM Boot Direct Starting Address = FFF00000?
```

The first location tested when PPCBug searches for a ROMboot module. (Default = $FFF00000)

```
ROM Boot Direct Ending Address = FFFFFFFC?
```

The last location tested when PPCBug searches for a ROMboot module. (Default = $FFFFFFFC)

```
Network Auto Boot Enable [Y/N] = Y?
```

Y The Network Auto Boot (NETboot) function is enabled. (Default)

N The NETboot function is disabled.

```
Network Auto Boot at power-up only [Y/N] = N?
```

Y NETboot is attempted at power-up reset only.

N NETboot is attempted at any reset. (Default)

```
Network Auto Boot Controller LUN = 00?
```

Refer to the *PPCBug Firmware Package User's Manual* for a listing of disk/tape controller modules currently supported by PPCBug. (Default = $00)

```
Network Auto Boot Device LUN = 00?
```

Refer to the *PPCBug Firmware Package User's Manual* for a listing of disk/tape controller modules currently supported by PPCBug. (Default = $00)

```
Network Auto Boot Abort Delay = 5?
```

The time in seconds that the NETboot sequence will delay before starting the boot. The purpose for the delay is to allow you the option of stopping the boot by use of the **BREAK** key. The time value is from 0-255 seconds. (Default = 5 seconds)

```
Network Auto Boot Configuration Parameters Offset (NVRAM) =
00001000?
```

The address where the network interface configuration parameters are to be saved/retained in NVRAM; these parameters are the necessary parameters to perform an unattended network boot. A typical offset might be $1000, but this value is application-specific. (Default = $00001000)

Caution

If you use the NIOT debugger command, these parameters need to be saved somewhere in the offset range $00000000 through $00000FFF. The NIOT parameters do not exceed 128 bytes in size. The setting of this ENV pointer determines their location. If you have used the same space for your own program information or commands, they will be overwritten and lost.

You can relocate the network interface configuration parameters in this space by using the ENV command to change the Network Auto Boot Configuration Parameters offset from its default of $00001000 to the value you need to be clear of your data within NVRAM.

```
Memory Size Enable [Y/N] = Y?
```

Y Memory will be sized for Self Test diagnostics. (Default)

N Memory will not be sized for Self Test diagnostics.

```
Memory Size Starting Address = 00000000?
```

The default Starting Address is $00000000.

```
Memory Size Ending Address = 02000000?
```

The default Ending Address is the calculated size of local memory. If the memory start is changed from $00000000, this value will also need to be adjusted.

```
DRAM Speed in NANO Seconds = 60?
```

The default setting for this parameter will vary depending on the speed of the DRAM memory parts installed on the board. The default is set to the slowest speed found on the available banks of DRAM memory.

```
ROM First Access Length (0 - 31) = 10?
```

This is the value programmed into the MPC105 “ROMFAL” field (Memory Control Configuration Register 8: bits 23-27) to indicate the number of clock cycles used in accessing the ROM. The lowest allowable ROMFAL setting is $00; the highest allowable is $1F. The value to enter depends on processor speed; refer to your *Processor/Memory Mezzanine Module User’s Manual* for appropriate values. The default value varies according to the system’s bus clock speed.

```
ROM Next Access Length (0 - 15) = 0?
```

The value programmed into the MPC105 “ROMNAL” field (Memory Control Configuration Register 8: bits 28-31) to represent wait states in access time for nibble (or burst) mode ROM accesses. The lowest allowable ROMNAL setting is $0; the highest allowable is $F. The value to enter depends on processor speed; refer to your *Processor/Memory Mezzanine Module User’s Manual* for appropriate values. The default value varies according to the system’s bus clock speed.

```
DRAM Parity Enable [On-Detection/Always/Never - O/A/N] = O?
```

O DRAM parity is enabled upon detection. (Default)

A DRAM parity is always enabled.

N DRAM parity is never enabled.

```
L2 Cache Parity Enable [On-Detection/Always/Never - O/A/N] = O?
```

O L2 Cache parity is enabled upon detection. (Default)

A L2 Cache parity is always enabled.

N L2 Cache parity is never enabled.

```
PCI Interrupts Route Control Registers (PIRQ0/1/2/3) = 0A0B0E0F?
```

Initializes the PIRQx (PCI Interrupts) route control registers in the IBC (PCI/ISA bus bridge controller). The **ENV** parameter is a 32-bit value that is divided by 4 to yield the values for route control registers PIRQ0/1/2/3. The default is determined by system type. For details on PCI/ISA interrupt assignments and for suggested values to enter for this parameter, refer to the *Maskable Interrupts* section of Chapter 4 in the *MVME1603/ MVME1604 Programmer’s Reference Guide*.

Configuring the VMEbus Interface

ENV asks the following series of questions to set up the VMEbus interface for the MVME1603/MVME1604 series modules. To perform this configuration, you should have a working knowledge of the VME2PCI and VMEchip2 ASICs as described in the *Programmer's Reference Guide*.

```
VME2PCI Master Master Enable [Y/N] = Y?
```

Y Set up and enable the VMEbus Interface (Default)

N Do not set up or enable the VMEbus Interface.


```
VME2PCI Slave Enable #1 [Y/N] = Y?
```

Y Set up and enable VME2PCI Slave Address Decoder #1 (Default)

N Do not set up or enable VME2PCI Slave Address Decoder #1.

```
VME2PCI Slave Starting Address #1 = 01000000?
```

Controls the starting address of the first PCI Memory Space for the VME2PCI's slave interface. PCI memory accesses within the range of this starting address and its associated ending address are passed on to the VMEchip2, after modification by the address offset value. Only the upper 16 bits of this address are significant. (Default = $01000000)

```
VME2PCI Slave Ending Address #1 = 1FFFFFFF?
```

Controls the ending address of the first PCI Memory Space for the VME2PCI's slave interface. Only the upper 16 bits of this address are significant. (Default = $1FFFFFFF)

```
VME2PCI Slave Address Offset #1 = 00000000?
```

Used in translating the most significant 16 bits of the address to be presented to the VMEchip2 from the PCI bus. The address presented is equal to the sum of PCI address (bits 31-16) and the value of this register (bits 31-16). Bits 15-00 will be zero. (Default = $00000000)

```
VME2PCI Slave Enable #2 [Y/N] = Y?
```

Y Set up and enable VME2PCI Slave Address Decoder #2. (Default)

N Do not set up or enable VME2PCI Slave Address Decoder #2.


```
VME2PCI Slave Starting Address #2 = 20000000?
```

Controls the starting address of the second PCI Memory Space for the VME2PCI's slave interface. PCI memory accesses within the range of this starting address and its associated ending address are passed on to the VMEchip2, after modification by the address offset value. Only the upper 16 bits of this address are significant. (Default = $20000000)

```
VME2PCI Slave Ending Address #2 = 2FFFFFFF?
```

Controls the ending address of the second PCI Memory Space for the VME2PCI's slave interface. Only the upper 16 bits of this address are significant. (Default = $2FFFFFFF)

```
VME2PCI Slave Address Offset #2 = D0000000?
```

Used in translating the most significant 16 bits of the address to be presented to the VMEchip2 from the PCI bus. The address presented is equal to the sum of PCI address (bits 31-16) and the value of this register (bits 31-16). Bits 15-00 will be zero. (Default = $D0000000)

Slave Address Decoders

The slave address decoders are used to allow another VMEbus master to access a local resource of the MVME1603/1604. There are two slave address decoders set. They are set up as follows:

```
Slave Enable #1 [Y/N] = Y?
```

Y Yes, set up and enable the Slave Address Decoder #1. (Default)

N Do not set up and enable the Slave Address Decoder #1.

```
Slave Starting Address #1 = 00000000?
```

Base address of the local resource that is accessible by the VMEbus. (Default = $0, base of local memory)


```
Slave Ending Address #1 = 03FFFFFF?
```

Ending address of the local resource that is accessible by the VMEbus. (Default = end of calculated memory)

```
Slave Address Translation Address #1 = 80000000?
```

Enables the VMEbus address and the local address to differ. The value in this register is the base address of the local resource associated with the starting and ending address selection from the previous questions. (Default = $80000000)

```
Slave Address Translation Select #1 = FE000000?
```

Defines which bits of the address are significant. A logical 1 indicates significant address bits, and a logical 0 is nonsignificant. (Default = $FE000000)

```
Slave Control #1 = 03FF?
```

Defines the access restriction for the address space defined with this slave address decoder. (Default = $03FF)

```
Slave Enable #2 [Y/N] = N?
```

Y Yes, set up and enable the Slave Address Decoder #2.

N Do not set up and enable the Slave Address Decoder #2. (Default)

```
Slave Starting Address #2 = 00000000?
```

Base address of the local resource that is accessible by the VMEbus. (Default = $00000000)

```
Slave Ending Address #2 = 00000000?
```

Ending address of the local resource that is accessible by the VMEbus. (Default = $00000000)

```
Slave Address Translation Address #2 = 00000000?
```

Enables the VMEbus address and the local address to differ. The value in this register is the base address of the local resource associated with the starting and ending address selection from the previous questions. (Default = $00000000)


```
Slave Address Translation Select #2 = 00000000?
```

Defines which bits of the address are significant. A logical 1 indicates significant address bits, and a logical 0 is nonsignificant. (Default = $00000000)

```
Slave Control #2 = 0000?
```

Defines the access restriction for the address space defined with this slave address decoder. (Default = $0000)

```
Master Enable #1 [Y/N] = Y?
```

Y Yes, set up and enable the Master Address Decoder #1. (Default)

N Do not set up and enable the Master Address Decoder #1.

```
Master Starting Address #1 = 00000000
```

The base address of the VMEbus resource that is accessible from the local bus. (Default = $00000000, end of calculated local memory)

```
Master Ending Address #1 = 1FFFFFFF?
```

The ending address of the VMEbus resource that is accessible from the local bus. (Default = $1FFFFFFF)

```
Master Control #1 = 0D?
```

Defines the access characteristics for the address space defined with this master address decoder. (Default = $0D)


```
Master Enable #2 [Y/N] = N?
```

Y Yes, set up and enable the Master Address Decoder #2.

N Do not set up and enable the Master Address Decoder #2. (Default)

```
Master Starting Address #2 = 00000000?
```

Base address of the VMEbus resource that is accessible from the local bus. (Default = $00000000)

```
Master Ending Address #2 = 00000000?
```

Ending address of the VMEbus resource that is accessible from the local bus. (Default = $00000000)

```
Master Control #2 = 00?
```

Defines the access characteristics for the address space defined with this master address decoder. (Default = $00)

```
Master Enable #3 [Y/N] = N?
```

Y Yes, set up and enable the Master Address Decoder #3.

N Do not set up and enable the Master Address Decoder #3. (Default)

```
Master Starting Address #3 = 00000000?
```

Base address of the VMEbus resource that is accessible from the local bus. (Default = $00000000)

```
Master Ending Address #3 = 00000000?
```

Ending address of the VMEbus resource that is accessible from the local bus. (Default = $00000000)

```
Master Control #3 = 00?
```

Defines the access characteristics for the address space defined with this master address decoder. (Default = $00)


```
Master Enable #4 [Y/N] = N?
```

Y Yes, set up and enable the Master Address Decoder #4.

N Do not set up and enable the Master Address Decoder #4. (Default)

```
Master Starting Address #4 = 00000000?
```

Base address of the VMEbus resource that is accessible from the local bus. (Default = $00000000)

```
Master Ending Address #4 = 00000000?
```

Ending address of the VMEbus resource that is accessible from the local bus. (Default = $00000000)

```
Master Address Translation Address #4 = 00000000?
```

Enables the VMEbus address and the local address to differ. The value in this register is the base address of the VMEbus resource associated with the starting and ending address selection from the previous questions. (Default = $00000000)

```
Master Address Translation Select #4 = 00000000?
```

Defines which bits of the address are significant. A logical 1 indicates significant address bits, and a logical 0 is nonsignificant. (Default = $00000000)


```
Master Control #4 = 00?
```

Defines the access characteristics for the address space defined with this master address decoder. (Default = $00)

```
Short I/O (VMEbus A16) Enable [Y/N] = Y?
```

Y Yes, enable the Short I/O Address Decoder. (Default)

N Do not enable the Master Address Decoder.

```
Short I/O (VMEbus A16) Control = 01?
```

Defines the access characteristics for the address space defined with the Short I/O address decoder. (Default = $01)

```
F-Page (VMEbus A24) Enable [Y/N] = Y?
```

Y Yes, enable the F-Page Address Decoder. (Default)

N Do not enable the F-Page Address Decoder.

```
F-Page (VMEbus A24) Control = 02?
```

Defines the access characteristics for the address space defined with the F-Page address decoder. (Default = $02)

```
VMEC2 Vector Base #1 = 06?
```

Defines the base interrupt vector for the component specified. (Default: VMEchip2 Vector 1 = $06)

```
VMEC2 Vector Base #2 = 07?
```

Defines the base interrupt vector for the component specified. (Default: VMEchip2 Vector 2 = $07)

`VMEC2 GCSR Group Base Address = 00?`

Defines the group address ($FFFF*xx*00) in Short I/O for this board. (Default = $00)

`VMEC2 GCSR Board Base Address = 00?`

Specifies the base address ($FFFF00*x*0) in Short I/O for this board. (Default = $00)

`VMEbus Global Time Out Code = 02?`

Controls the VMEbus time-out interval when the MVME1603/ 1604 is system controller. (Default = $02, 256 microseconds)

`VMEbus Access Time Out Code = 02?`

This controls the local-bus-to-VMEbus access time-out interval. (Default = $02, 32 milliseconds)

Related Documentation A

Motorola Computer Group Documents

This product has an installation and use manual which provides the necessary information to properly install and operate the board. This manual along with additional product documentation may be ordered by using any of the following methods:

- Contacting your local Motorola sales office.
- Accessing the World Wide Web site **http//: www.mcg.mot.com** (listed on the back cover of this and other MCG manuals) and selecting “Product Literature”.
- (USA and Canada only) - Contacting the Literature Center via phone or fax at the numbers listed under *Product Literature* at MCG’s World Wide Web site (above).

Any supplements issued for a specific revision of a manual or guide are furnished with that document. The “type” and “revision level” of a specific manual are indicated by the last three characters of the document number, such as “/IH2” (the second revision of an installation manual); a supplement bears the same number as a manual but has two additional characters that indicate the revision level of the supplement, for example “/IH2A1” (the first supplement to the second edition of the installation manual).

Table A-1. Motorola Computer Group Documents

Document Title	Publication Number
MVME1603/MVME1604 Single Board Computer Installation and Use*	V1600-1A/IH
MVME1603/MVME1604 Single Board Computer Programmer's Reference Guide*	V1600-1A/PG
PM603/PM604 Processor/Memory Mezzanine Module and RAM104 DRAM Memory Module User's Manual*	PM603A/UM
PPCBug Firmware Package User's Manual (Parts 1 and 2)*	PPCBUGA1/UM PPCBUGA2/UM
PPC1Bug Diagnostics Manual*	PPC1DIAA/UM
MVME712M Transition Module and P2 Adapter Board User's Manual	MVME712M/D
MVME760 Transition Module User's Manual	VME760A/UM
SIM705 Serial Interface Module Installation Guide	SIM705A/IH

Note Motorola documents marked with a ***** in the above list can be purchased as a set under part number **LK-V1600-1**.

Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. As an additional help, a source for the listed document is also provided. Please note that in many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

To further assist your development effort, Motorola has collected some of the non-Motorola documents in this list from the suppliers. This bundle can be ordered as part number **68-PCIKIT**.

Table A-2. Manufacturers' Documents

Document Title and Source	Publication Number
PowerPC 603™ RISC Microprocessor Technical Summary Motorola Literature and Printing Distribution Services P.O. Box 20924 Phoenix, Arizona 85036-0924 Telephone: (602) 994-6561 FAX: (602) 994-6430	MPC603/D
PowerPC 603™ RISC Microprocessor User's Manual Motorola Literature and Printing Distribution Services P.O. Box 20924 Phoenix, Arizona 85036-0924 Telephone: (602) 994-6561 FAX: (602) 994-6430 OR IBM Microelectronics Mail Stop A25/862-1 PowerPC Marketing 1000 River Street Essex Junction, Vermont 05452-4299 Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 FAX: 1-800-POWERfax FAX: 1-800-769-3732	MPC603UM/AD MPR603UMU-01

Table A-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
PowerPC 604™ RISC Microprocessor User's Manual Motorola Literature and Printing Distribution Services P.O. Box 20924 Phoenix, Arizona 85036-0924 Telephone: (602) 994-6561 FAX: (602) 994-6430 OR IBM Microelectronics Mail Stop A25/862-1 PowerPC Marketing 1000 River Street Essex Junction, Vermont 05452-4299 Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 FAX: 1-800-POWERfax FAX: 1-800-769-3732	MPC604UM/AD MPR604UMU-01
MPC105 PCI Bridge/Memory Controller User's Manual Motorola Literature and Printing Distribution Services P.O. Box 20924 Phoenix, Arizona 85036-0924 Telephone: (602) 994-6561 FAX: (602) 994-6430	MPC105UM/AD
PowerPC™ Microprocessor Family: The Programming Environments Motorola Literature and Printing Distribution Services P.O. Box 20924 Phoenix, Arizona 85036-0924 Telephone: (602) 994-6561 FAX: (602) 994-6430 OR IBM Microelectronics Mail Stop A25/862-1 PowerPC Marketing 1000 River Street Essex Junction, Vermont 05452-4299 Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 FAX: 1-800-POWERfax FAX: 1-800-769-3732	MPCFPE/AD MPRPPCFPE-01

Table A-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
Alpine™ VGA Family - CL-GD544X Technical Reference Manual Fourth Edition Cirrus Logic, Inc. (or nearest Sales Office) 3100 West Warren Avenue Fremont, California 94538-6423 Telephone: (510) 623-8300 FAX: (510) 226-2180	385439-004
DECchip 21040 Ethernet LAN Controller for PCI Hardware Reference Manual Digital Equipment Corporation Maynard, Massachusetts DECchip Information Line Telephone (United States and Canada): 1-800-332-2717 TTY (United States only): 1-800-332-2515 Telephone (outside North America): +1-508-568-6868	EC-N0752-72
PC87303VUL (Super I/O™ Sidewinder Lite) Floppy Disk Controller, Keyboard Controller, Real-Time Clock, Dual UARTs, IEEE 1284 Parallel Port, and IDE Interface National Semiconductor Corporation Customer Support Center (or nearest Sales Office) 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, California 95052-8090 Telephone: 1-800-272-9959	PC87303VUL
PC87323VF (Super I/O™ Sidewinder) Floppy Disk Controller, Keyboard Controller, Real-Time Clock, Dual UARTs, IEEE 1284 Parallel Port, and IDE Interface National Semiconductor Corporation Customer Support Center (or nearest Sales Office) 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, California 95052-8090 Telephone: 1-800-272-9959	PC87323VF

Table A-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
M48T18 CMOS 8K x 8 TIMEKEEPER™ SRAM Data Sheet SGS-Thomson Microelectronics Group Marketing Headquarters (or nearest Sales Office) 1000 East Bell Road Phoenix, Arizona 85022 Telephone: (602) 867-6100	M48T18
DS1643 Nonvolatile Timekeeping RAM Data Manual Dallas Semiconductor 4401 South Beltwood Parkway Dallas, Texas 75244-3292	DS1643/ DS1643LPM
82378 System I/O (SIO) PCI-to-ISA Bridge Controller Intel Corporation Literature Sales P.O. Box 7641 Mt. Prospect, Illinois 60056-7641 Telephone: 1-800-548-4725	290473-003
SYM 53CXX (was NCR 53C8XX) Family PCI-SCSI I/O Processors Programming Guide Symbios Logic Inc. 1731 Technology Drive, suite 600 San Jose, CA95110 Telephone: (408) 441-1080 Hotline: 1-800-334-5454	J10931I
SCC (Serial Communications Controller) User's Manual (for Z85230 and other Zilog parts) Zilog, Inc. 210 East Hacienda Ave., mail stop C1-0 Campbell, California 95008-6600 Telephone: (408) 370-8016 FAX: (408) 370-8056	DC-8293-02

Table A-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
Z8536 CIO Counter/Timer and Parallel I/O Unit Product Specification and User's Manual (in Z8000® Family of Products Data Book) Zilog, Inc. 210 East Hacienda Ave., mail stop C1-0 Campbell, California 95008-6600 Telephone: (408) 370-8016 FAX: (408) 370-8056	DC-8319-00
CS4231 Parallel Interface, Multimedia Audio Codec Data Sheet Crystal Semiconductor Corporation 4210 South Industrial Drive P.O. Box 17847 Austin, Texas 78744-7847 Telephone: 1-800-888-5016 Telephone: (512) 445-7222 FAX: (512) 445-7581	DS111PP4
CSB4231/4248 Evaluation Board Data Sheet Crystal Semiconductor Corporation 4210 South Industrial Drive P.O. Box 17847 Austin, Texas 78744-7847 Telephone: 1-800-888-5016 Telephone: (512) 445-7222 FAX: (512) 445-7581	DS111DB4
Award Classic KB42 Keyboard Controller Firmware for the National Semiconductor PC87323VUL-IAB SuperI/O™ Device Award Software International, Inc. Sales and Marketing 777 E. Middlefield Road Mountain View, California 94043 Telephone: (415) 968-4433	Award Classic KB42

Related Specifications

For additional information, refer to the following table for related specifications. As an additional help, a source for the listed document is also provided. Please note that in many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

Table A-3. Related Specifications

Document Title and Source	Publication Number
ANSI Small Computer System Interface-2 (SCSI-2), Draft Document Global Engineering Documents 15 Inverness Way East Englewood, CO 80112-5704 Telephone: 1-800-854-7179 Telephone: (303) 792-2181	X3.131.1990
ANSI Std X3T9.2, 1994 AT Attachment Interface for Disk Drives Global Engineering Documents 15 Inverness Way East Englewood, CO 80112-5704 Telephone: 1-800-854-7179 Telephone: (303) 792-2181	ANSI X3.221
Bidirectional Parallel Port Interface Specification Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	IEEE Standard 1284
IEEE - Common Mezzanine Card Specification (CMC) Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	P1386 Draft 2.0

Table A-3. Related Specifications (Continued)

Document Title and Source	Publication Number
IEEE - PCI Mezzanine Card Specification (PMC) Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	P1386.1 Draft 2.0
IEEE Standard for Local Area Networks: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	IEEE 802.3
Information Technology - Local and Metropolitan Networks - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications Global Engineering Documents 15 Inverness Way East Englewood, CO 80112-5704 Telephone: 1-800-854-7179 Telephone: (303) 792-2181 *(This document can also be obtained through the national standards body of member countries.)*	ISO/IEC 8802-3
Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange (EIA-232-D) Electronic Industries Association Engineering Department 2001 Eye Street, N.W. Washington, D.C. 20006	ANSI/EIA-232-D Standard

Table A-3. Related Specifications (Continued)

Document Title and Source	Publication Number
Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.0 PCI Special Interest Group P.O. Box 14070 Portland, Oregon 97214-4070 Marketing/Help Line Telephone: (503) 696-6111 Document/Specification Ordering Telephone: 1-800-433-5177or (503) 797-4207 FAX: (503) 234-6762	PCI Local Bus Specification
PowerPC Reference Platform (PRP) Specification, Third Edition, Version 1.0, Volumes I and II International Business Machines Corporation Power Personal Systems Architecture 11400 Burnet Rd. Austin, TX 78758-3493 Document/Specification Ordering Telephone: 1-800-PowerPC Telephone: 1-800-769-3772 Telephone: 708-296-9332	MPR-PPC-RPU-02
VME64 Specification VITA (VMEbus International Trade Association) 7825 E. Gelding Drive, Suite 104 Scottsdale, Arizona 85260-3415 Telephone: (602) 951-8866 FAX: (602) 951-0720 **NOTE:** An earlier version of this specification is available as: Versatile Backplane Bus: VMEbus Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333 OR Microprocessor system bus for 1 to 4 byte data Bureau Central de la Commission Electrotechnique Internationale 3, rue de Varembé Geneva, Switzerland	ANSI/VITA 1-1994 ANSI/IEEE Standard 1014-1987 IEC 821 BUS

Specifications

Table B-1 lists the general specifications for the MVME1600-001 and MVME1600-011 base boards. The subsequent sections detail cooling requirements and FCC compliance.

A complete functional description of the MVME1600-001 and MVME1600-011 base boards appears in Chapter 2. Specifications for the mezzanine modules (processor/memory, DRAM, and optional PCI mezzanine) can be found in the documentation for those modules.

Table B-1. MVME1600-001/MVME1600-011 Specifications

Characteristics	Specifications
Power requirements (Excluding Processor/ Memory mezzanine, transition module, keyboard, mouse)	+5Vdc (±5%), 2A typical, 3A maximum +12Vdc (±5%), 100mA maximum –12Vdc (±5%), 100mA maximum (in MVME1600-011; no –12Vdc in MVME1600-001)
Operating temperature	0°C to 55°C entry air with forced-air cooling (refer to *Cooling Requirements* section)
Storage temperature	–40°C to +85° C
Relative humidity	5% to 90% (non-condensing)
Physical dimensions Base board only Height Depth Base board with front panel and connectors Height Depth Front panel width With PM603 module With PM604 module	Double-high VMEboard 9.2 in. (233 mm) 6.3 in. (160 mm) 10.3 in. (262 mm) 7.4 in. (188 mm) 0.8 in. (20mm) 1.6 in. (40mm)

B

Cooling Requirements

The Motorola MVME1603/1604 family of Single Board Computers is specified, designed, and tested to operate reliably with an incoming air temperature range from 0° to 55° C (32° to 131° F) with forced air cooling of the entire assembly (base board and modules) at a velocity typically achievable by using a 100 CFM axial fan.

Temperature qualification is performed in a standard Motorola VMEsystem chassis. Twenty-five-watt load boards are inserted in two card slots, one on each side, adjacent to the board under test, to simulate a high power density system configuration. An assembly of three axial fans, rated at 100 CFM per fan, is placed directly under the VME card cage.

The incoming air temperature is measured between the fan assembly and the card cage, where the incoming airstream first encounters the module under test. Test software is executed as the module is subjected to ambient temperature variations. Case temperatures of critical, high power density integrated circuits are monitored to ensure component vendors' specifications are not exceeded.

While the exact amount of airflow required for cooling depends on the ambient air temperature and the type, number, and location of boards and other heat sources, adequate cooling can usually be achieved with 10 CFM and 490 LFM flowing over the module. Less airflow is required to cool the module in environments having lower maximum ambients. Under more favorable thermal conditions, it may be possible to operate the module reliably at higher than 55° C with increased airflow.

It is important to note that there are several factors, in addition to the rated CFM of the air mover, which determine the actual volume and speed of air flowing over a module.

EMC Compliance

The MVME1603/MVME1604 Single Board Computer was tested in an EMC-compliant chassis and meets the requirements for EN55022 Class B equipment. Compliance was achieved under the following conditions:

- Shielded cables on all external I/O ports.
- Cable shields connected to earth ground via metal shell connectors bonded to a conductive module front panel.
- Conductive chassis rails connected to earth ground. This provides the path for connecting shields to earth ground.
- Front panel screws properly tightened.

For minimum RF emissions, it is essential that the conditions above be implemented. Failure to do so could compromise the EMC compliance of the equipment containing the module.

Serial Interconnections C

Introduction

As described in previous chapters of this manual, the MVME1603/MVME1604 serial communications interface has four ports. Two of them are combined synchronous/asynchronous ports; the other two are asynchronous only. Between the MVME1600-001 and MVME1600-011 base boards, some differences exist in the implementation of the four ports. The differences are summarized in the following table.

Table C-1. MVME1600-001/MVME1600-011 Serial Ports

Base Board	Serial Interface
MVME1600-001	2 asynchronous ports (EIA-232-D DTE) via P2 and MVME760 transition module 2 synchronous/asynchronous ports (EIA-232-D or EIA-530 DCE/DTE) via P2 and MVME760 transition module
MVME1600-011	2 asynchronous ports (EIA-232-D DCE/DTE) via P2 and MVME712M transition module 2 synchronous/asynchronous ports (EIA-232-D DCE/DTE) via P2 and MVME712M *or* via front panel. Front panel I/O (DTE only) gives full sync/async functionality on both ports; MVME712M I/O makes port 3 *async only.*

Asynchronous Serial Ports

The MVME1603/MVME1604 uses a PC87303 ISASIO chip from National Semiconductor to implement the two asynchronous serial ports (in addition to the disk drive controller, parallel I/O, and keyboard/mouse interface).

The asynchronous ports provided by the ISASIO device are routed through P2 and the associated transition module. The TTL-level signals from the ISASIO chip are buffered through TTL drivers and series resistors. The EIA-232-D drivers and receivers that complete the asynchronous serial interface are located on the MVME760 (for the MVME1600-001 base board) or MVME712M (for the MVME1600-011 base board) transition module.

The MVME1603/MVME1604 hardware supports asynchronous serial baud rates of 110B/s to 38.4KB/s. For detailed programming information, refer to the PCI and ISA bus discussions in the *MVME1603/MVME1604 Single Board Computer Programmer's Reference Guide* and to the vendor documentation for the ISASIO device.

Synchronous Serial Ports

The MVME1603/MVME1604 uses a Zilog Z85230 ESCC (Enhanced Serial Communications Controller) with a 10MHz clock to implement the two synchronous/asynchronous serial communications ports, which for the MVME1600-001 base board are routed through P2 and for the MVME1600-011 base board are routed through the front panel as well as P2. The Z85230 handles both synchronous (SDLC/HDLC) and asynchronous protocols. The hardware supports asynchronous serial baud rates of 110B/s to 38.4KB/s and synchronous baud rates of up to 2.5MB/s.

Each port supports the CTS, DCD, RTS, and DTR control signals, as well as the TxD and RxD transmit/receive data signals and TxC/RxC synchronous clock signals. Since not all modem control lines are available in the Z85230, a Z8536 CIO device is used to provide the missing modem lines.

In addition to complementing the Z85230 ESCC by supplying modem control lines not present on the Z85230 ESCC, the Z8536 CIO device provides a way to request the module ID of the synchronous/asynchronous serial ports on the transition module. Refer to the Z8536 data sheet and to the *MVME1603/MVME1604 Single Board Computer Programmer's Reference Guide* for further information.

EIA-232-D Connections

The EIA-232-D standard defines the electrical and mechanical aspects of this serial interface. The interface employs unbalanced (single-ended) signaling and is generally used with DB25 connectors, although other connector styles (e.g., DB9 and RJ45) are sometimes used as well.

Table C-2 lists the standard EIA-232-D interconnections. Not all pins listed in the table are necessary in every application.

To interpret the information correctly, remember that the EIA-232-D serial interface was developed to connect a terminal to a modem. Serial data leaves the sending device on a Transmit Data (TxD) line and arrives at the receiving device on a Receive Data (RxD) line. When computing equipment is interconnected without modems, one of the units must be configured as a terminal (data terminal equipment: DTE) and the other as a modem (data circuit-terminating equipment: DCE). Since computers are normally configured to work with terminals, they are said to be configured as a modem in most cases.

Table C-2. EIA-232-D Interconnect Signals

Pin Number	Signal Mnemonic	Signal Name and Description
1		Not used.
2	TxD	**Transmit Data**. Data to be transmitted; input to modem from terminal.
3	RxD	**Receive Data**. Data which is demodulated from the receive line; output from modem to terminal.
4	RTS	**Request To Send**. Input to modem from terminal when required to transmit a message. With RTS off, the modem carrier remains off. When RTS is turned on, the modem immediately turns on the carrier.
5	CTS	**Clear To Send**. Output from modem to terminal to indicate that message transmission can begin. When a modem is used, CTS follows the off-to-on transition of RTS after a time delay.
6	DSR	**Data Set Ready**. Output from modem to terminal to indicate that the modem is ready to send or receive data.
7	SG	**Signal Ground**. Common return line for all signals at the modem interface.
8	DCD	**Data Carrier Detect**. Output from modem to terminal to indicate that a valid carrier is being received.
9-14		Not used.

Table C-2. EIA-232-D Interconnect Signals (Continued)

Pin Number	Signal Mnemonic	Signal Name and Description
15	TxC	**Transmit Clock** (DCE). Output from modem to terminal; clocks data from the terminal to the modem.
16		Not used.
17	RxC	**Receive Clock**. Output from terminal to modem; clocks input data from the terminal to the modem.
18, 19		Not used.
20	DTR	**Data Terminal Ready**. Input to modem from terminal; indicates that the terminal is ready to send or receive data.
21		Not used.
22	RI	**Ring Indicator**. Output from modem to terminal; indicates that an incoming call is present. The terminal causes the modem to answer the phone by carrying DTR true while RI is active..
23		Not used.
24	TxC	**Transmit Clock** (DTE). Input to modem from terminal; same function as TxC on pin 15.
25	BSY	**Busy**. Input to modem from terminal; a positive EIA signal applied to this pin causes the modem to go off-hook and make the associated phone busy.

Notes

1. A high EIA-232-D signal level is +3 to +15 volts. A low level is –3 to –15 volts. Connecting units in parallel may produce out-of-range voltages and is contrary to specifications.
2. The EIA-232-D interface is intended to connect a terminal to a modem. When computers are connected without modems, one computer must be configured as a modem and the other as a terminal.

Interface Characteristics

The EIA-232-D interface standard specifies all parameters for serial binary data interchange between DTE and DCE devices using unbalanced lines. EIA-232-D transmitter and receiver parameters applicable to the MVME1603/MVME1604 are listed in the following tables.

Table C-3. EIA-232-D Interface Transmitter Characteristics

Parameter	Value		Unit
	Minimum	Maximum	
Output voltage (with load resistance of 3000Ω to 7000Ω)	±8.5		V
Open circuit output voltage		±12	V
Short circuit output current (to ground or any other interconnection cable conductor)		±100	mA
Power-off output resistance	300		W
Output transition time (for a transition region of -3V to +3V and with total load capacitance, including connection cable, of less than 2500pF)		2	µs
Open circuit slew rate		30	V/µs

Table C-4. EIA-232-D Interface Receiver Characteristics

Parameter	Value		Unit
	Minimum	Maximum	
Input signal voltage		±25	V
Input high threshold voltage		2.25	V
Input low threshold voltage	0.75		V
Input hysteresis	1.0		V
Input impedance ($-15V < V_{in} < +15V$)	3000	7000	Ω

The MVME1603/MVME1604 conforms to EIA-232-D specifications. Note that although the EIA-232-D standard recommends the use of short interconnection cables not more than 50 feet (15m) in length, longer cables are permissible provided the total load capacitance measured at the interface point and including signal terminator does not exceed 2500pF.

EIA-530 Connections

The EIA-530 interface complements the EIA-232-D interface in function. The EIA-530 standard defines the mechanical aspects of this interface, which is used for transmission of serial binary data, both synchronous and

asynchronous. It is adaptable to balanced (double-ended) as well as unbalanced (single-ended) signaling and offers the possibility of higher data rates than EIA-232-D with the same DB25 connector.

Table C-2 lists the EIA-530 interconnections that are available at MVME760 serial ports 3 and 4 (J7 and J2 on the board surface, with port 4 also available as SERIAL 4 on the front panel) when those ports are configured via serial interface modules as EIA-530 DCE or DTE ports.

Table C-5. MVME760 EIA-530 Interconnect Signals

Pin Number	Signal Mnemonic	Signal Name and Description
1		Not used.
2	TxD_A	**Transmit Data (A).** Data to be transmitted; output from DTE to DCE.
3	RxD_A	**Receive Data (A).** Data which is demodulated from the receive line; input from DCE to DTE.
4	RTS_A	**Request to Send (A).** Output from DTE to DCE when required to transmit a message.
5	CTS_A	**Clear to Send (A).** Input to DTE from DCE to indicate that message transmission can begin.
6	DSR_A	**Data Set Ready (A).** Input to DTE from DCE to indicate that the DCE is ready to send or receive data. In DCE configuration, always true.
7	SG	**Signal Ground.** Common return line for all signals.
8	DCD_A	**Data Carrier Detect (A)**. Receive line signal detector output from DCE to DTE to indicate that valid data is being transferred to the DTE on the RxD line.
9	RxC_B	**Receive Signal Element Timing - DCE (B).** Control signal that clocks input data.
10	DCD_B	**Data Carrier Detect (B).** Receive line signal detector output from DCE to DTE to indicate that valid data is being transferred to the DTE on the RxD line.
11	TxCO_B	**Transmit Signal Element Timing - DTE (B).** Control signal that clocks output data.
12	TxC_B	**Transmit Signal Element Timing - DCE (B).** Control signal that clocks input data.
13	CTS_B	**Clear to Send (B).** Input to DTE from DCE to indicate that message transmission can begin.
14	TxD_B	**Transmit Data (B).** Data to be transmitted; output from DTE to DCE.
15	TxC_A	**Transmit Signal Element Timing - DCE (A).** Control signal that clocks input data.
16	RxD_B	**Receive Data (B).** Data which is demodulated from the receive line; input from DCE to DTE.
17	RxC_A	**Receive Signal Element Timing - DCE (A).** Control signal that clocks input data.
18	RTS_B	**Request to Send (B).** Output from DTE to DCE when required to transmit a message.
19	LL_A	**Local Loopback (A).** Reroutes signal within local DCE. In DTE configuration, always tied inactive and driven false. In DCE configuration, ignored

Table C-5. MVME760 EIA-530 Interconnect Signals (Continued)

Pin Number	Signal Mnemonic	Signal Name and Description
20	DTR_A	**Data Terminal Ready (A).** Output from DTE to DCE indicating that the DTE is ready to send or receive data.
21	RL_A	**Remote Loopback (A).** Reroutes signal within remote DCE. In DTE configuration, always tied inactive and driven false. In DCE configuration, ignored.
22	DSR_B	**Data Set Ready (B).** Input to DTE from DCE to indicate that the DCE is ready to send or receive data. In DCE configuration, always true.
23	DTR_B	**Data Terminal Ready (B).** Output from DTE to DCE indicating that the DTE is ready to send or receive data.
24	TxCO_A	**Transmit Signal Element Timing - DTE (A).** Control signal that clocks output data.
25	TM_A	**Test Mode (A).** Indicates whether the local DCE is under test. In DTE configuration, ignored. In DCE configuration, always tied inactive and driven false.

Interface Characteristics

C

In specifying parameters for serial binary data interchange between DTE and DCE devices, the EIA-530 standard assumes the use of balanced lines, except for the Remote Loopback, Local Loopback, and Test Mode lines, which are single-ended. Balanced-line data interchange is generally employed in preference to unbalanced-line data interchange where any of the following conditions prevail:

- The interconnection cable is too long for effective unbalanced operation.
- The interconnection cable is exposed to extraneous noise sources that may cause an unwanted voltage in excess of ±1V measured differentially between the signal conductor and circuit ground at the load end of the cable, with a 50Ω resistor substituted for the transmitter.
- It is necessary to minimize interference with other signals.
- Inversion of signals may be required (e.g., plus polarity MARK to minus polarity MARK may be achieved by inverting the cable pair).

EIA-530 interface transmitter and receiver parameters applicable to the MVME1603/MVME1604 are listed in the following tables.

Table C-6. EIA-530 Interface Transmitter Characteristics

Parameter	Value		Unit
	Minimum	Maximum	
Differential output voltage (absolute, with 100Ω load)	2.0		V
Open circuit differential voltage output (absolute)		6.0	V
Output offset voltage (with 100Ω load)	2.0		V
Short circuit output current (for any voltage between –7V and +7V)		±180	mA
Power off output current (for any voltage between –7V and +7V)		±100	µA
Output transition time (with 100Ω, 15pF load)		15	ns

Table C-7. EIA-530 Interface Receiver Characteristics

Parameter	Value		Unit
	Minimum	Maximum	
Differential input voltage		±12	V
Input offset voltage		±12	V
Differential input high threshold voltage		200	mV
Differential input low threshold voltage		–200	V
Input hysteresis	1.0		V
Input impedance (–15V < V_{in} < +15V)	3000	7000	Ω

Proper Grounding

An important subject to consider is the use of ground pins. There are two pins labeled GND. Pin 7 is the *signal ground* and must be connected to the distant device to complete the circuit. Pin 1 is the *chassis ground*, but it must be used with care. The chassis is connected to the power ground through the green wire in the power cord and must be connected to be in compliance with the electrical code.

The problem is that when units are connected to different electrical outlets, there may be several volts of difference in ground potential. If pin 1 of each device is interconnected with the others via cable, several amperes of current could result. This condition may not only be dangerous for the small wires in a typical cable, but may also produce electrical noise that causes errors in data transmission. That is why Table C-2 and Table C-5 show no connection for pin 1. Normally, pin 7 (*signal ground*) should only be connected to the *chassis ground* at one point; if several terminals are used with one computer, the logical place for that point is at the computer. The terminals should not have a connection between the logic ground return and the chassis.

Troubleshooting CPU Boards: Solving Startup Problems

D

Introduction

In the event of difficulty with your CPU board, try the simple troubleshooting steps on the following pages before calling for help or sending the board back for repair. Some of the procedures will return the board to the factory debugger environment. Note that the board was tested under these conditions before it left the factory. The selftests may not run in all user-customized environments.

Table D-1. Basic Troubleshooting Steps for *ALL* CPU Boards

Condition	Possible Problem	Try This:
I. Nothing works, no display on the terminal.	A. If the FUS (or RUN, PWR, +12V, or CPU LED, as appli-cable) is not lit, the board may not be getting correct power.	1. Make sure the system is plugged in. 2. Check that the board is securely installed in its backplane or chassis. 3. Check that all necessary cables are connected to the board, per this manual. 4. Check for compliance with System Considerations, per this manual. 5. Review the Installation and Startup procedures, per this manual. They include a step-by-step powerup routine. Try it.
	B. If the LEDs are lit, the board may be in the wrong slot.	1. For VMEmodules, the CPU board should be in the first (leftmost) slot. 2. Also check that the “system controller” function on the board is enabled, per this manual.
	C. The “system console” terminal may be configured incorrectly.	Configure the system console terminal per this manual.

Table D-1. Basic Troubleshooting Steps for *ALL* CPU Boards (Continued)

Condition	Possible Problem	Try This:
II. There is a display on the terminal, but input from the keyboard and/or mouse has no effect.	A. The keyboard or mouse may be connected incorrectly.	Recheck the keyboard and/or mouse connections and power.
	B. Board jumpers may be configured incorrectly.	Check the board jumpers per this manual.
	C. You may have invoked flow control by pressing a HOLD or PAUSE key, or by typing**:** **<CTRL>-S**	Press the HOLD or PAUSE key again. If this does not free up the keyboard, type in: **<CTRL>-Q**
YOU ARE FINISHED (DONE) WITH THIS TROUBLESHOOTING PROCEDURE. PROCEED WITH THE TROUBLESHOOTING PROCEDURE FOR YOUR PARTICULAR CPU BOARD, AS GIVEN IN THE FOLLOWING TABLE.		

Table D-2. Troubleshooting *MVME1603/MVME1604* Boards

Condition	Possible Problem	Try This:
III. Debug prompt `PPC1-Bug>` does not appear at powerup, and the board does not autoboot.	A. Debugger EPROM/Flash may be missing B. The board may need to be reset.	1. Disconnect *all* power from your system. 2. Check that the proper debugger EPROM or debugger Flash memory is installed per this manual. 3. Reconnect power. 4. Restart the system by "double-button reset": press the RESET and ABORT switches at the same time; release RESET first, wait seven seconds, then release ABORT. 5. If the debug prompt appears, go to step IV or step V, as indicated. If the debug prompt does not appear, go to step VI.
IV. Debug prompt `PPC1-Bug>` appears at powerup, but the board does not autoboot.	A. The initial debugger environment parameters may be set incorrectly. B. There may be some fault in the board hardware.	1. Start the onboard calendar clock and timer. Type: **set *mmddyyhhmm* <CR>** where the characters indicate the month, day, year, hour, and minute. The date and time will be displayed. **Caution** — Performing the next step will change some parameters that may affect your system operation. 2. Type in: **env;d <CR>** This sets up the default parameters for the debugger environment. 3. When prompted to Update Non-Volatile RAM, type in: **y <CR>** 4. When prompted to Reset Local System, type in: **y <CR>** 5. After clock speed is displayed, immediately (within five seconds) press the Return key: **<CR>** or **BREAK** to exit to the System Menu. Then enter a 3 for "Go to System Debugger" and Return: **3 <CR>** Now the prompt should be: `PPC1-Diag>` (continues>)

Table D-2. Troubleshooting *MVME1603/MVME1604* Boards (Continued)

Condition	Possible Problem	Try This:
		6. You may need to use the **cnfg** command (see your board Debugger Manual) to change clock speed and/or Ethernet Address, and then later return to: **env <CR>** and step 3. 7. Run the selftests by typing in: **st <CR>** The tests take as much as 10 minutes, depending on RAM size. They are complete when the prompt returns. (The onboard selftest is a valuable tool in isolating defects.) 8. The system may indicate that it has passed all the selftests. Or, it may indicate a test that failed. If neither happens, enter: **de <CR>** Any errors should now be displayed. If there are any errors, go to step VI. If there are no errors, go to step V.
V. The debugger is in system mode and the board autoboots, or the board has passed selftests.	A. No problems — troubleshooting is done.	No further troubleshooting steps are required. **Note** Even if the board passes all tests, it may still be bad. The selftest does not try out all functions in the board (for example, SCSI or VMEbus tests).
VI. The board has failed one or more of the tests listed above, and cannot be corrected using the steps given.	A. There may be some fault in the board hardware or the on-board debugging and diagnostic firmware.	1. Document the problem and return the board for service. 2. Phone 1-800-222-5640.
YOU ARE FINISHED (DONE) WITH THIS TROUBLESHOOTING PROCEDURE.		

Glossary

Abbreviations, Acronyms, and Terms to Know

This glossary defines some of the abbreviations, acronyms, and key terms used in this document.

10Base5	See thick Ethernet.
10Base2	See thin Ethernet.
10BaseT	See twisted-pair Ethernet.
ACIA	**A**synchronous **C**ommunications **I**nterface **A**dapter
AIX	**A**dvanced **I**nteractive e**X**ecutive (IBM version of UNIX)
architecture	The main overall design in which each individual hardware component of the computer system is interrelated. The most common uses of this term are 8-bit, 16-bit, or 32-bit architectural design systems.
ASCII	**A**merican **S**tandard **C**ode for **I**nformation **I**nterchange, a 7-bit code used to encode alphanumeric information. In the IBM-compatible world, this is expanded to 8 bits to encode a total of 256 alphanumeric and control characters.
ASIC	**A**pplication-**S**pecific **I**ntegrated **C**ircuit
AUI	**A**ttachment **U**nit **I**nterface
BBRAM	Battery Backed-up Random Access Memory
bi-endian	Having big-endian and little-endian byte ordering capability.
big-endian	A byte-ordering method in memory where the address *n* of a word corresponds to the most significant byte. In an addressed memory word, the bytes are ordered (left to right) 0, 1, 2, 3, with 0 being the most significant byte.

BIOS **B**asic **I**nput/**O**utput **S**ystem. The built-in program that controls the basic functions of communications between the processor and the I/O devices (peripherals). Also referred to as ROM BIOS.

BitBLT **Bit** Boundary **BL**ock **T**ransfer. A type of graphics drawing routine that moves a rectangle of data from one area of display memory to another. The data need not have any particular alignment.

BLT **BL**ock **T**ransfer

board The term more commonly used to refer to a PCB (printed circuit board). Basically, a flat board made of nonconducting material, such as plastic or fiberglass, on which chips and other electronic components are mounted. Also referred to as a circuit board or card.

bpi **b**its **p**er **i**nch

bps **b**its **p**er **s**econd

bus The pathway used to communicate between the CPU, memory, and various input/output devices, including floppy drives and hard disk drives. Available in various widths (8-, 16-, and 32-bit), with accompanying increases in speed.

cache A high-speed memory that resides logically between a central processing unit (CPU) and the main memory. This temporary memory holds the data and/or instructions that the CPU is most likely to use over and over again and avoids frequent accesses to the slower hard drive or floppy disk drive.

CAS **C**olumn **A**ddress **S**trobe. The clock signal used in dynamic RAMs to control the input of column addresses.

CD **C**ompact **D**isc. A hard, round, flat portable storage unit that stores information digitally.

CD-ROM **C**ompact **D**isk **R**ead-**O**nly **M**emory

CFM **C**ubic **F**eet per **M**inute

CISC **C**omplex-**I**nstruction-**S**et **C**omputer. A computer whose processor is designed to sequentially run variable-length instructions, many of which require several clock cycles, that perform complex tasks and thereby simplify programming.

CODEC — **CO**der/**DEC**oder

Color Difference (CD) — The signals of (R-Y) and (B-Y) without the luminance (-Y) signal. The Green signals (G-Y) can be extracted by these two signals.

Composite Video Signal (CVS/CVBS) — Signal that carries video picture information for color, brightness and synchronizing signals for both horizontal and vertical scans. Sometimes referred to as “Baseband Video”.

cpi — **c**haracters **p**er **i**nch

cpl — **c**haracters **p**er **l**ine

CPU — **C**entral **P**rocessing **U**nit. The master computer unit in a system.

DCE — **D**ata **C**ircuit-terminating **E**quipment.

DLL — **D**ynamic **L**ink **L**ibrary. A set of functions that are linked to the referencing program at the time it is loaded into memory.

DMA — **D**irect **M**emory **A**ccess. A method by which a device may read or write to memory directly without processor intervention. DMA is typically used by block I/O devices.

DOS — **D**isk **O**perating **S**ystem

dpi — **d**ots **p**er **i**nch

DRAM — **D**ynamic **R**andom **A**ccess **M**emory. A memory technology that is characterized by extremely high density, low power, and low cost. It must be more or less continuously refreshed to avoid loss of data.

DTE — **D**ata **T**erminal **E**quipment.

ECC — **E**rror **C**orrection **C**ode

ECP — **E**xtended **C**apability **P**ort

EEPROM — **E**lectrically **E**rasable **P**rogrammable **R**ead-**O**nly **M**emory. A memory storage device that can be written repeatedly with no special erasure fixture. EEPROMs do not lose their contents when they are powered down.

EISA (bus) — **E**xtended **I**ndustry **S**tandard **A**rchitecture (bus) (IBM). An architectural system using a 32-bit bus that allows data to be transferred between peripherals in 32-bit chunks instead of the 16-

	bit or 8-bit units that most systems use. With the transfer of larger bits of information, the machine is able to perform much faster than the standard ISA bus system.
EPP	**E**nhanced **P**arallel **P**ort
EPROM	**E**rasable **P**rogrammable **R**ead-**O**nly **M**emory. A memory storage device that can be written once (per erasure cycle) and read many times.
ESCC	**E**nhanced **S**erial **C**ommunication **C**ontroller
ESD	**E**lectro-**S**tatic **D**ischarge/Damage
Ethernet	A local area network standard that uses radio frequency signals carried by coaxial cables.
FDC	**F**loppy **D**isk **C**ontroller
FDDI	**F**iber **D**istributed **D**ata **I**nterface. A network based on the use of optical-fiber cable to transmit data in non-return-to-zero, invert-on-1s (NRZI) format at speeds up to 100 Mbps.
FIFO	**F**irst-**I**n, **F**irst-**O**ut. A memory that can temporarily hold data so that the sending device can send data faster than the receiving device can accept it. The sending and receiving devices typically operate asynchronously.
firmware	The program or specific software instructions that have been more or less permanently burned into an electronic component, such as a ROM (read-only memory) or an EPROM (erasable programmable read-only memory).
frame	One complete television picture frame consists of 525 horizontal lines with the NTSC system. One frame consists of two Fields.
graphics controller	On EGA and VGA, a section of circuitry that can provide hardware assistance for graphics-drawing algorithms by performing logical functions on data written to display memory.
HAL	**H**ardware **A**bstraction **L**ayer. The lower-level hardware interface module of the Windows NT operating system. It contains platform-specific functionality.

hardware The term used to describe any of the physical embodiments of a computer system, with emphasis on the electronic circuits (the computer) and electromechanical devices (peripherals) that make up the system. A computing system is normally spoken of as having two major components: hardware and software.

HCT **H**ardware **C**onformance **T**est. A test used to ensure that both hardware and software conform to the Windows NT interface.

I/O **I**nput/**O**utput

IBC PCI/**I**SA **B**ridge **C**ontroller

IDE **I**ntelligent **D**evice **E**xpansion

IEEE **I**nstitute of **E**lectrical and **E**lectronics **E**ngineers

interlaced A graphics system in which the even scanlines are refreshed in one vertical cycle (field), and the odd scanlines are refreshed in another vertical cycle. Its advantage is that the video bandwidth is roughly half that required for a non-interlaced system of the same resolution. This results in less costly hardware and may also make it possible to display a resolution that would otherwise be impossible on given hardware. The disadvantage of an interlaced system is flicker, especially when displaying objects that are only a few scanlines high.

IQ Signals Similar to the color difference signals (R-Y), (B-Y) but using different vector axis for encoding or decoding. Used by some USA TV and IC manufacturers for color decoding.

ISA (bus) **I**ndustry **S**tandard **A**rchitecture (bus). The de facto standard system bus for IBM-compatible computers until the introduction of VESA and PCI. Used in the reference platform specification. (IBM)

ISASIO **ISA S**uper **I**nput/**O**utput device

ISDN **I**ntegrated **S**ervices **D**igital **N**etwork. A standard for digitally transmitting video, audio, and electronic data over public phone networks.

LAN **L**ocal **A**rea **N**etwork

LED **L**ight-**E**mitting **D**iode

LFM **L**inear **F**eet per **M**inute

little-endian A byte-ordering method in memory where the address *n* of a word corresponds to the least significant byte. In an addressed memory word, the bytes are ordered (left to right) 3, 2, 1, 0, with 3 being the most significant byte.

MBLT **M**ultiplexed **BL**ock **T**ransfer

MCA (bus) **M**icro **C**hannel **A**rchitecture

MCG **M**otorola **C**omputer **G**roup

MFM **M**odified **F**requency **M**odulation

MIDI **M**usical **I**nstrument **D**igital **I**nterface. The standard format for recording, storing, and playing digital music.

MPC **M**ultimedia **P**ersonal **C**omputer

MPC105 The PowerPC-to-PCI bus bridge chip developed by Motorola for the Ultra 603/Ultra 604 system board. It provides the necessary interface between the MPC603/MPC604 processor and the Boot ROM (secondary cache), the DRAM (system memory array), and the PCI bus.

MPC601 Motorola's component designation for the PowerPC 601 microprocessor.

MPC603 Motorola's component designation for the PowerPC 603 microprocessor.

MPC603e Motorola's component designation for the PowerPC 603e microprocessor.

MPC604 Motorola's component designation for the PowerPC 604 microprocessor.

MPU **M**icro**P**rocessing **U**nit

MTBF **M**ean **T**ime **B**etween **F**ailures. A statistical term relating to reliability as expressed in power-on hours (poh). It was originally developed for the military and can be calculated several different ways, yielding substantially different results. The specification is based on a large number of samplings in one place, running continuously, and the rate at which failure occurs. MTBF is not representative of how long a device or any individual component is likely to last, nor is it a warranty, but rather an indicator of the relative reliability of a family of products.

multisession The ability to record additional information, such as digitized photographs, on a CD-ROM after a prior recording session has ended.

non-interlaced A video system in which every pixel is refreshed during every vertical scan. A non-interlaced system is normally more expensive than an interlaced system of the same resolution, and is usually said to have a more pleasing appearance.

nonvolatile memory A memory in which the data content is maintained whether the power supply is connected or not.

NTSC **N**ational **T**elevision **S**tandards **C**ommittee (USA)

NVRAM **N**on-**V**olatile **R**andom **A**ccess **M**emory

OEM **O**riginal **E**quipment **M**anufacturer

OMPAC **O**ver-**M**olded **P**ad **A**rray **C**arrier

OS **O**perating **S**ystem. The software that manages the computer resources, accesses files, and dispatches programs.

OTP **O**ne-**T**ime **P**rogrammable

palette The range of colors available on the screen, not necessarily simultaneously. For VGA, this is either 16 or 256 simultaneous colors out of 262,144.

parallel port A connector that can exchange data with an I/O device eight bits at a time. This port is more commonly used for the connection of a printer to a system.

PCI (local bus) **P**eripheral **C**omponent **I**nterconnect (local bus) (Intel). A high-performance, 32-bit internal interconnect bus used for data transfer to peripheral controller components, such as those for audio, video, and graphics.

PCMCIA (bus) **P**ersonal **C**omputer **M**emory **C**ard **I**nternational **A**ssociation (bus). A standard external interconnect bus which allows peripherals adhering to the standard to be plugged in and used without further system modification.

PDS **P**rocessor **D**irect **S**lot

physical address A binary address that refers to the actual location of information stored in secondary storage.

PIB **P**CI-to-**I**SA **B**ridge

pixel An acronym for picture element, also called a pel. A pixel is the smallest addressable graphic on a display screen. In RGB systems, the color of a pixel is defined by some Red intensity, some Green intensity, and some Blue intensity.

PLL **P**hase-**L**ocked **L**oop

PMC **P**CI **M**ezzanine **C**ard

POWER **P**erformance **O**ptimized **W**ith **E**nhanced **R**ISC architecture (IBM)

PowerPC™ The trademark used to describe the **P**erformance **O**ptimized **W**ith **E**nhanced **R**ISC microprocessor architecture for **P**ersonal **C**omputers developed by the IBM Corporation. PowerPC is superscalar, which means it can handle more than one instruction per clock cycle. Instructions can be sent simultaneously to three types of independent execution units (branch units, fixed-point units, and floating-point units), where they can execute concurrently, but finish out of order. PowerPC is used by Motorola, Inc. under license from IBM.

PowerPC 601™ The first implementation of the PowerPC family of microprocessors. This CPU incorporates a memory management unit with a 256-entry buffer and a 32KB unified (instruction and data) cache. It provides a 64-bit data bus and a separate 32-bit address bus. PowerPC 601 is used by Motorola, Inc. under license from IBM.

PowerPC 603™ The second implementation of the PowerPC family of microprocessors. This CPU incorporates a memory management unit with a 64-entry buffer and an 8KB (instruction and data) cache. It provides a selectable 32-bit or 64-bit data bus and a separate 32-bit address bus. PowerPC 603 is used by Motorola, Inc. under license from IBM.

PowerPC 603e™ A variant of the second implementation of the PowerPC family of microprocessors. This CPU incorporates a faster clock (100MHz) and 256KB L2 cache. PowerPC 603e is used by Motorola, Inc. under license from IBM.

PowerPC 604™ The third implementation of the PowerPC family of microprocessors currently under development. PowerPC 604 is used by Motorola, Inc. under license from IBM.

PowerPC Reference Platform (PRP)
A specification published by the IBM Power Personal Systems Division which defines the devices, interfaces, and data formats that make up a PRP-compliant system using a PowerPC processor.

PowerStack™ RISC PC (System Board)
A PowerPC-based computer board platform developed by the Motorola Computer Group. It supports Microsoft's Windows NT and IBM's AIX operating systems.

PRP See PowerPC Reference Platform (PRP).

PRP-compliant See PowerPC Reference Platform (PRP).

PRP Spec See PowerPC Reference Platform (PRP).

PROM **P**rogrammable **R**ead-**O**nly **M**emory

PS/2 **P**ersonal **S**ystem/**2** (IBM)

QFP **Q**uad **F**lat **P**ackage

RAM **R**andom-**A**ccess **M**emory. The temporary memory that a computer uses to hold the instructions and data currently being worked with. All data in RAM is lost when the computer is turned off.

RAS **R**ow **A**ddress **S**trobe. A clock signal used in dynamic RAMs to control the input of the row addresses.

Reduced-Instruction-Set Computer (RISC)
A computer in which the processor's instruction set is limited to constant-length instructions that can usually be executed in a single clock cycle.

RFI **R**adio **F**requency **I**nterference

RGB The three separate color signals: **R**ed, **G**reen, and **B**lue. Used with color displays, an interface that uses these three color signals as opposed to an interface used with a monochrome display that requires only a single signal. Both digital and analog RGB interfaces exist.

RISC See Reduced-Instruction-Set Computer (RISC).

ROM **R**ead-**O**nly **M**emory

RTC **R**eal-**T**ime **C**lock

SBC **S**ingle **B**oard **C**omputer

SCSI	**S**mall **C**omputer **S**ystems **I**nterface. An industry-standard high-speed interface primarily used for secondary storage. The SCSI-1 implementation provides up to 5 Mbps data transfer.
SCSI-2 (Fast/Wide)	An improvement over plain SCSI; and includes command queuing. Fast SCSI provides 10 Mbps data transfer on an 8-bit bus. Wide SCSI provides up to 40 Mbps data transfer on a 16- or 32-bit bus.
serial port	A connector that can exchange data with an I/O device one bit at a time. It may operate synchronously or asynchronously, and may include start bits, stop bits, and/or parity.
SIM	**S**erial **I**nterface **M**odule
SIMM	**S**ingle **I**nline **M**emory **M**odule. A small circuit board with RAM chips (normally surface mounted) that is designed to fit into a standard slot.
SIO	**S**uper **I/O** controller
SMP	**S**ymmetric **M**ulti**P**rocessing. A computer architecture in which tasks are distributed among two or more local processors.
SMT	**S**urface **M**ount **T**echnology. A method of mounting devices (such as integrated circuits, resistors, capacitors, and others) on a printed circuit board, characterized by not requiring mounting holes. Rather, the devices are soldered to pads on the printed circuit board. Surface-mount devices are typically smaller than the equivalent through-hole devices.
software	The term used to describe any single program or group of programs, languages, operating procedures, and documentation of a computer system. A computing system is normally spoken of as having two major components: hardware and software. Software is the real interface between the user and the computer.
SRAM	**S**tatic **R**andom **A**ccess **M**emory
SSBLT	**S**ource **S**ynchronous **BL**ock **T**ransfer
standard(s)	A set of detailed technical guidelines used as a means of establishing uniformity in an area of hardware or software development.

SVGA — **S**uper **V**ideo **G**raphics **A**rray (IBM). An improved VGA monitor standard that provides at least 256 simultaneous colors and a screen resolution of 800 x 600 pixels.

Teletext — One-way broadcast of digital information. The digital information is injected in the broadcast TV signal, VBI, or full field, The transmission medium could be satellite, microwave, cable, etc. The display medium is a regular TV receiver.

thick Ethernet (10Base5) — An Ethernet implementation in which the physical medium is a double-shielded, 50-ohm coaxial cable capable of carrying data at 10 Mbps for a length of 500 meters (also referred to as thicknet).

thin Ethernet (10Base2) — An Ethernet implementation in which the physical medium is a single-shielded, 50-ohm RG58A/U coaxial cable capable of carrying data at 10 Mbps for a length of 185 meters (also referred to as AUI or thinnet).

twisted-pair Ethernet (10BaseT) — An Ethernet implementation in which the physical medium is an unshielded pair of entwined wires capable of carrying data at 10 Mbps for a maximum distance of 185 meters.

UART — **U**niversal **A**synchronous **R**eceiver/**T**ransmitter

UV — **U**ltra**V**iolet

UVGA — **U**ltra **V**ideo **G**raphics **A**rray. An improved VGA monitor standard that provides at least 256 simultaneous colors and a screen resolution of 1024 x 768 pixels.

Vertical Blanking Interval (VBI) — The time it takes the beam to fly back to the top of the screen in order to retrace the opposite field (odd or even). VBI is on the order of 20 TV lines. Teletext information is transmitted over 4 of these lines (lines 14-17).

VESA (bus) — **V**ideo **E**lectronics **S**tandards **A**ssociation (or VL bus). An internal interconnect standard for transferring video information to a computer display system.

VGA	**V**ideo **G**raphics **A**rray (IBM). The third and most common monitor standard used today. It provides up to 256 simultaneous colors and a screen resolution of 640 x 480 pixels.
virtual address	A binary address issued by a CPU that indirectly refers to the location of information in primary memory, such as main memory. When data is copied from disk to main memory, the physical address is changed to the virtual address.
VL bus	See **V**ESA **L**ocal bus (VL bus).
VMEchip2	MCG second generation VMEbus interface ASIC (Motorola)
VME2PCI	MCG ASIC that interfaces between the PCI bus and the VMEchip2 device.
volatile memory	A memory in which the data content is lost when the power supply is disconnected.
VRAM	**V**ideo (Dynamic) **R**andom **A**ccess **M**emory. Memory chips with two ports, one used for random accesses and the other capable of serial accesses. Once the serial port has been initialized (with a transfer cycle), it can operate independently of the random port. This frees the random port for CPU accesses. The result of adding the serial port is a significantly reduced amount of interference from screen refresh. VRAMs cost more per bit than DRAMs.
Windows NT™	The trademark representing **Windows N**ew **T**echnology, a computer operating system developed by the Microsoft Corporation.
XGA	E**X**tended **G**raphics **A**rray. An improved IBM VGA monitor standard that provides at least 256 simultaneous colors and a screen resolution of 1024 x 768 pixels.
Y Signal	Luminance. Parameter that determines the brightness (but not the color) of each spot (pixel) on a CRT screen in color or B/W systems.

Index

A

Abort (interrupt) signal 2-23, 3-16, 3-19
access
    time-out 6-19
    times 3-26
ambient air temperature B-2
assembly language 5-2
Autoboot enable 6-6

B

backplane jumpers 1-39
base board(s)
    differences 1-1
    layout 1-7, 1-18
block diagram
    MVME1603/MVME1604 3-4
Board 3-16
    configuration 1-6
    configuration register 3-16
    placement 1-38
    information block 6-2
    structure 6-2

C

cables B-2
CNFG 6-2
commands 5-3
    debugger 5-4
conductive chassis rails B-3
configure
    PPC1Bug parameters 6-3
    VMEbus interface 6-12
Configure Board Information Block 6-2
connector pin assignments 4-1
console port selection 1-8, 1-24
control/status registers 1-46
cooling requirements B-2
counters 3-14

D

data circuit-terminating
    equipment (DCE) C-3
data terminal equipment (DTE) C-3
DCE 3-16
debugger
    commands 5-4
    firmware (PPCBug) 5-1, 6-1
decimal number 4
diagnostics 5-1
    test groups 5-7
disk drive
    connector 4-15
    controller 3-10, 3-12, C-1
DMA channels 2-24
DRAM
    base address 1-45
    speed 6-10
DTE 3-16

E

EIA-232-D
    interconnections C-3
EIA-530
    interconnections C-6
    interface characteristics C-8

endian issues 2-25
    53C825 or 53C810(SCSI) 2-28
    big-endian mode 2-26
    GD5434 (graphics) 2-28
    little-endian mode 2-27
    MPC105 function 2-25
    PCI domain 2-28
    processor/memory domain 2-25
    VME2PCI function 2-28
    VMEbus domain 2-28
ENV command 6-3
environmental parameters 6-1
ESD
    precautions 1-32
Ethernet
    address 3-7
Ethernet (see 82596CA and LAN) 1-46, 3-22
Ethernet transceiver
    interface 1-47, 3-23
    power 1-47
    power distribution 3-23

F

features
    hardware 3-1
    ISA Super I/O device 3-10
    VMEchip2 3-10
first access length (ROMFAL) 3-26
Flash device speed 3-26
forced air cooling B-2
F-Page address decoder 6-18
front panel controls 2-1, 3-21
functional description 3-25
fuses 3-16, 3-22, 3-23
    MVME1600-001 base board 1-46
    MVME1600-011 base board 1-47

G

general-purpose readable jumpers
    MVME1600-001 base board 1-8, 1-23
global bus timeout 1-45
graphics (GD5434) 2-28
graphics interface 3-8
ground connections C-9

H

hexadecimal character 4

I

IBC
    arbiter configuration diagram 2-19
    DMA channel assignments 2-24
    interrupt handler block diagram 2-22
installation
    considerations 1-45
    MVME712M transition module 1-42
    MVME760 transition module 1-39
    PM603/PM604 mezzanine 1-33
    RAM104 mezzanine 1-35
    VMEmodule assembly 1-38
interconnect signals 4-1
interconnections, serial C-3, C-6
interrupt support 2-20
ISA bridge controller
    functions 3-13

J

jumper headers
    MVME1600-001 base board 1-7
    MVME1600-011 base board 1-18
    MVME712M transition module 1-29
    MVME760 transition module 1-15

K

keyboaard/mouse interface 3-10

L

L2 cache 1-1, 3-1, 3-3, 4-6
LAN transceiver 1-46, 3-22
last access length (ROMNAL) 3-26
LCP2 adapter board 3-7
local reset (LRST) 2-2, 3-19
lowercase 5-8

M

machine check interrupt (MCP_) 2-21
manual terminology 4
manufacturers' documents A-2
maskable interrupts 2-21
master
    address decoders 6-15
    enable 6-15
MCP_ (machine check interrupt) 2-21
memory map(s) 2-4
    ISA/PCI I/O 2-7
    local I/O 2-6
    overall 2-5
    PCI local bus 2-9
    VME2PCI 2-10
memory size 6-10
mezzanine modules 1-1
minimum ROMFAL and ROMNAL
    values 3-26
module ID (syn/async ports) 3-16
multiplexing function (P2) 3-16, 3-18
MVME1603/MVME1604 interrupt
    architecture 2-20

N

NETboot enable 6-8
Network Auto Boot enable 6-8
Non-Volatile RAM (NVRAM) 6-1, 6-3
normal address range 2-4

O

operating parameters 6-1

P

P2
    adapter board 3-7, 3-28
    multiplexing function 3-16, 3-18
parallel port 3-10
PCI
    arbitration assignments 2-19
    bus 3-4, 3-9
pin assignments, connector 4-1
power distribution 3-22
PPCBug debugger firmware 5-1, 6-1

R

real-time clock 3-13
related specifications A-7
remote control/status connector 3-14
    MVME1600-011 base board 1-47
remote panel interface 3-23
remote status/control connector 3-24
    MVME1600-001 base board 1-13
    MVME1600-011 base board 1-25
required equipment 1-2
resetting the system 2-2, 3-20
restart mode 5-8
RF emissions B-3
ROMboot enable 6-7, 6-11
ROMFAL 6-10
ROMFAL/ROMNAL values 3-26
ROMNAL 6-11

S

SCSI
    (53C825 or 53C810) 2-28
    bus 6-5
    interface 3-6
    termination 3-7, 3-16
    terminator power 1-46, 1-47, 3-23, 3-22
serial communications interface 3-15, C-2
serial interface
    modules (SIMs) 3-27
    parameters C-4
serial ports 3-10, 3-15

set environment to bug/operating
    system (ENV) 6-3
shielded cables (see also cables) B-2
Short I/O address decoder 6-18
slave
    address decoders 6-13
    enable 6-14
sources of reset 2-24
speaker output 1-47, 3-14, 3-24
specifications, base board B-1
SYSFAIL* 6-5
system
    controller 1-38
    reset (SRST) 3-19

T

time-out 6-19
timers 3-14
transition modules 1-2, 1-47, 3-23, 3-27
    installation 1-38
transmitters
    EIA-232-D C-5
    EIA-530 C-8

U

uppercase 5-8
user-definable jumpers 1-8, 1-24

V

VGA port 3-8
video port 1-9
VME2PCI 6-3, 6-12
VMEbus
    address/data configurations 1-45
    interface 6-12
    time-out 6-19
VMEchip2 6-3, 6-12, 6-18

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