FUJITSU

SoC Reference Kit User Manual

Fujitsu Microelectronics America, Inc.
Corporate Headquarters
1250 East Arques Avenue, M/S 333
Sunnyvale, California 94088-7470
Tel: (800) 866-8608 Fax: (408) 737-5999
E-mail: inquiry@fma.fujitsu.com Web Site: www.fma.fujitsu.com

PN 5720-6104 Rev.1.1

TABLE OF CONTENTS

1. OVERVIEW

The System on Chip (SoC) Reference Kit is designed for Institute of Electrical Electronic Engineers (IEEE) 802.16-2004/WiMAX product developers for evaluation of WiMAX solutions from Fujitsu. The SoC Reference Kit includes the necessary software and hardware components to achieve a cost effective, fixed Broadband Wireless Access (BWA) system solution for

- Low-cost subscriber stations (SS),
- Enterprise SS, and
- Base stations (BS).

The Fujitsu 802.16 platform enables a BWA platform for SS or BS. It includes:

- Compliance with IEEE 802.16-2004 standard specification.
- Media Access Control (MAC) portability to different Real Time Operating System (RTOS).
- MAC security sublayer for SS authentication and data encryption.
- Multiple service class support to differentiate service quality.
- Dynamic service management to activate the service class when needed.

1.1 Reference Kit Content

The SoC Reference Kit consists of a combination of hardware and software components. The three (3) main components are the

- SoC Reference Board with the 802.16/WiMAX SoC Integrated Circuit (IC) core processor,
- Software package to run the SoC and the Reference Board, and
- Software package to install the SoC Reference Kit as a half-duplex WiMAX SS.

Figure 1 shows the hardware components included in the SoC Reference Kit, while Figure 2 illustrates the relationships between hardware and software components of the SoC Reference Kit.

The SoC Reference Board has a high-density connector that can be attached to either a Baseband Adaptor Board or an Radio Frequency (RF) Evaluation Board from SiGe Semiconductor.

Use two (2) SoC Reference Kits to create a simple point-to-point network, or purchase additional SoC Reference Kits to expand to a point-to-multipoint network. Additional RF boards can be purchased to evaluate other RF configurations (e.g., duplex mode or channel bandwidth). The software included in the SoC Reference Kit allows the user to customize operational configurations.

1.2 SoC Reference Board Specifications

1.2.1 General

- Duplexing: Half Duplex-Frequency Division Duplexing (HD-FDD) or Time Division Duplexing (TDD).
- Channel BW: 1.75 to 20MHz.
- Wire Interface: Ethernet 10/100BT.
- Radio Interface: Baseband, 3.5GHz Band.
- Operating Temperature Range: -40°C to +85°C.

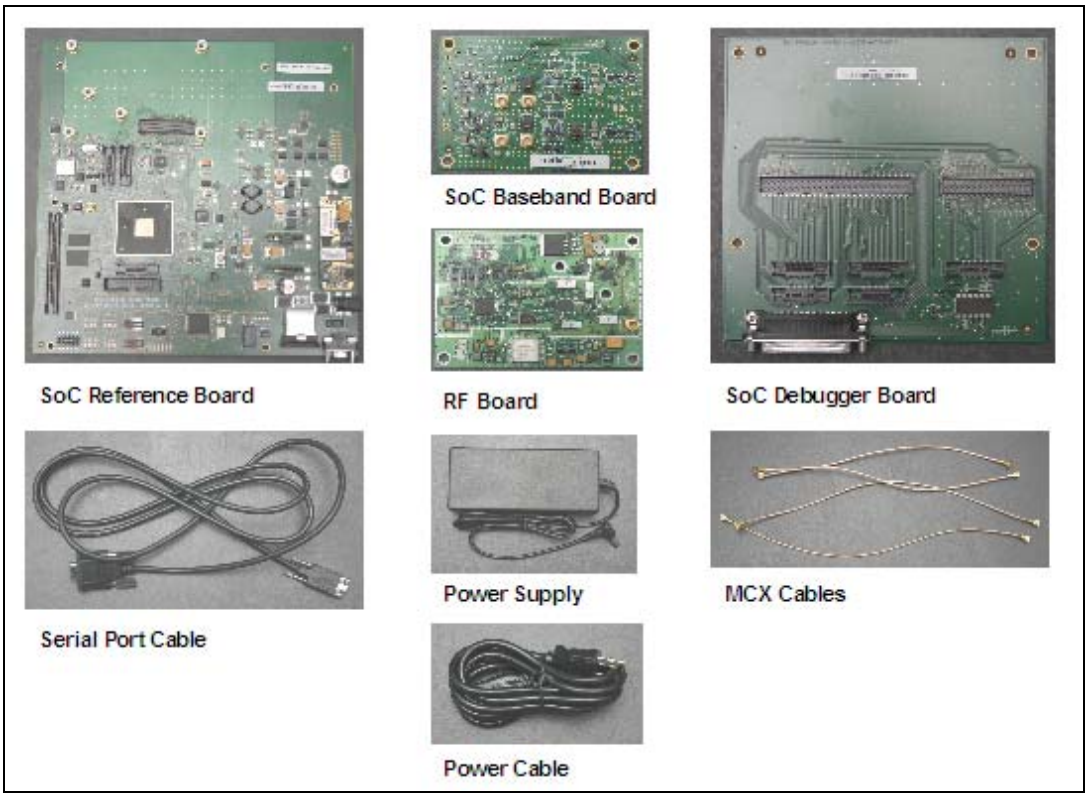


Figure 1: Hardware—SoC Reference Kit

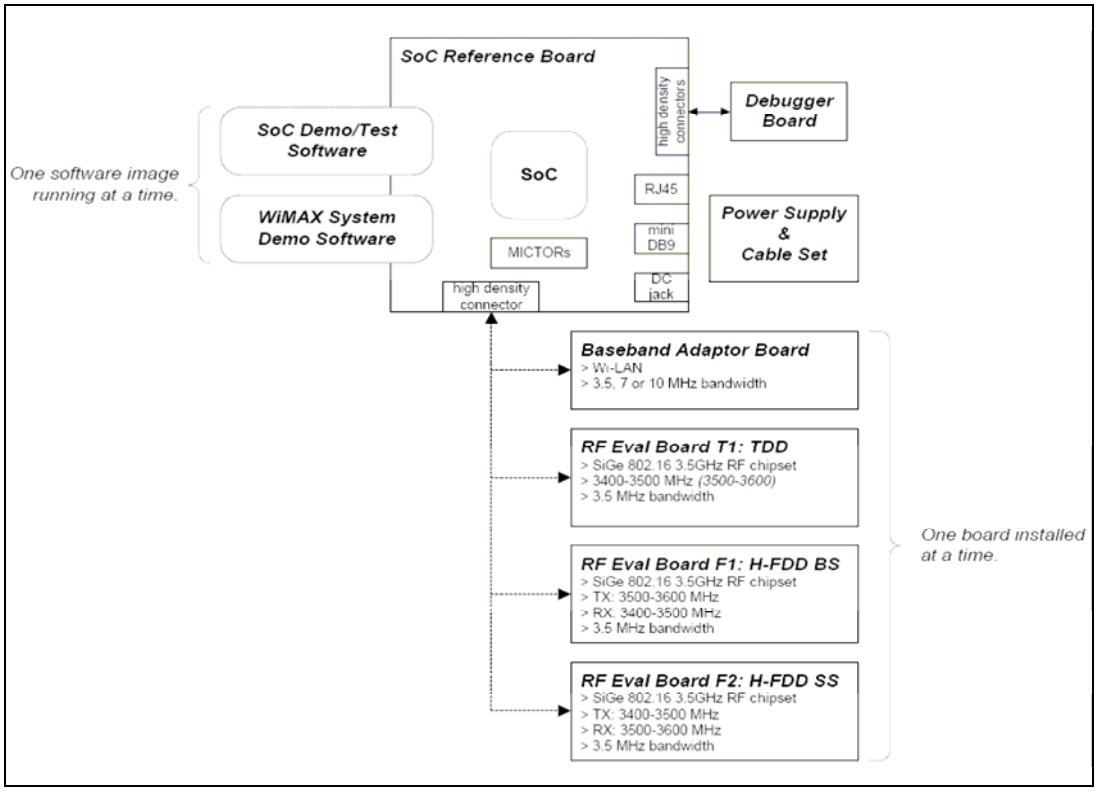


Figure 2: Relationships between Hardware and Software—SoC Reference Kit

1.2.2 Power Supply

- Power Requirements: 15W Max standalone or 25W Max with external processor board.
- Input: 48VDC.
- Connector: 5.5mm OD, 2.5mm ID, Center Positive DC Connector.
- Power Reset: Voltage supervisor resets processor when rails drop below 20% nominal value.
- Power Sequencing: Voltage rails are sequence to requirements of processor.

1.2.3 Processor

One (1) Fujitsu MB87M3400 WiMAX SoC.

1.2.4 Upper Media Access Control (UMAC) Processor Peripherals

- Processor: ARM 926 internal to SoC.
- Memory:
  - Synchronous Dynamic Random Access Memory (SDRAM): 128Mb 4Mx32 Micron MT48LC8M32LF-F5-10.
  - Flash: 4Mb.
- Ethernet Physical Layer (PHY):
  - AMD 79C874.
- General Purpose Input/Output (GPIO) Light Emitting Diode (LED) status:
  - LED status indicators for each 24 GPIOs for software development.
  - Dual In-line Package (DIP) switch pull down for 10 GPIOs for software development.

1.2.5 Clocks

- Clock Source: 20MHz Voltage Controlled Temperature Compensated Oscillator (VCTCXO), ±10ppm control, ±4.5ppm stability.
- Front End (FE) PHY Clock: Generated by programmable Direct Digital Synthesis (DDS), Analog Devices AD9834.
- Reference Board VCTCXO can be bypassed by a jumper when RF Boards are used.

1.2.6 I/Q Output

- Transmit (Tx) Analog Output:
  - 10mA outputs requiring 75ohm termination resistor.
  - Differential outputs.
- (Receive) Rx Analog Input:
  - 0.5VPP inputs.
  - 0.55V common mode differential inputs.
  - 1.2Kohm impedance.
- Digital to Analog Converter (DAC) Outputs:
  - 10-bit DAC outputs for option of using external DACs.
  - Outputs provided on 38-pin Mictors for logic analyzer access.
- Digital Analog to Digital Converter (ADC) Inputs:
  - 10-bit ADC inputs for option of using external ADC.
  - Inputs provided on 38-pin Mictors for logic analyzer access.

1.2.7 Baseband and RF Interface Connector

- Connector: Samtec TOLC-125-02-F-Q-LC.
- Supported Boards:
  - Baseband Adapter Board.
  - SiGe SE7351L-AK1.
  - SiGe SE7351L-AK2.
  - SiGe SE7351L-AK3.
  - SiGe SE7351L-AK4.
  - SiGe SE7351L-AK5.
  - SiGe SE7351L-AK6.

1.2.8 External Processor Interface Connector

- Connector: 152-pin Mictor Receptacle.
- External Processor Board: GDA Technologies MPC8560 Mezzanine Card.

1.2.9 Debugger Board Interface Connector

- Connectors: One (1) Samtec SOLC-130-02-S-LC and One (1) Samtec SOLC-150-02-S-LC.
- Interfaces to Debugger Board.

1.2.10 RS232 Connector

Connector: Micro D-Sub 9-Pin.

1.2.11 ARM Debug Connector

- Connector: 2x10 0.1” shrouded male header.
- Debugger: ARM Multi-Ice.

1.2.12 ARM Embedded Test Module (ETM) Connector

- Connector: 38-pin MICTOR Receptacle.
- ETM: ARM Multi-Trace.
- Supported Mode: Multiplexed, half clock mode.

1.3 SoC Baseband Board Specifications

The SoC Baseband Board and the SoC Reference Board interface via the baseband and RF interface connector.

- Connector: Samtec TOLC-125-02-F-Q-LC.
- Channel BW: 3.5MHz and 7MHz baseband filters selectable by shunt jumper.
- Rx Inputs: I & Q single-ended inputs on MCX cables.
- Tx Outputs: I & Q single-ended outputs on MCX cables.
- Power Supply: ±5VDC powered by the SoC Reference Board, via the power cable.

1.4 SoC Debugger Board Specifications

The SoC Debugger Board and the SoC Reference Board interface via the debugger connector.

- Connectors: One (1) Samtec TOLC-130-02-S-Q-LC and One (1) Samtec TOLC-150-02-S-Q-LC.
- ARC Debugger: DB25 female connector attached at the Personal Computer (PC) parallel port.
- Logic analyzer Interface: Five (5) 38-Pin MICTOR receptacles and ARM external memory interface, Serial Peripheral Interface (SPI), I^2C, Automatic Gain Control (AGC), RF control.

2. QUICK START GUIDE

Refer to Figure 3 to identify the components of the SoC Reference Board that are required for host PC requirements (Section 2.1) and Heatsink installation (Section 2.3).

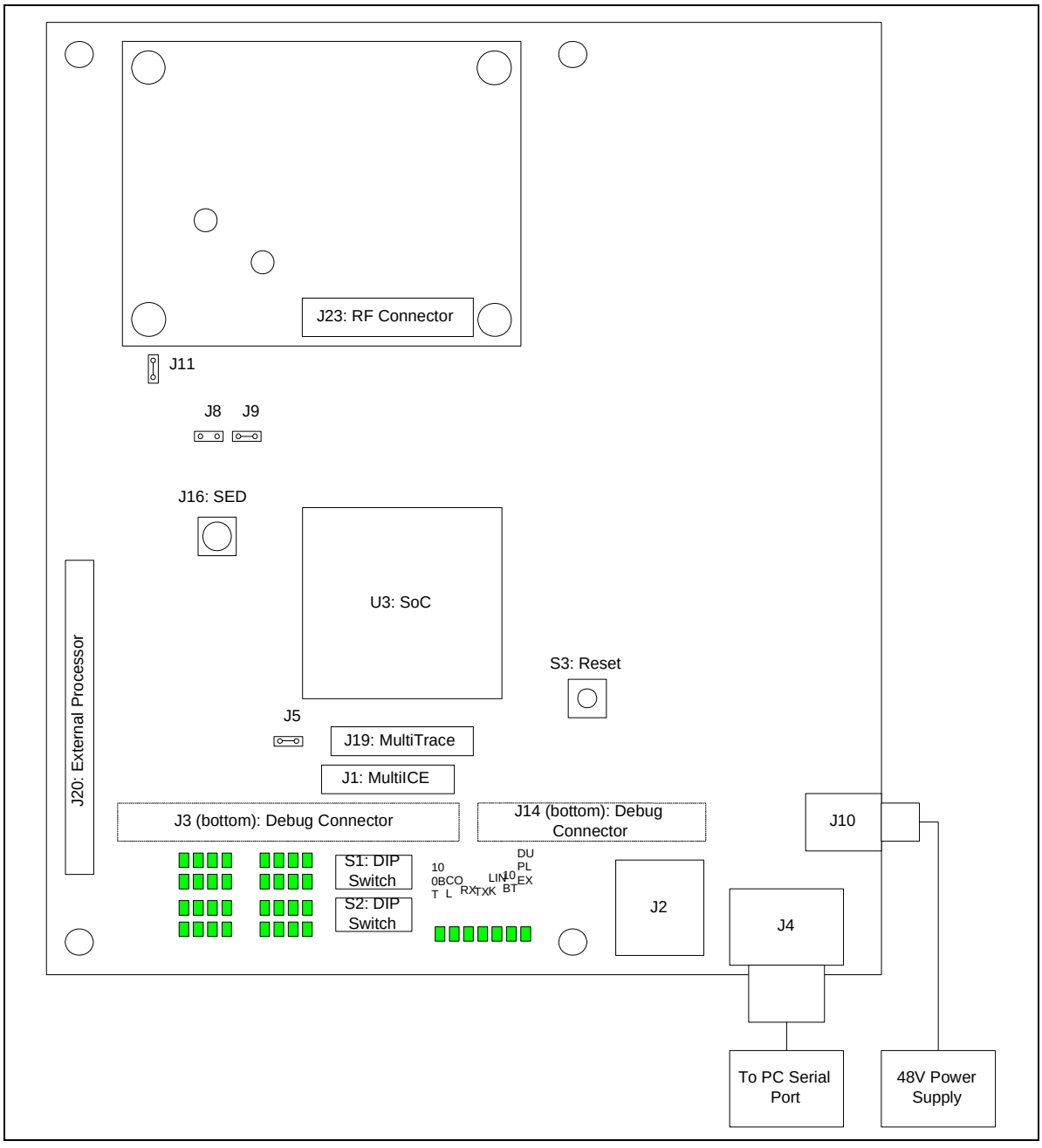


Figure 3: SoC Reference Board

2.1 Host PC Requirement

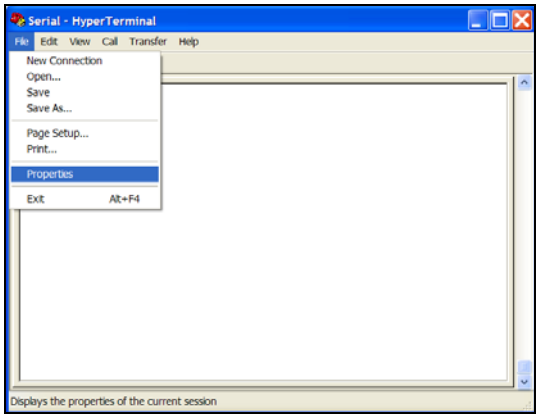
A host PC is required to change the default SoC Reference Kit software configuration and to initiate tests. To communicate with SoC you must have a computer system that meets the following hardware and software requirements:

- One (1) available, standard hardware serial port (DB9).
- An operating system that provides a standard RS-232 terminal program for the available hardware serial port (e.g., Microsoft Windows HyperTerminal).

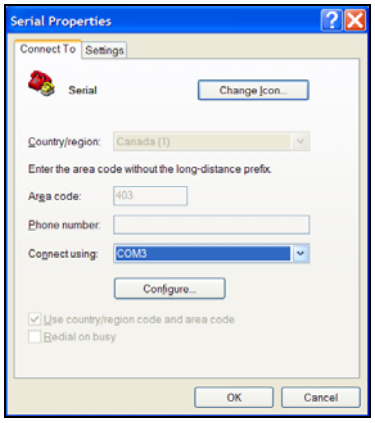
2.2 How To Configure HyperTerminal

The procedure for configuring HyperTerminal on a Windows-based PC is detailed below.

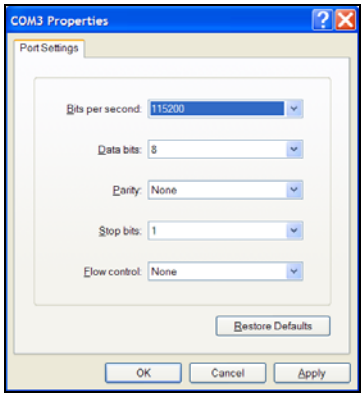
1. Select **File**, **Properties** from the main menu to display the **Serial Properties** screen.



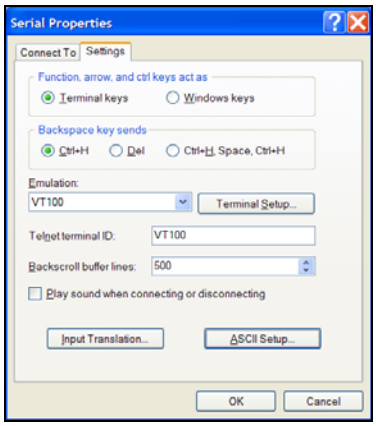
2. The **Serial Properties** screen defaults to the **Connect To** tab. Under the **Connect Using** dropdown menu select an available COM port then click **Configure** to configure this port.



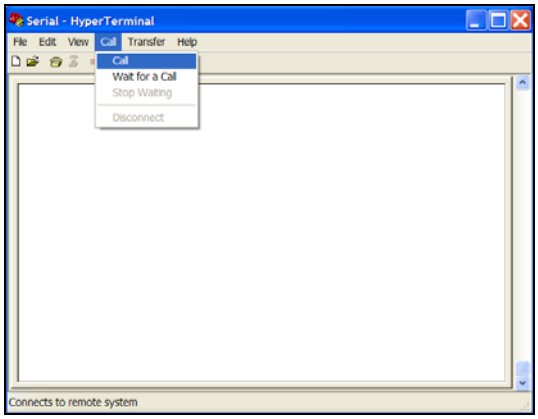
3. The **Com Properties** screen shows the **Port Settings** tab. Configure the port settings as shown below, then click **OK** to confirm and return to the **Serial Properties** screen.



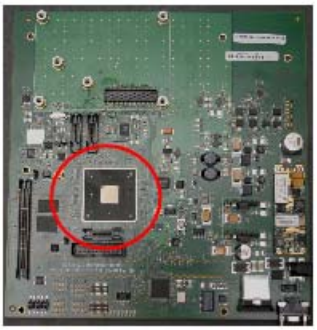
4. In the **Serial Properties** screen, select the **Settings** tab and configure it as shown below.



5. Return to the main HyperTerminal window. Select **Call**, **Call** to initiate communication with the SoC Reference Board.

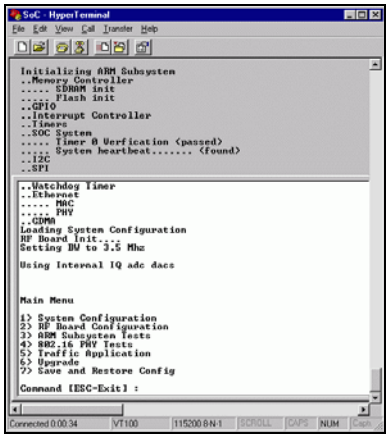


2.3 Installing Heatsink and Powering Up



The procedure for installing Heatsink and powering up the SoC Reference Board is given below. Figure 3 identifies the components mentioned in this procedure.

1. Remove the clear plastic cover from the back of Heatsink to expose the adhesive.
2. Adhere SoC (U3) to the corresponding flat, square surface on the Reference Board (the red circle in the adjacent photo).
3. Connect (J4) to a serial terminal (e.g., 115200 Band, 8 bits, no start bit, 1 stop bit) using the serial cable included in the SoC Reference Kit.
4. Plug in the 48V power supply into a wall outlet (100-240 Vac, 1.25A, 50-60Hz).
5. Connect the barrel connector from the 48V power supply to the SoC Reference Board (J10).
6. The LEDs light up on Reference Board and HyperTerminal display the following:



2.4 Setting Up SoC Reference Boards for a Traffic Test

Depending on if you install a Baseband Board or an RF Board on the SoC Reference Board, you can generate Baseband or RF traffic tests. The procedures for each are given below.

2.4.1 Baseband Traffic Procedure

1. Configure two (2) SoC Reference Boards as shown in Figure 4.
2. Install a Baseband Board on each of the SoC Reference Boards.
3. Connect the Tx/Rx I/Q ports of the Baseband Boards with the MCX cables provided in your SoC Reference Kit (refer to Figure 1).
4. Make sure that the shunts at J11 and J9 are installed and the shunt at J8 is removed.
5. From the SoC Main Menu (Section 3.1.1) select **(5) Traffic Application**, **(a) Run Traffic** to start traffic generation (see also Section 3.1.6).

2.4.2 RF Traffic Procedure

1. Configure two (2) SoC Reference Boards as shown in Figure 5.
2. Install an RF board on each of the SoC Reference Boards.
3. Access 60db of RF attenuation rated to at least 3.6GHz. Then, use adapters to couple the attenuation between the two RF Boards to prevent damage.

4. Make sure that the shunt at J8 is installed and the shunts at J11 and J9 are removed.
5. From the SoC Main Menu (Section 3.1.1) select (5) Traffic Application, (a) Run Traffic to start traffic generation (see also Section 3.1.6).

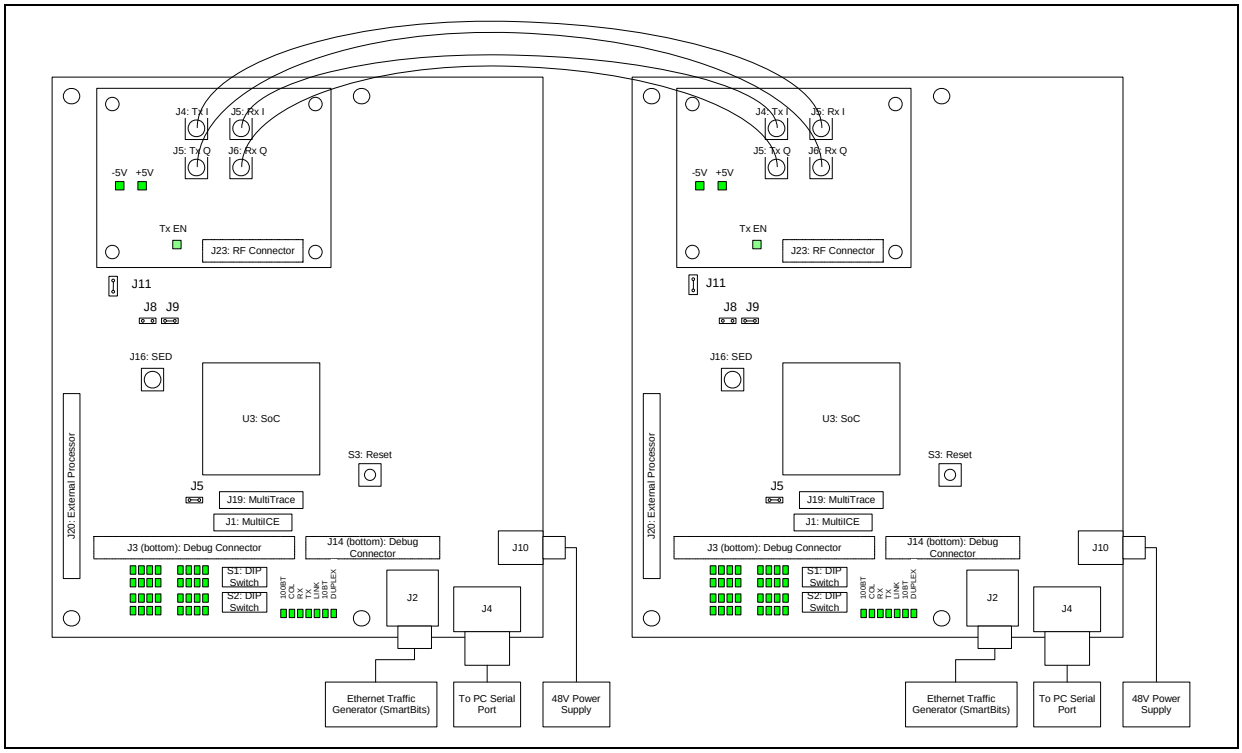


Figure 4: Baseband Traffic Test Configuration

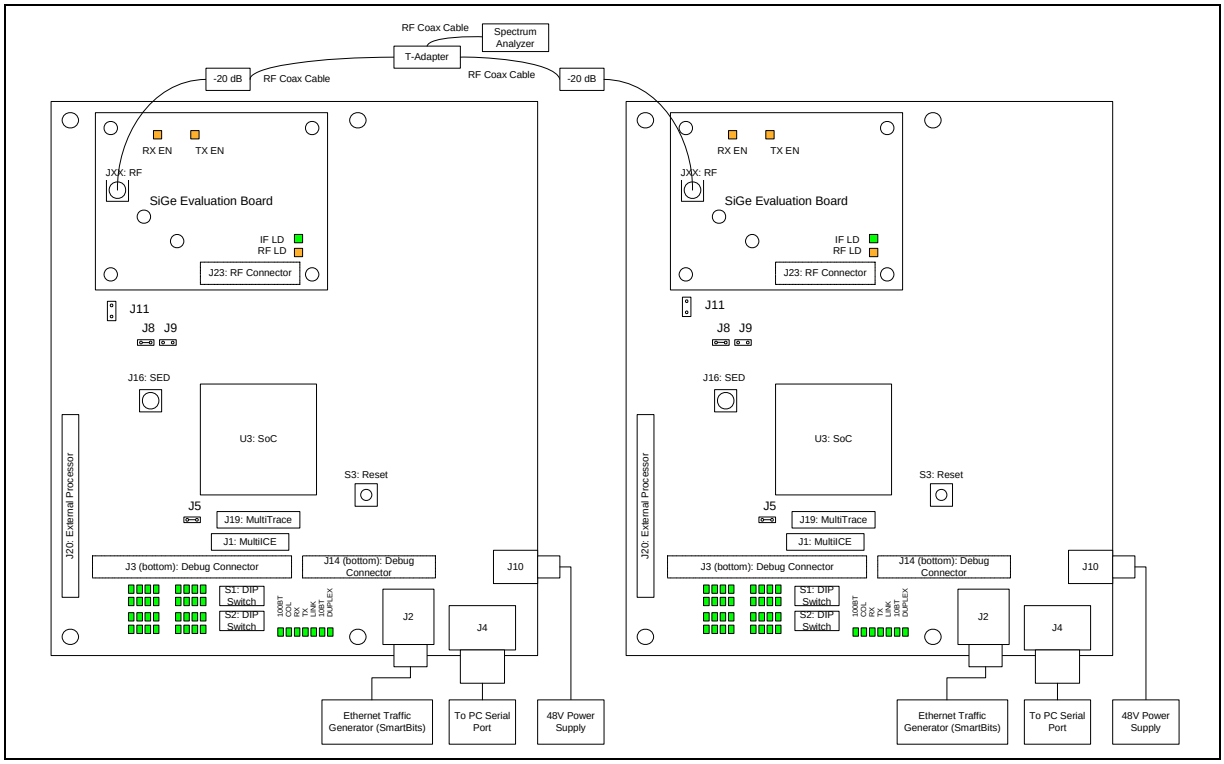


Figure 5: RF Traffic Test Configuration

3. USING THE REFERENCE KIT SOFTWARE

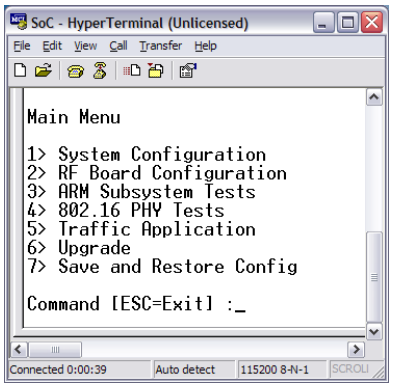
3.1 Terminal Setup

Windows HyperTerminal is the suggested interface for setting up the host PC and SoC Reference Board (Section 2.2 details how to configure HyperTerminal). However, any VT100 terminal will work with the following setup:

- Baud rate: 115200, 8-bit data, no parity bit, 1 stop bit, and no flow control.
- VT100 emulation must be chosen as terminal emulation type.
- Do not send line ends with line feeds.
- Do not echo locally typed characters.

3.1.1 SoC Main Menu

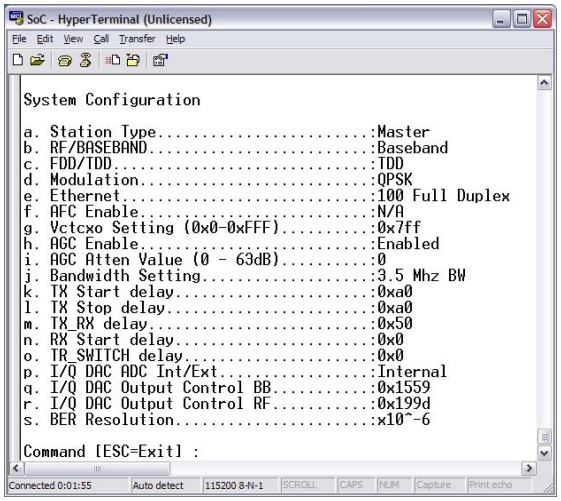
Once your PC has been setup, the SoC software defaults to the SoC Main Menu. Navigate through the submenus to setup the SoC Reference Board. On your keyboard, type the number corresponding to the submenu you want to access. At any stage during setup, you can return to a previous submenu hitting the **ESC** key or return to the Main Menu by hitting **ESC** a few times consecutively. Each submenu is described below.



1. System Configuration—Setup the SoC Reference Board system configuration. Examples of system configurations include Baseband or RF operation mode, TDD or FDD operation, and Modulation type.
2. RF Board Configuration—Manipulate the RF Board and its registers from this submenu.
3. ARM Subsystem Tests—Access useful memory and I^2C tests for the ARM subsystem.
4. 802.16 PHY Tests—Interact with 802.16 PHY. Peak the values for each register and configure registers using the poke command.
5. Traffic Application—Start traffic between the Master and the Slave.
6. Upgrade—Upgrade firmware using the XModem protocol. Erase the contents of Flash under this menu and retrieve firmware version information [see also Section 3.1.7, (b)].
7. Save and Restore Config—Save customized configurations for the SoC Reference Board that are maintained on reboot. Factory default settings are also available from this menu.

3.1.2 System Configuration Menu

Use the System Configuration Menu to change default settings for the SoC Reference Board. Develop custom configurations for Baseband/RF, TDD/FDD and Modulation. Each submenu is described below.



a. **Station Type**—Choose the station type of the board for the traffic tests. In Master mode the board initiates the PHY traffic. In Slave mode the Slave board will listen for the Master board and then sync to the Master before it can transmit uplink data.

b. **RF/BASEBAND**—Setup the board to allow RF or Baseband traffic. In Baseband mode the RF Board is not initialized, and AGC and Automatic Frequency Control (AFC) are not operational.

c. **FDD/TDD**—For an RF system, define the duplexing mode as either FDD or TDD. In FDD mode, Rx and Tx frequencies differ, while in TDD mode they are the same. Rx and Tx frequencies are set under the RF Board Configuration Menu (see Section 3.1.3).

d. **Modulation**—Change the modulation scheme. Choose from BPSK, QPSK, QAM16, and QAM64.

e. **Ethernet**—Configure the Ethernet PHY to Auto Negotiate, 100BT half Duplex, 100BT full Duplex, 10BT half Duplex or 10BT full Duplex.

f. **AFC Enable**—Enable or disable the Automatic Frequency Control (AFC). This feature is only applicable to Slave mode and cannot be enabled in Master mode. (Refer to VCTCXO Setting, below, to understand AFC requirements for system configuration.)

g. **VCTCXO Setting (0x0-0xFFF)**—Fine-tune the RF Center Frequency. This is critical for data transfer on an RF system (i.e., does not affect data transfer on a Baseband system).

   The VCTCXO Setting is the binary value of the VCTCXO adjustment, which is written to a 12-bit DAC that controls voltage at the control pin of the oscillator. AFC on the Slave board must be disabled in order for the VCTCXO value to take effect.

   To fine-tune the frequency write the value of **0x7FF** to DAC on both Master and Slave boards. The ideal value for 0x7FF differs for each board due to its unique electrical characteristics. Determine the ideal value using lab equipment (i.e., a frequency counter and spectrum analyzer) to ensure the RF Center Frequency is closely matched on Master and Slave.

h. **AGC Enable**—Enable or disable the Automatic Gain Control (AGC) of the receiver.

i. **AGC Atten Value**—Specify a desired level of constant attenuation to control the Rx signal. This setting is used when AGC is disabled but a specific amount of attenuation is desired.

j. **Bandwidth Setting**—Choose between the 3.5 MHz and 7.0 MHz data bandwidth.

*Refer to Figure 6 for items **k**, **l** and **o**, below.*

k. **TX Start Delay**—Time between when Tx is enabled and data is actually transmitted. Maintain the default setting of 0x25.

l. **TX Stop Delay**—Time delay between the end of Tx and when the system returns to the Tx enable low setting. Maintain the default setting of 0x25.

m. **TX_RX Delay**— Time delay between a Tx enable low setting and an Rx enable high setting. Maintain the default setting of 0x50.

n. **RX Start Delay**—Time delay between an Rx enable high setting and data being received. Maintain the default setting of 0x0.

o. **TR_Switch Delay**—Time delay between Tx enable high and TR_SWITCH high. Maintain the default setting of 0x0.

p. **I/Q DAC ADC Int/Ext**—Maintain the default setting of internal, as the external DAC and ADC are not connected to the I/Q output and can only be used to capture data.

q. **I/Q DAC Output Control BB**—DAC output amplitude adjustment setting for baseband configuration.

r. **I/Q DAC Output Control RF**—DAC output amplitude adjustment setting for RF configuration.

s. **Bit Error Rate (BER) Resolution**—Ratio of incorrect bits to the correct bits. The BER Resolution conveys the accuracy of the BER. For example, a 10:3 ratio reflects a BER out of 1000 bits and a 10:9 ratio reflects a BER rate out of 1 billion bits.

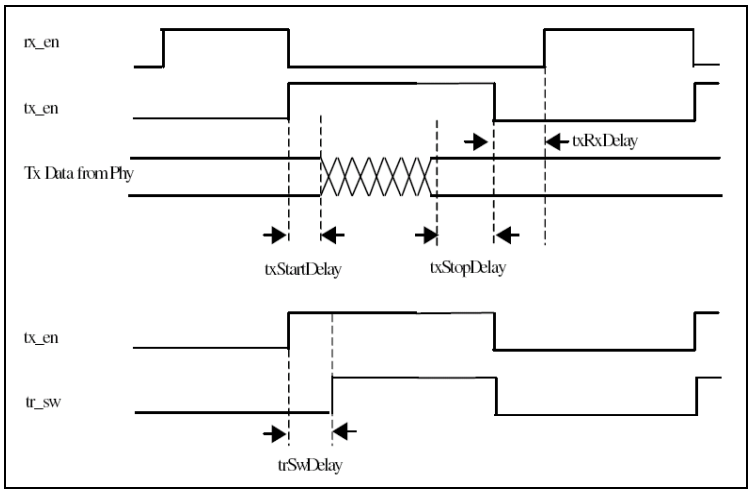
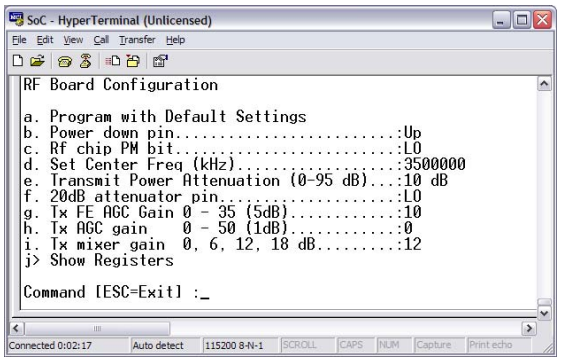


Figure 6: Tx and Rx Start/Stop Delay

3.1.3 RF Board Configuration Menu

Use the RF Board Configuration Menu to configure the RF Board. Each submenu is detailed below.



a. **Program with Default Settings**—Program the RF Board to factory default settings. The contents of the registers will reflect these default settings.

b. **Power down pin**—Control the digital line connected to the power down pin of the RF chip. This pin should be off for normal operation of the RF Board.

c. **Rf chip PM bit**—Manipulate the PM bit of the SYS0 register of the RF chip.

d. **Set Center Freq (KHz)**—Setup the RF center frequency. When the system is configured for TDD mode, you are prompted for a single center frequency that will be used for both Tx and Rx. In FDD mode you are prompted to enter a Tx frequency and an Rx frequency [Refer to Section 3.1.2, (c)]. Enter all frequencies in KHz.

   Tx and Rx frequencies must be reversed between Slave and Master for proper operation. It is important to ensure that the RF Board is capable of FDD mode operation *before* attempting this configuration. In FDD mode, Tx and Rx frequencies must be separated by 1MHz and the frequency channels must be 1MHz apart.

   The possible ranges of frequencies are:

   - 3.5MHz BW TDD radios:
     Center frequency range between 3,401,750 to 3,500,000KHz in 250KHz increments, e.g., Fc = 3,401,750 + 250n where n=0..393
   - 3.5MHz BW HD-FDD SS (Slave) radios:
     Tx center frequency range between 3,401,750 to 3,500,000KHz in 250KHz increments, e.g., Fc = 3,401,750 + 250n where n=0..393
     Rx center frequency range between 3,501,750 to 3,600,000KHz in 250KHz increments, e.g., Fc = 3,501,750 + 250n where n=0..393
   - 3.5MHz BW HD-FDD BS (Master) radios:
     Tx center frequency range between 3,501,750 to 3,600,000KHz in 250KHz increments, e.g., Fc = 3,501,750 + 250n where n=0..393
     Rx center frequency range between 3,401,750 to 3,500,000KHz in 250KHz increments, e.g., Fc = 3,401,750 + 250n where n=0..393
   - 7MHz BW TDD radios:
     Center frequency range between 3,403,500 to 3,500,000KHz in 250KHz increments, e.g., Fc = 3,403,500 + 250n where n=0..386
   - 7MHz BW HD-FDD SS (Slave) radios:
     Tx center frequency range between 3,403,500 to 3,500,000KHz in 250KHz increments, e.g., Fc = 3,403,500 + 250n where n=0..386
     Rx center frequency range between 3,503,500 to 3,600,000KHz in 250KHz increments, e.g., Fc = 3,503,500 + 250n where n=0..386
   - 7MHz BW HD-FDD BS (Master) radios:
     Tx center frequency range between 3,503,500 to 3,600,000KHz in 250KHz increments, e.g., Fc = 3,503,500 + 250n where n=0..386
     Rx center frequency range between 3,403,500 to 3,500,000KHz in 250KHz increments, e.g., Fc = 3,3403,500 + 250n where n=0..386

e. **Transmit Power Attenuation (0-95 dB)**—Control Tx power by attenuating the maximum possible Tx power by the given amount of attenuation. Values range between 0 to 95 dB of effective attenuation.

The next four (4) items under the RF Board Configuration Menu display current, read only values for the four attenuators on the RF Board.

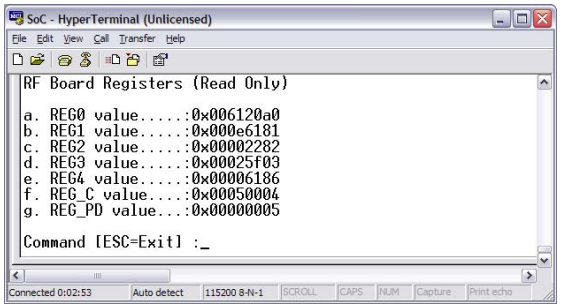
f. **20dB attenuator pin**

g. **Tx fe Agc Gain 0-35 (5dB steps**)

h. **Tx agc gain 0-50 (1dB steps**)

i. **Tx mixer gain (0, 6, 12, 18 dB**)

j. **Show Registers**—Display the read only RF Board Registers Menu. The RF Board is not automatically programmed with a modified register value. If you need to program the RF, do this after you manually modify each register value.



a. **Set REG0 Value**—Modify the SYS0 register of the RF chip.

b. **Set REG1 Value**—Modify the SYS1 register of the RF chip.

c. **Set REG2 Value**—Modify the SYS2 register of the RF chip.

d. **Set REG3 Value**—Modify the SYS3 register of the RF chip.

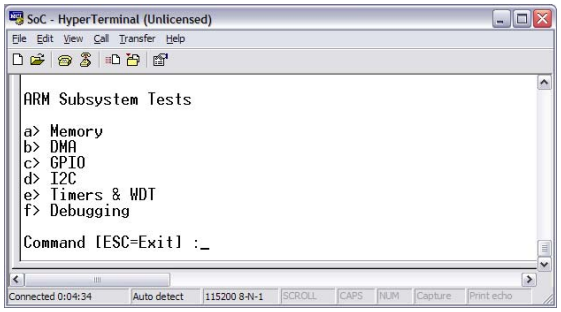
e. **Set REG4 Value**—Modify the SYS4 register of the RF chip.

f. **Set REG_C Value**—Modify the SYS_C register of the RF chip.

g. **Set REG_PD Value**—Modify the SYS_PD register of the RF chip.

3.1.4 ARM Subsystem Tests Menu

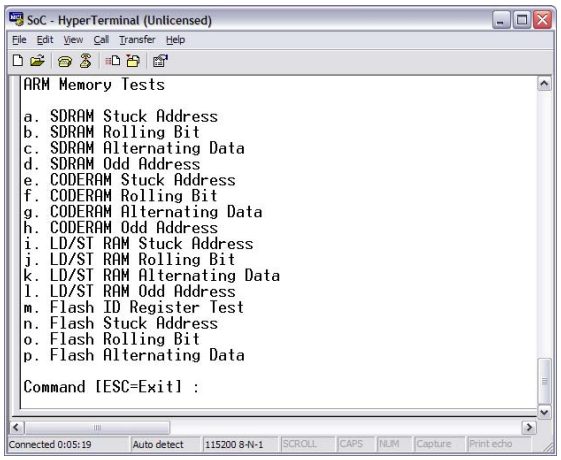
The Arm Subsystem Tests Menu lists six (6) specific sets of tests for ARM as described below.



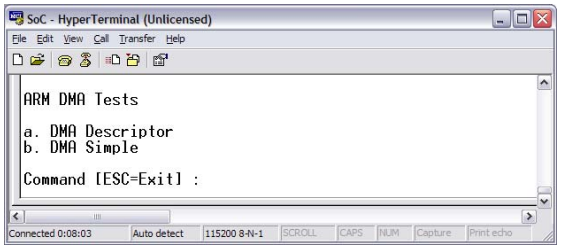
a. **Memory**—Internal and external memory tests for ARM as follows:

- **SDRAM** tests (**a-d**) are for the external SDRAM chip interfaced with the ARM subsystem.
- **Code Random Access Memory (CODERAM)** tests (**e-h**) verify the RAM memory contained in the ARC subsystem. This memory module is where the ARC executable is loaded and executes.

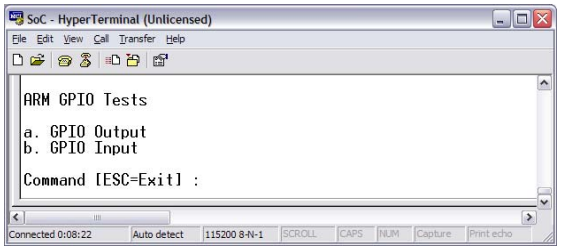
- **Load/Store (LD/ST)** tests (**i-l**) verify the load store RAM memory contained in the ARC subsystem. This memory module is where the interface between ARC and ARM occurs.
- **FLASH** tests (**m-p**) are geared to the external FLASH chip interfaced with the ARM subsystem. FLASH tests do not erase the software image.



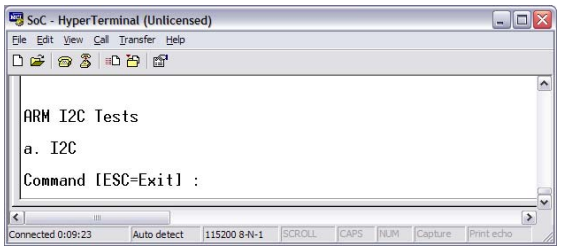
b. **Direct Memory Access (DMA)**—Test the general DMA of SoC in Descriptor or Simple mode.



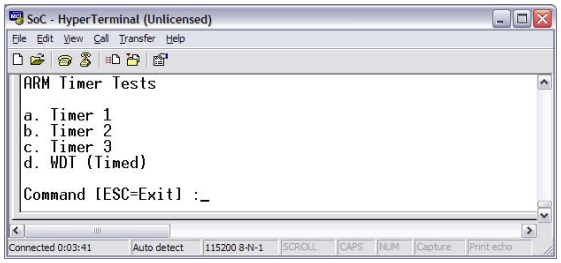
c. **GPIO**—Test the input/output functionality of the GPIO pins (4-11) of the ARM subsystem.



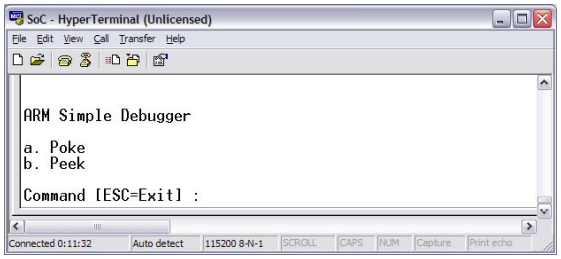
d. **I^2C** —Read the temperature (°C) of the SoC chip as measured by the on-chip sensor.



e. **Timers & WDT**—Verify that Timers 1, 2, 3, and the Watchdog Timer (WDT) are working. Testing the Timers and WDT does not reset the SoC Reference Board.



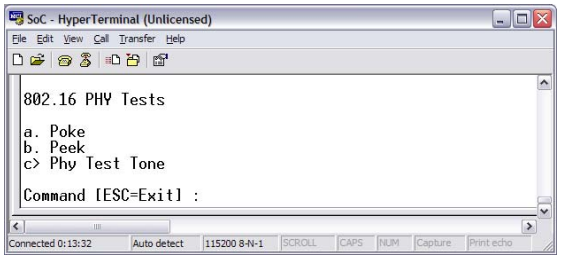
f. **Debugging**—Access two (2) ways to probe the ARM subsystem. **Poke** allows you to set a 32-bit value at a specific address location. **Peek** allows you to see the contents of a memory location.



3.1.5 802.16 PHY Tests Menu

The PHY Test Menu allows read and write access to the PHY registers. When writing to the PHY registers, the software default value to the registers is overwritten. By having PHY register access, the user can experiment with different PHY settings.

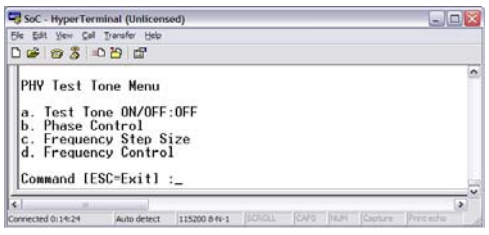
The PHY Test Menu has three (3) options that are used to interface the ARM to the PHY registers. For the PHY register memory map listing see the MB87M3400 data sheet.



a. **Poke**—Manipulate the PHY control registers. You are prompted to provide a PHY register address and the desired value of that register in Hexadecimal.

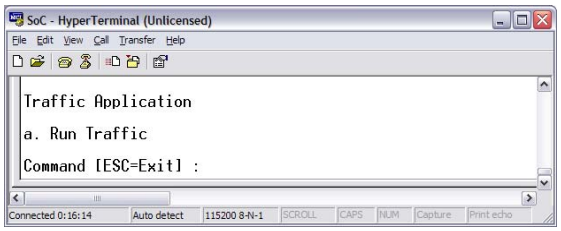
b. **Peek**—Read the contents of a PHY register. You are prompted to enter a PHY register address in Hexadecimal in order to display the contents of the register.

c. **Phy Test Tone**—Generate a sinusoidal signal. Turn the test tone utility on/off and manipulate the phase, size and tone of the test tone.



3.1.6 Traffic Application Menu

The Traffic Application Menu has only one option: **Run Traffic**.



a. **Run Traffic**—Start the Traffic application. In Master mode, Run Traffic commands SoC to transmit the Ethernet packets received at the RJ45 jack out through the PHY. In Slave mode with no Master connected**,** Run Traffic does not transfer data because the Slave is dependant on the Master Board to start the traffic process.

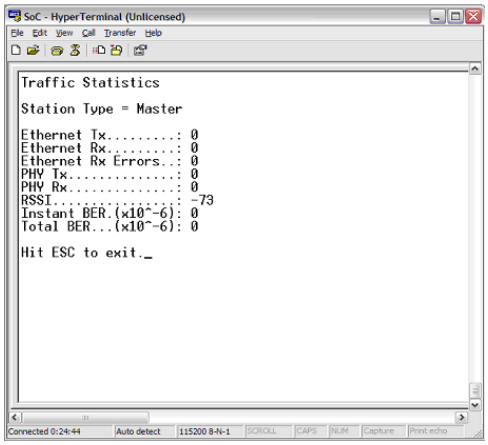
   If a Master and Slave are both used in either a Baseband or RF setup, the Slave will immediately sync to the signal transmitted from the Master to establish bi-directional traffic between the Slave and the Master Boards [see Section 3.1.2 (a)].

   Run Traffic also provides some statistics such as number of Ethernet packets received/transmitted and the number of PHY frames received/transmitted. Receiver Sensitivity Signal Strength (RSSI) and (BER) are also displayed on the screen.

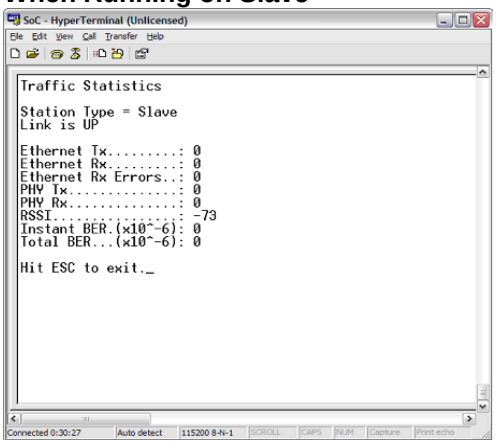
   The screenshots below show the traffic startup sequence for each type of Master/Slave configuration.

Traffic Startup Sequence

When Running and Connected on Master

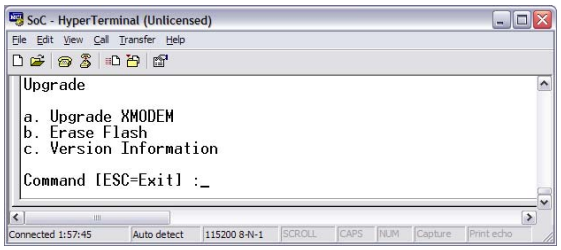


When Running on Slave



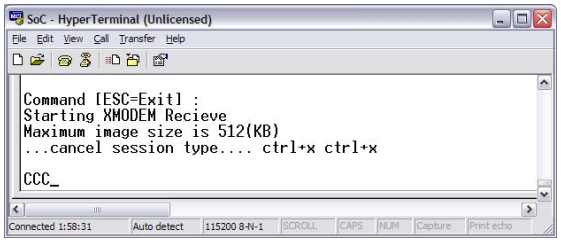
3.1.7 Upgrade Menu

The Upgrade Menu has three (3) operations, as described below.

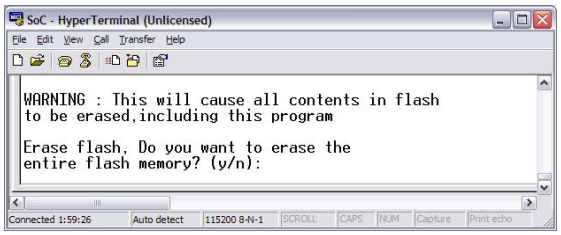


a. **Upgrade XMODEM**—Load a new version of the SoC software into the Flash chip using HyperTerminal. When the PC displays the HyperTerminal main menu, select **Transfer**, **Send File**. (Refer to Section 2.2 for details on how to configure HyperTerminal).

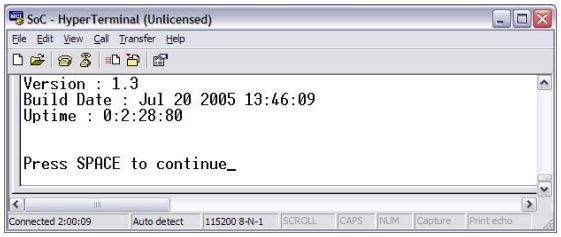
Ensure XMODEM 1K is selected as the transfer protocol, then locate the *.bin file (i.e., Pre-SoC-Ref-1-x.bin). Choose the *.bin file to begin Modem transfer. When the transfer is complete the firmware begins to update the contents of the Flash chip. Wait until the Upgrade Menu screen reappears, with a confirmation that the upgrade was successful. To run the newly upgraded software, you must reboot the system.



b. **Erase Flash**—This option is provided for advanced Flash chip programming purposes. **Caution: selecting this option completely erases the contents of the Flash chip.** This is not recommended, as the firmware will be lost.

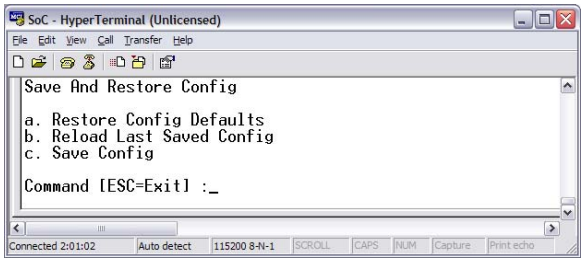


c. **Version Information**—Display version information for the SoC Reference Board software.



3.1.8 Save and Restore Configurations Menu

The Save and Restore Configurations Menu has three (3) options as described below.



a. **Restore Config Defaults**—Rollback the configuration parameters to factory default settings.

b. **Reload Last Saved Config**—Load the last saved configuration parameters into the system.

c. **Save Config**—Once you are satisfied with the configuration settings, save them on the Flash chip for future access.

APPENDICES

APPENDIX 1: DEFINITIONS AND ACRONYMS

ADC	Analog to Digital Converter
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
AHB	Advanced High Performance Bus
APB	Advanced Peripheral Bus
BER	Bit Error Rate
BS	Base Station
BWA	Broadband Wireless Access
CODERAM	Code Random Access Memory
DAC	Digital to Analog Converter
DDS	Direct Digital Synthesis
DIP	Dual In-line Package
DMA	Direct Memory Access
DSI	Direct Slave Interface
ETM	Embedded Test Module
FDD	Frequency Division Duplexing
FE	Front End
GPIO	General Purpose Input Output
HD	High Density
IC	Integrated Circuit
IEEE	Institute of Electrical Electronic Engineers
IF	Intermediate Frequency
LD/ST	Load/Store
LED	Light Emitting Diode
MAC	Media Access Control
PC	Personal Computer
PHY	Physical Layer
PLL	Phase Locked Loop
RF	Radio Frequency
RSSI	Receiver Sensitivity Signal Strength
RTOS	Real Time Operating System
Rx	Receive
SDRAM	Synchronous Dynamic Random Access Memory
SoC	System on Chip
SPI	Serial Peripheral Interface
SS	Subscriber Station
TDD	Time Division Duplexing
Tx	Transmit
UART	Universal Asynchronous Receiver Transmitter
UMAC	Upper Media Access Control
VCTCXO	Voltage Controlled Temperature Compensated Oscillator

Appendix 2: Reference Board Functional Description

1. INTRODUCTION

The SoC Reference Board consists of the following modules:

- 802.16 SoC.
- 20 MHz VCTCXO and DDS for generation of all system clocks.
- Memory components: Flash and SDRAM.
- Debug/development connectors: ARM MultiICE, ARM MultiTRACE, ARC Debugger, RS232 serial port.
- Ethernet PHY and connector.
- PowerPC connector for half-duplex BS testing.
- RF Board connector for connecting a RF deck such as the Radio Board.
- LEDs and DIP Switches for aiding software development/system integration.
- External high speed I&Q ADC and DAC.
- Reset supervisory and push button.

With the Radio Board the SoC Reference Board implements an 802.16 SS.

In the BS build configuration the SoC Reference Board can interface to a GDA MPC8560 PowerPC board to implement a half-duplex BS.

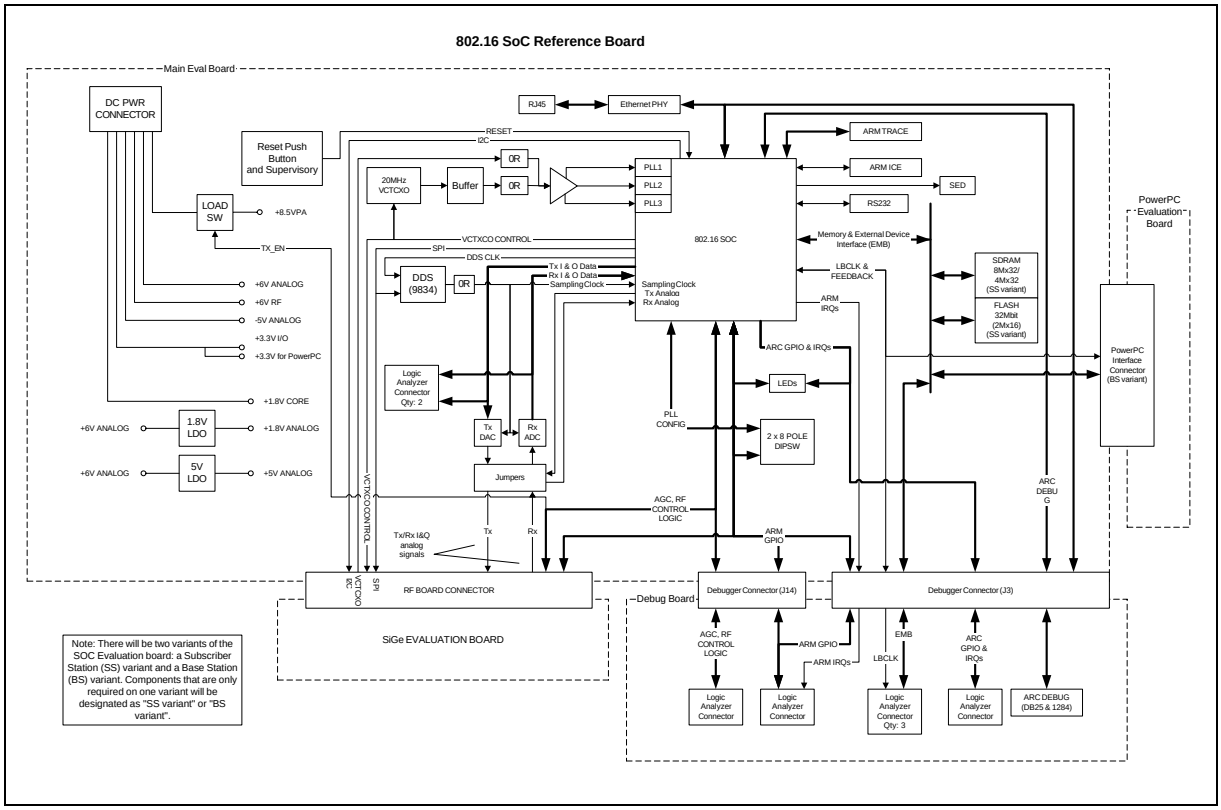


Figure A-1: SoC Reference Board Block Diagram

2. POWER SUPPLY

The SoC Reference Board requires a 48VDC input voltage @ 1A when configured as an SS. When configured as a BS the current requirement is 1.5A. The input voltage range can be 37VDC to 60VDC. The 48V power supply can be connected to the SoC Reference Board via a 2.5mm ID/ 5.5mm OD DC power jack [barrel connector, (J6)]. Inner pin is positive. Diode protection against polarity reversal is provided.

The 48V power supply feeds an isolated 48V to 12V power module. This power module feeds DC-to-DC converters to generate the following voltages:

- 1.8VDC@4A: SoC core voltage.
- 3.3VDC@0.5A/6A: SoC I/O voltage and digital components (0.5A)—Provides power to PowerPC Board in BS configuration (6A).
- 6VDC@1.5A: Analog components on SoC Reference Board. RF circuitry on Radio Board.
- 8.5VDC@1.5A: Tx power amp on Radio Board.
- -5VDC@0.1A: Analog components on SoC Reference Board.

The 1.8V core and 3.3V I/O rails are generated by Point of Load (POL) modules. The 6.0V and 8.5V rails are generated by LT1765 DC-to-DC converters. As RF circuitry is sensitive to power supply noise, the power supply rails for the Radio Board are kept separate from power supply rails for the SoC Reference Board. The 6.0V rail is partitioned into the 6.0VRF rail, which feeds the Radio Board and the 6.0VA rail, which feeds analog components on the SoC. The 8.5V power supply rail only feeds the Tx power amp on the Radio Board.

The SoC requires that power supplies be sequenced as follows: 1.8V core -> 3.3V I/O -> 1.8V analog on power up. The Intersil ISL6123 provides this sequencing. On power up it will sequentially turn on load switches that are gating these power supply rails.

3. DIGITAL ENGINE

3.1 Clocks

A 20 MHz VCTCXO is the main clock source for SoC Reference Board. It outputs a sinusoidal signal and feeds the RF LO, (intermediate Frequency) IF LO on the RF Board and digital Phase Locked Loops (PLLs) on the SoC.

The SoC's PLLs generate the following clocks:

- 160MHz ARM subsystem Clock (REFCLK1*8).
- 160MHz ARC subsystem Clock (REFCLK2*8).
- 100MHz PHY subsystem Clock (REFCLK3*5).
- 40 MHz DDS Synthesis Clock. (ARCCLK/4).

All of the above clocks are shown with default rates. However, each clock can be set to different rates as follows:

- ARM clock: 140, 160, 180 or 200 MHz;
- ARC clock: 140, 160, 180 or 200 MHz;
- PHY clock: 60 or 100 MHz; and
- DDS clock: 40, 80 or 160 MHz.

The VCTCXO frequency is centered on 20 MHz and is adjustable ±10ppm by the AFC function in the SoC. The AFC adjusts the VCTCXO frequency such that errors in the receive data from the access point are minimized.

The front-end clock for PHY subsystem is required to be variable to implement variable bandwidth. This is also used as the sampling clock for I & Q ADC and DAC. The front-end clock is generated by a Direct Digital Synthesis (DDS) device (U7, AD9834).

Table 1 shows the bandwidths supported by the SoC Reference Board. Each bandwidth has different filtering requirements in Baseband/IF/RF domain. The Radio Board only supports a bandwidth of either 3.5 or 7.0 MHz, depending on the build configuration (SAW filter).

Table 1: Supported Bandwidths

Bandwidth	Sampling Clock/ Front End Clock
1.5 MHz	3.440 MHz
3.0 MHz	6.880 MHz
5.5 MHz	12.640 MHz
1.75 MHz	4.000 MHz
3.5 MHz	8.000 MHz
7.0 MHz	16.000 MHz
10.0 MHz	23.040 MHz
14.0 MHz	32.000 MHz
20.0 MHz	46.080 MHz

3.2 Reset and Power Management

Power management is controlled by a voltage-monitoring supervisor, which holds the SoC at reset until the 3.3V I/O and 1.8V core supplies are up. If the 3.3V I/O falls below 88% or the 1.8V supply falls below 95% the voltage-monitoring supervisor will reset the SoC.

SoC can be reset manually by pressing push button S3, or by the voltage monitoring supervisor. After SoC is resent, the ARM subsystem boots up and holds ARC and PHY in reset mode. ARM then loads the ARC software into the on-chip ARC code memory and releases it from reset mode. When ARC boots up it releases the PHY from reset mode.

3.3 Digital Engine

- Interfaces to flash memory (16-bit data bus), and SDRAM memory (32-bit data bus)
- Interfaces to ARC core through internal Advanced High Performance Bus (AHB) bus
- MII interface to Ethernet Transceiver (AM79C874VI)
- RS-232 terminal interface to provide user interface to SoC Reference Board configuration
- Configures PLL synthesizers and Tx power settings on RF board
- Configures sampling clock frequency synthesizer (AD9834 DDS) through SPI port

Table 2: ARM I/O Pin Assignment

Signal	Description	Type	Location	Comments
VPEN	Flash Program Enable	Output	ARM_GPIO0	
/M_RESET	Ethernet Transceiver Reset	Output	ARM_GPIO1	
/RF_MEM_WP	RF EEPROM Write Protect	Output	ARM_GPIO2	
N/A	Not Used	N/A	ARM_GPIO3	
FE_AGC2	FE Tx Attenuation	Output	ARM_GPIO4	
FE_AGC1	FE Tx Attenuation	Output	ARM_GPIO5	
FE_AGC0	FE Tx Attenuation	Output	ARM_GPIO6	
SIGE_DATA	SE7051L Microwire Data	Output	ARM_GPIO9	
SIGE_CLK	SE7051L Microwire Clock	Output	ARM_GPIO10	
ANT_A_B_SW	Antenna A/B Switch	Output	ARM_GPIO11	
N/A	Not Used	N/A	ARM_GPIO12	
N/A	Not Used	N/A	ARM_GPIO13	
N/A	Not Used	N/A	ARM_GPIO14	
N/A	Not Used	N/A	ARM_GPIO15	
N/A	Not Used	N/A	ARM_GPIO16	
N/A	Not Used	N/A	ARM_GPIO17	
N/A	Not Used	N/A	ARM_GPIO18	
N/A	Not Used	N/A	ARM_GPIO19	
N/A	Not Used	N/A	ARM_GPIO20	
N/A	Not Used	N/A	ARM_GPIO21	
PD _SE7051L	Power down for SE7051L	Output	ARM_GPIO22	
SIGE_LE	SE7051L Microwire Latch Enable	Output	ARM_GPIO23	
ATT20	Tx Power-amp 20 dB Attenuation	Output	ARM_GPIO24	

Table 3: Interrupt Assignment

IRQx	Signal	Device	Description
0	ARM_EXT_IRQ0	SoC	FT_INT from SoC
1	ARM_EXT_IRQ1	Not Used	

Table 4: Chip Selects

Csx	Signal	Device	Width	Description
0	/ECS0	Flash	16-bit	Flash Read/Write
1	/ECS1	None	N/A	Not Used
2	/ECS2	None	N/A	Not Used
3	/ECS3	None	N/A	Not Used
4	/ECS4	SDRAM	32-bit	SDRAM Read/Write
5	/ECS5	None	N/A	Not Used. Spare SDRAM chip select

Table 5: Configuration Pins

Signal	Description	Default state SS mode	Default state BS mode
CMODE	Disables ARM subsystem when high. Used for BS mode	0 (ARM Enabled)	1 (ARM Disabled)
BOOT[1:0]	Selects 8, 16 or 32 bit boot device	01 (16-bit)	00
PLL1_SPEED[1:0]	Selects ARM subsystem PLL clock freq: 140, 160, 180, or 200MHz	01 (160MHz)	00 (N/A)
PLL2_SPEED[1:0]	Selects ARC subsystem PLL clock freq: 140, 160, 180 or 200MHz	01 (160MHz)	01 (160MHz)
PLL3_SPEED	Selects PHY subsystem PLL clock freq: 60 or 100 MHz	1 (100MHz)	1 (100MHz)
PLL1_S	ARM PLL enable	1 (enabled)	0 (disabled)
PLL2_S	ARC PLL enable	1 (enabled)	1 (enabled)
PLL3_S	PHY PLL enable	1 (enabled)	1 (enabled)

3.4 LEDs

ARM_GPIO[0:24] and ARC_GPIO[0:3] are routed to LEDs to aid testing and development with the SoC Reference Board.

Table 6: LED Routings

GPIO	LED
ARM_GPIO0	LD1
ARM_GPIO1	LD2
ARM_GPIO2	LD3
ARM_GPIO3	LD4
ARM_GPIO4	LD5
ARM_GPIO5	LD6
ARM_GPIO6	LD7
ARM_GPIO7	LD8
ARM_GPIO8	LD9
ARM_GPIO9	LD10
ARM_GPIO10	LD11
ARM_GPIO11	LD12
ARM_GPIO12	LD13
ARM_GPIO13	LD14
ARM_GPIO14	LD15

GPIO	LED
ARM_GPIO15	LD16
ARM_GPIO16	LD17
ARM_GPIO17	LD18
ARM_GPIO18	LD19
ARM_GPIO19	LD20
ARM_GPIO20	LD21
ARM_GPIO21	LD22
ARM_GPIO22	LD23
ARM_GPIO23	LD24
ARM_GPIO24	LD25
ARC_GPIO0	LD26
ARC_GPIO1	LD27
ARC_GPIO2	LD28
ARC_GPIO3	LD29

3.5 DIP Switches

DIP switches on the SoC Reference Board allow for ARM_GPIO level settings and PLL settings. For all DIP switches, setting the position to OFF causes logic level HIGH, while setting the position to ON causes logic level LOW. DIP switch settings for PLLs assume a REFCLK frequency of 20MHz.

Table 7: DIP Switch Default Settings

DIP SW	Signal	Default Setting
S1-1	ARM_GPIO8	OFF
S1-2	ARM_GPIO9	OFF
S1-3	ARM_GPIO10	OFF
S1-4	ARM_GPIO11	OFF
S1-5	ARM_GPIO12	OFF
S1-6	ARM_GPIO13	OFF
S1-7	ARM_GPIO14	OFF
S1-8	ARM_GPIO15	OFF

DIP SW	Signal	Default Setting
S2-1	ARM_GPIO16	OFF
S2-2	ARM_GPIO17	OFF
S2-3	PLL1_SPEED0	OFF
S2-4	PLL1_SPEED1	ON
S2-5	PLL2_SPEED0	OFF
S2-6	PLL2_SPEED1	ON
S2-7	PLL3_SPEED	OFF
S2-8	Not Used	N/A

Table 8: DIP Switch PLL Frequencies

S2-3	S2-4	PLL1 Multiplier	PLL1 Frequency (ARM)
ON	ON	7	140MHz
OFF	ON	8	160MHz (default)
ON	OFF	9	180MHz
OFF	OFF	10	200MHz

S2-5	S2-6	PLL2 Multiplier	PLL2 Frequency (ARC)
ON	ON	7	140MHz
OFF	ON	8	160MHz (default)
ON	OFF	9	180MHz
OFF	OFF	10	200MHz

S2-7	PLL3 Multiplier	PLL3 Frequency (PHY)
ON	3	60MHz
OFF	5	100MHz (default)

Table 9: Jumper Settings

Designator	Description	Settings
J7	RF Board FE_AGC routing	1-2: ARM_GPIO[6-4] routed to FE_AGC 2-3: AGC_CTRL[6-8] routed to FE_AGC (default)
J5	ARM_BYPASSYNC control	Must be installed for MultiICE to work
J8,J9 (only present on Rev. D)	20MHz Clock	J8 installed: RF board drives clock J9 installed: On board VCTCXO drives clock Either J8 or J9 to be installed not both. If no RF board is installed J9 must be installed for SoC to boot.

3.6 Memory Devices

- **SDRAM**—128Mb of SDRAM is configured as 4M x 32b. SDRAM is used for program execution and data storage. The SDRAM clock is 80MHz generated by the ARM subsystem's 160MHz clock (ARMCLK/2). The footprint is compatible with 256Mb and 512Mb devices. The SDRAM device is Micron P/N MT48LC4M32LFB5-10IT.
- **Flash**—The 32Mb of flash memory is configured as 2M x 16b. Flash memory is used for the boot loader and program images for the ARM and ARC subsystems. The footprint is compatible with 64Mb and 128Mb devices. The Flash device is Micron P/N MT28F320J3BS-11 ET. Signal VPEN, ARM_GPIO0 is used for write protection.

4. RS-232 INTERFACE

An RS-232 Interface connects to a terminal port to provide a menu-driven user interface for SoC configuration. Universal Asynchronous Receiver Transmitter (UART) in the ARM subsystem is connected to a RS-232 transceiver to provide a RS-232 port. The RS-232 port connector is a 9-pin Micro D-Sub connector. Molex P/N 83611-9006. Micro D-Sub to standard Dsub cables suitable for interfacing to a PC are available from Molex in 18", 36" and 72" lengths: 83421-9039, 83421-9040, 83421-9041. The RS-232 port connector pins are as follows:

1) Not Used
2) Transmit
3) Receive
4) Not Used
5) Ground
6) Not Used
7) Not Used
8) Not Used
9) Not Used

5. POWERPC CONNECTOR

The PowerPC connector (J20) is used in BS mode to interface to a PowerPC board. Power is provided to the PowerPC Board from 3.3V rail. The interface is designed for a GDA MPC8560 PowerPC board. The connector interfaces with the MPC8560 local bus data and address signals to the Direct Slave Interface (DSI) of SoC as well as IRQ signals and GPIOs.

Table 10: PowerPC Connector Signals

MPC8560 Signal	SoC Signal
LA[15:31]	LB_A[16:0]*
LD[0:31]	LB_D[31:0]*
LWE[0:3]	LB_BE[3:0]*
LGPL[0:2]	LBSIZE[0:2]
/LCS1	/LB_CS
LGPL4	LB_RDY
LGPL3	LB_W_/RD
/IRQ[0:2]	ARC_GPIO[0:2]
PA23	ARC_EXT_IRQ0
PA24	ARC_EXT_IRQ1

* A Big Endian to Little Endian interface requires the bus order to be reversed for these signals (i.e. LD[31] -> LB_D[0], LD[0] -> LB_D[31]).

6. ETHERNET TRANSCEIVER

Ethernet signals come into the SoC Reference Board through the 8-pin RJ45 and go through an Ethernet isolation transformer. This secondary transformer interfaces to the Ethernet transceiver. The Ethernet transceiver supports a MAC interface for 10/100Base-T operation and interfaces to the MAC module of the SoC's ARM subsystem via the MII interface.

LED Status indicators are provided on the PCB for the following:

- Transmit LD36
- Receive LD35
- Link LD37
- Duplex LD39
- Collision LD34
- 100BT LD33
- 10BT LD38

A SEMTECH diode array for ESD and Latch-up protection is on the primary side of the isolation transformer.

6.1 I²C bus

The I²C bus consists of a CSDA and a CSCL signal. Pull-up resistors are present on both these lines on the SoC Reference Board. These signals are present on the RF board connector (J23) to allow for storing of radio calibration data.

ARM_GPIO2 (/RF_MEM_WP) is used as a write protect for this device. An LM77 temperature sensor is placed on the I²C bus to allow testing of this interface.

6.2 ARC Subsystem

The ARC subsystem is intended to handle lower layer MAC functions. ARC interfaces to either the ARM subsystem in SS mode or to an external processor (e.g. PowerPC) in BS mode. ARC also interfaces to the 802.16 PHY and provides the only access to PHY from elsewhere in the system.

The ARC subsystem operates at a default 160MHz but can also operate at 140, 180 and 200MHz. Features of ARC include:

- ARC-4 RISC Core, Harvard Architecture.
- DES, AES-CCM, HCS, and CRC-32 hardware blocks.
- Extended Instructions for DEC, AES-CCM, HCS, and CRC-32.
- 64KB Load/Store Memory, 32KB CODERAM, 16KB Scratch Pad RAM.
- 6 Input Interrupts Lines.
- 15 GPIOs.
- Two (2) Timers.
- AHB Bus Interface for downloading to CODERAM and data transfer to/from LD/ST memory.
- DSI Bus Interface for External PowerPC processor or any other processor for BS functions.
- PHY Interface extended through the peripheral I/F.
- JTAG Debug Interface.

Table 11: I/O Assignments

Signal	GPIO	Description
PPC IRQ0	ARC_GPIO0	PowerPC Interrupt when operating as BS
PPC IRQ1	ARC_GPIO1	PowerPC Interrupt when operating as BS
PPC IRQ2	ARC_GPIO2	PowerPC Interrupt when operating as BS
CMODE	ARC_GPIO3	Indicates to ARC if configured as BS or SS

Table 12: Interrupt Assignments

Signal	IRQ
PPC PA23	ARC_EXT_IRQ0
PPC PA24	ARC_EXT_IRQ1

6.3 ARM Multi-ICE and ARM MultiTrace Ports

The ARM Multi-ICE port enables you to debug software running on the ARM processor. This port requires a Multi-ICE Interface unit with a 20-pin JTAG connector and debug software on the host PC.

The ARM MultiTrace port works in conjunction with ARM Multi-ICE to provide RealTrace functionality. The Multi-ICE connector plugs on to the MultiTrace debugger. A data port width of 8-bits has been implemented on the SoC.

The MultiTrace port must be run at half clock speed. This is configurable in the MultiTrace-enabled debugger running on the host PC.

6.4 ARC Debugger

The ARC debug signals are routed to a 200-pin Samtec SOLC connector (J3). The Debug Connector Board is required to connect to (J3) and bring the ARC debug signals to a DB-25 connector suitable for interfacing to a PC parallel port.

6.5 Debug Connectors

The Debug Connectors are two (2) Samtec SOLC connectors (200-pin and 120-pin) on the bottom of the SoC Reference Board [(J3) and (J14)]. Most of the digital signals that are useful for troubleshooting are routed to these connectors.

The Debug Connector Board makes these signals available on 38-pin MICTOR connectors suitable for connecting to a logic analyzer. It also serves double duty as an ARC debugger board.

6.6 SoC PHY Subsystem

Physical Layer Functionality for SoC includes:

- Mandatory Functionality:
  - Frequency Range: 2 – 11 GHz.
  - 256-point FFT.
  - 192 data carriers + 8 pilot carriers = 200 active carriers.
  - Forward Error Correction (FEC)—Concatenated Reed-Solomon/Viterbi. Mapping—BPSK, QPSK, 16-QAM with coding rates 1/2, 3/4.
  - Channel Quality Measurements.

- Optional Functionality:
  - 64-QAM with coding rates 2/3, 3/4.
  - Reed-Solomon Bypass (BPSK, Subchannels).
- Special Functions:
  - Alternate syncs.
  - Manufacturing Functions.

6.7 PHY Interface

PHY interface signals are described in Section 7, below.

PHY I & Q outputs are internally routed to on-chip high-speed ADC and DAC. These signals are also available in digital format for interfacing to external ADC and DAC.

6.8 Symbol Error Display (SED)

SED allows monitoring of PHY parameters for the purpose of debugging. Debugging is not limited to PHY testing but also RF testing in the field. Some parameters can be monitored without a software interface, while others require a software interface to read registered values.

The SED output is a 3-wire SPI interface designed to support a 12-bit serial DAC, such as Texas Instruments TLV5616.

On the SoC Reference Board SED interfaces with TLV5616. The output of TLV5616 is available on an MCX connector (J16).

7. RF AND ANALOG

7.1 RF Circuit Interface Signals

The RF circuit signals interface with the SoC on the Radio Board.

Table 13: RF Circuit Interface Signals

Signal	Signal Type/Direction	Description
AGC_CTRL[9:0]	Digital Output	Automatic Gain Control bus to control the Rx signal level on the Radio Board
AGC_STRB	Digital Output	Strobe for AGC_CTRL bus
/LD	Digital Input	PLL Lock detect from RF circuit
LD	Digital Input	PLL Lock detect from RF circuit
TX_EN	Digital Output	Transmitter Enable. Enables Tx path on Radio Board
RX_EN	Digital Output	Receiver Enable. Enables Rx path of Radio Board
TR_SW	Digital Output	Tx/Rx switch
RF_ENABLE	Digital Input	RF_ENABLE. Signal to allow external processor to enable the PHY RF interface when operating in BS mode
TX_PWR_DETECT	Analog Input	Input to power monitoring ADC
RX_PWR_DETECT	Analog Input	Input to power monitoring ADC
ATX_I_OUT+/-	Analog Output	High-speed 10-bit DAC differential analog output pair. Current output
ATX_Q_OUT+/-	Analog Output	High-speed 10-bit DAC differential analog output pair. Current output
ARX_I_IN+/-	Analog Input	High-speed 10-bit ADC differential analog input pair

Table 13: RF Circuit Interface Signals (continued)

Signal	Signal Type/Direction	Description
ATX_Q_OUT+/-	Analog Output	High-speed 10-bit DAC differential analog output pair. Current output
ARX_I_IN+/-	Analog Input	High-speed 10-bit ADC differential analog input pair
ARX_Q_IN+/-	Analog Input	High-speed 10-bit ADC differential analog input pair
ADC_DAC_CLK	Digital Output	Clock for digital I&Q outputs and inputs. For interfacing to external DAC and ADC.
BS_SYNC_OUT	Digital Output	BS Synchronization Output
BS_SYNC_IN	Digital Input	BS Synchronization Input
FT_INT	Digital Output	Frame Timer Interrupt
SED_CLK	Digital Output	Clock for Symbol Error Display (SED).
SED_DATA	Digital Output	Data for SED
SED_FS	Digital Output	Frame Synchronization for SED
DTX_I_OUT[9:0]	Digital Output	Digital outputs for interfacing to external DAC
DTX_Q_OUT[9:0]	Digital Output	Digital outputs for interfacing to external DAC
DRX_I_IN[9:0]	Digital Input	Digital inputs for interfacing to external ADC
DRX_Q_IN[9:0]	Digital Input	Digital inputs for interfacing to external ADC

7.2 RF Analog Interface

Due to differences in common mode voltage requirements between the SoC and the SE7051L a level shifting circuit is required on the receive path. On the SoC Reference Board Rev D this is implemented by differential op-amps U24 and U27. The SoC has common mode voltage requirement of 0.55V.

Since the output of the SoC DAC is in current mode, a resistor network is required on the Radio Board to provide a voltage level with the appropriate common mode voltage. This circuit needs to be physically close to the SE7051L modulator chip to minimize noise coupling. The SE7051L input requirements are 75 mVrms differential (nominal) and 13V-1.6V common mode.

7.3 FE_AGC[2:0] Multiplexing

FE_AGC[2:0] on SE7351L serves two functions:

- Tx mode: Transmit path attenuation at RF frequency.
- Rx mode: Receive path attenuation at RF frequency.

SoC is required to use AGC lines to control Rx attenuation. As a result, the AGC lines cannot be used for Tx attenuation. An external multiplexer (U35, SN74CB3Q3257) is required to properly interface these signals to the SE7351L.

The external multiplexer is controlled by a TR_SW signal. In Tx mode GPIOs are routed to the FE_AGC signals of SE7351L, while in Rx mode AGC signals are routed to SE7351L.

7.4 Power Monitoring

Monitor the power of the ADC radio receiver and transmitter. The voltage range for power monitoring is set internally in SoC at 0.825V-2.475V. This range can be overridden by driving the ADC2_VRH and ADC2-VRL pins of the SoC.

SoC pins for power monitoring are RX_POWER_DETECT and TX_POWER_DECTECT. These are exposed at the RF Board connector (J23).

The Radio Board has an AD8318 RF logarithmic power detector for Tx power detection. It is connected to the TX_POWER_DETECT pin of the SoC.

7.5 AFC

AFC is implemented by tuning 20MHz VCTCXO by +/- 10 ppm. SoC has a 12-bit AFC DAC for interfacing to the VCTCXO adjustment signal. DAC output comes out at pin VCTCXO_CNTL.

The AFC DAC voltage range is set to 0.5V – 2.5V at pins ADC2_VRH, ADC2_VRL to match Temex DVT4564A tuning voltage requirement of 1.5V +/- 1.0V for an adjustment of +/- 10 ppm.

7.6 RF Power Control and Monitoring

Tx power is controlled by the RF chipset through the Microwire interface and through the FE_AGC[2:0] and ATT20 signals (ARM_GPIO[4:6], ARM_GPIO24). This is controlled by the ARM subsystem.

The Radio Board has an AD8318 power monitoring device for monitoring Tx power. The RF signal is converted to a voltage that represents the power in dBm.

Power control for the Radio Board is user settable for up to 30 dBm. This device is connected to the TX_PWR_DETECT signal of SoC which is connected to an on-chip 10-bit ADC. ADC is read by the ARM subsystem through the APB bus.

7.7 RF Chipset Configuration

The ARM subsystem is responsible for writing configuration data to the SE7051L chip on the Radio Board in order to set the IF and RF frequencies and Tx power.

The signals required for the Radio Board configuration are:

- SIGE_DATA: SE7051L configuration data.
- SIGE_CLOCK: Clock for sending SE7051L configuration data.
- SIGE_LE: Latch enable for updating SE7051L with configuration data.
- FE_AGC[2:0]: SE7351L Tx power setting.
- ATT20: Tx power amp 20dB attenuation

7.8 RF Amplifier Control

/LD, LD—Lock detection signals that indicate when the RF PLLs are locked. /LD = LOW., while LD = HIGH. The /LD signal is active when the IF and RF PLLs on the Radio Board are locked. Both the /LD and LD signals must be locked for the TX_EN, RX_EN and TR_SW signals to operate.

TX_EN—Enables the transmit amplifier and the transmit paths for the SE7351L and SE7051L on the Radio Board.

RX_EN—Enables the receive paths for the SE7351L and SE7051L on the Radio Board.

I & Q High Speed ADC/DAC—Digital data transmitted from the PHY is converted to analog using a pair of 10-bit DACs. Similarly, analog data is converted to digital by the PHY using a pair of 10-bit

ADCs. Two (2) ADC/DACs are required for Quadrature Amplitude Modulation (QAM) to provide two streams of data, I and Q.

ADC/DAC sampling rates support the maximum data bandwidth of the system and oversampling requirements of the PHY. The maximum supported bandwidth is 20MHz with a sampling clock of 46MSPS.

ADC/DAC controls the inputs for registers such as output enable, data format (2's complement or binary) and power down. Registers are controlled by the PHY and are accessible by the ARM via ARC.

DAC requires an external reference of +1.1V. This is implemented on the SoC Reference Board by D9 and a resistor divider.

The ADC input range is 0.25V-0.85V. This is equivalent to a 0.6Vpp (1.2Vpp differential) signal with a common mode voltage of 0.55V.

Table 14: ADC and DAC Specifications

ADC Specifications	DAC Specifications
Resolution: 10 Bits	Resolution: 10 Bits
Data Throughput: 100MS/S	Data Throughput: 110MS/s
Data Format: Two's complement and binary.	Data Format: Binary
SNR (Signal to Noise Ratio at 10MHz input): 56dBFS min.	Spurious Free Dynamic Range with 110MHz clock: • At an output frequency of 110MHz/8 is –60DBc • At an output frequency of 110MHz/4 is –48DBc
SINAD (Signal to Noise and Distortion at 10MHz input): 54dBFS	
ENOB (Effective Number of Bits at 10MHz input): 8.7 bits	
SFDR (Spurious Free Dynamic Range at 10MHz): 60dBc	
THD (Total Harmonic Distortion at 10MHz input): -59dBc	

APPENDIX 3: CONNECTOR PINOUTS

Table 15: J3 Pinout—Debugger Connector

Pin	SS Name	BS Name	SS Description	BS Description
1	GND			
2	GND			
3	MA00	LBA00	Address Bus	Local Bus Address
4	MA01	LBA01	Address Bus	Local Bus Address
5	MA02	LBA02	Address Bus	Local Bus Address
6	GND			
7	MA03	LBA03	Address Bus	Local Bus Address
8	MA04	LBA04	Address Bus	Local Bus Address
9	MA05	LBA05	Address Bus	Local Bus Address
10	GND			
11	MA06	LBA06	Address Bus	Local Bus Address
12	MA07	LBA07	Address Bus	Local Bus Address
13	MA08	LBA08	Address Bus	Local Bus Address
14	GND			
15	MA09	LBA09	Address Bus	Local Bus Address
16	MA10	LBA10	Address Bus	Local Bus Address
17	MA11	LBA11	Address Bus	Local Bus Address
18	GND			
19	MA12	LBA12	Address Bus	Local Bus Address
20	MA13	LBA13	Address Bus	Local Bus Address
21	MA14	LBA14	Address Bus	Local Bus Address
22	GND			
23	MA15	LBA15	Address Bus	Local Bus Address
24	MA16	LBA16	Address Bus	Local Bus Address
25	MA17		Address Bus	
26	GND			
27	MA18		Address Bus	
28	MA19		Address Bus	
29	MA20		Address Bus	
30	GND			
31	MA21		Address Bus	
32	MA22		Address Bus	
33	MA23		Address Bus	
34	GND			
35	MA24		Address Bus	
36	MA25		Address Bus	
37	/CS0	LBSZ0	Chip Select	Local Bus Burst Size
38	GND			
39	/CS1	LBSZ1	Chip Select	Local Bus Burst Size
40	/CS2	LBSZ2	Chip Select	Local Bus Burst Size
41	/CS3		Chip Select	
42	GND			

Table 15: J3 Pinout—Debugger Connector (continued)

Pin	SS Name	BS Name	SS Description	BS Description
43	/CS4	LBRDYMD	Chip Select	Local Bus Ready Mode
44	/CS5	/LB_CS	Chip Select	Local Bus Chip Select
45	/WE0	/LB_BE0	SDRAM Write Enable	Local Bus Byte Enable
46	GND			
47	/WE1	/LB_BE1	SDRAM Write Enable	Local Bus Byte Enable
48	/WE2	/LB_BE2	SDRAM Write Enable	Local Bus Byte Enable
49	/WE3	/LB_BE3	SDRAM Write Enable	Local Bus Byte Enable
50	GND			
51	MII_TXD0		Ethernet Tx Data Bus	
52	MII_TXD1		Ethernet Tx Data Bus	
53	MII_TXD2		Ethernet Tx Data Bus	
54	GND			
55	MII_TXD3		Ethernet Tx Data Bus	
56	MII_TXCLK		Ethernet Tx Clock	
57	MII_TXEN		Ethernet Enable for Tx Data Bus	
58	GND			
59	MII_TXER			
60	MII_RXCLK		Ethernet Rx Clock	
61	MII_RXDV		Ethernet Rx Data Valid	
62	GND			
63	MII_RXER			
64	MII_COL		Ethernet Collision	
65	MII_CRS		Ethernet Carrier Sense	
66	GND			
67	MII_RXD0		Ethernet Rx Data Bus	
68	MII_RXD1		Ethernet Rx Data Bus	
69	MII_RXD2		Ethernet Rx Data Bus	
70	GND			
71	MII_RXD3		Ethernet Rx Data Bus	
72	MII_MDIO		Ethernet Management Data Input/Output	
73	MII_MDC		Ethernet Management Data Clock	
74	GND			
75	SPARE			
76	SPARE			
77	ARM_GPIO0		ARM General Purpose Input/Output	
78	GND			
79	ARM_GPIO1		ARM General Purpose Input/Output	
80	SD_CKE		SDRAM Clock Enable	
81	TXD1		UART Serial Tx Data	

Table 15: J3 Pinout—Debugger Connector (continued)

Pin	SS Name	BS Name	SS Description	BS Description
82	GND			
83	RXD1		UART Serial Rx Data	
84	SD_CLK		SDRAM Clock	
85	/PRESET		Power up reset	
86	GND			
87	SPARE			
88	GND			
89	SPARE			
90	GND			
91	SPARE			
92	3V3			
93	SPARE			
94	GND			
95	SPARE			
96	3V3			
97	3V3			
98	3V3			
99	3V3			
100	3V3			
101	GND			
102	GND			
103	MD00	LBD00	Data Bus	Local Bus Data
104	MD01	LBD01	Data Bus	Local Bus Data
105	MD02	LBD02	Data Bus	Local Bus Data
106	GND			
107	MD03	LBD03	Data Bus	Local Bus Data
108	MD04	LBD04	Data Bus	Local Bus Data
109	MD05	LBD05	Data Bus	Local Bus Data
110	GND			
111	MD06	LBD06	Data Bus	Local Bus Data
112	MD07	LBD07	Data Bus	Local Bus Data
113	MD08	LBD08	Data Bus	Local Bus Data
114	GND			
115	MD09	LBD09	Data Bus	Local Bus Data
116	MD10	LBD10	Data Bus	Local Bus Data
117	MD11	LBD11	Data Bus	Local Bus Data
118	GND			
119	MD12	LBD12	Data Bus	Local Bus Data
120	MD13	LBD13	Data Bus	Local Bus Data
121	MD14	LBD14	Data Bus	Local Bus Data
122	GND			
123	MD15	LBD15	Data Bus	Local Bus Data
124	MD16	LBD16	Data Bus	Local Bus Data

Table 15: J3 Pinout—Debugger Connector (continued)

Pin	SS Name	BS Name	SS Description	BS Description
125	MD17	LBD17	Data Bus	Local Bus Data
126	GND			
127	MD18	LBD18	Data Bus	Local Bus Data
128	MD19	LBD19	Data Bus	Local Bus Data
129	MD20	LBD20	Data Bus	Local Bus Data
130	GND			
131	MD21	LBD21	Data Bus	Local Bus Data
132	MD22	LBD22	Data Bus	Local Bus Data
133	MD23	LBD23	Data Bus	Local Bus Data
134	GND			
135	MD24	LBD24	Data Bus	Local Bus Data
136	MD25	LBD25	Data Bus	Local Bus Data
137	MD26	LBD26	Data Bus	Local Bus Data
138	GND			
139	MD27	LBD27	Data Bus	Local Bus Data
140	MD28	LBD28	Data Bus	Local Bus Data
141	MD29	LBD29	Data Bus	Local Bus Data
142	GND			
143	MD30	LBD30	Data Bus	Local Bus Data
144	MD31	LBD31	Data Bus	Local Bus Data
145	/RE	LB_W|/RD	Read Enable	Local Bus Read/Write
146	GND			
147	/SD_CAS		SDRAM Column Address Select	
148	/SD_RAS		SDRAM Row Address Select	
149	/SD_WE		SDRAM Write Enable	
150	GND			
151	CSDA		I^2C Data	
152	CSCL		I^2C Clock	
153	SPICLK		SPI CLK	
154	GND			
155	SPIDATAOUT		SPI Data Out	
156	/SPI_CS0		SPI Chip Select	
157	ARM_GPIO2		ARM General Purpose Input/Output	
158	GND			
159	/SPI_CS1		SPI Chip Select	
160	ARM_GPIO3		ARM General Purpose Input/Output	
161	ARM_EXT_IRQ0		ARM External Interrupt	
162	GND			
163	ARM_EXT_IRQ1		ARM External Interrupt	
164	ARC_EXT_IRQ0		ARC External Interrupt	

Table 15: J3 Pinout—Debugger Connector (continued)

Pin	SS Name	BS Name	SS Description	BS Description
165	ARC_EXT_IRQ1		ARC External Interrupt	
166	GND			
167	ARC_GPIO0		ARC General Purpose Input/Output	
168	ARC_GPIO1		ARC General Purpose Input/Output	
169	ARC_GPIO2		ARC General Purpose Input/Output	
170	GND			
171	ARC_GPIO3		ARC General Purpose Input/Output	
172	LB_CLK			
173	ARM_GPIO4		ARM General Purpose Input/Output	
174	GND			
175	ARM_GPIO5		ARM General Purpose Input/Output	
176	ARM_GPIO6		ARM General Purpose Input/Output	
177	ARM_GPIO7		ARM General Purpose Input/Output	
178	GND			
179	ARM_GPIO8		ARM General Purpose Input/Output	
180	ARM_GPIO9		ARM General Purpose Input/Output	
181	ARM_GPIO10		ARM General Purpose Input/Output	
182	GND			
183	ARM_GPIO11		ARM General Purpose Input/Output	
184	ARC_TDI		ARC Debugger Data In	
185	SPARE			
186	GND			
187	ARC_TMS		ARC Debugger Mode Select	
188	ARC_TCK		ARC Debugger Clock	
189	CLK_DDS		Clock for DDS synthesis	
190	GND			
191	ARC_TDO		ARC Debugger Data Out	
192	3V3			
193	ARC_SS1		ARM Debugger Port Reset	
194	GND			
195	SPARE			
196	3V3			
197	3V3			
198	3V3			
199	3V3			
200	3V3			

Table 16: J14 Pinout—Debugger Connector

Pin	Name	Description
1	ARM_GPIO12	ARM General Purpose Input/Output
2	GND	
3	ARM_GPIO13	ARM General Purpose Input/Output
4	ARM_GPIO14	ARM General Purpose Input/Output
5	ARM_GPIO15	ARM General Purpose Input/Output
6	GND	
7	ARM_GPIO16	ARM General Purpose Input/Output
8	ARM_GPIO17	ARM General Purpose Input/Output
9	ARM_GPIO18	ARM General Purpose Input/Output
10	GND	
11	ARM_GPIO19	ARM General Purpose Input/Output
12	ARM_GPIO20	ARM General Purpose Input/Output
13	ARM_GPIO21	ARM General Purpose Input/Output
14	GND	
15	ARM_GPIO22	ARM General Purpose Input/Output
16	ARM_GPIO23	ARM General Purpose Input/Output
17	ARM_GPIO24	ARM General Purpose Input/Output
18	GND	
19	SPARE	
20	SPARE	
21	SPARE	
22	GND	
23	AGC_CTRL0	Automatic Gain Control Bus
24	AGC_CTRL1	Automatic Gain Control Bus
25	AGC_CTRL2	Automatic Gain Control Bus
26	GND	
27	AGC_CTRL3	Automatic Gain Control Bus
28	AGC_CTRL4	Automatic Gain Control Bus
29	AGC_CTRL5	Automatic Gain Control Bus
30	GND	
31	AGC_STRB	Automatic Gain Control Bus
32	SPARE	
33	SPARE	
34	GND	
35	SPARE	
36	SPARE	
37	SPARE	
38	GND	
39	SPARE	
40	SPARE	
41	SPARE	
42	GND	
43	SPARE	
44	SPARE	

Table 16: J14 Pinout—Debugger Connector (continued)

Pin	Name	Description
45	SPARE	
46	GND	
47	SPARE	
48	SPARE	
49	SPARE	
50	GND	
51	SPARE	
52	SPARE	
53	SPARE	
54	GND	
55	5V	
56	3V3	
57	5V	
58	3V3	
59	5V	
60	3V3	
61	GND	
62	SPARE	
63	SPARE	
64	SPARE	
65	GND	
66	SPARE	
67	SPARE	
68	SPARE	
69	GND	
70	SPARE	
71	SPARE	
72	SPARE	
73	GND	
74	SPARE	
75	SPARE	
76	SPARE	
77	GND	
78	SPARE	
79	SPARE	
80	SPARE	
81	GND	
82	SPARE	
83	SPARE	
84	SPARE	
85	GND	
86	SPARE	
87	SPARE	

Table 16: J14 Pinout—Debugger Connector (continued)

Pin	Name	Description
88	SPARE	
89	GND	
90	SPARE	
91	TX_EN	Tx Enable
92	RX_EN	Rx Enable
93	GND	
94	TR_SW	Tx/Rx Switch
95	LD	
96	/LD	
97	GND	
98	AGC_CTRL6	Automatic Gain Control Bus
99	AGC_CTRL7	Automatic Gain Control Bus
100	SPARE	
101	GND	
102	SPARE	
103	SPARE	
104	SPARE	
105	GND	
106	SPARE	
107	AGC_STRB	Automatic Gain Control Strobe
108	SED_CLK	Symbol Error Display Clock
109	GND	
110	SED_DATA	Symbol Error Display Data
111	SED_FS	Symbol Error Display Frame Synchronization
112	SPARE	
113	SPARE	
114	BS_SYNC_IN	Base-Station Synchronization Input
115	BS_SYNC_OUT	Base-Station Synchronization Output
116	FT_INT	Frame Timer Interrupt Output
117	SPARE	
118	SPARE	
119	AGC_CTRL8	Automatic Gain Control Bus
120	AGC_CTRL9	Automatic Gain Control Bus

Table 17: J23 Pinout—RF Board Connector

Pin	Name	Description
1	20MHZ_RFCLK	20 MHz oscillator for RF frequency synthesizers
2	ARM_GPIO11	ARM General Purpose Input/Output
3	ARM_GPIO10	ARM General Purpose Input/Output
4	ARM_GPIO23	ARM General Purpose Input/Output
5	ARM_GPIO22	ARM General Purpose Input/Output
6	SPIDATAIN	
7	ARM_GPIO21	ARM General Purpose Input/Output
8	ARM_GPIO20	ARM General Purpose Input/Output
9	ARM_GPIO19	ARM General Purpose Input/Output
10	ARM_GPIO11	ARM General Purpose Input/Output
11	AGC_CTRL5	Automatic Gain Control Bus
12	AGC_CTRL4	Automatic Gain Control Bus
13	AGC_CTRL3	Automatic Gain Control Bus
14	AGC_CTRL2	Automatic Gain Control Bus
15	AGC_CTRL1	Automatic Gain Control Bus
16	AGC_CTRL0	Automatic Gain Control Bus
17	ARM_GPIO18	ARM General Purpose Input/Output
18	ARM_GPIO17	ARM General Purpose Input/Output
19	ARM_GPIO16	ARM General Purpose Input/Output
20	LD	Lock Detect output from radio
21	TR_SW	Tx/Rx Switch
22	AGND	
23	AGND	
24	ARM_GPIO15	ARM General Purpose Input/Output
25	ARM_GPIO14	ARM General Purpose Input/Output
26	ARM_GPIO13	ARM General Purpose Input/Output
27	ARM_GPIO12	ARM General Purpose Input/Output
28	RX_PWR_DECTECT	Rx Power Detection from radio
29	ARM_GPIO10	ARM General Purpose Input/Output
30	ARM_GPIO9	ARM General Purpose Input/Output
31	ARM_GPIO8	ARM General Purpose Input/Output
32	ARM_GPIO7	ARM General Purpose Input/Output
33	FE_AGC0	Multiplexed Automatic Gain Control/ Transmitter Power Control for SE7351L Front End
34	FE_AGC1	Multiplexed Automatic Gain Control/ Transmitter Power Control for SE7351L Front End
35	FE_AGC2	Multiplexed Automatic Gain Control/ Transmitter Power Control for SE7351L Front End
36	AGC_CTRL9	Automatic Gain Control Bus
37	ARM_GPIO24	ARM General Purpose Input/Output
38	TX_PWR_DETECT	Tx Power Detection from radio
39	TX_EN	Tx Enable
40	RX_EN	Rx Enable
41	DGND	

Table 17: J23 Pinout—RF Board Connector (continued)

Pin	Name	Description
42	ARM_GPIO2	ARM General Purpose Input/Output
43	AGND	
44	AGND	
45	8V5	Voltage for power amp. Switched by TX_EN
46	8V5	Voltage for power amp. Switched by TX_EN
47	AGND	
48	AGND	
49	8V5	Voltage for power amp. Switched by TX_EN
50	8V5	Voltage for power amp. Switched by TX_EN
51	VCTCXO_CNTL	Control Voltage for 20MHz oscillator
52	/LD	Lock Detect output from radio (active low)
53	AGND	
54	AGND	
55	ARX_I_IN+	Demodulated Analog Rx signal from radio
56	ARX_I_IN-	Demodulated Analog Rx signal from radio
57	AGND	
58	6V	Voltage for RF circuitry excluding power amp
59	6V	Voltage for RF circuitry excluding power amp
60	AGND	
61	ARX_Q_IN+	Demodulated Analog Rx signal from radio
62	ARX_Q_IN-	Demodulated Analog Rx signal from radio
63	AGND	
64	6V	Voltage for RF circuitry excluding power amp
65	6V	Voltage for RF circuitry excluding power amp
66	AGND	
67	AGND	
68	6V	Voltage for RF circuitry excluding power amp
69	6V	Voltage for RF circuitry excluding power amp
70	6V	Voltage for RF circuitry excluding power amp
71	AGND	
72	ATX_I_OUT-	Analog Tx signal to radio
73	ATX_I_OUT+	Analog Tx signal to radio
74	AGND	
75	ATX_Q_OUT+	Analog Tx signal to radio
76	ATX_Q_OUT-	Analog Tx signal to radio
77	AGND	
78	CSDA	I^2C Data
79	CSCL	I^2C Clock
80	6V	Voltage for RF circuitry excluding power amp
81	6V	Voltage for RF circuitry excluding power amp
82	DGND	
83	DGND	
84	5V	

Table 17: J23 Pinout—RF Board Connector (continued)

Pin	Name	Description
85	DGND	
86	5V	
87	DGND	
88	-5V	
89	DGND	
90	3V3	
91	DGND	
92	3V3	
93	AGND	
94	AGND	
95	8V5	Voltage for power amp. Switched by TX_EN
96	8V5	Voltage for power amp. Switched by TX_EN
97	AGND	
98	AGND	
99	8V5	Voltage for power amp. Switched by TX_EN
100	8V5	Voltage for power amp. Switched by TX_EN

Table 18: J20 Pinout—PowerPC Board Connector

Pin	SS Name	BS Name	SS Description	BS Description
1	ARM_GPIO24		ARM General Purpose Input/Output	
2	SPARE			
3	SPARE			
4	SPARE			
5	SPARE			
6	SPARE			
7	SPARE			
8	SPARE			
9	SPARE			
10	SPARE			
11	SPARE			
12	SPARE			
13	SPARE			
14	SPARE			
15	SPARE			
16	SPARE			
17	SPARE			
18	SPARE			
19	ARM_GPIO22		ARM General Purpose Input/Output	
20	SPARE			
21	SPARE			
22	PPC_LSYNC_IN			PowerPC Local Bus Synchronization Input
23	SPARE			
24	GND			
25	SPARE			
26	PPC_LSYNC_OUT			PowerPC Local Bus Synchronization Output
27	SPARE			
28	GND			
29	ARM_GPIO6		ARM General Purpose Input/Output	
30	SPARE			
31	CSCL		I^2C Clock	
32	GND			
33	CSDA		I^2C Data	
34	SPARE			
35	ARM_GPIO2		ARM General Purpose Input/Output	
36	GND			
37	SPARE			
38	LB_CLK			Local Bus Clock
39	ARC_GPIO0		ARC General Purpose Input/Output	
40	GND			
41	ARC_GPIO1		ARC General Purpose Input/Output	

Table 18: J20 Pinout—PowerPC Board Connector (continued)

Pin	SS Name	BS Name	SS Description	BS Description
42	SPARE			
43	ARC_GPIO2		ARC General Purpose Input/Output	
44	SPARE			
45	FT_INT		Frame Timer Interrupt Output	
46	SPARE			
47	BS_SYNC_OUT		Base-Station Synchronization Output	
48	SPARE			
49	SPARE			
50	SPARE			
51	SPARE			
52	SPARE			
53	SPARE			
54	SPARE			
55	SPARE			
56	SPARE			
57	SPARE			
58	SPARE			
59	SPARE			
60	SPARE			
61	SPARE			
62	SPARE			
63	ARC_EXT_IRQ1		ARC External Interrupt	
64	SPARE			
65	SPICLK		SPI CLK	
66	SPARE			
67	GND			
68	BS_SYNC_IN		Base-Station Synchronization Input	
69	/SPI_CS0		SPI Chip Select	
70	SPARE			
71	ARC_EXT_IRQ0		ARC External Interrupt	
72	GND			
73	SPIDATAOUT		Spi Data Output	
74	LB_RDY			Local Bus Ready Mode
75	SPARE			
76	GND			
77	/RE	LB_W|/RD	Read Enable	Local Bus Read/Write
78	GND			
79	RF_ENABLE		PHY RF Circuitry Enable	
80	/CS2	LBSZ2	Chip Select	Local Bus Burst Size
81	SPARE			
82	ARM_GPIO5		ARM General Purpose Input/Output	
83	/EXT_RESET		External Reset	
84	MD15	LBD15	Data Bus	Local Bus Data

Table 18: J20 Pinout—PowerPC Board Connector (continued)

Pin	SS Name	BS Name	SS Description	BS Description
85	/CS1	LBSZ1	Chip Select	Local Bus Burst Size
86	MD14	LBD14	Data Bus	Local Bus Data
87	ARM_GPIO4		ARM General Purpose Input/Output	
88	MD13	LBD13	Data Bus	Local Bus Data
89	/CS0	LBSZ0	Chip Select	Local Bus Burst Size
90	MD12	LBD12	Data Bus	Local Bus Data
91	ARM_GPIO23		ARM General Purpose Input/Output	
92	MD11	LBD11	Data Bus	Local Bus Data
93	/WE0	/LB_BE0	SDRAM Write Enable	Local Bus Byte Enable
94	MD10	LBD10	Data Bus	Local Bus Data
95	GND			
96	MD09	LBD09	Data Bus	Local Bus Data
97	/WE1	/LB_BE1	SDRAM Write Enable	Local Bus Byte Enable
98	MD08	LBD08	Data Bus	Local Bus Data
99	GND			
100	MD07	LBD07	Data Bus	Local Bus Data
101	/WE2	/LB_BE2	SDRAM Write Enable	Local Bus Byte Enable
102	MD06	LBD06	Data Bus	Local Bus Data
103	SPARE			
104	MD05	LBD05	Data Bus	Local Bus Data
105	/WE3	/LB_BE3	SDRAM Write Enable	Local Bus Byte Enable
106	MD04	LBD04	Data Bus	Local Bus Data
107	GND			
108	MD03	LBD03	Data Bus	Local Bus Data
109	SPARE			
110	MD02	LBD02	Data Bus	Local Bus Data
111	GND			
112	MD01	LBD01	Data Bus	Local Bus Data
113	SPARE			
114	MD00	LBD00	Data Bus	Local Bus Data
115	/CS5_/LB_CS		Chip Select	Local Bus Chip Select
116	GND			
117	SPARE			
118	SPARE			
119	MA15	LBA15	Address Bus	Local Bus Address
120	GND			
121	MA14	LBA14	Address Bus	Local Bus Address
122	MD31	LBD31	Data Bus	Local Bus Data
123	MA13	LBA13	Address Bus	Local Bus Address
124	MD30	LBD30	Data Bus	Local Bus Data
125	MA12	LBA12	Address Bus	Local Bus Address
126	MD29	LBD29	Data Bus	Local Bus Data
127	MA11	LBA11	Address Bus	Local Bus Address

Table 18: J20 Pinout—PowerPC Board Connector (continued)

Pin	SS Name	BS Name	SS Description	BS Description
128	MD28	LBD28	Data Bus	Local Bus Data
129	MA10	LBA10	Address Bus	Local Bus Address
130	MD27	LBD27	Data Bus	Local Bus Data
131	MA09	LBA09	Address Bus	Local Bus Address
132	MD26	LBD26	Data Bus	Local Bus Data
133	MA08	LBA08	Address Bus	Local Bus Address
134	MD25	LBD25	Data Bus	Local Bus Data
135	MA07	LBA07	Address Bus	Local Bus Address
136	MD24	LBD24	Data Bus	Local Bus Data
137	MA06	LBA06	Address Bus	Local Bus Address
138	MD23	LBD23	Data Bus	Local Bus Data
139	MA05	LBA05	Address Bus	Local Bus Address
140	MD22	LBD22	Data Bus	Local Bus Data
141	MA04	LBA04	Address Bus	Local Bus Address
142	MD21	LBD21	Data Bus	Local Bus Data
143	MA03	LBA03	Address Bus	Local Bus Address
144	MD20	LBD20	Data Bus	Local Bus Data
145	MA02	LBA02	Address Bus	Local Bus Address
146	MD19	LBD19	Data Bus	Local Bus Data
147	MA01	LBA01	Address Bus	Local Bus Address
148	MD18	LBD18	Data Bus	Local Bus Data
149	MA00	LBA00	Address Bus	Local Bus Address
150	MD17	LBD17	Data Bus	Local Bus Data
151	MA16	LBA16	Address Bus	Local Bus Address
152	MD16	LBD16	Data Bus	Local Bus Data

Table 19: J4 Pinout—Serial Connector

Pin	Name	Description
1	N/A	
2	TX_RS232	RS232 Serial Data Output
3	RX_RS232	RS232 Serial Data Input
4	N/A	
5	GND	
6	N/A	
7	N/A	
8	N/A	
9	N/A	

Table 20: J1 Pinout—ARM MultiICE Connector

Pin	Name	Description
1	3V3	
2	3V3	
3	ARM_NTRST	ARM JTAG Test Port Reset
4	GND	
5	ARM_TDI	ARM JTAG Test Data In
6	GND	
7	ARM_TMS	ARM JTAG Test Mode Select
8	GND	
9	ARM_TCK	ARM JTAG Test Clock
10	GND	
11	ARM_RTCK	ARM JTAG Return Test Clock
12	GND	
13	ARM_TDO	ARM JTAG Test Data Out
14	GND	
15	/PRESET	Power-up Reset
16	GND	
17	DBGRQ	ARM JTAG Debug Request
18	GND	
19	DBGACK	ARM JTAG Debug Acknowledge
20	GND	

Table 21: J19 Pinout—ARM MultiTRACE Connector

Pin	Name	Description
1	N/A	
2	N/A	
3	N/A	
4	N/A	
5	GND	
6	TRACECLK	ARM Trace Clock
7	DBGRQ	ARM JTAG Debug Request
8	DBGACK	ARM JTAG Debug Acknowledge
9	/PRESET	Power-up Reset
10	N/A	
11	ARM_TDO	ARM JTAG Test Data Out
12	3V3	
13	ARM_RTCK	ARM JTAG Return Test Clock
14	3V3	
15	ARM_TCK	ARM JTAG Test Clock
16	TRACEPKT7	ARM Trace Packet Data
17	ARM_TMS	ARM JTAG Test Mode Select
18	TRACEPKT6	ARM Trace Packet Data
19	ARM_TDI	ARM JTAG Test Data In
20	TRACEPKT5	ARM Trace Packet Data
21	ARM_NTRST	ARM JTAG Test Port Reset
22	TRACEPKT4	ARM Trace Packet Data
23	GND	
24	TRACEPKT3	ARM Trace Packet Data
25	GND	
26	TRACEPKT2	ARM Trace Packet Data
27	GND	
28	TRACEPKT1	ARM Trace Packet Data
29	GND	
30	TRACEPKT0	ARM Trace Packet Data
31	GND	
32	TRACESYNC	ARM Trace Synchronization Signal
33	GND	
34	PIPESTAT2	ARM Pipeline Status
35	GND	
36	PIPESTAT1	ARM Pipeline Status
37	GND	
38	PIPESTAT0	ARM Pipeline Status

APPENDIX 4: REFERENCE BOARD BILL OF MATERIALS (BOM)

Qty	Reference	Description	Part Number	Manufacturer
4	C50-53	CAP MONO 0805 0.1UF 50V X7R	GMC21X7R104J50NT	CAL-CHIP
4	C46 C49 C100 C600	CAP 1210 4.7UF 16V X5R	CC1210KRX7R7BB475	KYOCERA
1	C201	CAP ELEC SMD 1000UF 25V	NACZ102M25V12.5X14	NIC COMPONENTS
1	C23	CAP ELEC SMD 33UF 100V	EEV-HA2A330P	PANASONIC
2	C43 C604	CAP X7R 0603 0.10UF 25VDC 10%	06033C104KAT	AVX
1	C211	CAP CERAMIC 0805 1UF 10V Y5V	0805ZG105ZAT2A	AVX
57	C4-14 C21 C25 C32-34 C57-60 C64-65 C75-84 C86-96 C205-206 C210 C413 C415-416 C420-427	CAP CERAMIC 1210 10UF 10V X5R	1210ZD106KAT2A	AVX
1	C207	CAP MONO 0402 10PF 25V 2% COG	650L100JT	ATC
2	C97 C209	CAP MONO 0402 100PF 50V 5% COG	04025A101KAT2A	AVX
7	C27 C44 C66-69 C601	CAP MONO 0402 1000PF 50V 5% X7R	04025C102JAT2A	AVX
12	C26 C61-63 C98-99 C216 C220-222 C232 C412	CAP CER 16V 0.01UF 16V 10% X7R 0402	0402YC103KAT2A	AVX
203	C1-3 C15-20 C28-29 C42 C101-145 C148-200 C203-204 C212 C223-231 C233 C245-287 C289-304 C323-341 C344 C603	CAP CER 10V 0.1U 10% 0402 X5R	0402ZD104KAT2A	AVX
6	C55-56 C70-73	CAP MCNC 0402 22PF 50V 5% COG	04025A220JAT2A	AVX
1	C217	CAP MCNC 0402 0.022UF 16V 5% X7R	0402YC223JAT2A	AVX
2	C74 C85	CAP MCNC 0402 47PF 5% 50V COG	04025A470JAT2A	AVX
1	C219	CAP 0402 0.047UF 16V +80%/-20% Y5V	0402YG473ZA	AVX
1	C405	CAP MCNC 0402 56PF 5% 50V COG	04025A560JAT2A	AVX
1	C401	CAP MCNC 0402 68PF 5% 50V COG	04025A680JAT2A	AVX
1	C404	CAP MCNC 0402 82PF 5% 50V COG	04025A820JAT2A	AVX
2	C213-214	CAP TANT SMD_A 1UF 20V 20%	NTC-T105M20	NIC COMPONENTS
1	C218	CAP MCNC 0402 0.033UF 10V5%X7R	0402ZC333JAT2A	AVX
2	C402-403	CAP MONO 6.8PF 0402 25V COG	650L6R8BT 25T	ATC
1	C202	CAP TANT SMD_C 22UF 16V 20%	F931C226MC	NICHICON
2	C40-41	CAP TANT SMD_D 47UF 10V 10%	PCT47/10DK	NEMCO
1	C215	CAP TANT SMD D 100UF 10V 10%	TPSD107K010R0065	AVX
2	C45 C602	CAP TANT SMD E 100UF 16V 10%	TPSE107K016R0100	AVX
1	C54	CAP 1812 1000PF 2KV X7R 10%	1812GC102KA11A	AVX
4	C22 C30-31 C35	CAP 1812 0.01UF 60 0V X7R 10%	1812CC103KAT2A	AVX
1	C24	CAP SMD_C 68UF 6.3V 20% (ROHS - PB FREE)	NOJC686M006RWJ	AVX
1	L8	FERRITE BEAD 1206 3A 120R@100M	BLM31P121SG	MURATA

Qty	Reference	Description	Part Number	Manufacturer
35	L1 L3 L6-7 L9-12 L14-16 L21 L25-26 L28-29 L33-38 L127 Z1-12	FERRITE BEAD 0603 4A 27R	EXCML16A270U	PANASONIC
2	L24 L27	IND COILCRAFT 3.3UH SMD 6.4A	DO3316P-332	COILCRAFT
2	L19 L43	IND COMMON MODE 4000R 4A	CM3322P400R-00	STEWARD
5	L2 L4-5 L13 L22	IND COIL 6.8MH SMT 1.4A	DO1608C-682	COILCRAFT
2	L17-18	IND 1210 1.5UH 20%	380LB-1R5M	TOKO
2	L600 L30	IND POWER SMD 4.7 UH 2.2A	LQH66SN4R7M01	MURATA
2	XJ5 XJ9	SHUNT 2 PIN 2MM	2SN-BK-G	SAMTEC
1	J22	CONN DIL 2X5 PIN 0.1" SMT	TSM-105-01-L-DV	SAMTEC
1	J20	CONN 152 PIN MICTOR RECEPTACLE	2-767004-5	AMP/TYCO
1	J10	CONNECTOR DC PLUG 2.5MM	PJ-002B-SMT	CUI Inc.
3	J17-19	CONN 38PIN RCPTCL 0.64 CL	2-767004-2	AMP/TYCO
1	J7	CONN 1X3PIN 2MM 0.126" H SMT	TMM-103-01-G-S-SM (P)	SAMTEC
3	J5 J8-9	CONN 1X2PIN 2MM 0.126"H SMT	TMM-102-01-G-S-SM	SAMTEC
1	J1	TOP SHROUD TERMINAL STRIP	TST-110-01-S-D	SAMTECH
1	J4	CONN COMMERCIAL MICRO-D PLUG	83611-9006	MOLEX
1	J2	CONN RJ45S W/CONDUCT GASKET	155-P3-8-1	REGAL ELECTRONICS
1	J16	CONN RF MCX PCB JCK GGS	82MCX-50-0-17/111NH	HUBER & SUHNER
1	J14	CONN 4X30 PIN SOLC	SOLC-130-02-S-Q-LC	SAMTEC
1	J3	CONN 4X50 PIN SOLC	SOLC-150-02-S-Q-LC	SAMTEC
1	J23	CONNECTOR - QUAD ROW TERMINAL SMT	TOLC-125-02-F-Q-LC	SAMTEC
1	Y1	CRYSTAL 20M 50PPM HC49S	ECS-200-S-5P	ECS
1	X2	CRYSTAL 25M 50 PPM -40C TO+85C	PM-2MM 25.0000MHZ	M-TRON
1	X1	VCTCXO 20MHZ SMD +3V 4.0PPM	SBTO16DDVY20.000MHz	SANGSHIN
1	D6	LED RECT RD SMD	SML-LX1206IC	LUMEX
51	D1 D3 D605 LD1-48	LED GREEN 0603	SML-LX0603GW-TR	LUMEX
6	H7-12	STANDOFF FLARE-MOUNTED #6-32 0.250" L	KFB3-632-8ET	PENN ENGINEERING
1	U16	IC SDRAM 128MBIT VFBGA 90	MT48LC4M32LFB5-10 IT	MICRON
1	U23	IC 10-BIT 80 MPSP DUAL D/A CONVERTER	AD9218BST-80	ANALOG DEVICES
1	U25	IC 10-BIT 125 MSPS DUAL DAC	AD9763AST	ANALOG DEVICES
1	U41	IC DAC 12 BIT SOIC-8	TLV5616ID	TEXAS INSTRUMENTS
1	U11	IC VOLTLTG SPRVOLTSR 5VOLT SOIC8	ADM708TAR	ANALOG DEVICES
1	U37	IC POWER SEQUENCING CONTROLLER	ISL6123	INTERSIL
1	U17	IC Q FLASH MEMORY W/ P0 SOFTWARE LOAD	MT28F320J3BS-11ET	MICRON
2	U33 U600	IC VOLT REG 1.25 MHZ LT1765 3A	LT1765ES8	LINEAR TECHNOLOGY
2	U4 U34	IC VOLT REG 5.0VOLT 0.8A LDO	LM1117IMPX-5.0	NATIONAL

Qty	Reference	Description	Part Number	Manufacturer
1	U26	IC VOLTAGE REG 1.8VOLT 0.8A	LM1117MPX-1.8	NATIONAL
1	U36	IC VOLT INVOLT -5VOLT SOT23-6	LTC1983ES6-5	LINEAR TECHNOLOGY
1	D9	IC 1.24V TO 5.30V ADJUSTABLE REGULATOR	LM285M	NATIONAL
1	U10	IC DRIVER RX DUAL SO16	ADM3202ARN	ANALOG DEVICES
1	U1	IC XCEIVER 10/100 BASET PQT80	AM79C874VI	AMD
1	U7	IC DDS 50MHZ TSS0P20	AD9834BRU	ANALOG DEVICES
3	U14 U18 U30	IC AMP R-R HISPD SOT-23-5	AD8051ART	ANALOG DEVICES
2	U24 U27	IC OPAMP DIFFERENTIAL AD8132	AD8132ARM	ANALOG DEVICES
1	U29	IC ZERO DELAY BUFFER SOIC8	CY2305SI-1H	CYPRESS
2	U2 U31	IC SINGLE SCHMITT TRIGGER INV	MC74VHC1G14DFT2	ON SEMI
5	U6 U8 U15 U19-20	IC OCTAL BUFFER/DRIVER W/ 3 STATE OUTPUTS	SN74LVC244APWR	TEXAS INSTRUMENTS
1	U32	IC ZERO DELAY BUFFER PROGRAMMABLE	CY2302SI	CYPRESS
1	U35	IC LOW V HIGH BANDWIDTH BUS SWITCH	SN74CB3Q3257PWR	TEXAS INSTRUMENTS
1	U5	IC TEMP SENSOR 12C 9-BIT SIGN	LM77CIMX-3	NATIONAL
2	U21-22	AUSTIN-LYNX PROGRAMMABLE POWER MODULE NON-ISOLATED	AXA005A0X	TYCO
1	U3	FUJITSU AIRMAN 802.16 CHIP	MB87M3400	FUJITSU
1	U28	CNVRTR DC/DC +/-48V TO +12V	PKB4713PINB	ERICSSON
121	R2 R31 R36-37 R39-44 R46-47 R119-120 R123-125 R128-129 R136-138 R140 R142-145 R153-157 R160-163 R169 R171 R173 R175-176 R194 R218 R222 R225-226 R232-233 R235 R239 R241 R243 R245 R247 R249 R255-256 R261 R265 R271-272 R291 R295 R297 R299-306 R316 R320 R323 R330 R333-336 R378-384 R399 R404-405 R419-441 R460 R500 R502 R523-524 R529 R540 R543	RES 0402 0R 5% 1/16W	RM04J000CT	CAL-CHIP
7	R198 R258 R450 R452 R454 R456 R533	RES 0402 100OHM 0.062W 1%	RM04F1000CT	CAL-CHIP
27	R55 R80 R89 R209 R212 R227-229 R236-237 R262-263 R286 R329 R397-398 R408-410 R451 R453 R455 R457 R466 R476 R601-602	RES 0402 1.0KOHM 0.062W 1%	RM04F1001CT	CAL-CHIP
39	R8 R18 R25-27 R32-34 R48 R65-66 R87 R118 R127 R131 R147 R223 R324 R331 R411-412 R415-418 R442-443 R458 R477-478 R495-499 R503-504 R544-545	RES 0402 10.0KOHM 0.062W 1%	RM04F1002CT	CAL-CHIP

Qty	Reference	Description	Part Number	Manufacturer
2	R215 R407	RES 0402 1MOHM 0.062W 1%	RM04F1004CT	CAL-CHIP
1	R200	RES 1/16W 1.1K 1% 0402	CR05-1101F-T	AVX
1	R21	RES 0402 1.21KOHM 0.062W 1%	RM04F1211CT	CAL-CHIP
1	R22	RES 0402 12.1KOHM 0.062W 1%	RM04F1212CT	CAL-CHIP
1	R149	RES 0402 13K7 0.062W 1%	RM04F1372CT	CAL-CHIP
43	R3 R9-14 R16 R84-86 R90-98 R102-113 R116 R224 R254 R264 R274-277 R402-403 R481	RES 0402 150 OHM 0.062W 1%	RM04F1500CT	CAL-CHIP
3	R158 R206 R214	RES 0402 1.5KOHM 0.062W 1%	RM04F1501CT	CAL-CHIP
1	R394	RES 0402 1.82KOHM 0.062W 1%	RM04F1821CT	CAL-CHIP
3	R67-68 R71	RES 0402 200OHM 0.062W 1%	RM04F2000CT	CAL-CHIP
1	R207	RES 0402 20K0 OHM 1% .062W	RM04F2002CT	CAL-CHIP
1	R24	RES 0402 2.43KOHM 0.062W 1%	RM04F2431CT	CAL-CHIP
3	R201 R230 R459	RES 0402 2.74KOHM 0.062W 1%	RM04F2741CT	CAL-CHIP
4	R314-315 R479-480	RES 0402 332OHM 0.062W 1%	RM04F3320CT	CAL-CHIP
1	R337	RES 0402 3.32KOHM 0.062W 1%	RM04F3321CT	CAL-CHIP
1	R328	RES 0402 36.5KOHM 0.062W 1%	RM04F3652CT	CAL-CHIP
2	R396 R600	RES 0402 3.92KOHM 0.062W 1%	RM04F3921CT	CAL-CHIP
2	R325 R401	RES 0402 432OHM 0.062W 1%	RM04F4320CT	CAL-CHIP
1	R7	RES 0402 4.75KOHM 0.062W 1%	RM04F4751CT	CAL-CHIP
4	R117 R406 R534-535	RES 0402 499 OHM 0.062W 1%	RM04F4990CT	CAL-CHIP
1	R391	RES 0402 4.99KOHM 0.062W 1%	RM04F4991CT	CAL-CHIP
1	R208	RES 0402 49.9KOHM 0.062W 1%	RM04F4992CT	CAL-CHIP
1	R148	RES 0402 5K11 0.0625W 1%	RM04F5111CT	CAL-CHIP
2	R393 R395	RES 0402 5.62KOHM 0.062W 1%	RM04F5621CT	CAL-CHIP
1	R390	RES 0402 681OHM 0.062W 1%	RM04F6810CT	CAL-CHIP
1	R338	RES 0402 7.50KOHM 0.062W 1%	RM04F7501CT	CAL-CHIP
1	R332	RES 0402 8.25KOHM 0.062W 1%	RM04F8251CT	CAL-CHIP
1	R392	RES 0402 931OHM 0.062W 1%	RM04F9310CT	CAL-CHIP
1	R23	RESISTOR 9.53K 1% 1/16W 0402	ERJ-2RKF9531X	PANASONIC
4	R83 R151 R193 R213	RES 0402 10.0OHM 0.062W 1%	RM04F10R0CT	CAL-CHIP
116	R5-6 R19 R29-30 R51 R53-54 R56-62 R69-70 R72-79 R81-82 R100 R114-115 R130 R133-134 R152 R164-168 R177-192 R195-197 R199 R202-205 R219-221 R251-252 R268-270 R273 R280 R282-285 R339-366 R368-377 R538	RES 0402 33.2OHM 0.062W 1%	RM04F33R2CT	CAL-CHIP
14	R4 R35 R38 R45 R49 R99 R139 R141 R266 R278 R386-389	RES 0402 49.9OHM 0.062W 1%	RM04F49R9CT	CAL-CHIP
6	R1 R50 R210-211 R216-217	RES 0402 75.0OHM 0.062W 1%	RM04F75R0CT	CAL-CHIP
1	R327	RES 0603 4K75 1%	ERJ3EKF4751	PANASONIC
3	R52 R63-64	RES ARRAY ISOLATED 33RX12 5%	PRN1102433R0J	CMD
2	R28 R267	RES ARRAY BUSSED 10KX15 5%	PRN111161002J	CMD
2	D5 D601	DIODE STKY RECT 2A 60V	MBRS260T3	ON SEMI

Qty	Reference	Description	Part Number	Manufacturer
1	D11	DIODE ULTRAFAST RECT 200V/3A	MURS320T3	ON SEMI
1	D10	DIODE ZENER 6.2V 200MW SOD323	MM3Z6V2T1	ON SEMI
1	U9	SLVU2.8-8 EPD DIODE ARRAY	SLVU2.8-8.TB(E)	PROTEK
2	D4 D600	DIODE SW HISPD 100V 0.2A S0T23	MMBD914LT1	MOTOROLA
4	Q6-7 Q10 Q12	TRANS NPN 3904 1A SOT23	MMBT3904	FAIRCHILD
3	Q1 Q3 Q11	MOSFET PWR N-CH 100V 6.9A SOIC-8	IRF7420	INT RECTIFIER
5	Q2 Q4-5 Q8-9	MOSFET PWR N-CH 20V 7.0A SOIC-8	IRF7401	INT RECTIFIER
1	S3	SW NO PB RA PCB MOUNT	KT11P2SM	C&K
2	S1-2	SWITCH HALF PITCH DIP	97C08S	GRAYHILL
1	T1	XFORMER SINGLE 10/100BTX SOIC	TG110-S050N2	HALO

APPENDIX 5: REFERENCE BOARD SCHEMATICS

Schematics of the SoC Reference Board and the RF Boards are included on the SoC Reference Kit CD-Rom in PDF format.