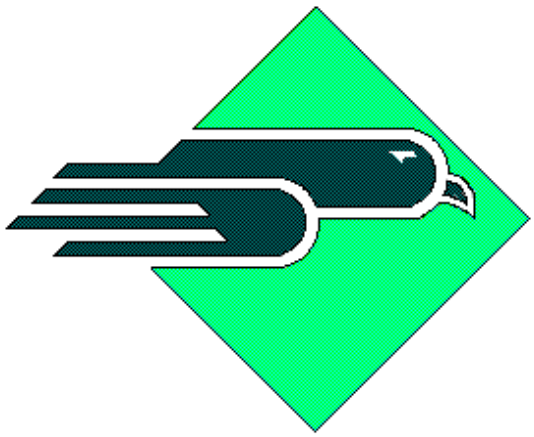

WESTERN AVIONICS

SHUTTLE BUS PCI
INTELLIGENT INTERFACE BOARD

P/N 1U10953G01 Rev A

User Manual
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13/14 Shannon Free Zone
Co. Clare
Ireland

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1. ABBREVIATIONS

1.1. General

SBIIB	Shuttle-Bus Intelligent Interface Board
LDB_BCT	LDB Mode Bus Controller Terminal
LDB_MRT	LDB Mode Multi-Remote Terminal
GDB_BCT	GDB Mode Bus Controller Terminal
GDB_MRT	GDB Mode Multi-Remote Terminal
MDM_MRT	MDM Mode Multi-Remote Terminal
PRM_MDE	Primitive Mode
BUS_MON	Bus Monitor mode
CAL_MDE	SBIIB calibration mode
IRQ	Interrupt Request
CAR	Current Address Register
TOR	Trigger Occurrence Register
TSP	Trigger Setup Pointer
MDB	Message Descriptor Block

1.2. LDB Shuttle-Bus Command Codes

Mnemonic	Value	Description	Direction
SRQ	**0010**	Status Request	Command
IND	**0011**	Interrogate with no GPC data	Command
GAH	**0101**	Go-Ahead	Command
HCD	**1001**	Here comes GPC data	Command
STA	**1010**	Status	Command
IWD	**1101**	Interrogate with GPC data available	Command
NNB	**0011**	No need for the bus	Response
DTT	**0110**	GDB has data to transmit to GPC	Response
GTX	**1100**	Good transmission	Response
TXD	**1011**	GDB enable for transmission of GPC data	Response

2. GENERAL INFORMATION

2.1. Introduction

The Shuttle-Bus Intelligent Interface Board (SBIIB) is a standard PCI board designed to interface to the Launch Data Bus (LDB), Ground Data Bus (GDB), and Cargo Integration Test Equipment Uplink (CUL) data bus.

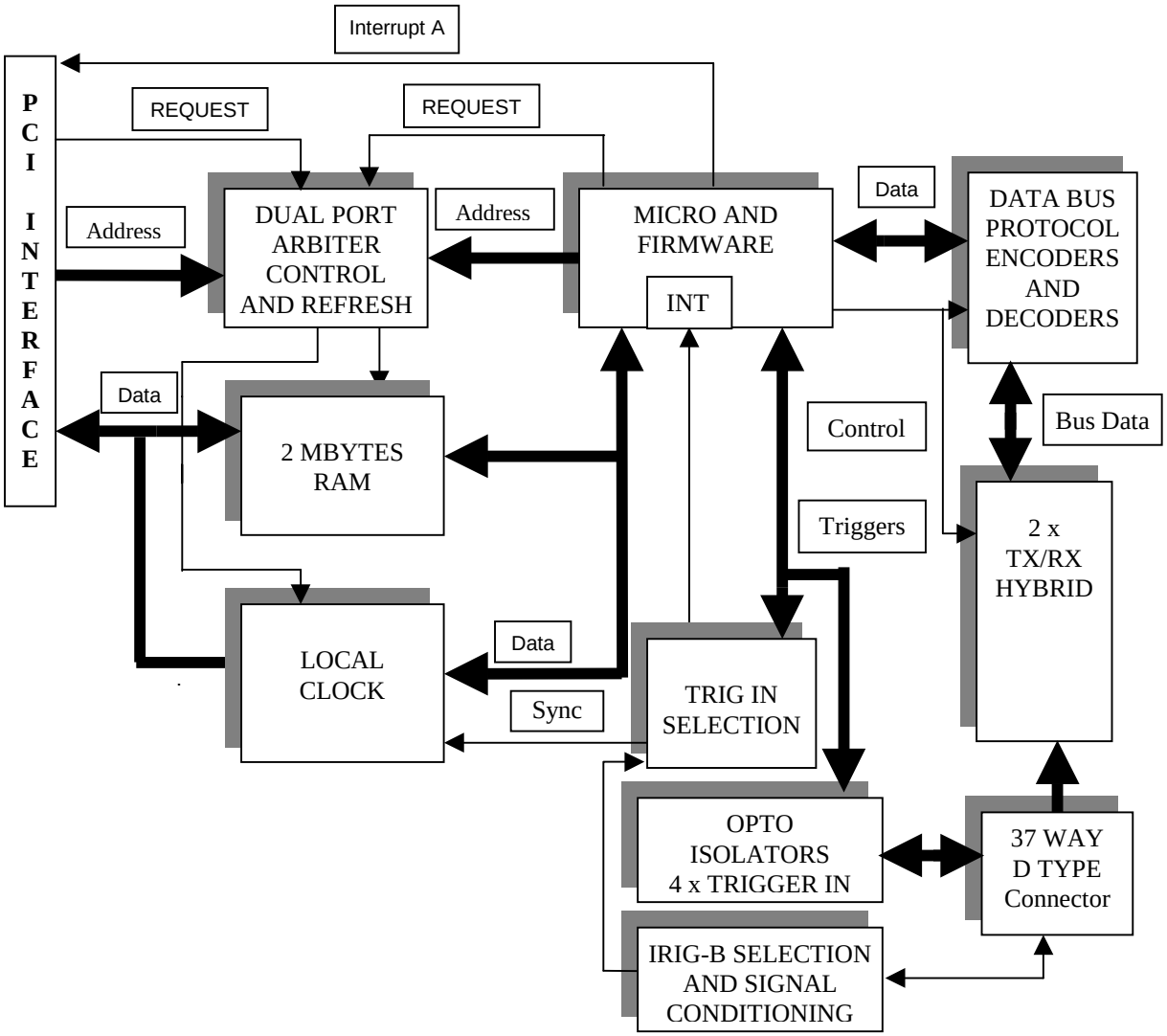
The SBIIB board is designed to operate in the following modes:

1. LDB_BCT Launch Data Bus Controller (Simplex or Half-Duplex)
2. LDB_MRT Launch Data Bus Multi-Remote terminal (Simplex or Half-Duplex)
3. BUS_MON Bus Monitor mode (24-bt or 40-bit)
4. GDB_BCT Ground Data Bus Controller (24-bit or 40-bit)
5. GDB_MRT Ground Data Bus Multi-Remote terminal (24-bit or 40-bit)
6. MDM_MRT Multiplex-De-multiplex Multi-Remote Terminal
7. PRM_MDE Primitive Mode
8. CAL_MDE SBIIB calibration mode

These modes are available providing a comprehensive test and simulation facility for communication with the Space Shuttle Data Buses.

2.2. Architecture

A functional block diagram of the SBIIB is shown below.



2.2.1. PCI interface

The PCI interface on the SBIIB matches the PCI Local Bus Specification Revision 2.2 for 32 bit specification. The SBIIB is presented as a 2Mbyte linear memory map to the PCI bus interface with a write only 16-bit Control Register and read only 32-bit Local Clock mapped at the start of the 2Mbyte block. The remainder of the 2Mbyte block is shared memory used for reading and writing set-ups and test results. The PCI interface includes an INT A interrupt.

Required Signals:

AD[31..0]	Address and Data
C/BE[3..0]	
PAR	
FRAME#	Interface Control
TRDY#	
IRDY#	
STOP#	
DEVSEL#	
IDSEL	
PERR#	
SERR#	Error Reporting
CLK	System
RST#	
INTA#	Interrupts

Power Requirements:

+5V, +12V, -12V and GND

Interrupts:

- Single hardware interrupt INTA.
- Interrupt is released on write to control register.

2.2.2. 2Mbyte of shared memory

2Mbyte of fast RAM is used for the storing of set-ups and the recording of results. This memory is dual-ported to enable simultaneous protected access from the PCIbus and the on-board DSP.

An intelligent multi-port arbiter is used to controls the flow of data to and from the memory to enable maximum efficiency at all times.

2.2.3. Dual Port Arbiter Control

An intelligent multi-port arbiter is used to controls the flow of data to and from the memory and LOCAL CLOCK to enable maximum efficiency at all times.

2.2.4. The Local Clock

The SBIIB has an on-board clock for time-tagging events. This clock has a resolution of 0.5uS and can be programmed to either run freely or is synchronised with a demodulated IRIG-B time code data stream and its 1KHz carrier waveform. This clock is memory mapped as one 32-bit word starting at the base address of the card. The clock is a read only device and is read as follows:

1. Execute a write to the 16-bit control register at the base address of the card. This will latch the current clock value into the output buffer and initialise the device output stage for reading.
2. Wait a minimum time of 0.5uS to ensure that the latching process is complete.
3. Execute 2 consecutive reads of the 32-bit location at the base address of the card.

The first 48 bits will be the current clock time as decoded from the IRIG-B time code. The last 16 bits will be a value 0-1999 defining the fraction of a millisecond with a resolution of 0.5uS per tick.

1st read - upper word:	N0 CC DDDDDDD HHHHH	C = Days x 100, D = Days, H = Hours
1st read - lower word:	0000 MMMMMM SSSSSS	M = Minutes, S = Seconds
2nd read - upper word:	000000 MMMMMMMMMM	M = Milliseconds
2nd read - lower word:	00000 UUUUUUUUUU	U = 0.5uS ticks

If the MSB of the 1st 16-bit word (N) is set, the card is not locked with the incoming IRIG-B signal.

2.2.5. Micro and Firmware

The protocol management consists of a 40MHz DSP processor with extensive support logic. The PMU interfaces with the Shuttle-Bus interface and the 2Mbyte of memory. The DSP is totally controlled by the on-board firmware and hence can be modified to suit any future protocol changes or special requirements.

2.2.6. Data Bus Protocol Encoders and Decoders

The data bus protocol encoders and decoders consists of two transceiver hybrids and a high density EPLD for decoding/encoding and interfacing to the DSP.

2.2.7. Trigger IN / Trigger OUT

There are 4 trigger IN and 4 trigger OUT signals that can be fed to the card via the 37-way D connector on the front panel. These signals are opto-isolated.

2.2.8. IRIG-B Selection and Signal Conditioning

As well as the 4 trigger IN/OUT signals there are a number of IRIG-B related signal inputs available. Modulated IRIG-B time code can be input at the 37-way connector on the front panel. This signal is then be fed to an IRIG-B demodulator that produces a 1KHz waveform and a TTL demodulated IRIG-B signal for synchronising the local clock. Alternatively, a demodulated TTL IRIG-B waveform and 1KHz synchronised waveform can be fed directly to the local clock from the 37-way connector for synchronisation.

NOTE: All the special IRIG-B signals are **not** opto-isolated so care **must** be taken when using these inputs.

2.2.9. Environmental and Electrical Requirements

Power Requirements:

+5V @ 2.10 Amps (Max)
+12V @ 500 mAmps (Max)
-12V @ 250 mAmps (Max)

Temperature/Humidity:

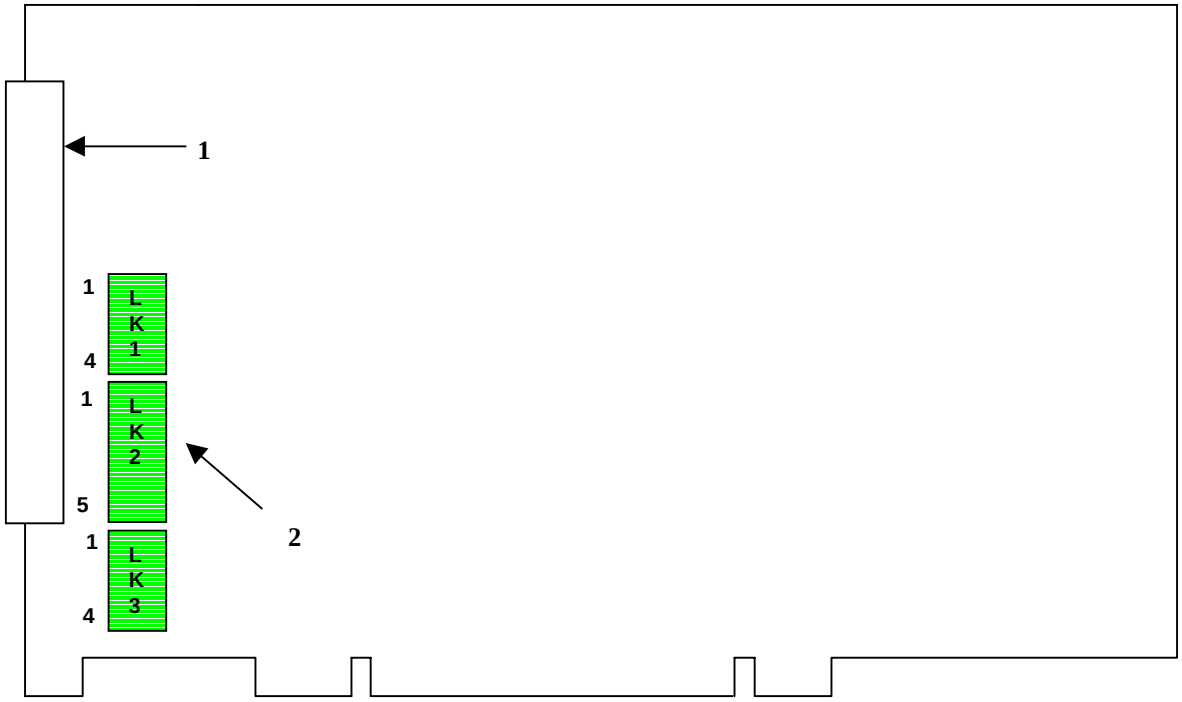
Operating Temp. range:	0 to 50 degrees C (32 to 122 F) at 0% to 95% RH, non-condensing.
Storage Temp. range:	-20 to 65 degrees C (-4 to 150 F) at 0% to 95% RH, non-condensing

MTBF: (Per MIL-HDBK-217E)

195,660 Hours (Ground Benign, 20 degrees Centigrade)
160,953 Hours (Ground Benign, 30 degrees Centigrade)
119,497 Hours (Ground Benign, 40 degrees Centigrade)

2.3. Configuration Jumpers and Front Panel Connector Location Diagram

1. 37-Way D connector for trigger and bus.
2. LK1-LK3 Configuration jumpers.



2.4. Front Panel Connector J1.

The 37-way D-type connector J1 is used for the supply of trigger-in, trigger-out and SBIIB bus signals.

PIN	SIGNAL	PIN	SIGNAL
1	GROUND		
2	TRIG-IN 3 ANODE	20	TRIG-IN 3 CATHODE
3	TRIG-IN 2 ANODE	21	TRIG-IN 2 CATHODE
4	TRIG-IN 1 ANODE	22	TRIG-IN 1 CATHODE
5	TRIG-IN 0 ANODE	23	TRIG-IN 0 CATHODE
6	1KHz CARRIER INPUT	24	DEMODULATED INPUT
7	RESERVED	25	IRIG-B SIGNAL INPUT
8	TRIG-OUT 3	26	TRIG-OUT 2/3 GND
9	TRIG-OUT 2	27	TRIG-OUT 2/3 VCC
10	TRIG-OUT 1	28	TRIG-OUT 0/1 GND
11	TRIG-OUT 0	29	TRIG-OUT 0/1 VCC
12	GROUND	30	GROUND
13	BUS 4 DATA POSATIVE	31	BUS 4 DATA NEGATIVE
14	GROUND	32	GROUND
15	BUS 3 DATA POSATIVE	33	BUS 3 DATA NEGATIVE
16	GROUND	34	GROUND
17	BUS 2 DATA POSATIVE	35	BUS 2 DATA NEGATIVE
18	GROUND	36	GROUND
19	BUS 1 DATA POSATIVE	37	BUS 1 DATA NEGATIVE

Note: Reserved pin (7) **must not** be used.

2.5. Jumper Selection

The SBIIB has a number of jumper headers to allow selection of a number of options.

2.5.1. LK1 - Trigger-Out Power Source Selection Header

This header is used to connect/disconnect the cards internal +5V and Ground supplies to the Trigger Out. Please see use of external Power and Ground for these Trigger-Out signals under paragraph 2.4. (J1 Front Panel Connector).

LINK	SIGNAL
L1	+5V for TRIGGER-OUT 0 and 1
L2	GND for TRIGGER-OUT 0 and 1
L3	+5V for TRIGGER-OUT 2 and 3
L4	GND for TRIGGER-OUT 2 and 3

2.5.2. LK2 - Local Clock Synchronise Signal Selection Header

This header is used to select the 75-Ohm load terminator for the IRIG-B input, and select the TTL carrier and demodulated IRIG-B signal for the on-board clock.

LINKS	SIGNAL FOR SYNCRONISATION
L1	SELECT 75 OHM LOAD TERMINATOR FOR IRIG-B INPUT
L2	SELECT ON-BOARD DEMODULATED IRIG-B FOR CLOCK
L3	SELECT 37-WAY DEMODULATED IRIG-B FOR CLOCK
L4	SELECT ON-BOARD RECOVERED CARRIER FOR SYNC
L5	SELECT 37-WAY CARRIER FOR SYNC

2.5.3. LK3 - Trigger-In Interrupt Selection Header

Any one of the trigger-in signals, T0-T3, can be routed to the on-board DSP special interrupt input via this header. This special interrupt feature is for future development and is at present undefined.

LINK	TRIGGER
L1	TRIGGER-IN 0
L2	TRIGGER-IN 1
L3	TRIGGER-IN 2
L4	TRIGGER-IN 3

3. BASE REGISTERS

The base registers are the only registers that are fixed and reside at the start of the Shuttle-Bus card 2Mbyte of memory. The reserved locations are for configuration data and **must not** be used.

1 = LDB_BCT **2** = LDB_MRT **3** = BUS_MON **4** = GSE_BCT
5 = GSE_MRT **6** = MDM_MRT **7** = PRM_MDE

ADDR	NAME	USED BY						
		1	2	3	4	5	6	7
0x00	Control Register (Write)/Clock HI (read)	*	*	*	*	*	*	*
0x02	Clock LO (Read Only)	*	*	*	*	*	*	*
0x04	Command Register (CR)	*	*	*	*	*	*	*
0x06	Status Register (SR)	*	*	*	*	*	*	*
0x08	Program Pointer (BRP)	*			*			
0x0A	RT Simulation Table Pointer		*			*	*	
0x0C	HI Priority Queue Pointer	*	*		*		*	*
0x0E	LO Priority Queue Pointer	*	*		*		*	*
0x10	BIN Queue Pointer	*	*					
0x12	BIN Trigger-out Event Register	*	*	*				
0x14	Reserved							
0x16	Reserved							
0x18	IRQ Selection Register	*	*	*	*	*	*	*
0x1A	Gap Time Register	*	*	*	*	*	*	*
0x1C	RT Response Time Register		*				*	
0x1E	RT Response Time-out Register	*	*		*	*	*	
0x20	Bus Select Register	*	*	*			*	*
0x22	Bus Monitor Trigger Set-up Pointer			*				
0x24	Bus Monitor Current Address HI Register			*				
0x26	Bus Monitor Current Address LO Register			*				
0x28	Bus Monitor Trigger Occurrence HI Register			*				
0x2A	Bus Monitor Trigger Occurrence LO Register			*				
0x2C	Load Clock HGH Register	*	*	*	*	*	*	*
0x2E	Load Clock LOW Register	*	*	*	*	*	*	*
0x30	Inter-word Timeout Register	*	*				*	*
0x32	Watchdog Timeout Register	*	*		*	*	*	
0x34	Watchdog Change Register	*	*		*	*	*	
0x36	Polling Timeout Register		*					
0x38	TX Amplitude Register	*	*	*	*	*	*	*
0x3A	Uplink Queue Pointer				*	*		*
0x3C	Downlink Queue Pointer				*			*
0x3E	TX PRI Register	*	*	*	*	*	*	*
0x40	TX SEC Register	*	*	*	*	*	*	*
0x42	RX PRI Register	*	*	*	*	*	*	*
0x44	RX SEC Register	*	*	*	*	*	*	*
0x46	RT Address Register		*					
0x48	Wrap-round HI Register	*						
0x4A	Wrap-round LO Register	*						
0x4C	RESERVED							
0x3F4	RESERVED							
0x3F6	Serial number HI	*	*	*	*	*	*	*
0x3F8	Serial number LO	*	*	*	*	*	*	*
0x3FA	Firmware checksum HI	*	*	*	*	*	*	*
0x3FC	Firmware checksum LO	*	*	*	*	*	*	*
0x3FE	Firmware REV level	*	*	*	*	*	*	*

3.1. Control Register

Write only @ Base+0x00

This register is used for controlling the reset, interrupt and initialisation functions of the card.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	FR	0	IQ1	IQ0	0	0	0	1	C0

C0: When set to 0 will generate a Command Request interrupt to the on-board processor.
FR: When set to 0 will reset the on-board firmware.
IQ1, IQ0: Used to clear/set an INTA interrupt as follows:

IQ1	IQ0	
0	0	Normal access
0	1	Not used
1	0	Force INTA interrupt
1	1	Clear INTA interrupt

With IQ1 set, the level if the INTA interrupt line will be forced to the level defined by IQ0. For normal operation the only values that should be used are 00 and 11. However, the user can force the interrupt line active using 10 for testing interrupt service routines during development.

Example: The value 0x0102 will generate a **Command Req.** whilst keeping FR set.

3.2. Clock HI/LO

Read only @ Base+0x00 and Base+0x02

These two registers are for reading the current value of the on-board clock. A read of the Clock HI will request the current value of the clock to be latched into the output buffer. The user must wait a minimum time of >0.5uS before beginning to read the clock value to ensure latching has completed. Four consecutive reads of the Clock LO location will return the clock value as: -

1st word:	N0 CC DDDDDDD HHHHH	C = Days x 100, D = Days, H = Hours
2nd word:	0000 MMMMMM SSSSSS	M = Minutes, S = Seconds
3rd word:	000000 MMMMMMMMMM	M = Milliseconds
4th word:	00000 UUUUUUUUUU	U = 0.5uS ticks

If the MSB of the 1st word (N) is set, the card is not locked with the incoming IRIG-B signal.

To **Load** the clock with a new value:

1. Write the new value in the base registers Load Clock HGH, LOW.

   1st word: LL CC DDDDDDDD HHHH
   2nd word: HH MMMMMMM SSSSSSS

LL	Leap year	(0-3)
CC	Days x 100	(0-3)
DDDDDDDD	Days	(0-66 in BCD)
HHHHHH	Hours	(0-23 in BCD)
MMMMMMM	Minutes	(0-59 in BCD)
SSSSSSS	Seconds	(0-59 in BCD)

   To allow decoding of IRIG-B the clock always adds 1 second to the programmed value. Therefore, the above time must be set to the desired time minus 1 second. Leap year value should be 00 = Leap year, 01 = 1st year after leap year etc.

2. Write the Load Clock command code into the command register.
3. Now execute generate a command request (write 0x0302 in control register).

If the 1st word is set to LL11111111111111, the free running clock will not be loaded. The LL bits will be used to define the leap year and the clock will be forced into external sync mode.

If the 1st word is **not** set to LL11111111111111, the free running clock will be loaded and the clock will be forced into free running mode.

3.3. Command Register

Read/Write @ Base+0x04

This register is used to define the particular command to be carried out by the on-board processor. The code should be placed in this register prior to generating a command request in the control register. The following commands are available:

CODE	COMMAND
0x0000	Illegal
0x0001	Go to LDB_BCT mode
0x0002	Go to LDB_MRT mode
0x0003	Go to BUS_MON mode
0x0004	Go to GDB_BCT mode
0x0005	Go to GDB_MRT mode
0x0006	Go to MDM_MRT mode
0x0007	Go to PRM_MDE mode
0x0008	Reserved
0x0009	Reserved
0x000A	Start card running
0x000B	Stop card
0x000C	Load Clock
0x000D	Execute Self-test
0x000E	Execute Full Wrap-round test
0x000F	Go to CAL_MDE mode (only when in LDB_BCT mode)

Note:
The selftest and wrap-round test should only be commanded when the card is in the 'selftest complete' state or when the card is in the LDB_BCT idle state.

3.4. Status Register

Read/Write @ Base+0x06

The on-board firmware will dynamically update this register with the cards current status.
The possible states the card can be in are as follows:

CODE	MEANING
0x0000	Not allowed
0x0010	LDB_BCT Idle
0x0020	LDB_MRT Idle
0x0030	BUS_MON Idle
0x0040	GDB_BCT Idle
0x0050	GDB_MRT idle
0x0060	MDM_MRT idle
0x0070	PRM_MDE idle
0x0011	LDB_BCT running
0x0021	LDB_MRT running
0x0031	BUS_MON running
0x0041	GDB_BCT running (active)
0x9041	GDB_BCT running (passive)
0x0051	GDB_MRT running
0x0061	MDM_MRT running
0x0071	PRM_MDE running
0x9011	LDB_BCT software paused
0xA011	LDB_BCT hardware paused
0xA041	GDB_BCT hardware paused
0x000F	Executing self-test
0x8??F	Self-test complete
0x000A	Executing Full wrap-round test
0x80?A	Wrap-round test complete

3.4.1. Selftest

The status register will contain the following information after completion of self-test:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
1	0	0	0	0	SB	LC	M5	M4	M3	M2	M1	1	1	1	1

SB: Set to 1 if Shuttle-Bus interface failed.
LC: Set to 1 if local clock test failed.
M5: Set if memory test 5 failed.
M4: Set if memory test 4 failed.
M3: Set if memory test 3 failed.
M2: Set if memory test 2 failed.
M1: Set if memory test 1 failed.

Several bits can be set simultaneously. If no self-test errors are detected the SYSFAIL LED will go out and the code in the status register will be 0x800F.

3.4.2. Full Wrap-Round Test

The wrap-round test assumes that there are two external cables connecting BUS 1 to BUS 2 and BUS 3 to BUS 4. The pattern and SYNC type used for the Wrap-round test is defined in the base registers. The status register will contain the following information after completion of a full wrap-round test:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
1	0	0	0	R8	R7	R6	R5	R4	R3	R2	R1	1	0	1	0

R1: Set to 1 if TX from BUS 1 to BUS 2 failed.
R2: Set to 1 if TX from BUS 3 to BUS 4 failed.
R3: Set to 1 if TX from BUS 2 to BUS 1 failed.
R4: Set to 1 if TX from BUS 4 to BUS 3 failed.
R5: Set to 1 if TX from BUS 1 to BUS 1 failed (on-board wrap-round test).
R6: Set to 1 if TX from BUS 2 to BUS 2 failed (on-board wrap-round test).
R7: Set to 1 if TX from BUS 3 to BUS 3 failed (on-board wrap-round test).
R8: Set to 1 if TX from BUS 4 to BUS 4 failed (on-board wrap-round test).

If no errors are detected the status register will be 0x800A.
Bits R5-R8 are the result of an on-board wrap test up to the output transformers and should pass with or without external cables.

3.5. Program Pointer

Read/Write @ Base+0x08

This register is only used when the card is in LDB_BCT or GDB_BCT mode.

LDB_BCT mode:
The user shall set the contents of this register to point to the absolute address in the bottom 64Kbytes of card memory where the start of the bus controller program resides.

GDB_BCT mode:
This shall contain the 64Kbyte block number in memory where the polling table starts. This value must be > 0 and is continually read in GDB_BCT mode to allow dynamic table switching. For further details, see the GDB_BCT mode description.

3.6. RT Simulation Table Pointer

Read/Write @ Base+0x0A

This register is only used when the card is in LDB_MRT, GDB_MRT or MDM_MRT mode. The user shall set the contents of this register to point to the absolute address in the bottom 64Kbytes of card memory where the start of the RT Simulation Table resides.

3.7. HI/LO Priority Queue Pointers

Read/Write @ Base+0x0C and Base+0x0E

LDB, MDM and PRM modes:
Two report queues are available for the onboard processor to push information regarding events detected on the Shuttle-bus.

GDB mode:
These queues are for COMMAND insertion. For further details, see the GDB_BCT mode description.

These queues are 512 bytes long. The address of these queues can reside anywhere in the bottom 64Kbytes of memory providing they are set on an even 512 byte boundary. These registers must be initialised by the user to define where the queues are to be located.

3.8. BIN Queue Pointer

Read/Write @ Base+0x10

In LDB_BCT, LDB_MRT and MDM_MRT modes, this queue shall be used to save any invalid or unsolicited command and data words. Each entry in the queue will consist of 8 words as follows:

1. TTAG HIGH (Clock value high)
2. TTAG MID (Clock value mid)
3. TTAG LOW (Clock value low)
4. TTAG TICKS (Clock ticks value)

5. ERRORS and DATA HGH

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
B1	B0	0	Sy	Py	Mn	Lg	Sh	D	D	D	D	D	D	D	D

Sy = Sync type. 1 = Command Sync
Py = 1 = Parity error
Mn = 1 = Manchester error
Lg = 1 = Long word (too many bits)
Sh = 1 = Short word (too few bits)
D = Most significant 8 bits of word

B1	B0	LDB_BCT	LDB_MRT
0	0	Unsolicited data on TX PRI bus	Not Allowed
0	1	Unsolicited data on TX SEC bus	Not Allowed
1	0	Unsolicited data on RX PRI bus	Invalid/Unsolicited data on PRI bus
1	1	Unsolicited data on RX SEC bus	Invalid/Unsolicited data on SEC bus

6. DATA LOW

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

D = Least significant 16 bits of word

7. Other EVENTS

The contents of this location will describe any activity on the alternate bus when the push to the BIN queue was carried out as follows:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
GC	GD	BC	BD	Py	Mn	Lg	Sh	1	1	1	1	1	1	1	1

GC: Good command to enabled RT received on other bus
GD: Good data to enabled RT received on other bus
BC: Bad command received on other bus
BD: Bad data received on other bus
Py: Parity error detected on other bus
Mn: Manchester error detected on other bus
Lg: Long word error detected on other bus
Sh: Short word error detected on other bus

8. 0xFFFF

This queue is 512 bytes long. The address of this queue can reside anywhere in the bottom 64Kbytes of memory providing it is set on an even 512 byte boundary. This register must be initialised by the user to define where the queues are to be located.

3.9. BIN Trigger-out Event Register

Read/Write @ Base+0x12

When in LDB mode this register shall define the conditions required to cause the transistor output of the trigger-out 2 opto-isolator to be turned on.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X	0	0	0	0	0	0	0	Tg	Rp	Cs	Ds	Py	Mn	Lg	Sh

X: = 1 = Disable Error Bits Py, Mn, Lg, Sh from trigger condition
Tg = 1 = Generate trigger-out when monitor trigger condition is met (BUS_MON only)
Rp = 1 = Generate trigger-out when MRT polling timeout occurs (LDB_MRT only)
Cs = 1 = Generate trigger-out when a Command Sync is detected
Ds = 1 = Generate trigger-out when a Data Sync is detected
Py = 1 = Generate trigger-out when a Parity error is detected
Mn = 1 = Generate trigger-out when a Manchester error is detected
Lg = 1 = Generate trigger-out when a Long word is detected (too many bits)
Sh = 1 = Generate trigger-out when a Short word is detected (too few bits)

Note:

- If the MSB of this register is set to 1, then the error bits will take no part in the trigger condition.
- If more than one of the Py, Mn, Lg, Sh bits are set then the trigger will occur if any of these errors occur.
- At least one of Cs and Ds **must** be set to 1. Setting both will result on a trigger on any sync.
- The trigger-out will occur on trigger-out 2.
- In LDB_BCT mode a trigger will only occur if the word was unsolicited and is pushed to the BIN queue.
- In LDB_MRT mode a trigger will only occur if the word was unsolicited and is pushed to the BIN queue or if a polling timeout occurs.
- In BUS_MON the Tg bit and the Cs, Ds, Py, Mn, Lg, Sh bits are applicable. A trigger-out can be generated on the occurrence of an error word or when the monitor trigger condition is met.
- In all three modes, the trigger-out condition is a logical OR of all these bits.
- When in LDB_BCT or LDB_MRT mode, if an invalid word is detected during data reception, the data word will be stored in the data buffer and a positive 1uS pulse will be output on trigger-out 1 and trigger-out 2 simultaneously.
- Once the trigger-out has occurred, the trigger-out will give a positive output pulse of 1uS duration.

3.10. IRQ Selection Register

Read/Write @ Base+0x18

This register is used to select the particular physical interrupt(s) required for a particular event as follows:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	0	0	0	B	0	H	0	L

LDB and MDM modes:
H: Set to generate an INTA interrupt when a push to the HI priority reports queue is made.
L: Set to generate an INTA interrupt when a push to the LO priority report queue is made.
B: Set to generate an INTA interrupt when a push to the BIN report queue is made.

GDB_BCT and PRM_MDE modes:
H: Set to generate an INTA interrupt when an UPLINK IRQ is requested.
L: Set to generate an INTA interrupt when a DOWNLINK IRQ is requested.

GDB_MRT mode:
H: Set to generate an INTA interrupt when the received command response is enabled.
L: Set to generate an INTA interrupt when the received command response is disabled.

3.11. Gap Time Register

Read/Write @ Base+0x1A

LDB, PRM mode:
In LDB and PRM modes this register is used to define the required gap time between consecutive TX data words.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
M	0	0	0	0	0	0	0	0	0	0	T	T	T	T	T

T: Five-bit number defining the required inter-word gap. LSB = 0.5uS
M: In LDB mode this bit shall be set to 0.
In PRM_MDE this bit shall be set to define if the card is to act in 24 or 40-bit mode.
1 = 40-bit mode.

GSE_BCT and BUS_MON modes:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
M	0	0	0	0	0	0	T	T	T	T	T	T	T	T	T

M: This bit shall be set to define if the card is to act in 24 or 40-bit mode. 1 = 40-bit mode.
T: GSE_BCT mode - Timeslot duration in uS. The minimum allowable value for this is 90uS.
BUS_MON mode - The 'T' bits are not applicable.

3.12. RT Response Time Register

Read/Write @ Base+0x1C

This register shall define the response time in microseconds for the simulated LDB/MDM RTs.

3.13. RT Response Time-out Register

Read/Write @ Base+0x1E

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
ED	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T

T: In LDB_BCT and LDB_MRT modes this value shall define the time, in microseconds, the card is to wait before deciding that a RT has failed to respond to a command from the Bus Controller.
In GSE_BCT mode this value shall define the number of time-slots the BC shall wait before deciding that a RT has failed to respond to a command. This value shall be in the range 1-31.

ED: In GSE_BCT mode, this bit enables/disables the timeout feature. 1 = disable.
In LDB_BCT and LDB_MRT modes, this must be cleared.

3.14. Bus Select Register

Read/Write @ Base+0x20

In LDB_BCT mode, this register shall define which bus the card shall test for alternative BC activity. If other BC activity is detected on the bus/buses defined by this register, the BC shall halt.
During BC dead periods, such as 'software pause', the BC polls the 4 buses for unsolicited activity. If activity is detected, the received data is stored on the BIN queue, regardless of the bus it was detected on, and the appropriate interrupt is generated. The BC will then determine if the bus was a BC RX bus and if the data had a Command sync type. If both are true, the BC will test the bits in this register to determine if the user wishes the card to automatically halt on this event.

In LDB_MRT, PR_MDE this register shall define which bus the card shall listen to for bus messages.

In BUS_MON mode, this register shall define which buses are to be listened to.

Global disable bits for checksum and TX error injection are also in this register.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	C	E	0	0	0	0	BUS 4	BUS 3	BUS 2	BUS 1

C = Checksum error disable. If set, the checksum algorithm in LDB_MRT mode will be disabled.
E = Global TX error disable. If set, all TX errors defined in the card will be disabled.

BUS 2	**BUS 1**	**LDB_BCT**	**LDB_MRT**
0	0	Halt on none	Not allowed
0	1	Halt on secondary command	Listen on secondary bus
1	0	Halt on primary command	Listen on primary bus
1	1	Halt on any	Listen on both buses

In BUS_MON mode, if any of the BUS 4, BUS 3, BUS 2, BUS 1 bits are set then the monitor will listen to the corresponding front panel connections for bus activity.

Note: In LDB_BCT and LDB_MRT mode, BUS 3 and BUS 4 **must** be set to 0.

3.15. Bus Monitor Trigger Setup Pointer (TSP)

Read/Write @ Base+0x22

This register is only used when the card is in monitor mode. This register shall be set by the user to define the absolute address within the bottom 64Kbytes where the Bus Monitor trigger and stack definition registers reside. For further details, see the BUS_MON mode description.

3.16. Bus Monitor Current Address HI/LO Register (CAR)

Read/Write @ Base+0x24 and Base+0x26

This register is only used when the card is in monitor mode. These registers form a 32-bit address pointer defining where the bus monitor is currently operating within the bus monitor stack. For further details, see the BUS_MON mode description.

3.17. Bus Monitor Trigger Occurrence HI/LO Register (TOR)

Read/Write @ Base+0x28 and Base+0x2A

This register is only used when the card is in monitor mode. These registers form a 32-bit address pointer defining where the bus monitor found the pre-defined trigger condition within the bus monitor stack. For further details, see the BUS_MON mode description.

3.18. Load Clock HGH/LOW Registers

Read/Write @ Base+0x2C Base+0x2E

These registers are used to define the value to load into the clock when a Load Clock command is asserted.

3.19. Inter-word Timeout Register

Read/Write @ Base+0x30

This register defines the time, in microseconds, the LDB_BCT, LDB_MRT, MDM_MRT or PRM_MDE shall wait to decide if another data word is arriving on the bus. The minimum allowable value for this register is 5uS.

3.20. Watchdog Timeout Register

Read/Write @ Base+0x32

The LDB_BCT, LDB_MRT, GSB_BCT, GSB_MRT or MDM_MRT will periodically read the contents of the Watchdog Change Register. If this register does not change value within the time set in the Watchdog Timeout Register, the card will automatically force a halt command and return itself to the idle state. The resolution of this register is 1mS per count. If the MSB of this register is set, the watchdog feature will be disabled.

3.21. Watchdog Change Register

Read/Write @ Base+0x34

If the Watchdog Timeout feature is enabled, this register must be updated with a new value within the Watchdog Timeout Register time. Failing to do so will result in the LDB_BCT, LDB_MRT GSB_BCT, GSB_MRT or MDM_MRT automatically halting.

3.22. Polling Timeout Register

Read/Write @ Base+0x36

The LDB_MRT will continuously poll for a new LDB_BCT command. During this period the LDB_MRT will timeout and generate an interrupt if the time, as defined by this register, has expired. This interrupt will cause an error word with the poll timeout error bit set followed by 3 consecutive values of 0xFFFF to be pushed onto the HI priority queue. The state machine for the RT, as defined in the RT Address Register, will be forced to WFI (wait for interrogate).

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
E	C	T	T	T	T	T	T	T	T	T	T	T	T	T	T

T: Time in milliseconds of polling timeout.
E: Set to disable this feature.
C: If set the MRT will go to the idle state after a timeout. If clear the LDB_MRT will continue to poll after generating an interrupt.
.

3.23. TX Amplitude Register

Read/Write @ Base+0x38

This register defines the TX amplitude for the card.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X	M	0	0	0	0	0	0	A	A	A	A	A	A	A	A

If M is set to 1:
The value of 'A' will be used as an absolute value to be programmed into the TX DAC.
If M is set to 0:
The value of A will be the desired voltage. This value is in 0.1 volt steps with the maximum value of 200 decimal for 20 volts. This mode will use calibration DAC values saved in EEPROM.

X: If set will use the IRIG-B input signal to synchronise the on-board clock.
If clear, the on-board clock will free run.

3.24. Uplink Queue Pointer

Read/Write @ Base+0x3A

When in GDB_BCT mode, a queue is available for saving uplink data transmitted in active mode or received in passive mode.

When in GDB_MRT mode, a queue is available for storing all the command word information from the GDB bus controller.

This queue is 2048 bytes long and can reside anywhere in the bottom 64Kbytes of memory providing it is set on an even 2048 byte boundary. This register must be initialised by the user to define where the queue is to be located.

When in PRM_MDE this shall define the address of the first buffer to be transmitted when the card is commanded to start.

3.25. Downlink Queue Pointer

Read/Write @ Base+0x3C

When in GDB_BCT, a queue is available for saving downlink received. This queue is 2048 bytes long and can reside anywhere in the bottom 64Kbytes of memory providing it is set on an even 2048 byte boundary. This register must be initialised by the user to define where the queue is to be located.

When in PRM_MDE, this shall define the address of the first buffer for storing received messages.

3.26. TX PRI Register, TX SEC Register

Read/Write @ Base+0x3E and Base+0x40

These registers shall be set to define which front panel connections shall be used as the primary and secondary TX connectors. In GDB mode, only the PRI register is relevant.

CONNECTOR	VALUE
BUS 1	0x0008
BUS 2	0x0004
BUS 3	0x0002
BUS 4	0x0001

3.27. RX PRI Register, RX SEC Register

Read/Write @ Base+0x42 and Base+0x44

These registers shall be set to define which front panel connections shall be used as the primary and secondary RX connectors. In GDB mode, only the PRI register is relevant.

CONNECTOR	VALUE
BUS 1	0x0008
BUS 2	0x0004
BUS 3	0x0002
BUS 4	0x0001

Note:
In LDB mode, if it is required to run the card in HALF-DUPLEX mode, the user **must** select the same connector for TX and RX buses.

3.28. RT Address Register

Read/Write @ Base+0x46

This register shall be set to a value in the range 0-31 defining the RT address for simulation or monitoring in LDB_MRT mode.

3.29. Wrap-round HI/LO Registers

Read/Write @ Base+0x46

These two registers shall define the test pattern and sync type to be transmitted for a wrap-round test as follows:

HI Register

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	S	0	0	0	0	0	0	D	D	D	D	D	D	D	D

S: Sync type to be transmitted. 1 = Command sync
D: Most significant 8 bits of data pattern.

LO Register

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

D: Least significant 16 bits of data pattern.

4. LDB MRT MODE

When the card is in LDB_MRT mode the card is capable of fully simulating/monitoring a single Remote Terminal. If the RT is disabled then the TX and RX data buffers will be filled with the actual activity for that RT as monitored on the Shuttle-Bus. The definition of the RT is defined in the MRT Simulation table. The MRT Simulation Table Pointer in the base registers defines the address of this table. This table must reside in the bottom 64Kbytes of memory. The RT address to be simulated/monitored is defined in the base registers.

4.1. RT Simulation Table

Table offset	Register Name
+0x0000	RT Mode
+0x0002	RT State Machine Register
+0x0004	RT IRQ Control Word A
+0x0006	RT IRQ Control Word B
+0x0008	RT TX data buffer HI
+0x000A	RT TX data buffer LO
+0x000C	RT RX data buffer HI
+0x000E	RT RX data buffer LO
+0x0010	PRI Bus Last Command Time Stamp HIGH
+0x0012	PRI Bus Last Command Time Stamp MIDDLE
+0x0014	PRI Bus Last Command Time Stamp LOW
+0x0016	PRI Bus Last Command Time Stamp TICKS
+0x0018	PRI Bus Last Command Value most significant 8 bits
+0x001A	PRI Bus Last Command Value least significant 16 bits
+0x001C	PRI Bus Last Response Value most significant 8 bits
+0x001E	PRI Bus Last Response Value least significant 16 bits
+0x0020	SEC Bus Last Command Time Stamp HIGH
+0x0022	SEC Bus Last Command Time Stamp MIDDLE
+0x0024	SEC Bus Last Command Time Stamp LOW
+0x0026	SEC Bus Last Command Time Stamp TICKS
+0x0028	SEC Bus Last Command Value most significant 8 bits
+0x002A	SEC Bus Last Command Value least significant 16 bits
+0x002C	SEC Bus Last Response Value most significant 8 bits
+0x002E	SEC Bus Last Response Value least significant 16 bits
+0x0030	PRI Bus State Machine Update Value
+0x0032	SEC Bus State Machine Update Value
+0x0034	RT GAH TX Error Injection word
+0x0036	RT GAH TX Error Injection word number
+0x0038	RT IND TX Error Injection word
+0x003A	RT IND TX Error Injection word number
+0x003C	RT IWD TX Error Injection word
+0x003E	RT IWD TX Error Injection word number
+0x0040	RT SRQ TX Error Injection word
+0x0042	RT SRQ TX Error Injection word number
+0x0044	RT FRC TX Error Injection word
+0x0046	RT FRC TX Error Injection word number
+0x0048	Reserved
|	|
+0x004E	Reserved

4.1.1. Mode Word

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
M	E	0	S2	S1	S0	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0

M: If the 'E' bit is clear and 'M' is 0 the RT will be passively monitored.
If the 'E' bit is clear and 'M' is 1 the RT will be simulated.

E: If set the RT will be disabled.

Normal mode

S2: 1 = Not ready to RX data

S1: 1 = Data to TX

S0: 1 = TX data is not critical

S2, S1, S0:
000 = No Data to Send, Respond to IWD with TXD (ready)
001 = Not allowed
010 = Critical Data to Send
011 = Non-Critical Data to Send, Respond to IWD with TXD
100 = No Data to Send, Respond to IWD with NNB (not ready)
101 = Not allowed
110 = Not allowed
111 = Non-Critical Data to Send, Respond to IWD with NNB (not ready)

T9-T0: If the poll response is DDT, the word-count field of the DDT will be set to the value of T9-T0.

Forced Message mode

S2, S1, S0:
000 = Attempt to RX number of data words defined by T9-T0
001 = Do not attempt to RX or TX any data words
010 = TX number of data words defined by T0-T9
011 = Not allowed

T9-T0: Number of data words to RX or TX.

4.1.2. State Machine Register

The contents of this register will reflect the current state in the data transfer cycle the RT is in. The possible states are as follows:

Value 0x01: Waiting for interrogate (WFI)
Value 0x02: Waiting for Go-head command (WFGAH)
Value 0x04: Waiting for Here-comes-data command (WFHCD)
Value 0x08. Waiting for Status command (WFS)
Value 0x10: Waiting for Status-request command (WFSR)
Value 0x20: Waiting for Status-request command after error (WFSRE)
Value 0x40: Forced RX/TX message mode (FORCED).

For normal operation, the value of this register MUST be initialised to the value WFI. From then on, this register will be automatically updated by the firmware. However, if the user wishes to override the state machine algorithm, writing a new value to this register can do this. For further details of the state machine algorithm see design specification document EN0054 Revision A.

Setting the value of this register to 'FORCED' will set the RT in Forced Message mode. After receiving a valid command, the RT will attempt to TX or RX the number of data words as defined by T9-T0 in the Mode Word Register. The value of this register will remain at 'FORCED' until the user changes it back into normal mode.

4.1.3. IRQ Control Word A/B

IRQ Word A

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	Q	B	G	Q	B	G	Q	B	G	Q	B	G	Q	B	G
	- FORCED -			---- SRQ ----			---- IND ----			---- GAH ----			---- HCD ----		

IRQ Word B

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	Q	Y	Y	Q	B	G	Q	B	G
							---- ILL ----			---- IWD ----			---- STA ----		

Q: If an interrupt is to be generated due to this message type, this bit shall define which queue the result shall be pushed onto.
Q=0 for LO priority queue. Q=1 for HI priority queue.

B, G : 00 = Do not interrupt on this message
01 = Interrupt only if message is good
10 = Interrupt only if message is bad
11 = Interrupt always on this message

Y For illegal Commands (ILL) an IRQ will be generated if D6 or D7 is set.

4.1.4. TX data buffer HI/LO

This shall be set to the byte offset from the base of the card, of the TX data buffer associated with this RT.

4.1.5. RX data buffer HI/LO

This shall be set to the byte offset from the base of the card, of the RX data buffer associated with this RT.

4.1.6. PRI/SEC Bus Last Command HI/LO/Value/Resp

These two 8 location blocks will be updated with the time-stamp and value of the most recent valid command to the RT. If the command was received and processed on the primary bus then the PRI bus locations will be updated. . If the command was received and processed on the secondary bus then the SEC bus locations will be updated. The last two words will be updated with the first word of the response from the RT. If the RT did not respond then these two words will be set to 0xFFFF. If the RT responded to data due to a GAH command, these two words will be set to 0xDABF indicating that the data response is in the TX data buffer.

4.1.7. PRI/SEC Bus State Machine Update Value

When a message is processed, the new RT state machine value will be saved in one of these registers according to the bus (PRI/SEC) that the message was processed on.

4.1.8. TX Error Injection and Word Number

Each message type that is capable of transmitting a response has it's own TX error definition. These messages are:

GAH	Go-Ahead
SRQ	Status Request
IND	Interrogate with no GPC data
IWD	Interrogate with GPC data available
FRC	Forced message mode

The format of the TX error word and TX error word number is as follows:

TX Error Word

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X	X	X	X	X	X	X	NE	T1	T0	I	I	I	I	I	I

NE = Error enable/disable, 0 = Enable.

T1	T0	
0	0	Parity Error
0	1	Sync Error
1	0	Manchester Error
1	1	Bit count Error

I = Error Information

For Parity Error	-- I = "don't care".
For Sync Error	-- I = pattern of the sync to TX in 6 segments.
For Man Error	-- I = bit number in word for Manchester Error.
For Bit Count Error	-- I = number of bits to TX.

TX Error Word Number

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	W	W	W	W	W	W	W	W	W	W

W = Word number in message for TX error injection.

If W = 0 the error will be injected in the 1st word transmitted.

4.2. TX/RX Data Buffers

Both the TX and RX data buffers have the same format as follows:

Buffer offset	Register Name
+0x0000	Time-stamp value HGH
+0x0002	Time-stamp value MID
+0x0004	Time-stamp value LOW
+0x0006	Time-stamp value TICKS
+0x0008	Buffer Size
+0x000A	Status Register
+0x000C	Word-count
+0x000E	Checksum Value
+0x0010	Next Address HI
+0x0012	Next Address LO
+0x0014	First word HI (most significant 8 bits and errors)
+0x0016	First word LO (least significant 16 bits)
|	|
|	|
+0xNNNN	Last word HI (most significant 8 bits and errors)
+0xNNNN	Last word LO (least significant 16 bits)

4.2.1. Time-stamp HGH/MID/LOW/TICKS

These 4 words shall be the 64-bit value of the local clock when the message started.

4.2.2. Buffer Size

This shall define the size of the buffer. When the number of words being transmitted or received exceeds the value in this register, the buffer overflow error (Ov) will be set. If the buffer is being used to RX data, the storing of data words will stop once the number of received words equals the value in this register.

4.2.3. Status Register

0x8000 = Message buffer being accessed

The error word shall be stored here on completion of the message. The value of this word will be 0x0000 if the message was good. If an error occurred a bit will be set defining the error type. These error bits shall be as defined for the HI/LO Priority Queues except for the MSB which will always be set to '0' on completion of the message.

4.2.4. Word-count

Number of data words received/transmitted in this buffer.

4.2.5. Checksum Value

When a message is received, the calculated checksum value for the message will be stored in this register. This will always occur regardless of the state of the checksum enable bit in the Bus Select Register.

4.2.6. Next Address HI/LO

This defines the address of the next RX/TX buffer to be filled once this buffer has been accessed. This feature is used where the user wishes to create a linked list of buffers. If only one buffer is required then this value should be set to the address of its own buffer.

4.2.7. Data word HI

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	Sy	Py	Mn	Lg	Sh	D	D	D	D	D	D	D	D

Sy = Sync type. 1 = Command Sync
Py = 1 = Parity error
Mn = 1 = Manchester error
Lg = 1 = Long word (too many bits)
Sh = 1 = Short word (too few bits)
D = Most significant 8 bits of word

4.2.8. Data word LO

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

D = Least significant 16 bits of word

4.3. HI/LO Priority Message Queues

Both HI and LO priority queues are 512 bytes long. Each entry will be 4 words resulting in 64 entries before wrap-round. The format of the QUEUE entries is as follows:

1st word:
Command word of message (LS byte = most significant 8 bits).
If bit 15 is set, the command was received on the secondary bus.

2nd word:
Command word of message (least significant 16 bits).

3rd word:
Errors if any detected as follows:-

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Pt	Rc	Is	Ck	Ig	Ev	Ov	Id	Nr	Ta	Wc	Sy	Py	Mn	Lg	Sh

Pt: 1 = Poll Timeout occurred
Rc: 1 = Real RT responded with illegal code
Is: 1 = Invalid message sequence
Ck: 1 = RX checksum error
Ig: 1 = Illegal Command Code
Ev: 1 = Alternate bus event occurred (see 4th word)
Ov: 1 = Buffer overflow error
Id: 1 = Illegal data word (status bits <> 101 for HCD message)
Nr: 1 = RT did not respond
Ta: 1 = Incorrect RT terminal address
Wc: 1 = Word-count error
Sy: 1 = Sync type error
Py: 1 = Parity error
Mn: 1 = Manchester encoding error
Lg: 1 = Long word error (too may bits)
Sh: 1 = Short word error (too few bits)

4th word:

This word will describe any activity that occurred on the other bus during message processing as follows:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
GC	GD	BC	BD	Py	Mn	Lg	Sh	1	1	1	1	1	1	1	1

GC: Good command to enabled RT received on other bus
GD: Good data to enabled RT received on other bus
BC: Bad command received on other bus
BD: Bad data received on other bus
Py: Parity error detected on other bus
Mn: Manchester error detected on other bus
Lg: Long word error detected on other bus
Sh: Short word error detected on other bus

This value is always non-zero and should be used for clearing by the user when the entry has been interrogated.

5. LDB BCT MODE

5.1. Background Program

In the LDB_BCT mode, the Background Running Pointer in the base registers directs the firmware to the location of a Background Program, which can be used to organise the message sequencing.
The various background program instructions are as follows:

Mnemonic	Code	Additional Info.	Description
DELAY	0x0000	VVVV	Wait for VVVV microseconds
NOP1	0x0001	None	PC = PC + 1
NOP2	0x0002	None	PC = PC + 2
NOP3	0x0003	None	PC = PC + 3
BSR	0x0004	VVVV	VVVV = 16-bit signed branch to subroutine
JSP	0x0005	VVVV	VVVV = Absolute address of subroutine
BRA	0x0006	VVVV	VVVV = 16-bit signed branch
JMP	0x0007	VVVV	VVVV = Absolute address for jump
RTS	0x0008	None	Return from subroutine
LOOP	0x0009	VVVV	Load loop counter with value VVVV
DBNE	0x000A	VVVV	Decrement loop counter and if non zero branch to signed offset VVVV
INITF	0x0000B	AAAA BBBB	Initialise frame duration to the value of 0xAAAA, 0xBBBB. These values shall define the frame duration as a 32 bit value with a resolution of 0.5uS per bit.
SWPSE	0x000C	None	Wait for new start of frame
HALT	0x000D	None	Halt BC operation
TRIGOUT	0x000E	VVVV	If the MSB of VVVV is set, a 1uS pulse will appear on TRIGGER OUT 3. The polarity of this pulse is defined by the LSB of VVVV. If the MSB of VVVV is clear, the TRIGGER OUT 3 will go to the level defined by the LSB of VVVV.
SMB	0x000F	VVVV NNNN	Execute MDB at 0xVVVV. If SMB is returned true jump to 0xNNNN else continue.
SITH	0x0010	AAAA BBBB	Set HI PRIORITY queue interrupt and save words AAAA, BBBB on HI queue.
SITL	0x0011	AAAA BBBB	Set LO PRIORITY queue interrupt and save words AAAA, BBBB on HI queue.
HWPSE	0x0012	VVVV	Wait for transition on TRIG-IN input. VVVV(16 bits) = E00000000000TTTT. If bit ‘E’ set - card will wait for LO-HI. If bit ‘E’ clear - card will wait for HI-LO. One of the ‘T’ bits must be set to indicate which Trigger-In is to be polled – T3,T2,T1 or T0

5.2. Message Descriptor Block (MDB)

An SMB (Send Message Block) instruction will point to an MDB for defining the parameters associated with the message as follows:

MDB offset	Register Name
0x0000	Message Number
0x0002	IRQ Control Register
0x0004	Command HI word
0x0006	Command LO word
0x0008	TX Error Word
0x000A	TX Error Word Number
0x000C	Data Buffer Address HI
0x000E	Data Buffer Address LO
0x0010	Data Word-count Register
0x0012	Message Event Register
0x0014	Bit Pattern HI Register
0x0016	Bit Pattern LO Register
0x0018	Bit Mask HI Register
0x001A	Bit Mask LO Register
0x001C	Gap-time HGH
0x001E	Gap-time LOW

5.2.1. Message Number

This value will be used by the firmware as a handle to define which message information is on the interrupt queues. See HI/LO Priority Message Queues.

5.2.2. IRQ Control Register

The format of this register is as follows:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	0	0	0	0	0	Q	B	G

Q: If an interrupt is to be generated due to this message, this bit shall define which queue the result shall be pushed onto.

Q=0 for LO priority queue. Q=1 for HI priority queue.

B,G: 00 = Do not interrupt on this message
01 = Interrupt only if message is good
10 = Interrupt only if message is bad
11 = Interrupt always on this message

5.2.3. Command HI Register

This register shall define the upper most significant 8 bits of the command word to be transmitted and the bus that the message is to be transmitted on. The format of these words is as follows:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
P	S	0	0	0	0	0	0	C23	C22	C21	C20	C19	C18	C17	C16

C23-C16: Most significant 8 bits of command word
P: Set to 1 if TX is to be on Primary Bus.
S: Set to 1 if TX is to be on Secondary Bus.

5.2.4. Command LO Register

This register shall define the least significant 16 bits of the command word to be transmitted.

5.2.5. TX Error Word

This register shall define the error, if any, to be injected into the message.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X	X	X	X	X	X	X	NE	T1	T0	I	I	I	I	I	I

NE = Error enable/disable, 0 = Enable.

T1	T0	
0	0	Parity Error
0	1	Sync Error
1	0	Manchester Error
1	1	Bit count Error

I = Error Information

For Parity Error -- I = "don't care".
For Sync Error -- I = pattern of the sync to TX in 6 segments.
For Man Error -- I = bit number in word for Manchester Error.
For Bit Count Error -- I = number of bits to TX.

5.2.6. TX Error Word Number

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	W	W	W	W	W	W	W	W	W	W

W = Word number in message for TX error injection.

Note:
If W = 0 the error will be injected in the 1st word transmitted.

5.2.7. Data Buffer Address HI/LO

These two registers shall define the address of the data buffer associated with the message.

5.2.8. Data Word-count Register

This register shall define the number of words to follow the command word and the direction of transfer.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
D	S	0	0	0	0	C09	C08	C07	C06	C05	C04	C03	C02	C01	C00

D: If set to 1, BC shall follow command with C09-00 data words from the buffer.
If set to 0, BC shall expect a response of C09-00 data words from the RT.
S: If set to 1, BC shall interrogate the least significant 3 bits of each RX word and set the illegal data word bit 'Id' if the bits <> 101.
C09-00 Data word-count for message.

5.2.9. Message Event Register

The SMB command has a conditional JUMP associated with it. On completion of the message the SMB returns TRUE or FALSE. If the result is returned TRUE the background program jumps to the location defined by 0xNNNN (see SMB command description). If the result is returned FALSE the program continues at the next location after the 0xNNNN value. This register shall define the event required for the result to be returned TRUE.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	Bp	Bs	Ov	Id	Nr	Ta	Wc	Sy	Py	Mn	Lg	Sh

Bp: 1 = SMB jump if word received from RT as defined in pattern and mask registers
Bs: 1 = SMB jump if transmission on Wrong or Both Buses
Ov: 1 = SMB jump if buffer overflow
Id: 1 = SMB jump if word received from RT with status bits <> 101
Nr: 1 = SMB jump if RT did not respond
Ta: 1 = SMB jump if incorrect RT terminal address
Wc: 1 = SMB jump if Word-count error
Sy: 1 = SMB jump if Sync type error
Py: 1 = SMB jump if Parity error
Mn: 1 = SMB jump if Manchester encoding error
Lg: 1 = SMB jump if Long word error (too may bits)
Sh: 1 = SMB jump if Short word error (too few bits)

The error bits D09-D00 are an OR function such that setting all bits D08-D00 shall cause the SMB function to return TRUE if any error occurs.

5.2.10. Bit Pattern HI/LO Register

These two registers shall define the bit pattern requirement of a received RT data word to set the Bp event in the Message Event Register.

5.2.11. Bit Mask HI/LO Register

These two registers shall define the bits in the Bit Pattern HI/LO registers that are "don't care". If a bit is set to 1 in these registers that bit will not take part in the data word comparison.

Example:
Bit Pattern HI register = 0x0012
Bit Pattern LO register = 0x1234
Bit Mask HI register = 0x00FF
Bit Mask LO register = 0xFFF0

If the Bp bit is set in the Event Register the SMB will be returned true and a jump to 0xNNNN will be made if any RT word is received with the value XXX4.

5.2.12. Gap-time HGH/LOW

These registers shall define the gap-time before the next message is to be transmitted. These two registers form a 32 bit value defining the intermessage gap time with a resolution of 0.5uS per bit.

5.3. Data Buffers

The format of the data buffers is as follows:

Buffer offset	Register Name
+0x0000	Time-stamp value HGH
+0x0002	Time-stamp value MID
+0x0004	Time-stamp value LOW
+0x0006	Time-stamp value TICKS
+0x0008	Buffer Size
+0x000A	Status Register
+0x000C	Word-count
+0x000E	Reserved
+0x0010	Next Address HI
+0x0012	Next Address LO
+0x0014	First word most significant 8 bits
+0x0016	First word least significant 16 bits
|	|
|	|
+0xNNNN	Last word most significant 8 bits
+0xNNNN	Last word least significant 16 bits

5.3.1. Time-stamp HGH/MID/LOW/TICKS

These 4 words shall be the 64-bit value of the local clock when the message started.

5.3.2. Buffer Size

This shall define the size of the buffer. When the number of words being received exceeds the value in this register, the buffer overflow error (Ov) will be set. The storing of data words will stop once the number of received words equals the value in this register.

5.3.3. Status Register

0x8000 = Message buffer being accessed

The error word shall be stored here on completion of the message. The value of this word will be 0x0000 if the message was good. If an error occurred a bit will be set defining the error type. These error bits shall be as defined for the HI/LO Priority Queues.

5.3.4. Word-count

Number of data words received/transmitted in this buffer.

5.3.5. Next Address HI/LO

This defines the address of the next RX/TX buffer to be filled once this buffer has been accessed. This feature is used where the user wishes to create a linked list of buffers. If only one buffer is required then this value should be set to the address of its own buffer.

5.4. HI/LO Priority Message Queues

Both HI and LO priority queues are 512 bytes long. Each entry will be 2 words resulting in 128 entries before wrap-round. The format of the QUEUE entries is as follows:

1st word:

Errors if any detected as follows:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	Bs	Ov	Id	Nr	Ta	Wc	Sy	Py	Mn	Lg	Sh

Bs: 1 = Transmission on Wrong or Both Buses
Ov: 1 = Buffer overflow error
Id: 1 = Illegal data word received (status bits <> 101)
Nr: 1 = RT did not respond
Ta: 1 = Incorrect RT terminal address
Wc: 1 = Word-count error
Sy: 1 = Sync type error
Py: 1 = Parity error
Mn: 1 = Manchester encoding error
Lg: 1 = Long word error (too may bits)
Sh: 1 = Short word error (too few bits)

2nd word:

Message number from MDB.

Note:
If the BC halts due to detecting command activity on an enabled bus, two words of value 0xFFFF will be pushed to the HI priority queue.

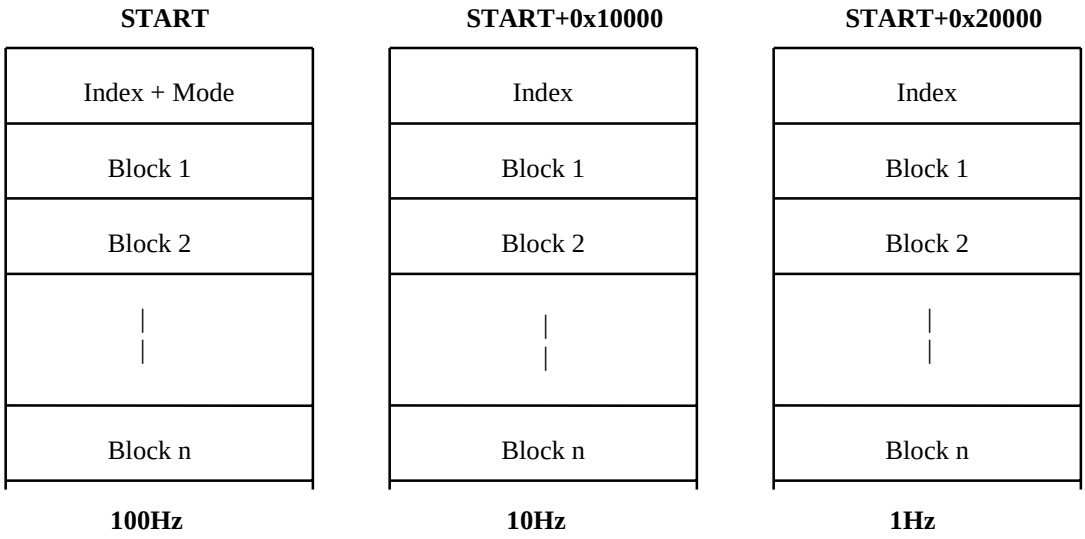
6. GDB BCT MODE

6.1. Introduction

The GDB interface consists of three components. The measurement poll tables, the command queues and the uplink/downlink queues. The poll tables define the GDB data bus operation by specifying the measurement poll and command execution rates. For measurement polls, the tables also contain the measurement addressing information. Nominally, the tables are executed at a fixed rate of 100uS per entry. However, the Gap Time Register in the base registers defines this duration allowing the time to be programmable from 90 to 500uS.

6.2. Measurement Poll Tables

In the GDB_BCT mode, the Program Pointer in the base registers directs the firmware to the start of a 64Kbyte block where the Poll Tables reside. These tables shall be as follows:



The Program Pointer shall be set to a number defining the 64Kbyte block within the 2Mbyte memory for the start of the tables. For example, if the Program Pointer is set to 4 then the tables must start at 0x40000 offset from the base address of the card. The start 10Hz table shall be 64Kbytes after the start of the 100Hz table. The1Hz table shall be 64Kbytes after the start of the 10Hz table.
The Program Pointer is continually updated so that dynamic switching between different tables is achieved by changing the value in the Program Pointer whilst the GDB_BCT is running.

Note:
The tables **must not** reside in the bottom 64Kbytes of the card and hence the value of 0 in the Program Pointer is not allowed.

6.2.1. Index Register

The Index Register is in the 1st 16 bit word location of each of the 3 tables. This shall point to the next block in the table to be executed. The user must initialise this register. When the GDB_BCT is running these values will be continually updated.

Note:
The block numbers start at 1. The Index Register **must not** be initialised to 0.

6.2.2. Mode Register

This register is only applicable to the 100Hz table. For the 10Hz and 1Hz tables the 3 words following the Index Register are not used. In the case of the 100Hz table the word following the Index Register shall be the Mode Register:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
M	0	0	0	0	0	0	ER	0	QT	PU	PD	UQ	UI	GU	GD

M: 1 = Passive Monitor Mode, 0 = Active Mode.
QT: 1 = Halt if UPLINK or DOWNLINK queue is full.
PU: 1 = Generate interrupt on receipt of an UPLINK word in Passive Monitor Mode.
PD: 1 = Generate interrupt on receipt of a DOWNLINK word in Passive Monitor Mode.
UQ: 1 = Push unsolicited response words to the DOWNLINK queue.
UI: 1 = Generate interrupt on receipt of an unsolicited response word.
GU: 1 = Global UPLINK interrupts enabled.
GD: 1 = Global DOWNLINK interrupts enabled.
ER: 1 = Global TX errors disabled.

This register is continually updated to allow dynamic change over from Passive to Active modes and enable/disable of interrupt definitions. The two words following the Mode Register are not used.

6.2.3. Polling Table Blocks

Each Polling Table Block consists of four 16 bit words. The first word is an opcode defining the action to be taken. The meaning of the remaining three words is dependant on the opcode. The allowable opcodes are:

NOOP (Value 0x0000)

The index pointer for the table will be incremented and **no operation** will be carried out during the polling time. The remaining three words of the block are not used.

CMND (Value 0x1000)

The **command** opcode will direct the card to interrogate the HI and LO command insertion queues. If there is an entry on the HI or LO priority command queues a TX of a command word onto the GDB bus will be initiated using the information stored on the queue. If there is an entry on both queues then the HI priority queue value will be used. If both queues are empty, the **command** will be treated as a NOOP. For further details see the HI and LO Command Queue description.
The remaining three words of the block are not used.

MSRE (Value 0x2nnn)

The **measure** opcode will initiate a TX of a command word onto the GDB bus. The most significant four bits of the measure opcode shall be set to 0010. The remaining bits shall define the TX error injection required for the word as follows:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	1	0	0	0	0	NE	T1	T0	I	I	I	I	I	I

NE = Error enable/disable, 0 = Enable.

T1	T0	
0	0	Parity Error
0	1	Sync Error
1	0	Manchester Error
1	1	Bit count Error

I = Error Information

For Parity Error -- I = "don't care".
For Sync Error -- I = pattern of the sync to TX in 6 segments.
For Man Error -- I = bit number in word for Manchester Error.
For Bit Count Error -- I = number of bits to TX.

The remaining 3 words of the block shall be as follows:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	DQ	DI	UQ	UI	DE	Sy	R	R	R	R	R	R	R	R

DQ: 1 = Push response from this command onto the DOWNLINK queue.
DI: 1 = Generate an interrupt when the response to this command is received.
UQ: 1 = Push this command to the UPLINK queue when it is transmitted.
UI: 1 = Generate an interrupt when this command is transmitted.
DE: 1 = Only push downlink response to queue if an error is encountered (active mode only).
Sy: Sync type for word. 1 = Command sync, 0 = Data sync.
R: RT address bits for command word.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M

M: For 24-bit data mode this shall be the remaining bits of the command word to be transmitted.
For 40-bit data mode this shall be the next 16 bits of the command word to be transmitted..

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

L: For 24-bit data mode this word is not used.
For 40-bit data mode this shall be the remaining bits of the command word to be transmitted.

SWCH (Value 0x3000)

This opcode can only be used in the 100Hz and 10Hz tables. The index pointer for the table is incremented and the control is **switched** to the next table. The next table index pointer is then read and used as the pointer for the new opcode to be executed. The switch opcode does not take up the polling time. It is a level of indirection to get to the actual opcode to be executed. The remaining three words of the block are not used.

ETAB (Value 0x4000)

The **end of table** opcode causes the index pointer for the table to be reset to 1. The opcode at index 1 of the table will then be immediately executed. The remaining three words of the block are not used.

TRIG (Value 0x5000)

The index pointer for the table will be incremented and the TRIGGER 3 output will be set to the value of the LSB of the word following the opcode. No other operation will be carried out during the polling time. The remaining two words of the block are not used.

HALT (Value 0x6000)

The **halt** opcode will cause the GDB_BCT to immediately stop executing and go into an idle state. The remaining three words of the block are not used.

6.3. Hi and LO Priority Command Insertion Queues

Two queues are available in the bottom 64Kbytes of memory for inserting acyclic commands. The address of these queues is defined by the value set in the HI/LO Priority Queue Pointers in the base registers.
When a **CMND** opcode is encountered in the polling tables these two queues will be interrogated for an entry. If an entry exists then the information in the queue will be used to TX a command word onto the GDB bus. If there is an entry in both queues then the HI Priority Queue data will be used. An entry consists of four 16 bit words as follows:

1st word:

This must be set the same as a measure opcode. When the entry has been serviced, this value will be cleared.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	1	0	0	0	0	NE	T1	T0	I	I	I	I	I	I

NE = Error enable/disable, 0 = Enable.

T1	T0	
0	0	Parity Error
0	1	Sync Error
1	0	Manchester Error
1	1	Bit count Error

I = Error Information

For Parity Error -- I = "don't care".
For Sync Error -- I = pattern of the sync to TX in 6 segments.
For Man Error -- I = bit number in word for Manchester Error.
For Bit Count Error -- I = number of bits to TX.

2nd Word:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X1	X0	DQ	DI	UQ	UI	DE	Sy	R	R	R	R	R	R	R	R

X1,X1 These bits **must** be set to 01 for LO priority and 10 for HI priority queue entries
DQ: 1 = Push response from this command onto the DOWNLINK queue.
DI: 1 = Generate an interrupt when the response to this command is received.
UQ: 1 = Push this command to the UPLINK queue when it is transmitted.
UI: 1 = Generate an interrupt when this command is transmitted.
DE: 1 = Only push downlink response to queue if an error is encountered (active mode only).
Sy: Sync type for word. 1 = Command sync, 0 = Data sync.
R: RT address bits for command word.

3rd Word

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M

M: For 24-bit data mode this shall be the remaining bits of the command word to be transmitted.
For 40-bit data mode this shall be the next 16 bits of the command word to be transmitted.

4th Word

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

L: For 24-bit data mode this word is not used.
For 40-bit data mode this shall be the remaining bits of the command word to be transmitted.

These queues are 512 bytes long allowing up to 64 pending commands to be stored. The address of these queues can reside anywhere in the bottom 64Kbytes of memory providing they are set on an even 512 byte boundary. It is the responsibility of the user to clear these queues prior to runtime.

6.4. Uplink Queue

A queue is available in the bottom 64Kbytes of memory for the storing of uplink information. If commanded the card will store uplink information as four 16 bit words as follows:

1st Word

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X1	X0	0	Sy	Py	Mn	Lg	Sh	R	R	R	R	R	R	R	R

X1,X0 00 = Word from table, 01 = Word from LO priority Command Queue
10 = Word from HI priority Command Queue
Sy: 1 = Uplink word had a command SYNC type
Py: 1 = Uplink word had a Parity error
Mn: 1 = Uplink word had a Manchester encoding error
Lg: 1 = Uplink word had a Long word error (too may bits)
Sh: 1 = Uplink word had a Short word error (too few bits)
R: Most significant 8 bits of word

The Py, Mn, Lg and Sh bits are only applicable when the card is reading in the real BC uplink data in passive monitor mode.

2nd Word

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M

M: For 24-bit data mode this shall be the remaining bits of the command word.
For 40-bit data mode this shall be the next 16 bits of the command word.

3rd Word

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

L: For 24-bit data mode this word is not used.
For 40-bit data mode this shall be the remaining bits of the command word.

This queue is 2048 bytes long allowing up to 256 uplink words be stored before wrap-round. The address of this queue can reside anywhere in the bottom 64Kbytes of memory providing it is set on an even 2048 byte boundary. It is the responsibility of the user to clear this queue prior to runtime.

4th Word

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
T1	T0	I	I	I	I	I	I	I	I	I	I	I	I	I	I

T1, T0: 01 = 100Hz table, 10 = 10Hz table, 11 = 1Hz table
I: Index in table that caused uplink entry.

When in passive monitor mode this value will always be set to 0x0001.

The value of this word will always be non-zero. It is the responsibility of the user to keep record of this queue and to clear this word once the entry is finished with.

6.5. Downlink Queue

A queue is available in the bottom 64Kbytes of memory for the storing of downlink information. If commanded the card will store downlink information as four 16 bit words as follows:

1st Word

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X1	X0	Nr	Sy	Py	Mn	Lg	Sh	R	R	R	R	R	R	R	R

X1,X0 00 = Response to word from table
01 = Response due to word from LO priority Command Queue
10 = Response due to word from HI priority Command Queue
11 = Response was unsolicited
Nr: 1 = No response to uplink command
Sy: 1 = Downlink word had a command SYNC type
Py: 1 = Downlink word had a Parity error
Mn: 1 = Downlink word had a Manchester encoding error
Lg: 1 = Downlink word had a Long word error (too may bits)
Sh: 1 = Downlink word had a Short word error (too few bits)
R: Most significant 8 bits of word

The Nr bit is only applicable in active mode. If this bit is set then all other error bits in the 1st word will be clear. The 4th word will define the table and index number as normal. The least significant 8 bits of the 1st word and the contents of the 2nd and 3rd words will contain the bit pattern of the uplink command that caused the no response.

2nd Word

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M

M: For 24-bit data mode this shall be the remaining bits of the response word.
For 40-bit data mode this shall be the next 16 bits of the response word.

3rd Word

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

L: For 24-bit data mode this word is not used.
For 40-bit data mode this shall be the remaining bits of the response word.

This queue is 2048 bytes long allowing up to 256 downlink words be stored before wrap-round. The address of this queue can reside anywhere in the bottom 64Kbytes of memory providing it is set on an even 2048 byte boundary. It is the responsibility of the user to clear the queue prior to runtime.

4th Word

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
T1	T0	I	I	I	I	I	I	I	I	I	I	I	I	I	I

T1,T0: 01 = 100Hz table, 10 = 10Hz table, 11 = 1Hz table
I: Index in table that caused downlink entry.

When in passive monitor mode this value will always be set to 0x0001.
If the received word is due to an unsolicited response, this value will be set to 0xFFFF.

NOTE:
Any response that does not have the correct address or is invalid will be regarded as unsolicited.
The value of this word will always be non-zero. It is the responsibility of the user to keep record of this queue and to clear this word once the entry is finished with.

6.6. Passive Monitor Mode

When the most significant bit of the MODE word is set, the card will go into passive monitor mode and the status register will change to the value 0x9041.
In this mode, both the uplink and downlink buses will be monitored and the received data stored on their respective queues. Global interrupt enable/disable flags for both uplink and downlink buses are available in the mode word.
As the mode word is continually updated, the Passive/Active mode of operation can be changed dynamically without having to stop the card.

7. GDB MRT MODE

When the card is in GDB_MRT mode the card is capable of simulating/monitoring all 256 Remote Terminals. The global definition for each RT is defined in the MRT Simulation table. The RT Simulation Table Pointer in the base registers defines the address of this table. This table must reside in the bottom 64Kbytes of memory on an even 4Kbyte boundary.

7.1. RT Simulation Table

Table offset	Register Name
+0x0000	RT000 Pointer HI
+0x0002	RT000 Pointer LO
+0x0004	RT000 2nd Response HGH
+0x0006	RT000 2nd Response MID
+0x0008	RT000 2nd Response LOW
+0x000A	TX error word
+0x000C	Not used
+0x000E	Not used
|	|
|	|
+0x0FF0	RT255 Pointer HI
+0x0FF2	RT255 Pointer LO
+0x0FF4	RT255 2nd Response HGH
+0x0FF6	RT255 2nd Response MID
+0x0FF8	RT255 2nd Response LOW
+0x0FFA	TX error word
+0x0FFC	Not used
+0x0FFE	Not used

7.1.1. Pointer HI Register

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
R	DQ	DI	EI	0	0	0	ER	0	0	0	A	A	A	A	A

R: 1 = RT enabled, 0 = RT disabled.
DQ: 1 = Push commands that have the responses disabled to the queue.
DI: 1 = Generate an interrupt for response disabled commands.
EI: 1 = Global interrupt enable.
A: 1 = Upper address of channel lookup table.
ER: 1 = Global TX errors disabled.

Note:
The DQ, DI and EI bits are global control bits and reside in the Pointer HI Register for RT 000 only. These bits are used to globally control the interrupt generation for all commands of all the RTs. The card continually reads the Pointer HI Register for RT 000 thus allowing dynamic changes to the global interrupt enable/disable bits.

7.1.2. Pointer LO Register

This register shall contain the least significant 16 bits of the address of the channel lookup table. The most significant 5 bits of this address is defined in the HI register.

7.1.3. 2nd Response HGH word

If a particular channel of an RT is commanded to send an extra response then the word will be as defined in the 2nd response register. It is possible to define one unique 2nd response for each RT. This is used for simulating unsolicited responses.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	S	0	0	0	0	0	0	R	R	R	R	R	R	R	R

S: 0 = Data Sync, 1 = Command
R: Most significant 8 bits of response word.

7.1.4. 2nd Response MID/LOW words

These two locations shall contain the remaining bits of the 2nd response to be transmitted.
If the card is in 24-bit mode, the LOW register will not be used.

7.1.5. TX Error Word

This shall define the error injection required for the TX of the word.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	1	0	0	0	0	NE	T1	T0	I	I	I	I	I	I

NE = Error enable/disable, 0 = Enable.

T1	T0	
0	0	Parity Error
0	1	Sync Error
1	0	Manchester Error
1	1	Bit count Error

I = Error Information

For Parity Error	-- I = "don't care".
For Sync Error	-- I = pattern of the sync to TX in 6 segments.
For Man Error	-- I = bit number in word for Manchester Error.
For Bit Count Error	-- I = number of bits to TX.

7.2. 40 Bit Mode Intermediate Lookup Table

If the card is running in 40-bit data mode then the address pointer in the RT Simulation Table must point to a 256 element lookup table. Each element shall consist of two 16 bit words defining the address of a channel lookup table as follows:

1st Word

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
E	0	0	0	0	0	0	0	0	0	0	A	A	A	A	A

E: 0 = Channel disabled, 1 = Channel Enabled.
A: Most significant 5 bits of the channel lookup table address.

2nd Word

This shall contain the least significant 16 bit of the channel lookup table address.
The value of the most significant 8 bits of the 16 bit channel number, as received from the bus controller command word, will be used as an offset to select 1 of the 256 elements in the Intermediate Lookup Table.

7.3. Channel Lookup Table

In 40-bit data mode this table will be pointed to by one of the elements of an **Intermediate Table**.
In 24-bit data mode this table will be pointed at directly from the **RT Simulation Table**.

The Channel Lookup Table consists of 256 elements. Each element shall consist of eight 16 bit words defining the response to a command as follows:

1st Word

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
E	S	U	I	C	T1	T0	ER	R	R	R	R	R	R	R	R

E: 0 = Channel disabled, 1 = Channel enabled.
S: 0 = Data Sync, 1 = Command
U: 1 = Follow response with unsolicited response as defined in the RT Simulation Table
I: 1 = Generate an interrupt
C: 1 = Respond with RT address bits as defined in command word. Do not use 'R' bits.
R: Most significant 8 bits of the response word.
ER: 1 = Disable TX errors for this channel.

The 'C' bit allows different RTs to share the same Channel Lookup Table without generating incorrect RT address responses.

The type T1, T0 bits and the SYNC type of the incoming command word defines the message type as follows:

T1	T0	SYNC TYPE	
0	0	Command	COMMAND
0	0	Data	MEASUREMENT
0	1	Command	DISCRETE
0	1	Data	MEASUREMENT
1	0	Don't care	MEASUREMENT
1	1	Don't care	ANALOG

COMMAND

For COMMAND channels word 5 is a bit-reset mask, word 6 is a bit-set mask. The received data from the GDB command is logically ANDed with NOT word 5 then logical ORed with word 6.
The final result forms the response data to be output and also stored back in the response word (word 2 for 24-bit, word 3 for 40-bit).

DISCRETE

DISCRETE channels contain two adjacent bits per discrete. In 24-bit mode, each channel contains 4 discretes, with 8 per channel in 40-bit mode. A value of 01 (binary) indicates discrete on and a value of 10 indicates discrete off. Command data may also contain 00 or 11 to indicate no change for that discrete. When a command data word is received, only the discrete(s) containing 01 or 10 are affected as follows:

Previous channel value:	0xaa
Command data:	0x01
Normal response value:	0xa9

Word 5 is a bit-reset mask, word 6 is a bit-set mask. The data from the GDB command is used to form the normal response as previously defined. This response is then logically ANDed with NOT word 5 then logical ORed with word 6. The final result forms the response data to be output and also stored back in the response word (word 2 for 24-bit, word 3 for 40-bit).

MEASUREMENT

For MEASUREMENT channels word 5 is a bit-reset mask, word 6 is a bit-set mask. The response data (word 2 for 24-bit, word 3 for 40bit) is logically ANDed with NOT word 5 then logical ORed with word 6. The final result forms the response data.

ANALOG

If the command data is 0xA9 (0x00A9 in 40-bit mode), word 5 is used as the response data (LO cal data). If the command data is 0xAA (0x00AA in 40-bit mode), word 6 is used as the response data (HI cal data).
Otherwise the response is normal (word 2 for 24-bit, word 3 for 40-bit).

Note:
Words 5 and 6 contain data only. When in 24-bit mode the 8-bit data will be right justified in the 16 bit word with the upper 8 bits always zero. The channel address is always as already defined (upper 8 bits of word 2 in 24-bit mode, all of word 2 in 40-bit mode).

2nd and 3rd Word

These two locations shall contain the remaining bits of the response to be transmitted. If the card is in 24-bit mode, the 3rd word will not be used.

4th Word

This shall define the response time in microseconds from the end of the received command word to the start of the response word.

In 40-bit data mode the value of the least significant 8 bits of the 16 bit channel number, as received from the bus controller command word, will be used as an offset to select 1 of the 256 elements in the Channel Lookup Table.
In 24-bit data mode the value of the least 8 bit channel number, as received from the bus controller command word, will be used as an offset to select 1 of the 256 elements in the Channel Lookup Table.

5th Word

NOT-AND mask. For further details, see the message TYPE descriptions.

6th Word

OR mask. For further details, see the message TYPE descriptions.

7th Word

Not used.

8th Word

Not used.

7.4. Command Receive Queue

A queue is available in the bottom 64Kbytes of memory for the storing received commands. The position of this queue is defined by the Uplink Queue Pointer in the base registers. The card will store the information as four 16 bit words as follows:

1st Word

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	Sy	Py	Mn	Lg	Sh	R	R	R	R	R	R	R	R

Sy: 1 = Word had a command SYNC type
Py: 1 = Word had a Parity error
Mn: 1 = Word had a Manchester encoding error
Lg: 1 = Word had a Long word error (too may bits)
Sh: 1 = Word had a Short word error (too few bits)
R: Most significant 8 bits of word

2nd Word

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M

M: For 24-bit data mode this shall be the remaining bits of the command word.
For 40-bit data mode this shall be the next 16 bits of the command word.

3rd Word

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

L: For 24-bit data mode this word is not used.
For 40-bit data mode this shall be the remaining bits of the command word.

This queue is 2048 bytes long allowing up to 256 words be stored before wrap-round. The address of this queue can reside anywhere in the bottom 64Kbytes of memory providing it is set on an even 2048 byte boundary. It is the responsibility of the user to clear this queue prior to runtime.

4th Word

This shall be 1 of 2 values:
0x0001 Command words that were responded to by the card.
0xFFFF Command words that had the response disabled (if allowed in the global control bits).

The value of this word will always be non-zero. It is the responsibility of the user to keep record of this queue and to clear this word once the entry is finished with.

8. BUS MON MODE

The bus monitor function allows the capture and storage of Shuttle-bus activity on a stack. This stack will wrap-round such that continuous monitoring is possible. Two Interrupts are available for indicating to the user when the trigger condition is met and when wrap-round occurs. These interrupts are defined in the base registers in the same way as for BCT and MRT modes. However, in this case there are no HI and LO priority queues. The HI priority interrupt is used to indicate when the trigger has occurred and the LO priority is used to indicate when wrap-round or end of post trigger data has occurred.
When the card is commanded to run, the monitor will capture all data activity and save it on the stack. When the pre-defined trigger condition is found, an interrupt will be generated and the address in the stack where the trigger occurred will be saved in the Trigger Occurrence Register (TOR) in the base registers. After this, the monitor will save data up to the pre-defined post trigger count. This will enable the user to capture both pre and post trigger data. However, if the user wishes, the post trigger count can be set to a 'forever' condition such that capture will continue until the card is commanded to stop. A second interrupt will be generated when the card gets to the end of the stack and begins storing back at the top (wrap-round). The Current Address Register (CAR) in the base registers will be continually updated with the address in the stack where the monitor is storing data.

Note:
In BUS_MON mode, the memory area **0x10000 to 0x1FFFF is reserved** for use by the on-board DSP and **must not** be modified by the application or used as part of the stack.

8.1. Trigger Set-up Data

The value of the Trigger Set-up Pointer shall point to a data block defining the trigger condition for the capture of data by the Bus Monitor. The format of this data block shall be as follows:

Set-up offset	Register Name
+0x0000	Mode Select Register
+0x0002	Bus Definition Register
+0x0004	Bus Definition Disable Register
+0x0006	Bit Pattern HGH Register
+0x0008	Bit Pattern MID Register
+0x000A	Bit Pattern LOW Register
+0x000C	Bit Mask HGH Register
+0x000E	Bit Mask MID Register
+0x0010	Bit Mask LOW Register
+0x0012	Error Event Register
+0x0014	RT Selection Lookup Table Pointer
+0x0016	Post Trigger Count HI Register
+0x0018	Post Trigger Count LO Register
+0x001A	Stack Start HI Register
+0x001C	Stack Start LO Register
+0x001E	Stack End HI Register
+0x0020	Stack End LO Register

8.1.1. Mode Select Register

LDB: If set to 0, the selective capture will use the 5 MSBs of the word for determining the RT address
GDB: If set to 1, the selective capture will use the 8 MSBs of the word for determining the RT address

8.1.2. Bus Definition Register

This register shall be set to 1 of 4 values defining the particular bus the RX word must be received on to meet the bus monitor trigger condition.

BUS 1 = 0x0000, BUS 2 = 0x4000, BUS 3 = 0x8000, BUS 4 = 0xC000

8.1.3. Bus Definition Disable Register

This register shall be set to one of two values:

0x0000 = Enable bus definition
0xC000 = Disable bus definition (RX bus is "don't care" for trigger condition).

8.1.4. Bit Pattern HGH/MID/LOW Register

These three registers shall define the bit pattern requirement of a data word for the trigger condition to be met. If the card is running in 24-bit mode, the LOW register is not relevant.

8.1.5. Bit Mask HGH/MID/LOW Register

These three registers shall define which bits of the Bit Pattern Registers are "don't care" such that they play no part in the trigger condition test. If a bit is set in this register, the corresponding bit in the Bit Pattern Register will become a "don't care" condition.

40-bit mode example:
Bit Mask HGH = 0x00FF
Bit Mask MID = 0xFFFF
Bit Mask LOW = 0xFFFF **……..** Trigger on any word.

Note: If the card is running in 24-bit mode, the LOW mask value **must be set to 0xFFFF**.

8.1.6. Error Event Register

The value of this register shall define what error(s) and sync type must occur before the trigger condition is met.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X	0	0	0	0	0	0	0	0	0	Cs	Ds	Py	Mn	Lg	Sh

X: 1 = Disable Error Bits Py, Mn, Lg, Sh from trigger condition
Cs: 1 = Trigger on Command Sync
Ds: 1 = Trigger on Data Sync
Py: 1 = Parity error
Mn: 1 = Manchester encoding error
Lg: 1 = Long word error (too may bits)
Sh: 1 = Short word error (too few bits)

Note:
- If the MSB of this register is set to 1 then the error bits will take no part in the trigger condition.
- If more than one of the Py, Mn, Lg, Sh bits are set then the trigger will occur if any of these errors occur.
- At least one of Cs and Ds **must** be set to 1. Setting both will result on a trigger on any sync.
- For this register to take no part in the trigger condition set to the value 0x8030.
- The value 0x0030 will cause a trigger on any sync with **no** error.

8.1.7. RT Selection Lookup Table Pointer

The contents of this register shall point to a 256 word lookup table in the bottom 64K of memory. Each location of this lookup table represents a particular RT number (0 = RT0, 255 = RT255). If the location in the lookup table corresponding to that RT is clear then any bus word with the RT field set to the same address will NOT be saved on the stack. This will allow selective capture of particular RT messages.

Note:
Setting this register to 0 will disable the selective mode such that all bus traffic will be stored.

8.1.8. Post Trigger Count HI/LO Register

The contents of these two registers shall define the number of words to save on the stack after the trigger condition is met. If the value of these registers is 0 the card will continue forever filling the stack, with wrap-round, until the user commands the card to stop.

8.1.9. Stack Start HI/LO Register

The contents of this register shall define the absolute address for the start of the stack.

8.1.10. Stack End HI/LO Register

The contents of this register shall define the absolute address for the end of the stack.

NOTE:
Each bus word is represented by 16 bytes. The user **must** make the total stack size a multiple of 16 bytes.

8.2. Stack Data

Each BC command – RT response will be represented on the stack in 8 words as follows:

1. Time-tag HGH
2. Time-tag MID
3. Time-tag LOW
4. Time-tag TICKS
5. Errors and Pattern HGH
6. Pattern MID
7. Pattern LOW
8. Not used

8.2.1. Command Time-tag HIGH/MIDDLE/LOW/TICKS

These 4 words shall be the 64-bit value of the local clock when the command word arrived.

8.2.2. Errors and Pattern HI

This word shall contain the errors detected and the most significant 8 bits of the command data field as follows:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
B1	B0	0	Sy	Py	Mn	Lg	Sh	P	P	P	P	P	P	P	P

B1	B0	
0	0	Word received on BUS 1
0	1	Word received on BUS 2
1	0	Word received on BUS 3
1	1	Word received on BUS 4

Sy: 1 = Word had Command Sync, 0 = Word had Data Sync
Py: 1 = Parity error
Mn: 1 = Manchester encoding error
Lg: 1 = Long word error (too may bits)
Sh: 1 = Short word error (too few bits)

P: Most significant 8 bits of data field.

8.2.3. Pattern MID/LOW

These words shall contain the remaining bits of the word.
In 24-bit mode the LOW word is not used.

9. MDM MRT MODE

When in MDM_MRT mode the card is capable of simulating all 32 Remote Terminals. Each RT is defined in the MRT Simulation table. The MRT Simulation Table Pointer in the base registers defines the address of this table. This table must reside in the bottom 64Kbytes of memory on an even 2Kbyte boundary. Each RT definition is separated by 0x0040 bytes.

9.1. RT Simulation Table

Table offset	Register Name
+0x0000	RT00 Mode
+0x0002	RT00 IRQ Control Word A
+0x0004	RT00 IRQ Control Word B
+0x0006	RT00 IRQ Control Word C
+0x0008	BITE Config Pointer
+0x000A	PROM Pointer
+0x000C	CHANNEL table pointer HI
+0x000E	CHANNEL table pointer LO
+0x0010	RCP TX Error Injection Word
+0x0012	RCP TX Error Injection Word Number
+0x0014	EPS TX Error Injection Word
+0x0016	EPS TX Error Injection Word Number
+0x0018	BT2 TX Error Injection Word
+0x001A	BT2 TX Error Injection Word Number
+0x001C	BT4 TX Error Injection Word
+0x001E	BT4 TX Error Injection Word Number
+0x0020	IFI TX Error Injection Word
+0x0022	IFI TX Error Injection Word Number
+0x0024	RBC TX Error Injection Word
+0x0026	RBC TX Error Injection Word Number
+0x0028	RCW TX Error Injection Word
+0x002A	RCW TX Error Injection Word Number
+0x002C	Reserved
+0x002E	Reserved
+0x0030	Last CMND TTAG HGH
+0x0032	Last CMND TTAG MID
+0x0034	Last CMND TTAG LOW
+0x0036	Last CMND TTAG TICKS
+0x0038	Last CMND Value HGH
+0x003A	Last CMND Value LOW
+0x003C	Primary BSR
+0x003E	Secondary BSR
|	|
|	|
+0x07C0	RT31 Mode
+0x07C2	RT31 IRQ Control Word A
+0x07C4	RT31 IRQ Control Word B
|	|
+0x07FC	Primary BSR
+0x07FE	Secondary BSR

9.1.1. Mode Word

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
E	0	0	0	0	0	P	0	0	0	0	0	0	0	S	M

E: If set to 1, RT will be simulated.

M: If set to 1, RT will simulate an Enhanced MDM allowing individual input/output Modules to be reset.

P: Power Interrupt Flag. It is the responsibility of the user to set this bit to '1' and set both BSR registers to 0x8000 prior to starting the card executing commands on the bus.

S: If set to 1, RT will simulate a Solid Rocket Booster MDM (this flag is reserved for future use).

9.1.2. IRQ Control Word A/B/C

IRQ Word A

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	Q	B	G	Q	B	G	Q	B	G	Q	B	G
				---- IFI ----			---- OTI ----			---- EPS ----			---- RCP ----		

IRQ Word B

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	Q	B	G	Q	B	G	Q	B	G	Q	B	G
				---- LBT ----			---- RCW ----			---- MRS ----			---- RBT ----		

IRQ Word C

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	Q	Y	Y	Q	B	G	Q	B	G	Q	B	G	Q	B	G
	---- ILL ----			---- BT4 ----			---- BT3 ----			---- BT2 ----			---- BT1 ----		

RCP: Return contents of PROM command
EPS: Execute PROM sequence command
OTI: Output to IOM command
IFI: Input from IOM command
RBT: Return BSR command
MRS: Master Reset command
RCW: Return Command Word command
LBT: Load BSR command
BT1: BITE 1 command
BT2: BITE 2 command
BT3: BITE 3 command
BT4: BITE 4 command
ILL: Illegal command (code not defined)

Q: If an interrupt is to be generated due to this message type, this bit shall define which queue the result shall be pushed onto.
Q=0 for LO priority queue. Q=1 for HI priority queue.

B, G: 00 = Do not interrupt on this message
01 = Interrupt only if message is good
10 = Interrupt only if message is bad
11 = Interrupt always on this message

Y: For illegal commands an IRQ will be generated if D13 or D12 is set.

9.1.3. BITE Config Pointer

This register shall point to a table of data for use in BITE 1,2,3,4 commands. The data in this table would normally be known constant values. This table is supplied to allow these known constants to be set to illegal values. The contents of this table shall be as follows:

Offset	Register Name	Description
0x00	BITE_1_BSR	Value to update the BSR on a BITE 1 command
0x02	BITE_2_BSR	Value to update the BSR on a BITE 2 command
0x04	BITE_2_W1	BITE 2 command storage word 1
0x06	BITE_2_W2	BITE 2 command storage word 2
0x08	BITE_2_W3	BITE 2 command storage word 3
0x0A	BITE_2_W4	BITE 2 command storage word 4
0x0C	BITE_2_W5	BITE 2 command storage word 5
0x0E	BITE_3_BSR	Value to update the BSR on a BITE 3 command
0x10	BITE_4_ DI_00	BITE 4 DI channel 0 1st word (normally 0x0FF0)
0x12	BITE_4_ DI_01	BITE 4 DI channel 0 2nd word (normally 0xF00F)
0x14	BITE_4_ DI_10	BITE 4 DI channel 1 1st word (normally 0x0F0F)
0x16	BITE_4_ DI_11	BITE 4 DI channel 1 2nd word (normally 0xF0F0)
0x18	BITE_4_ DI_20	BITE 4 DI channel 2 1st word (normally 0x0FF0)
0x1A	BITE_4_ DI_21	BITE 4 DI channel 2 2nd word (normally 0x0F0F)
0x1C	BITE_4_ SIO_0	BITE 4 SIO 1st word (normally 0xAAAA)
0x1E	BITE_4_ SIO_1	BITE 4 SIO 2nd word (normally 0x5555)
0x20	BITE_4_TAC_06	BITE 4 TAC channel 0-6 value (normally 0xA9AA)
0x22	BITE_4_TAC_7	BITE 4 TAC channel 7 mask (normally 0xA1AA)
0x24	BITE_4 _PLUS	BITE 4 10-bit +VE constant
0x26	BITE_4 _MINUS	BITE 4 10-bit -VE constant
0x28	RCW_WORD	If D0=1, D15-D2 will be returned for a RCW command

9.1.4. PROM Pointer

Each RT shall have two PROMS, a LOCAL PROM and the ACTUAL PROM. The value of the PROM pointer shall define the address of the LOCAL PROM in the bottom 0-0xFFFF of the board. The ACTUAL PROM will reside at this address + 0x10000. The LOCAL PROM shall have a format that is compatible with the SBIIB architecture. The ACTUAL PROM shall be as would be expected in a real MDM. It is the task of the user to ensure that the two PROMS are correctly configured and are compatible with each other. Should the PROM require changing in real time, it is suggested that the users make copies of both PROMS, do the change in the copies and then change the pointer in the SIM table.

LOCAL PROM format

0-15:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
P	0	0	0	0	0	0	0	0	0	0	0	0	I	I	I

P: Parity of ACTUAL PROM location (1 = odd parity)

I: IOM Type -
- 000 No IOM
- 001 DI
- 010 AI16
- 011 AI32
- 100 DO
- 101 SIO
- 110 TAC
- 111 AO

16-511:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
P	M	M	S	S	S	S	S	N	N	N	N	I	I	I	I

P: Parity of ACTUAL PROM location (1 = odd parity)
M: Mode - 00 Output to IOM
01 Input to IOM
10 Return BITE Status Register (BSR)
11 Execute BITE 4 test
S: Start channel address
N: Number of channels
I: IOM address

9.1.5. CHANNEL Table Pointer HI/LO

The CHANNEL Table Pointer HI/LO registers define a 32 bit address for the RT channel table. The format of this table shall be as follows:

Table offset	Description
+0x0000	IOM_00 channel 0
|	|
+0x003E	IOM_00 channel 31
|	|
|	|
+0x03C0	IOM_15 channel 0
|	|
+0x03FE	IOM_15 channel 31

If an IOM is defined as type SIO then the first 8 channel values will be used as 4 x 32 bit addresses of the 0 to 3 channel SIO RX/TX buffers. For example, if IOM_01 is defined as type SIO and the channel number is 2 then:

IOM_00 Channel_4,Channel_5 will be used as a 32 bit address of the SIO RX/TX buffers.

Each SIO RX/TX buffer will be as follows:

Offset	Description
+0x0000	RX buffer word 0
|	|
+0x003E	RX buffer word 31
+0x0040	TX buffer word 0
|	|
+0x007E	TX buffer word 31

Note:

- All channel tables **must** reside on an even 1Kbyte boundary
- All SIO RX/TX buffers **must** reside on an even 128byte boundary

9.1.6. TX Error Injection Word/Number

Each message type that requires a response from the MDM MRT has a TX error injections word and TX error injection word number associated with it. These message types are:

RCP: Return contents of PROM command
EPS: Execute PROM sequence command
BT2: BITE 2 command
BT4: BITE 4 command
IFI: Input from IOM command
RBC: Return BSR command
RCW: Return Command Word command

The format of the TX error injection words is as follows:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	E7	E6	E5	E4	E3	E2	E1	E0	I	I	I	I	I	I

E7	**E6**	**E5**	**E4**	**E3**	**E2**	**E1**	**E0**	
0	0	0	0	0	0	0	0	Parity Error
0	0	0	0	0	0	0	1	Sync Error
0	0	0	0	0	0	1	0	Manchester Error
0	0	0	0	0	0	1	1	Bit Count Error
0	0	0	0	0	1	0	0	No Error Injection
0	0	0	0	1	1	0	0	No Response
0	0	0	1	0	1	0	0	+ Word Count Error
0	0	1	0	0	1	0	0	- Word Count Error
0	1	0	0	0	1	0	0	SEV Bit Error
1	0	0	0	0	1	0	0	RT Address Error

Parity Error: I = Don't Care
Sync Error: I = Pattern of the sync to TX in 6 segments
Manchester Error: I = Bit number in word for Manchester Error
Bit Count Error: I = Number of bits to TX
No Response: I = Don't Care
+ Word Count: I = Number of extra words to TX
- Word Count: I = Number of words to subtract from the correct TX word count
SEV Bit Error I = The 3 LSBs shall define the SEV bit pattern to TX
RT Address Error: I = The 5 LSBs shall define the RT address bits to TX

The format of the TX error injection word number is as follows:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	W	W	W	W	W	W	W	W	W	W

W: Word number in message for TX error injection. If W=0 the error will be injected in the first word transmitted.

Note:

- In the case of No Response, +Word Count and -Word Count errors the TX error injection word number is not relevant
- All E7-E0 values not defined are illegal and **must not be used**

9.1.7. Last Command HI/LO Value

These 6 locations will be updated with the time-stamp and value of the most recent valid command to this RT. The MSB of the Last CMND Value HGH will be set if the command was received on the secondary bus.

9.2. HI/LO Priority Message Queues

Both HI and LO priority queues are 512 bytes long. Each entry will be 4 words resulting in 64 entries before wrap-round. The format of the QUEUE entries is as follows:

1st word:

Command word of message (LS byte = most significant 8 bits).
If bit 15 is set, the command was received on the secondary bus.

2nd word:

Command word of message (least significant 16 bits).

3rd word:

Errors if any detected as follows:-

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	Ig	Bh	Ic	Id	Pp	Ta	Wc	Sy	Py	Mn	Lg	Sh

Ig: 1 = Illegal Command Code
Bh: 1 = Simultaneous command detected on other bus
Ic: 1 = Illegal channel
Id: 1 = Illegal data word (status bits <> 101)
Pp: 1 = PROM parity error
Ta: 1 = Incorrect RT terminal address
Wc: 1 = Word-count error
Sy: 1 = Sync type error
Py: 1 = Parity error
Mn: 1 = Manchester encoding error
Lg: 1 = Long word error (too may bits)
Sh: 1 = Short word error (too few bits)

4th word:

Set to value 0xFFFF. This is for clearing by the user when the entry has been interrogated.

10. PRIMITIVE MODE

The PRM_MDE mode of operation allows data bus operations to be performed independent of any specific message format. This mode will transmit all bus words provided by the host CPU and will make all bus words received available to the host CPU. This mode supports both 28-bit and 44-bit word lengths.

10.1. Transmit/Receive Buffers

Both the TX and RX buffers are a linked list of buffers defining messages to be transmitted and areas for receiving data. The value of the UPLINK queue pointer in the base registers shall point to the first Transmit Buffer to be used. The value of the DOWNLINK queue pointer in the base registers shall point to the first Receive Buffer to be used. Each individual transmit and receive buffer will point to a new buffer creating a linked list. The format of these buffers is as follows:

Buffer offset	**Register Name**
+0x0000	Control/Status Register
+0x0002	Buffer ID register
+0x0004	Next Address Register
+0x0006	Word Count Register
+0x0008	Buffer Size Register
+0x000A	TX Error injection Register
+0x000C	TX Error Word Number Register
+0x000E	Selective Data Pattern HGH
+0x0010	Selective Data Pattern MID
+0x0012	Selective Data Pattern LOW
+0x0014	Selective Data Mask HGH
+0x0016	Selective Data Mask MID
+0x0018	Selective Data Mask LOW
+0x001A	Time-stamp value HGH
+0x001C	Time-stamp value MID
+0x001E	Time-stamp value LOW
+0x0020	Time-stamp value TICKS
+0x0022	First Data word HGH(most significant 8 bits and errors)
+0x0024	First Data word MID (next 16 bits)
+0x0026	First Data word LOW (last 16 bits)
|	|
|	|
+NNNN	Last Data word HGH(most significant 8 bits and errors)
+NNNN	Last Data word MID (next 16 bits)
+NNNN	Last Data word LOW (last 16 bits)

Note:
All TX and RX buffers **must** reside in the bottom 64Kbytes of the card.

10.1.1. Control/Status Register

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
En	Rs	Bs	Iq	Tg	By	0	0	0	0	0	0	0	0	0	Ov

En: If the buffer is the next TX buffer, the buffer will not be transmitted until the user sets this bit. If the buffer is the next RX buffer, all RX of data will be inhibited until this bit is set.

Rs: If this bit is set, the 'En' bit will be automatically cleared after the TX/RX message is completed.

Bs: For TX buffers this shall define the bus for the message. 0 = PRI, 1 = SEC.

Iq: If set, an interrupt will be generated when the buffer is transmitted or the RX message has been stored.

Tg: If this bit is set, a 1uS pulse will be output on TRIGGER 3 on completion of the TX/RX message.

By: The card will set this BUSY bit when the buffer is being transmitted or data is being stored in it. On completion, this bit will be cleared.

Ov: This bit will be set by the card if the RX data count exceeded the value in the Buffer Size Register.

10.1.2. Buffer ID Register

This register shall be set to a unique non-zero value defining the ID of the buffer. If an interrupt is requested, this value will be pushed to the appropriate HI/LO priority queue.

10.1.3. Next Address Register

This defines the address of the next RX/TX buffer to be used once this buffer has been accessed. This feature is used where the user wishes to create a linked list of buffers. If only one buffer is required then this value should be set to the address of its own buffer.

10.1.4. Word Count Register

If a TX buffer, this shall be set to the number of words to be transmitted. If an RX buffer, this register will report the number of bus words saved in the buffer.

10.1.5. Buffer Size Register

This shall define the maximum number of words that can be stored in the buffer. This is not applicable if the buffer is a TX type.

10.1.6. TX Error Injection and Word Number Register

These two registers shall define the error injection for the TX message as follows:

TX Error Word

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X	X	X	X	X	X	X	NE	T1	T0	I	I	I	I	I	I

NE = Error enable/disable, 0 = Enable.

T1	T0	
0	0	Parity Error
0	1	Sync Error
1	0	Manchester Error
1	1	Bit count Error

I = Error Information

For Parity Error	-- I = "don't care".
For Sync Error	-- I = pattern of the sync to TX in 6 segments.
For Man Error	-- I = bit number in word for Manchester Error.
For Bit Count Error	-- I = number of bits to TX.

TX Error Word Number

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	W	W	W	W	W	W	W	W	W	W

W = Word number in message for TX error injection.

If W = 0 the error will be injected in the 1st word transmitted.

10.1.7. Selective Data Pattern HGH/MID/LOW Register

These three registers shall define the bit pattern requirement of a data word for storing in the buffer. If the card is running in 24-bit mode, the LOW register is not relevant.

10.1.8. Selective Data Mask HGH/MID/LOW Register

These three registers shall define which bits of the Bit Pattern Registers are "don't care" such that they play no part in the selective data test condition. If a bit is set in this register, the corresponding bit in the Bit Pattern Register will become a "don't care" condition.

40-bit mode example:
Bit Mask HGH = 0x00FF
Bit Mask MID = 0xFFFF
Bit Mask LOW = 0xFFFF …….. Save any word.

Note: If the card is running in 24-bit mode, the LOW mask value **must** be set to 0xFFFF.

10.1.9. Time-stamp HGH/MID/LOW/TICKS

These 4 words shall be the 64-bit value of the local clock when the message started.

10.1.10. Data word HGH

RX buffers:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Bs	0	0	Sy	Py	Mn	Lg	Sh	D	D	D	D	D	D	D	D

For RX buffers the encoding errors and SYNC type will be reported as follows:

Bs = Bus data received on. 0 = PRI, 1 = SEC.
Sy = Sync type. 1 = Command Sync
Py = 1 = Parity error
Mn = 1 = Manchester error
Lg = 1 = Long word (too many bits)
Sh = 1 = Short word (too few bits)
D = Most significant 8 bits of word

TX buffers:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	Sy	0	0	0	0	0	0	D	D	D	D	D	D	D	D

Sy = If set in the first data word, the first data word will be transmitted with a command sync. This is only applicable to the first data word. All following data words will automatically be transmitted with a data sync.
D = Most significant 8 bits of word

10.1.11. Data word MID

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

24-bit mode:
D = Least significant 16 bits of word
40-bit mode:
D = Next 16 bits of word

10.1.12. Data word LOW

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

24-bit mode:
D = Don’t care
40-bit mode:
D = Least significant 16 bits of word

10.2. HI/LO Priority Message Queues

Both HI and LO priority queues are 512 bytes long. If an interrupt is requested for a TX buffer, the buffer ID word will be pushed to the HI priority queue after the last word is transmitted. If an interrupt is requested for an RX buffer, the buffer ID word will be pushed to the LO priority queue after the last word is received.

11. CAL MDE MODE

The CAL_MDE mode of operation is a special mode of operation used for calibration and test purposes. This mode can only be entered when the card is in LDB_BCT mode and is not intended for normal applications. This mode allows the user to program the serial EEPROM that contains all the configuration data for the card. It is **strongly** advised **not** to put the card into this mode unless absolutely necessary. Once the card is put into this mode the card can only be returned to normal operation by asserting a reset.

Once in this mode the user can carry out a number of operations on the card. The on-board processor will poll the command register (base+0x0004) for a valid command code. Once a valid code is detected, the processor will use a number of the following words as information related to this command. It is important that this further information be put in place prior to writing the command. Once the command has been completed, the processor will clear the command word at base+0x0004. There are no interrupts in this mode. All operations must be done on a polling basis using the command register.

11.1. Transmit DAC Level (0x5551)

The code 0x5551 will command the processor to transmit a 28 bit word on all four buses approximately every 13mS. This word will comprise of a data sync, 24 manchester '0' bits and a parity bit of '1'. The amplitude of this word shall be defined by the word following the 0x5551 command word at address base+0x0006. The 8-bit TX DAC for the card will be loaded with the LS byte of this word.

11.2. Write Value to EEPROM (0x5552)

The code 0x5552 will command the processor to write a value to the configuration serial EEPROM. The word following the 0x5552 command shall be set to the required word address within the EEPROM and the next location shall define the value to be written.

11.3. Read Value from EEPROM (0x5553)

The code 0x5553 will command the processor to read a value from the configuration serial EEPROM. The word following the 0x5552 command shall be set to the required word address within the EEPROM and, on completion, the next location will contain the value read from the EEPROM.

11.4. Transmit Pattern (0x5554)

The code 0x5554 will command the processor to transmit a data pattern simultaneously on all four buses. The pattern, error injection, frequency etc. shall be defined by the following locations:

Base+0x0006	TX ERRORS
Base+0x0008	Pattern HI
Base+0x000A	Pattern LO
Base+0x000C	Gap Time
Base+0x000E	TX Count
Base+0x0010	Amplitude

TX ERRORS:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X	X	X	X	X	X	X	NE	T1	T0	I	I	I	I	I	I

NE = Error enable/disable, 0 = Enable.

T1	T0	
0	0	Parity Error
0	1	Sync Error
1	0	Manchester Error
1	1	Bit count Error

I = Error Information

For Parity Error	-- I = "don't care".
For Sync Error	-- I = pattern of the sync to TX in 6 segments.
For Man Error	-- I = bit number in word for Manchester Error.
For Bit Count Error	-- I = number of bits to TX.

Warning: When transmitting **very** short words, the result can sometimes be unpredictable.

PATTERN HI:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	S	0	0	0	0	0	0	P23	P22	P21	P20	P19	P18	P17	P16

P23-P16:	Most significant 8 bits of pattern.
S:	Set to 1 if TX is to be on Secondary Bus.

PATTERN LO:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P01	P00

P15-P00: Least significant 16 bits of pattern.

GAP TIME:

This location shall contain the gap in microseconds between each consecutive word transmitted.

TX COUNT:

This location shall define the number of words to be transmitted before stopping. If this value is set to 0, the card will transmit continually until a new command is entered.

AMPLITUDE:

The least significant byte of this location shall define the value to be loaded into the 8-bit TX DAC prior to transmission.