Module CC9P9360_2

Users Manual

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Release of Document:	January 17, 2006
Filename:	UM_Module_CC9P9360_2.doc
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Program Version	

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1. Revision History

2005-03-09 (V1.00) KR: Initial Version, derived from A9M9360_1 spec

2005-04-05 (V1.00) KR: Transfer to standard document format

2005-05-30 (V1.00) KR: Migration to A9M9360_2

2. General

A9M9360 Module is a member of the ModARM9 family with a NetSilicon NS9360 CPU. The ModARM9 family includes several modules with the same size, connectors and a set of common pins and functions (see “Arm9 module pinning table.xls”) with CPUs from different manufacturers. There are two modules with Netsilicon CPUs in this family available: A9M9750 and A9M9360.

2.1. Common Features

Below are the common features of this module, which will be covered in further detail later in the document.

- ARM9 core with MMU
- Size 60mm x 44mm with 240-pin connectors
- SDRAM 16MB – 256MB
- NAND Flash 32MB – 256MB
- 4 Serial RS232 interfaces
- Host and device USB interface, USB2.0 compliant
- 10/100Mbps Ethernet interface
- I²C interface, 100KHz and 400KHz
- SPI interfaces
- JTAG interface

2.2. Differences between A9M9750 and A9M9360 Modules

Netsilicon CPU NS9360 is a low cost version of the NS9750. It has many features from the NS9750 including CPU core and most peripherals.

Differences:

1. CPU clock is 100..177MHz (NS9750 up to 200MHz)

2. Two SDRAM banks allowing up to 2 * 256MByte memory.

3. No PCI (CardBus) on A9M9360. All pins used by PCI on A9M9750 are unconnected on A9M9360.

4. NS9360 has 73 GPIOs multiplexed with other functions (NS9750 has 50). The same number of GPIOs are available on the A9M9360 connectors as the A9M9750 provides (GPIO0..48). Additional GPIO66..72 are available too, but have non GPIO function names (A22..A25, I2C_SCL, I2C_SDA, WAIT#) and will be used normally in this function.

5. LCD function limited to 18bit LCD data. LCD adapters with 18bit TFT LCD used for A9M9750 will run with A9M9360 too.

6. Dedicated I2C pins IIC_SDA and IIC_SCK on A9M9750 can be GPIO70,71 or A26, A27 on A9M9360 also.

7. 8 timers on A9M9360 (16 on A9M9750).

8. 4 PWM channels added on A9M9360 (each uses 2 timers).

9. Additional USB device modul on A9M9360, needs external USB PHY connected to GPIO42..48.

2.3. Existing Variants of A9M9360_1

Current state (02/2005):

1. 0381: CPU speed 177MHz, 16MByte SDRAM, 32MByte NAND flash, 8KByte SPI boot EEPROM, 8KByte I2C EEPROM, RTC, 0..70°

2. 0382: CPU speed 177MHz, 32MByte SDRAM, 32MByte NAND flash, 8KByte SPI boot EEPROM, 8KByte I2C EEPROM, RTC, 0..70°

3. 0383: CPU speed 177MHz, 64MByte SDRAM, 64MByte NAND flash, 8KByte SPI boot EEPROM, 8KByte I2C EEPROM, RTC, 0..70°

Due to a bug in the NS9360 CPU the module generation A9M9360_1 is stopped. A safe start in SPI boot mode needs a hardware workaround realised in A9M9360_2

2.4. Existing Variants of A9M9360_2

Current state (05/2005):

4. 0381: CPU speed 177MHz, 16MByte SDRAM, 32MByte NAND flash, 8KByte SPI boot EEPROM, 8KByte I2C EEPROM, RTC, 0..70°

5. 0382: CPU speed 177MHz, 32MByte SDRAM, 32MByte NAND flash, 8KByte SPI boot EEPROM, 8KByte I2C EEPROM, RTC, 0..70°

6. 0383: CPU speed 177MHz, 64MByte SDRAM, 64MByte NAND flash, 8KByte SPI boot EEPROM, 8KByte I2C EEPROM, RTC, 0..70°

3. Detailed Description

3.1. Size 60 x 44 mm

The A9M9360 module has a size of 60 X 44 mm.

3.2. 2 x 120-pin Connectors

Two 120-pin connectors on the long side of the module allow accessing most signals of the NetSilicon NS9360 CPU. An optional extension with another two 60-pin connectors is planned. This will extend the length of the module from 60mm to approximately 95mm.

Pin-compatible in power supply and main port functions to other ModARM9 modules.

3.3. NS9360 CPU

For details see “9360_HardwareReferenceManual.pdf” from NetSilicon. The CPU is offered in three speed and temperature variants:

- 177MHz: 0..70°C
- 155MHz: -40..+85°C
- 103MHz: 0..70°C

3.4. Configuration Pins CPU

Several pins allow configuration of the CPU before booting. CPU pins have weak pull ups (value range is 15..300K) for a default configuration. Most pins do not have configuration options, some are connected for internal configuration on the module. 32 of the 73 GPIO pins allow user specific configurations. They are latched in the GEN_ID register (address 0xA0900210) 5 clock cycles after the rising edge of RESET#. Important configuration pins are protected, i. e. not accessible externally until strapping information configured on module is latched. For details see Spec_A9M9360_2.pdf.

Normally the hardware module configuration needs never to be changed by the client; wrong configuration can make the module unbootable.

Module configuration (details see “specification_A9M9360_2.pdf”:

- little endian mode selected
- PLL active (PLL bypassed not allowed)
- PLL_FS divider set to 2
- PLL_ND multiplier set to 24 (177MHz), 21 (154MHz) or 14 (103MHz)
- Boot from SPI EEPROM (spi.bin)

3.5. Configuration Pins Module

Module configuration pins change either hardware configurations on the module (HCONF0..3) or they are user specific and can be read in the GEN_ID register (SCONF0..3).

Signal name	Function	PU/PD	external pin name	Comment
DEBUG_EN#	CPU Mode Select 0 = Disconnects TRST# and PWRGOOD for JTAG and Boundary scan debug mode 1 = TRST# and PWRGOOD connected for normal mode (default)	PU 10K	HCONF0	
FWP#	internal NAND flash write protect 0 = write protect active 1 = no write protect	PU 10K	HCONF1	
OCD_EN#	JTAG / Boundary Scan function selection 0 = ARM Debug Mode, BISTEN# set to high 1 = Boundary Scan Mode, BISTEN# set to low (default)	PU 10K	HCONF2	Select JTAG mode, DEBUG_EN# has to be low too
	unused		HCONF3	no function, n.c.
GPIO38	User defined software configuration pin, can be read in GEN ID register bit 28, default high		SCONF0	read Bit 28 GEN_ID
GPIO39	User defined software configuration pin, can be read in GEN ID register bit 29, default high		SCONF1	read Bit 29 GEN_ID
GPIO40	User defined software configuration pin, can be read in GEN ID register bit 30, default high		SCONF2	read Bit 30 GEN_ID
GPIO41	User defined software configuration pin, can be read in GEN ID register bit 31, default high		SCONF3	read Bit 31 GEN_ID

Recommended Combinations of DEBUG_EN# and OCD_EN#:

HCONF0	HCONF2	Mode	Comments
OFF	OFF	Normal mode	ok
ON	OFF	Debug mode	ok

OFF	ON	not recommended, may hang	avoid
ON	ON	OCD mode	ok

3.6. Clock Generation

Summary Clock Frequencies on 177MHz Module:

Clock Tape	Settings, Result
Crystal	29,4912MHz
PLL_ND(4:0), PLL Multiplier	b10010, d24, CPU PLL active
PLL_FS(1:0), PLL divider	b11, d2, CPU PLL active
PLL_IS(1:0), value	b11, ND16..31, CPU PLL active
resulting PLL clock	353,8944 MHz
CPU clock	176,9472 MHz
AHB, SDRAM and external clock	88,4736 MHz
BCLK clock	44,2368 MHz
UART Baud Rate Clock BBus	44,2368 MHz
LCD clock	88,4736MHz, 44,2368MHz, 22,1184MHz or 11,0592MHz

By writing in the NDSW, CPCC, FSEL and PLLSW fields of the SCON_PLLCR register the CPU speed can be changed. IMPORTANT: Changing PLL parameters ends with a 4 ms RESET to allow changed PLL to stabilize. Applications using this feature have to discriminate between cold start and warm start.

3.7. Boot Process

A9M9360 modules are preconfigured to boot with SPI channel B from a serial SPI EEPROM containing memory controller setup for SDRAM bank 0 and an initial boot program that moves the boot loading program from NAND flash to SDRAM bank 0 and starts it.

The serial SPI EEPROM has a size of 8KByte.

3.8. Chip Selects, Memory Map

NS9360 CPU provides 8 chip selects divided in 4 channels for dynamic RAMs and 4 static chip selects. Every chip select has a 256MB range. Below the whole memory map of the NS9360 chip:

Name	Pin	Address Range	Size [Mbyte]	Usage	Comments
SDM_CS0#	B4	0x00000000.. 0x0FFFFFFF	256	SDRAM bank 0	1st bank on module
SDM_CS1#	A3	0x10000000.. 0x1FFFFFFF	256	SDRAM bank 1	2nd bank on module
SDM_CS2#	D5	0x20000000.. 0x2FFFFFFF	256	n. c.	
SDM_CS3#	C4	0x30000000.. 0x3FFFFFFF	256	n. c.	
EXT_CS0#	B3	0x40000000.. 0x4FFFFFFF	256	external, CS0#	
EXT_CS1#	C1	0x50000000.. 0x5FFFFFFF	256	NAND-Flash	Program Memory
EXT_CS2#	D2	0x60000000.. 0x6FFFFFFF	256	external, CS2#	
EXT_CS3#	E3	0x70000000.. 0x7FFFFFFF	256	external, CS3#	
Reserved	-	0x80000000.. 0x8FFFFFFF	256		
BBus	-	0x90000000.. 0x9FFFFFFF	256	BBus memory	
Reserved	-	0xA0000000.. 0xA03FFFFF	4		
Bridge	-	0xA0400000.. 0xA04FFFFF	1	BBus to AHB Bridge	
reserved	-	0xA0500000.. 0xA05FFFFF	1	reserved	
Ethernet	-	0xA0600000.. 0xA06FFFFF	1	Ethernet Communication Module	
Memory	-	0xA0700000.. 0xA07FFFFF	1	Memory Controller	
LCD	-	0xA0800000.. 0xA08FFFFF	1	LCD Controller	
System	-	0xA0900000.. 0xA09FFFFF	1	System Control Module	
reserved	-	0XA0A00000. .0xFFFFFFFF	1526	reserved	

3.9. NAND Flash

A9M9360 has 32Mx8, 64Mx8 or 128Mx8 NAND Flash onboard. Optionally greater sizes can be populated (depending on availability). The NS9360 limits the address range of a single chip select to 256MByte, but this is not relevant for NAND Flash, as the interface to the NAND flash needs always 32 kByte here due to usage of A13, 14 for address and command control.

The NAND flash is accessed with EXT_CS1#. The chip can be write protected externally with the signal FWP#.

3.10. 1..2 * 16/64 MBytes SDRAM

Two SDRAM banks are available on the module. They are connected to CS4# (D_CS0#) and CS5# (D_CS1#). CS6# (D_CS2#) and CS7# (D_CS3#) are lost. The module does not provide external SDRAM connection.

A9M9360 has one or two 1X4MX32, 2X4MX32 or 4X4MX32 SDRAM onboard. The highest address connected is A12. Range of chip select is 256M.

BA0, 1 are connected to A13, 14. The SDRAM controller connects the right address line to allow a gapless memory space at different SDRAM sizes.

3.11. Usage of 2nd SDRAM bank

The SPI loader used on A9M9360 module initializes only SDRAM bank 0 with SD_CS0. When the system is running from SDRAM, the 2nd bank cannot be initialized, because it uses the same registers for different parameters as the running bank. Especially the Dynamic Memory Control Register has to be changed from normal to set mode command while starting the 2nd bank. So the initialization routine has to be run either from NOR flash (if booting with flash) or from another memory place. A good choice may be the ethernet TX buffer descriptor RAM starting at address 0xA0601000 with a space of 256 * 32bit words. Before using this RAM it must be enabled by setting bit 23 of the Ethernet General Control register 1 to high.

3.12. 73 GPIO Pins (multiplexed with other Functions)

NS9360 has 73 GPIO pins, 23 more than NS9750. All pins are multiplexed with other functions (UART, SPI, USB, Ethernet, DMA, parallel port IEEE1284, IIC port, LCD port, timers, interrupt inputs, some memory bus address and control pins). Using a pin as GPIO means always to give up another functionality. GPIO0..48, GPIO66..72 are accessible on the connectors. GPIO13 is used for RTC interrupt on module (allows sharing with open drain ORing). GPIO49..65 are used on the module and not external accessible. All GPIOs are set to GPIO input function after RESET. Usage in another function needs configuring the GPIO registers at start up.

Port Name, Function 03 (default at power up)	**Alternate Function 00, UART**	**Alternate Function 00, misc.**	**Alternate Function 01**	**Alternate Function 02**	**Module on DEV Board default usage**
GPIO0	TXDB	SPI_Boot_DO SPIB_DO	DMA0 DONE dupe	Timer 1 dupe	TXDB, SPI_Boot_DO or external SPIB_DO
GPIO1	RXDB	SPI_Boot_DI SPIB_DI	DMA0 REQ. Dupe	EIRQ0	RXDB, SPI_Boot_DI or external SPIB_DI
GPIO2	RTSB#		Timer 0	DMA1 ACK	RTSB#, DMA
GPIO3	CTSB#		1284 ACK#	DMA0 REQ	CTSB#, DMA
GPIO4	DTRB#		1284 BUSY	DMA0 DONE	DTRB#
GPIO5	DSRB#		1284 ERR	DMA0 ACK	DSRB#, DMA
GPIO6	RIB#	SPI_Boot_CLK SPIB_CLK, ext RXCLK_A	1284 P_JAM	Timer 7 dupe	RIB#, SPI_Boot_CLK or external SPIB_CLK
GPIO7	DCDB#	SPI Boot CE# SPIB_CE#, ext TXCLK_A	DMA0 Ack dupe	EIRQ1	DCDB#, SPI_Boot_CE# or external SPIB_CE#
GPIO8	TXDA	SPIA_DO	Reserved	Reserved	TXDA, SPI A
GPIO9	RXDA	SPIA_ DI	Reserved	Reserved	RXDB, SPI A
GPIO10	RTSA#t		Reserved	**PWM0 dupe**	GPIO10
GPIO11	CTSA#		EIRQ2 dupe	Timer 0 dupe	GPIO11
GPIO12	DTRA#		Reserved	**PWM1 dupe**	GPIO12
GPIO13	DSRA#		EIRQ0 dupe	**PWM2 dupe**	EIRQ0 connected to RTC_INT# on module
GPIO14	RIA#	SPIA_CLK,	Timer 1	**PWM3**	SPI A

Port Name, Function 03 (default at power up)	Alternate Function 00, UART	Alternate Function 00, misc.	Alternate Function 01	Alternate Function 02	Module on DEV Board default usage
		ext RXCLK_B		**dupe**	
GPIO15	DCDA#	SPIA_EN#, ext TXCLK_B	Timer 2	**LCD_CLKIN**	SPI A
GPIO16		USB Overcurrent	1284 P_JAM dupe	**Reserved**	USB_OVCUR
GPIO17		USB Power Relay	Reserved	Reserved	USB_PREL
GPIO18		Ethernet CAM Reject	LCD PWREN	EIRQ3 dupe	LCD
GPIO19		Ethernet CAM Request	LCD HSYNC	DMA1 ACK dupe	LCD
GPIO20	DTRC#		LCD CLK	Reserved	LCD
GPIO21	DSRC#		LCD VFSYNC	Reserved	LCD
GPIO22	RIC#	SPIC_CLK, ext RXCLK_C	LCD BIAS_D_EN	Reserved	LCD
GPIO23	DCDC#	SPIC_EN#, ext TXCLK_C	LCD LINE_END	**Reserved**	LCD
GPIO24	DTRD#		LCDD0	Reserved	LCD
GPIO25	DSRD#		LCDD1	**Reserved**	LCD
GPIO26	RID#	SPID_CLK, ext RXCLK_D	LCDD2	Timer 3	LCD
GPIO27	DCDD#	SPID_EN#, ext TXCLK_D	LCDD3	Timer 4	LCD
GPIO28		EIRQ 1 dupe	LCDD4	LCDD8 dupe	LCD
GPIO29		Timer 5	LCDD5	LCDD9 dupe	LCD
GPIO30		Timer 6	LCDD6	LCDD10 dupe	LCD
GPIO31		Timer 7	LCDD7	LCDD11 dupe	LCD
GPIO32		EIRQ 2	1284 D1	LCDD8	LCD
GPIO33		**Reserved**	1284 D2	LCDD9	LCD
GPIO34		**IIC_SCL**	1284 D3	LCDD10	LCD
GPIO35		**IIC_SDA**	1284 D4	LCDD11	LCD
GPIO36		**PWM0**	1284 D5	LCDD12	LCD
GPIO37		**PWM1**	1284 D6	LCDD13	LCD

Port Name, Function 03 (default at power up)	Alternate Function 00, UART	Alternate Function 00, misc.	Alternate Function 01	Alternate Function 02	Module on DEV Board default usage
GPIO38		**PWM2**	1284 D7	LCDD14	LCD
GPIO39		**PWM3**	1284 D8	LCDD15	LCD
GPIO40	TXDC	SPIC_DO	IRQ3	LCDD16	LCD
GPIO41	RXDC	SPIC_DI	**Reserved**	LCDD17	LCD
GPIO42	RTSC#		**Reserved**	**USB_PHY_D+**	**USB_EXTPHY_D+**
GPIO43	CTSC#		**1284 DIRCON**	**USB_PHY_D-**	**USB_EXTPHY_D-**
GPIO44	TXDD	SPID_DO	**1284 SELECT**	**USB_PHY_TXOUT_EN**	**USB_EXTPHY_OE#**
GPIO45	RXDD	SPID_DI	1284 STRB	**USB_PHY_RXD**	**USB_EXTPHY_RXD**
GPIO46	RTSD#		1284 ALFD	**USB_PHY_RXD+**	GPIO46
GPIO47	CTSD#		1284 INIT	**USB_PHY_RXD-**	GPIO47 drives DEBUG-LED
GPIO48		**USB_PHY_SUSP**	1284 P_SEL	DMA1 REQ	**USB_EXTPHY_SUSP**
GPIO49		**USB_PHY_SPEED**	1284 P_LOG	DMA1 DONE	R/B# NAND-Flash (GPIO) control on module
GPIO50		**MII_MDIO**	**Reserved**	**USB_PHY_D+ dupe**	**MII_MDIO**
GPIO51		**MII_RXDV**	**Reserved**	**USB_PHY_D- dupe**	**MII_RXDV**
GPIO52		**MII_RXER**	**Reserved**	**USB_PHY_TXOUT_EN**	**MII_RXER**
GPIO53		**MII_RXD0**	**Reserved**	**USB_PHY_RXD dupe**	**MII_RXD0**
GPIO54		**MII_RXD1**	**Reserved**	**USB_PHY_SUSP dupe**	**MII_RXD1**
GPIO55		**MII_RXD2**	**Reserved**	**USB_PHY_SPEED dupe**	**MII_RXD2**
GPIO56		**MII_RXD3**	**Reserved**	**USB_PHY_RXD+ dupe**	**MII_RXD3**
GPIO57		**MII_TXEN**	**Reserved**	**USB_PHY_RXD- dupe**	**MII_TXEN**
GPIO58		**MII_TXER**	**Reserved**	**Reserved**	**MII_TXER**
GPIO59		**MII_TXD0**	**Reserved**	**Reserved**	**MII_TXD0**

Port Name, Function 03 (default at power up)	Alternate Function 00, UART	Alternate Function 00, misc.	Alternate Function 01	Alternate Function 02	Module on DEV Board default usage
GPIO60		MII_TXD1	Reserved	Reserved	MII_TXD1
GPIO61		MII_TXD2	Reserved	Reserved	MII_TXD2
GPIO62		MII_TXD3	Reserved	Reserved	MII_TXD3
GPIO63		MII_COL	Reserved	Reserved	MII_COL
GPIO64		MII_CRS	Reserved	Reserved	MII_CRS
GPIO65		MII_PHY_INT	Reserved	Reserved	MII_MDINT#
GPIO66		A22	Reserved	Reserved	A22
GPIO67		A23	Reserved	Reserved	A23
GPIO68		A24	MCKE_0	IRQ0 dupe	A24
GPIO69		A25	MCKE_1	IRQ1 dupe	A25
GPIO70		A26	MCKE_2	IIC_SCL dupe	IIC_SCL
GPIO71		A27	MCKE_3	IIC_SDA dupe	IIC_SDA
GPIO72		TA_STB	Reserved	Reserved	ext WAIT

3.13. External Interrupts

4 external interrupts are multiplexed with other functions on the GPIO pins. Every interrupt is routed to two or three different GPIOs to increase the chance of using them without giving up another vital function.

External Interr.	1st Pos.	other functions 1st Pos.	2nd Pos. (dupe)	other functions 2nd Pos.
EIRQ0	GPIO1	RXDB, SPIBoot_DI + SPIB_DI, DMA0_REQ dupe	GPIO13	DSRA#, PWM2 dupe, **used on module for RTC interrupt**
EIRQ1	GPIO7	DCDB#, SPIBoot_CE# and SPIB_CE#, DMA0ACK dupe	GPIO28	LCD_D4, LCD_D8 dupe
EIRQ2	GPIO32	LCDD8, 1284_D0	GPIO11	CTSA#, Timer0 dupe
EIRQ3	GPIO40	TXDC, SPIC_DO, LCDD16	GPIO18	LCD_PWREN, ETH_CAMREJ

EIRQ0 and EIRQ1 have a third position on the NS9360:

EIRQ0 dupe: GPIO68, also A24

EIRQ1 dupe: GPIO69, also A25

Both address lines are routed to the modules connectors. If not used on the base board or application, the interrupts are available by changing the GPIO configuration

3.14. 10/100Mbps Ethernet Port

The 10/100Mbps Ethernet port of the NS9360 allows a glueless connection of a 3.3V MII or RMII PHY chip that generates the physical Ethernet signals.

The module has a MII PHY chip LXT972 in a LQFP-64 case on board. No transformer or Ethernet connector is on the module, these parts have to be provided by the base board. PHY clock of 25MHz is generated in the PHY chip with a 25MHz crystal.

3.15. USB 2.0 full and low speed Host and Device Controller

The USB section of the NS9360 CPU provides USB signals for a host and device channel. All external configuration for a USB host and/or a USB device interface has to be made on the base board. 48MHz USB clock is generated on the CPU with a 48MHz crystal in fundamental configuration.

The internal USB PHY in the NS9360 CPU can be used for the USB host or device channel (USB_INTPHY_DP, USB_INTPHY_DN).These signals are **not** 5V tolerant and have to be protected on the base board. A 2nd independant USB device channel is provided, when an external unidirectional or bidirectional PHY is connected to the USB device control signals GPIO42..45, 48. In this case the internal PHY has to be used in host mode.

3.16. UART Channels

Up to 4 UART channels with all handshake signals are provided (channels A=GPIO8..15, B=GPIO0..7, C=GPIO20..23 & GPIO40..43, D=GPIO24..27 & GPIO44..47). They can be used in asynchronous mode as UART. Baud rates are supported up to 1.8MHz in asynchronous mode.

3.17. SPI Channels

Four SPI channels are provided by the NS9360. Usage in master or slave mode is possible. SPI channel B (GPIO0,1,6,7) is connected to the serial 8Kx8 SPI EEPROM containing the boot program and the initial SDRAM parameters for booting via SPI when RESET# is asserted. External usage of this channel after boot at runtime is provided with additional hardware. The other SPI channels can be used free if not used in UART or LCD or USB mode or blocked by other GPIO usage.

3.18. Usage UART and SPI on A9M9360 Module

ARM9 modules have 2 serial ports A, B wired with at least TXD, RXD, RTS# and CTS# as common port lines.

The NS9360 chip allows only the usage of UART channels A,B for UART and/or SPI function, if the LCD function is used too. If all signals of the LCD function realised on the module are used, channel C for UART and/or SPI function is blocked. Usage USB with external PHY needs GPIOs providing SPI channel D.

3.19. Baudrate Table

Baud rate generators in the NS9360 have different clock sources selectable:

1. X1_SYS_OSC/M. It is the frequency of the input crystal divided by M. M depends on the multiplier settings PLL_ND of the PLL. M = 2 at PLL_ND >= 8 decimal (14.7456MHz with 29.4912MHz quartz), unusable for PLL_ND < 8 (baud clock instable and/or wrong frequency at CPU speeds < 58.9824MHz). Cannot be used with PLL bypassed.

2. BCLK. For 176,9472MHz CPU clock is BCLK = AHBCLK/2 = 44,2368MHz. Only internal source when PLL bypassed.

3. External receive clock from GPIO6, 14, 22, 26 pins.

4. External transmit clock from GPIO7, 15, 23, 27 pins.

Count values vs. Baud Rate Clock:

Baud Rate	N, X1_SYS/2 = 14.745600MHz, (Error) [%]	N, BCLK = 44,236800MHz, (Error) [%]	N, BCLK = 38,707200MHz, (Error) [%]	N, BCLK = 25,804800MHz, (Error) [%]
75	12287, (-)	-	32255, (-)	21503, (-)
150	6143, (-)	18431, (-)	16127, (-)	10751, (-)
300	3071, (-)	9215, (-)	8063, (-)	5375, (-)
600	1535, (-)	4607, (-)	4031, (-)	2687, (-)
1200	767, (-)	2303, (-)	2015, (-)	1343, (-)
2400	383, (-)	1151, (-)	1007, (-)	671, (-)
4800	191, (-)	575, (-)	503, (-)	335, (-)
7200	127, (-)	383, (-)	335, (-)	223, (-)
9600	95, (-)	287, (-)	251, (-)	167, (-)
14400	63, (-)	191, (-)	167, (-)	111, (-)
19200	47, (-)	143, (-)	125, (-)	83, (-)
28800	31, (-)	95, (-)	83, (-)	55, (-)
38400	23, (-)	71, (-)	62, (-)	41, (-)
57600	15, (-)	47, (-)	41, (-)	27, (-)
115200	7, (-)	23, (-)	20, (-)	13, (-)
230400	3, (-)	11, (-)		6, (-)
460800	1, (-)	5, (-)		
921600	0, (-)	2, (-)		
1843200	-	-		

A9M9360 module is using PLL, so modules with 177MHz, 155MHz and 103MHz will use the values from column 1 allowing baud rates from 75..921600Bd.

3.20. I²C Bus

This bus with the signals IIC_SCL (GPIO70 and muxed signal A26 lost) and IIC_SDA (GPIO71 and muxed signal A27 lost) is connected on the module to a serial EEPROM with I²C interface on device address 0xA0, 0xA1. Device address 0xD0, 0xD1 connects to an RTC on board. All other addresses can be used externally.

Due to a timing bug in the I²C state machine the maximum clock frequency in slow mode should be 50KHz and 200KHz in fast mode. Otherwise minimum setup time for the target can be violated (SDA changes after half low time of SCK instead of shortly after falling edge, so setup time for data is 2.5µs @ 100KHz and 612.5ns @ 400KHz).

Important: Use only 3.3V devices!

3.21. LCD Controller (STN & TFT)

An LCD interface for STN or TFT LCD's is provided with up to 18 data lines and 6 control lines. Usage for LCD disables serial ports C, D and most GPIOs.

The module provides the full LCD interface: 18 data lines LCCD0..17 (GPIO24..41) and 6 control lines GPIO18..23.

This interface allows connection of most TFT and STN monchrome and color LCDs. Details see NS9360 hardware user manual.

3.22. Serial EEPROM for storing Configuration Parameters

The nonvolatile storage of parameters like MAC address etc. is supported with a serial 8Kx8 EEPROM (24LC64 or similar in TSSOP8 case) connected to the I²C bus at device address 0xA0, 0xA1. Write protect WP and optional address lines A0, A1, A2 are grounded (some manufacturers leave these pins n. c.).

3.23. RTC

An RTC (MAXIM/DALLAS DS1337 in µSOP8 case) on the module is connected to the I²C bus (device address 0xD0, 0xD1). It has its own 32.768KHz clock crystal. Power is taken from +3.3V when provided, otherwise from V_{BAT} fed by an external battery. An interrupt line (GPIO13 configured as IRQ0) is connected to the RTC pin AINT# (open drain, default disabled); the connection can be opened by depopulating resistor R2.

3.24. JTAG, Boundary Scan

NS9360 support JTAG and boundary scan with the signals TCK, TMS, TDI, TDO and TRST#. The signal RTCK is not connected to external.

Selection between normal mode and debug mode is done with the external signal DEBUG_EN# (HCONF0). Selection between ARM debug mode and boundary scan mode is done with the signal OCD_EN# (HCONF2). See table below:

DEBUG_EN#	OCD_EN#	Mode	Comments
1	1	normal	
1	0	not recommended	Boundary Scan possible here too, but TRST# is connected with SRST#, system may hang
0	1	ARM debug	
0	0	Boundary Scan	

3.25. Single 3.3V Power Supply; Power Sequencing

The module has +3.3V_IN and VLIO (3.3V too for A9M9360) supply pins. Internal voltages: 1.5V core voltage with up to 400mA will be converted by a switching regulator from VLIO to keep losses small.

Power-up and power-down behaviour recommended by NetSilicon for the NS9360 (see 9360_power_sequencing.doc from NetSilicon) will be ensured by hardware. Due to generation of 1.5V from 3.3V_IN or VLIO with a step-down switching regulator the core voltage will rise later than the I/O voltage 3.3V_IN. A FET switch controls the switching of the I/O voltage 3.3V into the module.

Important: Every base board has to switch its 3.3V supply according to the module. Otherwise power sequencing on the module is influenced by backfeeding the module with 3.3V from the base board. The signal PWREN is provided for this purpose.

4. Bootloader

Every module is delivered with a bootloader (UBOOT) pre-installed in NAND Flash. The bootloader is capable of booting the Operating System from NAND Flash, via a serial port or via Ethernet. Parameters can be passed to the kernel from the bootloader.

5. Software

The ARM926 core in the NS9360 contains an MMU thus allowing Operating Systems such as Linux and Windows CE to be supported. Board Support Packages for Windows CE .net 4.2 and Linux, using kernel 2.6.x, are in development. Other Operating Systems can be supported on request**.**

5.1. Software Hints

This chapter just lists some problems, which occurred while bringing a NS9360 FORTH into life:

- UARTs: all four channels have their RESET bit set. Reset bits in SCON_MRES, other wise system hangs at access to UART registers.

- I2C: Reset bit in SCON_MRES. Same effect as mentioned for UARTs

- System Memory Chip Select X Memory Mask register: Bit 0 has to be 1, otherwise chip select is blocked. Is undocumented chip select enable, now documented.

- SDRAM bank 1 can be used if initilization is running not from SDRAM bank 0 (see chapter SDRAM).

6. Mechanics

The module size is defined to 60 x 44mm. Two holes, for M2 screws, catercornered, are provided to enable fixing of the module on the base board.

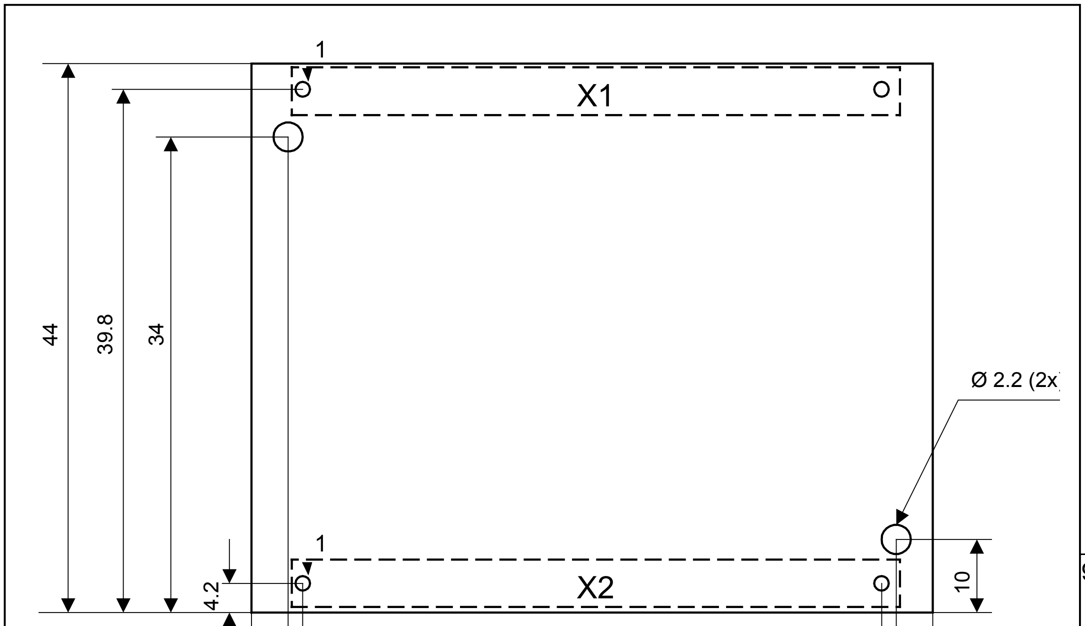
Two board-to-board connectors are used on the module. Depending on the counterpart on the base board, different distances between module and base board can be realized. The minimum distance is 5mm.

Therefore, the height of the parts mounted on the bottom side of the module should not exceed 2.5mm. The height of the parts mounted at the top side should not exceed 4.1mm.

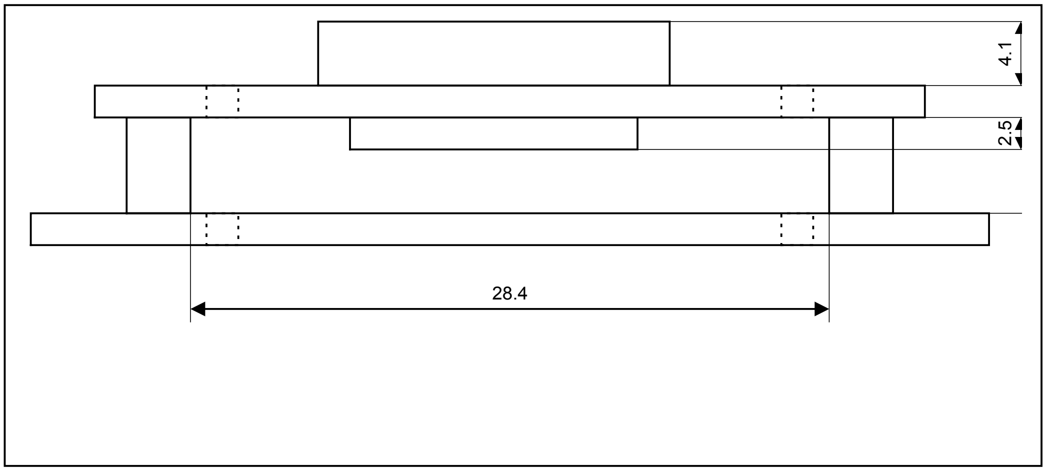
Board-to-Board Distance h	Module Connector X1, X2			
	No. of Pins	**Qty**	**Supplier**	**Order No.**
5 mm	120	2	AMP Berg	177983-5 61082-121000
6 mm				
7 mm				
8 mm				

Base Board Connector X1, X2		
No. Of Pins	**Supplier**	**Order No.**
120	AMP Berg	177984-5 61083-121000
120	AMP Berg	179029-5 61083-122000
120	AMP Berg	179030-5 61083-123000
120	AMP Berg	179031-5 61083-124000

Mechanical Drawing from TOP View:



Mechanical Drawing from Side View:



The size of h depends on the board-to-board connectors.

The size between the board-to-board connectors is measured from pad to pad.

6.1. Extended Module

For further modules in the ModARM9 family, it might be necessary to have some additional hardware placed on the module, which will need more signal lines connected between module and base board than currently available. To meet these future requirements, an extended board was defined, which has two additional board-to-board connectors with 60 pins each.

The size of the extended module is defined as 92 x 44mm. Two holes, for M2 screws, catercornered, are provided to enable fixing of the module on the base board.

Board-to-Board Distance h	Module Connector X3, X4			
	No. of Pins	**Qty**	**Supplier**	**Order No.**
5 mm	60	2	AMP Berg	177983-2 61082-061009
6 mm				
7 mm				
8 mm				

Base Board Connector X3, X4		
No. Of Pins	**Supplier**	**Order No.**
60	AMP Berg	177984-2 61083-061009
60	AMP Berg	179029-2 61083-062009
60	AMP Berg	179030-2 61083-063009
60	AMP Berg	179031-2 61083-064009

7. Known Faults and Limitations

7.1. SDRAM Clocks: Clockout1-3 not switchable

Only SDM_CLKOUT0 can be switched off by software. Switching SDM_CLKOUT1-3 does not work.

CPU fault, can be fixed only by NetSilicon.

Workaround: None; all 4 signals used on module with 2 SDRAM banks equipped.

7.2. I2C: Setup Time Data always half low time of Clock

I2C_SDA from NS9360 changes after half low time of I2C_SCL instead of short time after high to low edge of clock as other I2C devices do.

CPU fault, can be fixed only by NetSilicon.

Workaround: Use half clock speed, i. e. 50KHz in slow mode and 200KHz in fast mode.

7.3. SPI Boot System needs Hardware Workaround

The SPI EEPROM boot engine has a fault that prevents sometimes a proper setup of the SDRAM controller. A hardware workaround is necessary that watches via a spare SDRAM chip select the successful initialization of the SDRAM controller (chip select toggling for refresh). Otherwise a 2nd reset is necessary which will always result in a proper setup and the system will start. This workaround is implemented in the A9M9360_2 module.

8. Appendix

8.1. Pinning Module

The pinning for all currently planned and realised modules are defined in the file “Arm9 Module Pinning Table.XLS”.

8.2. Pinning Description Module

A detailed pin description is available as “Pin_Description_A9M9360_X.pdf” or “*.doc”.

8.3. Pinning Module on A9MVali Validation Board

This pinning is included in the specification of the validation board: “A9MVali_X.doc” or “*.pdf”. Important: If possible, avoid usage of A9M9360 modules on A9MVALI_X boards due to missing power sequencing on this base board. Module powerup and powerdown may be disturbed by backfeeding 3.3V signals from base board. Prefered base board is A9M9750DEV_1.

8.4. Pinning Module on Development Board

This pinning is included in the specification of the Development board: “Spec_Devkit_A9M9750_A9M9360_X.doc” or “*.pdf”.

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Module CC9P9360_2

[1] Erste Fußnote

Users Manual

17. January 2006

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Table of Contents:

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Date	Version	Responsible	Description
2004/07/28	0.1	Dieter Fögele	Initial Version, preliminary for proposal

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