

PowerBrick™ 5.0

User's Manual
Edition 2.0



3 Generation Intel® i7 Industrial Computer



Acura Embedded Systems Inc.

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1.0 INTRODUCTION

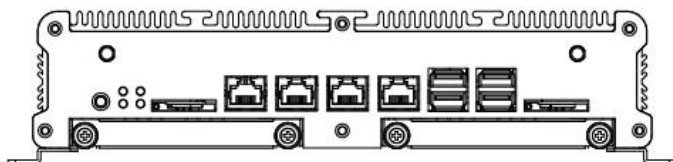
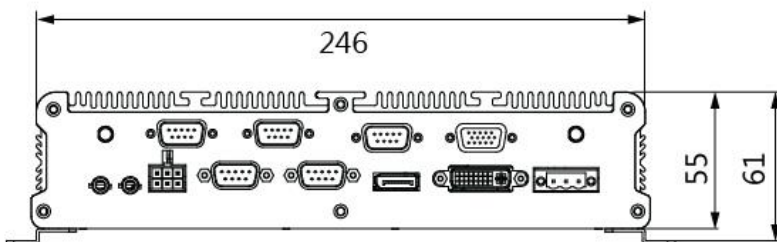
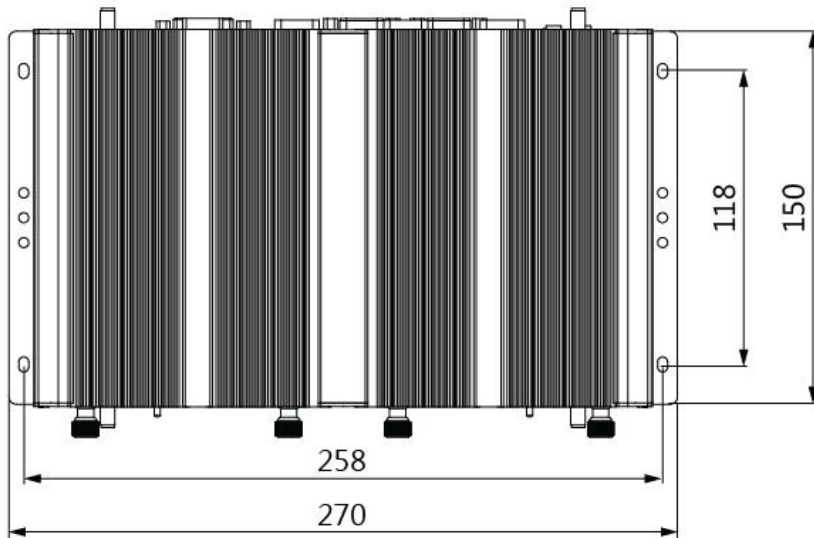
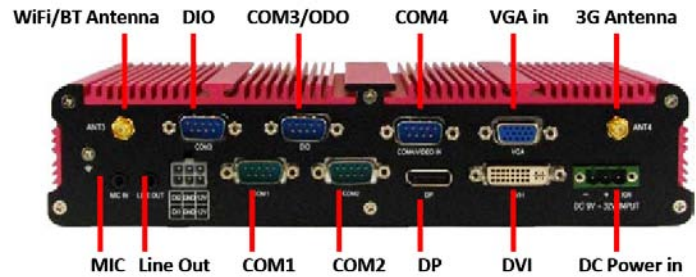
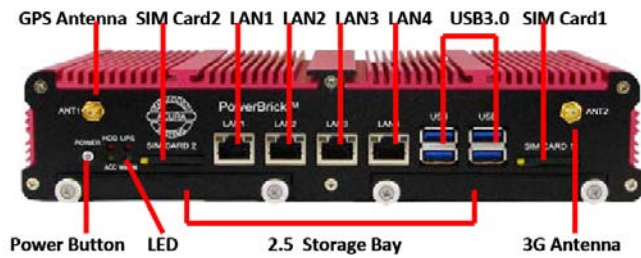
1.1 Specification



System	
CPU	Intel Gen 3 Core i7-3217UE 1.7GHz
Memory	1 x DDR3 1066/1333/1600 MHz SO-DIMM up to 8 GB
Chipset	QM77
LAN Chipset	Intel I210-AT Gb/s Ethernet Controllers Onboard Support PXE and WOL
Audio	Realtek ALC662 HD Codec onboard
Watchdog	Watchdog Timer Support, Offer 1 – 255 Step
Power Requirement	
Power Input	9V-32V DC Power input
Power Protection	Automatics Recovery Short Circuit Protection
Power Management	Vehicle Power Ignition for Variety Vehicle
Power Off Control	Power off Delay Time Setting by Software
Battery	Internal Battery Kit for 10 Mins Operating (Optional)
Storage	
Type	2 x 2.5" Drive Bay for SATA Type HDD / SSD, Support RAID 0, 1 1 x SATA DOM

Graphics	
Graphics	Intel® HD Graphics 4000 DirectX Video Acceleration (DXVA) for Accelerating Video Processing - Full AVC/VC1/MPEG2 HW Decode Supports DirectX 11/10.1/10/9 and OpenGL 3.0
Resolution	Up to 1920 x 1200
Qualification	
Certifications	CE, FCC Class A, E-mark
I/O	
Serial Port	4 x RS-232 (COM1,2 with RS-422/485, RS-485 Support Auto Direction Control)
USB Port	4 x USB 2.0 Ports on Front I/O
LAN	2 x RJ45 Ports for GbE
Video Port	1 x DVI-I, 1 x VGA and 1 x Display Port Output
DIO Port	4 in and 4 out with Relay 12V / 80mA
Audio	1 x Line-out and 1 x MIC-in
SIM Card Socket	2 x SIM Card sockets supported onboard with eject
Environment	
Operating Temp.	-40°C ~ 70°C (Default CPU 17Watt)
Storage Temp.	-40 ~ 80°C
Relative Humidity	0% RH– 95% RH
Vibration (random)	2.5g@5~500 Hz with SSD
Vibration Operating	MIL-STD-810F, Method 514.5, Category 20, Ground Vehicle-Highway
Truck Storage	MIL-STD-810F, Method 514.5, Category 24, Integrity Test
Shock	Operating: MIL-STD-810F, Method 516.5, Procedure I, Trucks and semi-trailers=40G (11ms) with SSD
Crash Hazard	MIL-STD-810F, Method 516.5, Procedure V, Ground equipment=100
Mechanical	
Construction	Aluminum alloy
Mounting	Supports both of wall-mount/VESA-mount
Weight	1.780 kg (bare-bone)
Dimensions	250 x 150 x 55 mm

1.2 System



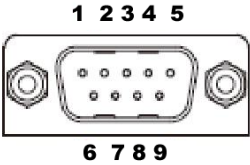
2.0 CONNECTOR SPECIFICATION

2.1 VGA Connector

VGA	Pin	Signal	Pin	Signal
	1	RED	2	GREEN
	3	BLUE	4	NC
	5	CER_DET	6	GND
	7	GND	8	GND
	9	+5V	10	GND
	11	NC	12	DAC_SDA
	13	HSYNC	14	VSYNC
	15	DAC_SCL	16	NC

2.2 GPIO Connector

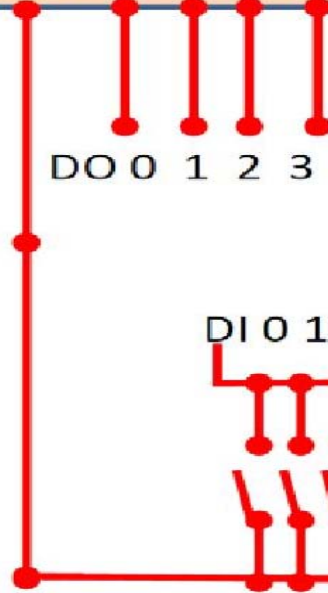
GPIO Pin	Pin	Signal	Pin	Signal
	1	GPI0	2	GPI1
Definition				
	3	GPI2	4	GPI3
	5	GPO0	6	GPO1
	7	GPO2	8	GPO3
	9	GND		



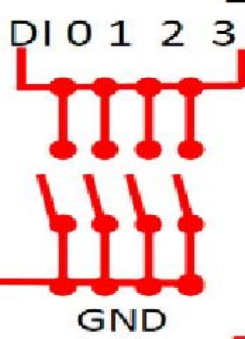
Switch

GND + + + +

DO 0 1 2 3



DI 0 1 2 3



Digital Output

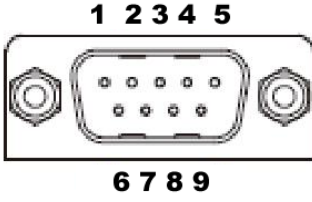
- High : 12V / 80mA
- Low : 0V
- Push Pull High to 12V

Digital Input Source :

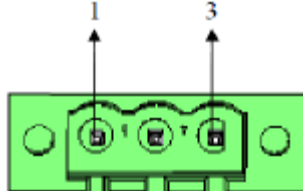
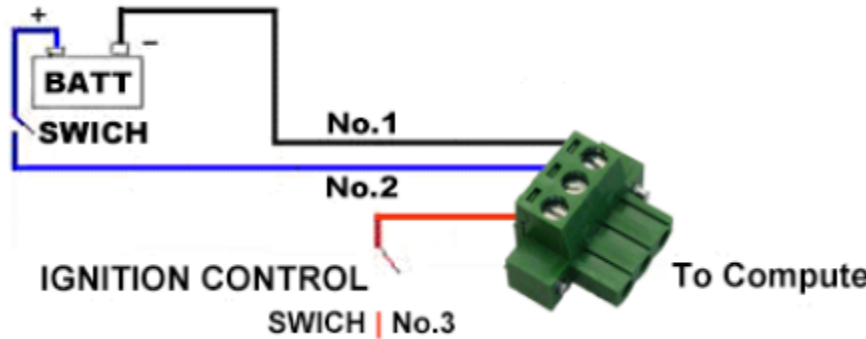
- Input Low = <3.0V
- Input High= >3.3V
- Max. Input = <32V

DI Dry Contact Wiring

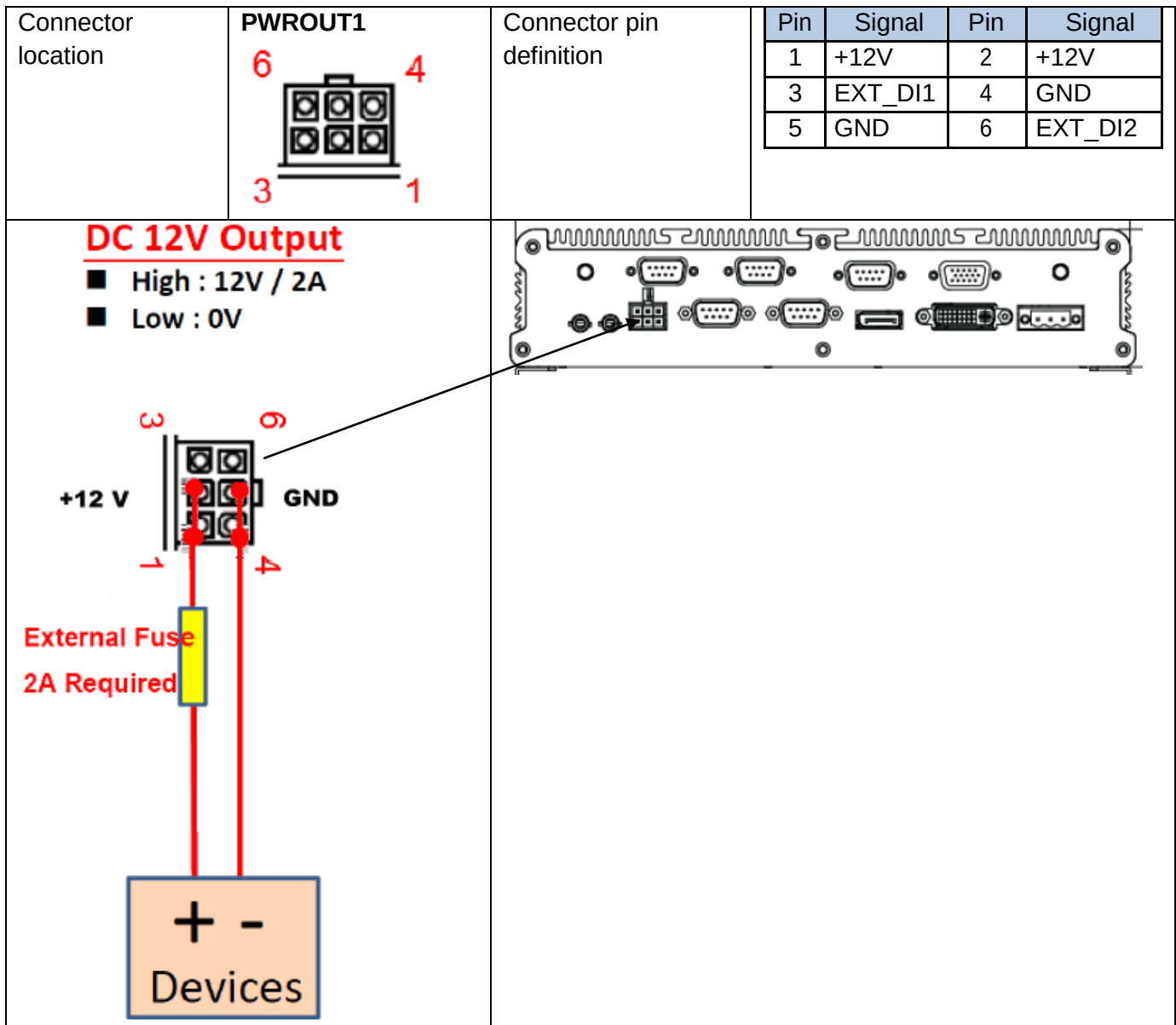
2.3 COM Port Connector (COM)

Connector pin COM 1,2,3,4 	Pin	Signal	Pin	Signal
		COM1,2,3,4_DCD (COM1,2_RS- 485_TXD-/RXD-)		COM1,2,3,4_RXD (Com1,2_RS- 485_TXD+/RXD+)
	1		2	
	3	COM_TXD	4	COM_DTR
	5	GND	6	COM_DSR
	7	COM_RTS	8	COM_CTS
	9	COM_RI#		

2.4 Power Input Connector

PWRIN1 	Connector definition	Pin	Signal
		1	GND
Power Brick 5.0 Power Wiring Diagram		2	VIN (9-32V)
		3	IGNITION

2.5 ATX 6PIN Connector (POWER OUT)



3.0 IGNITION POWER MANAGEMENT

Startup/shutdown conditions from the IGNITION signal:

- IGNITION startup signal must be valid during 3 sec. (anti noise protection).
- IGNITION shutdown – IGNITION signal must be inactive during 3 Sec, then PIC controller initiate Power Button signal (**OS must be set to shutdown from the Power Button**). It generate Main Button shutdown event and then goes to complete power off.

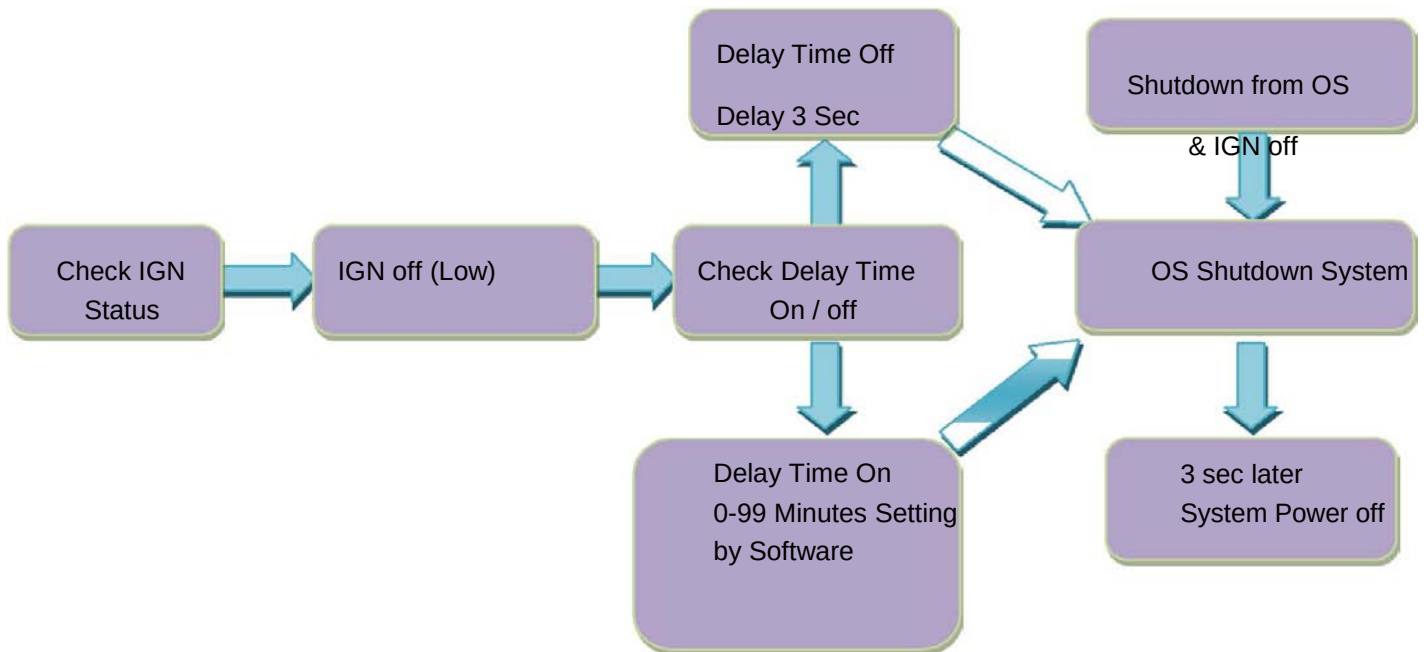
Typically the system can start only from IGNITION signal, because startup PIC controller is disconnected from the power source.

The system can be switched off from:

- Power IGNITION OFF signal.
- ACPI OS shutdown
- Power Button – generate ACPI event (OS dependent).



Power Ignition Startup Procedure



Power Ignition Shutdown Procedure

Power Management

- Power-off delay time is selectable by Software to disable and enable in 0-99 minutes
- Ignition On/Off status detectable by SW
- If the ignition is off and the system is still on after 3 Sec, PowerBrick 5.0 will shut down automatically.
- If the ignition is turned on again and the power-off delay is in progress, PowerBrick 5.0 will cancel the delay function and will continue to operate normally.
- If the ignition is turned on again and the power-off delay ended, PowerBrick 5.0 will shut down completely will power-on again automatically.

4.0 GPIO & Delay Time Setting

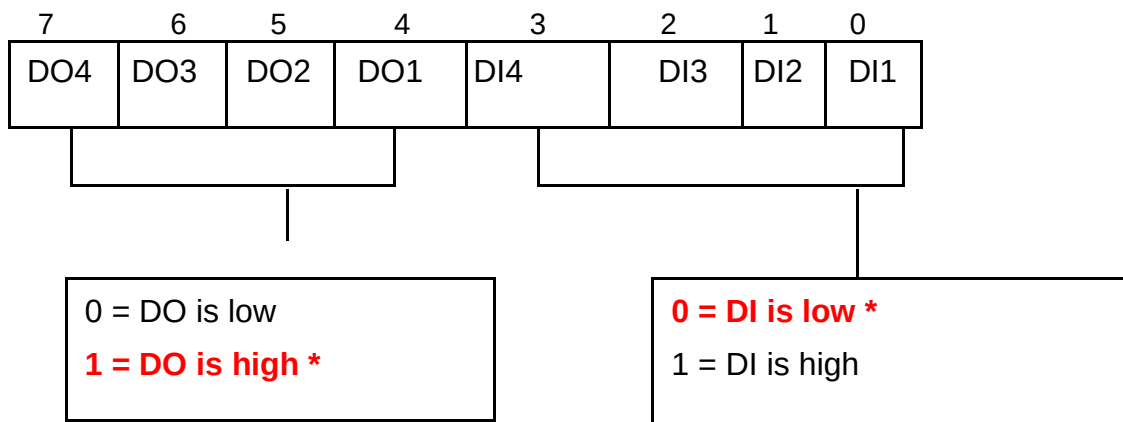
4.1 GPIO and Ignition Control Register

The General Purpose I/O is an interface available on some devices. These can read digital signals from other parts of a circuit, or output to control other devices. At GPIO control register, the GPI is use to receive data, the GPO is set data to send.

I/O port: **0xA35 (base address)** for Control Register (Read 0xA2h / Write 0xA1h)
0xA36 (base address) for Control Data Value

Debug Command Line

- O A35 A1
- O A36 0F // Set Bit 4-7 to Low



PIO5 Output Enable Register – Index A0h

Bit	Name	R/W	Default	Description
7	GPIO57_OE	R/W	0	0 : GPIO57 is input 1 : GPIO57 is output
6	GPIO56_OE	R/W	0	0 : GPIO56 is input 1 : GPIO56 is output
5	GPIO55_OE	R/W	0	0 : GPIO55 is input 1 : GPIO55 is output
4	GPIO54_OE	R/W	0	0 : GPIO54 is input 1 : GPIO54 is output
3	GPIO53_OE	R/W	0	0 : GPIO53 is input 1 : GPIO53 is output
2	GPIO52_OE	R/W	0	0 : GPIO52 is input 1 : GPIO52 is output
1	GPIO51_OE	R/W	0	0 : GPIO51 is input 1 : GPIO51 is output
0	GPIO50_OE	R/W	0	0 : GPIO50 is input

GPIO5 Output Data Register – Index A1h

Bit	Name	R/W	Default	Description
7	GPIO57_DATA	R/W	1	GPIO57 output data in output mode.
6	GPIO56_DATA	R/W	1	GPIO56 output data in output mode.
5	GPIO55_DATA	R/W	1	GPIO55 output data in output mode.
4	GPIO54_DATA	R/W	1	GPIO54 output data in output mode.
3	GPIO53_DATA	R/W	1	GPIO53 output data in output mode.
2	GPIO52_DATA	R/W	1	GPIO52 output data in output mode.
1	GPIO51_DATA	R/W	1	GPIO51 output data in output mode.
0	GPIO50_DATA	R/W	1	GPIO50 output data in output mode.

GPIO5 Pin Status Register – Index A2h

Bit	Name	R/W	Default	Description
7	GPIO57_ST	R	1	GPIO57 pin status.
6	GPIO56_ST	R	1	GPIO56 pin status.
5	GPIO55_ST	R	1	GPIO55 pin status.
4	GPIO54_ST	R	1	GPIO54 pin status.
3	GPIO53_ST	R	1	GPIO53 pin status.
2	GPIO52_ST	R	1	GPIO52 pin status.
1	GPIO51_ST	R	1	GPIO51 pin status.
0	GPIO50_ST	R	1	GPIO50 pin status.

GPIO5 Drive Enable Register – Index A3h

Bit	Name	R/W	Default	Description
7	GPIO57_DRV_ENST	R/W	0	GPIO57 Drive Enable : GPIO57 is open drain. : GPIO57 is push pull.
6	GPIO56_DRV_ENST	R/W	0	GPIO57 Drive Enable : GPIO56 is open drain. : GPIO56 is push pull.
5	GPIO55_DRV_ENST	R/W	0	GPIO57 Drive Enable : GPIO55 is open drain. : GPIO55 is push pull.
4	GPIO54_DRV_ENST	R/W	0	GPIO57 Drive Enable : GPIO54 is open drain. : GPIO54 is push pull.
3	GPIO53_DRV_ENST	R/W	0	GPIO57 Drive Enable : GPIO53 is open drain. : GPIO53 is push pull.
2	GPIO52_DRV_ENST	R/W	0	GPIO57 Drive Enable : GPIO52 is open drain. : GPIO52 is push pull.
1	GPIO51_DRV_ENST	R/W	0	GPIO57 Drive Enable : GPIO51 is open drain. : GPIO51 is push pull.
0	GPIO50_DRV_ENST	R/W	0	GPIO57 Drive Enable : GPIO50 is open drain. : GPIO50 is push pull.

I/O port: I/O port: **0xA35 (base address)** for Control Register (Read 0xF2h bit 3)
0xA36 (base address) for Control Data Value

7	6	5	4	3	2	1	0
X	X	X	X	Ignition Status	X	X	X

0 = Ignition off
1 = Ignition on

Debug Command Line

- O A35 F2
- I A36 // Check Bit 3 Status

4.2 WDT Setting

I/O port: **A10 (base address) + 05h and 06h** 1 Watchdog Timer Control Register

The Watchdog Timer Control Register controls the WDT working mode. Write the value to the WDT Configuration Port. The following table describes the Control Register bit definition:

7	6	5	4	3	2	1	0
0	0	1	1	Timer Unit	0	Select output pulse width of RSTOUT#	

0 = 1 sec
1 = 60 sec *

00 = 1 ms
01 = 25 ms
10 = 125 ms*
11 = 5 sec

Debug Command Line

- O A16 05
- O A15 32 // 5 sec // 3A ☐ 5 minutes

Watchdog Timer Function

Watch dog timer is provided for system controlling. If time-out can trigger one signal to high/low level/pulse, the signal is depend on register setting.

The time unit has two ways from 1sec or 60sec. In pulse mode, there are four pulse widths can be selected (1ms/25ms/125ms/5sec). Others, please refer the device register description as below.

Watchdog Timer Configuration Register 1- base address +05h

Bit	Name	R/W	Default	Description
7	Reserved	R	0	Reserved
6	WDTMOUT_ST	R/W	0	If watchdog timeout event occurs, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
5	WD_EN	R/W	0	If this bit is set to 1, the counting of watchdog time is enabled.
4	WD_PULSE	R/W	0	Select output mode (0:level, 1:pulse) of RSTOUT# by setting this bit.
3	WD_UNIT	R/W	0	Select time unit (0:1sec, 1:60sec) of watchdog timer by setting this bit.
2	WD_HACTIVE	R/W	0	Select output polarity of RETOUT# (1:high active, 0:low active) by setting the bit.
1-0	WD_PSWIDTH	R/W	0	Select output pulse width of RSTOUT# 0:1 ms 1:25 ms 2:125 ms 3:5 sec

Watchdog Timer Configuration Register 2- base address +06h

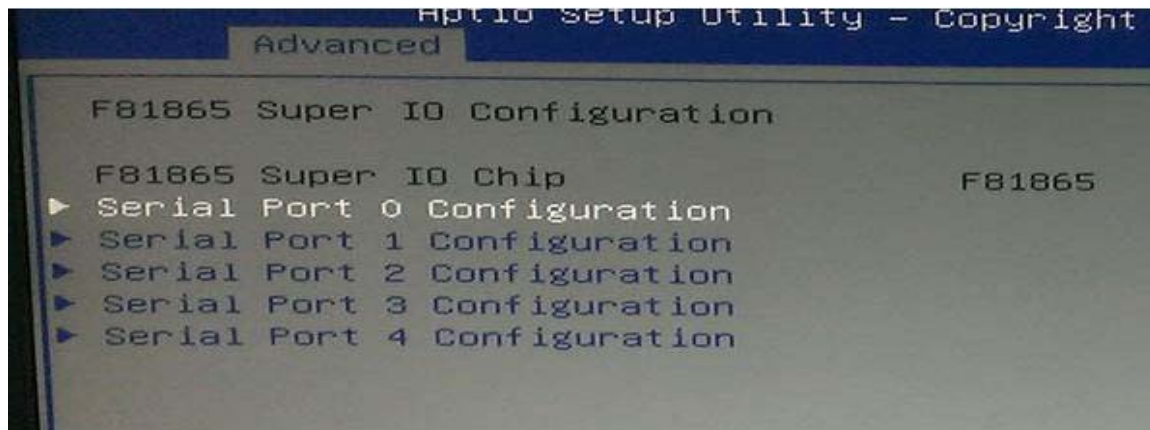
Bit	Name	R/W	Default	Description
7-0	WD_TIME	R/W	0	Time of watchdog timer

Watchdog PME Control Register - base address + 0Ah

Bit	Name	R/W	Default	Description
7	WDT_PME	R	--	The PME Status This bit will set when WDT_PME_EN is set and the watchdog timer is 1 unit before time out (of time out)
6	WDT_PME_EN	R/W	0	0 : Disable Watchdog PME. 1 : Enable Watchdog PME
5-1	Reserved	--	--	Reserved
0	WDOUT_EN	R/W	0	0 : disable Watchdog time out output via WDTRST# 1 : enable Watchdog time out output via WDTRST#

5.0 BIOS Setting

Super IO Configuration



Select Serial Port Mode





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Technical Support:

For **technical support** contact your **Salesperson**

support@acuraembedded.com

Mailing address:

Acura Embedded Systems Inc.

Unit #1, 7711-128th Street, Surrey, BC V3W 4E6, CANADA

Ph: (604) 502-9666 Fax: (604) 502-9668

Toll Free 1-866-502-9666